CMOS PLL SYNTHESIZERS

Analysis and Design

Keliu Shu
Edgar Sánchez-Sinencio

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Contents

List of Acronyms and Symbols

AAC	Automatic Amplitude Control
BPF	Band-Pass Filter
CCO	Current-Controlled Oscillator
CDR	Clock and Data Recovery
CMOS	Complementary Metal Oxide Semiconductor
CP	Charge-Pump
DAC	Digital-to-Analog Converter
DAS	Direct Analog Synthesizer
DDS	Direct Digital Synthesizer
DFDD	Digital Frequency Difference Detector
DLL	Delay-Locked Loop
DPA	Digital Phase Accumulator
DUT	Device Under Test
FDC	Frequency-to-Digital Converter
FF	Flip-Flop
FHSS	Frequency-Hopping Spread Spectrum
FM	Frequency Modulation
FN	Fractional-N
FS	Frequency Synthesizer
GSM	Global System for Mobile communications
IC	Integrated Circuit
ILFD	Injection-Locked Frequency Divider
ISF	Impulse Sensitivity Factor
ISM	Industrial Scientific Medicine
LF	Loop Filter
LO	Local Oscillator
LTI	Linear Time-Invariant
LSB	Least-Significant-Bit

MASH	Multi-stage noise Shaping
NAND	Negative AND logic
NCO	Numerically Controlled Oscillator
NMOS	N-channel Metal Oxide Semiconductor
NOR	Negative OR logic
OPA	Operational Amplifier
OSR	Over Sampling Ratio
OTA	Operational Transconductance Amplifier
PD	Phase Detector
PFD	Phase-Frequency Detector
PGS	Patterned Ground Shield
PLL	Phase-Locked Loop
PMOS	P-channel Metal Oxide Semiconductor
PSD	Power Spectral Density
RF	Radio Frequency
rms	Root-Mean-Square
SC	Switched Capacitor
SCL	Source-Coupled Logic
SDM	Sigma-Delta Modulator
SNR	Signal-to-Noise Ratio
SSB	Single-Sideband
TSPC	True-Single-Phase-Clock
VCO	Voltage-Controlled Oscillator
XOR	Exclusive OR logic

ω	angular frequency in *rad/s*
ω_{-3dB}	PLL $-3dB$ loop bandwidth
ω_c	PLL loop (unity-gain / crossover) bandwidth
ω_{c1}	1^{st} corner frequency of capacitance multiplier impedance
ω_{c2}	2^{nd} corner frequency of capacitance multiplier impedance
ω_{c3}	3^{rd} corner frequency of capacitance multiplier impedance
ω_n	natural frequency
ω_{p1}	1^{st} pole-frequency of loop filter transimpedance
ω_{p2}	2^{nd} pole-frequency of loop filter transimpedance
ω_{p3}	3^{rd} pole-frequency of loop filter transimpedance
ω_{ref}	PLL reference angular frequency (at PFD)
ω_z	zero-frequency of loop filter
$\omega_{1/f}$	corner angular frequency of $1/f$ noise
$\Delta\omega_{1/f^3}$	corner angular frequency of oscillator $1/f^3$ phase noise

$\Delta\omega$	angular frequency offset from carrier
$\Delta\omega_H$	PLL hold range
$\Delta\omega_L$	PLL lock range
$\Delta\omega_P$	PLL pull-in range
$\Delta\omega_{PO}$	PLL pull-out range
ϕ	phase
ϕ_m	phase margin
$\Delta\phi$	amplitude of phase modulation
$\Delta\phi_{rms}$	PLL output *rms* phase noise
θ	phase
θ_e	phase error at PFD inputs
θ_{in}	input phase (noise)
θ_{out}	output phase (noise)
θ_{vco}	VCO phase noise
φ	random phase variation
ζ	damping factor
ε	normalized settling frequency error of PLL
£	phase noise in *dBc/Hz*
σ_c	*rms* of cycle jitter
σ_{cc}	*rms* of cycle-to-cycle jitter
τ	time
δ	impulse function (Dirac delta function)
δ_T	periodic impulse function with period T
Γ	ISF function
B	current ratio
C_1	1st capacitance of passive loop filter
C_2	2nd capacitance of passive loop filter
C_3	3rd capacitance of passive loop filter
C_{p1}	1st parasitic capacitance of capacitance multiplier
C_{p2}	2nd parasitic capacitance of capacitance multiplier
f	frequency in *Hz*
f_0	carrier frequency
f_c	PLL loop (unity-gain / crossover) bandwidth
f_{div}	loop divider output frequency
f_m	modulation frequency

f_{ref}	PLL reference frequency (at PFD)
f_{vco}	VCO frequency
f_{RF}	RF frequency (of mixer)
f_{LO}	local oscillator frequency
Δf	offset frequency from the carrier
$\Delta f_{1/f^3}$	corner frequency of oscillator $1/f^3$ phase noise
F	active device noise factor
g	conductance, transconductance
G	conductance, transconductance
h	transfer function
H	transfer function
H_{cl}	PLL closed-loop input-to-output phase (noise) transfer function
H_e	PLL input phase (noise) to PFD phase error transfer function
H_{ol}	PLL open-loop input-to-output phase (noise) transfer function
H_{V_C}	PLL input phase to LF output voltage transfer function
i	current
i_{cp}	charge-pump current noise
I	current in-phase signal
I_c	control current of CCO
I_{cp}	charge-pump current
I_{cpi}	charge-pump current of integration path
I_{cpp}	charge-pump current of proportional path
I_{dn}	charge-pump current for discharging the load capacitor
I_p	output current of LF's proportional path
I_{up}	charge-pump current for charging the load capacitor
I_z	output current of LF's integration path
j	integer number
k	binary integer input of DPA or digital SDM Boltzmann constant
K	PLL loop gain
K_{pd}	PFD and charge-pump gain in *A/rad*
K_{vco}	VCO conversion gain in *rad/s/V*
K_{cco}	CCO conversion gain in *rad/s/A*

L	integer number (order of SDM) inductance
m	integer number
M	modulus of DPA or digital SDM
n	integer number
n_Q	output integer of digital SDM
N	number (nominal) frequency divide ratio of loop divider
N_B	integer part of fractional-N divide ratio
P	prescaler divide ratio power
P_r	PLL reference spur level in *dBc*
q	charge
Q	quadrature signal quality factor quantization noise
Q_L	loaded quality factor
R	resistance auto-correlation function
R_1	1st resistance of passive loop filter
R_2	2nd resistance of passive loop filter
R_φ	auto-correlation function of random phase φ
S	power spectrum
S_φ	power spectral density of random phase variation
S_V	power spectral density of signal $V(t)$
t	time
t_{on}	charge-pump turn-on time in locked state
T	time temperature
T_L	PLL lock-in time (rough estimation)
T_P	PLL pull-in time
T_{ref}	period of PLL reference signal
ΔT_{abs}	absolute jitter
ΔT_{cn}	cycle-to-average jitter
ΔT_{ccn}	cycle-to-cycle jitter
u	unit step function
v	voltage
V	voltage

V_c	VCO control voltage, LF output voltage
V_p	output voltage of LF's proportional path
V_z	output voltage of LF's integration path
v_{lf}	loop filter output voltage noise
y	admittance
z	impedance
Z	impedance, transimpedance
Z_{lf}	loop filter transimpedance

Preface

Thanks to the advance of semiconductor and communication technology, the wireless communication market has been booming in the last two decades. It evolved from simple pagers to emerging third-generation (3G) cellular phones. In the meanwhile, broadband communication market has also gained a rapid growth. As the market always demands high-performance and low-cost products, circuit designers are seeking high-integration communication devices in cheap CMOS technology.

The phase-locked loop frequency synthesizer is a critical component in communication devices. It works as a local oscillator for frequency translation and channel selection in wireless transceivers and broadband cable tuners. It also plays an important role as the clock synthesizer for data converters in the analog-and-digital signal interface.

This book covers the design and analysis of PLL synthesizers. It includes both fundamentals and a review of the state-of-the-art techniques. The transient analysis of the third-order charge-pump PLL reveals its locking behavior accurately. The behavioral-level simulation of PLL further clarifies its stability limit. Design examples are given to clearly illustrate the design procedure of PLL synthesizers. A complete derivation of reference spurs in the charge-pump PLL is also presented in this book.

The in-depth investigation of the digital $\Sigma\Delta$ modulator for fractional-N synthesizers provides insightful design guidelines for this important block. As the prescaler is often the speed bottleneck of high-frequency PLL synthesizers, it is covered in a single chapter in this book. An inherently glitch-free low-power phase-switching prescaler was developed. The timing analysis of the switching control loop gives good understanding for a sound design. As spurs generated from the delay mismatch in the phase-switching

prescaler might be a concern, it is mathematically examined. Another single chapter in this book is devoted to the loop filter, which is an integration bottleneck in narrow-band PLL because its big capacitor takes a large chip area. A simple area-efficient on-chip loop filter solution was proposed. It is based on a capacitance multiplier, which is of very low complexity and power consumption. Detailed analysis and design of this novel loop filter was addressed.

As this book features a complete coverage of PLL synthesizer design and analysis techniques, the authors hope it will be a good manual for both acdemia researchers and industry designers in the PLL area.

Chapter 1

INTRODUCTION

1.1 Motivation

In the last decade, the rapid growth of wireless applications has led to an increasing demand of fully integrated, low-cost, low-power, and high-performance transceivers. The applications of wireless communication devices include pagers, cordless phones, cellular phones, global positioning systems (GPS), and wireless local area networks (WLAN), transmitting either voice or data. A standard specifies how devices talk to each other. Numerous standards emerged and are optimized for certain applications. For voice, examples include AMPS, NMT, TACS, D-AMPS, DECT, GSM, DCS, PCS, PDC, TDMA, CDMA, etc. It has evolved from analog to digital, from the 1G (first generation) to the current existing 2.5G, such as GPRS and EDGE. Devices in the 3G wireless standards, which include UMTS (WCDMA), CDMA2000 and TD-SCDMA, are also emerging in some areas of the world. For data, there are 802.11a/b/g WLAN, HiperLAN, Bluetooth, HomeRF, and so on. More recently, a significant interest has grown in the ultra wideband communications [1], [2]. Figure 1-1 briefly illustrates the frequency band of some wireless communication standards.

The recent boom of the mobile telecommunication market has driven worldwide electronic and communication companies to produce small-size, low-power, high-performance and certainly low-cost mobile terminals. The current wireless transceivers involve SiGe bipolar, GaAs and CMOS integrated RF front end and some discrete high-performance components. From a cost of technology point of view, the standard CMOS process is the cheapest one. With a constantly decreasing feature size, it is possible to

design the radio frequency integrated circuits (RFIC) in CMOS technology. A single-chip transceiver with a minimum number of off-chip components is preferred to reduce the cost and size of wireless devices, like cellular phones [3]-[7].

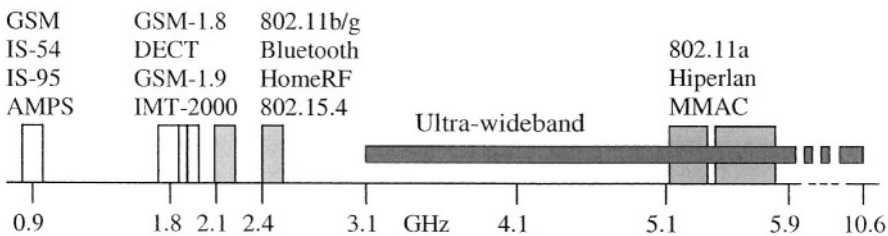

Figure 1-1. Frequency band of wireless communication standards

There are still many difficulties, however, in the process of integration of RF front-end due to the lack of high-quality components on chip. This book focuses on the design of the frequency synthesizer, one of the key building blocks of the RF front-end in CMOS technology. The frequency synthesizer is used as a local oscillator for frequency translation and channel selection in the RF front-end of wireless transceivers. It is a critical component in terms of the performance and cost of a wireless transceiver [8].

1.2 Summary of book

This book focuses on both fundamentals and advanced design techniques of PLL-based frequency synthesizers. A $2.4GHz$ fully integrated $\Sigma\Delta$ fractional-N frequency synthesizer prototype is implemented in $0.35\mu m$ CMOS technology. Efforts have been put on the prescaler and loop filter, which are the speed and integration bottlenecks, respectively.

A low-power and robust prescaler using an enhanced phase-switching architecture was proposed [9]-[12]. The new architecture is based on generating eight 45°-spaced phases and judiciously arranging the phase-switching sequence to yield an inherently glitch-free phase-switching operation.

In the existing phase-switching architecture [13], the switching is made between four 90°-spaced phases generated by cascading two stages of ÷2 dividers. The prescaler's input frequency is divided by a factor of 4 before switching occurs. Since the frequency of the four signals to be switched by the multiplexer (MUX) is still high, the MUX is usually implemented with current-steering logic and voltage-level amplification is needed. In the proposed enhanced phase-switching architecture, one additional ÷2 divider is used to generate eight 45°-spaced signals. Since the input-signal frequency is

reduced by half, from 1/4 to 1/8 of the prescaler's input frequency, the MUX can be implemented with standard digital cells to save power consumption and the robustness of phase-switching operation is improved.

Furthermore, the main problem associated with the existing phase-switching architecture is the potential glitches if the switching occurs in the incorrect timing window. Thus, various significant efforts have been made in the literature to yield a glitch-free phase-switching prescaler [13]-[16]. However, all these glitch-removing schemes are not robust and often cost considerable power and area, or even sacrifice the prescaler's maximum operating speed. But in the proposed enhanced phase-switching architecture, an inherently glitch-free phase-switching operation is obtained by means of reversing the switching sequence. Thus, no retiming or synchronization circuit is needed for the switching control and the robustness of the switching operation is guaranteed.

To provide a further insight into the switching operation in the proposed phase-switching architecture, a detailed delay timing analysis of the switching control loop is given. By calculating the delay budget in the loop, we conclude that usually the first ÷2 divider is the only speed constraint of this enhanced phase-switching architecture.

The loop filter is a barrier in fully integrating a narrow-band PLL because of its large integrating capacitor. To make the loop capacitance of a narrow-band PLL as small as possible while keeping the same loop bandwidth, designers increase the loop resistance and reduce the charge-pump current. However, there are practical limitations for both the loop resistance and the charge-pump current. Thermal noise in the large resistor modulates the control voltage and generates phase noise in the VCO, and the charge-pump noise increases while the current decreases.

The dual-path topology has been a popular solution to this problem [17]-[22]. It equivalently scales down the largest integrating and zero-generating capacitance by the scaling factor of the dual charge-pump currents. Besides the increased noise and power due to active devices, the charge-pump of the integration path is still working with a very small current and contributes significant noise. Also, the delay mismatch of the dual charge-pumps may change the loop parameters. Furthermore, at least for the implementations in [18]-[20] and [22], the voltage decay of the low-pass path causes undesirable ripples on the VCO control voltage.

To overcome the constraints of the dual-path topology, a novel loop filter solution is proposed [10]-[12]. A capacitance multiplier [23] is used to reduce the capacitance by a large factor and make it easily integratable within a small chip area.

Besides contributions on the prescaler and loop filter, a comparative study of digital $\Sigma\Delta$ modulator for fractional-N PLL synthesizers is made [24] to investigate the optimal design of the digital $\Sigma\Delta$ modulator. A third-order

three-level digital ΣΔ modulator is employed to reduce the instantaneous phase error at the PFD. The folding of the ΣΔ-shaped phase noise is minimized by reducing nonlinearities of the PFD and charge pump [10]-[12], [24].

Furthermore, the derivation of the settling time of the third-order PLL, the derivation of spurs due to delay/phase mismatches in the phase-switching prescaler, a complete analysis of the reference spur in the charge-pump PLL, and the behavioral-level verification of the PLL stability limit are all presented in this book.

A prototype chip of the ΣΔ PLL synthesizer was fabricated in TSMC $0.35\mu m$, 4-metal 2-poly (4M2P) CMOS process through MOSIS. The die size is $2mm \times 2mm$. It includes a fully integrated ΣΔ fractional-N frequency synthesizer and some standalone building blocks for testing. The PLL takes an active area of $0.85mm^2$, of which the digital ΣΔ modulator occupies $0.5mm^2$. With a power supply of 1.5-V for VCO and prescaler, and 2.0-V for other blocks, the whole PLL system consumes 16mW, of which the VCO consumes $9mW$. With the reference frequency of $50MHz$, the measured phase noise is $-128dBc/Hz$ at $10MHz$ offset and the reference spur is $-57dBc$.

The proposed prescaler only takes an area of $0.04mm^2$. With a 1.5-V power supply, it works well within the PLL's tuning range of 2.23~2.45GHz and consumes $3mW$. The proposed loop filter occupies $0.05mm^2$ and its power consumption ($0.2mW$) and noise are negligible compared with the whole PLL.

1.3 Book organization

In Chapter 2, the fundamentals of the frequency synthesizer including its features, applications, implementations, and key parameters (jitter and phase noise) are reviewed. Various synthesizer architectures and their pros and cons are discussed.

In Chapter 3, the analysis of the PLL-based frequency synthesizer is covered. It includes the continuous-time linear analysis, discrete-time analysis, stability concerns, operation modes, and fast-locking techniques, etc. An integer-N PLL frequency synthesizer design example is given to illustrate the design procedure.

Chapter 4 concentrates on analysis and design of the ΣΔ fractional-N PLL frequency synthesizer. ΣΔ noise mapping methods are reviewed. A comparative study of digital ΣΔ modulators for fractional-N synthesis is conducted to provide detailed design considerations and guidelines for this block. Other applications of ΣΔ-PLL are surveyed and a design example of the ΣΔ-PLL is also included.

Chapter 5 is devoted to the design of the prescaler. The existing design techniques are overviewed. An enhanced, inherently glitch-free phase-switching prescaler is presented. Its architecture and circuit implementation are addressed in great detail. The delay budget of the switching control loop is analyzed to demonstrate its robustness. Furthermore, spurs generated from delay/phase mismatches are derived.

Chapter 6 covers the design of the on-chip loop filter. Current design approaches are addressed. An area- and power-efficient implementation of the on-chip loop filter based on a simple capacitance multiplier is proposed. The detailed design, analysis, and simulation results are provided.

In Chapter 7, the implementation of other building blocks of a $\Sigma\Delta$ PLL prototype is elaborated. It includes the phase-frequency detector (PFD), the charge-pump (CP), the *LC*-tuned voltage-controlled oscillator (VCO), the digital $\Sigma\Delta$ modulator (SDM), and the programmable pulse-swallowing frequency divider. A complete reference spur analysis is also made.

Chapter 8 gives the experimental results of the prototype frequency synthesizer and some standalone building blocks, such as the novel prescaler and loop filter. Measurement results verified the feasibility and robustness of the phase-switching prescaler and the practicality of the loop capacitance multiplier.

Conclusions of this book are drawn in Chapter 9.

Finally, the Matlab simulation of the charge-pump PLL is given in the Appendix. The PLL stability limit is verified through behavioral-level simulations.

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Chapter 2

FREQUENCY SYNTHESIZER FOR WIRELESS APPLICATIONS

This chapter describes some fundamentals of frequency synthesizers. It covers the definition, specification, implementation and application of frequency synthesizers. The timing jitter and phase noise, the architecture of frequency synthesizers, and the frequency synthesizer's specification for wireless applications are overviewed.

2.1 Definition and characteristics

A frequency synthesizer (FS) is a device that generates one or many frequencies from one or a few frequency sources. Fig. 2-1 illustrates the input and outputs of an FS.

The output of an FS is characterized by its frequency tuning range, frequency resolution, and frequency purity. Ideally, the synthesized signal is a pure sinusoidal waveform. But in reality, its power spectrum features a peak at the desired frequency and tails on both sides. The uncertainty of a synthesizer's output is characterized by its phase noise (or spur level) at a certain frequency offset from the desired carrier frequency in unit of *dBc/Hz* (or *dBc).* The unit of *dBc/Hz* measures the ratio (in *dB)* of the phase noise power in 1Hz bandwidth at a certain frequency offset to the carrier power. Similarly, the unit of *dBc* measures the ratio (in *dB)* of the spur (also known as tone) power at a certain frequency offset to the carrier power. More discussions on the phase noise are covered in the next section. The phase noise requirement of a frequency synthesizer depends on applications. For

example, the most stringent phase noise requirement in the frequency synthesizer for 900*MHz* GSM receivers is –121*dBc/Hz* at 600*kHz* frequency offset.

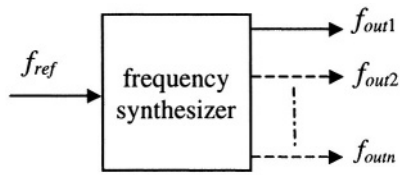

Figure 2-1. Frequency synthesizer

2.2 Phase noise and timing jitter

2.2.1 Phase noise and spurious tone

The ideal synthesizer produces a pure sinusoidal waveform

$$V(t) = V_0 \sin(2\pi f_0 t) \tag{2.1}$$

When amplitude and phase fluctuations are accounted, the waveform becomes

$$V(t) = (V_0 + v(t))\sin(2\pi f_0 t + \phi(t)) \tag{2.2}$$

where *v(t)* and $\phi(t)$ represent amplitude and phase fluctuations, respectively. Because amplitude fluctuations can be removed or greatly alleviated by a limiter or an automatic amplitude control (AAC) circuit [1], [2], we concentrate on phase fluctuation effects in a frequency synthesizer output only.

We consider two types of phase fluctuations, the periodic variation and the random variation [3]. In mathematical form, $\phi(t)$ can be written as:

$$\phi(t) = \Delta\phi \sin(2\pi f_m t) + \varphi(t) \tag{2.3}$$

The first term represents the periodic phase variation, and it produces a spurious tone at an offset frequency of f_m from the carrier frequency f_0. The magnitude of the spurious tone can be derived as follows:

$$\begin{aligned} V(t) &= V_0 \sin(2\pi f_0 t + \Delta\phi \sin(2\pi f_m t)) \\ &= V_0 [\sin(2\pi f_0 t)\cos(\Delta\phi \sin(2\pi f_m t)) + \cos(2\pi f_0 t)\sin(\Delta\phi \sin(2\pi f_m t))] \end{aligned} \tag{2.4}$$

For very small phase modulation, i.e., $\Delta\phi << \pi / 2$

$$\cos(\Delta\phi \sin(2\pi f_m t)) \approx 1 \tag{2.5}$$

$$\sin(\Delta\phi \sin(2\pi f_m t)) \approx \Delta\phi \sin(2\pi f_m t) \tag{2.6}$$

Then (2.4) yields:

$$\begin{aligned} V(t) &\approx V_0 [\sin(2\pi f_0 t) + \Delta\phi \cos(2\pi f_0 t)\sin(2\pi f_m t)] \\ &= V_0 \left[\sin(2\pi f_0 t) - \frac{\Delta\phi}{2} \sin(2\pi (f_0 - f_m)) + \frac{\Delta\phi}{2} \sin(2\pi (f_0 + f_m)) \right] \end{aligned} \tag{2.7}$$

From (2.7) we observe that the two spurious tones at $f_0 + f_m$ and $f_0 - f_m$ are both $-20\log(\Delta\phi / 2)\, dB$ below the carrier.

The second term of $\phi(t)$ in (2.3) represents the random phase variation and it produces phase noise. The spectral density of phase variation is

$$S_\varphi(f) = \int_{-\infty}^{+\infty} R_\varphi(\tau) e^{-j2\pi f\tau} d\tau \tag{2.8}$$

where $R_\varphi(\tau)$ is the auto-correlation of the random phase variation $\varphi(t)$:

$$R_\varphi(\tau) = E[\varphi(t)\varphi(t-\tau)] \tag{2.9}$$

When the root-mean-square *(rms)* value of $\varphi(t)$ is much smaller than 1 *radian,* the power spectrum density of *V(t)* can be approximated as

$$S_V(f) = \frac{V_0^2}{2} [\delta(f - f_0) + S_\varphi(f - f_0)] \tag{2.10}$$

It consists of the carrier power at f_0 and the phase noise power at frequency offsets from f_0. The single-sideband (SSB) phase noise is defined as the ratio of noise power in $1Hz$ bandwidth at a certain frequency offset ($\Delta f = f - f_0$) from the carrier to the carrier power. The unit is *dBc/Hz*.

$$\pounds(\Delta f) = 10\log\frac{P_{noise}(1\text{Hz at } f)}{P_{carrier}} = 10\log\frac{S_{\varphi}(\Delta f)}{2} \quad dBc/Hz \qquad (2.11)$$

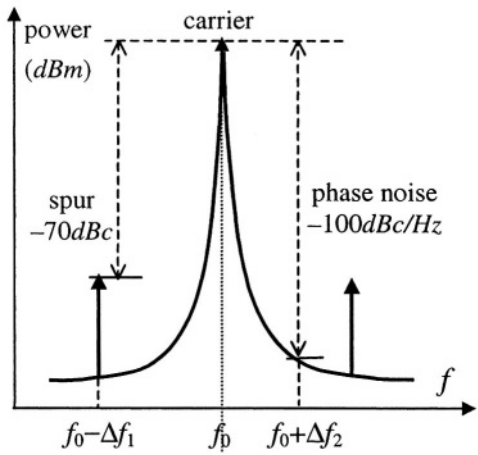

Figure 2-2. Phase noise and spur

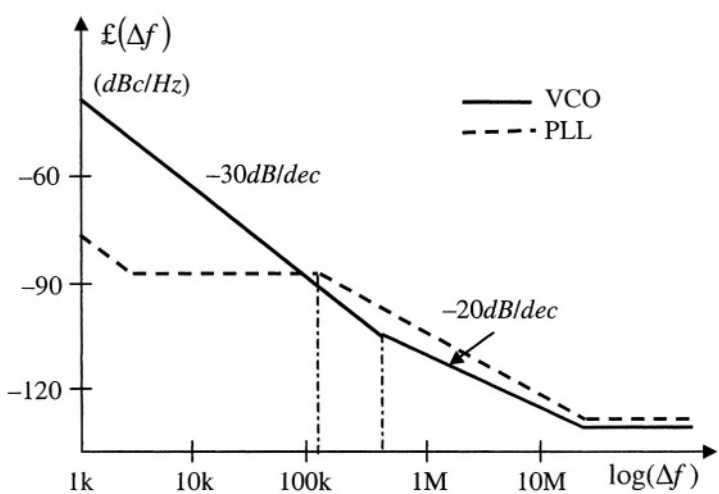

Figure 2-3. Phase noise of VCO and PLL

Therefore, the phase noise *dBc/Hz* value observed on the spectrum analyzer is numerically equivalent to $10\log[S_{\varphi}(\Delta f)] - 3$.

Fig. 2-2 illustrates the phase noise and spurs of a synthesized signal of frequency f_0. The spur level at an offset frequency of $-\Delta f_1$ is *–70dBc,* and the phase noise at an offset frequency of Δf_2 is –100*dBc/Hz.*

Figure 2-3 conceptually shows the phase noise of a voltage-controlled oscillator (VCO) and a phase-locked loop (PLL). The phase noise of a VCO demonstrates regions with slopes of –30*dBc/dec* and –20*dBc/dec,* and a flat region. A PLL's in-band phase noise is usually as flat as its reference input, while its out-band phase noise follows that of the VCO.

2.2.2 Timing jitter

Analogous to phase noise, which is the frequency domain characterization of the uncertainty of a synthesizer or oscillator's output, the timing jitter is the characterization in time domain. Denote the period of the nth cycle of an oscillator's output as T_n, and its average period is $\overline{T}$. There are basically three-types of jitters:

(1) The cycle jitter, or cycle-to-average jitter, is defined as:

$$\Delta T_{cn} = T_n - \overline{T} \tag{2.12}$$

The *rms* (root-mean-square) of the cycle jitter is

$$\sigma_c = \lim_{N\to\infty} \sqrt{\frac{1}{N}\sum_{n=1}^{N}\left(\Delta T_{cn}\right)^2} \tag{2.13}$$

(2) The cycle-to-cycle jitter is expressed as:

$$\Delta T_{ccn} = T_{n+1} - T_n \tag{2.14}$$

The *rms* value of the cycle-to-cycle jitter is:

$$\sigma_{cc} = \lim_{N\to\infty} \sqrt{\frac{1}{N}\sum_{n=1}^{N}\left(\Delta T_{ccn}\right)^2} \tag{2.15}$$

(3) The absolute jitter, also known as long-term jitter or accumulated jitter, of the N th cycle can be described as:

$$\Delta T_{abs}(N) = \sum_{n=1}^{N}\left(T_n - \overline{T}\right) = \sum_{n=1}^{N}\left(\Delta T_{cn}\right) \tag{2.16}$$

For white noise sources, an oscillator's absolute jitter with a measurement interval Δt is related to σ_{cc} as [4]:

$$\Delta T_{abs}(\Delta t) = \sqrt{\frac{f_0}{2}} \cdot \sigma_{cc}\sqrt{\Delta t} \tag{2.17}$$

For white noise sources, two successive oscillator periods are uncorrelated, thus

$$\sigma_{cc} = \sqrt{2}\sigma_c \tag{2.18}$$

Figure 2-4 conceptually illustrates the absolute timing jitter *(rms* value σ_τ) of a VCO and a PLL as a function of the time interval (τ). Since the absolute jitter accumulates continuously, it increases with the measurement interval. Uncorrelated noises (e.g. white noise) add in a mean-square sense and hence result in a square root dependence on the time interval [5], while correlated noises (e.g. $1/f$ noise) add directly resulting in a region with a slope of one on log-log axes [6]. The absolute jitter of a PLL has a flat region due to in-band VCO noise suppression [5], [7]. If the PLL bandwidth is small, a unit-slope region exists between the half-slope and the flat regions [8].

Weigandt *et al.* derived the relationship between the single-side-band phase noise and the *rms* of cycle jitter (σ_c) as follows [9]:

$$\pounds(\Delta f) = \frac{f_0^3\sigma_c^2}{(\Delta f)^2} \tag{2.19}$$

Herzel and Razavi derived the following formula [4]

$$\pounds(\Delta\omega) = \frac{\left(\omega_0^3/4\pi\right)\sigma_{cc}^2}{(\Delta\omega)^2 + \left(\omega_0^3/8\pi\right)^2\sigma_{cc}^4} \tag{2.20}$$

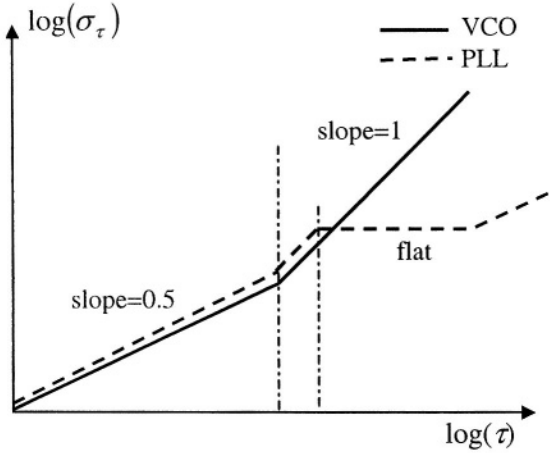

Figure 2-4. Timing jitter of VCO and PLL

Note that, (2.20) reduces to (2.19) when $|\omega - \omega_0| >> (\omega_0^3 / 8\pi)\sigma_{cc}^2$.

Demir *et al.* derived the self-referred jitter and phase noise of oscillators with white noise as in (2.21) and (2.22), respectively [10].

$$\pounds(\Delta f) = \frac{f_0^2 c}{(\Delta f)^2 + \pi^2 f_0^4 c^2} \tag{2.21}$$

$$\sigma^2(\Delta t) = \Delta t \cdot c \tag{2.22}$$

The constant c in both equations describes jitter and spectral spreading in a noisy oscillator. In fact, the self-referred jitter $\sigma(\Delta t)$ is another definition of the absolute jitter $\Delta T_{abs}(\Delta t)$ in a less strict but more practical sense. Comparing (2.22) and (2.17), we obtain the expression of the constant c as

$$c = \frac{f_0}{2}\sigma_{cc}^2 \tag{2.23}$$

Substituting (2.23) into (2.21), we can verify the equivalence between (2.21) and (2.20).

The above derivations are only valid for white noise. A more general relationship between jitter and phase noise for any wide sense stationary noise derived in [11] is

$$\sigma^2(\Delta t) = \frac{T_0^2}{(2\pi)^2} E\left\{[\phi(t+\Delta t) - \phi(t)]^2\right\} = \frac{2}{\pi^2 f_0^2} \int_0^\infty \pounds(\Delta f) \sin^2(\pi \Delta f \cdot \Delta t) d\Delta f \tag{2.24}$$

An experimental verification of the relationship between phase noise and timing jitter was made in [12]. More discussions on the relationship between phase noise and timing jitter can be found in [13]-[17].

2.3 Implementations of frequency synthesizer

As shown in Table 2-1, frequency synthesizers can be grouped into four classes: direct analog synthesizer (DAS), direct digital synthesizer (DDS), phase-locked loop frequency synthesizer (PLL-FS), and delay-locked loop frequency synthesizer (DLL-FS). A brief discussion of these classes follows.

Table 2-1. Classification of frequency synthesizers

frequency synthesis	direct synthesis	DAS	multiplier + mixer + divider	
		DDS	NCO+DAC	
	indirect synthesis	PLL-based	integer-N	
			factional-N	phase estimation by DAC
				random jittering
				noise shaping by ΣΔ
				phase interpolation
				pulse generation
		DLL-based	frequency multiplied by the number of equal-spacing phases	

2.3.1 Direct analog frequency synthesizer

The direct analog synthesizer is realized by cascading stages of frequency multipliers, dividers, mixers and band-pass filters (BPF) [18], [19]. A large number of separate frequencies or channels can be generated from a single reference. The desired output signals can be rapidly switched between any set of frequencies. Many manufactures of commercial test equipment use mix-and-divide design for their synthesizers and they report that excellent phase noise and spurious performance can be achieved with adequate physical/electrical isolation between the stages. The major drawback of this scheme is the sheer size and power that would be required to make a synthesizer of this type for certain applications. Figure 2-5 shows an example of DAS [20]. The output frequency is

$$f_{out} = f_1 + 0.1f_2 + 0.01f_3 \tag{2.25}$$

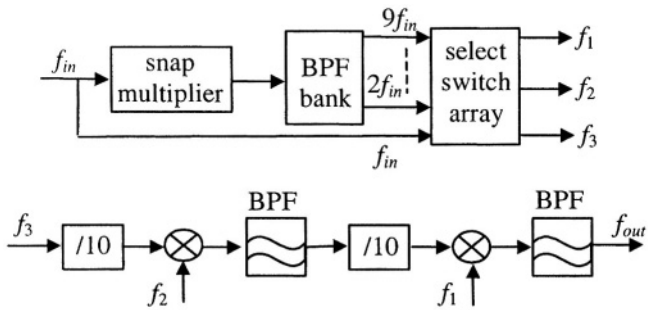

Figure 2-5. An example of DAS

Since f_1, f_2 and f_3 can be 0 to 9 times of the input frequency, f_{in}, f_{out} can be varied from 0 to $1.99f_{in}$ with a resolution of $0.01f_{in}$.

2.3.2 Direct digital frequency synthesizer

The direct digital synthesizer is a technology that has been around since the early 1970's. The two major components of the DDS are a numerically controlled oscillator (NCO) and a digital-to-analog converter (DAC). The NCO consists of an adder-register pair (also known as phase accumulator) and a ramp-to-sinewave lookup ROM. Figure 2-6 shows the block diagram of a DDS. The output of the DDS is related to the phase accumulator input by the following equation:

$$f_{out} \approx \frac{K}{2^N} \cdot f_{clock} \tag{2.26}$$

where N is the bit-length of the accumulator and K is the accumulator's input [21]. The DDS typically provides a low frequency output with extremely high resolution and excellent frequency switching speed. The resolution of DDS can be made arbitrarily small with very little additional circuitry or added circuit complexity. Due to sampling theory a DDS can only generate frequencies up to a maximum of half of the clock rate of the digital circuitry. The primary disadvantage of most direct digital synthesizers is the typically high spurious content caused by quantization and linearity limitation of the DAC. A rough rule of thumb is that the spurious level generated by DAC quantization equals $6dB$ times the number of input bits (e.g. an 8-bit DAC would have quantization spurious $48dB$ lower than the carrier). However, as

the DAC is clocked at frequencies approaching its upper limit, spurs caused by non-linearities in the DAC become dominant [22]. Recent advances in the design of DDS can be found in [23]-[33].

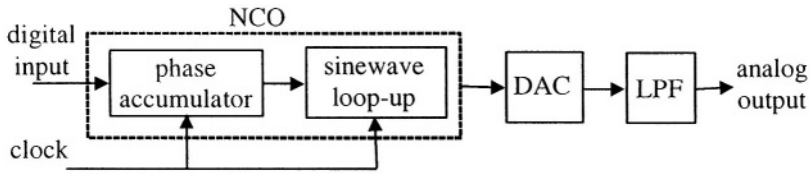

Figure 2-6. Block diagram of DDS

2.3.3 PLL-based frequency synthesizer

A. Integer-N PLL-FS

Figure 2-7 depicts a PLL-based integer-N frequency synthesizer. It consists of a phase-frequency detector (PFD), a charge-pump (CP), a loop filter, a voltage-controlled oscillator (VCO), and a programmable frequency divider. For an integer-N frequency synthesizer, the output frequency is a multiple of the reference frequency:

$$f_{out} = N \cdot f_{ref} \tag{2.27}$$

where N, the loop frequency divide ratio, is an integer. Whereby the frequency resolution of the integer-N frequency synthesizer is equal to the reference frequency f_{ref}.

Due to the limitation of frequency resolution equal to the reference frequency, for narrow-band applications, the reference of the synthesizer is very small and the frequency divide ratio is very large. For example, for 900*MHz* GSM and 2.4*GHz* Bluetooth, the reference frequencies are 200*kHz* and 1*MHz,* respectively, and the corresponding divide ratios are around 4500 and 2400, respectively. The conventional integer-N PLL with low reference frequency has several disadvantages. First, the lock time is long due to its narrow loop-bandwidth. Second, the reference spur and its harmonics are located at low offset frequencies. Third, the large divide ratio (N) increases the in-band phase noise associated with the reference signal, the PFD, the charge-pump and the frequency divider by 20log*(N) dB*. Finally, with a small loop-bandwidth, the phase noise of the VCO will not be sufficiently suppressed at low offset frequencies.

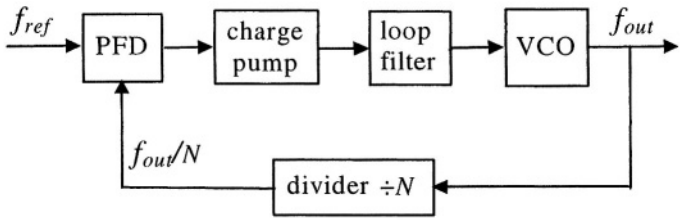

Figure 2-7. Integer-N PLL-FS

B. Fractional-N PLL-FS

Fractional-N frequency synthesizers (FN-FS) are used to overcome the above-mentioned disadvantages of integer-N synthesizers. In the fractional-N synthesizer, the frequency divide ratio can be a fractional number, so a large reference can be used to achieve a small frequency resolution. However, the principle disadvantage of the fractional-N frequency synthesis is the unwanted low-frequency spurs due to the fixed pattern of the dual-modulus (or multi-modulus) divider. Since these spurs can reside inside the loop bandwidth, fractional-N synthesizers are not practical unless fixed in-band spurs are suppressed to a negligible level. Five main spur reduction techniques are addressed in the literature. Their prominent features and problems are summarized in Table 2-2 [34], [35].

Table 2-2. Spur reduction techniques for fractional-N synthesis

technique	feature	problem
DAC phase estimation	cancel spur by DAC	analog mismatch
random jittering	randomize divide ratio	frequency jitter
ΣΔ noise shaping	modulate divide ratio	quantization noise
phase interpolation	inherent fractional divider or multiphase VCO	interpolation jitter
pulse generation	insert pulses	interpolation jitter

The block diagram of a fractional-N synthesizer using DAC phase estimation is illustrated in Fig. 2-8. An accumulator is used to control the instantaneous divide ratio. If the overflow *(OVFL)* is 1, the divide ratio is $N_B + 1$, otherwise the divide ratio is N_B. Since the average of the overflow is k/M, where k is the input to the accumulator and M is the modulus of the accumulator. Thus, the fractional divide ratio is $N = N_B + k/M$ and the frequency resolution is f_{ref}/M. Since the instantaneous divide ratio varies periodically, strong fractional spurs would appear at the synthesizer output. The DAC is used to convert the instantaneous phase error, which is proportional to the residue of the accumulator, into an equivalent amount of

charge-pump current to compensate the phase error. The accuracy of this compensation is limited by the DAC and is sensitive to process variations.

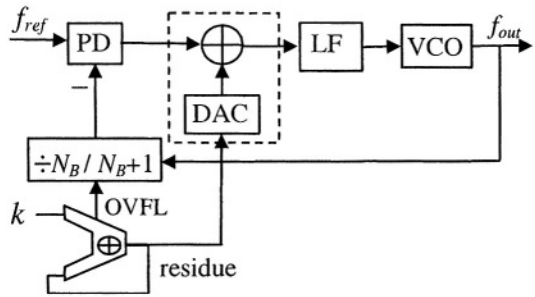

Figure 2-8. FN-FS using DAC phase interpolation

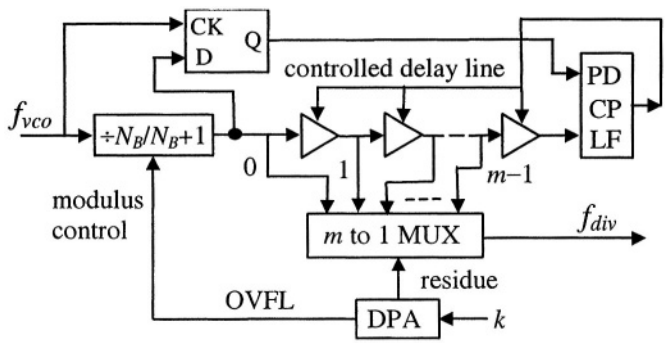

Figure 2-9. An inherent fractional divider for FN-FS

Figure 2-9 shows an inherent fractional divider for fractional-N synthesizer using phase interpolation. An m-stage delay-line is used to produce a total delay of one input VCO signal cycle, $1/f_{vco}$. The modulus of the digital phase accumulator (DPA) is also m. Therefore, the frequency resolution of a fractional-N synthesizer using this fractional divider is f_{ref}/m. Although fractional spurs generated from the mismatches of the delay stages are usually negligible, the number m cannot be made large as f_{vco} goes high. When f_{vco} is very high, a single stage delay would be more than $1/f_{vco}$. Thus, the corresponding fractional divider does not exist at all. Phase interpolation can also be based on a multiphase VCO. Since the phase mismatch of the multi-phase VCO is often a concern, phase calibration is needed to reduce the fractional spurs caused by phase mismatch [36]-[38].

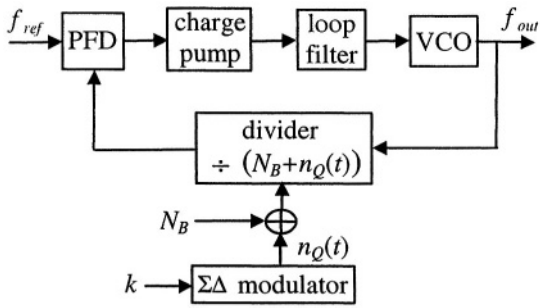

Figure 2-10. ΣΔ fractional-N frequency synthesizer

The phase noise shaping by ΣΔ modulation [39]-[41] is similar to the random jittering method which just randomize the jitter of the divider output. However, it does not have a $1/f^2$ phase noise spectrum due to the noise shaping property of the ΣΔ modulator. As shown in Fig. 2-10, fractional division based on an accumulator is similar in concept to the 1st-order ΣΔ modulator for dc inputs. Since the 2nd order or higher-order ΣΔ modulator does not generate fixed tones for dc inputs, they can more effectively shape the phase noise spectrum than the first-order ΣΔ modulator. The effective over-sampling ratio (OSR) can be defined by the ratio of the reference frequency to the PLL bandwidth. When high-order modulators are used, the PLL needs more poles in the loop filter to suppress the quantization noise at high frequencies.

C. Multi-loop PLL-FS

To avoid the large division ratio in an integer-N PLL synthesizer, one alternative is to use multiple loops to reduce the division ratio. Dual-loop PLL is frequently used to improve the tradeoff among phase noise, channel spacing, reference frequency and the locking speed [42]. Some dual-loop PLL frequency synthesizer architectures are shown in Fig. 2-11. In Fig. 2-11 (a), PLL1 is used to generate reference frequencies for PLL2. In Fig. 2-11 (b) PLL1 output is up-converted by PLL2 and a single-sideband (SSB) mixer. PLL1 generates tunable IF frequencies, while PLL2 generates a fixed RF frequency. In Fig. 2-11 (c) and (d), PLL2 and a SSB down-conversion mixer are used to reduce the divide ratio in PLL1. Recent works used the dual-loop PLL topology shown in Fig. 2-11 (e) for GSM receivers [42]-[44]. The drawback of the dual-loop PLL is that it may require two references, and/or at least one SSB mixer, which might introduce additional phase noise. Moreover, when one PLL is used as a reference for the other, the reference noise is much higher than that of crystal oscillators.

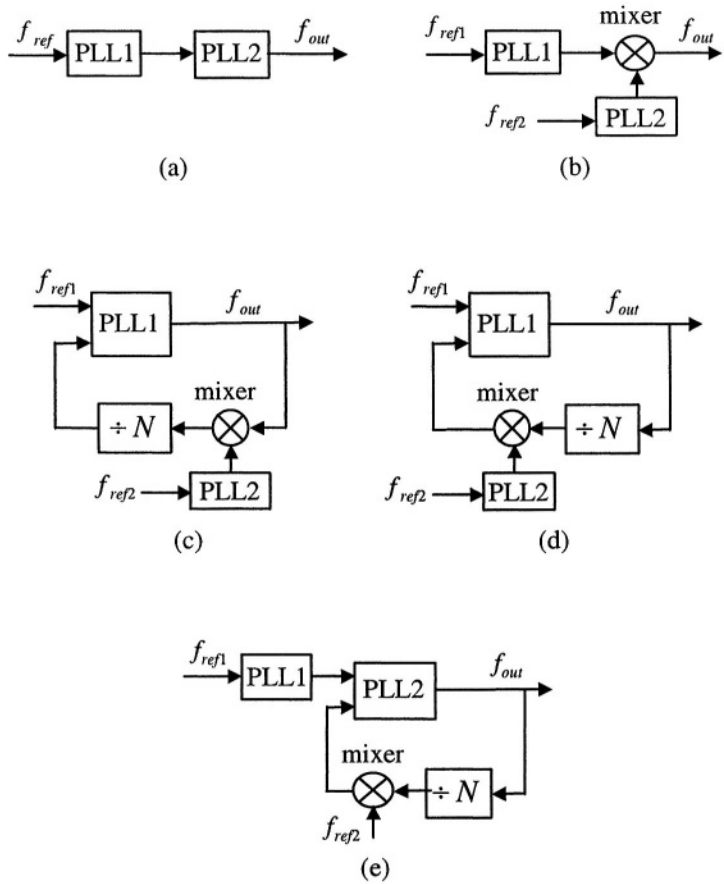

Figure 2-11. Dual-loop PLL frequency synthesizers

2.3.4 DLL-based frequency synthesizer

More recently, designers use DLL as a frequency multiplier or for multi-phase generation [45], [46]. Unlike PLL, there is no phase accumulation in DLL and extremely low phase noise can be achieved. The big drawback of the DLL frequency synthesizer is that it is not programmable. Other problems, such as limited multiplication factor and high power consumption also limit its application. With self-calibration, DLL-based synthesizers can achieve extremely low phase noise. The block diagram of a DLL-FS is shown in Fig. 2-12.

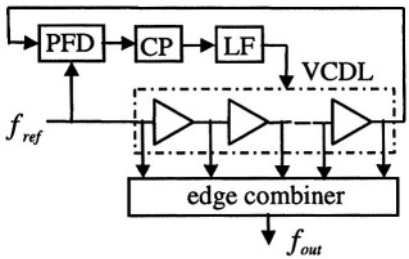

Figure 2-12. Block diagram of DLL-FS

2.3.5 Hybrid frequency synthesizer

Many systems incorporate a mixture or hybrid of these basic approaches in order to take advantage of the benefits of increased speed or improved resolution that one approach may have over another. For example, sometimes a PLL synthesizer may incorporate a DDS in its reference circuitry to increase resolution or to reduce switching time [47]. A major drawback of this approach is that the PLL acts as a multiplier on any phase noise or spurs in its reference and a DDS may have high spurs. The resulting noise at PLL output can seriously degrade system performance.

2.3.6 Summary and comparison of synthesizers

The most widely used frequency synthesizer architecture is based on PLL. It can be easily integrated in current technologies, consumes reasonable power, and meets most of the wireless and wired RF applications. The ΣΔ-PLL brought fractional-N synthesis into maturity and is the dominant fractional-N synthesizer architecture. Direct analog synthesizers may find their applications in microwave, where very high frequencies need to be generated. Direct digital synthesis is used where frequency switching-time is very short, like frequency-hopping spread spectrum (FHSS) systems. A brief comparison of different synthesizer architectures can be found in Table 2-3.

Table 2-3. Comparison of frequency synthesizer architectures

architecture	pros	cons
DAS	fast switching, low noise and spur, good for microwave	big size and power
DDS	fast switching, fine resolution	big power, high spur
integer-N	low power, low noise	slow switching
FN-PLL	relatively faster switching	fractional spur
DLL	very low noise	non-programmable, big power
Hybrid	fast switching, low noise	more complex

2.4 Frequency synthesizer for wireless transceivers

Frequency synthesizers are used as local oscillators (LO) in the wireless transceivers for frequency translation and channel selection. Figure 2-13 shows the popular super-heterodyne receiver architecture [1]. It is a two-step down-conversion architecture. A tunable RF LO is for both the first step frequency conversion and channel selection, and an IF fixed-frequency LO is for further frequency down-conversion to baseband.

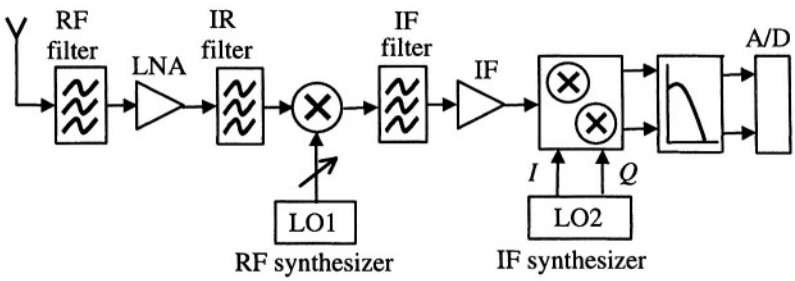

Figure 2-13. Super-heterodyne receiver architecture

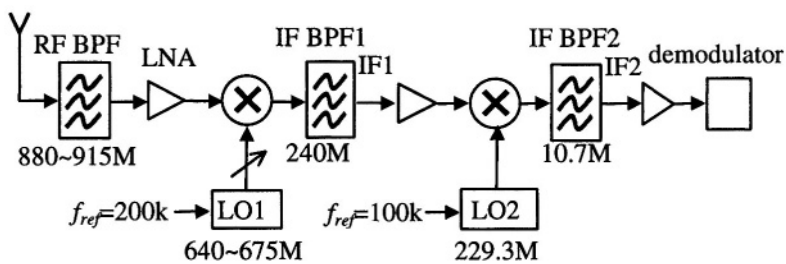

Figure 2-14. GSM base station receiver architecture

Figure 2-14 illustrates a typical low-IF (10.7*MHz*) architecture for a GSM base-station receiver. In this architecture the FS for LO1 is tunable between 640*MHz* to 675*MHz*. For a reference frequency of 200*kHz*, the PLL divide ratio varies between 3200 and 3375.

The signal mixing is actually a frequency convolution shown in Fig. 2-15. Suppose an incoming RF signal f_{RF} has a block signal level of P_{blk} *(dBm)* at an offset frequency of $f_{RF} + \Delta f$, and the phase noise of LO signal f_{LO} at $f_{LO} + \Delta f$ is $\pounds(\Delta f)$ *(dBc/Hz)*. The LO phase noise will down-convert the block signal to the same IF frequency $f_{RF} - f_{LO}$ as the received signal.

And the total noise in a channel of bandwidth f_{BW} *(dBHz)* due to this undesired down-conversion is

$$P_{noise}(\mathrm{dBm}) = P_{blk}(dBm) + f_{BW}(dBHz) + \pounds(\Delta f)(dBc/Hz) + const. \tag{2.28}$$

With the received RF signal power of P_{sig}, the down-converted IF signal power is

$$P_{IFsig}(dBm) = P_{sig}(dBm) + const. \tag{2.29}$$

Thus, the signal-to-noise ratio (SNR) after down-conversion is

$$\begin{aligned} \mathrm{SNR}(dB) &= P_{IFsig}(dBm) - P_{noise}(dBm) \\ &= P_{sig}(dBm) - [P_{blk}(dBm) + \pounds(\Delta f)(dBc/Hz) + f_{BW}(dBHz)] \end{aligned} \tag{2.30}$$

Therefore, for the minimum received signal level of $P_{sig\_\min}$, the maximum block signal level of $P_{blk\_\max}$, and the minimum required SNR, the phase noise requirement $\pounds(\Delta f)$ can be calculated as [49]:

$$\begin{aligned} \pounds(\Delta f)(dBc/Hz) < {} & P_{sig\_\min}(dBm) - P_{blk\_\max}(dBm) \\ & - f_{BW}(dBHz) - \mathrm{SNR}(dB) \end{aligned} \tag{2.31}$$

Similarly, the spur requirement can be calculated as [49]:

$$\mathrm{spur}(\Delta f)(dBc) < P_{sig\_\min}(dBm) - P_{blk\_\max}(dBm) - \mathrm{SNR}(dB) \tag{2.32}$$

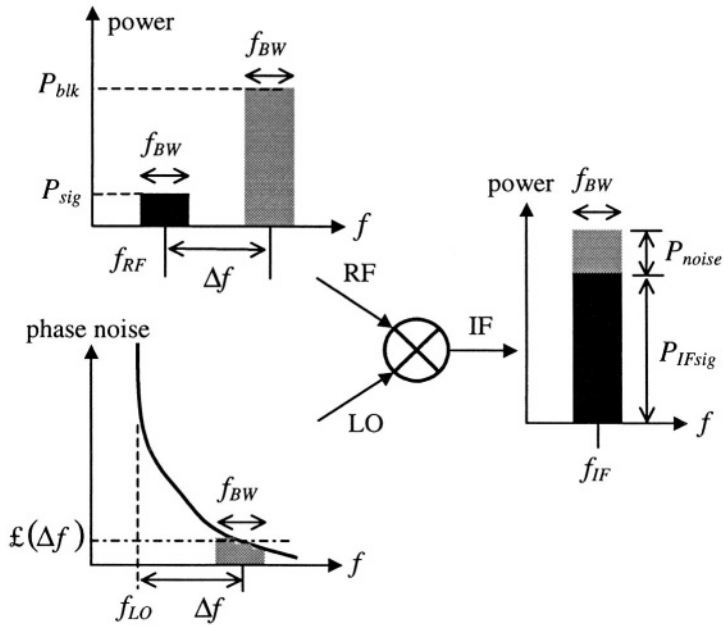

Figure 2-15. Down-conversion with phase noise

For example, in the GSM standard the minimal received signal (sensitivity) is –120*dBm,* the maximum interference power level from 600*kHz* to 1.6*MHz* offset is –43*dBm,* the channel bandwidth is 200*kHz,* and the required SNR is 9*dB*. According to (2.31) and (2.32), in this offset frequency range, the phase noise and spur level should be less than –121*dBc/Hz* and –68*dBc,* respectively. Another example is the derivation of phase noise requirement for Bluetooth receiver at 3*MHz* offset. The out-of-band interference power beyond 3*MHz* offset is –40*dBm,* the channel bandwidth is 1*MHz,* the required SNR is 16*dB,* and the block margin at 3*MHz* is 6*dB*. If we want to achieve an input sensitivity of –82*dBm* (better than the specified –70*dBm),* the phase noise at 3*MHz* should be less that –124*dBc/Hz*.

2.5 Other applications of PLL and frequency synthesizer

The basic PLL is a phase synchronization system through negative feedback shown in Fig. 2-16. The output signal is generated by an analog VCO (voltage-controlled oscillator). The output signal phase θ_{out} is compared with the input signal phase θ_{in} by a PD (phase detector). The phase error is converted into voltage at the PD output. This voltage is filtered by the low-pass loop filter (LF) and used to control the VCO. For example,

if θ_{out} leads θ_{in}, the VCO control voltage reduces. Thus it causes the VCO output frequency and phase (θ_{out}) to reduce.

The basic PLL finds its application in clock de-skew for high-speed digital and mixed-signal IC's, clock synthesis, carrier recovery, clock recovery, modulation and demodulation of frequency or phase [50], and filter tuning [51], [52].

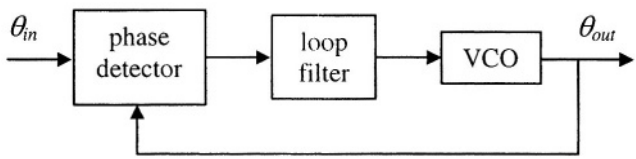

Figure 2-16. Basic PLL diagram

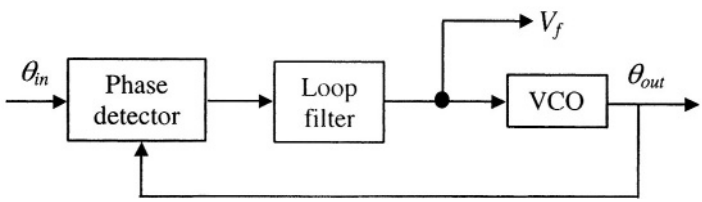

Figure 2-17. PLL for frequency demodulation

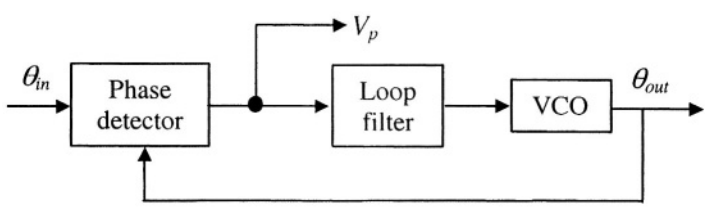

Figure 2-18. PLL for phase demodulation

Figure 2-17 shows the analog frequency demodulation based on the basic PLL. The demodulated signal is actually the VCO control voltage. In frequency demodulation the PLL loop bandwidth is wide, so that the VCO output frequency f_{out} tracks the input frequency f_{in}. Figure 2-18 shows the analog phase demodulation and the demodulated signal is the PD output. In phase demodulation the PLL loop bandwidth is narrow, so that the VCO

output frequency f_{out} tracks the input carrier frequency f_{in} and θ_{out} is the average of θ_{in}.

As shown before (see Figs. 2-7 and 2-10), with a frequency divider added between VCO and PD, the PLL's output frequency can be either an integer or a fractional times of the reference frequency. Like basic PLL's, frequency synthesizers are widely used in electrical engineering. It applications include frequency translation and channel selection in wireless and broadband communications, clock and data recovery in receivers, frequency or phase modulation and demodulation, detection in radar systems, special purpose instruments, and on-chip clock generation and synchronization for digital and mixed-signal IC's, etc.

The clock and data-recovery (CDR) based on PLL is to synchronize the random data to a clock signal generated by a VCO in the PLL. Quadricorrelator shown in Fig. 2-19 is a good technique to implement the reference-less frequency detection [53], [54].

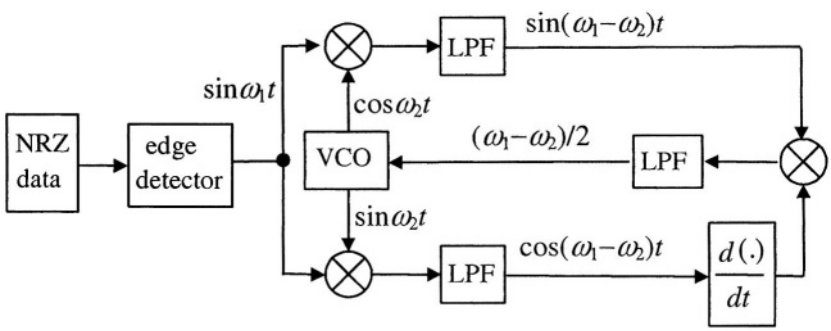

Figure 2-19. Simplified quadricorrelator CDR architecture

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Chapter 3

PLL FREQUENCY SYNTHESIZER

This chapter presents the analysis of PLL-based frequency synthesizers. It includes the continuous-time linear analysis, discrete-time analysis, operation modes, stability, and fast-locking techniques. An integer-N PLL synthesizer design example is given to illustrate the system-level parameter design procedure.

3.1 PLL frequency synthesizer basics

3.1.1 Basic building blocks of charge-pump PLL

The block diagram of the PLL frequency synthesizer is shown in Fig. 3-1. It is based on a charge-pump PLL [1] and consists of a phase-frequency detector (PFD), a charge-pump (CP), a loop filter (LF), a voltage-controlled oscillator (VCO), a dual-modulus prescaler, and a programmable pulse-swallowing divider. The divide ratio of the dual-modulus prescaler is P or $P+1$. M and A are programmable integers [2], [3]. Each divider output cycle consists of $(P+1)\cdot A+P\cdot(M-A)$ VCO cycles. Thus the nominal frequency divide ratio is:

$$N = M \cdot P + A \tag{3.1}$$

The synthesizer output frequency is

$$f_{out} = N \cdot f_{in} = (M \cdot P + A) \cdot f_{in} \tag{3.2}$$

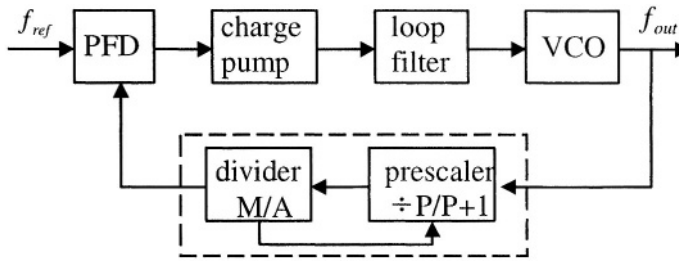


Figure 3-1. Charge-pump PLL frequency synthesizer

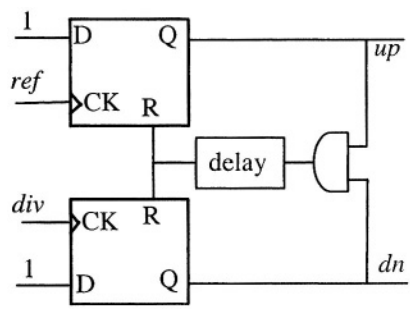


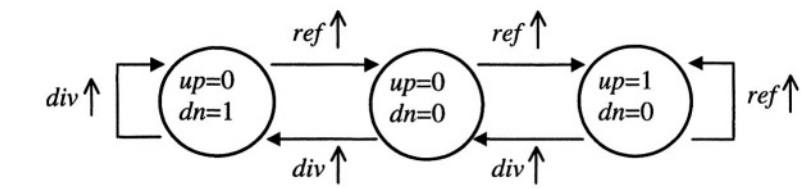
Figure 3-2. Tri-state phase-frequency detector (PFD)

The phase detector (PD) detects the phase difference between the reference signal and the feedback signal from the VCO and frequency divider. Note that, although the PD of a PLL can be an analog multiplier, an exclusive-or (XOR) gate or a J-K flip-flop, etc, for a frequency synthesizer we always use the charge-pump PLL with a tri-state phase-frequency detector (PFD) that also detects frequency errors [3]. Note that, this tri-state PFD is also referred to as "type-4" PD in the literature. The charge-pump PLL has two poles at the origin (type-II) in its open-loop transfer function. It locks faster and its static phase error is zero if mismatches and leakages are negligible. Moreover, its capture range is only limited by its VCO tuning range. A PFD is usually built with memory elements such as flip-flops, latches, etc. Figure 3-2 shows a widely used PFD based on two flip-flops. This edge-triggered tri-state PFD has a linear phase detection range of $\pm 2\pi$ radians. It is duty-cycle insensitive. The delay in the reset path is used to eliminate the dead zone (undetectable phase difference range).

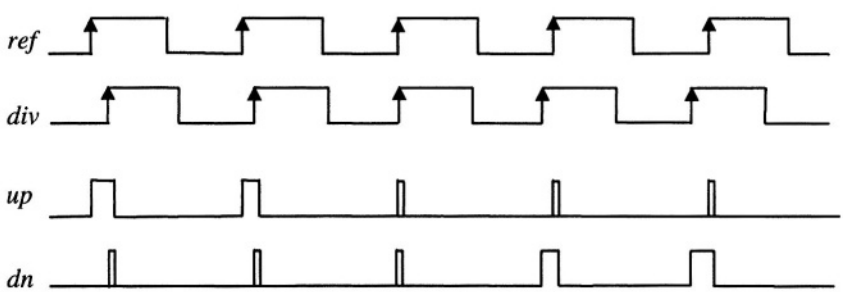
The functionality of the PFD is depicted by its state machine diagram, and waveforms of its inputs and outputs shown in Fig. 3-3. When the rising edge of the reference input *ref* leads that of the divided VCO feedback input *div,* the PFD output *up* is high and the charge pump delivers charges to the

capacitors in the loop filter. Thus, the loop filter output voltage increases and so do the VCO output frequency and phase.

The charge-pump transfers phase difference into current. Fig. 3-4 shows the principles of charge-pump and loop filter. The charge-pump converts the *up* and *dn* pulses into current (I_{cp}) pulses and these current pulses change voltage drop V_c on the loop filter impedance Z_{lf}. V_c is also the VCO control voltage. The dual-modulus prescaler is a high-speed frequency divider to bridge the gap between the low-speed programmable divider and the high frequency (e.g. a few *GHz*) VCO. The quantitative analysis of reference spurs due to charge-pump nonidealities in [4] is reexamined in Chapter 7.



(a) State machine



(b) Signal waveforms

Figure 3-3. Functionality of PFD

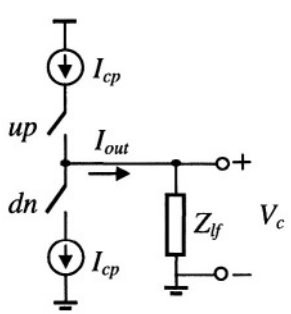


Figure 3-4. Charge-pump and loop filter

The transfer characteristic from the phase error at PFD input to the average charge-pump output current per reference period is shown in Fig. 3-5. It indicates that the PFD has a linear input range of $-2\pi \sim +2\pi$.

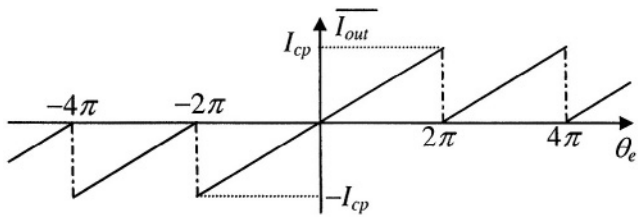


Figure 3-5. PFD/CP transfer function characteristic

3.1.2 Continuous-time linear phase analysis

Since PLL's used for frequency synthesizers are unanimously charge-pump PLL (CP-PLL). Here all analyses are based on this type of PLL. Figure 3-6 gives the linear phase (noise) analysis model of charge-pump PLL. The PFD and charge-pump are combined as one block. Phase noise generated by each building block is referred to its output.

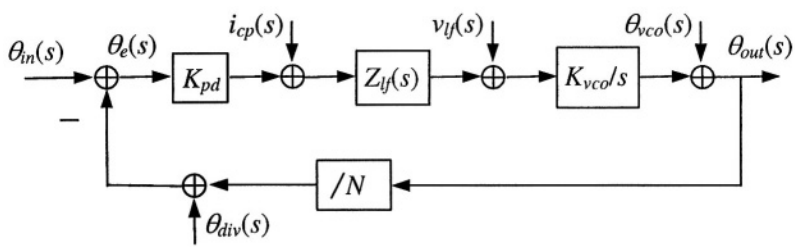


Figure 3-6. PLL linear phase noise model

$\theta_{in}(s)$: input phase noise, mainly from the reference signal
$i_{cp}(s)$: current noise associated with PFD and charge pump
$v_{lf}(s)$: voltage noise generated by loop filter
$\theta_{vco}(s)$: VCO output phase noise
$\theta_{out}(s)$: PLL output phase noise
$\theta_{div}(s)$: phase noise generated by the frequency divider (including prescaler)
K_{pd}: gain of PFD and charge pump, which is $I_{cp}/2\pi$ *(A/rad)*, I_{cp} is the CP current
$Z_{lf}(s)$: transimpedance of low-pass loop filter
K_{vco}: VCO conversion gain *(rad/s/V)*

N: frequency division ratio

Disconnecting the feedback loop between the divider and PFD, we define the PLL open-loop phase transfer function as:

$$H_{ol}(s) = \frac{K_{pd} K_{vco} Z_{lf}(s)}{N \cdot s} \tag{3.3}$$

The transfer function for each noise source to the output phase noise is listed in Table 3-1.

Table 3-1. PLL phase noise transfer function

noise source	Phase transfer function		
input noise	$\theta_{out}(s) / \theta_{in}(s)$	$N \cdot \frac{H_{ol}(s)}{1+H_{ol}(s)}$	low-pass
PFD/CP noise	$\theta_{out}(s) / i_{cp}(s)$	$\frac{N}{K_{pd}} \cdot \frac{H_{ol}(s)}{1+H_{ol}(s)}$	low-pass
LF noise	$\theta_{out}(s) / v_{lf}(s)$	$\frac{K_{vco}}{s} \cdot \frac{1}{1+H_{ol}(s)}$	band-pass
VCO noise	$\theta_{out}(s) / \theta_{vco}(s)$	$\frac{1}{1+H_{ol}(s)}$	high-pass
divider noise	$\theta_{out}(s) / \theta_{div}(s)$	$-N \cdot \frac{H_{ol}(s)}{1+H_{ol}(s)}$	low-pass

From Table 3-1, we know that the input noise and divider noise have the same transfer function magnitude to the PLL output.

Due to the inherent pole at origin provided by VCO, the PLL is always one order higher than the loop filter. Figure 3-7 (a) shows a passive third-order loop filter for charge-pump PLL. C_1 produces the first pole at the origin for the type-II PLL. Together with C_1, R_1 is used to generate a zero for loop stability. C_2 is used to smooth the control voltage ripples and to generate the second pole ω_{p2}. R_3 and C_3 are used to generate the third pole ω_{p3} to further suppress reference spurs and the high-frequency noise in the ΣΔ-PLL. The pole-zero location and Bode-plot of the third-order loop filter's transimpedance are illustrated in Fig. 3-7 (b) and (c), respectively. The first-order loop filter has R_1 and C_1 only. It is not used in practice due to the voltage ripple, but it simplifies the linear analysis of a second-order charge-pump PLL. The second- and third-order loop filters are used in practice. Higher order loop filters are rarely used because the phase margin is reduced with more poles.

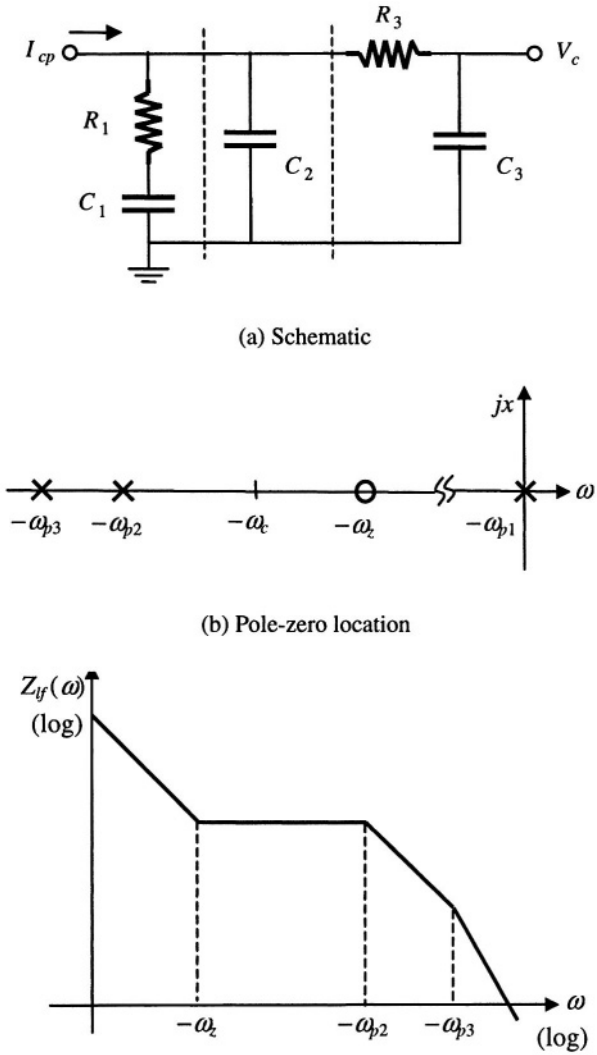


Figure 3-7. Passive loop filter for charge-pump PLL

Poles and zero of the open-loop PLL can be calculated from loop filter parameters. The phase-margin ϕ_m and cross-over (or unity-gain) bandwidth ω_c can be observed from the Bode plot of the PLL open-loop transfer function in (3.3). However, the closed-loop damping factor ζ and natural frequency ω_n provide more insights into the PLL dynamic behavior. Now we derive the relationship between these parameters for a second-order PLL. The impedance of a first-order loop filter, which is composed by R_1 and C_1 only in Fig. 3-7 (a), is:

$$Z_{lf}(s)=\frac{V_c(s)}{I_{cp}(s)}=R_1\frac{1+sR_1C_1}{sR_1C_1}=R_1\frac{\omega_z+s}{s} \tag{3.4}$$

where

$$\omega_z=1/(R_1C_1) \tag{3.5}$$

is the zero in the loop filter for loop stability. The pole is located in the origin, i.e., ω_{p1}=0. The PLL open-loop (disconnecting the divider and PFD) gain is:

$$H_{ol2}(s)=\frac{K_{pd}K_{vco}R_1}{Ns}\cdot\frac{1+sR_1C_1}{sR_1C_1}=K\frac{1+sR_1C_1}{s^2R_1C_1} \tag{3.6}$$

where the PLL loop gain is:

$$K=\frac{K_{pd}K_{vco}R_1}{N} \tag{3.7}$$

Thus the crossover frequency, where the open-loop gain is unity, is solved from $|H_{ol}(j\omega_c)|=1$:

$$\omega_c=\sqrt{\frac{K^2+K\sqrt{K^2+4\omega_z^2}}{2}} \tag{3.8}$$

or simply

$$\omega_c=\frac{K}{\sin(\phi_m)} \tag{3.9}$$

where the phase margin is:

$$\phi_m=\tan^{-1}\left(\frac{\omega_c}{\omega_z}\right) \tag{3.10}$$

The second-order PLL closed-loop gain is:

$$H_{cl2}(s)=\frac{\theta_{out}(s)}{\theta_{in}(s)}=N\frac{K(s+\omega_z)}{s^2+Ks+K\omega_z} \tag{3.11}$$

Thus, the damping factor and natural frequency are as follows:

$$\omega_n=\sqrt{K\omega_z}=\omega_c\sqrt{\cos(\phi_m)} \tag{3.12}$$

$$\zeta=\frac{1}{2}\left(\sqrt{\frac{K}{\omega_z}}\right)=\frac{1}{2}\sin(\phi_m)/\sqrt{\cos(\phi_m)} \tag{3.13}$$

Equation (3.11) yields:

$$H_{cl2}(s)=N\frac{2\zeta\omega_n s+\omega_n^2}{s^2+2\zeta\omega_n s+\omega_n^2} \tag{3.14}$$

From (3.14) we know that the closed loop gain has a low-pass characteristic. It is equal to the frequency divide ratio N when $\omega<<\omega_n$ or $\omega=\sqrt{2}\omega_n$. It is reduced by 3dB at

$$\omega_{-3dB}=\sqrt{\left(2\zeta^2+1\right)+\sqrt{\left(2\zeta^2+1\right)^2+1}}\cdot\omega_n \tag{3.15}$$

Table 3-2 lists the relationship between ω_{-3dB}/ω_n ratio and the damping factor ζ.

Table 3-2. Relationship between *–3dB* bandwidth and damping factor

ζ	0.5	0.707	1.0	1.414	2.0
ω_{-3dB}/ω_n	1.82	2.06	2.27	3.18	4.25

Note that $\omega_c\approx\omega_{-3dB}$, and as in this book we refer to the PLL open-loop unity gain frequency ω_c as the PLL bandwidth.

The natural frequency to crossover frequency ratio ω_n/ω_c and damping factor ζ versus phase margin ϕ_m is plotted in Fig. 3-8.

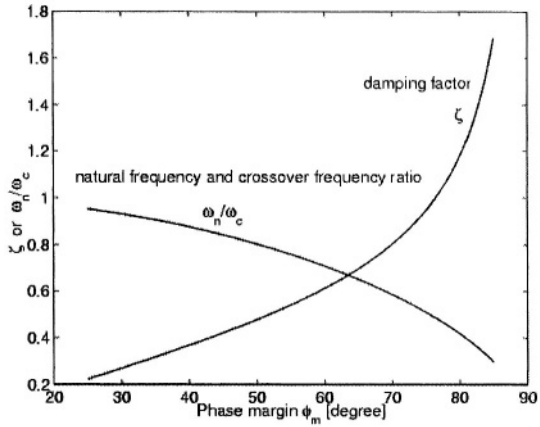


Figure 3-8. Natural frequency and damping factor vs. phase margin

For the second-order passive loop filter (with $R_3 = 0$ and $C_3 = 0$ in Fig. 3-7 (a)), the transimpedance is

$$Z_{lf}(s) = R_1 \frac{1 + sR_1C_1}{sR_1(C_1 + C_2) + s^2 R_1C_1R_1C_2} = R_1 \frac{1 + s/\omega_z}{s(1 + s/\omega_{p2})/\omega_z} \frac{b-1}{b} \tag{3.16}$$

where $b = 1 + C_1 / C_2$, and the second pole is:

$$\omega_{p2} = \frac{1}{R_1 \dfrac{C_1C_2}{C_1 + C_2}} = b\omega_z \approx \frac{1}{R_1C_2} \tag{3.17}$$

The open-loop gain is

$$H_{ol3}(s) = K \frac{1 + s/\omega_z}{s^2(1 + s/\omega_{p2})/\omega_z} \frac{b-1}{b} \tag{3.18}$$

The bandwidth of a third-order charge-pump PLL is:

$$\omega_c = K \cdot \frac{b-1}{b} \cdot \frac{\cos(\phi_{p2})}{\sin(\phi_z)} \tag{3.19}$$

where $\phi_z = \tan^{-1}(\omega_c / \omega_z)$ and $\phi_{p2} = \tan^{-1}(\omega_c / \omega_{p2})$. The open-loop phase-margin is:

$$\phi_m = \phi_z - \phi_{p2} = \tan^{-1}\left(\frac{\omega_c}{\omega_z}\right) - \tan^{-1}\left(\frac{\omega_c}{\omega_{p2}}\right) \tag{3.20}$$

For maximum phase margin, we have

$$\omega_c = \sqrt{\omega_{p2}\omega_z} = \sqrt{b}\omega_z \tag{3.21}$$

Therefore, the optimal phase margin is

$$\phi_m = \tan^{-1}\sqrt{\frac{\omega_{p2}}{\omega_z}} - \tan^{-1}\sqrt{\frac{\omega_z}{\omega_{p2}}} = \tan^{-1}\frac{b-1}{2\sqrt{b}} \tag{3.22}$$

Thus, the maximum phase margin is exclusively determined by the capacitor ratio b. In the meantime, $\sin(\phi_z) = \cos(\phi_{p2})$, and the PLL bandwidth in (3.19) is simplified as:

$$\omega_c = K \cdot \frac{b-1}{b} = K \cdot \frac{C_1}{C_1 + C_2} \approx K \tag{3.23}$$

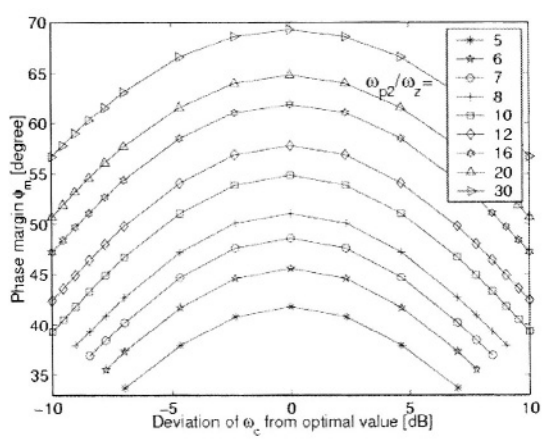


Figure 3-9. Phase margin with ω_c variation for different ω_{p2} / ω_z values

In a real PLL, the inaccuracy of resistance and capacitance of an on-chip loop filter and variance of VCO conversion gain K_{vco} affects the phase margin. The variation of resistance and capacitance is typically 10%~20%, while the variation of K_{vco} can be more than a factor of 2. Therefore, we have to keep enough phase-margin to accommodate variations of design parameters. Figure 3-9 illustrates the PLL phase margin for different ω_{p2}/ω_z values from 5 to 30, when ω_c deviates from its optimal value of $\sqrt{\omega_{p2}\omega_z}$. It shows that the phase margin is not much sensitive to the variation of ω_c and ω_{p2}/ω_z ratio. For example, in case of $\omega_{p2}/\omega_z = 10$, the optimal phase margin is 55°, and it degrades to 48.7° when ω_c deviates from its optimal value by a factor of 2, i.e., $\pm 6dB$.

The closed-loop phase (noise) transfer function of charge-pump PLL with second-order passive loop filter is:

$$H_{cl3}(s) = N\frac{1+s/\omega_z}{1+s/\omega_z+s^2/(\omega_z\omega_c)+s^3/(\omega_z\omega_c\omega_{p2})} \tag{3.24}$$

When the loop bandwidth is chosen for maximum phase margin (see 3.21), (3.24) can be written as

$$H_{cl3}(s) = N\frac{\omega_c^3+\sqrt{b}\omega_c^2 s}{(s+\omega_c)\left[s^2+(\sqrt{b}-1)\omega_c s+\omega_c^2\right]} \tag{3.25}$$

Equation (3.25) can be rewritten as:

$$H_{cl3}(s) = N\frac{(2\zeta+1)\omega_n^2 s+\omega_n^3}{(s+\omega_n)(s^2+2\zeta\omega_n s+\omega_n^2)} \tag{3.26}$$

where the damping factor and natural frequency are as follows.

$$\zeta = (\sqrt{b}-1)/2 \tag{3.27}$$

$$\omega_n = \omega_c \tag{3.28}$$

If $\zeta \neq 1$ (i.e., $b \neq 9$), $H_{cl3}(s)$ in (3.26) has three different poles as shown in (3.29).

$$H_{cl3}(s)=\frac{N}{\zeta-1}\left[\frac{\zeta\omega_n}{s+\omega_n}-\frac{\omega_n^2+\zeta\omega_n s}{s^2+2\zeta\omega_n s+\omega_n^2}\right] \tag{3.29}$$

When $\zeta=1$ (i.e., b = 9), $H_{cl3}(s)$ in (3.26) has three poles at the loop bandwidth ω_c $(=\omega_n)$ and one zero at one-third of ω_c, as shown in (3.30).

$$H_{cl3}(s)=N\frac{3\omega_n^2 s+\omega_n^3}{(s+\omega_n)^3} \tag{3.30}$$

For the third-order passive loop filter (see Fig. 3-7 (a)), the transimpedance is

$$Z_{lf}(s)=\frac{1}{s}\frac{(1+sR_1C_1)/(C_1+C_2+C_3)}{1+s\dfrac{R_1C_1(C_2+C_3)+R_3C_3(C_1+C_2)}{C_1+C_2+C_3}+s^2\dfrac{R_1R_3C_1C_2C_3}{C_1+C_2+C_3}} \tag{3.31}$$

Usually, $C_1 >> C_2, C_3$ and $R_1 > R_3$

$$\begin{aligned} Z_{lf}(s)&\approx\frac{1}{s(C_1+C_2+C_3)}\cdot\frac{1+s/\omega_z}{1+sR_1(C_2+C_3)+s^2R_1R_3C_2C_3}\\ &=\frac{1}{s(C_1+C_2+C_3)}\cdot\frac{1+s/\omega_z}{(1+s/\omega_{p2})(1+s/\omega_{p3})}\end{aligned} \tag{3.32}$$

Therefore, the two non-zero poles are as follows.

$$\omega_{p2}\approx\frac{1}{R_1(C_2+C_3)} \tag{3.33}$$

$$\omega_{p3}\approx\frac{1}{R_3C_2C_3/(C_2+C_3)} \tag{3.34}$$

The bandwidth of a fourth-order charge-pump PLL is:

$$\omega_c=K\cdot\frac{C_1}{C_1+C_2+C_3}\cdot\frac{\cos(\phi_{p2})\cdot\cos(\phi_{p3})}{\sin(\phi_z)} \tag{3.35}$$

where $\phi_{p3} = \tan^{-1}(\omega_c / \omega_{p3})$. The open-loop phase-margin is:

$$\phi_m = \phi_z - \phi_{p2} - \phi_{p3} = \tan^{-1}\left(\frac{\omega_c}{\omega_z}\right) - \tan^{-1}\left(\frac{\omega_c}{\omega_{p2}}\right) - \tan^{-1}\left(\frac{\omega_c}{\omega_{p3}}\right) \quad (3.36)$$

Usually, the phase-margin degradation (ϕ_{p3}) due to the third pole (ω_{p3}) is very small, the maximum ϕ_m still occurs around $\omega_c = \sqrt{\omega_{p2}\omega_z}$. Since $\sin(\phi_z) \approx \cos(\phi_{p2}) \cdot \cos(\phi_{p3})$, the PLL bandwidth in (3.35) is simplified as:

$$\omega_c \approx K \cdot \frac{C_1}{C_1 + C_2 + C_3} \approx K \quad (3.37)$$

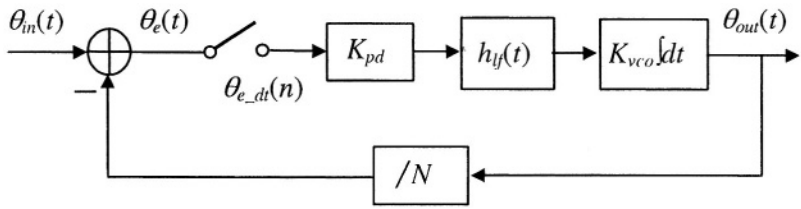
More discussions on high-order loop filter design can be found in the literature [5]-[9]. For example, the exact relationship among ω_c, ω_z, ω_{p2} and ω_{p3} in the fourth-order PLL for maximum ϕ_m is derived in [9].

Note that the above phase-margin calculation is based on the continuous-time linear model of the charge-pump PLL. This model is good for loop bandwidth f_c less than 1/10 of the reference frequency f_{ref}. Otherwise the settling behavior will differ from the calculations significantly. With the loop delay t_d taken into account, the PLL open-loop gain and phase margin become:

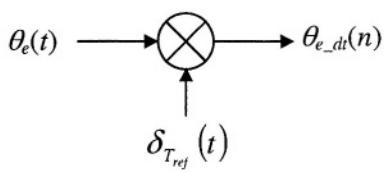
$$H_{ol}^{'}(s) = H_{ol}(s) \cdot e^{-st_d} \quad (3.38)$$

$$\phi_m^{'} = \phi_m - \omega_c t_d \qquad rad \quad (3.39)$$

Therefore, the loop delay degrades the phase margin, and hence reduces the damping factor [10]. Usually, the loop delay is small and the phase margin degradation is negligible. In [11], the PLL sampling delay due to discrete-time operation of PFD is modeled as the PFD update period T_{ref}. However, the sampling delay is exaggerated in [11]. As shown in Fig. 3-10, the PFD operation is the impulse sampling, not the sample-and-hold. An accurate result of the stability limit based on linearized approximate difference equations was derived in [1], and it agrees well with the Matlab behavioral modeling in the Appendix.



(a) Model in time domain



(b) PFD sampling function

Figure 3-10. PLL phase model with sampling

The sampling pulse function $\delta_{T_{ref}}(t)$ is a sequence of $\delta(t)$ with period T_{ref}, that is,

$$\delta_{T_{ref}}(t) = \sum_{n=-\infty}^{\infty} \delta(t - nT_{ref}) \tag{3.40}$$

$$\theta_{e\_dt}(n) = \theta_e(t) \cdot \delta(t - nT_{ref}) = \theta_e(nT_{ref}) \tag{3.41}$$

3.1.3 Locking time

Considering that the PLL is initially locked and the frequency divide ratio changes due to channel switching, we calculate the locking time for a given frequency error. Locking time is also referred to as settling time or switching time.

For the third-order loop filter shown in Fig. 3-7 (a), its transimpedance is given by:

$$Z_{lf}(s) = \frac{1 + s \cdot k_0}{s(k_1 \cdot s^2 + k_2 \cdot s + k_3)} \tag{3.42}$$

where $k_0 = R_1 C_1$, $k_1 = R_1 R_3 C_1 C_2 C_3$, $k_2 = R_1 C_1 (C_2 + C_3) + R_3 C_3 (C_1 + C_2)$ and $k_3 = C_1 + C_2 + C_3$. Note that the two non-zero poles of $Z_{lf}(s)$ are unequal real numbers because

$$k_2^2 - 4k_1 k_3 = [R_1 C_1 (C_2 + C_3) - R_3 C_3 (C_1 + C_2)]^2 + 4R_1 R_3 C_1^2 C_3^2 > 0 \quad (3.43)$$

Equation (3.42) leads to the following PLL closed-loop phase or frequency transfer function:

$$H_{cl4}(s) = \frac{K_{pd} K_{vco} N \cdot (1 + s \cdot k0)}{k_1 N \cdot s^4 + k_2 N \cdot s^3 + k_3 N \cdot s^2 + K_{pd} K_{vco} k_0 \cdot s + K_{pd} K_{vco}} \quad (3.44)$$

For simplicity, we ignore these high order terms, which are smaller than lower order terms. The consequences of this simplification are more on the initial characteristics, such as overshoot, and less on long time behavior, such as lock time. The simplified second-order expression is:

$$H_{cl2}(s) \approx \frac{\frac{K_{pd} K_{vco}}{k_3} \cdot (1 + s \cdot k0)}{s^2 + \frac{K_{pd} K_{vco} k_0}{k_3 N} \cdot s + \frac{K_{pd} K_{vco}}{k_3 N}} \quad (3.45)$$

Defining the damping factor and natural frequency:

$$\zeta = \frac{k_0}{2} \sqrt{\frac{K_{pd} K_{vco}}{k_3 N}} \quad (3.46)$$

$$\omega_n = \sqrt{\frac{K_{pd} K_{vco}}{k_3 N}} \quad (3.47)$$

Equation (3.45) becomes:

$$H_{cl2}(s) = \frac{N(2\zeta\omega_n \cdot s + \omega_n^2)}{s^2 + 2\zeta\omega_n \cdot s + \omega_n^2} \quad (3.48)$$

Thus, the two poles of the second-order transfer function are:

$$\omega_{cl\_p1,2} = \begin{cases} \left(\zeta \pm j\sqrt{1-\zeta^2}\right)\omega_n & \zeta < 1 \\ \omega_n & \zeta = 1 \\ \left(\zeta \pm \sqrt{\zeta^2-1}\right)\omega_n & \zeta > 1 \end{cases} \tag{3.49}$$

When the PLL output frequency changes from f_1 to f_2 due to the change of N, it is equivalent to change the reference frequency from f_1/N to f_2/N. Note that, the value of N used in all of these equations should be the value corresponding to the new output frequency f_2. This approximation does not cause much error when the change in the value of N is relatively small and the instantaneous phase error is less than 2π. The lock time can be readily evaluated by means of the final value theorem of the Laplace transformation, which states that:

$$\lim_{t\to\infty}\theta(t) = \lim_{s\to 0} s\theta(s) \tag{3.50}$$

The PLL output frequency responds to the input frequency step as:

$$f_{out}(s) - f_1 = \frac{f_2 - f_1}{N \cdot s} H_{cl2}(s) \tag{3.51}$$

Using inverse Laplace transformation, the normalized frequency error is:

$$\varepsilon_2(t) = \frac{f_{out}(t) - f_2}{f_1 - f_2}$$

$$= \begin{cases} e^{-\zeta\omega_n t}\left[\cos\left(\omega_n t\sqrt{1-\zeta^2}\right) + \dfrac{-\zeta}{\sqrt{1-\zeta^2}}\sin\left(\omega_n t\sqrt{1-\zeta^2}\right)\right] & 0 < \zeta < 1 \\ e^{-\omega_n t}\left(1-\omega_n t\right) & \zeta = 1 \\ e^{-\zeta\omega_n t}\left[\cosh\left(\omega_n t\sqrt{\zeta^2-1}\right) + \dfrac{-\zeta}{\sqrt{1-\zeta^2}}\sinh\left(\omega_n t\sqrt{\zeta^2-1}\right)\right] & \zeta > 1 \end{cases} \tag{3.52}$$

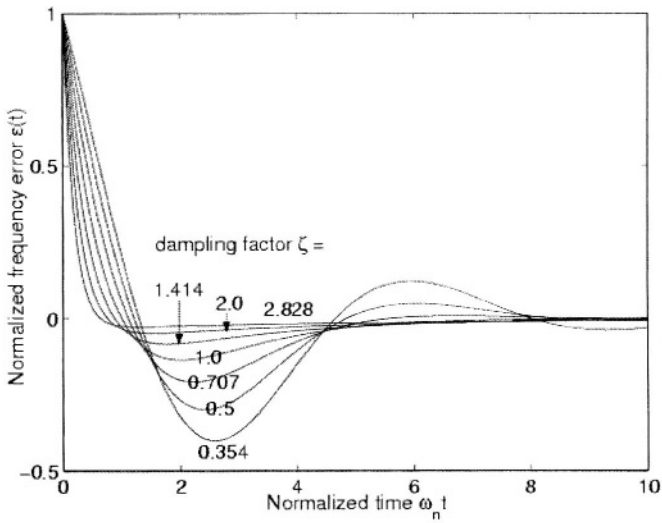
Equation (3.52) is plotted in Fig. 3-11 (a). The normalized time for x-axis is $\omega_n t$. It is under-damped for $0<\zeta<1$, critical-damped for $\zeta=1$, and over-damped for $\zeta>1$.

To check the error introduced by the approximation in (3.45), the exact $\varepsilon(t)$ for the third-order charge-pump PLL is derived in (3.53) using $H_{cl3}(s)$ in (3.29) and (3.30). Note that, the damping factor ζ and natural frequency ω_n in (3.53) are those defined for the third-order PLL in (3.27) and (3.28), respectively.

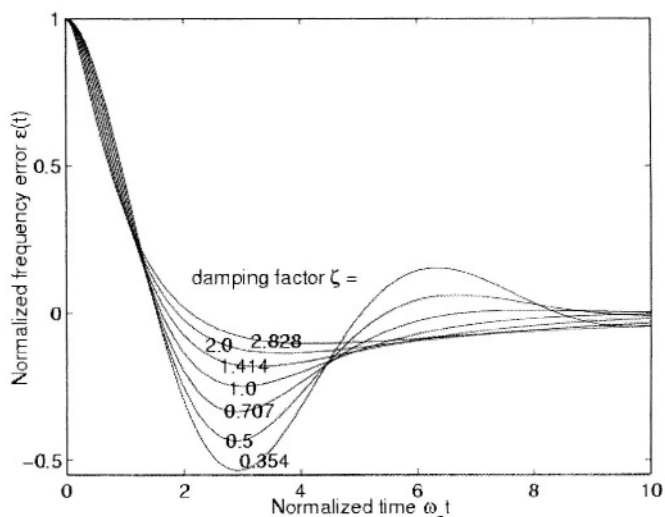
$$\varepsilon_3(t)=\begin{cases}\dfrac{1}{\zeta-1}\left[\zeta e^{-\omega_n t}-e^{-\zeta\omega_n t}\cos\left(\omega_n t\sqrt{1-\zeta^2}\right)\right] & 0<\zeta<1\\ e^{-\omega_n t}\left(1+\omega_n t-\omega_n^2 t^2\right) & \zeta=1\\ \dfrac{1}{\zeta-1}\left[\zeta e^{-\omega_n t}-e^{-\zeta\omega_n t}\cosh\left(\omega_n t\sqrt{\zeta^2-1}\right)\right] & \zeta>1\end{cases} \tag{3.53}$$

As illustrated in Fig. 3-11 (b), we see the discrepancy between the settling behavior of the second- and the third-order PLL's. Although it is difficult to derive the exact $\varepsilon(t)$ for the fourth-order PLL, its difference from that of the third-order one is negligible because the third pole of the loop filter ω_{p3} is usually more than one order larger than the PLL bandwidth ω_c.

Figure 3-12 illustrates the PLL output frequency-settling behavior for a relative frequency error of $\varepsilon=10^{-5}$. For example, from this figure we read that for damping factor $\zeta=1$, the settling time, which is normalized by a factor of ω_n, is about 14 and 17 for the second and third-order PLL, respectively. Figure 3-13 (a) gives the MATLAB simulated normalized settling time for $0.25\le\zeta\le 2\sqrt{2}$, and $\varepsilon=10^{-3}$, 10^{-4}, 10^{-5}, and 10^{-6}. For PLL with the second-order PLL, ω_n and ζ can be mapped into ω_c and ϕ_m using (3.12) and (3.13). Therefore, the locking time, which is normalized by a factor of ω_c, is plotted against ϕ_m in Fig. 3-13 (b). The accurate locking time of a third-order PLL in terms of ω_c $(=\omega_n)$ and ϕ_m is shown in Fig. 3-13 (c).

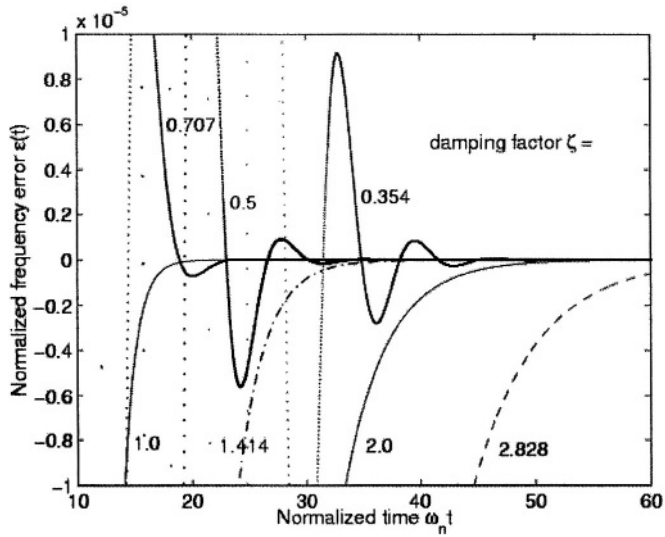


(a) Second-order PLL

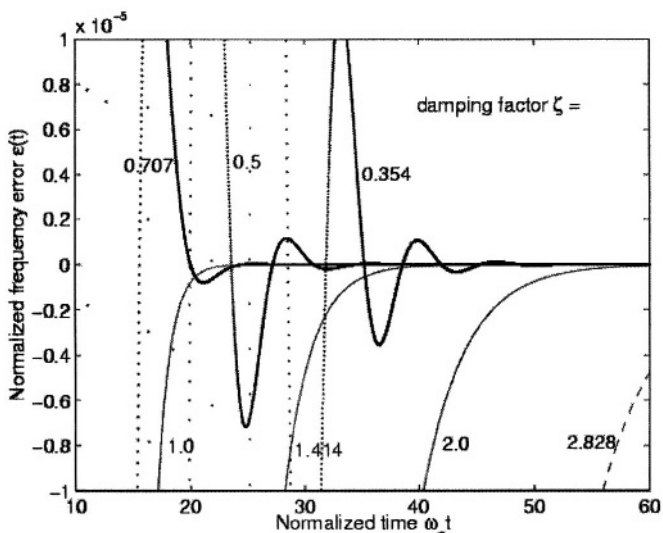


(b) Third-order PLL

Figure 3-11. PLL settling behavior vs. damping factor (continued)

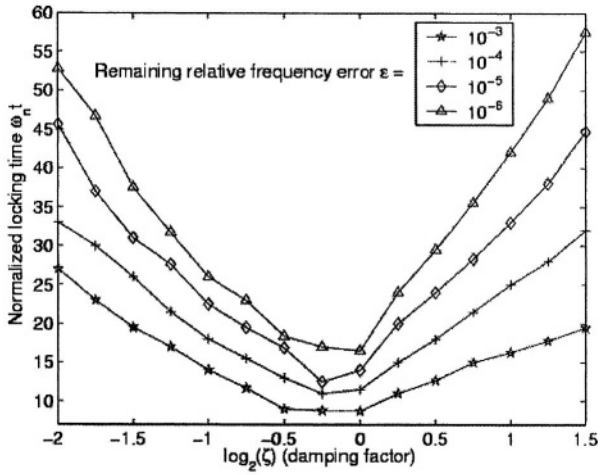


(a) Second-order PLL

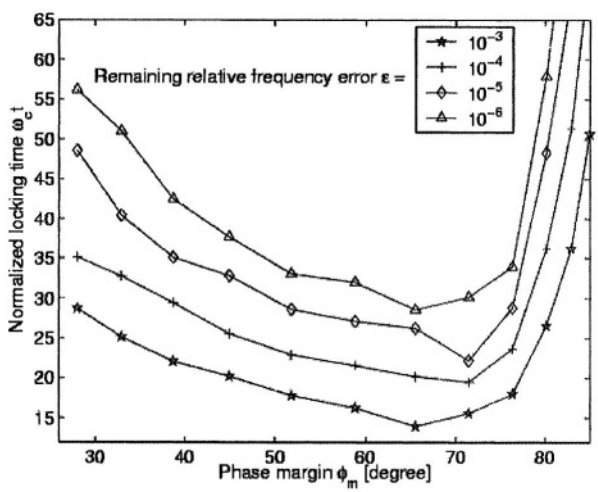


(b) Third-order PLL

Figure 3-12. PLL settling behavior for relative phase error of 10^{-5}

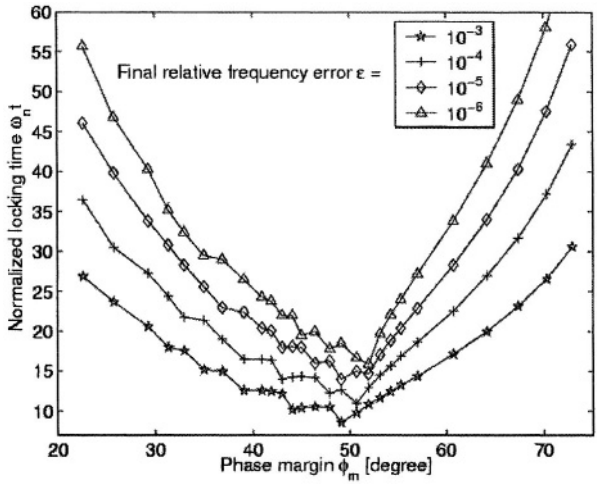


(a) Second-order PLL (time normalized to $\omega_n t$)



(b) Second-order PLL (time normalized to $\omega_c t$)

Figure 3-13. PLL locking time



(c) Third-order PLL

Figure 3-13. PLL locking time (continued)

Approximate formulas to calculate the settling time in the literature are mostly based on (3.52), which is accurate for the second-order PLL. For most design, $0 < \zeta < 1$, and the term in the brackets of (3.52) has a maximum value of $1/\sqrt{1-\zeta^2}$, therefore the locking time is [3], [12]:

$$T_L = -\frac{\ln\left(\varepsilon\sqrt{1-\zeta^2}\right)}{\zeta\omega_n} \tag{3.54}$$

where the specified frequency accuracy is:

$$\varepsilon = \frac{f_{error}}{|f_2 - f_1|} \tag{3.55}$$

However, the charge-pump PLL is either third or fourth order in practical design. We have observed the settling discrepancy of the second and third order PLL from either equations (3.52) and (3.53), or Fig. 3-13. We can also use a second-order least error fit to approximate the locking time of the third-order PLL in Fig. 3-13 (c). For example, for final relative frequency settling error $\varepsilon = 10^{-5}$, the locking time can be expressed as:

$$T_L = \frac{1}{\omega_c}\left(0.0554\phi_m^2 - 5.183\phi_m + 137.84\right) \tag{3.56}$$

The locking time formula of the third-order PLL based on transient simulations given in [13] is:

$$T_L = -\frac{\ln(\varepsilon)}{f_c \zeta_e(\phi_m)} \tag{3.57}$$

where $\zeta_e(\phi_m)$ is defined as an effective damping factor depending on phase margin ϕ_m. Reference [13] only gives the average $\zeta_e(\phi_m)$ for $\ln(\varepsilon) = -10$ obtained from transient simulations. Based on behavioral-level simulation, the discrete-time effect on the third-order PLL locking time is also provided in [13], which shows that the increase of PLL locking time due to PFD delay is relatively small.

The locking time formula for a simple first-order PLL derived in [14] is:

$$T_L = -\frac{\ln(\varepsilon)}{\omega_c} \tag{3.58}$$

and the formula for the second-order PLL given in [15] is:

$$T_L = -\frac{\ln(\zeta\varepsilon)}{\zeta\omega_n} \tag{3.59}$$

Further simplified [16] locking time expression is:

$$T_L = \frac{4}{f_c} \tag{3.60}$$

Note that the above locking time calculations are based on the linear continuous-time model of the charge-pump PLL. This model is good for loop bandwidth f_c much less than 1/10 of the reference frequency f_{ref}. Otherwise the settling behavior will deviate from the calculations substantially as shown in [17].

Moreover, to check if the maximum phase error θ_e during the settling is in the linear PFD range of $\pm 2\pi$, we calculate the maximum PFD phase error during the transient response to a frequency step input.

The transfer function of the input phase to PFD phase error θ_e in a second-order charge-pump PLL is

$$H_e(s)=\frac{\theta_e(s)}{\theta_{in}(s)}=1-\frac{H_{cl}(s)}{N} \tag{3.61}$$

Therefore, the instantaneous PFD phase error for a frequency step input is

$$\theta_e(s)=H_e(s)\cdot\frac{2\pi(f_2-f_1)}{Ns^2}=\left[1-\frac{H_{cl}(s)}{N}\right]\cdot\frac{2\pi(f_2-f_1)}{Ns^2} \tag{3.62}$$

Given the expression $H_{cl}(s)$ of the second and third order PLL in (3.48) (or (3.14)) and (3.25), respectively, the inverse Laplace transformation gives the transient phase error in time domain as

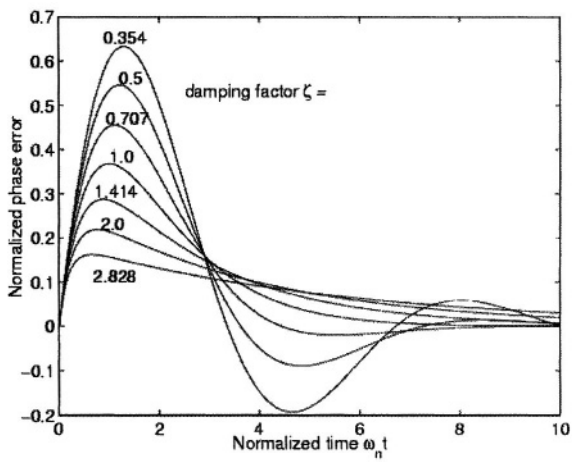
$$\theta_{e2}(t)=\frac{2\pi(f_2-f_1)}{N\omega_n}\times\begin{cases}e^{-\zeta\omega_n t}\dfrac{1}{\sqrt{1-\zeta^2}}\sin\left(\omega_n t\sqrt{1-\zeta^2}\right) & 0<\zeta<1\\ e^{-\omega_n t}\cdot\omega_n t & \zeta=1\\ e^{-\zeta\omega_n t}\dfrac{1}{\sqrt{\zeta^2-1}}\sinh\left(\omega_n t\sqrt{\zeta^2-1}\right) & \zeta>1\end{cases} \tag{3.63}$$

$$\theta_{e3}(t)=\frac{2\pi(f_2-f_1)}{N\omega_n}\times$$
$$\begin{cases}\dfrac{1}{1-\zeta}\left\{\zeta e^{-\omega_n t}+e^{-\zeta\omega_n t}\left[\begin{array}{l}-\zeta\cos\left(\omega_n t\sqrt{1-\zeta^2}\right)+\\ \sqrt{1-\zeta^2}\sin\left(\omega_n t\sqrt{1-\zeta^2}\right)\end{array}\right]\right\} & 0<\zeta<1\\ e^{-\omega_n t}\cdot\left(\omega_n t+\omega_n^2 t^2\right) & \zeta=1\\ \dfrac{1}{1-\zeta}\left\{\zeta e^{-\omega_n t}+e^{-\zeta\omega_n t}\left[\begin{array}{l}-\zeta\cosh\left(\omega_n t\sqrt{\zeta^2-1}\right)-\\ \sqrt{\zeta^2-1}\sinh\left(\omega_n t\sqrt{\zeta^2-1}\right)\end{array}\right]\right\} & \zeta>1\end{cases} \tag{3.64}$$

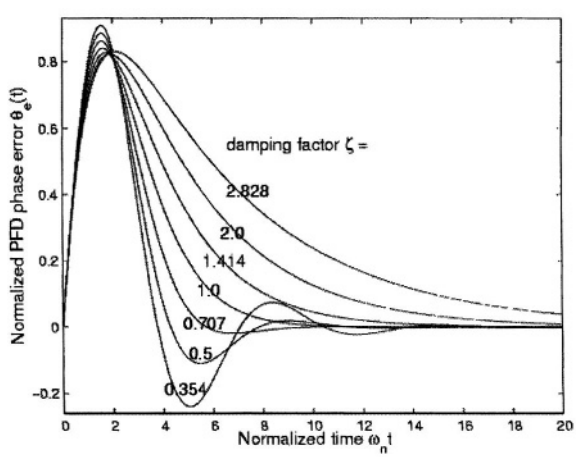
The normalized PFD phase error, $\theta_e(t)\cdot\dfrac{N\omega_n}{2\pi(f_2-f_1)}$, is plotted in Fig. 3-14. For example of $\zeta=0.707$, the normalized phase error has a maximum

value of 0.45 (or 0.85) for the second (or third) order PLL. Fig. 3-14 (b) reveals that to keep the phase error in the range of $\pm 2\pi$ for a third-order PLL, the input referred frequency step, $(f_2 - f_1)/N$, should be in the range of $\pm 1.1\omega_c$. A similar result based on transient simulations of a third-order PLL is given in [17] as:

$$\left|\frac{f_2 - f_1}{N}\right| < 1.25\omega_c \tag{3.65}$$



(a) Second-order PLL

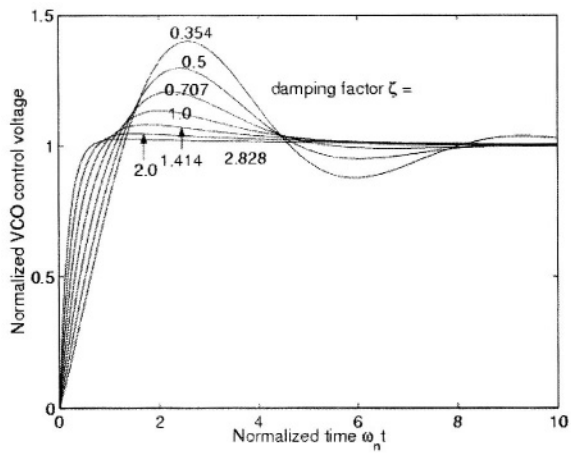


(b) Third-order PLL

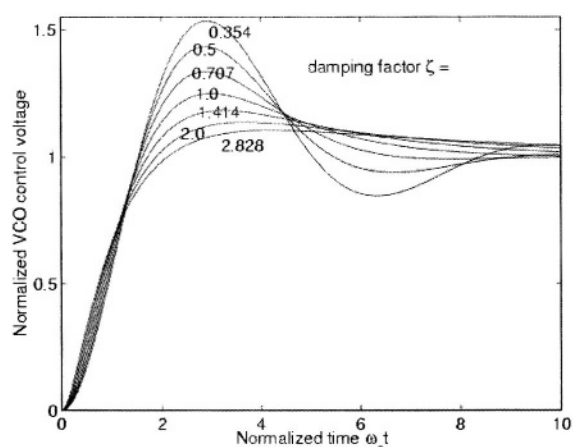
Figure 3-14. Normalized PFD phase error during locking

Finally, if the overload of charge pump or VCO occurs due to under-damped overshoot, the locking time will be longer. We can calculate the overshoot to check if overload occurs. The transfer function of the input phase to the VCO control voltage in a charge-pump PLL is

$$H_{Vc}(s)=\frac{V_c(s)-V_{c1}}{\theta_{in}(s)}=\frac{H_{cl}(s)\cdot s}{K_{vco}} \tag{3.66}$$



(a) Second-order PLL



(b) Third-order PLL

Figure 3-15. VCO control voltage during locking

where V_{c1} is the VCO control voltage corresponding to output frequency f_1. When the VCO output frequency changes from f_1 to f_2, the transient response of VCO control voltage change is

$$V_c(s) - V_{c1} = H_{Vc}(s) \cdot \theta_{in}(s) = \frac{2\pi(f_2 - f_1)}{K_{vco}} \cdot \frac{H_{cl}(s)}{Ns} \tag{3.67}$$

Using inverse Laplace transformation, it yields

$$V_c(t) - V_{c1} = \frac{2\pi(f_2 - f_1)}{K_{vco}}[1 - \varepsilon(t)] \tag{3.68}$$

where $\varepsilon(t)$ for the second or third-order PLL is given in (3.52) or (3.53). The normalized control voltage change is plotted in Fig. 3-15. Overshoot increases when damping factor ζ decreases. For example, when $\zeta = 0.707$, the overshoot is about 20% and 30% of the control voltage change for the second and third order PLL's, respectively.

3.1.4 Tracking and acquisition

Tracking is the transient response of a PLL output to the change of input phase in the locked state, and acquisition is the process of bringing an unlocked loop into lock. Although the tracking or acquisition process was originally defined for a PLL with analog multiplier PD, it can be extended to the charge-pump PLL frequency synthesizers. The four PLL operation ranges are as follows:

(1) The hold range $\Delta\omega_H$ is the frequency range in which PLL operation can be statistically stable. For charge-pump PLL, $\Delta\omega_H \to \infty$. Thus, the actual hold range is only restricted by the PLL tuning range.

(2) The lock range $\Delta\omega_L$, by definition is the frequency offset between the inputs of analog multiplier PD, which causes the PLL to acquire lock in one beat note for linear PLL. For charge-pump PLL, $\Delta\omega_L \approx 4\pi\zeta\omega_n$. Since the lock-in process is roughly completed within one cycle of the damped oscillation, the lock-in time $T_L \approx \frac{2\pi}{\omega_n}$.

(3) The pull-in range $\Delta\omega_P$: This is the range within which a PLL will always become locked, but the process can be rather slow. The pull-in process is a nonlinear phenomenon and is very difficult to calculate. For PFD, the average output pulse duty cycle is approximately 50% during

the pull-in process. Thus the pull-in time is $T_P = \dfrac{2C \cdot \Delta\omega}{I_{cp} K_{vco}}$, and the pull-in range $\omega_P \to \infty$.

(4) The pull-out range $\Delta\omega_{PO}$ is the size of the frequency step applied to the reference input which causes the PLL to lose phase tracking. Because the PFD output is linear in the range of $-2\pi < \theta_e < 2\pi$, it can be computed explicitly using the linear model.

$$\Delta\omega_{PO} = \begin{cases} 2\pi\omega_n \exp\left(\dfrac{\zeta}{\sqrt{1-\zeta^2}} \tan^{-1} \dfrac{\sqrt{1-\zeta^2}}{\zeta}\right) & \zeta < 1 \\ 2\pi\omega_n & \zeta = 1 \\ 2\pi\omega_n \exp\left(\dfrac{\zeta}{\sqrt{\zeta^2-1}} \tanh^{-1} \dfrac{\sqrt{\zeta^2-1}}{\zeta}\right) & \zeta > 1 \end{cases} \tag{3.69}$$

The least-square fit gives the linear approximation [18]:

$$\Delta\omega_{PO} = 11.55\omega_n(\zeta + 0.5) \tag{3.70}$$

The operating ranges of a second-order charge-pump PLL are summarized in Table 3-3.

Table 3-3. Operating ranges of charge-pump PLL

Parameter		Frequency range	Time
acquisition	hold range	$\Delta\omega_H \to \infty$	NA
	lock range	$\Delta\omega_L \approx 4\pi\zeta\omega_n$	$T_L \approx \dfrac{2\pi}{\omega_n}$
	pull-in range	$\omega_P \to \infty$	$T_P = \dfrac{2C \cdot \Delta\omega}{I_{cp} K_{vco}}$
tracking	pull-out range	$\Delta\omega_{PO} = 11.55\omega_n(\zeta + 0.5)$	NA

For PLL's with other types of phase detector, such as the analog multiplier, XOR gate and JK flip-flop, the formulas of their operating ranges can be found in [18].

3.2 Fast-locking techniques

Fast locking in frequency synthesizer is required for modern communication systems, such as digital cellular mobile systems [19], car radio receivers [13] and frequency-hopped (FH) systems [20]. Since for a charge-pump PLL, the locking time is inversely proportional to the loop bandwidth, the locking time might be longer than a specific requirement for a given loop bandwidth. For example, for the frequency synthesizer in [13], the SNR constraint asks for 800*Hz* bandwidth, but the settling times requires at least 3.2*kHz* bandwidth. Thus various techniques have been used to achieve fast PLL locking after the channel switching. Basically, these techniques are divided into two categories: speed-up mode and VCO pre-tuning.

3.2.1 Bandwidth gear-shifting

The basic idea behind this scheme is gear-shifting, that is, using a larger loop bandwidth during the frequency switching transition and shifting the loop bandwidth to the normal value after the PLL is locked or after a certain (programmable) period of time.

One speed-up mode is to use both proportional (I_{cpp}) and integral (I_{cpi}) charge-pump currents, as shown in Fig. 3-16. The loop filter output voltage in the speed-up mode is:

$$V_c(s) = \frac{I_{cpp}\cdot(1+sR_1C_1)}{s(sR_1C_1C_2+C_1+C_2)} + \frac{I_{cpi}\cdot(1+sR_1C_2)}{s(sR_1C_1C_2+C_1+C_2)}\cdot\frac{1/sC_2}{R_1+1/sC_2}$$
$$= \frac{(I_{cpp}+I_{cpi})\left(1+sR_1C_1\dfrac{I_{cpp}}{I_{cpp}+I_{cpi}}\right)}{s(sR_1C_1C_2+C_1+C_2)} \tag{3.71}$$

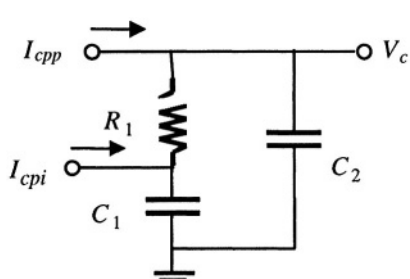


Figure 3-16. Speed-up mode with integration path

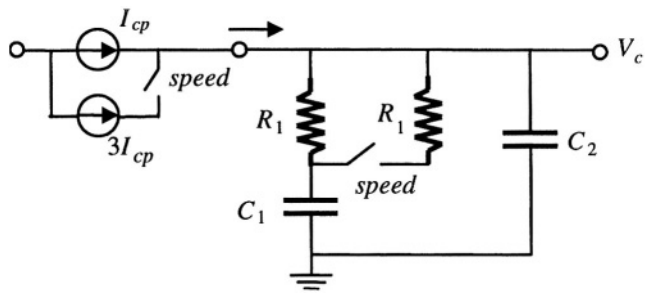


Figure 3-17. Speed-up mode with enlarged loop bandwidth

The zero and loop gain are increased by a factor of $(1+I_{cpi}/I_{cpp})$, while the poles are not changed in the speed-up mode. Thus, the loop stability is unchanged in speed-up mode.

As depicted in Fig. 3-17, another speed-up mode is to increase charge-pump current by a factor of 4 $(I_{cp} \rightarrow 4 \times I_{cp})$, while reducing the shunt resistance by a factor of 2 $(R_1 \rightarrow 0.5 \times R_1)$. So the PLL open-loop cross-zero frequency, the pole and zero $(1/R_1C_1$ and $1/R_1C_2)$ are all increased by a factor of 2. The loop stability is unaffected. The problem associated with this and the previous fast-locking approaches is the disturbance of the VCO tuning voltage at the moment the current is switched from high to low.

For the automatic switching between the speed-up mode and normal mode operation, we can either use lock-detection circuit to control the mode switching or use a programmable counter to control the speed-up mode operation time after each channel switching.

Adaptive control of the charge-pump current and the resistor in the loop filter, which is the output resistance of the regulating amplifier in the dual-path loop filter, is used in [21]. An adaptive active loop filter is used in [22], lock-detection circuit is used to control the transconductance of the OTA's (operational transconductance amplifier) used in the active loop filter to vary the loop bandwidth. An optimum gear-shifting algorithm in the sense of MMSE (minimum-mean-square-error) criterion was proposed in [23]. The adaptive control is achieved by means of changing the charge-pump current, which affects the PLL loop gain, while keeping the loop stable. But this idea is too academic to be worthwhile and practical. An analog adaptive scheme based on the phase error at PFD was used in [24], where the PLL loop bandwidth increases with the phase error.

Instead of using lock-detection circuit to control the adaptive operation mode switching, a frequency difference detector [25] or discriminator-aided phase detector (DAPD) [26] can be used to control the increasing of charge-pump current and the decreasing of the loop resistance for a fast lock.

To avoid the switching of charge-pump current and loop components, a fast locking PLL with two loops working in parallel was design in [13]. The

wide-band loop is active only during tuning of the radio, which is adaptively controlled by a dead-zone block.

To break the limitation of loop bandwidth less than 1/10 of reference frequency in the charge-pump PLL, adaptive change of reference frequency was proposed in [27] and [11]. In [27] one large reference frequency is employed, and in [11] a series of reference frequencies are used with the help of a digital frequency difference detector (DFDD) [28] to control the shifting among several gears.

3.2.2 VCO pre-tuning

The pre-tuning of VCO oscillating frequency, through selecting capacitance/inductance or setting control voltage can be implemented by presetting its control voltage (through a DAC) or switching the oscillation band (in case of multi-band VCO). A fast frequency-switching scheme using a switched-capacitor array to directly change the VCO oscillating frequency was implemented in [29]. As shown in Fig. 3-18, it actually uses a multi-band VCO and channel selection is directly mapped to VCO frequency-band selection.

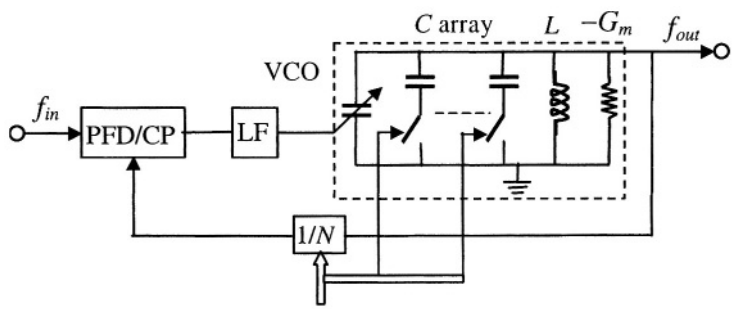


Figure 3-18. Fast-locking with multi-band VCO

3.3 Discrete-time analysis and nonlinear modeling

3.3.1 *z*-domain transfer function and stability analysis

Although the linear continuous-time *s*-domain model is good for phase (noise) analysis in the locked state, there are some features arising from the actual discrete operation that need attention [1], [30], [31]. The primary features are loop stability, VCO control-voltage ripple, and loop transfer functions etc. These features are caused by the granularity effects, *z*-domain analysis gives more accurate results of above features. As derived in [1], the transimpedance of the third-order loop filter (see 3.16) is:

$$Z(s)=\frac{b-1}{b}\cdot\frac{1+s/\omega_z}{sC_1(1+s/\omega_z/b)} \tag{3.72}$$

The z-domain analysis based on linearized approximate difference equations gives the following stability requirement:

$$K/\omega_z<\frac{4(1+a)}{\frac{2\pi(b-1)}{b\omega_{ref}/\omega_z}\left[\frac{2\pi(1+a)}{\omega_{ref}/\omega_z}+\frac{2(1-a)(b-1)}{b}\right]} \tag{3.73}$$

where $a=\exp\left(-\frac{2\pi b}{\omega_{ref}/\omega_z}\right)$ and ω_{ref} is the PLL reference angular frequency.

For a second-order charge-pump PLL, that is, with C_2 omitted in the loop filter, the loop stability requirement is:

$$K/\omega_z<\frac{1}{\frac{\pi}{\omega_{ref}/\omega_z}\left(1+\frac{\pi}{\omega_{ref}/\omega_z}\right)} \tag{3.74}$$

which is equivalent to:

$$\omega_n<\frac{\omega_{ref}}{\sqrt{\pi(\omega_{ref}/\omega_z+\pi)}} \tag{3.75}$$

Equation (3.75) leads to the well-known rule of thumb in the CP-PLL design, that is, the loop bandwidth should be less than 1/10 of the reference frequency for loop stability. More discussions on the loop stability can be found in the Appendix.

In [30], the impulse-invariant transformation from s to z is used for the z-domain discrete model of the second-order CP-PLL, and the jitter transfer function in z-domain is proved to be more accurate. Furthermore, the discrete nonlinear analysis of the second-order CP-PLL was made in [31], where the stability limit and the charge-pump/VCO overload limit partly due to the control voltage ripple were derived.

3.3.2 Nonlinear dynamic behavior modeling

If the input phase error is out of the range of $-2\pi \sim 2\pi$, the PFD has a nonlinear phase detection characteristic. Thus, the nonlinear PLL modeling and simulation is used to investigate the dynamic characteristics of a PLL, such as the accurate channel switching time, control voltage overshoot, charge-pump or VCO overloads, etc.

There are three memory blocks in the PLL, the PFD, the loop filter and the VCO. States are needed to record the output level of PFD, the voltage stored on the capacitors of the loop filter and the output phase of the VCO. Thus, the number of states is one more than the order of the PLL. Difference equations are used to update the states during the iterations.

With a set of nonlinear autonomous difference equations [31], or event-driven model non-autonomous difference equations [32] plus some techniques for enhancing simulation speed [33], we can program our own PLL simulators [34], [35]. In the event-driven model, time between two iterations is not constant and may vary from one iteration to the other. By events we mean the rising (or falling) edges of the input and feedback signals and overloads.

The other PLL modeling alternative is to build the behavioral macro-model of each block and use existing simulation tools, such as Spice, HSpice, Spectre, Spectre HDL, Verilog-A, Simulink, etc [36]-[40].

3.4 Design example: 2.4*GHz* integer-N PLL for Bluetooth

Bluetooth is a short-range (10~100 *meters*) wireless data communication standard. It operates in the 2.4*GHz* Industrial Scientific Medicine (ISM) band. Specifications for the 2.4*GHz* frequency synthesizer for Bluetooth receiver [41]-[51] are listed in Table 3-4.

Table 3-4. Specifications of 2.4GHz Bluetooth synthesizer

Frequency range	2.400~2.478*GHz* (2*MHz* IF receiver)
Channel spacing	1*MHz*
Frequency resolution	1*MHz*
Settling time	<200μs
Phase noise	<-124*dBc/Hz* @ 3*MHz*
Spur level	<-60*dBc* @ 1*MHz*

The design procedure of an integer-N PLL frequency synthesizer for Bluetooth receivers is as follows.

Step 1: VCO design. From the specified output frequency range and out-of-band phase noise level, design an on-chip VCO. For a process like 0.35μm CMOS process, *LC*-VCO is a good option for this application. To

cover the process variation, the VCO tuning range is designed as twice as specified, that is 2.36~2.52GHz with the center frequency of 2.44GHz. Thus the VCO tuning range is 160MHz. If we suppose the VCO tuning voltage range is 1.0V, then the average VCO conversion gain is $K_{vco} = 2\pi \times 160M \cdot rad/s$. Note that the conversion gain can be made smaller with a multi-band VCO or calibrated VCO [52]. Make sure that the VCO phase noise at 3MHz meets the specification.

Step 2: Choose the reference frequency and find the divide ratio range. The reference frequency is equal to the frequency resolution of 1MHz in the integer-N PLL synthesizer. The divide ratio range would be N = 2400~2478. Keep in mind that, the in-band PLL noise is enhanced by a factor of $20\log(N) \approx 68\,dB$.

Step 3: Loop filter design. From the settling time, calculate the minimum loop bandwidth. To achieve a settling time of $200\mu s$, the minimum loop bandwidth calculated from (3.60) is 20kHz. Here a loop bandwidth of $f_c = \omega_c/(2\pi) = 30\ kHz$, which is 50% more than the minimum value, is chosen. Note that there are also other limitations on the loop bandwidth. For example, the loop bandwidth should be less than 1/10 of the reference frequency for stability concerns. Moreover, the loop bandwidth affects the noise transfer characteristic of the PLL. To minimize the phase noise, the optimal loop bandwidth is where the high-pass VCO noise contribution is equal to the total low-pass noise contribution from the reference, PFD and charge-pump, etc.

Since the reference spur level requirement is not very stringent, a second-order passive loop filter is adopted. Choose $\omega_z = \omega_c/3$ and $\omega_{p2} = 3\omega_c$, that is, $f_z = \omega_z/(2\pi) = 10\ kHz$ and $f_{p2} = \omega_{p2}/(2\pi) = 90\ kHz$. Therefore, the phase margin calculated from (3.20) is $\phi_m = 53°$. A large phase margin helps cover variations of the VCO conversion gain and loop filter values to guarantee the loop stability. Now, with a charge-pump current of $I_{cp} = 100\mu A$, we can calculate the loop filter values, R_1, C_1 and C_2, from (3.5), (3.7), (3.17), and (3.23).

$$\omega_c = \frac{I_{cp} R_1 K_{vco}}{2\pi N} \cdot \frac{C_1}{C_1 + C_2} = 2\pi \times 30 \times 10^3 \quad rad/s \tag{3.76}$$

From the above equation, we can calculate $R_1 = 31.9k\Omega$. Therefore, the two capacitors are $C_1 = 1/(\omega_z R_1) = 499\,pF$ and $C_2 \approx 1/(\omega_{p2} R_1) = 62\,pF$. The design parameters of this integer-N PLL frequency synthesizer are summarized in Table 3-5.

Table 3-5. Design parameters of 2.4GHz Bluetooth synthesizer

On-chip VCO	tuning range	2.36 ~ 2.52GHz
	conversion gain	160MHz/V
	phase noise	<−124dBc/Hz @ 3MHz
Reference frequency		1MHz
Loop bandwidth		30kHz
Divide ratio		2400~2478
Charge-pump current		100μA
Passive loop filter	R_1	31.9$k\Omega$
	C_1	499pF
	C_2	62pF

Step 4: Check the phase noise transfer functions. The open-loop gain and phase margin of the PLL is plotted in Fig. 3-19 to check the loop bandwidth and phase margin. The closed-loop input and VCO noise to PLL output transfer functions are plotted in Fig. 3-20. The input and VCO noise gain is –4dB and 0dB at 3MHz, respectively. Therefore, their phase noises at 3MHz should less than –120dBc/Hz and –124dBc/Hz, respectively, to meet the synthesizer's phase noise requirement.

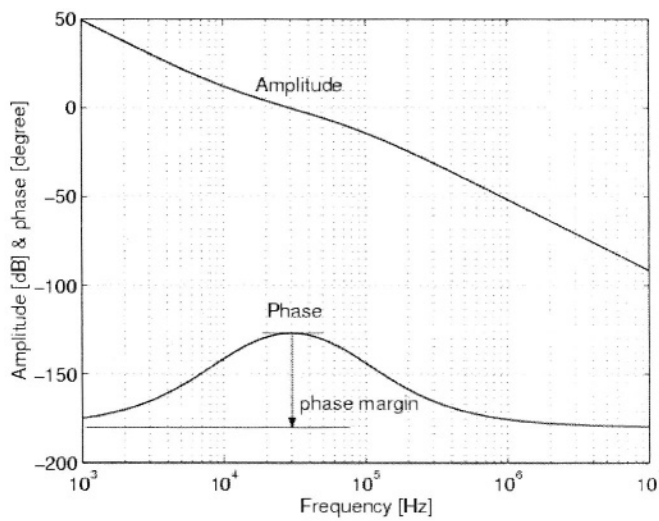


Figure 3-19. Bluetooth PLL open-loop gain and phase (margin)

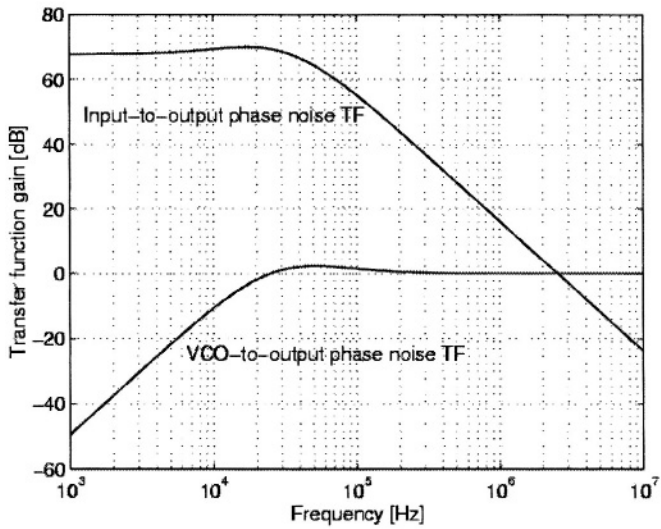


Figure 3-20. Bluetooth PLL closed-loop phase transfer function

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Chapter 4

ΣΔ FRACTIONAL-N PLL SYNTHESIZER

This chapter focuses on the analysis of ΣΔ fractional-N PLL synthesizers. The mapping of the ΣΔ quantization noise to the PLL phase noise is the main issue addressed in this chapter. A comparative study of the digital ΣΔ modulator (SDM) provides design guidelines of this block. A ΣΔ PLL example is given to show the design procedure.

4.1 ΣΔ fractional-N frequency synthesizer

The ΣΔ fractional-N PLL synthesizer compensates the fractional spur in the digital domain. The digital noise-shaping ΣΔ modulator is used to randomize the instantaneous loop divide ratio. This idea can be traced back to King [3] and Wells' [4] patents in 1980 and 1984, respectively. Fig. 4-1 shows the concept of ΣΔ fractional-N synthesizer. A digital SDM is used to control the frequency division ratio in the PLL. The instantaneous division ratio is the sum of a base integer, N_B, and the integer output of the SDM, $n_Q(t)$, so the average fractional division ratio is

$$N = N_B + \overline{n_Q(t)} \tag{4.1}$$

where $\overline{n_Q(t)}$ is the average output of SDM, and

$$\overline{n_Q(t)} = \frac{k}{M} \tag{4.2}$$

where k is the input number to the SDM, and M is the modulus used in the SDM. When the PLL reaches the steady state, its output frequency is:

$$f_{out} = N \cdot f_{ref} = \left(N_B + \frac{k}{M} \right) \cdot f_{ref} \tag{4.3}$$

and the frequency resolution would be

$$\Delta f = \frac{1}{M} f_{ref} \tag{4.4}$$

The SDM used in a synthesizer is to randomize the instantaneous division ratio and hence eliminate or suppress fractional spurs. Another advantage of the SDM is its noise-shaping characteristic. It pushes the phase noise associated with the divider from low frequencies to high frequencies. The loop filter filters out the phase noise in high frequencies.

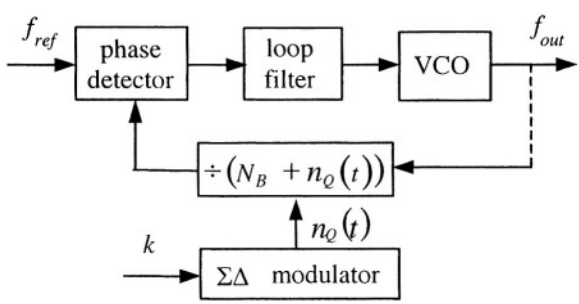


Figure 4-1. Mapping quantization noise into phase noise

4.1.1 ΣΔ quantization noise to phase noise mapping

Open-loop approximation is used to map the SDM quantization noise into PLL output phase noise [1]. This approach opens the connection between the VCO and frequency divider and assumes that the input to the frequency divider is an ideal signal with exactly the desired frequency $N \cdot f_{ref}$. So the phase noise generated by the frequency divider is

$$S_{\theta div}(f)=\left[\frac{f_{ref}\cdot Q(f)}{f\cdot N}\right]^2 \qquad rad^2/Hz \tag{4.5}$$

where $Q(f)$ is the *rms* spectral density of the ΣΔ-shaped quantization noise, and

$$Q(f)=\sqrt{\frac{1}{12f_{ref}}}\left|H_{NTF}(z)\right|_{z=e^{j2\pi f}} \tag{4.6}$$

For the L-th order MASH SDM, $Q(z)=\left(1-z^{-1}\right)^L/\sqrt{12f_{ref}}$, then (4.5) becomes

$$S_{\theta div}(f)=\frac{f_{ref}}{12(Nf)^2}\left[2\sin\left(\frac{\pi f}{f_{ref}}\right)\right]^{2L} \qquad rad^2/Hz \tag{4.7}$$

Since the phase transfer function from the divider to the PLL output is the same as the one from input to output, we can view $S_{\theta div}(f)$ as an equivalent input phase noise and use a closed-loop input-to-output phase transfer function to estimate output phase noise generated by the SDM.

$$S_{\theta out}(f)=S_{\theta div}(f)\cdot\left|H_{cl}(f)\right|^2 \qquad rad^2/Hz \tag{4.8}$$

Since within the PLL bandwidth, $H_{cl}(f)=N$, the in-band ΣΔ introduced PLL phase noise is:

$$S_{\theta out}(f)=\left[\frac{f_{ref}\cdot Q(f)}{f}\right]^2 \qquad rad^2/Hz \tag{4.9}$$

As far as the PLL loop bandwidth is not very large and the SDM introduced phase noise does not dominate the PLL output phase noise, the approximation is valid and the so-called chicken-and-egg effect is negligible.

It is interesting to mention that, the ΣΔ fractional-N PLL synthesizer revived first in [2] in 1990, but unfortunately the ΣΔ noise mapping in [2] is only valid at in-band frequencies. The assumption made in [2] is that the PLL instantaneous output frequency f_{out} is always equal to the product of the instantaneous divide ratio and the reference frequency f_{ref}:

$$f_{out}(z) = [N + Q(z)] \times f_{ref} \tag{4.10}$$

This assumption means that the PLL locking time is ideally zero. The resulting PLL output phase noise power spectrum density (PSD) derived in [2] is:

$$S_{\theta out}(f) = \frac{[2\pi Q(f)]^2}{\left|1 - z^{-1}\right|^2}, \qquad z = e^{j2\pi f / f_{ref}} \tag{4.11}$$

Only at low offset frequencies where $\left|1 - z^{-1}\right| \approx 2\pi f / f_{ref}$, the assumption might be valid and the above Equation is simplified as:

$$S_{\theta out}(f) = \left[\frac{f_{ref} Q(f)}{f}\right]^2 \qquad rad^2/Hz \tag{4.12}$$

Here we observe the agreement between (4.12) and (4.9). For the *L*-th order MASH SDM, (4.11) becomes

$$S_{\theta out}(f) = \frac{(2\pi)^2}{12 f_{ref}} \cdot \left[2\sin\left(\frac{\pi f}{f_{ref}}\right)\right]^{2(L-1)} \qquad rad^2/Hz \tag{4.13}$$

At low offset frequencies, it is simplified as:

$$S_{\theta out}(f) = \frac{(2\pi)^2}{12 f_{ref}} \cdot \left(\frac{2\pi f}{f_{ref}}\right)^{2(L-1)} \qquad rad^2/Hz \tag{4.14}$$

Moreover, the above MASH SDM phase noise is converted to the more familiar *dBc/Hz* representation in [5], but we need to be aware of the validity of this formula. We can extend formula of (4.8) to the *dBc/Hz* representation as follows.

$$S_{\theta out}(f) = 10\log\left\{\frac{f_{ref}}{12(Nf)^2} \cdot \left|H_{NTF}\left(e^{j2\pi f / f_{ref}}\right)\right|^2 \cdot \left|H_{cl}(f)\right|^2\right\} dBc/Hz \tag{4.15}$$

Within the PLL bandwidth, it is simplified as

$$S_{\theta out}(f) = 10\log\left\{\frac{f_{ref}}{12f^2}\cdot\left|H_{NTF}\left(e^{j2\pi f/f_{ref}}\right)\right|^2\right\} \quad dBc/Hz \qquad (4.16)$$

4.1.2 ΣΔ quantization noise to timing jitter mapping

Furthermore, the bandwidth limitation of a ΣΔ-PLL for a given integrated phase error θ_{rms} [*rms rad*] is derived in [6] as:

$$f_c < \left[\left(\frac{\theta_{rms}}{\sqrt{2}}\right)^2\cdot\frac{L+0.5}{(2\pi)^{2L}}\right]^{1/(2L-1)}\cdot f_{ref} \qquad (4.17)$$

where L is the order of ΣΔ modulator as defined before.

4.2 A Comparative study of digital ΣΔ modulators

ΣΔ noise shaping technique has been widely used to suppress fractional spurs in fractional-N frequency synthesizers [1], [2], [7]-[13]. There are various topologies for analog ΣΔ modulators (SDM) used in data converters. Similarly, there are different topologies of digital SDM's for synthesizers. A large number of publications on the design of analog SDM's can be found in the literature [14]-[17]. However, little attention has been paid to the design of digital ones [18], [19].

4.2.1 Design considerations

Based on observations from ΣΔ noise mapping, we have the requirements for an SDM used in PLL-FS as follows:

1) As tone-free as possible
2) Stable dc input range meets particular applications
3) Output levels as few as possible to reduce noise mixed down due to nonlinearities in phase/frequency detector, charge-pump, loop-filter, and VCO [6], and also to reduce the phase noise introduced by phase detector and charge-pump.
4) Suitable for high frequency operation
5) As simple as possible to reduce power consumption and chip area.

When the fractional divide ratio is a rational number (e.g. 0.25, 0.5, 0.75, etc), strong tones occur in the PSD of digital SDM output. Dithering technique is required to destroy these tones. Long input bit-length with LSB set to 1 is used in [2], toggling the LSB of the first accumulator once when the circuit is reset is used in [8], and high-pass filtered input dither is used in

[20]. The frequency error caused by setting LSB in [2] can be eliminated by generating random 1 and –1 sequence for LSB.

4.2.2 Four types of digital ΣΔ modulators

SDM's are basically divided into two types: single-stage and cascaded. Digital SDM's, unlike their analog counterparts, do not have any non-idealities, and when the modulator is stable, there is no overload problem. Cascaded digital modulators no longer suffer from mismatches and noise leakage from front stages, and multi-bit quantizers are free of all non-linearities, which does not exit in the digital modulator at all. For the application to fractional-N frequency synthesis, the outputs from the digital SDM can only be taken as integers. Since the input to the digital SDM is a dc level, to avoid limited cycles in the modulators, a long bit-length input has to be used. An 18-bit input with the LSB set to 1 is used in the following simulation.

2nd and 3rd-order ΣΔ modulators are practically used for fractional-N synthesizers [1], [2], [10]-[13], [18], [19]. 4th or even higher order modulators are rarely used because it is difficult to suppress the phase noise at higher frequencies by a limited order of loop filter [8]. For 2^{nd}-order modulators, the architecture is almost unanimously MASH 1-1 [10]. This part of the book concentrates on the study of different topologies of 3^{rd}-order modulators.

A. MASH 1-1-1

The MASH 1-1-1 architecture based on digital accumulators is depicted in Fig. 4-2 [2], [21]. It is very simple. The overflow from the accumulator is usually one bit, i.e., either 0 or 1. Therefore, the noise cancellation logic is of low complexity. The output has 8-levels and spreads from –3 to 4 with an average between 0 and 1. The stable input range normalized to the modulus is from 0 to 1. It is inherently stable. This topology is suitable for pipeline operation with very high clock frequencies.

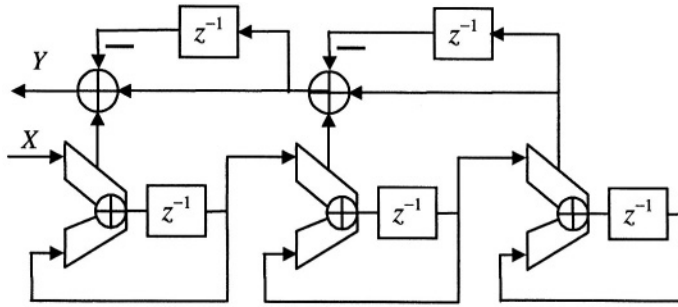
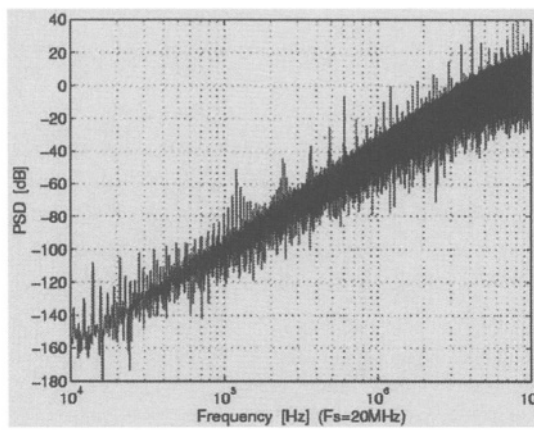
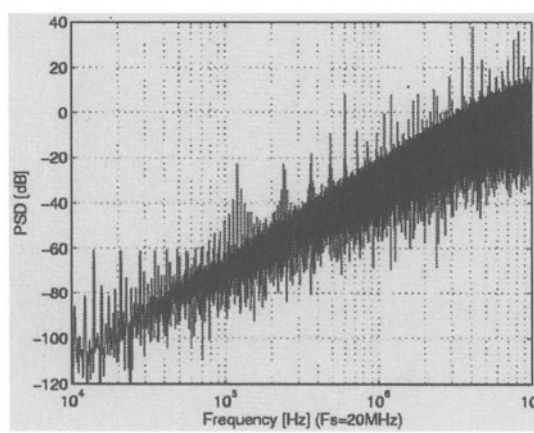


Figure 4-2. MASH 1-1-1 topology



(a) SDM output



(b) Phase error

Figure 4-3. MASH 1-1-1 simulation of PSD

The signal and quantization noise transfer function is:

$$Y(z) = X(z) \cdot z^{-3} + Q(z) \cdot \left(1 - z^{-1}\right)^3 \tag{4.18}$$

where $Q(z)$ is the quantization noise associated with the third accumulator.

The Matlab simulation of MASH 1-1-1 topology is made to evaluate its performance. The simulation was run on 2^{18} points and the clock frequency is 20MHz. Figure 4-3 shows the power spectrum density (PSD) of the SDM output and instantaneous phase error seen by the phase detector. The SDM output corresponds to instantaneous frequency, and the phase error at PFD input is the integration of the corresponding frequency. Thus, the PSD's of the SDM output and the phase error rise up $60dB/dec$ and $40dB/dec$, respectively.

Figure 4-4 shows the phase error sequence in the time domain and its distribution histogram. The phase error is normalized by a factor of $N/(2\pi)$, where N is the nominal frequency divide ratio in fractional-N synthesis. Hence, one unit of the normalized phase error equals one VCO cycle in the time domain. We observe that the output is quite tonal and the phase error spreads widely. Although the input stable range covers from 0 to 1, input levels too close to 0 or 1 will generate high-level in-band spurs at the synthesizer output [8].

To demonstrate the PLL nonlinearity effects on phase noise folding (or mixing), Fig. 4-5 shows the PSD of phase error when 2% of the charge-pump current mismatch is taken into account. With input x and output y, the nonlinear system is described as:

$$y = \begin{cases} x & x \geq 0 \\ 1.02x & x < 0 \end{cases} \tag{4.19}$$

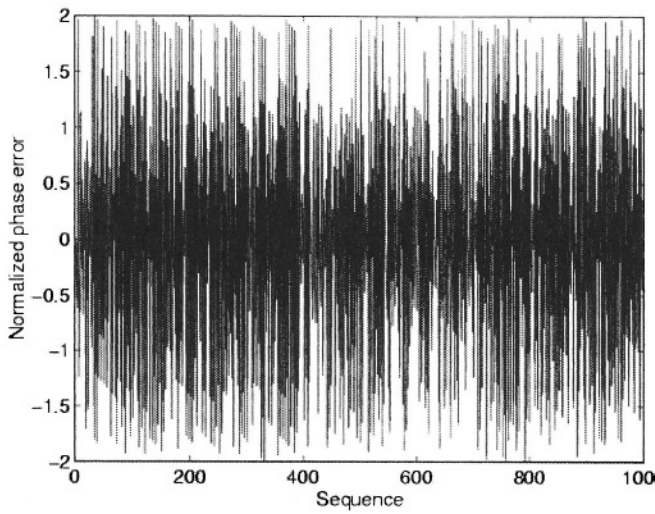
We observe that the phase error PSD below $300kHz$ flats at a level about $-45dB$.

B. MASH 1-2

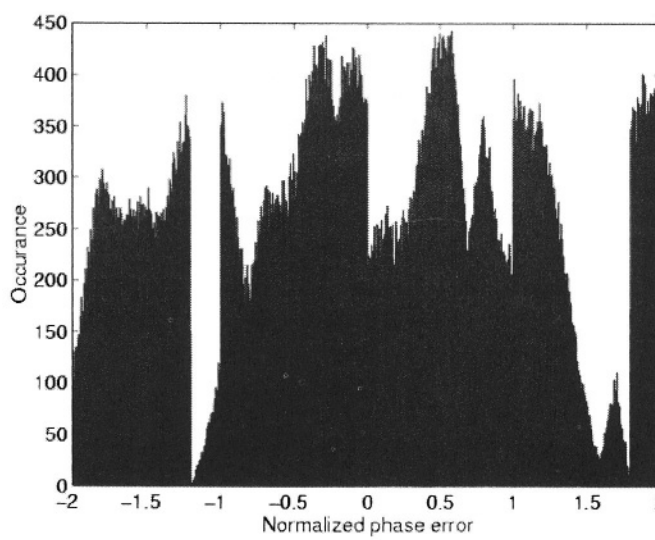
To reduce the number of output levels, MASH 1-2 as shown in Fig. 4-6 was used in [19]. The output has four levels from –1 to 2. The transfer function of this topology is:

$$Y(z) = X(z) + Q(z) \cdot \left(1 - z^{-1}\right)^3 \tag{4.20}$$

where $Q(z)$ is the quantization noise associated with the second quantizer.



(a) Sequence



(b) Distribution

Figure 4-4. MASH 1-1-1 normalized phase error

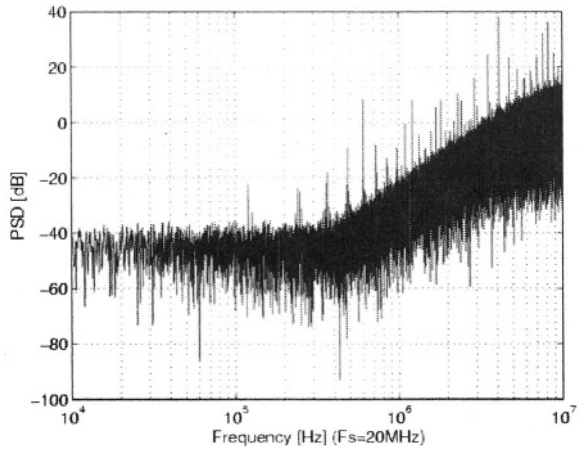


Figure 4-5. MASH 1-1-1 phase error PSD with nonlinearity

The simulation results are shown in Figs. 4-7, 4-8 and 4-9. The spurious content of the PSD is better than that of MASH 1-1-1, but the spurs in high frequencies will be mixed down to low frequencies by the non-linearity of analog circuits in the PLL. Its phase error is much more concentrated than that of MASH 1-1-1. The normalized phase error spreads between from –1 to 1, which is half of that of MASH 1-1-1. The PSD of normalized phase error flats at $-52dB$ below $200kHz$.

The big disadvantage of MASH 1-2 is that it only allows the input to operate about 75% of the whole fractional range [19]. This will limit its application in fractional-N frequency synthesizers unless multi-bit quantizers are used.

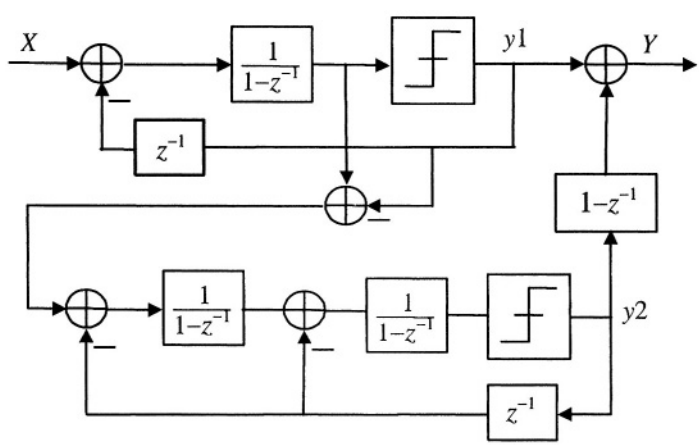
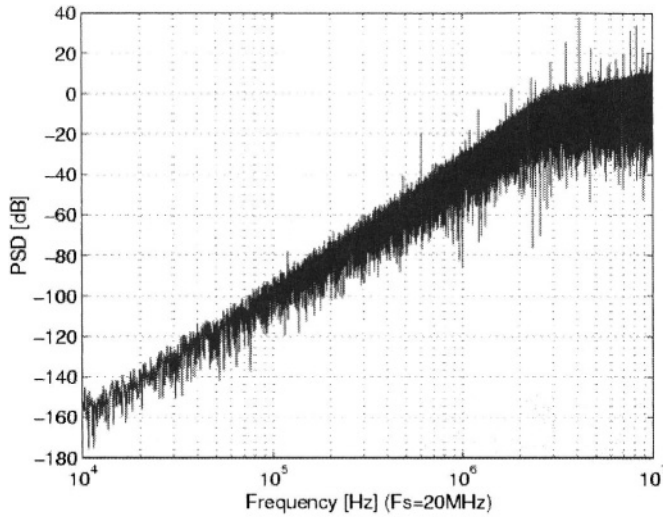
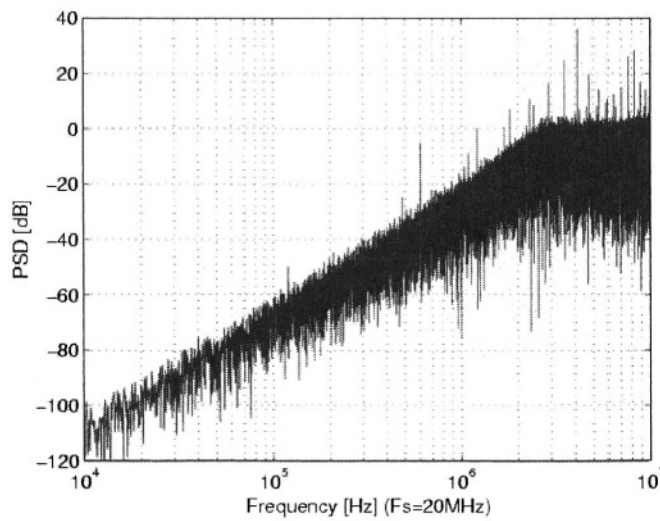


Figure 4-6. MASH 1-2 topology

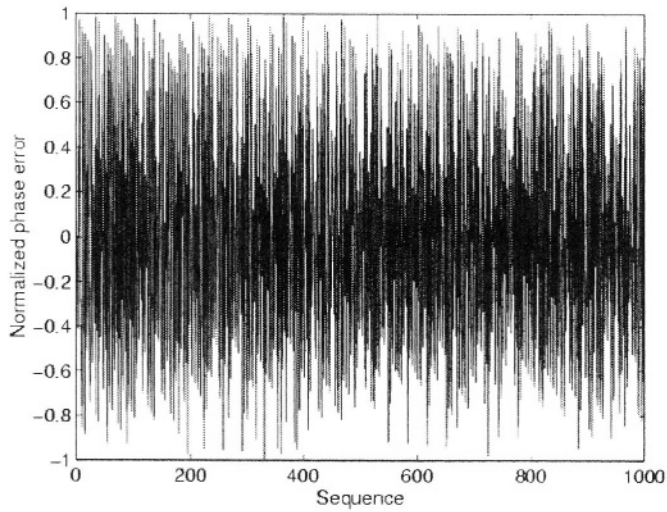


(a) SDM output

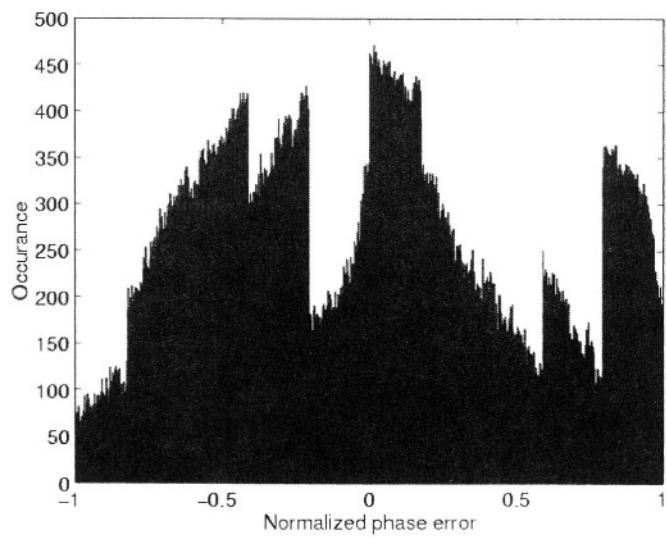


(b) Phase error

Figure 4-7. MASH 1-2 simulation of PSD



(a) Sequence



(b) Distribution

Figure 4-8. MASH 1-2 normalized phase error

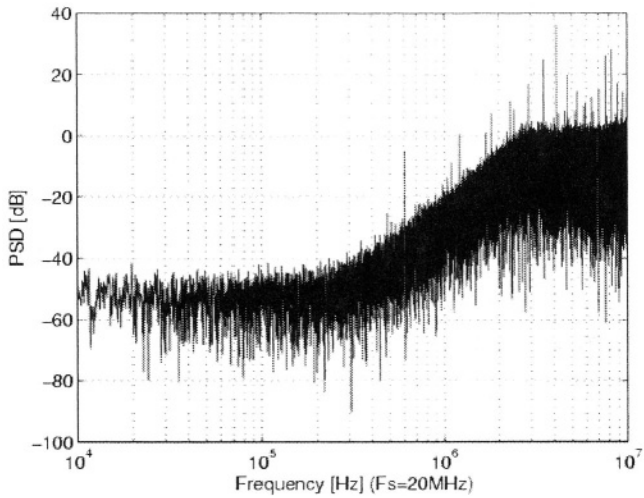


Figure 4-9. MASH 1-2 phase error PSD with nonlinearity

C. *Single-stage with multiple feedforward (FF3)*

Compared with MASH architecture, single-stage architecture has better noise shaping characteristics for dc inputs. But it is subject to instability and smaller stable input range. The latter limitation can be eliminated with a multi-bit quantizer in digital SDM's.

A modified single-loop multiple feedforward modulator used in [1] is shown in Fig. 4-10. The transfer function is:

$$Y(z) = X(z)\cdot\frac{z^{-1}\left(2-3z^{-1}+1.25z^{-2}\right)}{1-z^{-1}+0.25z^{-2}} + Q(z)\cdot\frac{\left(1-z^{-1}\right)^3}{1-z^{-1}+0.25z^{-2}} \quad (4.21)$$

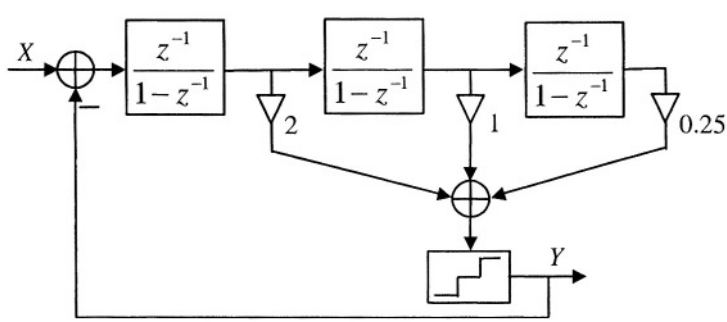
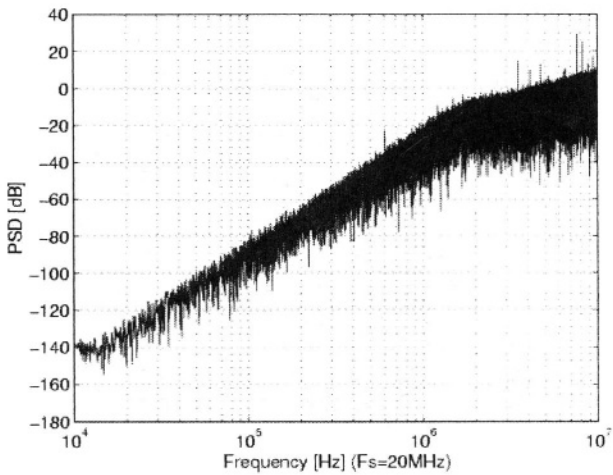
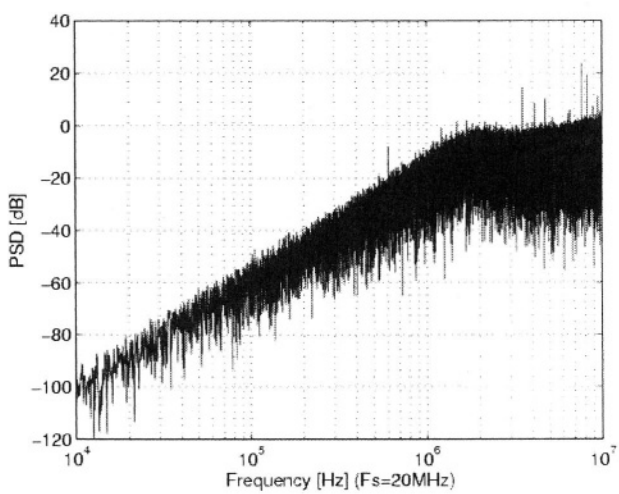


Figure 4-10. Single-stage multiple feedforward topology (FF3)

Here the quantizer output is limited to three levels: 0, 1 and 2. The feedforward branches can be truncated to reduce the circuit complexity, power and area. Simulation shows that the input stable range covers the fractional range of 0.5~1.5. As shown in Fig. 4-11, a few tones are observed in the PSD's of the SDM output and the phase error. Since the SDM output has only three levels, the phase error at the PFD input is well concentrated (see Fig. 4-12). Figure 4-13 shows the PSD of the phase error with the same nonlinearity as before. It flats at a level of –60*dB* below 100*kHz*.

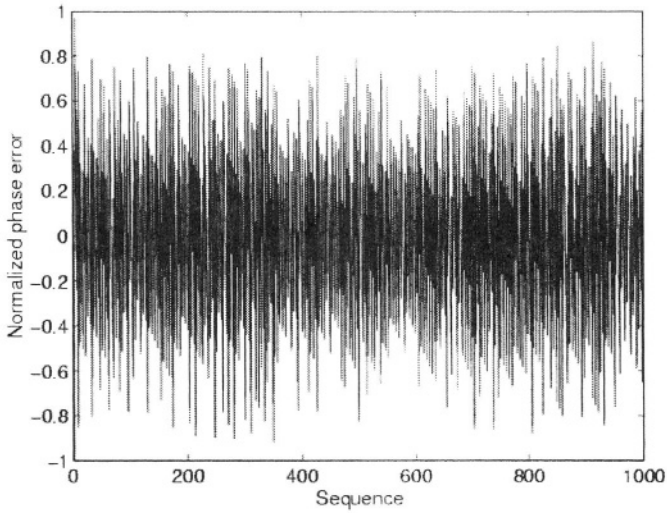


(a) SDM output

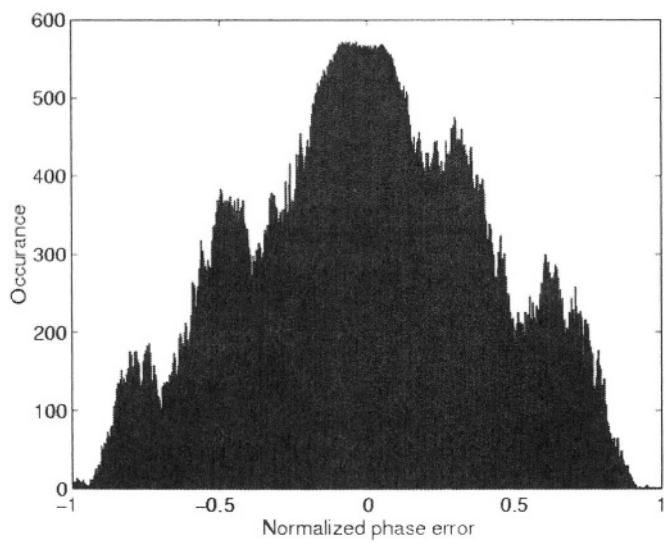


(b) Phase error

Figure 4-11. FF3 simulation of PSD



(a) Sequence



(b) Distribution

Figure 4-12. FF3 normalized phase error

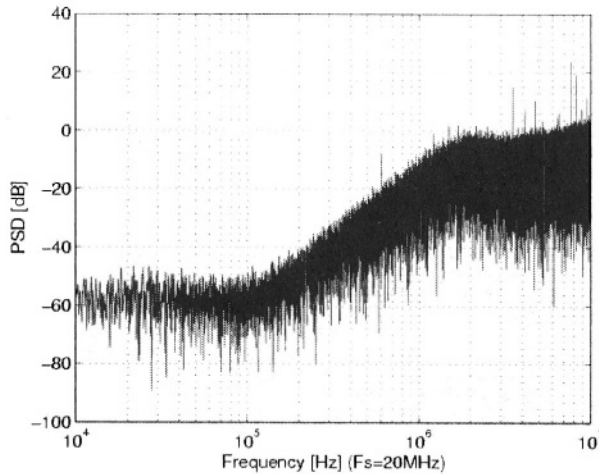


Figure 4-13. FF3 phase error PSD with nonlinearity

D. Single-stage with multiple feedback (FB3)

Another alternative of single-stage implementation considered in this book is the multi-feedback topology shown in Fig. 4-14. It is used in [13]. Its transfer function is:

$$Y(z) = X(z) \cdot z^{-1} + Q(z) \cdot \left(1 - z^{-1}\right)^3 \tag{4.22}$$

In this architecture, to obtain reasonable stable input range we have to set the number of quantization levels as many as nine, i.e., from –4 to 4. The bit-lengths of the adders before the accumulators are much shorter than the accumulators themselves, so the complexity of these adders is relatively low. Simulation shows that if we reduce the number of output levels, we have to scale the input to each accumulator and each feedback branch as indicated in [17]. In that case, the noise shaping and spurious contents are much worse. Quantization noise flattens at high frequencies and noise level at low frequencies rises.

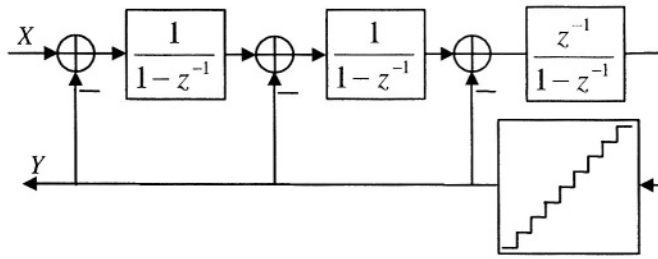
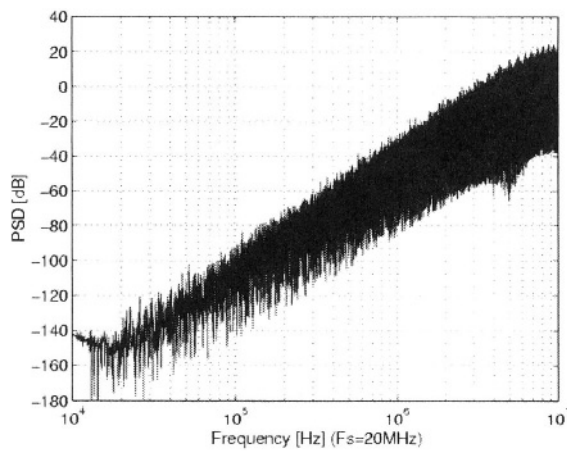
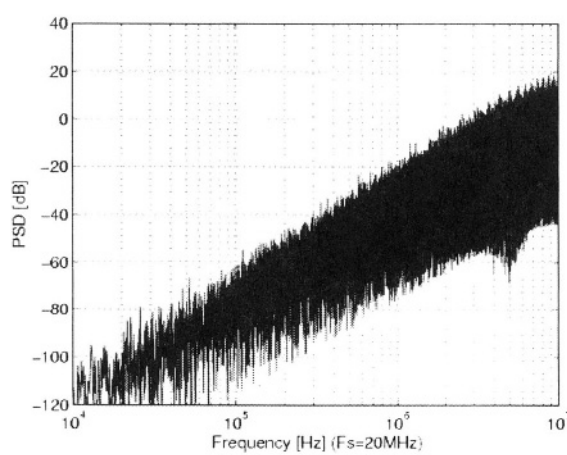


Figure 4-14. Single-stage multiple feedback topology (FB3)

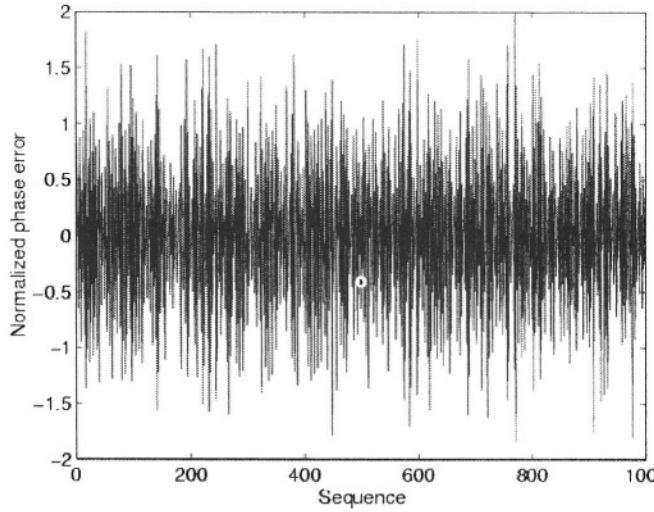


(a) SDM output

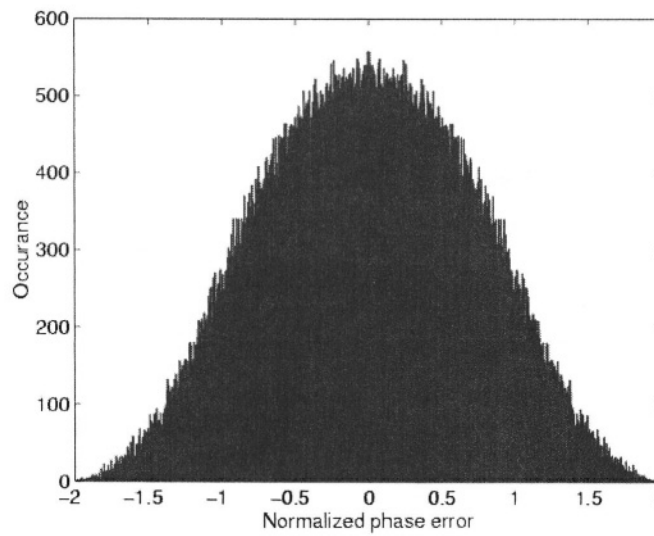


(b) Phase error

Figure 4-15. FB3 simulation of PSD



(a) Sequence



(b) Distribution

Figure 4-16. FB3 normalized phase error

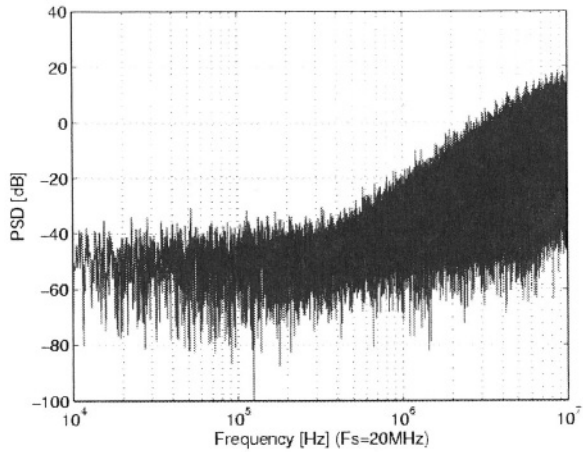


Figure 4-17. FB3 phase error PSD with nonlinearity

The simulation results shown in Fig. 4-15 reveals that we get almost tone-free spectrums of SDM output and phase error at the expense of large number of output levels. Although the quantizer in this SDM has as many as 9 levels, the number of output levels for a fixed dc input is only a few. Therefore, compared with MASH 1-1-1, which has eight output levels, the phase error (Fig. 4-16) is better concentrated. It flats at a level of $-50dB$ below $200kHz$ for the assumed nonlinearity in (4.19) (Fig. 4-17).

4.2.3 Summary of comparative study

From the simulation results of 3rd-order digital SDM's presented before, we observe that the single-stage architecture is better than the cascaded one in terms of spurious content. The more levels of the quantizer, the larger stable dc input range, better noise shaping characteristics and fewer tones. However, fewer output levels are preferred in terms of quantization noise folding and phase noise associated with charge-pump. So there is a tradeoff in choosing the number of output levels. Intuitively, if the basic division number N_B is small, fewer output levels are preferred. Note that, although for each SDM topology the simulation results vary with the dc input level, the variation is much less distinct than the difference between different topologies. Furthermore, when the fractional divide ratio approaches an integer number, the randomness of the instantaneous divide ratio disappears and strong spurs exist at the spectrum of the SDM and the PLL output [2], [6], [7].

Table 4-1 provides a concise comparison of the performances of the 4 types of digital SDM's.

Table 4-1. Performance comparison of SDM's

topology #	A	B	C	D
noise shaping	good	fair	fair	good
spurious content	many tones	some tones	a few tones	almost tone-free
stable dc input range	8 levels: 0~1	4 levels: 0.125~0.875	3 levels: 0.263~1.678	9 levels: −2.50~2.50
output levels	−3~4	−1~2	0~2	−4~4
nonlinear noise level	$-45dB$ @ $<300kHz$	$-52dB$ @ $<200kHz$	$-60dB$ @ $<100kHz$	$-50dB$ @ $<200kHz$
max clock frequency	f_{max}	$0.5f_{max}$	$\approx f_{max}$	$0.33f_{max}$
complexity / area / power	About the same, since accumulators dominate and each has 3 accumulators			

As listed in Table 4-1, the PLL nonlinearities, like the charge-pump current mismatch, significantly fold the high-pass shaped ΣΔ phase noise from high frequencies into low frequencies due to the intermodulation effect. Therefore, the PLL in-band phase noise often increases when it works in the fractional-N mode [7], [22], [23]. If a phase offset seen by PFD is intentionally introduced to make the PFD phase error always either positive or negative, the conversion from ΣΔ phase error to charge-pump output charge will be much more linear, and the noise folding due to charge-pump mismatch can be alleviated [23].

Figure 4-18 depicts the above mentioned linearization technique by adding an offset current in parallel with the charge-pump. Suppose the minimum turn-on time of charge-pump switches is $1ns$, and the charge current 2% more than the discharge current as shown in Fig. 4-19 (a). In the locked-state and without the offset current, the charge and discharge current pulse-widths are $1ns$ and $1.02ns$, respectively, when there is no noise in the PLL. However, if we take the ΣΔ quantization noise only into account, the scenario would be different. Positive and negative PFD phase errors increase the charge and discharge current pulse widths, respectively. As illustrated in Fig. 4-19 (b), the mapping of phase error into net charge is nonlinear due to current mismatch. As shown in Fig. 4-20 (a), the offset current introduces a phase offset in the lock state [23]. Suppose the reference period is $T_{ref} = 50ns$, an offset current $I_{offset} = 0.0208I_{cp}$ is required to make the PFD input offset equal to $1ns$. If the ΣΔ phase error is less than $1ns$, it only changes the pulse duration of charge current and the discharge current pulse duration is always equal to the minimum turn-on time of $1ns$. Therefore, as shown in Fig. 4-20 (b), with an intentionally introduced PFD phase offset larger than the instantaneous ΣΔ phase error, the mapping of phase error into net charge becomes linear.

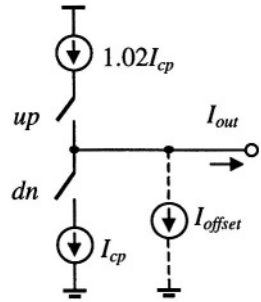
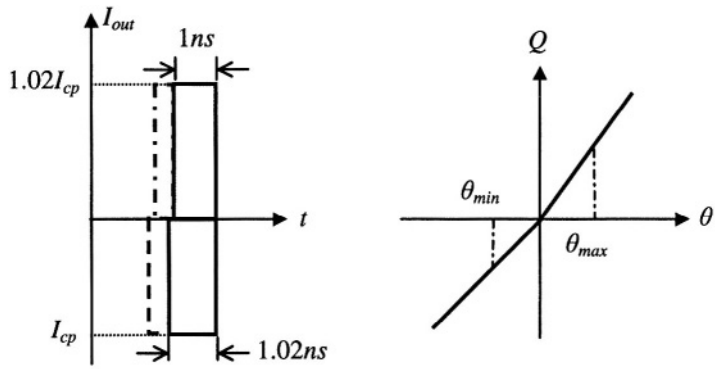
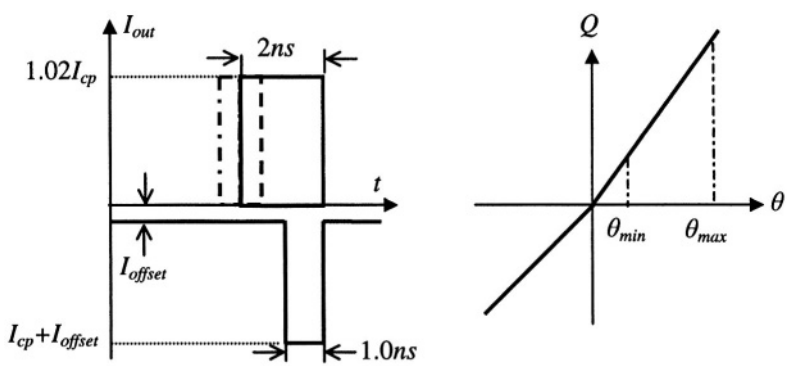


Figure 4-18. Charge-pump with current mismatch



(a) Output current pulses (b) Phase to charge conversion

Figure 4-19. Charge-pump mismatch and nonlinearity



(a) Output current pulses (b) Phase to charge conversion

Figure 4-20. Charge-pump with offset current for linearity

4.3 Other applications of ΣΔ-PLL

4.3.1 Direct digital modulation

Since the ΣΔ-PLL can generate high-resolution frequency output controlled by the programmable fractional divide ratio, it can be employed as a direct digital phase/frequency modulator in transmitters [8]-[11], [24]-[28]. It eliminates the DAC, mixer and filter in traditional transmitters [29], [30]. Note that the digital modulation in [9] is based on a variation of ΣΔ-PLL synthesizer using ΣΔ frequency discriminator (ΣΔFD) [31]-[33]. Since the PLL loop bandwidth is a limitation on the modulation date rate, a compensation filter is used to greatly enhance the data transmission bandwidth [9], [10]. The direct digital modulation diagram in [9] and [10] are shown in Fig. 4-21 and Fig. 4-22, respectively.

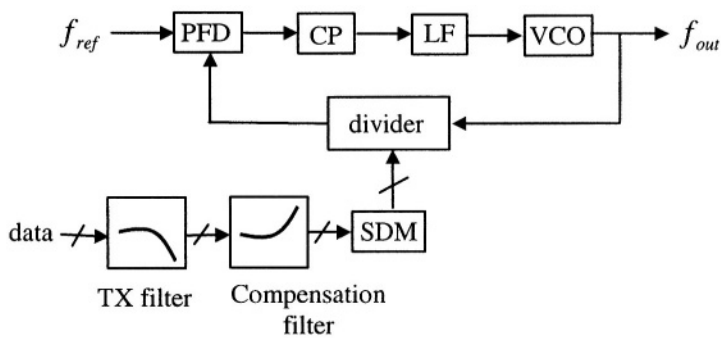


Figure 4-21. Direct digital modulation of ΣΔ-PLL synthesizer

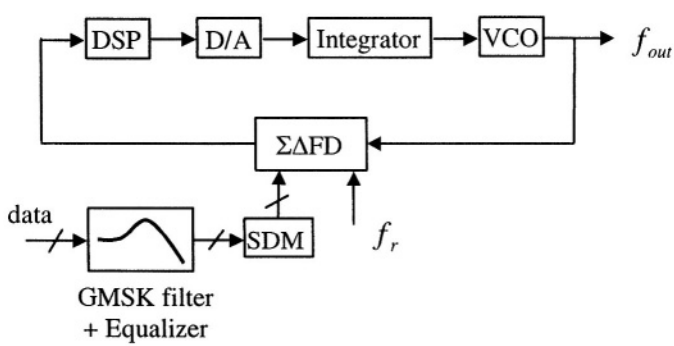


Figure 4-22. Direct digital modulation of ΣΔFD-based synthesizer

A survey of ΣΔ-PLL (or ΣΔFD) for direct digital modulation reported in the literature is summarized in Table 4-2.

Table 4-2. A survey of ΣΔ-PLL for digital modulation

PLL (SD)	[8]	[9]	[10]	[11]	[27]
ref. freq. [*Hz*]	20*M*	23*M*	20*M*	48*M*	26*M*
output freq. [*Hz*]	915*M*	1.9*G*	1.8*G*	2.4*G*	915*M*/1.8*G*
loop BW [*Hz*]	100*k*	30*k*	84*k*	700*k*	135*k*
modulation	GMSK	GMSK	GFSK	GFSK	GMSK
topology	mash-4	mash-2	mash-2	3rd, 3b	mash-3
data rate [*bit/s*]	62.5*k*	271*k* (max 1*M*)	2.5*M*	2*M*	271*k*

4.3.2 Frequency-to-digital conversion

PLL frequency discriminator based on ΣΔ noise shaping of quantization noise can be found in [34], [35]. Figure 4-23 shows the simplified block diagram of the second-order ΣΔ frequency discriminator (ΣΔFD) in [35]. The quantization noise is high-pass shaped in the same way as ΣΔ analog-to-digital converter (ADC).

Another version of frequency-to-digital converter proposed by Galton *et al.* [36]-[39] is shown in Fig. 4-24. Also, an analog-input digital PLL (ADPLL) employing ΣΔ noise shaping in [40] is claimed to be good for frequency or phase demodulation.

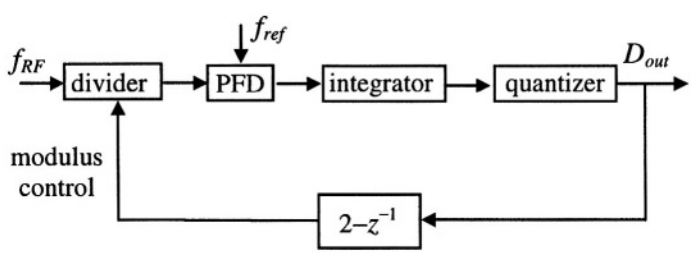


Figure 4-23. A second-order ΣΔ frequency discriminator

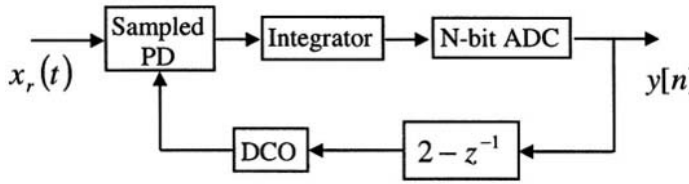


Figure 4-24. A second-order ΣΔ frequency-to-digital converter

4.4 Modeling and simulation of ΣΔ-PLL

A straightforward modeling approach for ΣΔ-PLL is developed in [41]. As in [42], which presents a *z*-domain model of PLL, one important idea is to use an impulse sequence to approximate a width-modulated pulse sequence in modeling the PFD/CP output, so the loop filter output can be easily calculated using its impulse response and no difference equation is needed for iteration. Note that, this approximation is valid only when the PLL is in steady or near-steady state where the pulse width of charge-pump output current is much less than the reference period.

Denote the *j*-th phase of the reference and divider output as $\theta_{ref}[j]$ and $\theta_{div}[j]$, respectively. And the period of the fixed reference is T_{ref}. Then the output pulse width of the *j*-th PFD output is:

$$\Delta t_j = \frac{T_{ref}}{2\pi}\left(\theta_{ref}[j] - \theta_{div}[j]\right) \tag{4.23}$$

Using an impulse sequence approximation, the PFD output is:

$$E(t) \approx \sum_{j=-\infty}^{\infty} \Delta t_j \delta\left(t - jT_{ref}\right) \tag{4.24}$$

The charge pump output is the PFD output scaled by the charge pump current I_{cp}:

$$I = I_{cp} \cdot E(t) \tag{4.25}$$

Denote the impulse response of the loop filter as $h_{lf}(t)$, then its output voltage can be easily calculated as:

$$V_c(t) = E(t) \cdot h_{lf}(t) \tag{4.26}$$

Denote the VCO conversion gain as K_{vco}, and $V_c(t)$ is the VCO control voltage deviation from the nominal value that generates the nominal VCO output frequency f_{nom}. The VCO output phase deviation is:

$$\theta_{out}(t) = \int K_{vco} V_c(t) dt \tag{4.27}$$

Define the instantaneous divide ratio as $N_{st}[j]$, and its deviation from the nominal fractional divider ratio N as $n[k] = N_{st}[k] - N$. The divider samples the VCO continuous output phase as $\theta_{out}(j) = \theta_{out}(t_j) \approx \theta_{out}(t_j + \Delta t_j)$. As such, the PFD output pulse width is:

$$\Delta t_j = \frac{T_{ref}}{2\pi} \frac{1}{N} \left(2\pi \sum_{m=-\infty}^{j} n[m-1] - \theta_{out}[j] \right) \tag{4.28}$$

Assuming $\theta_{ref}[j] = 0$, we have

$$\theta_{div}[j] = \frac{1}{N} \left(-2\pi \sum_{m=-\infty}^{j} n[m-1] + \theta_{out}[j] \right) \tag{4.29}$$

The entire time-domain model of **ΣΔ-PLL** is shown in Fig. 4-25. Note that this model is accurate for steady or near-steady state PLL analysis rather than dynamic behavior analysis due to the impulse approximation of the charge-pump output. Furthermore, phenomena such as overloads and nonlinearities need to be taken into account for the dynamic behavior modeling.

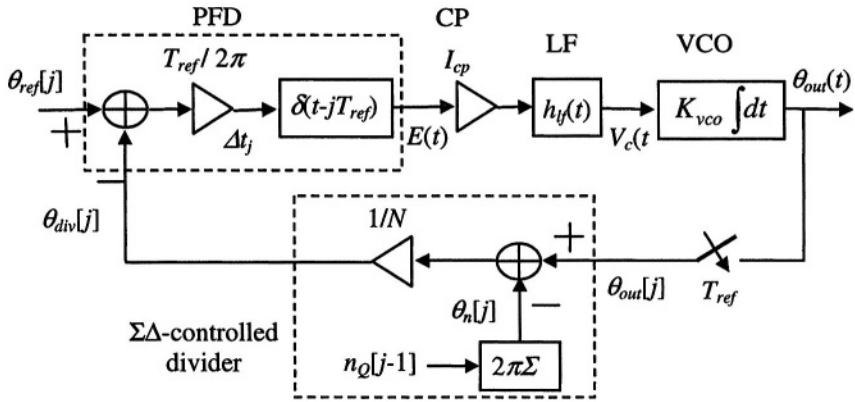


Figure 4-25. Time domain model of ΣΔ-PLL

The frequency domain PLL model in [41] is similar to the one shown in Fig. 4-26. It is the same as the well-known linear phase (noise) model as addressed in Chapter 3. The treatment of ΣΔ phase noise is the same as the mapping methods proposed by Riley *et al.* in [1]. Examples of ΣΔ-PLL phase noise calculation and simulation can be found in [7], [41], and [43], which are all claimed to be in good agreement with measurement results.

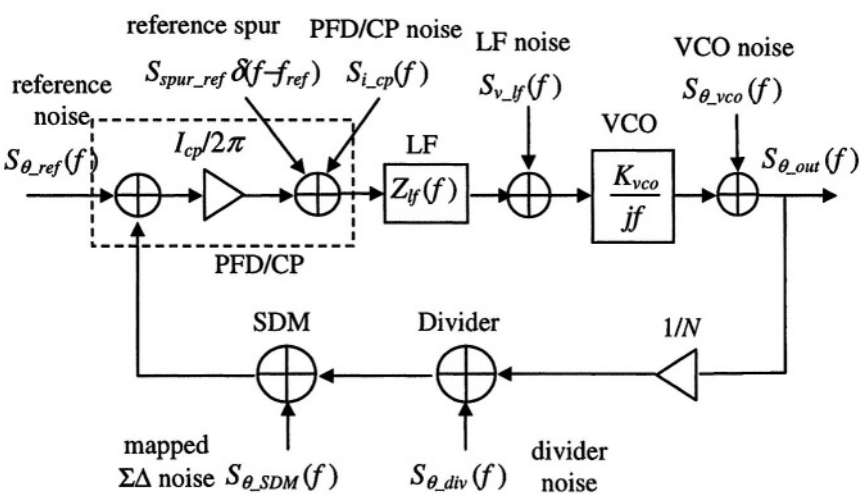


Figure 4-26. Frequency domain model of ΣΔ-PLL

4.5 Design example: 900MHz ΣΔ-PLL for GSM

GSM is one of the most popular wireless communication standards for cellular phones in the world. The GSM receiver has a RF input frequency range of 935.2~959.8MHz. Specifications for the frequency synthesizer for GSM receiver are summarized in Table 4-3 [44]-[46].

Table 4-3. Specifications of 900MHz GSM synthesizer

frequency range	865.2~889.8MHz (70MHz IF receiver)
channel spacing	200kHz
frequency resolution	200kHz
settling time	<577μs
phase noise	<–121dBc/Hz @ 600kHz
spur level	<–68dBc @ 600kHz <–88dBc @ 3MHz

The design procedure of a ΣΔ fractional-N PLL frequency synthesizer for the GSM application is as follows. Here we use the MASH 1-1-1 SDM.

Step 1: VCO design. From the specified output frequency range and stringent out-of-band phase noise level, design an on-chip VCO. For a process like $0.35\mu m$ CMOS process, *LC*-VCO is a good option for this application. For example, a 3V, 9mW, 0.84 ~ 1.03GHz, $0.4\mu m$ CMOS *LC*-VCO with –123.5dBc/Hz at 600kHz is reported in [47]. To cover the process variation, the VCO tuning range is simply designed as twice as specified here, that is, 852~902MHz with the center frequency of 877MHz. Suppose the VCO tuning voltage range is 1.0V, then the average VCO conversion gain is $K_{vco} = 2\pi \times 50M \cdot rad/s$. Make sure that the VCO phase noise at 600kHz be less than – 121dBc/Hz.

Step 2: Choose the reference frequency and find the divide ratio range. Unlike integer-N PLL, the reference frequency of fractional-N PLL can be much larger than the frequency resolution (200kHz). With a reference frequency of 13MHz, the divide ratio range would be 66.54 ~ 68.46. The MASH 1-1-1 SDM output range is –3 ~ 4 for input fractional number from 0 to 1. Therefore, the programmable divider must be able to implement divide ratio range of N = 63 ~ 71. The PLL in-band noise enhancement is $20\log(N) \approx 37\,dB$.

Step 3: Loop filter design. From the settling time of $577\mu s$, the minimum loop bandwidth calculated from (3.60) is 6.9kHz. A loop bandwidth of $f_c = 50kHz$ is adopted to take advantage of the fractional-N architecture. A large loop bandwidth helps reduce the loop filter capacitance and suppress the in-band VCO noise. However, the suppression of the ΣΔ noise imposes an upper constraint on the loop bandwidth.

To suppress ΣΔ noise at high frequencies and reduce the reference spur, a third-order passive loop filter is used. Choose $f_z = f_c/3 = 16.7kHz$, $f_{p2} = 3f_c = 150kHz$ and $f_{p3} = 15f_c = 750kHz$. Therefore, the phase margin calculated from (3.36) is $\phi_m = 49°$. Now, with a charge-pump current of $I_{cp} = 20\mu A$, we can calculate the resistance and capacitance values in the loop filter. The PLL bandwidth (see 3.37) is:

$$\omega_c = \frac{I_{cp} R_1 K_{vco}}{2\pi N} \cdot \frac{C_1}{C_1 + C_2 + C_3} = 2\pi \times 50 \times 10^3 \quad rad/s \qquad (4.30)$$

From this equation, we can calculate $R_1 = 24k\Omega$. Therefore, the largest capacitor is $C_1 = 1/(\omega_z R_1) = 397pF$. $C_2 + C_2 \approx 1/(\omega_{p2} R_1) = 44pF$ (see 3.33). Let $C_2 = 24pF$, then $C_3 = 20pF$. Again, from $R_3 \approx 1/(\omega_{p3} C_2 C_3 / (C_2 + C_3))$ (see 3.34), we have $R_3 = 19k\Omega$. The design parameters of this integer-N PLL frequency synthesizer are summarized in Table 4-4.

Table 4-4. Design parameters of 900*MHz* GSM synthesizer

on-chip VCO	tuning range	852 ~ 902*MHz*
	conversion gain	50*MHz/V*
	phase noise	<–121*dBc/Hz* @ 600*kHz*
reference frequency		13*MHz*
loop bandwidth		50*kHz*
ΣΔ modulator topology		Mash 1-1-1
divide ratio		63 ~ 71
charge-pump current		20μA
passive loop filter	R_1	24*kΩ*
	C_1	397*pF*
	C_2	24*pF*
	R_3	19*kΩ*
	C_3	20*pF*

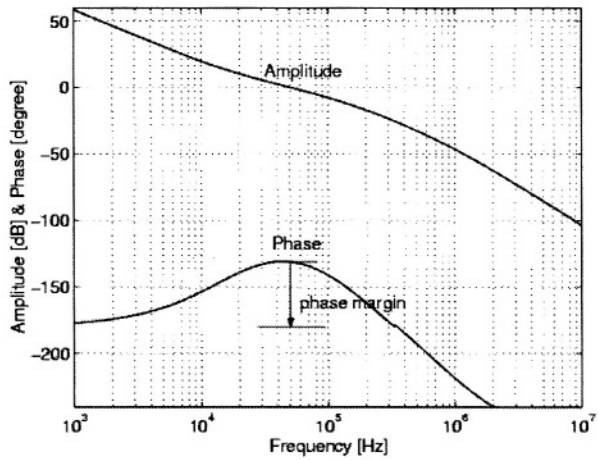


Figure 4-27. GSM PLL open-loop gain and phase (margin)

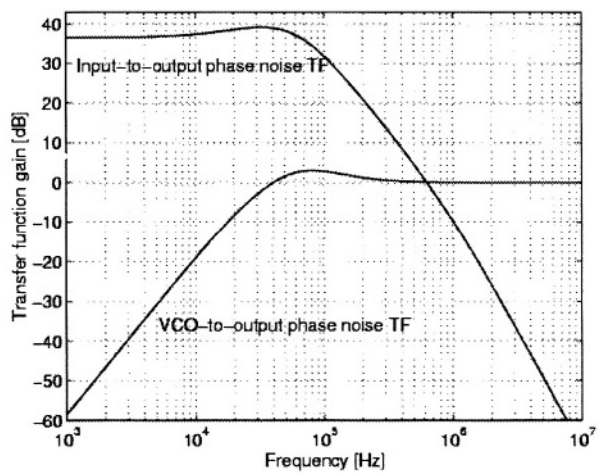


Figure 4-28. GSM PLL closed-loop phase transfer function

Step 4: The open-loop gain and phase margin of the PLL is plotted in Fig. 4-27 to check the loop bandwidth and phase margin. The closed-loop input and VCO noise to PLL output transfer functions are plotted in Fig. 4-28. For example, both phase (noise) transfer function gains at $600kHz$ offset are about $0dB$.

Step 5: Plot and check the **ΣΔ** introduced phase noise. From (4.7), the equivalent divider phase noise introduced by the MASH 1-1-1 **ΣΔ** modulator is plotted in Fig. 4-29. We observe that the input-referred **ΣΔ** phase noise level at $1MHz$ is about $-115dBc/Hz$.

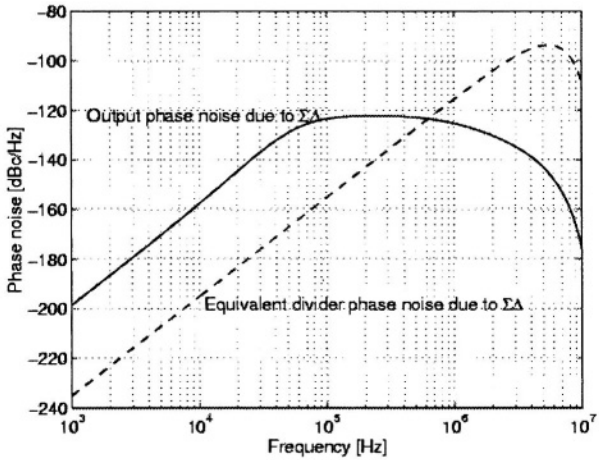


Figure 4-29. GSM PLL input-referred SD phase noise

The PLL output phase noise introduced by the ΣΔ modulator is also plotted in Fig. 4-29. It shows that the output-referred ΣΔ phase noise at $600kHz$ is about $-123dBc/Hz$. It indicates that a smaller loop bandwidth is preferred to further suppress the ΣΔ phase noise.

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Chapter 5

ENHANCED PHASE SWITCHING PRESCALER

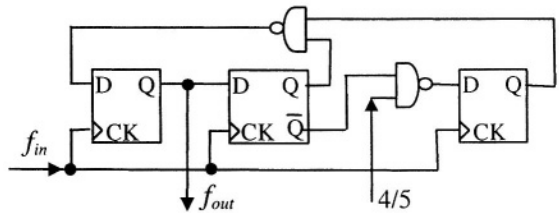
This chapter is dedicated to the prescaler design. Conversional prescaler design techniques are overviewed, followed by the enhanced high-speed, low-power and robust phase-switching prescaler. The analysis and design of this new prescaler are elaborated in great detail.

5.1 Prescaler architecture

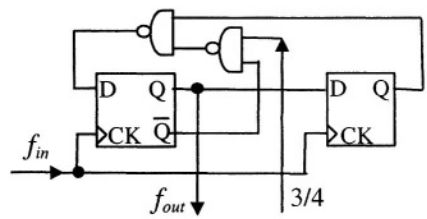
The prescaler is included in the loop of the frequency synthesizer as shown in Fig. 3-1. It is in fact a high-speed frequency divider. For example, in a 2.4-*GHz* PLL in 0.35μm CMOS, the *LC*-VCO oscillates at 2A*GHz,* but the frequency divider implemented with standard digital cells can only work at a frequency less than 400*MHz*. To bridge this speed gap, a specially designed high-speed frequency divider is needed. The prescaler is usually dual-modulus or multi-modulus in a tunable PLL.

5.1.1 Conventional prescaler

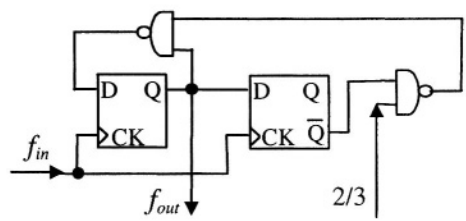
The conventional dual-modulus prescaler [1]-[7] uses a dual-modulus synchronous counter as its input stage. Figure 5-1 shows the divide-by-4/5, divide-by-3/4 and divide-by-2/3 synchronous counters for the conventional prescaler. The flip-flops in these counters are usually specially designed high-speed ones.



(a) Divide-by-4/5



(b) Divide-by-3/4



(c) Divide-by-2/3

Figure 5-1. Synchronous counters for conventional prescaler

Figure 5-2 depicts a conventional divide-by-32/33 prescaler. It consists of a divide-by-4/5 synchronous counter and a divide-by-8 asynchronous counter. When division mode control (MC) input is high, the prescaler's divide ratio is 32. Otherwise, the divide ratio is 33.

For this prescaler, the three flip-flops used in the input stage work at the highest input frequency and therefore consume significant power. Furthermore, compared with an asynchronous ÷2 divider based on the same flip-flop, this synchronous counter can only work at much lower input frequency due to the additional gates in the feedback loop. The divide-by-2/3 or divide-by-3/4 counter itself consumes less power than the divide-by-4/5 one, but the following stages have to operate at higher frequencies and the timing of the divide-by-2/3 or divide-by-3/4 selection is more critical [1].

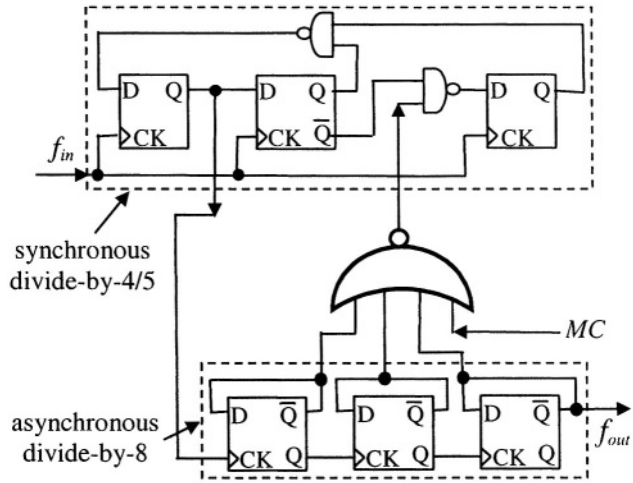


Figure 5-2. Conventional divide-by-32/33 prescaler

As shown in Figure 3-1, the dual-modulus *(P/P+1)* prescaler is combined with two programmable counters M and A, which are implemented with standard digital cells, to realize a programmable divide ratio of *MP+A*. The limitation of this scheme is that the lower limit of the continuous divide ratio is *P*(*P*–1). To eliminate this limit, the multi-modulus prescaler/divider is often used to provide more flexible divide ratios. One widely used scheme is cascading a number of ÷2/3 stages [8], [9]. For example, nine stages are connected in cascade in [8], and any divide ratio between 512 and 1024 can be realized by external control signal. Sometimes the multi-modulus prescaler/divider is designed to realize a certain range of divide ratio for a particular application [10]-[12]. For example, the divide ratio in [11] is 220~225 for a HIPERLAN frequency synthesizer.

5.1.2 Phase switching prescaler

The phase-switching architecture was first proposed by Craninckx and Steyaert [13] to increase the maximum operating frequency and save power consumption. Figure 5-3 shows the block diagram of a prescaler using the existing phase-switching technique. It has two divide-by-2 stages in cascade and only the first FF operates at the highest input frequency. The second master-slave FF operates at half of the input frequency and generates four 90°-spaced outputs, namely, in-phase, quadrature, and their reverse signals [13]. Each output lags behind the other by one input signal period. At any time instant, only one of these four signals is connected to *Y* through a 4-to-1 MUX. If we switch *Y* from *I* to *Q* properly, it is equivalent to swallow an input cycle and increase the instantaneous division ratio (from f_{in} to *Y*) by 1,

i.e., from 4 to 5. For the whole prescaler shown in Fig. 5-3, if the mode control (MC) is high, phase-switching occurs once per output cycle and the divide ratio (from f_{in} to f_{out}) is $4N+1$. Otherwise, no switching occurs in an output cycle and the divide ratio is $4N$.

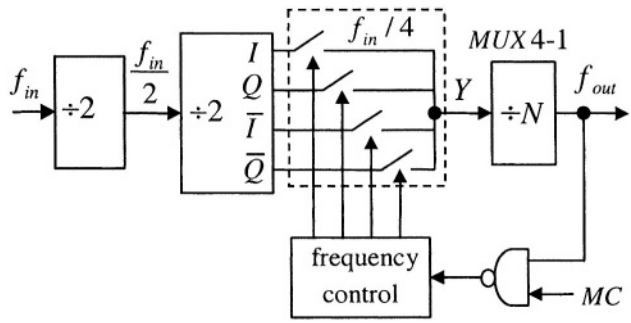


Figure 5-3. Existing phase-switching prescaler

Since in the phase-switching prescaler only the first ÷2 FF works at the highest input frequency, a prescaler with the same speed as an asynchronous divider can be obtained. Although the phase-switching architecture has the above advantages over the conventional one, it may suffer from glitches. Figure 5-4 illustrates the correct (case 1) and wrong (case 2) switching timing windows [14]. In Fig. 5-4, when switching Y from I to Q happens at timing point **a** where I and Q are at the same logic level (case 1), the instantaneous divide ratio is increased from 4 to 5. However, when ill-timed switching happens at timing point **b** where I and Q are of different logic levels (case 2), it generates a glitch in the output. This kind of glitches can cause the following ÷N counter to miscount. Phase-switching prescalers have been popular in the literature [13]-[16] and various significant efforts have been made to remove the glitches. As summarized in [14], a long rising-time MUX control signal is used in [13], but it is not robust due to the sensitivity to process variation. Feedback from MUX is used in [15], however it reduces the operation speed. A synchronizing flip-flop is used in [16] to retime MUX control signal. Similarly, a retiming circuit is used in [14], which unfortunately increases the circuit complexity and consumes more power and area. With synchronization or retiming, the phase-switching operation is still not very robust because it is difficult to implement such a high-speed circuit and the timing requirement of this circuit itself is very stringent.

Multi-modulus prescaler/divider can also be implemented based on phase-switching input stage [14], [17]. For example, the divide ratio in [17] is 64~71 for a DCS-1800 frequency synthesizer.

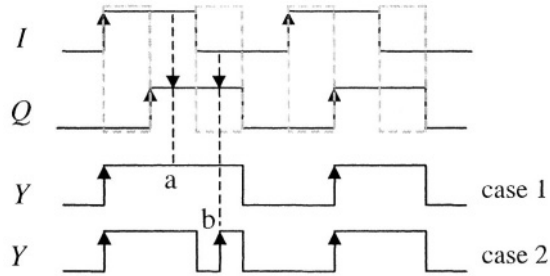


Figure 5-4. Timing windows of correct and incorrect switching

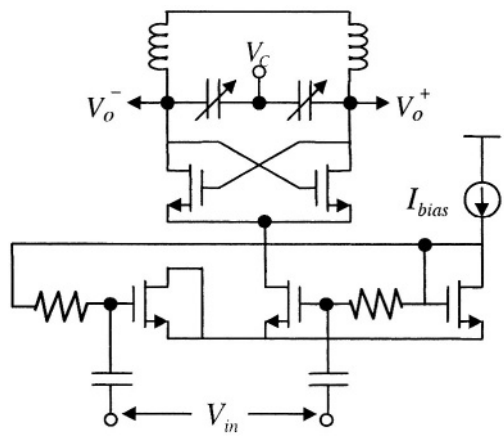


Figure 5-5. Schematic of a differential ÷2 ILFD

5.1.3 Injection-locked prescaler

To further compete with the oscillating frequency of the *LC*-VCO, an analog frequency divider called injection-locked frequency divider (ILFD) can be employed [12], [18]-[21]. It trades the operating frequency range with power consumption. ILFD's based on both *LC*-VCO and ring-VCO are investigated in the literature. The divide-by-2 ILFD based on *LC*-VCO is shown in Fig. 5-5. It can be tuned simultaneously with the proceeding *LC*-VCO to enhance its operating frequency band. Besides the small input bandwidth, ILFD is usually very sensitive to process variations and it is not programmable unless combined with the phase-switching architecture.

5.1.4 Summary and comparison of prescalers

The prescaler is a high-speed frequency divider and it is the speed bottleneck of a high-frequency PLL. The speed of traditional digital

prescalers is limited by the synchronous input counter, which might be only half of the flip-flop's toggling speed, f_{FF} [22]. Moreover, the traditional prescaler is usually power and area consuming [12]. To increase the toggling speed of a flip-flop, designers limit the internal signal swing in the flip-flop [13], [23], [24]. However, the residual phase noise of the prescaler increases with small internal voltage swing [24], [25].

The phase-switching prescaler can be regarded as a derivative of the multiphase VCO and inherent fractional divider discussed in Chapter 2. It can work as fast as f_{FF} and saves power. The main problem of the existing phase-switching prescaler is the possible glitches and the current glitch-removing techniques are not robust and even involve significant power. The superharmonic ILFD is a low-power analog divider that can work around n times of the VCO self-oscillating frequency, f_{VCO}, where n is the order of superharmonic. n is 2 for ILFD based on LC-VCO in [12], and n equals the number of stages of the ring oscillator in [21]. The disadvantages of ILFD include small input frequency range, non-programmability and sensitivity to process variation. However, if we combine the ILFD and phase-switching technique, we may design a very high-speed and programmable prescaler. Note that at radio frequencies, the boundary between digital and analog disappears. Both the input synchronous counter in a traditional prescaler [1], [24] and the input toggling flip-flop in phase-switching prescaler self-oscillate in the absence of input [14]. Thus these input stages can be interpreted as an injection-locked oscillator [23]. A comparison of existing prescaler architectures is summarized in Table 5-1.

Table 5-1. Comparison of existing prescaler architectures

architecture	conventional	phase-switching	injection-locked
speed	$\approx 0.5 f_{FF}$	$\approx f_{FF}$	$\approx n \cdot f_{VCO}$
power	high	middle	low
frequency	large	large	small
programmability	good	good	bad

5.2 Enhanced phase-switching prescaler

With the ever increasing input frequency and the speed constraint of the CMOS process, it is preferable to further divide down the input frequency before phase-switching occurs to increase the robustness of the switching operation. One more ÷2 stage is used in the enhanced phase-switching prescaler shown in Fig. 5-6 [26], [27]. Since the MUX operating speed is reduced by half, it can be implemented with standard digital cells and level amplification is saved to reduce power. This stage consists of two master-slave flip-flops working in parallel. It generates eight outputs with 45°

spacing. The spacing in time domain remains to be one input cycle. However, the output waveforms can be either of two patterns shown in Fig. 5-7. It depends on the initial status of the two flip-flops and the beginning order of their clock signals, which are difficult to predict. Circuit simulation shows that both patterns can occur.

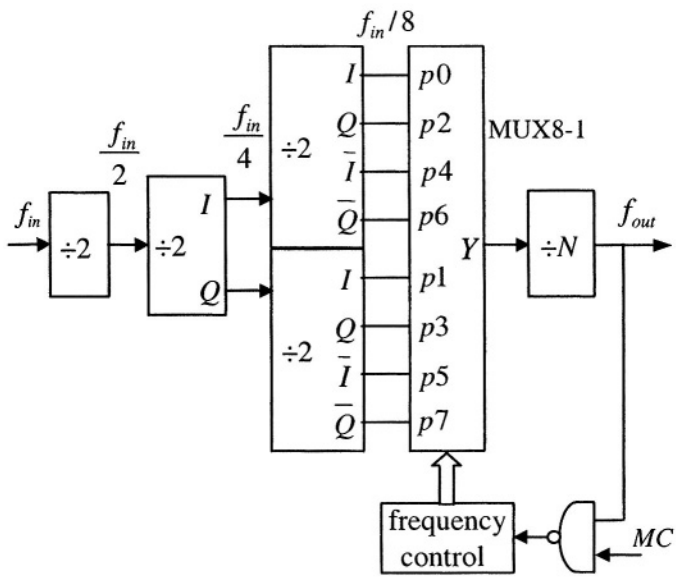


Figure 5-6. Enhanced phase-switching prescaler architecture

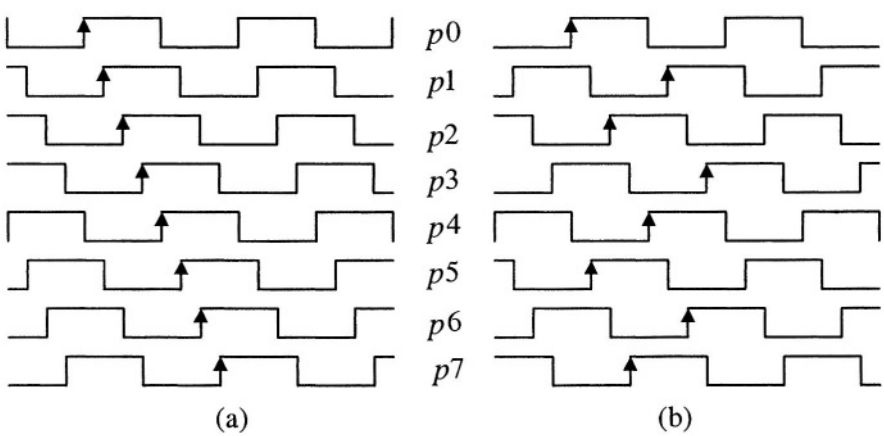


Figure 5-7. Two potential phase patterns of 8 outputs

The waveform in Fig. 5-7 (a) is what we desire. For the pattern in Fig. 5-7 (b), we need to exchange signal pairs ($p1$, $p5$) and ($p3$, $p7$) to yield the same pattern as in Fig. 5-7 (a). Fortunately, this problem can be tackled by detecting the phase difference between $p0$ and $p1$ and using the detection result to control the 8-to-1 MUX operation. We will explain this in more detail in the next section.

If we use the conventional phase-switching sequence as shown in Fig. 5-8 (a), although the correct timing window is now three times as large as incorrect timing window, glitches can still happen without additional retiming circuit to synchronize the MUX control inputs. However, we can completely remove the glitches by simply reversing the switching sequence as shown in Fig. 5-8 (b). By changing the switching sequence, the instantaneous divide ratio is decreased by 1, that is, from 8 to 7 when switching occurs. We can obtain an inherently glitch-free phase-switching prescaler and save silicon area and power consumption. The divide ratio of the prescaler is $P=8N-1$ if the mode control input is high and $P+1=8N$, otherwise. For instance, the divide ratio $P/P+1$ becomes 15/16 when $N=2$.

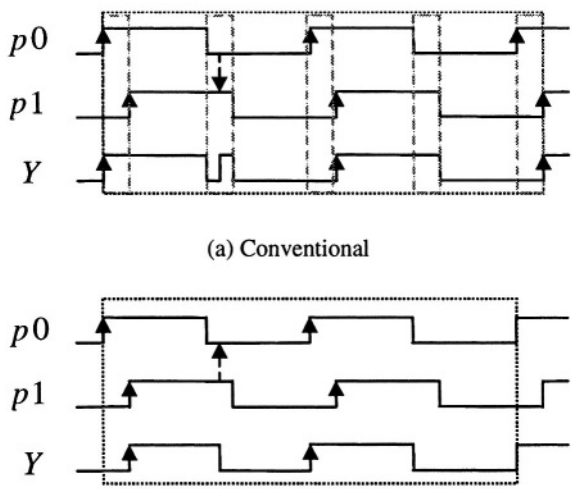


Figure 5-8. Phase-switching sequence

5.3 Circuit design and simulation results

5.3.1 Eight 45°-spaced phases generation

The four ÷2 FF's shown in Fig. 5-6 are implemented using the same topology shown in Fig. 5-9. It is the source-coupled logic (SCL) without tail current [28]. With the omission of the tail current, the FF can work under

lower power supply and higher frequency. The transistors are sized to work properly even beyond 2.4-GHz with $0.35\mu m$ CMOS technology and each stage can drive the next stage directly. Fig. 5-10 shows the simulated output waveforms of the divide-by-8 stage. These FF's are the main power and area consumers.

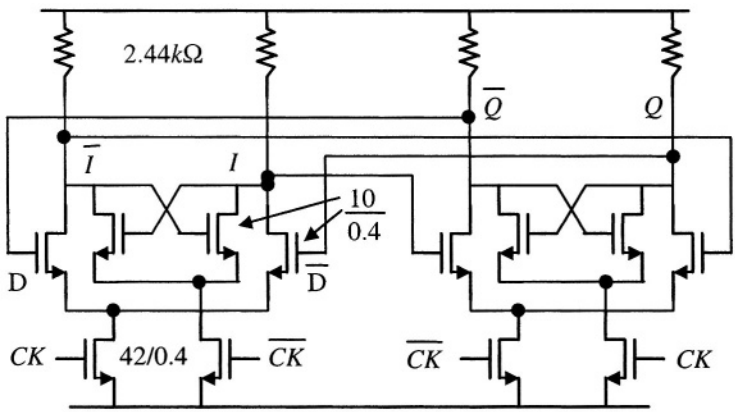


Figure 5-9. SCL flip-flop configured as divide-by-2

As shown in Fig. 5-11, an exclusive-or (XOR) gate is used to detect the relative phases between $p0$ and $p1$, which represent the upper and lower FF's in the third ÷2 stage in Fig. 5-6, respectively. Following the XOR, a buffer with long channel-length transistors is used to filter out narrow spikes. The output of the detection circuit is low if $p0$ leads $p1$ by 45° and high if $p0$ leads $p1$ by 225°. Dummy loads are added to other 6 outputs, $p2$ through $p7$, to keep the same load effect for all eight phases.

5.3.2 8-to-1 multiplexer

The 8-to-1 multiplexer (MUX) is shown Fig. 5-12. This low-speed MUX is built with standard digital cells instead of current-mode logic to save power. To match the delays from 8 phases, $p0$ through $p7$, to the multiplexer output Y, 2-input symmetric NAND and NOR gates shown in Fig. 5-13 (a) and (b) are used in the multiplexer. For $0 \le n \le 7$, if selection control input Sn is high, phase input pn will be connected to the MUX output Y, that is,

$$Y = p7 \cdot S7 + p6 \cdot S6 + p5 \cdot S5 + p4 \cdot S4 + p3 \cdot S3 + p2 \cdot S2 + p1 \cdot S1 + p0 \cdot S0 \tag{5.1}$$

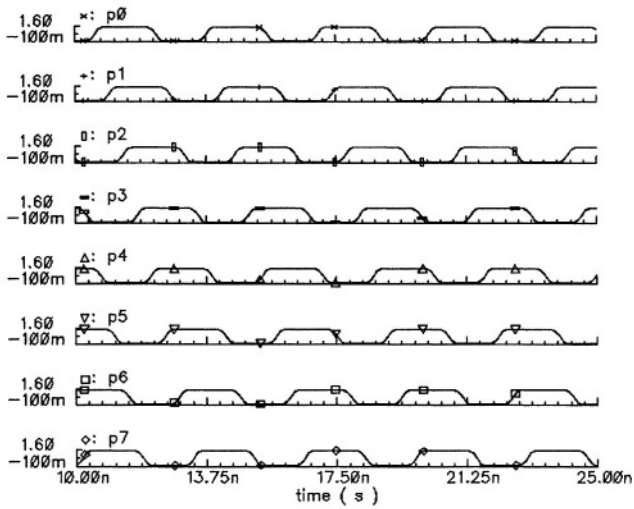


Figure 5-10. Simulated eight 45°-spaced divide-by-8 waveforms

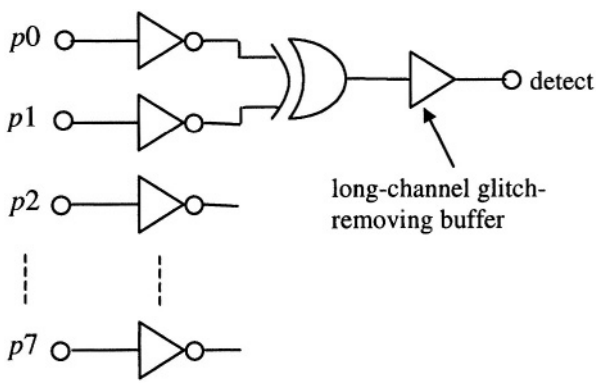


Figure 5-11. Phase pattern detection circuit

5.3.3 Switching control circuit

A robust phase-switching control circuit is used in this design. An 8-bit shift register is used to generate phase selection signals, *S*0 to *S*7 for the 8-to-1 MUX. At any time, only one of the eight phase selection signals is high. As mentioned in the previous section, since there are two possible phase patterns (see Fig. 5-7) for signals *p*0 to *p*7, we need to use the phase detection result to adjust the phase selection sequence. If the detection result is low, that is, *p*0 leads *p*1 by 45° (Fig. 5-7 (a)), the phase-switching will occur in the following sequence $p0 \rightarrow p7 \rightarrow p6 \rightarrow \cdots \rightarrow p0$. Otherwise, the phase-switching sequence will be $p0 \rightarrow p3 \rightarrow p6 \rightarrow p1 \rightarrow p4 \rightarrow p7 \rightarrow p2 \rightarrow p5 \rightarrow p0$.

This is equivalent to exchanging two phase-pairs, ($p1$, $p5$) and ($p3$, $p7$), for the phase pattern in Fig. 5-7 (b).

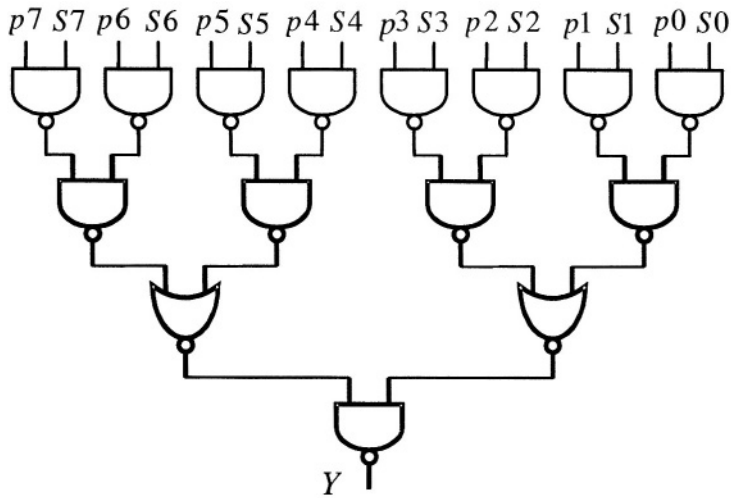


Figure 5-12. 8-to-1 multiplexer

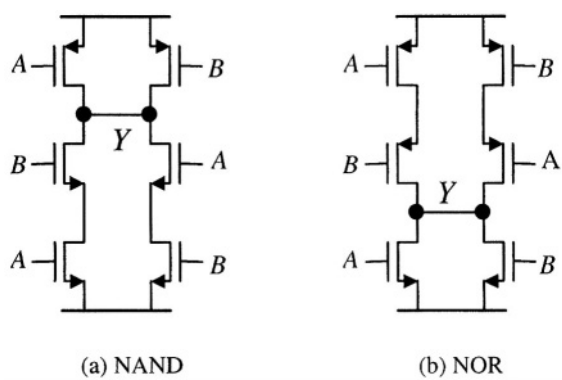


Figure 5-13. Symmetric 2-input gates

5.3.4 Asynchronous frequency divider

The asynchronous ÷N divider, where N is 2 in this ÷15/16 prescaler, consists of one true-single-phase-clock (TSPC) FF [29], [30] shown in Fig. 5-14. It is simple and can work well at high frequencies.

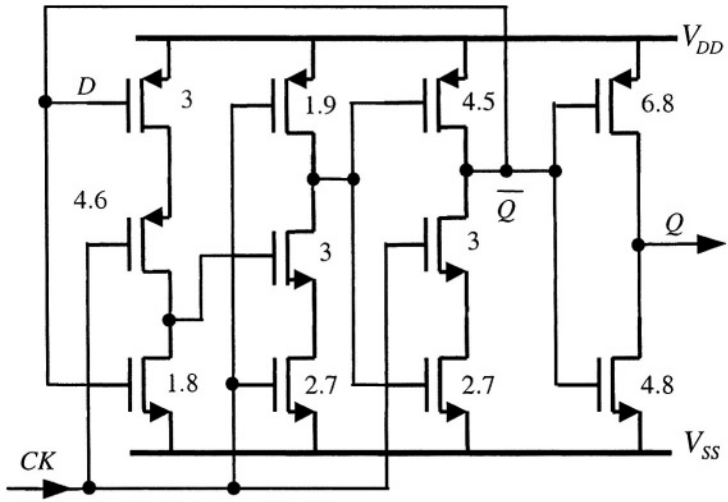


Figure 5-14. True-single-phase-clock flip-flop

Note that in Fig. 5-14 the transistors' widths are in the unit of μm, and all lengths are $0.4\mu m$.

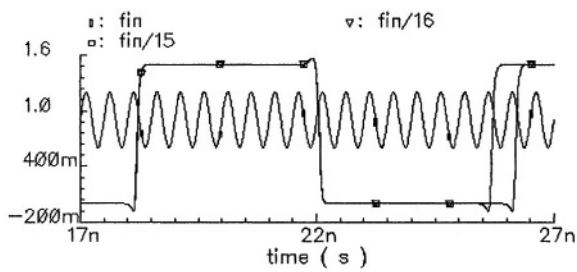


Figure 5-15. Simulated prescaler input and output waveforms

The whole prescaler consumes $2mA$ at $1.5V$ supply with $2.4GHz$ inputs in simulation. Its divide ration is 16 when the mode control is low and 15 otherwise. The simulated input and output waveforms are shown in Fig. 5-15. The duty cycles of MUX output Y and the ÷16 output f_{out} are not exactly 50% because the rise and fall propagation delays of both the MUX and asynchronous ÷N divider are not exactly equal. The duty cycles of both Y and f_{out} are not important in this inherently glitch-free phase-switching architecture.

5.4 Delay budget in the switching control loop

Figure 5-16 shows the timing relationship when it switches from phase $p1$ to phase $p0$. Timing analysis is required to determine the delay budget in the phase-switching control loop, which consists of the MUX8-1, the asynchronous $\div N$ divider, and the frequency control (including the NAND gate) in Fig. 5-6. The following delay timing analysis is very helpful for understanding the timing of the phase-switching control loop and provides guidelines for a sound design of this loop. The notation used in Fig. 5-15 is defined next. Here we use $p1\uparrow \rightarrow Y\uparrow$ to indicate the propagation from the rising edge of $p1$ to the rising edge of Y.

Δt_{MUX} : the rising edge propagation delay of MUX in the absence of switching $(p1\uparrow \rightarrow Y\uparrow)$

Δt_{DIV} : the rising edge propagation delay of the $\div N$ divider $(Y\uparrow \rightarrow f_{out}\uparrow)$

Δt_{CTL} : the rising edge propagation delay of the frequency control generation $(f_{out}\uparrow \rightarrow S0\uparrow)$

Δt_{sp1} : the amount of time that rising edge of $S0$ leads the next rising edge of phase $p0$

Δt_{pY1} : the first rising edge propagation delay of MUX after switching occurs $(p0\uparrow \rightarrow Y\uparrow)$

Δt_{sp2} : the amount of time that rising edge of $S0$ leads the second next rising edge of phase $p0$

Δt_{pY2} : the second rising edge propagation delay of MUX after switching occurs $(p0\uparrow \rightarrow Y\uparrow)$

T7: the delay from the rising edge of $p1$ to the next rising edge of $p0$. $T7 = 7T_{in}$, where T_{in} is the prescaler' s input period

T_{Ysw} : the first period of Y when phase-switching occurs

T_{out} : the period of the prescaler's output when phase-switching occurs, which is $15T_{in}$ if the prescaler works properly

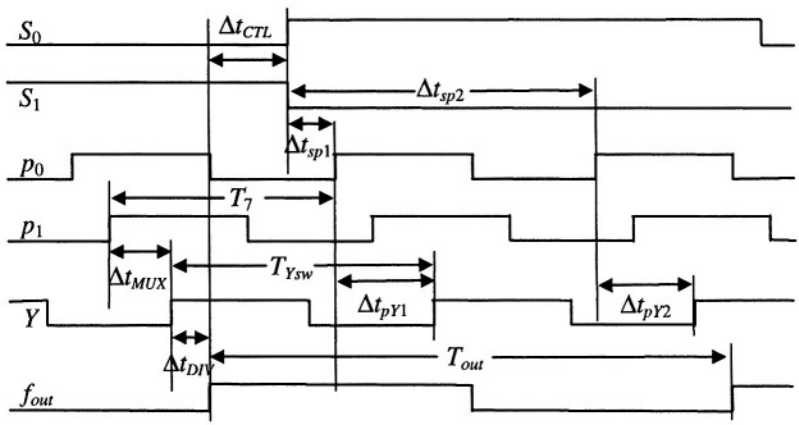


Figure 5-16. Simulated phase-switching waveforms

From timing analysis of the delays shown in Fig. 5-16, we observe that:

1) If $\Delta t_{sp1} = 7T_{in} - \Delta t_{MUX} - \Delta t_{DIV} - \Delta t_{CTL}$ is longer than the maximum propagation delay of the MUX, which is approximately Δt_{MUX}, then the logic propagations due to change of phase selection signal *S*0 and phase *p*0 do not interfere with each other in MUX. Under this condition, $\Delta t_{pY1} = \Delta t_{MUX}$ and it guarantees that $T_{Ysw} = 7T_{in}$. Otherwise, T_{Ysw} can be anywhere from $7T_{in}$ to $8T_{in}$. Thus, the constraint on delays in the control loop for the phase-switching to be completed in the first cycle of *Y* is $2\Delta t_{MUX} + \Delta t_{DIV} + \Delta t_{CTL} \le 7T_{in}$. If this constraint is satisfied, a multi-modulus prescaler [14] [17] (÷14/15/16) can also be implemented. The divide ratio of 14 can be achieved by modifying the switching control to switch the phase twice during one prescaler output cycle.
2) If the phase-switching can not be completed in the first cycle of *Y*, but $\Delta t_{sp2} = 15T_{in} - \Delta t_{MUX} - \Delta t_{DIV} - \Delta t_{CTL}$ is long enough, so that the logic rising of *S*0 doesn't interfere with the second logic rising of *p*0 in the MUX, then $\Delta t_{pY2} = \Delta t_{MUX}$ and it guarantees that $T_{out} = 15T_{in}$. Hence the constraint on delays in the phase-switching control loop for a ÷15/16 prescaler is $2\Delta t_{MUX} + \Delta t_{DIV} + \Delta t_{CTL} \le 15T_{in}$.
3) If we increase the prescaler division factor, for example, to 31/32, we increase both prescaler output period, T_{out}, and delay of asynchronous ÷*N* divider, Δt_{DIV}, by approximately a factor of 2. Since $T_{out} > \Delta t_{DIV}$, it has more delay budget and the prescaler operation is safer. So usually the circuit delays in the switching control loop is not a problem and the

first toggling FF is the only speed limit of this improved phase-switching architecture.

From the relationship between delays in the phase-switching control loop and the prescaler's input signal period, we can schedule the delays in the control loop for a sound design.

5.5 Spurs due to nonideal 45° phase spacing

Ideally the eight phases, $p0$ through $p7$, are evenly spaced for the phase pattern shown in Fig. 5-10. However, like a multi-phase VCO [31]-[35] or delay stages [36], [37], there is a systematic delay (or phase) mismatch in each physical implementation of the phase-switching prescaler. The operation of the loop frequency divider, which incorporates a divide-by-15/16 phase-switching prescaler, can be classified into three modes. The first one is an integer-N divide ratio that is a multiple of 16, and no phase switching occurs in this mode. The second one is an integer-N divide ratio that is not a multiple of 16, and the phase switching occurs periodically. The third one is a fractional-N divide ratio, and the phase switching occurs randomly due to the ΣΔ modulation. It is obvious that the phase mismatch does not matter in the first divider operation mode, while spurs resulting from the phase mismatch are generally eliminated in the fractional-N operation mode [31]. Thus, we need to analyze spurs due to the phase mismatch in the second divider operation mode.

With the delay mismatch of the 8-to-l MUX also taken into account, the systematic nonideal spacing of the eight phases is illustrated in Fig. 5-17, where the dashed and solid lines represent the ideal and nonideal positions of the output phases.

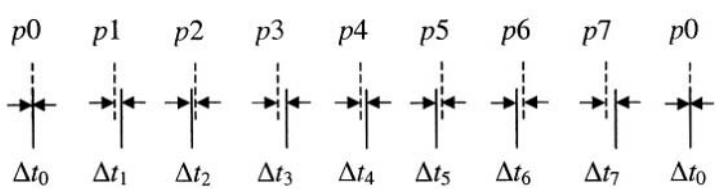


Figure 5-17. Phase mismatch in the phase-switching prescaler

When the PLL loop divide ratio is $N=16m+15$, where m is an integer number, the phase switching occurs once in every divider output cycle, and the phase error of the divider output varies through the following sequence periodically:

$$\Delta\theta_7,\ \Delta\theta_6,\ \Delta\theta_5,\ \Delta\theta_4,\ \Delta\theta_3,\ \Delta\theta_2,\ \Delta\theta_1,\ \Delta\theta_0 \qquad (5.2)$$

where the phase error is

$$\Delta\theta_i = 2\pi \frac{\Delta t_i}{T_{ref}} \qquad i = 0, 1, \ldots, 7 \tag{5.3}$$

Similarly, when divide ratio N=16m+30, the phase switching occurs twice during each divider output period, and the periodic divider output phase error sequence is:

$$\Delta\theta_6, \Delta\theta_4, \Delta\theta_2, \Delta\theta_0 \quad \text{or} \quad \Delta\theta_7, \Delta\theta_5, \Delta\theta_3, \Delta\theta_1 \tag{5.4}$$

Thus, we see that the phase error of the loop divider output varies periodically due to the delay mismatch in the phase-switching prescaler. When the number of phase switching is odd during each divider output cycle, the period of the phase error sequence is 8; when the number of switching is 2 or 6, the period is 4; when the number of switching is 4, the period is 2.

The loop divider output spurs caused by the delay mismatch in the phase-switching prescaler can be calculated from the discrete Fourier transformation (DFT) [38] of the phase error sequence. For example, when the loop divider output phase error is the sequence of (5.2), its DFT coefficients [38] are

$$\Theta_k = \frac{1}{8}\sum_{i=0}^{7} \Delta\theta_i e^{-j\frac{\pi}{4}i\cdot k} \qquad k = 0, 1, \ldots, 7 \tag{5.5}$$

The spur level (in *dBc*) of the divider output at frequency of $(k/8)f_{ref}$ is

$$P_{spur\_div}(k) = \begin{cases} 20\log|\Theta_k| + 3 & 1 \le k \le 7, \quad k \ne 4 \\ 20\log|\Theta_k| & k = 4 \end{cases} \tag{5.6}$$

The single-sideband spur level (in *dBc*) at the PLL output is

$$P_{spur}(k) = \begin{cases} 20\log[|\Theta_k| \cdot N] + 20\log\left|H_{ol}\left(j\frac{k}{8}\omega_{ref}\right)\right| & 1 \le k \le 7, \quad k \ne 4 \\ 20\log[|\Theta_k| \cdot N] - 3 + 20\log\left|H_{ol}\left(j\frac{k}{8}\omega_{ref}\right)\right| & k = 4 \end{cases} \tag{5.7}$$

where the PLL open-loop gain $H_{ol}(j\omega)$ is defined in (3.3). Remember that the PLL output period is $T_0 = T_{ref} / N$. If we define the phase error as

$$\Delta\theta_i' = 2\pi \frac{\Delta t_i}{T_0} = \Delta\theta_i \cdot N \qquad i = 0, 1, \ldots, 7 \tag{5.8}$$

Then its DFT is

$$\Theta_k' = \frac{1}{8}\sum_{i=0}^{7} \Delta\theta_k' e^{-j\frac{\pi}{4}i\cdot k} = \Theta_k \cdot N \qquad k = 0, 1, \ldots, 7 \tag{5.9}$$

From (5.9) and (5.7), the PLL output spur level can be written in terms of Θ_k' as

$$P_{spur}(k) = \begin{cases} 20\log\left|\Theta_k'\right| + 20\log\left|H_{ol}\left(j\frac{k}{8}\omega_{ref}\right)\right| & 1 \le k \le 7, \quad k \ne 4 \\ 20\log\left|\Theta_k'\right| - 3 + 20\log\left|H_{ol}\left(j\frac{k}{8}\omega_{ref}\right)\right| & k = 4 \end{cases} \tag{5.10}$$

Therefore, we see that the spur level is actually not dependent on the loop division ratio *N,* but the ratio of the delay mismatch and the PLL output period ($\Delta t_i / T_0$). Table 5-2 gives a numerical example of the delay mismatches ($T_0 = 1ns$) and values of the first term of spur formula (5.10).

Table 5-2. A numerical example of delay mismatches and spurs

i, k	0	1	2	3	4	5	6	7
Δt_i [ps]	−0.353	−0.198	−0.283	−1.10	0.466	0.325	−1.168	0.079
$\lvert\Theta_k'\rvert$ [dB]	−55.1	−68.5	−56.4	−54.3	−69.1	−54.3	−56.4	−68.5

Even though the delay mismatch sequence (Δt_i) of the phase-switching prescaler for each physical implementation is fixed, its values are statistically distributed among different implementations. Therefore, it is necessary to investigate the corresponding statistical distribution of the spurs induced. For simplicity, we assume that (Δt_i (i=0, 1, ⋯, 7) sequence has independent Gaussian distribution.

Let us look at the statistical distribution of the DFT coefficients of a data sequence with normal distribution. Assuming x_i (i=0, 1, ⋯, 7) are

independent Gaussian variables with zero mean and variance of σ_x. The corresponding DTF coefficients are

$$y_k = \frac{1}{8}\sum_{i=0}^{7} x_i e^{-j\pi \cdot i \cdot k/4} \tag{5.11}$$

Therefore, we have

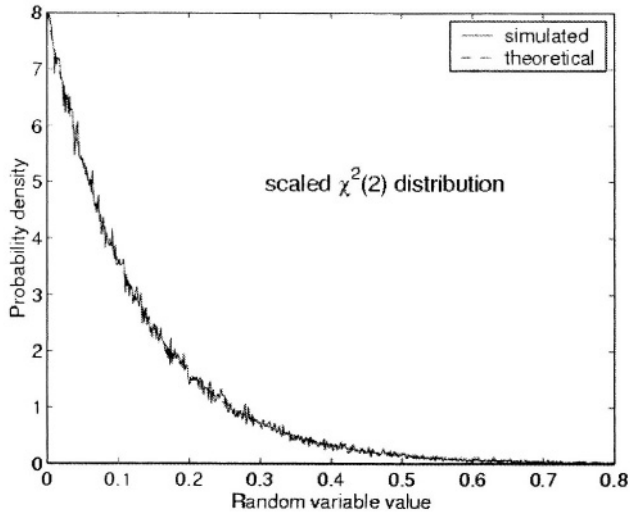
$$\begin{aligned} |y_1|^2 = |y_7|^2 = \frac{1}{64}\left(x_0 + \frac{\sqrt{2}}{2}x_1 - \frac{\sqrt{2}}{2}x_3 - x_4 - \frac{\sqrt{2}}{2}x_5 + \frac{\sqrt{2}}{2}x_7 \right)^2 \\ + \frac{1}{64}\left(\frac{\sqrt{2}}{2}x_1 + x_2 + \frac{\sqrt{2}}{2}x_3 - \frac{\sqrt{2}}{2}x_5 - x_6 - \frac{\sqrt{2}}{2}x_7 \right)^2 \end{aligned} \tag{5.12}$$

$$|y_2|^2 = |y_6|^2 = \frac{1}{64}(x_0 - x_2 + x_4 - x_6)^2 + \frac{1}{64}(x_1 - x_3 + x_5 - x_7)^2 \tag{5.13}$$

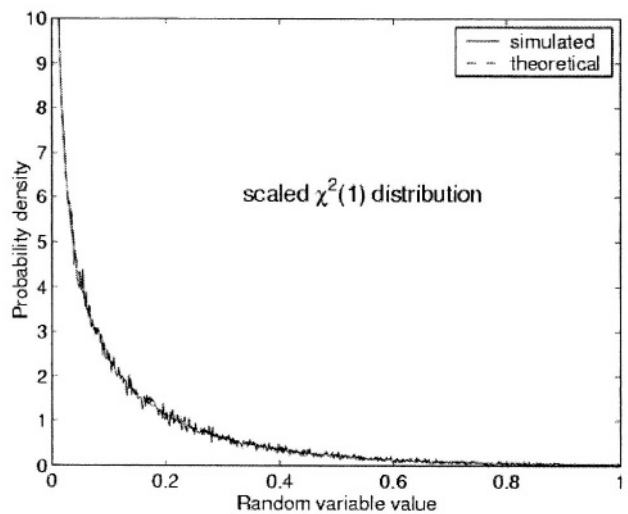
$$\begin{aligned} |y_3|^2 = |y_5|^2 = \frac{1}{64}\left(x_0 - \frac{\sqrt{2}}{2}x_1 + \frac{\sqrt{2}}{2}x_3 - x_4 + \frac{\sqrt{2}}{2}x_5 - \frac{\sqrt{2}}{2}x_7 \right)^2 \\ + \frac{1}{64}\left(\frac{\sqrt{2}}{2}x_1 - x_2 + \frac{\sqrt{2}}{2}x_3 - \frac{\sqrt{2}}{2}x_5 + x_6 - \frac{\sqrt{2}}{2}x_7 \right)^2 \end{aligned} \tag{5.14}$$

and

$$|y_4|^2 = \frac{1}{64}(x_0 - x_1 + x_2 - x_3 + x_4 - x_5 + x_6 - x_7)^2 \tag{5.15}$$



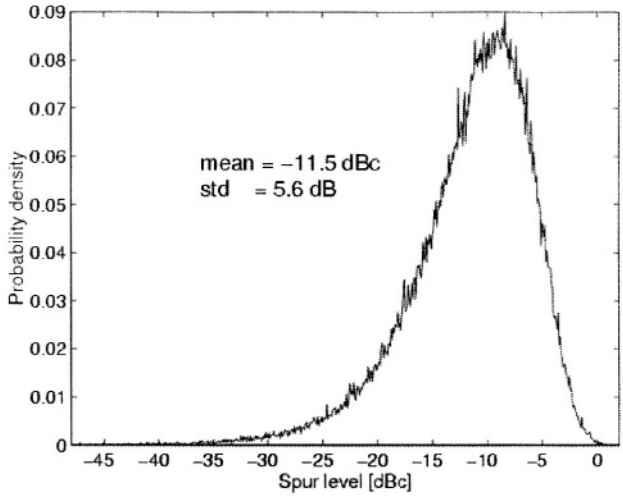
(a) $|y_k|^2$, $1 \le k \le 7$, $k \ne 4$



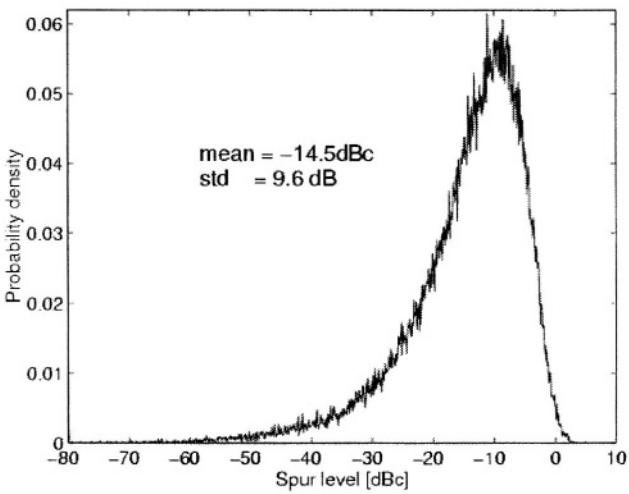
(b) $|y_4|^2$

Figure 5-18. Statistical distribution of DFT of delay mismatches

From (5.12), (5.13) and (5.14), we find that $|y_k|^2$, for $1 \le k \le 7$ and $k \ne 4$, has a scaled Chi-square distribution of dimension 2 [39] shown in (5.16). Note that, although the two terms in each pair of parenthesis in (5.12) and (5.14) share some common variables, they are uncorrelated Gaussian variables and are hence independent [40].



(a) $20\log|y_k|$, $1 \le k \le 7$, $k \neq 4$



(b) $20\log|y_4|$

Figure 5-19. Statistical distribution of spurs due to delay mismatches

$$|y_k|^2 \sim \chi^2(2) \cdot \frac{\sigma_x^2}{16} \qquad 1 \le k \le 7,\ k \neq 4 \tag{5.16}$$

However, $|y_4|^2$ has a scaled Chi-square distribution of dimension 1 [39] shown in (5.17)

$$|y_4|^2 \sim \chi^2(1) \cdot \frac{\sigma_x^2}{8} \tag{5.17}$$

Figure 5-18 shows the Matlab simulated distributions of $|y_k|^2$ ($1 \le k \le 7$, $k \ne 4$) and $|y_4|^2$ with $\sigma_x = 1$, which agree well with the theoretical formula in (5.16) and (5.17), respectively.

The Matlab simulated distributions of $20\log|y_k|$ ($1 \le k \le 7$, $k \ne 4$) and $20\log|y_4|$ with $\sigma_x = 1$ are shown in Fig. 5-19 (a) and (b), respectively. Again we use a numerical example to give a quantitative insight into the spurs. If the variance of normally distributed Δt_i is $0.5ps$ and $T_0 = 1ns$, then the variance of θ_k' defined in (5.8) is 0.628%, i.e., $-50dB$. Further, if $H(j\omega_{ref}/8) = -30dB$, from Fig. 5-19 (a) and equation (5.10) the expected value of the PLL output spur at $f_{ref}/8$ is $-91.5dBc$, that is, $-50dB - 30dB - 11.5dBc = -91.5dBc$. As indicated in Fig. 5-19 (a), the variance of this spur is $5.6dB$.

Attention was paid for good symmetry and matching in the layout of the phase generating flip-flops, the frequency control circuit and the MUX. By careful design and layout, the spurs generated by non-ideal 45°-spacing can be suppressed to negligible levels [41].

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Chapter 6

LOOP FILTER WITH CAPACITANCE MULTIPLIER

This chapter concentrates on the loop filter design. Various loop filter topologies are reviewed, and a novel loop filter based on the capacitance multiplier is presented. The capacitance multiplier emulates the large loop capacitor very well. The new loop filter is very power and area efficient.

6.1 Loop filter architecture

6.1.1 Passive loop filter

The passive loop filter for charge-pump PLL shown in Fig. 3-7 (a) is repeated in Fig. 6-1.

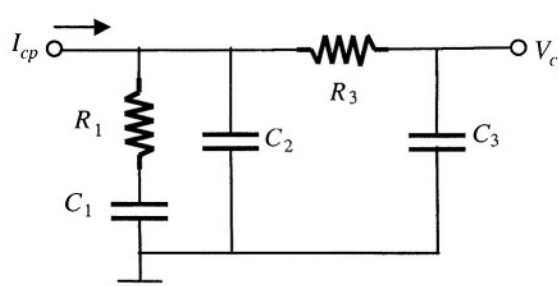


Figure 6-1. Third-order passive loop filter

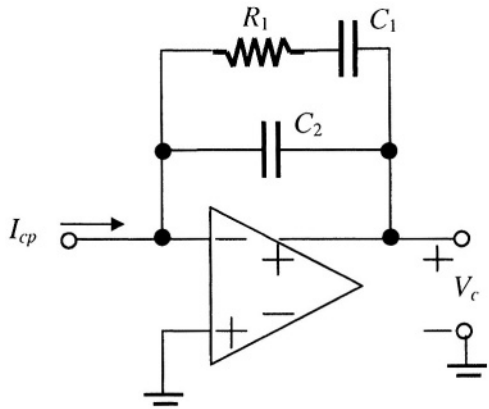


Figure 6-2. Second-order active loop filter

Besides the passive implementation, the active loop filter is another option. Figure 6-2 shows an example of the second-order active loop filter. Active filters have the advantage of more flexible pole/zero arrangement. Especially for off-chip loop filter, the operational amplifier (OPA) can work with a higher supply voltage source to increase control voltage swing [1]. Also, for active filters like the one shown in Fig. 6-2, the charge-pump output voltage is fixed and its current matching improves. Furthermore, for a fully differential PLL implementation, active loop filter implementation is necessary for controlling the VCO common-mode control voltage [2]. The disadvantages of active loop filters include additional power consumption and noise contribution.

6.1.2 Dual-path loop filter

The loop filter is the integration bottleneck of narrow-band PLL frequency synthesizers. Dual-path loop filter is widely used to solve the problem of integrating a large loop capacitor on chip [3]-[8]. As illustrated in Fig. 6-3, the dual-path loop filter has an integration path (on the left), a low-pass path (on the right, also referred to as proportional path) and a voltage adder.

The dual-path loop filter's transfer function is derived as follows:

$$V_z = \frac{I_{cp}}{sC_z} \tag{6.1}$$

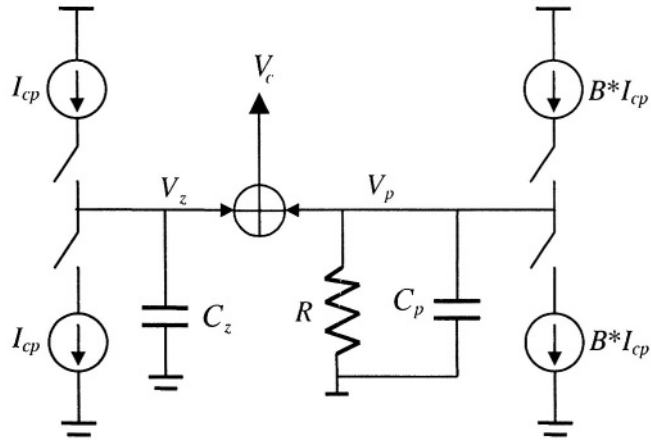


Figure 6-3. Dual-path loop filter

$$V_p = \frac{B \cdot I_{cp} \cdot R}{1 + sRC_z} \tag{6.2}$$

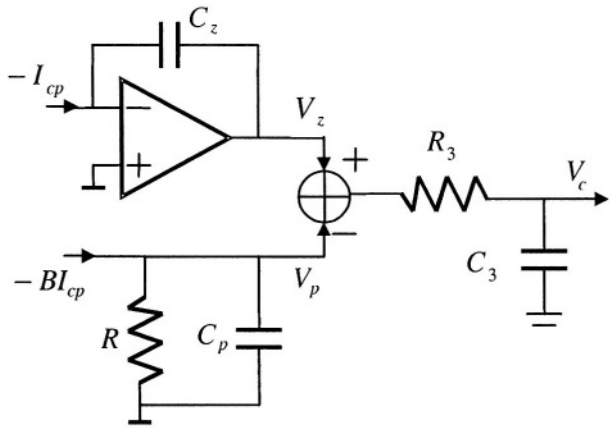
$$V_c = V_z + V_p = \frac{I_{cp}\left[1 + sR\left(B \cdot C_z + C_p\right)\right]}{sC_z\left(1 + sRC_z\right)} \tag{6.3}$$

From (6.3), we observe that the zero in this dual-path loop filter is

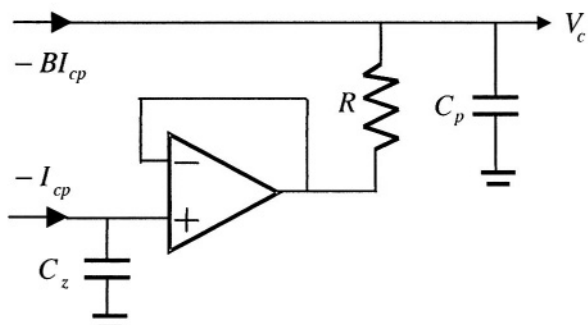
$$\omega_z = \frac{1}{R\left(B \cdot C_z + C_p\right)} \tag{6.4}$$

Thus, by scaling the dual charge-pump currents, it is equivalent to scaling up the integration capacitance C_z by the current scaling factor B of dual charge-pumps.

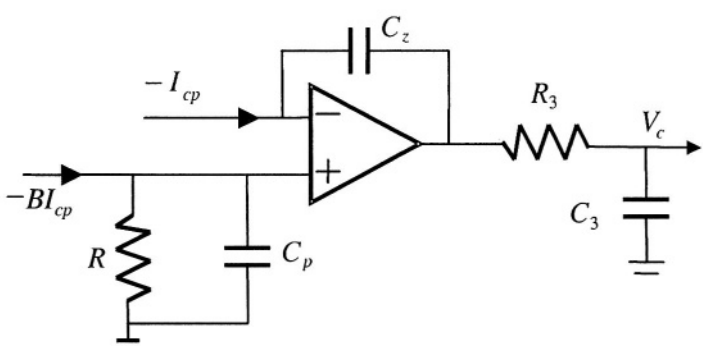
Figure 6-4 (a) shows a third-order dual-path loop filter implemented in [4]. Two active devices are used, one operational amplifier and one voltage adder. Figure 6-4 (b) is the dual-path loop filter implementation in [7]. Compared with the previous implementation, this one does not need a floating capacitor and only use one active device, the buffer. Another similar implementation in [8] is shown in Fig. 6-4 (c).



(a)



(b)



(c)

Figure 6-4. Dual-path loop filter implementation

In spite of many advantages in the dual-path architecture, it also bears lots of disadvantages. Besides increased noise and power due to active devices, the charge-pump of the integration path is still working with a very small current and contributes significant noise. Also, the delay mismatch of the dual charge pumps may change the loop parameters. Furthermore, at least for the implementations in [4]-[6], [8] the voltage decay due to the parallel *R* and *C* in the low-pass path might cause undesirable ripples on the VCO control voltage [9].

6.1.3 Sample-reset loop filter

A sample-reset loop filter for a PLL with a current controlled oscillator (CCO) was introduced in [10]. It is used to average the oscillator proportional control current that provides the feed-forward zero during the entire update period and hence produces a ripple-free control signal. The ripple-free control current eliminates the need for additional filtering poles, leading to a nearly 90° phase margin which minimizes input jitter peaking and transient locking overshoot.

The simplified diagram of the sample-reset loop filter is illustrated in Fig. 6-5. The key idea of this architecture is to generate a proportional current that is constant over the entire update period and has a value equal to the average current. This value leads to the same position of stabilizing zero as in the standard charge-pump PLL, but generates a ripple free oscillator control current, and thus minimizes the jitter. It can be achieved by first sampling the phase difference for each reference period (here reference frequency refers to the PFD update frequency) on a capacitor C_2 and then injecting a constant control current proportional to the sampled phase difference during the rest of the update period. At the beginning of each reference period, a reset must be performed on the sampling capacitance voltage to eliminate the memory of proportional path. This eliminates an additional pole at the origin that would otherwise make the loop unstable. The reset signal is synchronized with the reference frequency and is generated by the PFD. Two sampling and reset capacitors of value C_2, which operate in recycling order, are used to implement this idea. A comparison between the proportional path current in standard charge-pump PLL (I_{cpp}) and the sample-reset PLL (I_p) is shown in Fig. 6-6.

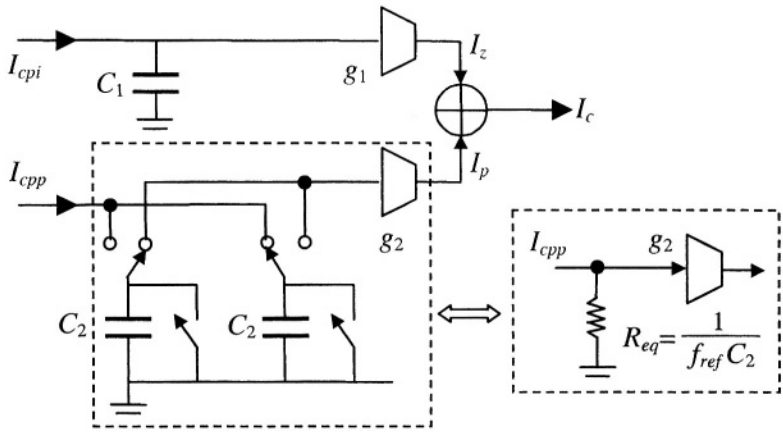


Figure 6-5. Sample-reset loop filter

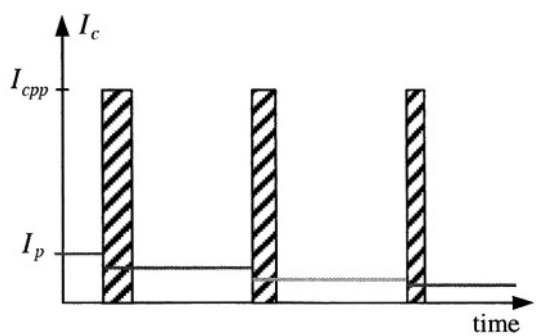


Figure 6-6. Sample-reset versus standard PLL

With the PFD phase error θ_e, the control current (I_c) is:

$$\frac{I_z}{\theta_e}(s) = \frac{I_{cpi}}{2\pi} \cdot \frac{1}{sC_1} \cdot g_1 \tag{6.5}$$

$$\frac{I_p}{\theta_e}(s) = \frac{I_{cpp}}{2\pi} \cdot \frac{1}{f_{ref}C_2} \cdot g_2 \tag{6.6}$$

$$\begin{aligned}\frac{I_c}{\theta_e}(s) &= \frac{I_z}{\theta_e}(s) + \frac{I_p}{\theta_e}(s) \\ &= \frac{I_{cpi}}{2\pi}\cdot\frac{g_1}{sC_1}\cdot\left(1+\frac{s}{f_{ref}}\cdot\frac{I_{cpp}}{I_{cpi}}\cdot\frac{C_1}{C_2}\cdot\frac{g_2}{g_1}\right)\end{aligned} \tag{6.7}$$

It shows that this sample-rest PLL is a type-II second order PLL. Its open loop gain is:

$$H_{ol}(s) = \frac{I_{cpi}}{2\pi}\cdot\frac{g_1}{sC_1}\cdot\left(1+\frac{s}{f_{ref}}\cdot\frac{I_{cpp}}{I_{cpi}}\cdot\frac{C_1}{C_2}\cdot\frac{g_2}{g_1}\right)\cdot\frac{K_{cco}}{s}\cdot\frac{1}{N} \tag{6.8}$$

Its zero is:

$$\omega_z = f_{ref}\frac{I_{cpi}}{I_{cpp}}\cdot\frac{C_2}{C_1}\cdot\frac{g_1}{g_2} \tag{6.9}$$

The natural frequency and damping factor are as follows:

$$\omega_n = \sqrt{\frac{K_{cco}I_{cpi}g_1}{2\pi C_1 N}} \tag{6.10}$$

$$\zeta = \frac{\omega_n}{2\omega_z} = \frac{1}{2f_{ref}}\sqrt{\frac{K_{cco}I_{cpi}C_1}{2\pi N g_1}}\cdot\frac{I_{cpp}}{I_{cpi}}\cdot\frac{g_2}{C_2} \tag{6.11}$$

Although the sample-reset loop filter tries to smooth the voltage ripple in the traditional charge-pump PLL, the voltage ripple still exists due to nonideal switching operation. Furthermore, the circuitry complexity and power/area is high, and additional noise comes from active devices used in this architecture. When the reference spur is not a big concern, this complicated architecture may not be worthwhile.

6.1.4 Other loop filter architectures

In [11], Larsson implemented an effective loop capacitance of $40nF$ as shown in Fig. 6-7. The resistance ratio is $B=R_x/R_y=40$.

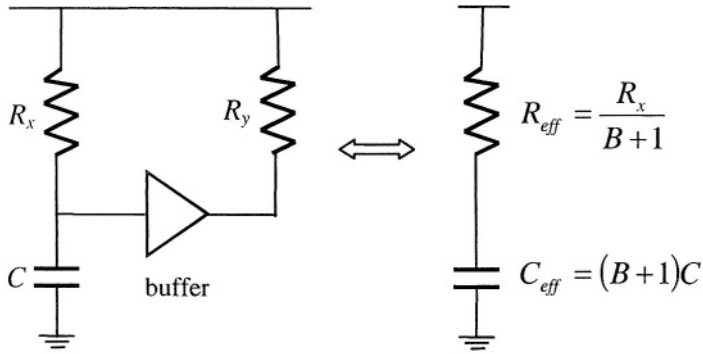


Figure 6-7. Loop filter in [11]

As indicated in Fig. 6-7, the effective resistance and capacitance of this second-order loop filter are

$$C_{eff} = (B+1) \cdot C \tag{6.12}$$

and

$$R_{eff} = R_x / (B+1) \tag{6.13}$$

Since R_x is scaled up by a factor of B+1, which is 41 in this case, its noise contribution beyond the bandwidth of the buffer might be significant. To increase the bandwidth of the buffer, it will cost considerable power. Moreover, the buffer might reduce the swing range of the VCO control voltage.

A discrete-time delay cell is used in [12] to emulate the zero-generating resistor R_1 (see Fig. 6-1) in the loop filter as shown in Fig. 6-8 (a). ΔT is much smaller than the loop time constant, so $e^{-s\Delta T} \approx 1 - s\Delta T$. The transfer function of PFD/CP/LF combination is

$$\begin{aligned} \frac{V_c}{\theta_e}(s) &= \frac{I_{cp}}{2\pi}\frac{1}{sC_2} + \frac{BI_{cp}}{2\pi}\frac{1}{sC_1}e^{-s\Delta T} \\ &\approx \frac{I_{cp1}}{2\pi}\left(B\frac{\Delta T}{C_1} + \frac{1}{sC_2} + B\frac{1}{sC_1}\right) \end{aligned} \tag{6.14}$$

with a zero frequency of

$$\omega_z = \frac{C_1 / C_2 + B}{-B} \frac{1}{\Delta T} \tag{6.15}$$

Figure 6-8 (b) illustrates the switched-capacitor implementation of the delay line in Fig. 6-8 (a). Since the PLL reference frequency f_{ref} is usually much larger than the loop bandwidth, the interleaved switched-capacitor branch can be represented by an equivalent resistor $R_{eq} = \left(f_{ref} C_S\right)^{-1}$ for the continuous-time model shown in Fig. 6-8 (c). With charge-pump current of I_{cp}, the equivalent transimpedance of the loop filter is

$$Z_{lf}(s) = \frac{(1+B)\left(1 + sR_{eq}\frac{C_1}{1-\alpha}\right)}{s(C_1 + C_2)\left(1 + sR_{eq}\frac{C_1 \cdot C_2}{C_1 + C_2}\right)} \tag{6.16}$$

of which the zero frequency is

$$\omega_z = (1+B)\frac{C_S}{C_1} f_{ref} \tag{6.17}$$

Like the sample-reset loop filter, this loop filter has ω_z independent of process and temperature, and the large capacitance in the passive loop filter can be avoided. Unlike the dual-path loop filter, no charge pump needs to work with a small current. For example, with current ratio B =–0.9 it is equivalent to amplifying the value of C_1 by a factor of $(1+B)^{-1} = 10$.

As pointed out before, the active implementation of loop filter is very flexible. The loop filter topology in [13] and [14] is shown in Fig. 6-9. It can be interpreted as a dual-path loop filter with an integration path, a low-pass path, and a differential charge-pump (i.e., the current scaling factor is –1). The resistor in the low-pass path is implemented with a switched-capacitor. The frequency of the two non-overlapping switching clocks is the same as the reference frequency $f_{ref} = 20MHz$. The transimpedance of the loop filter is given by

$$Z_{lf}(s) = \frac{1}{sC_1} \frac{1 + s \cdot (C_1 + C_2 + C_3)/(f_{ref} C_4)}{1 + s \cdot C_3 / (f_{ref} C_4)} \tag{6.18}$$

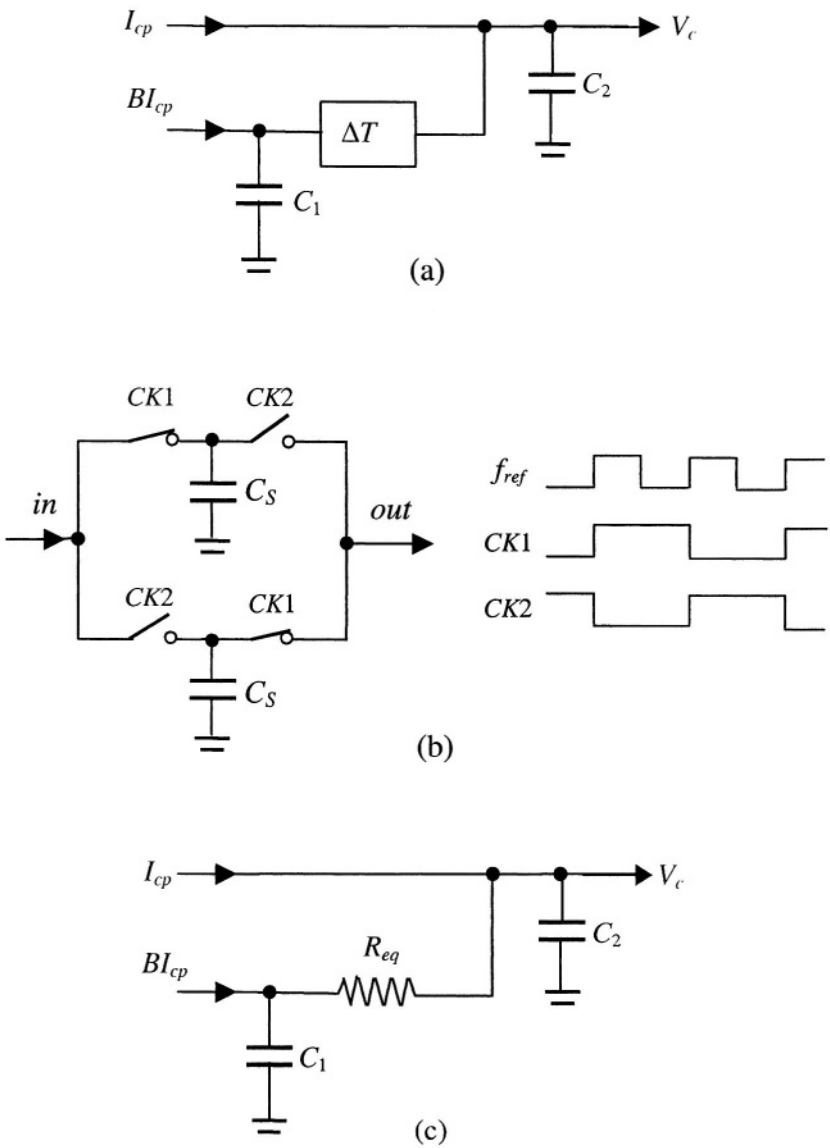


Figure 6-8. Loop filter in [12]

With the capacitors' values shown in Fig. 6-9, the zero frequency is

$$f_z = \frac{1}{2\pi}\frac{C_4}{C_1 + C_2 + C_3} f_{ref} = 10.6kHz \tag{6.19}$$

and the second pole frequency is

$$f_{p2} = \frac{1}{2\pi}\frac{C_4}{C_3} f_{ref} = 127kHz \tag{6.20}$$

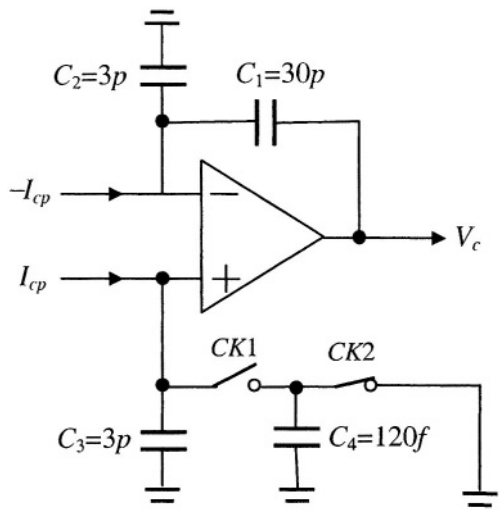


Figure 6-9. Loop filter in [13]

6.1.5 Summary and comparison of loop filters

Passive loop filters consist of resistors and capacitors only. The biggest capacitor might be too large for integration, and the zero and pole frequencies are susceptible to process variation. Active loop filters are more flexible and can provide larger tuning range, but they cost more power and introduce active noise. The largest capacitor in the passive filters can be scaled down by a factor of current or resistance ratios. A switched-capacitor can be used to replace the resistor, and it make some loop parameters proportional to capacitance ratios and be less sensitive to process variation. However, switched-capacitors introduce clock feedthrough and charge sharing. In conclusion, a comparison of different loop filter architectures is summarized in Table 6-1. Note that, as mention before, more disadvantages of some dual-path loop filters, such as voltage decay and small current in the integration paths, are not listed in the Table.

Table 6-1. comparison of existing loop filter architectures

architecure	features	pros	cons
passive	*R* and *C* only	no active noise	large C
active (basic)	OPA	large voltage, more flexibility	more power, active noise
dual-path	two CP, OPA	smaller C	more power, active noise
sample-reset [10]	two CP, OPA, SC	less ripple, smaller C, less sensitivity	more power, active noise, clock feedthrough, charge-sharing
Larsson [11]	buffer, R scaling	smaller C	more power, active noise
Lee [12]	two CP, SC	less ripple, smaller C, less sensitivity	active noise, clock feedthrough, charge-sharing
Perrott [13]	two CP, OPA, SC	less sensitivity	more power, active noise, clock feedthrough, charge-sharing

6.2 Loop filter and charge-pump noise mapping

Keep in mind that, as shown in PLL design examples, the bandwidth ω_c, VCO conversion gain K_{vco} and frequency divide ratio N are directly derived from synthesizer specifications and architecture. For a given bandwidth ω_c (see (3.7), (3.31), (3.37)) and loop zero ω_z (see (3.5)), products $I_{cp} \cdot R_1$ and $R_1 \cdot C_1$ are fixed. To reduce the size of C_1, we need to increase R_1 and hence to decrease I_{cp}. However, phase noises introduced by both I_{cp} and R_1 increase in doing so. To provide a quantitative insight into this issue, we calculate the PLL phase noise introduced by the loop filter and charge-pump in the example PLL for GSM in Chapter 4.

The third-order passive loop filter is again shown in Fig. 6-10. We want to map its resistance noise ($v_{nR}^2 = 4kTR$) to the PLL output phase noise.

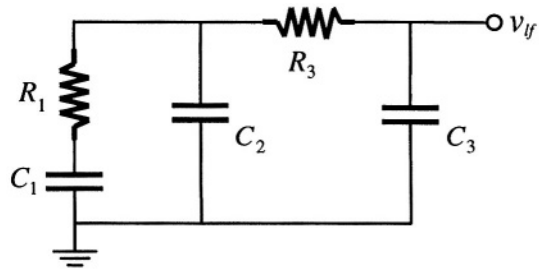


Figure 6-10. A third-order passive loop filter

First, we map the thermal voltage noise of the two resistors, R_1 and R_3 into the voltage noise at the loop filter output. The voltage transfer functions are as follows.

$$\frac{v_{lf}}{v_{nR1}}(s)=\frac{C_1}{C_1+C_2+C_3}\frac{1}{(1+s/\omega_{p2})(1+s/\omega_{p3})} \tag{6.21}$$

$$\frac{v_{lf}}{v_{nR3}}(s)=\frac{C_1+C_2}{C_1+C_2+C_3}\frac{1+sR_1C_1C_2/(C_1+C_2)}{(1+s/\omega_{p2})(1+s/\omega_{p3})} \tag{6.22}$$

As listed in Table 3-1, the loop filter control voltage noise to the PLL output phase noise transfer function is

$$\frac{\theta_{out}}{v_{lf}}(s)=\frac{N\cdot K_{vco}}{N\cdot s+K_{pd}K_{vco}Z_{lf}(s)} \tag{6.23}$$

The above transfer function for the example GSM PLL in Chapter 4 is plotted in Fig. 6-11. The phase noise contribution of loop resistors in the GSM PLL is illustrated in Fig. 6-12. We read that the phase noises generated by R_1 and R_3 at $600kHz$ offset are $-131dBc/Hz$ and $-125dBc/Hz$, respectively.

Denote the current noise of the charge-pump as i_{cp}. As listed in Table 3-1, we have

$$\frac{\theta_{out}}{i_{cp}}(s)=\frac{N\cdot K_{vco}Z_{lf}(s)}{N\cdot s+K_{pd}K_{vco}Z_{lf}(s)} \tag{6.24}$$

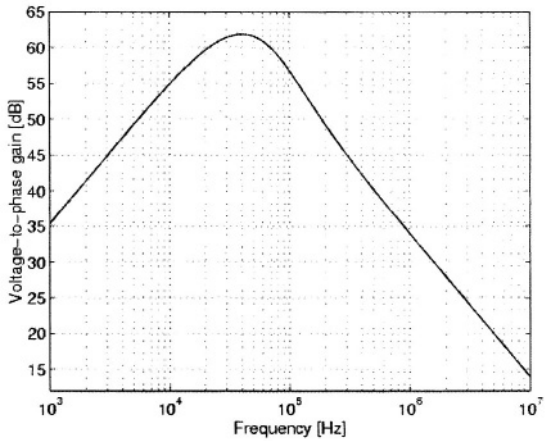


Figure 6-11. Loop filter noise transfer function of the GSM PLL

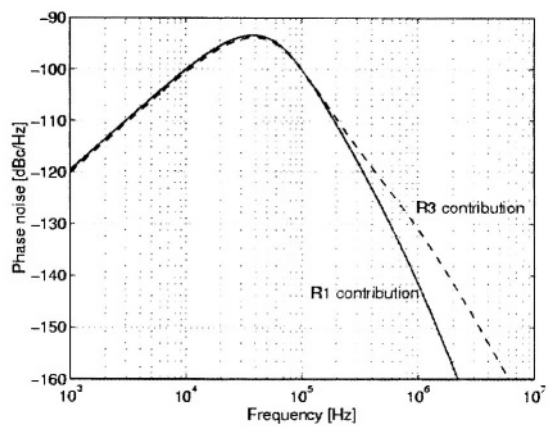


Figure 6-12. Loop filter induced phase noise in the GSM PLL

We consider the thermal noise the charge-pump current and neglect the flicker noise of the switches [15]. The charge pump current noise can be represented as [16]

$$i_{cp}^2 = 2\frac{t_{on}}{T_{ref}} \cdot 4kT \cdot \frac{2I_{cp}}{V_{od\_cp}} \tag{6.25}$$

where t_{on} is the turn-on time of the charge pump, $T_{ref} = 1/f_{ref}$ is the PFD update period, and V_{od_cp} is the gate-to-source overdrive voltage

($V_{GS} - V_T$) of the current source/sink transistor in the charge pump (see Fig. 3-4).

From (6.24) and (6.25), we find that for a given PLL bandwidth and a fixed V_{od_cp}, the PLL phase noise θ_{out}^2 is inversely proportional to charge-pump current I_{cp}. Figure 6-13 shows the phase noise contribution of the charge pump in the example GSM PLL. Here we use $t_{cp\_on} = 1ns$ and $V_{od\_cp} = 0.3V$. It indicates that the phase noise generated by the charge pump at $600kHz$ is $-143dBc/Hz$. Therefore, if we reduce the charge-pump current from $20\mu A$ to $20nA$, its phase noise contribution at $600kHz$ would be $-113dBc/Hz$, which is larger than the specification of $-121dBc/Hz$. On the other hand, when the charge-pump current I_{cp} is decreased by a factor of 1000, the loop resistance R_1 needs to be increased by the same factor of 1000. Then the phase noise induced by R_1 would be $-101dBc/Hz$ (=–131+30) at $600kHz$, which is much larger than the specified value of $-121dBc/Hz$. Moreover, when we scale down the charge-pump current and loop capacitance, the reference spur due to charge-injection and clock feed-through of switches also increases.

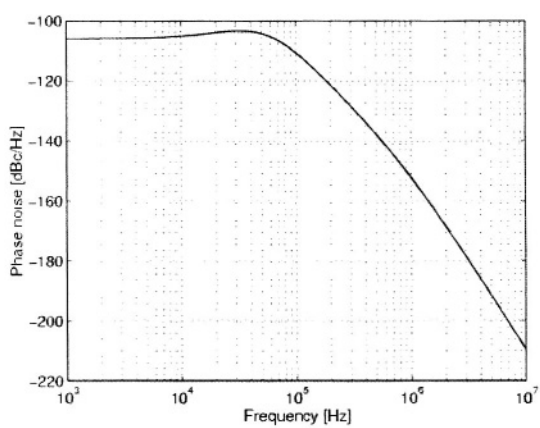


Figure 6-13. Charge pump induced phase noise in the GSM PLL

6.3 Loop filter with capacitance multiplier

6.3.1 Third-order passive loop filter

The third-order passive loop filter for the charge-pump PLL (see Fig. 6-1) is already discussed in detail in Chapter 3. In this work, the loop filter values are: $R_1 = 10k\Omega$, $C_1 = 160pF$, $C_2 = 10pF$, $R_3 = 1k\Omega$, and

$C_3 = 10pF$. With PLL bandwidth of about 270*kHz,* calculation from (3.36) shows that the PLL phase margin is about 51° .

6.3.2 Capacitance multiplier

To overcome the disadvantages of the dual-path topology, capacitance scaling technique [17], [18] was employed in the design of the third-order on-chip loop filter. In TSMC $0.35\mu m$ CMOS process, the $160pF$ poly-to-poly capacitor (C_1) would occupy about $0.2mm^2$ of die area. To reduce its area, it was built with a capacitor $C_i = 10pF$ scaled up by a factor of 16 as shown in Fig. 6-14. This capacitance multiplier is a special example of impedance scaling based on current amplifier shown in Fig. 6-15. The input impedance is

$$z_{in} = \frac{v_{in}}{i_{in}} = \frac{v_{in}}{(B+1)i_0} = \frac{Z_0}{B+1} \tag{6.26}$$

Thus, the impedance is scaled up if the current ratio $-1 < B < 0$. On the contrary, the impedance is scaled down if $B > 0$. In case of capacitance multiplier, the capacitance is scaled up by a factor of $B+1$ when $B > 0$.

To minimize the current leakage at node **A**, cascode current mirrors with long-channel transistors are used. The equivalent small signal admittance at the input terminal is:

$$y_{in} = \frac{i_{in}}{v_{in}} = g_{oA} + s\left[C_{p2} + (B+1)C_i \frac{1 + s\dfrac{C_{p1}}{(B+1)g_{m1}}}{1 + s\dfrac{C_i + C_{p1}}{g_{m1}}} \right] \tag{6.27}$$

C_{p1} and C_{p2} are parasitic capacitors at node **A** and **B**, respectively. Usually, $C_{p1} << C_i$ and $C_{p2} << C_{p1}$ because C_{p1} includes the large parasitic capacitance between the bottom plate of poly-poly capacitor C_i and ground. g_{m1} is the transconductance of transistor M1, and g_{oA} is the overall conductance at node **A**. B = 15 is the current gain of the current mirror (or current amplifier).

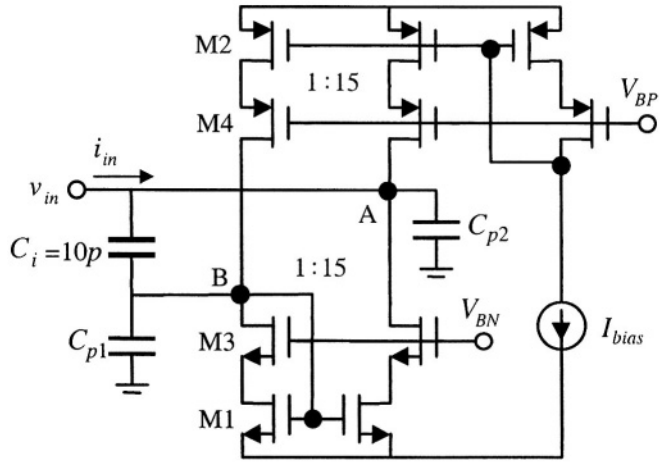


Figure 6-14. Capacitance multiplier

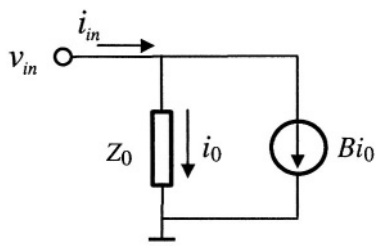


Figure 6-15. Impedance scaling based on current amplifier

Figure 6-16 shows the simulated frequency responses of $1/y_{in}$ in comparison with an ideal $160pF$ capacitor. The three corner frequencies of $1/y_{in}$ are:

$$\omega_{c1} = \frac{g_{oA}}{C_{p2} + (B+1)C_i} \approx \frac{g_{oA}}{C_1} \tag{6.28}$$

$$\omega_{c2} = \frac{g_{m1}}{(C_i + C_{p1})} \approx \frac{(B+1)g_{m1}}{C_1} \tag{6.29}$$

and

$$\omega_{c3} = \frac{(B+1)g_{m1}}{C_{p1}} \tag{6.30}$$

ω_{c1} and ω_{c3} are poles while ω_{c2} is a zero. y_{in} can be approximated in the four frequency ranges separated by the above three corner frequencies as follows:

1) At very low frequencies, i.e., $\omega < \omega_{c1}$,

$$y_{in} \approx g_{oA} \tag{6.31}$$

2) In the frequency range of $\omega_{c1} < \omega < \omega_{c2}$,

$$y_{in} \approx s\left(C_{p2} + (B+1)C_i\right) \approx sC_1 \tag{6.32}$$

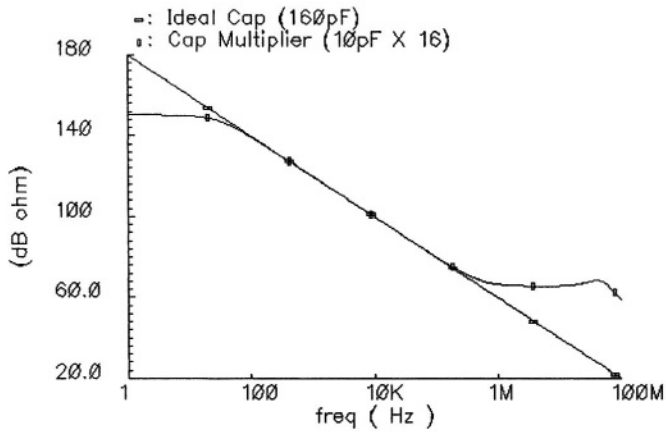
which is the intended capacitance.

3) In the frequency range of $\omega_{c2} < \omega < \omega_{c3}$,

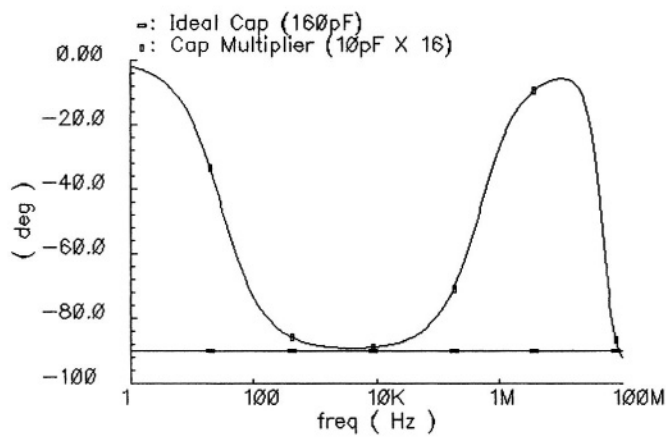
$$y_{in} \approx sC_{p2} + \frac{(B+1)C_i}{C_i + C_{p1}} g_{m1} \approx (B+1)g_{m1} \tag{6.33}$$

4) At very high frequencies, i.e., $\omega > \omega_{c3}$,

$$y_{in} \approx s\left(C_{p2} + \frac{C_i C_{p1}}{C_i + C_{p1}}\right) \approx sC_{p1} \tag{6.34}$$



(a) Magnitude



(b) Phase

Figure 6-16. Simulated capacitance multiplier impedance

6.3.3 Simulation of loop filter with capacitance multiplier

The following two constraints on the corner frequencies of the scaled capacitance are imposed for this application:

i) To minimize the current leakage, a small value of g_{oA} is needed to make ω_{c1} as low as possible. Also, the current mismatch between the top and bottom sources at node **A** should be minimized.

ii) To keep the PLL's phase margin unchanged, it is desirable that the second corner frequency ω_{c2} should be much larger than the zero of the loop filter ω_z, i.e., $\omega_{c2} >> \omega_z$.

The first requirement can be easily met by using cascode current mirrors with long-channel transistors, but the second requirement may not be satisfied in some cases. Therefore, we need to investigate the impact on the loop filter's frequency response when $\omega_{c2} >> \omega_z$ is not satisfied.

In the frequency range of $\omega_{c1} << \omega << \omega_{c3}$, from (6.27), we have:

$$y_{in} \approx \frac{s(B+1)C_i}{1+s\dfrac{C_i}{g_{m1}}} = \frac{1}{\dfrac{1}{sC_1}+\dfrac{1}{(B+1)g_{m1}}} \tag{6.35}$$

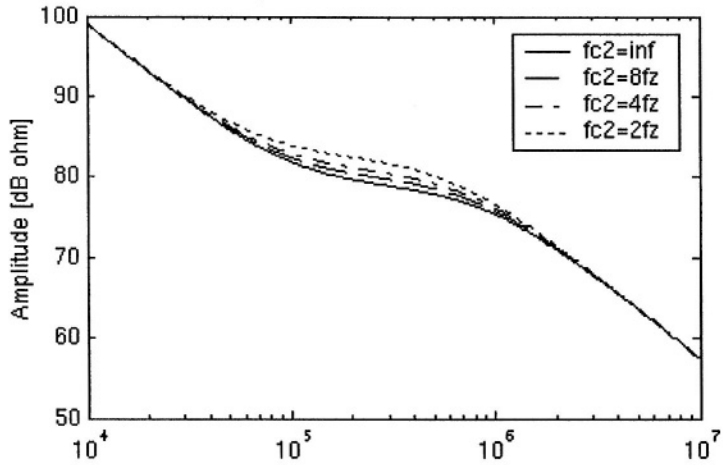
Thus in this frequency range, the capacitance multiplier is equivalent to the desired capacitance C_1 in series with a resistance of $[(B+1)g_{m1}]^{-1}$ value. Since R_1 is in series with the capacitance multiplier, then the overall resistance is increased and the zero of the loop filter becomes:

$$\omega_z' = \frac{1}{\left(R_1+\dfrac{1}{(B+1)g_{m1}}\right)C_1} = \frac{\omega_z}{1+\dfrac{1}{(B+1)g_{m1}R_1}} \tag{6.36}$$

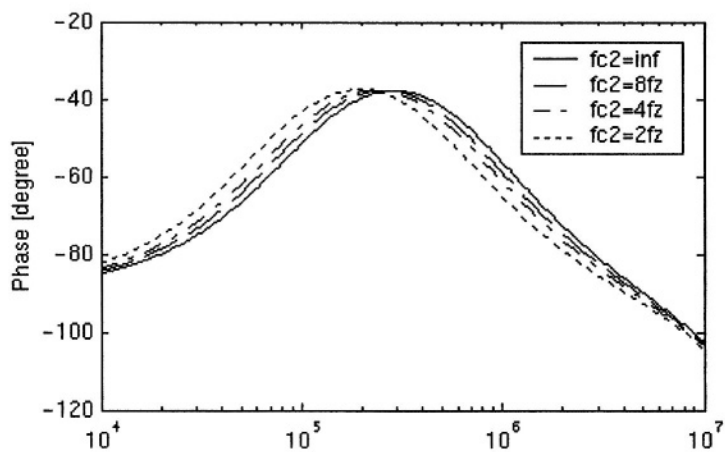
Figure 6-17 illustrates the frequency responses of the loop filter's magnitude and phase with ω_{c2} equal to $2\omega_z$, $4\omega_z$, $8\omega_z$ and infinite (ideal case), respectively. It shows that the deviation of frequency response from ideal case is negligible when $\omega_{c2} \geq 4\omega_z$, i.e.,

$$g_{m1} \geq \frac{4}{(B+1)R_1} \tag{6.37}$$

Otherwise, the PLL's open-loop crossover frequency ω_c increases (Fig. 6-18 (a)) while the frequency corresponding to the maximum phase margin decreases (Fig. 6-18 (b)). Therefore, we need to reduce the value of R_1 by the amount of $[(B+1)g_{m1}]^{-1}$ to keep loop parameters unchanged. This imposes that $[(B+1)g_{m1}]^{-1}$ should never be grater the nominal value of R_1. The simulated frequency responses of this loop filter with scaled capacitor and non-scaled capacitor, respectively, is shown in Fig. 6-18. It indicates that the resistance at node **A** ($=1/g_{oA}$) is around $30M\Omega$, which is large enough to make the current leakage negligible, and one can say that the capacitance multiplier emulates a large grounded capacitance very well in this application.

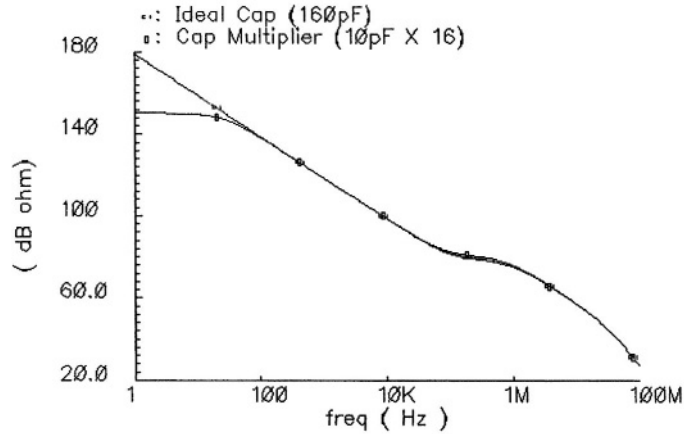


(a) Magnitude vs. frequency

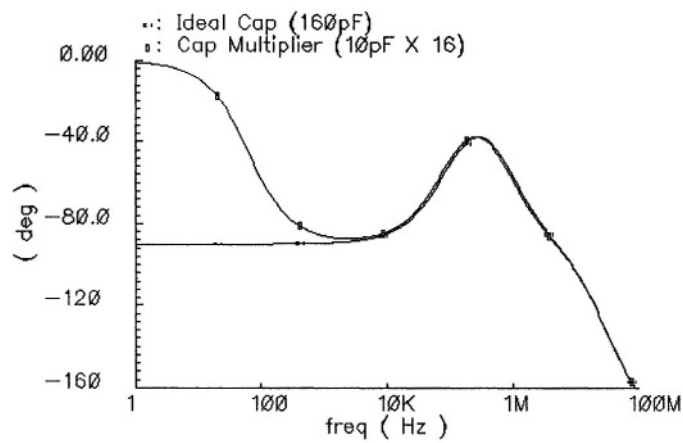


(b) Phase vs. frequency

Figure 6-17. Effects of limited f_{c2} on loop stability



(a) Magnitude vs. frequency



(b) Phase vs. frequency

Figure 6-18. Simulated loop filter transimpedance with capacitance multiplier

6.3.4 Noise consideration

Finally, we must check the noise introduced by the capacitance multiplier to make sure that it is negligible. We consider the phase noise caused by the capacitance multiplier at $1MHz$ offset because the phase noise requirement around $1MHz$ is the most stringent for most of the wireless applications. Since the thermal noise dominates at $1MHz$, a simple way is to compare the equivalent noise resistance of the capacitance multiplier with R_1. From Fig 6-16 (a) and the analysis made before, we know that the admittance of the capacitance multiplier at $1\,MHz$ is approximately $(B+1)g_{m1}$. Neglecting the

minimized noise of the bias, the voltage noise density of the capacitance multiplier is approximately given by:

$$v_n^2 = \frac{8kT}{3(B+1)g_{m1}}\left(1 + g_{m2}/g_{m1}\right) \tag{6.38}$$

g_{m2}, which is the transconductance of transistor M2, can be less than g_{m1} for noise optimization, but let us consider the case $g_{m2} \approx g_{m1}$, then (6.38) yields:

$$v_n^2 = \frac{16kT}{3(B+1)g_{m1}} \tag{6.39}$$

Therefore, the thermal noise produced by the capacitance multiplier is equivalent to the one generated by a resistance of $\frac{4}{3(B+1)g_{m1}}$ value. To make the noise contribution from capacitance multiplier at $1MHz$ negligible, we need to have $\frac{4}{3(B+1)g_{m1}} \le R_1$, i.e.:

$$g_{m1} \ge \frac{4}{3(B+1)} \cdot \frac{1}{R_1} \tag{6.40}$$

As far as the noise contribution from R_1 [19] is negligible for a certain application, the noise contributed by the capacitance multiplier is also negligible.

In this design, the sizes of transistors M1 ~ M4 are 12/2, 6/3, 12/3 and 12/3 in the unit of μm, respectively. The dc current of this branch is $5\mu A$. $g_{m1} \approx 0.1\,mA/V$, which is large enough to satisfy conditions in (6.37) and (6.40). This capacitance multiplier consumes only $0.2mW$ including its bias.

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Chapter 7

OTHER BUILDING BLOCKS OF PLL

This chapter covers the design of PLL synthesizer blocks of the experimental PLL prototype other than the prescaler and loop filter. General analysis and design techniques of each building block are overviewed. The analysis methods of the VCO phase noise are summarized. A complete analysis of the reference spur is also made in this chapter.

7.1 VCO

Basically, there are two types of on-chip VCO's for high frequency PLL's: the ring oscillator and the *LC*-tuned oscillator. The ring oscillator consists of a number of delay stages. It usually takes less area and has a large tuning range. The *LC* oscillator often takes more chip area due to spiral inductors and has a smaller tuning range, but it can run at a much higher frequency and generally its phase noise is better.

7.1.1 LC-VCO

Figure 7-1 shows the schematic of the *LC*-VCO. Cross-coupled transistors M1 and M2 are used to generate a negative resistance to compensate the parasitic parallel resistance of *LC* tank for oscillation to occur. M3 and M4 are used to generate bias current. M5 and M6 are used as varactors for frequency tuning [1]-[4].

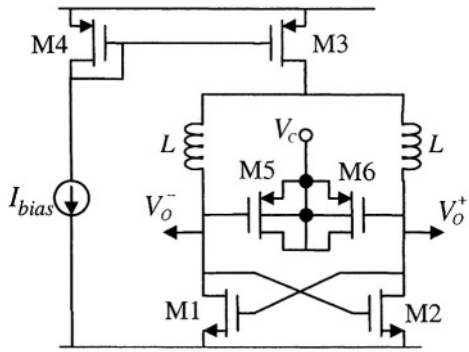


Figure 7-1. LC-VCO schematic

Efforts are put on the robust connection between the VCO and the prescaler, which are the two RF blocks in the PLL prototype. The DC level of the VCO output matches that of the pseudo-differential input NMOS pairs in the prescaler. Therefore, the VCO can drive the prescaler directly and robustly. No RF buffer, or AC coupling capacitor, or DC bias of the prescaler input, is needed in this scheme.

7.1.2 Varactor

A. Diode varactor

The reverse-biased diode, which is usually made of p-diffusion in n-well can be used as a varactor. It is a lateral device consisting of p^+-n^--n^+diffusion sequence. Since the n-well has a high resistivity (at least hundreds of Ω/square), the parasitic resistance introduced by the diode varactor is of a big concern. Efforts in optimizing the layout have been made in the literature to reduce the parasitic resistance [5]-[7]. Also caution should be used to keep the diode varactor working in reverse-biased mode in the VCO tuning range and oscillating range.

B. PMOS varactor

The well-known *C-V* characteristic of MOS transistor can be employed as a varactor for *LC*-VCO. The gate-to-substrate capacitance of a MOS transistor, C_{mos}, varies with the voltage drop between substrate and gate, V_{BG}. Usually, the *C-V* characteristic of a MOS transistor is for a very small v_{bg} signal superimposed on bias voltage V_{BG}. If the LC-VCO, the signal v_{bg} is large and the instantaneous value of C_{mos} changes through the

oscillating period, nut the average value of C_{mos} still varies with control voltage V_{BG}.

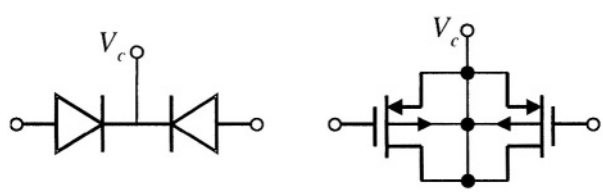
For a p-sub, n-well CMOS process, the MOS varactor can be two PMOS sharing the same n-well. The bias of the n-well, which is the substrate of the two PMOS transistors, is used as the frequency control node of the VCO. To reduce the parasitic resistance of MOS varactor, minimum channel length should be used to minimize the channel resistance, and the multi-finger layout is used to reduce the resistance of the poly gate. The Q of a MOS varactor is roughly proportional to the reverse of channel length and the typical Q value is between 10 and 100 [7]-[10].

C. Inversion-mode PMOS varactor (I-MOS)

Since the MOS transistor has a non-monotonic C-V characteristic, the VCO with PMOS varactors shows a non-monotonic tuning characteristic. One way to obtain a quasi-monotonic tuning characteristic MOS varactor is by ensuring that the transistor does not enter the accumulation region for a very wide range of values of V_G. This is accomplished by connecting the substrate to the highest DC voltage, i.e., V_{DD}.

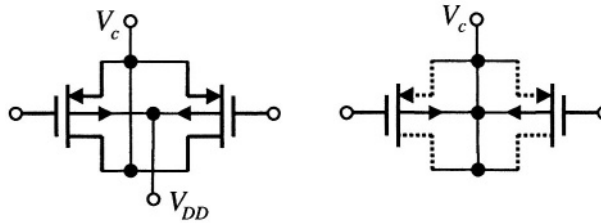
D. Accumulation-mode PMOS varactor (A-MOS)

A more attractive alternative is the use of the PMOS device in the depletion and accumulation regions only [8], [10] to ensure that the formation of the strong, moderate, and weak inversion regions is inhibited, which requires the suppression of hole-injection in the channel. This, in turn, can be accomplished by replacing p^+-diffusion (source and drain) with n^+-diffusion (same as n-well contacts). It can also be regarded as a NMOS transistor made in the n-well.



(a) Diode (b) PMOS

Figure 7-2. Different types of varactors



(c) I-MOS (d) A-MOS

Figure 7-2. Different types of varactors (continued)

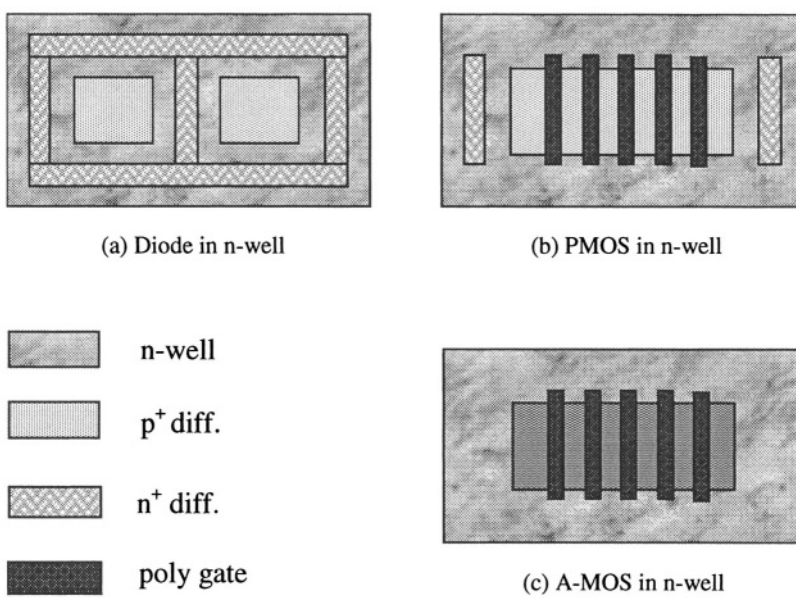


Figure 7-3. Top view of varactors in CMOS technology

Figure 7-2 shows four types of varactors used for *LC*-VCO in CMOS technology. The top views of diode and MOS varactors are illustrated in Fig. 7-3. The *C*-*V* characteristics of the I-MOS and A-MOS varactor compared with the one of the PMOS varactor are illustrated in Fig. 7-4.

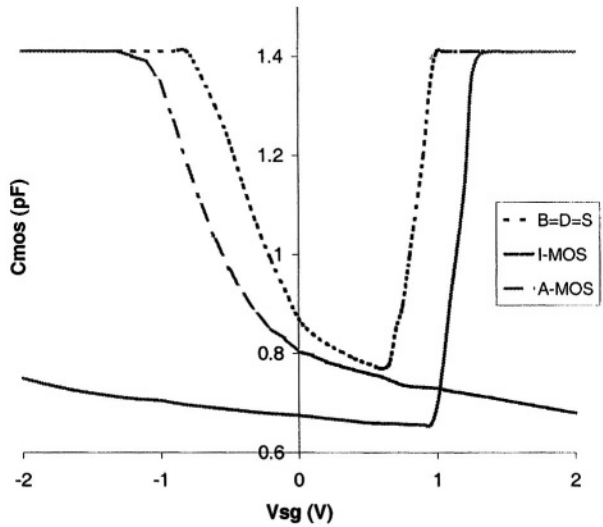


Figure 7-4. C-V characteristic of MOS capacitors

7.1.3 Inductor

On-chip inductors for *LC*-VCO's have been widely investigated in the literature [11]-[21]. The mostly used approach is the spiral inductor made of metal tracks available in the standard digital CMOS process. A spiral inductor can be made of single metal layer or multiple metal layers. For single layer implementation, we use the top metal layer, which is furthest from the conductive substrate and is usually the thickest metal layer. The large distance to the substrate reduces the magnetic coupling with the conductive substrate. The top metal layer has the smallest resistance due to its thickness. These two factors help increase the quality (Q) factor of spiral inductors. The multi-layer series spiral inductor is also often used because of its smaller chip area compared with the planar spiral inductor. The substrate coupling effect is alleviated with smaller chip area. Multi-layer parallel inductor is sometimes used to reduce the series resistance of metal tracks. The typical Q of on-chip spiral inductors is less than 5 in standard digital CMOS [22], [23].

Another approach is to make use of the inductance of on-chip bondwires [24]. Compared with the spiral inductor, the bondwire inductor has superior performances. Its Q is around 30 to 50. The main concern in the use of bondwires as tank inductors is that their values are affected by a large spread.

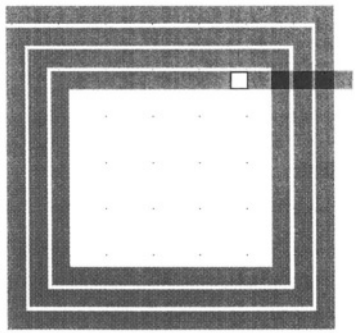


Figure 7-5. On-chip spiral inductor

The spiral inductor designed in this work is shown in Fig. 7-5. It is built with metal4 tracks. The outside dimension is $140\mu m$. The metal track width and spacing are $8.5\mu m$ and $1.5\mu m$, respectively. ASITIC [17] is used to simulate the inductance value and quality factor. The simulated inductance and quality factor are $2.02nH$ and 4.5, respectively. The inductor's quality factor is overestimated because eddy current is not considered. Characterization of spiral inductors in a similar CMOS process shows that the actual quality factor is even less than half of the simulated value [25].

The design parameters of the *LC*-VCO (see Fig. 7-1) are summarized in Table 7-1.

Table 7-1. Design parameters of LC-VCO

M1/M2	M3	M4	M5/M6	*L*
36(10μ/0.4μ)	160(24μ/0.8μ)	20(24μ/0.8μ)	150(5μ/0.4μ)	$2.02nH$

7.1.4 VCO phase noise

The oscillator's phase noise model, which has historically been used to describe oscillator's phase noise, was heuristically deduced by Leeson [26]. This model is widely used throughout industry. Based on this model, the oscillator's single-sideband phase noise spectrum is given by

$$\pounds(\Delta f) = \frac{2FkT}{P_s}\left[1+\left(\frac{f_0}{2Q_L\Delta f}\right)^2\right]\left(1+\frac{\Delta f_{1/f^3}}{|\Delta f|}\right) \tag{7.1}$$

where

F = active device noise factor

k = Boltzmann constant (1.3807×10^{-23} *Joules/Kelvin*)

T = temperature
P_s = output power
f_0 = oscillator center frequency
Q_L = loaded resonator quality factor
Δf = frequency offset from carrier
$\Delta f_{1/f^3}$ = corner frequency of $1/f^3$ phase noise

This linear time-invariant (LTI) model can be derived by the noise shaping due to the band-pass *LC* filtering effect. A simple model for the *LC* oscillator is shown in Fig. 7-6. The impedance for parallel *RLC,* for $\Delta f << f_0$, is

$$Z(f_0 + \Delta f) = \frac{1}{G_L} \cdot \frac{1}{1 + j2Q_L(\Delta f / f_0)} \tag{7.2}$$

where G_L is the parallel conductance of the tank. At steady state oscillation, we have $G_m = G_L$. Therefore, for a parallel current source, the closed-loop transfer function of the oscillator is given by the imaginary part of the impedance in (7.3).

$$H(\Delta f) = \frac{v_{out}(\Delta f / f_0)}{i_{in}(\Delta f / f_0)} = -j\frac{1}{G_L} \cdot \frac{f_0}{1 + j2Q_L\Delta f} \tag{7.3}$$

The current noise of the equivalent parallel resistance is:

$$\overline{i_n^2} / \Delta f = 4FkTG_L \tag{7.4}$$

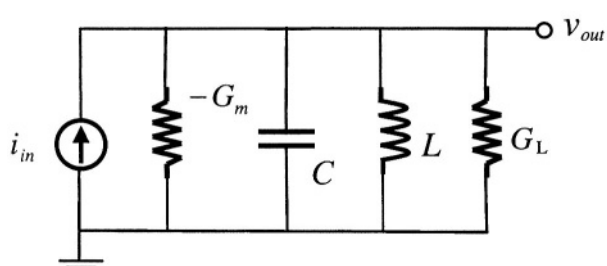


Figure 7-6. Simple *LC* oscillator noise model

where F is the excess noise factor. Therefore, the phase noise in the $1/f^2$ region is

$$\begin{aligned} \pounds(\Delta f) &= 10\log\left(\frac{\overline{v_n^2}}{v_s^2}\right) \\ &= 10\log\left(\frac{1/2\cdot|H(\Delta f)|^2\overline{i_n^2}/\Delta f}{1/2\cdot V_{\max}^2}\right) = 10\log\left[\frac{2FkT}{P_s}\left(\frac{f_0}{2Q_L\Delta f}\right)^2\right] \end{aligned} \tag{7.5}$$

Note that, the $1/f^3$ portion of the phase noise is completely empirical. In reality, both the $1/f^3$ and $1/f^2$ phase noise are generated by noise upconversion due to phase modulation and other nonlinear effects in VCO instead of noise shaping of *LC* filtering.

Furthermore, Lesson's phase noise model for the *LC*-VCO was extended to the ring oscillator by defining an effective Q factor of the latter one [27].

Hajimiri *et al.* developed a more accurate phase noise model for oscillators [28]-[32], which acknowledges the true periodically time-varying nature of all oscillators. This model is based on linear time-varying periodical analysis of an oscillator's impulse response of excess phase to current injection at a certain node.

First, the linear relationship between the injected charge to a certain node in the oscillator and the excess phase at the oscillator's output is verified through both simulation and experiment. The unit impulse response for the excess phase to the injected charge is:

$$h_\phi(t,\tau) = \frac{\Gamma(\omega_0\tau)}{q_{\max}}\cdot u(t-\tau) \tag{7.6}$$

where $u(t-\tau)$ is a step function, $q_{\max}$ is the maximum charge swing across the capacitor on the node of interest, and $\Gamma(\omega_0\tau)$ is defined as an impulse sensitivity function (ISF), where ω_0 is the oscillating frequency. Thus, the excess phase can be calculated as:

$$\phi(t) = \int_{-\infty}^{\infty} h_\phi(t,\tau)\cdot i(\tau)d\tau = \frac{1}{q_{\max}}\int_{-\infty}^{t}\Gamma(\omega_0\tau)i(\tau)d\tau \tag{7.7}$$

Since $\Gamma(\omega_0\tau)$ is periodic, it can be expanded into a Fourier series,

$$\Gamma(\omega_0\tau) = \frac{c_0}{2} + \sum_{n=1}^{\infty} c_n \cos(n\omega_0\tau) \tag{7.8}$$

The excess phase becomes

$$\phi(t) = \frac{1}{q_{\max}}\left[\frac{c_0}{2}\int_{-\infty} i(\tau)d\tau + \sum_{n=1}^{\infty} c_n \int_{-\infty} i(\tau)\cos(n\omega_0\tau)d\tau\right] \tag{7.9}$$

Applying a current $i(t) = I_n \cos[(n\omega_0 + \Delta\omega)t]$ close to any integer multiple of the oscillation frequency will result two equal sidebands at $\pm\Delta\omega$ in $S_\phi(\omega)$, because the excess phase is

$$\phi(t) \approx \frac{I_n c_n \sin(\Delta\omega \cdot t)}{2q_{\max}\Delta\omega} \tag{7.10}$$

The resulting sideband power relative to the carrier is given by

$$P_{SBC}(\Delta\omega) = 10\log\left(\frac{I_n c_n}{4q_{\max}\Delta\omega}\right)^2 \tag{7.11}$$

Consider an input noise current with a white PSD $\overline{i_n^2}/\Delta f$. (7.5) becomes

$$\pounds(\Delta\omega) = 10\log\left(\frac{\Gamma_{rms}^2}{q_{\max}^2}\frac{\overline{i_n^2}/\Delta f}{2\Delta\omega^2}\right) \tag{7.12}$$

where Γ_{rms} is the *rms* value of $\Gamma(\omega_0\tau)$, and

$$\Gamma_{rms}^2 = \frac{1}{2\pi}\int_0^{2\pi} |\Gamma(x)|^2 dx = \frac{1}{2}\sum_{n=0}^{\infty} c_n^2 \tag{7.13}$$

Similarly, applying flick noise current

$$\overline{i_{n,1/f}^2}/\Delta f = \overline{i_n^2}\frac{\omega_{1/f}}{\Delta\omega} \tag{7.14}$$

The $1/f^3$ phase noise is

$$\pounds(\Delta\omega) = 10\log\left(\frac{c_0^2}{q_{\max}^2}\frac{\overline{i_n^2}/\Delta f}{8\Delta\omega^2}\frac{\omega_{1/f}}{\Delta\omega}\right) \tag{7.15}$$

The $1/f^3$ phase noise corner is given by

$$\omega_{1/f^3} = \omega_{1/f}\frac{c_0^2}{4\Gamma_{rms}^2} \approx \omega_{1/f}\frac{1}{2}\left(\frac{c_0}{c_1}\right)^2 \tag{7.16}$$

Furthermore, in addition to the periodically time-varying nature of the system itself, some of the oscillator's noise sources are cyclostationary. Consider a white cyclostationary noise current $i_n(t)$ decomposed as:

$$i_n(t) = i_{n0}(t)\cdot\alpha(\omega_0 t) \tag{7.17}$$

where $i_{n0}(t)$ is a white stationary process and $\alpha(\omega_0 t)$ is a normalized deterministic periodic function describing the amplitude modulation. Applying (7.13) into (7.3), the excess phase is given by

$$\phi(t) = \frac{1}{q_{\max}}\int_{-\infty}^{t} i_{n0}(\tau)\cdot\alpha(\omega_0\tau)\Gamma(\omega_0\tau)d\tau \tag{7.18}$$

So the cyclostationary noise source can be treated as a stationary noise source with an effective ISF given by

$$\Gamma_{eff}(\omega_0\tau) = \alpha(\omega_0\tau)\cdot\Gamma(\omega_0\tau) \tag{7.19}$$

In comparison, the traditional phase noise model, in which only the noise around ω_0 is converted into phase noise, is equivalent to discard all but $c_1 = 1$ with $F = 2\Gamma_{rms}$ and $\omega_{1/f^3} = \omega_{1/f}\cdot c_0^2/\Gamma_{rms}^2$.

The phase noise result from this time-variant analysis agrees well with the commercially available software packages for phase noise simulation, such as SpectreRF and EldoRF [33]. However, the calculation of ISF for this model is not easy [28].

The limitation of phase noise models based on the linear perturbation analysis, either time-invariant or time-variant, can be seen from (7.1), (7.12), and (7.15). These formulas become invalid when frequency offset, Δf, approaches zero, because they predict infinite noise power density at the carrier as well as infinite total integrated noise power. More recently, a

unifying theory and numerical methods for characterizing phase noise in oscillators were proposed by Demir *et al.* in [34] and [35]. This general noise model for autonomous oscillators is based on nonlinear perturbation analysis. For example, the phase noise formula for white noise source [34] (see (2.21)) is

$$\pounds(\Delta f) = 10\log\left(\frac{f_0^2 c}{\left(\pi f_0^2 c\right)^2 + \Delta f^2}\right) \tag{7.20}$$

where the constant c [in $s^2 \cdot Hz$] describes all white noise contributions in the oscillator. As mentioned in section 2.2 (see (2.20)), this phase noise model in equivalent to the one in [36]. The phase noise model with colored-noise sources (e.g., $1/f$ noise) is more complicated and can be found in [35]. This rigorous and exact phase noise model has a finite value at $\Delta f = 0$. It eliminates errors of models based on linear analysis, and applies to any oscillatory system described by differential equations. The PSD of an ideal sine wave oscillator output is a δ function at f_0. The phase noise in a real oscillator spreads the carrier power in the δ function as given in (7.20).

Finally, the above models do not provide the direct relationship between noise sources (device, supply, and substrate noise) and the oscillator phase noise, because all this information is indirectly hidden behind some constants in the models. On the contrary, the noise analyses in other literatures help understand the noise upconversion mechanism in oscillators more directly and provide some helpful design implications [36]-[54].

7.1.5 Layout

Attention has been paid to the symmetry in the VCO layout. Noises from the substrate, supply and cross-talk are minimized. The layout of the *LC*-VCO is shown in Fig. 7-7.

The spiral inductor shown in Fig. 7-7 was shielded with patterned ground shield (PGS) that consists of poly layer with slots orthogonal to the spiral [20]. The ground strips are merged together around the four outer edges of the spiral, but no closed ring is formed about the spiral to avoid unwanted loop current. Transistor pairs, M1-2 and M5-6 (see Fig. 7-1), are laid out with interdigitized and common-centroid geometries for good matching. Big sizes of PMOS bias current mirror, M3-4, help reduce the $1/f$ noise, and their big parasitic capacitance help reduce VCO phase noise [55]-[57]. Open-drain NMOS buffers are used for VCO output measurement [9].

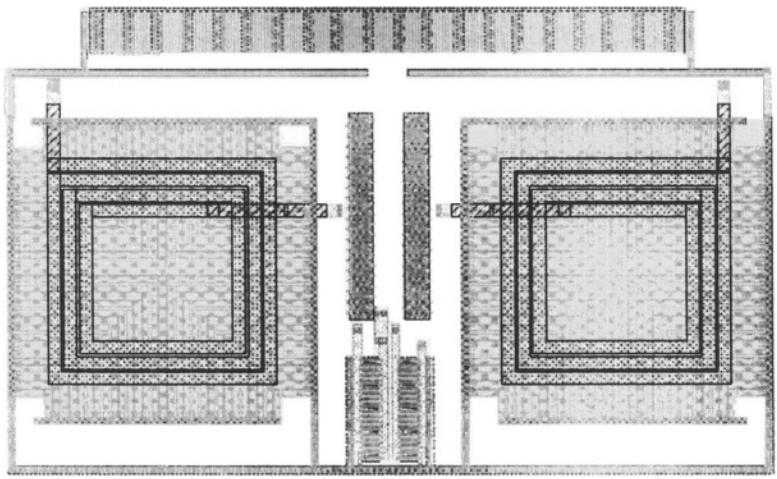


Figure 7-7. Layout of the LC-VCO

7.2 Phase-frequency detector

Dynamic implementations of the flip-flops for PFD (see Fig. 3-2) are shown in Fig. 7-8 [58]-[60]. It is a simplified version of the high-speed TSPC flip-flop [61] since the flip-flop's input *D* is always tied to 1.

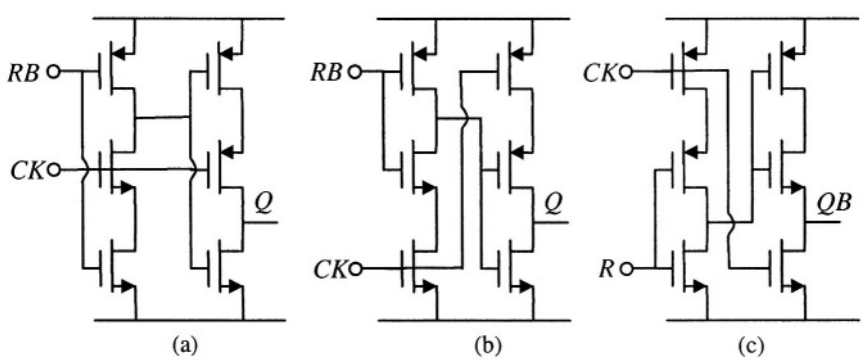


Figure 7-8. Implementations of dynamic FF for PFD

Alternative implementations of PFD, the so-called precharge PFD [62] and a simplified precharge PFD [63], are shown in Fig. 7-9. Note that, the simplified version is sensitive to the duty cycles of two input signals. Other variations of precharge PFD can be found in [64]-[66].

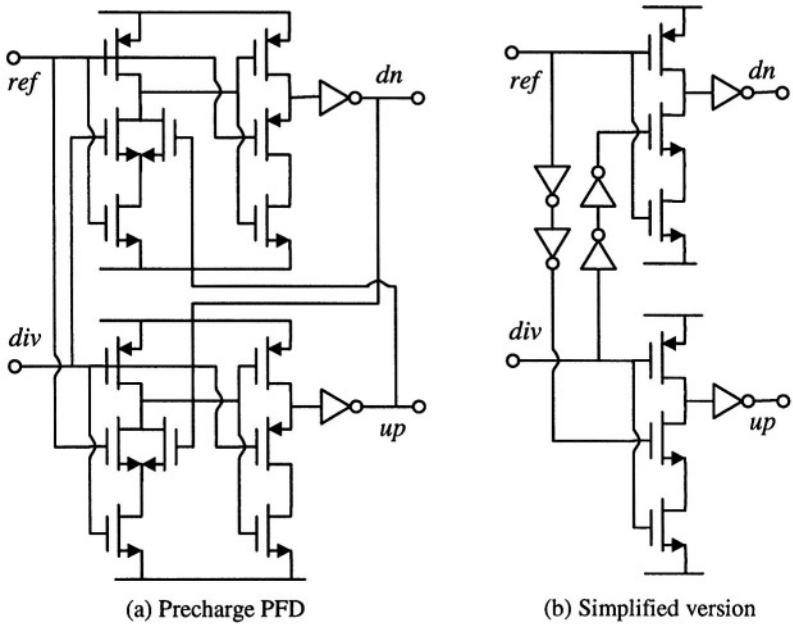


Figure 7-9. Other implementations of PFD

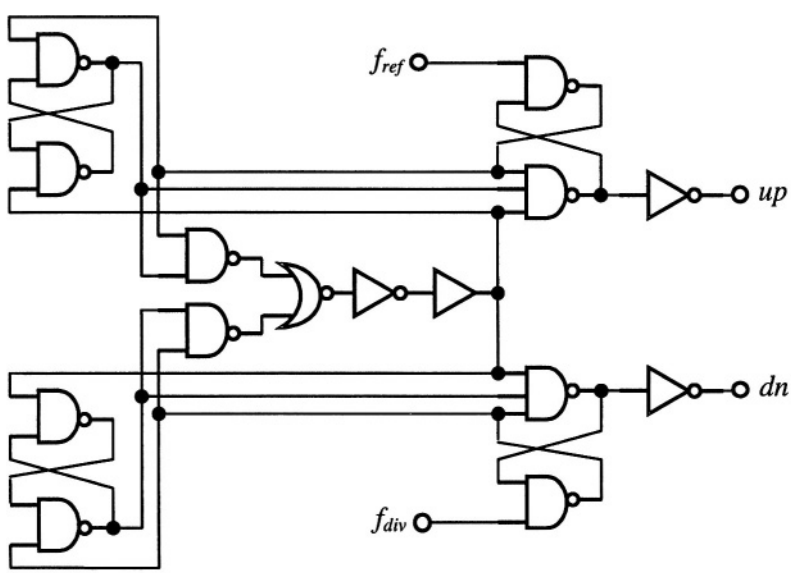


Figure 7-10. PFD using *RS* latch

The PFD used in this design is the one illustrated in Fig. 7-10. It is an asynchronous state machine based on *RS* latches and is widely used in the literature [5], [67]-[69].

7.3 Charge pump

7.3.1 Reference spur

The conceptual diagram of the charge pump is shown in Fig. 7-11. It consists of two switched current sources driven by the tri-state PFD. The width of the output current (I_{out}) pulse is proportional to the phase error (θ_e) at the PFD inputs. Thus the phase error is converted into a proportional amount of charge at the charge pump output.

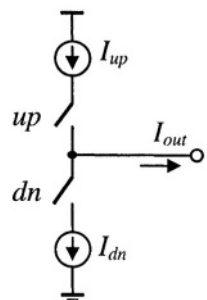


Figure 7-11. Conceptual diagram of charge pump

In the PLL, the reference frequency modulates the VCO generating sidebands around the carrier. Ideally, the charge and discharge currents are equal, that is, $I_{up} = I_{dn} = I_{cp}$. Therfore in the locked-state, the VCO control voltage (V_c) variation is only due to noises in the PLL. In practice, the nonidealities of the charge-pump cause periodic ripples on V_c.

Since the variation of V_c is very small in the locked-state, the narrow-band frequency modulation (FM) theory is reviewed here. The VCO output is expressed as:

$$V_{out}(t) = V_0 \cos\left[\omega_0 t + K_{vco}\int_0^t V_c(\tau)d\tau + \theta_0\right] \tag{7.21}$$

In the case of narrow-band FM, the maximum phase deviation $\Delta\phi$ is much less than $\pi/2$, that is:

$$\Delta\phi = \left| K_{vco} \int_0^t V_c(\tau) d\tau \right|_{\max} << \frac{\pi}{2} \tag{7.22}$$

Suppose the initial phase $\theta_0 = 0$, (7.21) yields:

$$\begin{aligned} V_{out}(t) &= V_0 \cos\left[\omega_0 t + K_{vco} \int_0^t V_c(\tau) d\tau \right] \\ &= V_0 \cos(\omega_0 t)\cos\left[K_{vco} \int_0^t V_c(\tau) d\tau \right] - V_0 \sin(\omega_0 t)\sin\left[K_{vco} \int_0^t V_c(\tau) d\tau \right] \\ &\approx V_0 \cos(\omega_0 t) - V_0 K_{vco} \int_0^t V_c(\tau) d\tau \cdot \sin(\omega_0 t) \end{aligned} \tag{7.23}$$

Let $V_c(t)$ be a sinusoidal signal with the reference frequency:

$$V_c(t) = A_m \cos(\omega_{ref} t) \tag{7.24}$$

Then (7.22) and (7.23) reduce to the following:

$$\Delta\phi = \left| K_{vco} \int_0^t A_m \cos(\omega_{ref} \tau) d\tau \right|_{\max} = \frac{K_{vco} A_m}{\omega_{ref}} \tag{7.25}$$

$$V_{out}(t) \approx V_0 \left[\cos\omega_0 t - \frac{\Delta\phi}{2}\cos(\omega_0 - \omega_{ref})t + \frac{\Delta\phi}{2}\cos(\omega_0 + \omega_{ref})t \right] \tag{7.26}$$

From (7.26) we observe that reference spurs at $f_0 + f_{ref}$ and $f_0 - f_{ref}$ are:

$$P_r = 20\log\left(\frac{K_{vco} A_m}{2\omega_{ref}} \right) dBc \tag{7.27}$$

In the charge-pump PLL, the PFD outputs, *up* and *dn,* produce a narrow pulse in each phase comparison period (T_{ref}). Noises in PLL generate the random part of the charge-pump output current (I_{out}), while mismatches in the charge-pump generate deterministic and periodic part of I_{out}.

Recall that in the linear and continuous-time PLL phase noise model in Fig. 3-6, the noise associated with each block of the PLL can produce non-

zero phase errors θ_e at PFD. Figure 7-12 illustrates the I_{out} pulse sequences generated by noises in PLL.

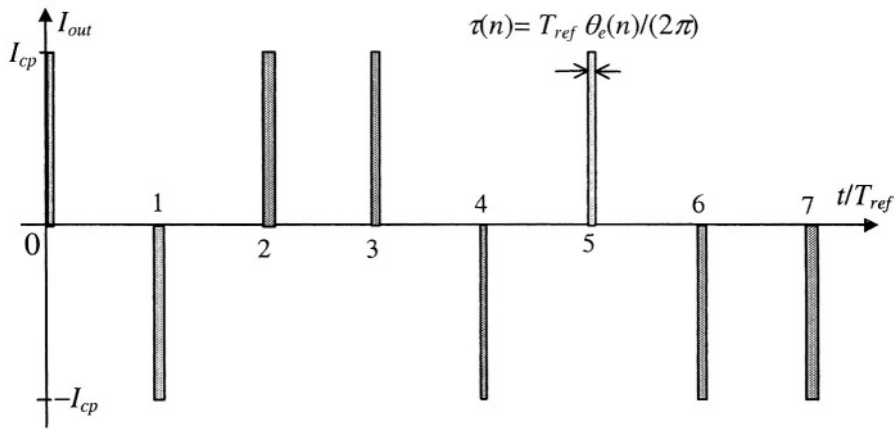


Figure 7-12. Charge-pump output current in locked state due to noise

Since the PFD and charge-pump actually operate in a discrete-time manner (see Fig. 3-10), the spectrum folding due to sampling effect occurs. According to (3.41), the spectrum of discrete-time phase error θ_{e_dt} is that of the continuous-time θ_e repeated in the frequency domain with period equal to the reference frequency ω_{ref}.

$$\theta_{e\_dt}(\omega) = \sum_{n=-\infty}^{\infty} \theta_e(\omega + n\omega_{ref}) \tag{7.28}$$

This spectrum folding effect produces phase noise around offset frequencies of $n\omega_{ref}$, where $n = \pm 1, \pm 2, \cdots$. The phase noise around offset frequencies $\pm\omega_{ref}$ is accounted for the reference spur here. The noise transfer functions from different noise sources in the PLL to the reference spur are listed in Table 7-2. In the table, we use the following approximation for $\omega << \omega_{ref}$:

$$H_{ol}\left[j(\omega + \omega_{ref})\right] \approx H_{ol}(j\omega_{ref}) \tag{7.29}$$

Table 7-2. Phase noise transfer functions for reference spur

noise source		transfer function to $\theta_{out}[j(\omega+\omega_{ref})]$	
input	$\theta_{in}(j\omega)$	$N\dfrac{H_{ol}(j\omega_{ref})}{1+H_{ol}(j\omega)}$	high-pass
PFD/CP	$i_{cp}(j\omega)$	$\dfrac{N}{K_{pd}}\dfrac{H_{ol}(j\omega_{ref})}{1+H_{ol}(j\omega)}$	high-pass
LF	$v_{lf}(j\omega)$	$\dfrac{K_{vco}}{j\omega_{ref}}\dfrac{H_{ol}(j\omega_{ref})}{1+H_{ol}(j\omega)}$	band-pass
VCO	$\theta_{vco}(j\omega)$	$-\dfrac{H_{ol}(j\omega_{ref})}{1+H_{ol}(j\omega)}$	high-pass
divider	$\theta_{div}(j\omega)$	$-N\dfrac{H_{ol}(j\omega_{ref})}{1+H_{ol}(j\omega)}$	high-pass

Denote the PLL output *rms* phase error in *rad* as $\Delta\phi_{rms}$. Comparing Table 7-2 and Table 3-1, the upper bound of the reference spur due to various noises is given by:

$$P_r < 20\log(\Delta\phi_{rms}) + 20\log\left(\left|H_{ol}(j\omega_{ref})\right|\right) \tag{7.30}$$

The reference spur reaches this upper bound when the noise contribution of the VCO and loop filter dominates $\Delta\phi_{rms}$. When $\Delta\phi_{rms} = \pi/180$, i.e., 1°, $20\log(\Delta\phi_{rms}) \approx -35dB$.

Combining (3.3), (3.32), (3.37) and the fact that $\omega_z << \omega_{ref}$, we have

$$\left|Z_{lf}(j\omega_{ref})\right| \approx R_1 \cdot \frac{C_1}{C_1+C_2+C_3}\frac{1}{\sqrt{1+(\omega_{ref}/\omega_{p2})^2}}\frac{1}{\sqrt{1+(\omega_{ref}/\omega_{p3})^2}} \tag{7.31}$$

and

$$\left|H_{ol}(j\omega_{ref})\right| \approx \frac{\omega_c}{\omega_{ref}}\frac{1}{\sqrt{1+(\omega_{ref}/\omega_{p2})^2}}\frac{1}{\sqrt{1+(\omega_{ref}/\omega_{p3})^2}} \tag{7.32}$$

Note that (7.31) and (7.32) can be further simplified if $\omega_{p2} << \omega_{ref}$ and/or $\omega_{p3} << \omega_{ref}$.

Mismatches in the charge-pump generate deterministic and periodic ripples of the VCO control voltage. Figure 7-13 illustrates the charge-pump output current (I_{out}) in one reference period (T_{ref}) due to nonidealities of the charge pump. The incomplete derivations of reference spur due to mismatches in [70] are reexamined here.

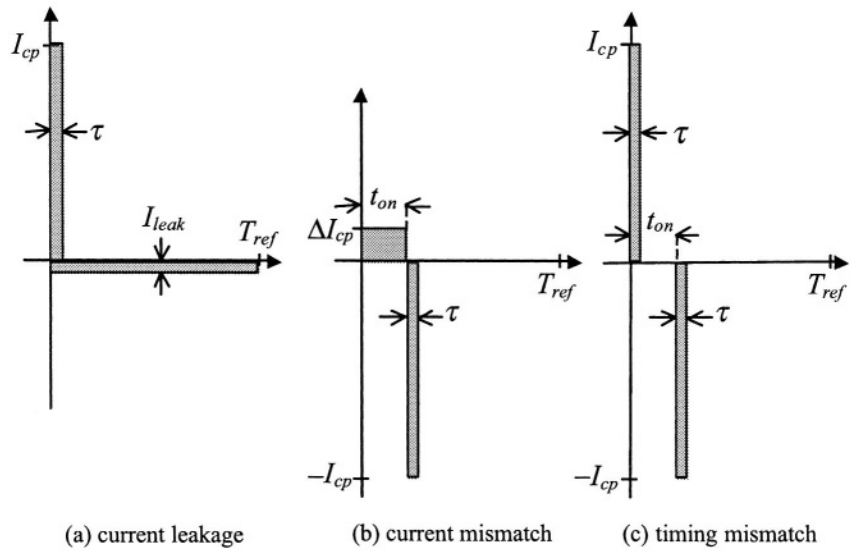


Figure 7-13. Charge-pump output current in locked state due to mismatch

Since the charge-pump output current I_{out} is a periodic signal with period of T_{ref}, it can be decomposed into discrete Fourier series as [71]:

$$I_{out}(t) = \sum_{k=1}^{\infty} c_k e^{jk\omega_{ref}t} \tag{7.33}$$

The VCO control voltage is

$$V_c(s) = I_{out}(s) \cdot Z_{lf}(s) \tag{7.34}$$

Thus, the reference spur level in *dBc* is

$$\begin{aligned} P_r &= 20\log\frac{K_{vco}|c_1|\cdot|Z_{lf}(j\omega_{ref})|}{2\omega_{ref}} \\ &= 20\log\left(N\pi\cdot\frac{|c_1|}{I_{cp}}\right)+20\log\left(|H_{ol}(j\omega_{ref})|\right) \end{aligned} \tag{7.35}$$

In Fig. 7-13 (a), the pulse width of current I_{cp} to compensate the leakage current I_{leak} is:

$$\tau = \frac{I_{leak}}{I_{cp}}T_{ref} \tag{7.36}$$

The coefficients of Fourier series in (7.33) are:

$$\begin{aligned} c_k &= \frac{1}{T_{ref}}\left[\int_0^{\tau} I_{cp}e^{-jk\omega_{ref}t}dt - \int_0^{T_{ref}} I_{leak}e^{-jk\omega_{ref}t}dt\right] \\ &= I_{leak}\frac{\sin(k\omega_{ref}\tau/2)}{k\omega_{ref}\tau/2}e^{-jk\omega_{ref}\tau/2} \end{aligned} \tag{7.37}$$

From (7.36), we have $\tau << T_{ref}$ when $I_{leak} << I_{cp}$. Thus the coefficient corresponding to the reference spur is:

$$|c_1| \approx I_{leak} \tag{7.38}$$

For example, if $I_{leak} = 10nA$, $I_{cp} = 100\mu A$ and N = 100, then in (7.35) the term $20\log(N\pi\cdot|c_1|/I_{cp})$ is about $-30dB$.

In Fig. 7-13 (b), the current mismatch between I_{up} and I_{dn} is:

$$\Delta I_{cp} = I_{up} - I_{dn} \tag{7.39}$$

The pulse width of current $-I_{cp}$ to compensate this current mismatch is

$$\tau = \frac{\Delta I_{cp}}{I_{cp}}t_{on} \tag{7.40}$$

Usually $\Delta I_{cp} << I_{cp}$ and $t_{on} << T_{ref}$, thus $\tau << t_{on}$. The Fourier coefficients of charge-pump output current in (7.33) are:

$$\begin{aligned} c_k &= \frac{1}{T_{ref}}\left[\int_0^{t_{on}} \Delta I_{cp} e^{-jk\omega_{ref}t}dt - \int_{t_{on}}^{t_{on}+\tau} I_{cp} e^{-jk\omega_{ref}t}dt\right] \\ &= \Delta I_{cp}\frac{t_{on}}{T_{ref}}\frac{\sin\left(k\omega_{ref}t_{on}/2\right)}{k\omega_{ref}t_{on}/2}e^{-jk\omega_{ref}t_{on}/2} \\ &\quad - I_{cp}\frac{\tau}{T_{ref}}\frac{\sin\left(k\omega_{ref}\tau/2\right)}{k\omega_{ref}\tau/2}e^{-jk\omega_{ref}(\tau/2+t_{on})} \end{aligned} \tag{7.41}$$

Thus the coefficient for the reference spur due to current mismatch is:

$$|c_1| \approx \pi\Delta I_{cp}\left(\frac{t_{on}}{T_{ref}}\right)^2 \tag{7.42}$$

As a numerical example, if $\Delta I_{cp}/I_{cp} = 10\%$, $T_{ref} = 100ns$, $t_{on} = 1ns$ and N = 100, then in (7.35) the term $20\log\left(N\pi\cdot|c_1|/I_{cp}\right)$ is about $-40dB$.

Figure 7-13 (c) shows the charge-pump output current due to the timing mismatch between the turn-off of *up* and *dn* switches. It might be due to the delay mismatch between falling-edges of *up* and *dn,* or the turn-off time mismatch between the two switches themselves. It generates both a positive and negative current pulse I_{cp} of the same width. Again, we denote the current pulse width as τ, and the Fourier coefficients are:

$$\begin{aligned} c_k &= \frac{1}{T_{ref}}\left[\int_0^{t_{on}} I_{cp} e^{-jk\omega_{ref}t}dt - \int_{t_{on}}^{t_{on}+\tau} I_{cp} e^{-jk\omega_{ref}t}dt\right] \\ &= j\cdot 2I_{cp}\frac{\tau}{T_{ref}}\frac{\sin\left(k\omega_{ref}\tau/2\right)}{k\omega_{ref}\tau/2}\sin\left(\frac{k\omega_{ref}t_{on}}{2}\right)e^{-jk\omega_{ref}(\tau+t_{on})/2} \end{aligned} \tag{7.43}$$

So the coefficient for the reference spur due to the timing mismatch is:

$$|c_1| \approx 2\pi I_{cp}\frac{\tau}{T_{ref}}\cdot\frac{t_{on}}{T_{ref}} \tag{7.44}$$

Thus, if $T_{ref} = 100ns$, $t_{on} = 1ns$, $\tau = 0.1ns$ and $N = 100$, then in (7.35) the term $20\log\left(N\pi \cdot |c_1| / I_{cp}\right)$ is approximately $-34dB$.

Besides the three kinds of mismatches discussed above, mismatches of clock feed-through and charge sharing of *up* and *dn* switches also contribute to the reference spur. Sometimes, dummy switches are used to reduce clock feedthrough and charge sharing.

Note that in a PLL with on-chip loop filter and VCO, the reference spur can be partially contributed by the periodic supply noise and substrate noise due to the periodic operation of the PFD, charge-pump and loop divider.

It is interesting to notice that in the standard charge-pump PLL, the reference spur is directly related to the pulse sampling of θ_e (see Fig. 7-12 and Fig. 7-13). If we sample θ_e using the zero-order sample-and-hold function as explained in (7.45), the reference spur will be significantly reduced. Compare with (7.28) of impulse sampling, the spectrum of sample-and-hold is given by

$$\theta_{e\_dt}(\omega) = \frac{\sin\left(\pi\omega / \omega_{ref}\right)}{\pi\omega / \omega_{ref}} \cdot \sum_{n=-\infty}^{\infty} \theta_e\left(\omega + n\omega_{ref}\right) \tag{7.45}$$

For the example of PLL with a sample-reset loop filter in [73] (see Fig. 6-5 and Fig. 6-6), the spectrum of the charge-pump output current is:

$$\begin{aligned} I_{out}(j\omega) = & \frac{1}{j\omega C_1} \frac{I_{cpi}}{2\pi} \cdot \sum_{n=-\infty}^{\infty} \theta_e\left(\omega - n\omega_{ref}\right) \\ & + R_{eq} \frac{I_{cpp}}{2\pi} \frac{\sin\left(\pi\omega / \omega_{ref}\right)}{\pi\omega / \omega_{ref}} \cdot \sum_{n=-\infty}^{\infty} \theta_e\left(\omega - n\omega_{ref}\right) \end{aligned} \tag{7.46}$$

7.3.2 Charge pump architectures

As summarized in [70], three generic topologies of charge-pumps are shown in Fig. 7-14. The switch is put at the drain, gate and source of the current source (or sink) transistor in Fig. 7-14 (a), (b) and (c), respectively. The one with switch at drain has the shortest switch time, but its peak current matching is a problem [70]. The one with switch at gate has the longest switch time and it is less used in practice.

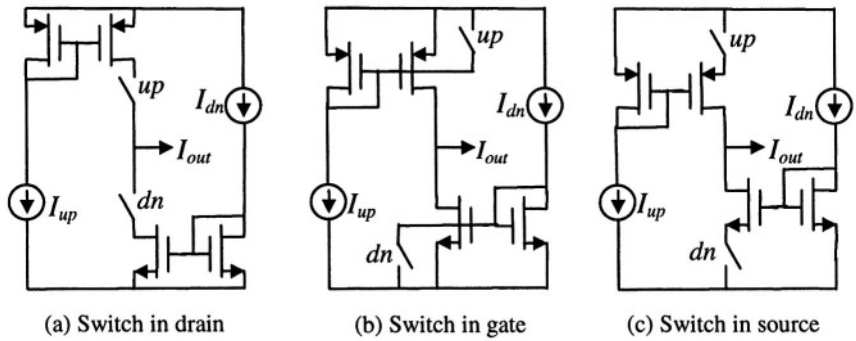


Figure 7-14. Simplified schematic of generic charge-pumps

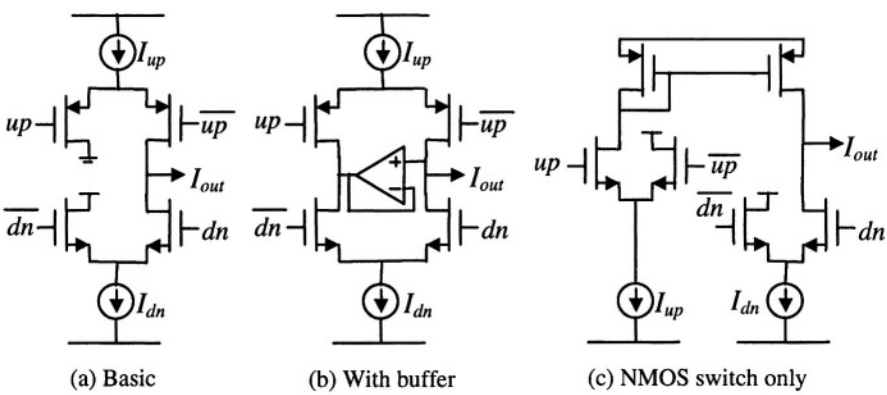


Figure 7-15. Current steering charge-pumps

Charge-pumps using the current steering technique [70] shown in Fig. 7-15 feature faster transient response and no supply current glitches. A buffer is used in Fig. 7-15 (b) to better match the charge and discharge currents, and to minimize charge sharing at the output [66], [70], [72]. The charge-pump in Fig. 7-15 (c) uses symmetric switches, but the two switch-to-output paths are asymmetric.

Many efforts have been made to improve current matching and/or reduce charge-injection and charge-sharing due to switching operation in the literature [70]-[85]. However, we also need to pay attention to the transient characteristic of charge pump because the PFD pulse width is very small (typically around 1*ns*) in the locked state. Fast and symmetrical transient response is critical for good matching in the charge pump. Fortunately, the reference frequency is very high in the fractional-N synthesis and the reference spur is much less concerned. The simplified schematic of the

charge pump in the prototype PLL is the same as the one illustrated in Fig. 7-15 (a). It has the properties of fast transient response and good timing delay matching from switching controls, $\overline{UP}$ and DN, to output current I_{out}.

In TSMC $0.35\mu m$ CMOS, a typical delay of an inverter with 2-V supply and the same inverter load is $0.3ns$. To increase the linearity of the charge-pump, the exclusive-or (XOR) gates are employed to generate switching controls UP and DN and their inverse signals $\overline{UP}$ and $\overline{DN}$ for better alignment. Simulation shows that the timing misalignment is less than $50ps$ with the circuitry shown in Fig. 7-16. Note that, an alternative approach, which is often used, is shown in Fig. 7-17. Even and odd numbers of inverters are used for the in-phase and inverse UP (or DN) control, respectively. The inverter size and/or load in both paths are scaled to obtain equal delay.

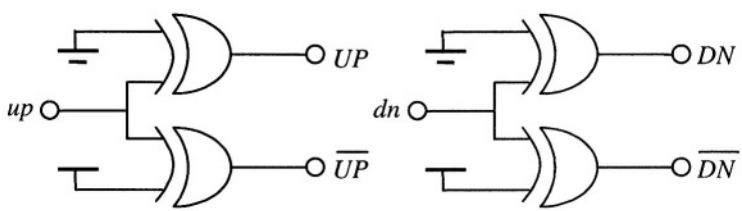


Figure 7-16. Aligning UP (or DN) and its reverse

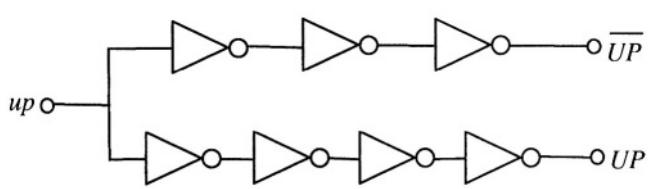


Figure 7-17. Aligning with scaled inverters

7.4 Programmable divider

A pulse-swallowing programmable divider as shown in Fig. 7-18 was used. It is a combination of a dual-modulus prescaler and two programmable counters. In each output cycle, the prescaler divide ratio is $P + 1$ for A times, and P for the remaining $M - A$ times. Therefore, the total frequency divide ratio is:

$$N = A \cdot (P+1) + (M-A) \cdot P = M \cdot P + A \tag{7.47}$$

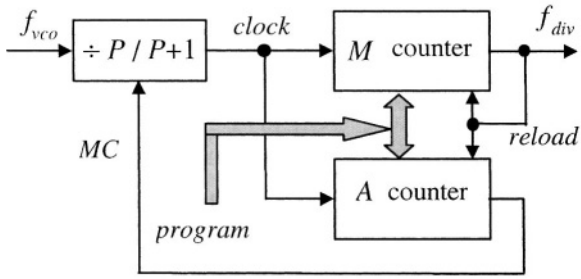


Figure 7-18. Pulse-swallow programmable frequency divider

In this work, the prescaler modulus (P/P+1) is 15/16, and the programmable M and A counters are 6-bit and 4-bit, respectively.

The lower boundary of continuous divide ratios of a pulse-swallowing divider with a dual-modulus prescaler is $P\cdot(P-1)$. For $P = 15$, this boundary is 210. Since continuous divide ratios in a large range (e.g. from 100 to 200) are often required, we can either reduce the modulus P of the dual-modulus prescaler or use a multi-modulus prescaler. For example, the lower continuous divide ratio boundary of a four-modulus prescaler ($P/P + 1/P + 2/P + 3$) is $P\cdot(P-1)/3$. This boundary equals 80 when $P = 16$. Generally, the lower boundary of an m-modulus prescaler ($P/P + 1/\cdots/P + m-1$) is $P \cdot M_{\min}$, where $M_{\min}$ is the maximum integer number that satisfies:

$$(P+m-1)\cdot M_{\min}+1 \le P\cdot(M_{\min}+1) \tag{7.48}$$

$$M_{\min} \le \frac{P-1}{m-1} \tag{7.49}$$

The loop divider, which is usually a combination of a high-speed dual-modulus prescaler and a programmable low-speed divider, is modeled as $1/N$ in the linear and continuous phase noise analysis. But in reality, the frequency divider is a discrete digital block and it down samples the VCO output phase noise. For an integer divide ratio of N , the relationship between the divider's input and output phase noise is:

$$\theta_{div}(m) = \theta_{vco}(m\cdot N)/N \tag{7.50}$$

In frequency domain, we have

$$\theta_{div}\left(e^{j\Omega}\right)=\frac{1}{N^2}\sum_{k=0}^{N-1}\theta_{vco}\left(e^{j(\Omega-2\pi k)/N}\right) \tag{7.51}$$

where the Ω is the normalized angle frequency of the divider output:

$$\Omega = 2\pi f / f_{div} \tag{7.52}$$

From (7.51), we know that the VCO phase noise power out of the frequency range of $-f_{div}/2 \sim f_{div}/2$, is folded within this frequency range due to the alias effect of the down sampling.

If we take the VCO phase noise as continuous and the divider output phase noise as a sampling of the VCO phase noise, we have

$$\theta_{div}(m)=\theta_{vco}(m\cdot T_{div})/N \tag{7.53}$$

The sampling function is:

$$H_{div}(f)=\frac{1}{N}e^{-j\pi f/f_{div}}\frac{\sin(\pi f/f_{div})}{\pi f/f_{div}}=\frac{1}{N}e^{-j\pi f/f_{div}}\sin c\left(\frac{\Omega}{2}\right) \tag{7.54}$$

The magnitude of this sampling function (without scaling factor of 1/*N*) for a 900*MHz* GSM frequency synthesizer is illustrated in Fig. 7-19. Note that, the reference frequency is 200*kHz* and the divide ratio *N* is 4500. The transfer function has zeros at multiples of the sampling frequency, that is, the divider output frequency.

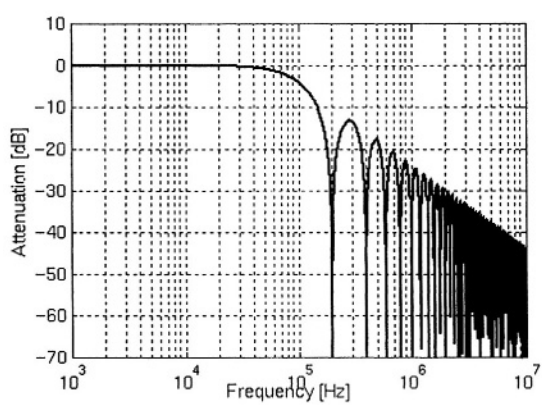


Figure 7-19. Frequency divider sampling function

For a carrier signal with spurious tones (see (2.4)) passing the frequency divider, the divider output (assumed as sine wave) is:

$$\begin{aligned} V_{div}(t) &= V_0 \sin\left(\frac{2\pi f_0 t + \Delta\phi \sin(2\pi f_m t)}{N}\right) \\ &= V_0 \sin\left(2\pi \frac{f_0}{N} t + \frac{\Delta\phi}{N} \sin(2\pi f_m t)\right) \end{aligned} \tag{7.55}$$

Thus, the spur frequency relative to the carrier is not changed, but the spur level is attenuated by 20log(*N*) *dB* at the divider output.

7.5 Digital ΣΔ modulator

The third-order three-level multi-feedforward digital ΣΔ modulator [86] as studied in Chapter 4 is employed in the experimental PLL prototype. It generates smaller instantaneous phase error at PFD input. Thus the phase noise associated with PFD and charge-pump is reduced. The noise folding (or mixing) due to nonlinearities of PFD, charge-pump and VCO in the PLL is also reduced.

7.6 Chip layout

The layout of the whole chip, which includes a fully integrated ΣΔ fractional-N frequency synthesizer and some standalone building blocks, such as prescaler, loop filter and VCO, is shown in Fig. 7-20. The whole chip measures 2*mm*×2*mm*. Each building block is encircled by double guard-rings to minimize substrate noise interference. The big ESD protection transistors are removed for RF pads, such as the VCO output and prescaler input pads. Empty areas are filled with poly, metal3 and/or metal4 layers to meet the requirement on the minimum density of these layers.

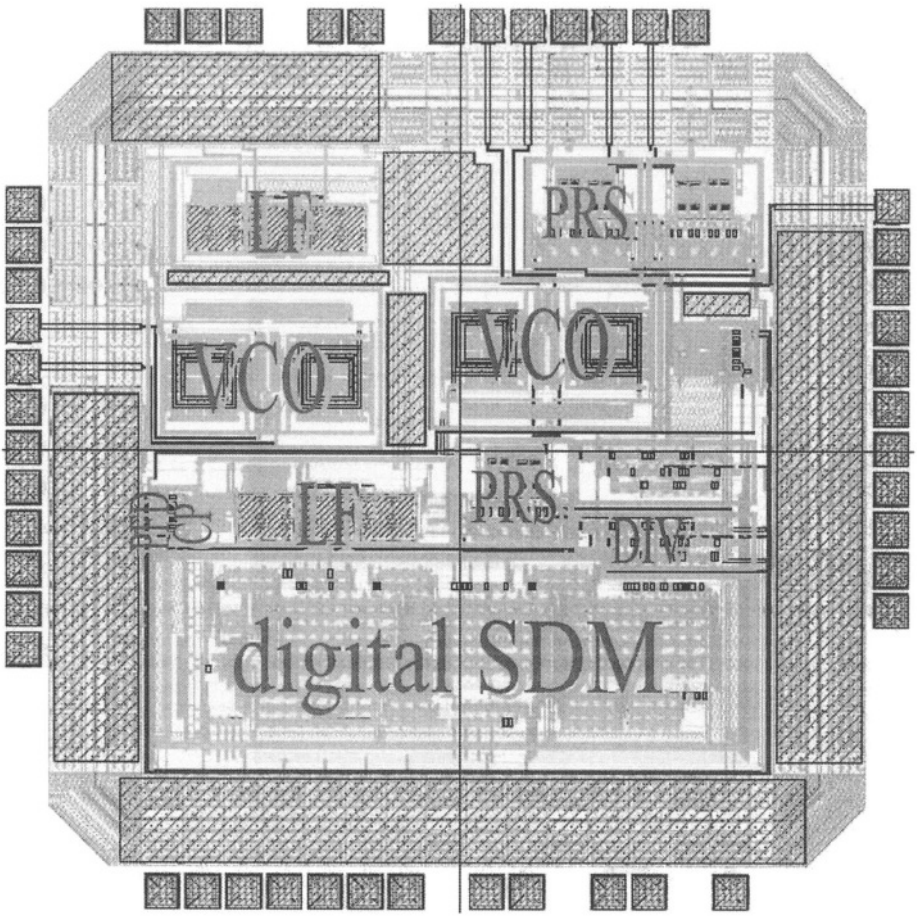


Figure 7-20. Layout of the whole chip

Table 7-3 summarizes the area distribution of the monolithic frequency synthesizer. It shows that the digital ΣΔ modulator takes more than half of the synthesizer's total area.

Table 7-3. Synthesizer active area distribution

block	area	percentage
digital SDM	$0.5mm^2$	58.8%
LC-VCO	$0.15mm^2$	17.7%
loop filter	$0.05mm^2$	5.9%
prescaler	$0.4mm^2$	4.7%
others	$0.11mm^2$	12.9%
total	$0.85mm^2$	100%

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Chapter 8

PROTOTYPE MEASUREMENT RESULTS

The ΣΔ fractional-N synthesizer prototype design was sent to MOSIS later in October 2001 for fabrication. It was fabricated in $0.35\mu m$ double-poly four-metal (2P4M) CMOS process by TSMC early in January 2002. The corresponding MOSIS run ID is T1AA. The chip was packaged in TQFP-48pin and received late in January 2002. The standalone blocks, prescaler and loop filter, and the whole PLL were characterized to prove both the enhanced phase-switching prescaler and the loop filter with capacitance multiplier on silicon.

8.1 Prescaler measurement

The microphotograph of the standalone prescaler is shown in Fig. 8-1. It takes $210\mu m \times 180\mu m$. Four SCL master-slave flip-flops can be figured out on the photo. Because the prescaler input has dual pseudo-differential NMOS pairs, differential input signals have to be applied in the measurement set-up shown in Fig. 8-2.

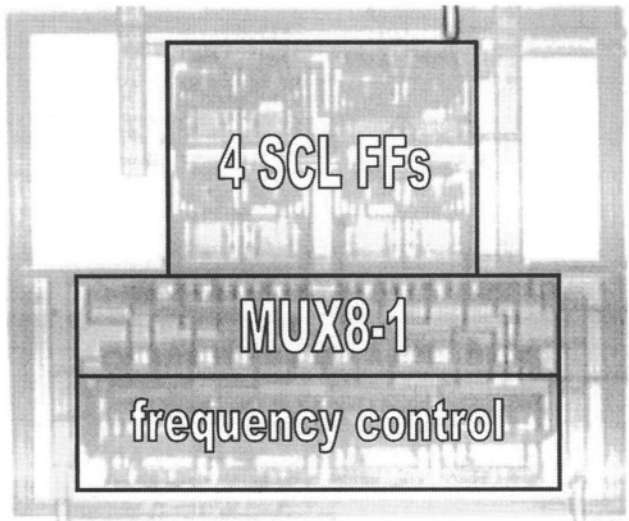


Figure 8-1. Microphotograph of prescaler

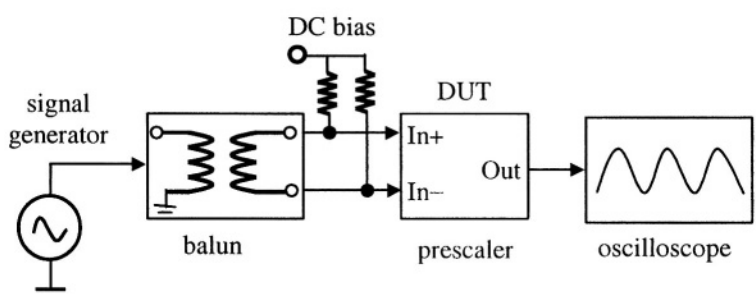


Figure 8-2. Prescaler measurement set-up

The packaged standalone prescaler works up to 2.1*GHz* with a 1.5*V* supply and consumes 2*mA* excluding the output buffer. However, it is also verified that the prescaler within the PLL works well within the 2.23~2.45GHz tuning range with 1.5*V* supply.

When the supply voltage increases, the maximum operating frequency and power consumption of the prescaler also increases. At 3.0*V* supply, the prescaler works up to 4.1*GHz* as shown in Fig. 8-3.

At 1.5*V* supply, the prescaler input sensitivity (without input buffer) is shown in Fig. 8-4. The self-resonant frequency of the prescaler in absence of ac input is 1.316*GHz*. The upper limit of input power is limited to 10*dBm,* which is the maximum output power level from the signal generator.

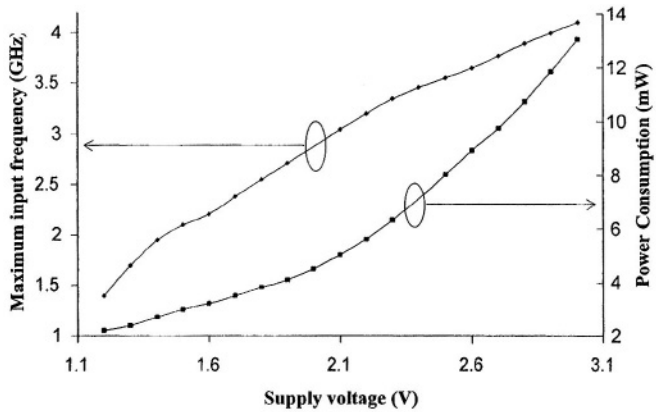


Figure 8-3. Maximum speed and power consumption vs. supply voltage

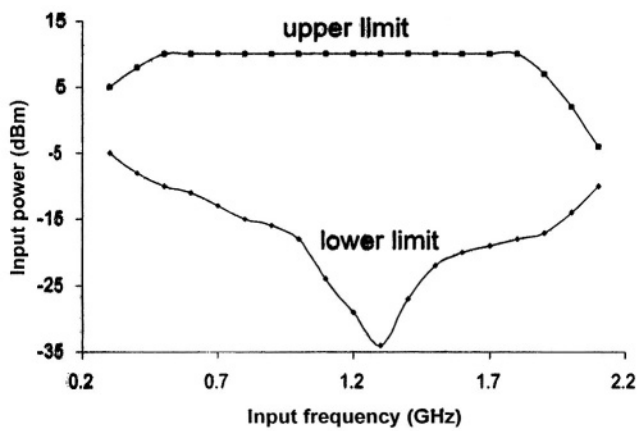


Figure 8-4. Input sensitivity over frequency (VDD=1.5V)

Finally, the residual phase noise of the prescaler is shown in Fig. 8-5. The phase noise level at $1kHz$ is $-124dBc/Hz$.

A comparison between this prescaler and those recently reported in the literature is summarized in Table 8-1. It shows that this low-supply-voltage ($1.5V$), low-power ($3mW$), small-area ($0.04mm^2$) and robust phase-switching prescaler has the smallest figure-of-merit (FOM), which is defined as power-speed ratio, than other CMOS prescalers. Its power-speed ratio is comparable to the low-power bipolar prescaler reported in [4], but its supply voltage is lower and its area is less than one-sixth of the bipolar one.

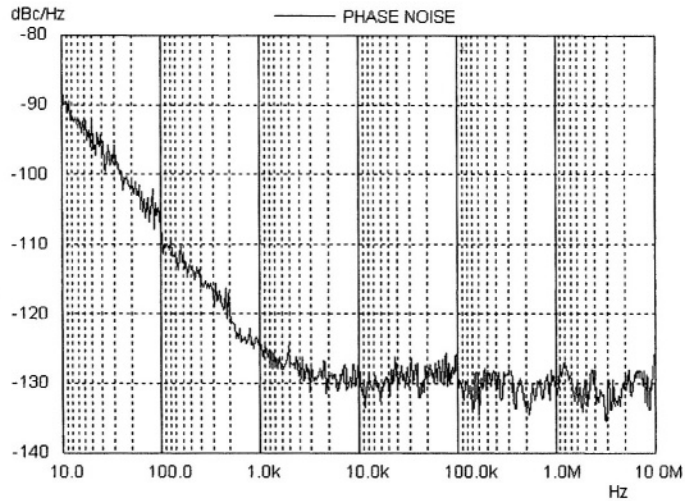


Figure 8-5. Measured residual phase noise

Table 8-1. Prescaler performance comparison

ref#	pro-cess	divider ratio	supply [*V*]	power [*mW*]	area [mm^2]	speed [*GHz*]	FOM *mW/GHz*
[1]	0.7μ	128/129	3.0	24	0.63*	1.75	13.7
[2]	0.5μ	16/17	2.7	1.9	NA	1.5	1.27
[3]	0.25μ	220~224	2.2	59	0.09	5.35	11.0
[4]	52G	128/129	2.0/2.7	2.0/2.7	0.25	2/2.45	1.0/1.1
	BJT	256/257	2.7/5.0	30/56	0.25	12/13.5	2.5/4.15
[5]	0.35μ	2^8~2^{18}−1	2.2	NA	NA	0.94	1.3
		2^9~2^{19}−1	2.2	NA	NA	1.8	1.75
[6]	0.8μ	128/129	5.0	12.8	0.013	1.59	8.05
[7]	0.24μ	22/23	1.5	19	≈0.3	≥2.5	≤7.6
[8]	0.25μ	128~256	2.5	15	NA	2.41	6.22
ours	0.35μ	15/16	1.5	3	0.04	≥	≤1.22

* including pads

8.2 Loop filter measurement

The microphotograph of the loop filter is shown in Fig. 8-6. It takes an active area of less than $0.05mm^2$. A standalone loop filter is included on the chip for testing.

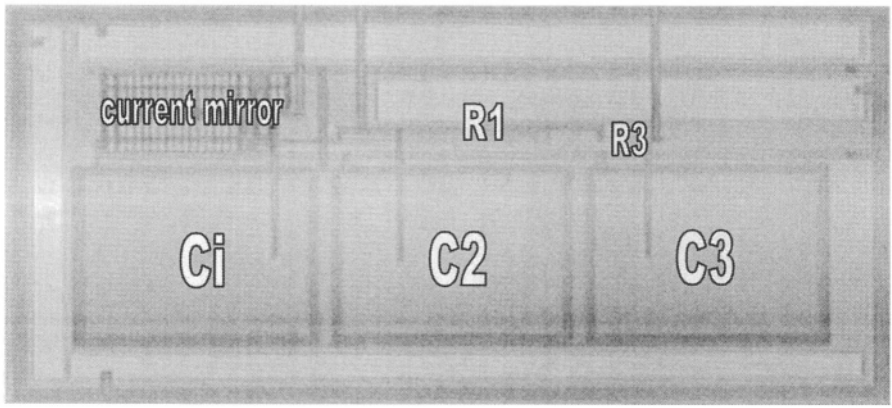


Figure 8-6. Microphotograph of loop filter

Due to the unavailability of the impedance analyzer, the loop filter's transimpedance was measured indirectly by the HP89410A DC-10MHz vector signal analyzer. The measurement setup is shown in Fig. 8-7. The transfer function of loop filter with $100k\Omega$ resistor in series at the input and a buffer at the output was measured.

The measured amplitude and phase are shown in Fig. 8-8, which agree well with simulated values with inaccuracies of no-chip resistance and capacitance, and parasitic capacitance taking into account. The impedance of the loop filter was extracted from the measurement results of Fig. 8-8. The magnitude and phase of the loop filter impedance are shown in Fig. 8-9 together with simulation results for comparison. It shows that the discrepancies between the measured and simulated results mainly come from the parasitic capacitance at the loop filter output.

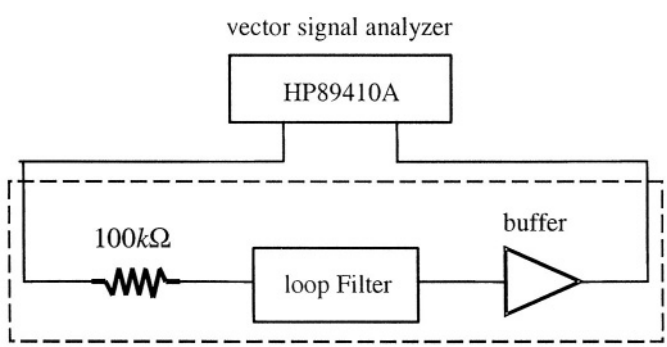
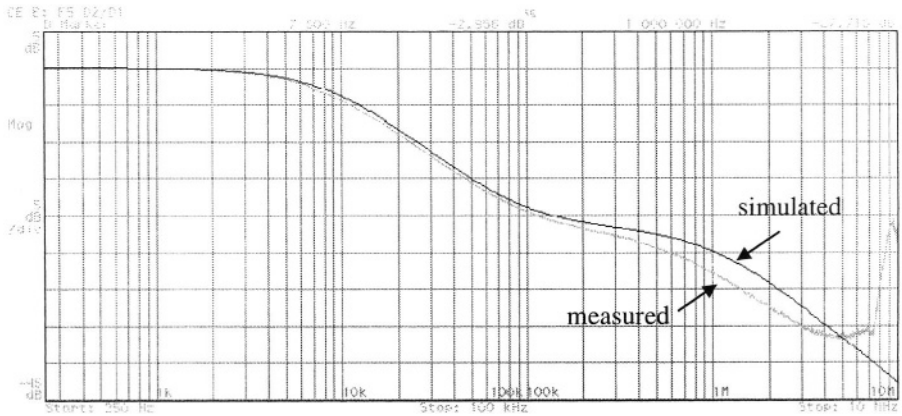
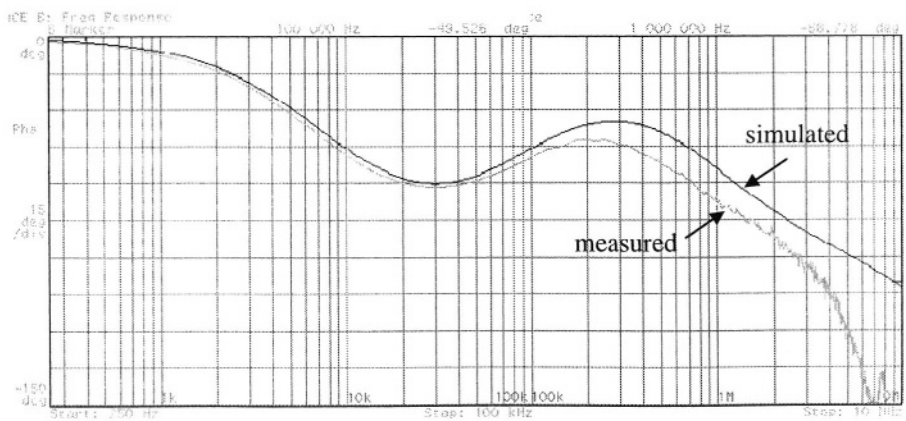


Figure 8-7. Loop filter measurement setup



(a) Amplitude



(b) Phase

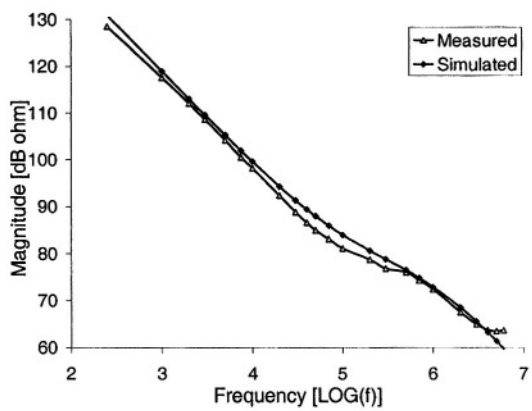
Figure 8-8. Measured LF transimpedance in series with a $100k\Omega$ resistor

8.3 PLL measurement

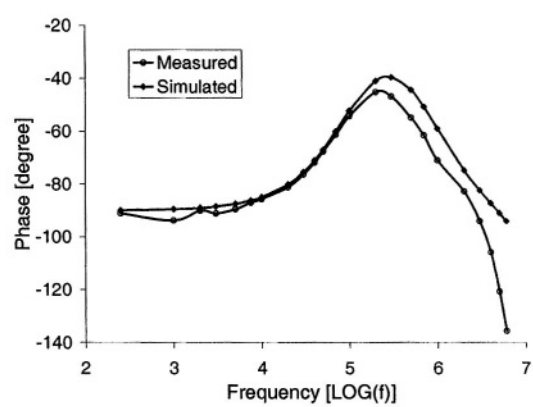
Figure 8-10 shows the microphotograph of the whole chip, which includes the monolithic PLL and some standalone blocks for testing. Each building block is encircled by double guard rings to minimize the substrate noise. The monolithic PLL has an area of $0.85mm^2$ out of which the digital $\Sigma\Delta$ modulator, the VCO, the loop filter and the prescaler occupy $0.5mm^2$, $0.15\ mm^2$, $0.05\ mm^2$ and $0.04\ mm^2$, respectively. The VCO and the prescaler draw $6mA$ and $2mA$ from a 1.5-V supply, respectively and other blocks draw $2mA$ from a 2-V supply in total, whereby the whole PLL system consumes $16mW$. The VCO draws lots of current because the inductor's Q is only

about 2 and it needs a sufficient output voltage swing to drive the prescaler's pseudo-differential NMOS input pairs directly. Compared with the 18*mW* dual-path loop filter in [9], the proposed capacitance multiplier only consumes 0.2*mW*.

The power spectrum and phase noise of the PLL output were measured by Rohde & Schwarz FSEB30 spectrum analyzer, and they are shown in Fig. 8-12 and Fig. 8-13, respectively. Reference spurs of –52*dBc* and –57*dBc* are observed with reference frequencies of 20*MHz* and 50*MHz*, respectively, in Fig. 8-12. The PLL output tuning range is 9.4%, from 2.23*GHz* to 2.45*GHz*. The PLL loop bandwidth is 270*kHz*. The phase noise levels at 10*MHz* offset are –125*dBc* and –128*dBc/Hz* with the reference frequency of 20*MHz* and 50*MHz*, respectively, which is mainly limited by the low quality inductor. The spurs caused by the non-ideal 45°-spacing in the phase-switching prescaler are negligible.



(a) Amplitude



(b) Phase

Figure 8-9. Simulated and measured LF transimpedance

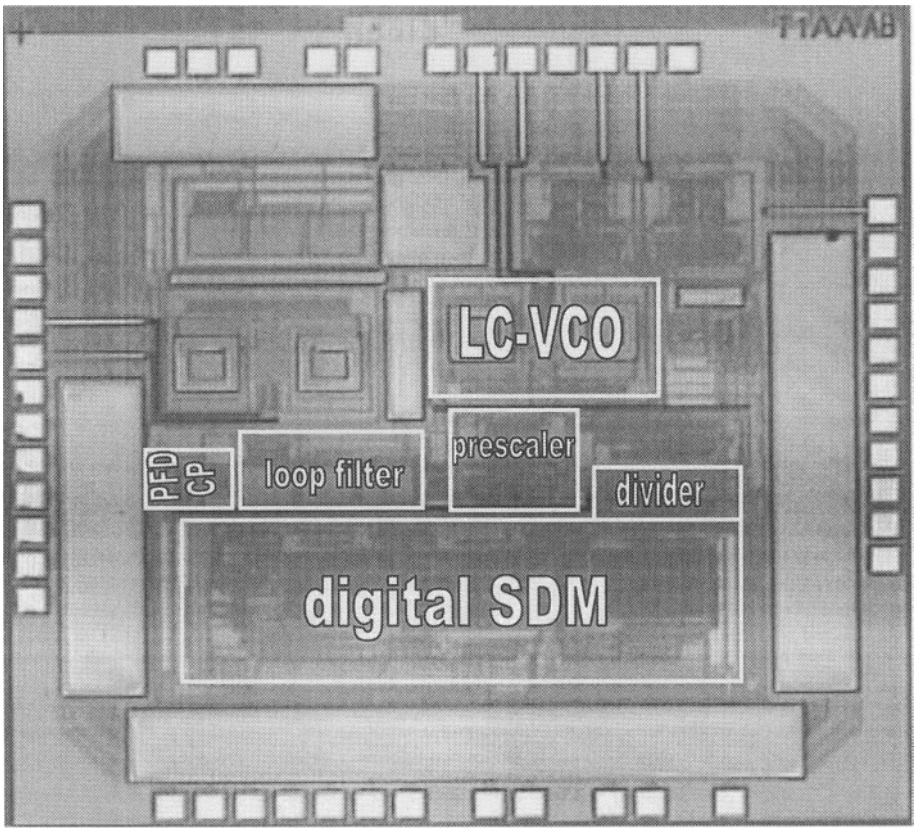


Figure 8-10. Microphotograph of the whole chip

The PLL measurement set-up is shown in Fig. 8-11.

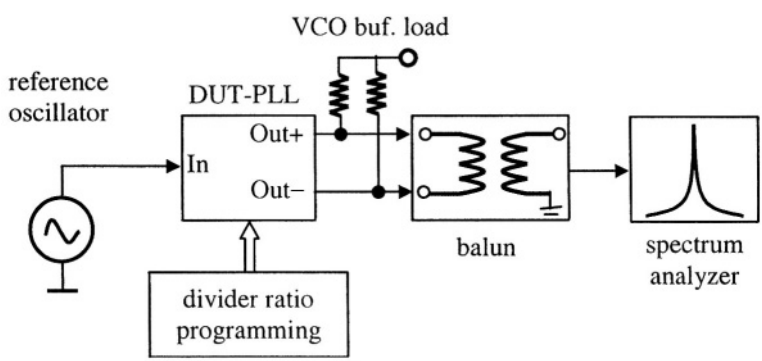
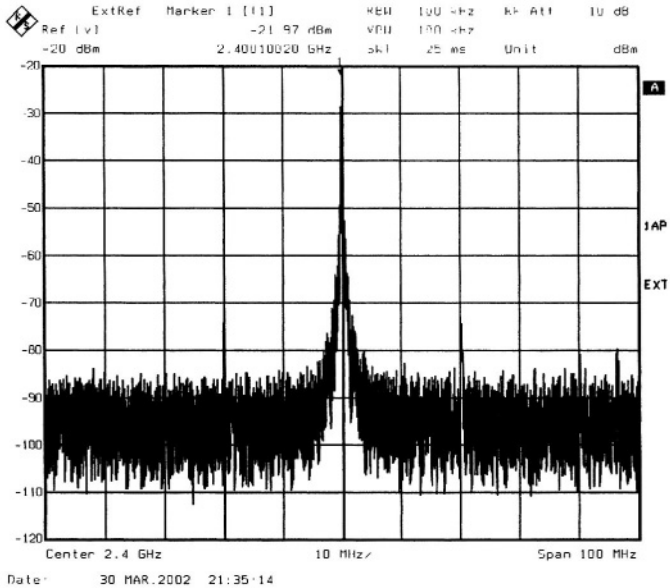
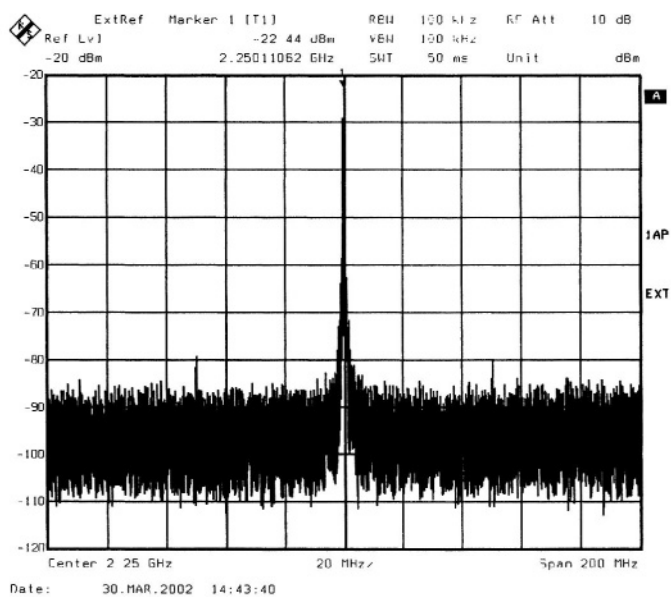


Figure 8-11. PLL measurement set-up

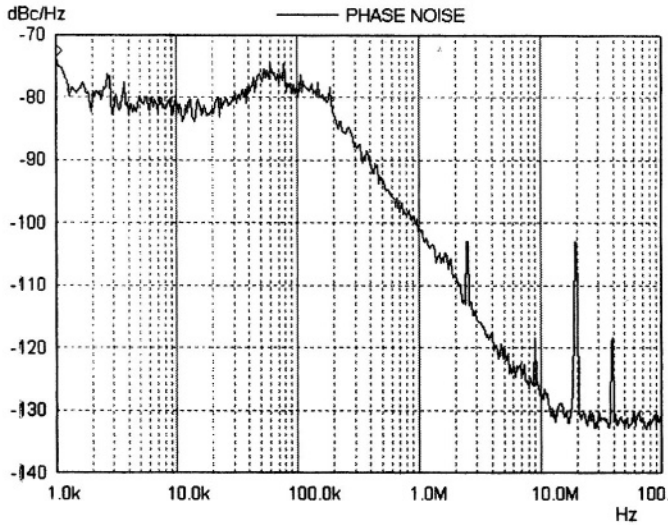


(a) $f_{ref} = 20MHz$

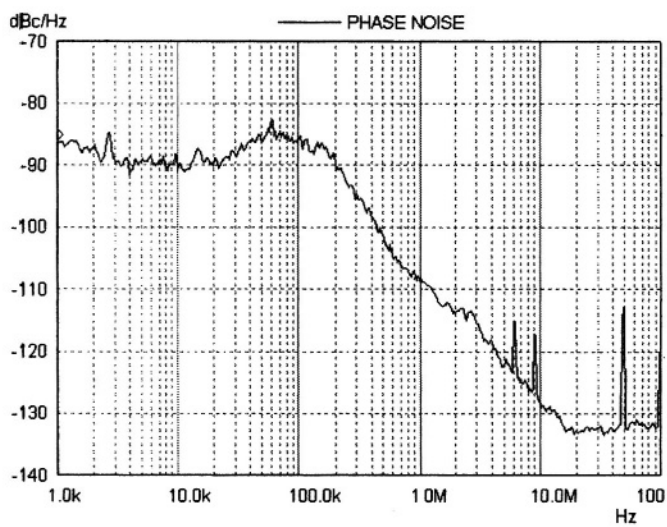


(b) $f_{ref} = 50MHz$

Figure 8-12. Measured PLL spectrum with different reference frequencies



(a) $f_{ref} = 20MHz$



(b) $f_{ref} = 50MHz$

Figure 8-13. Measured PLL phase noise with different reference frequencies

The characteristics of the PLL-based fractional-N frequency synthesizer are summarized in Table 8-2.

Table 8-2. Characteristics of frequency synthesizer

tuning range	2.23~2.45GHz (9.4%)
reference frequency	50MHz
loop bandwidth	270kHz
frequency resolution	<100Hz
reference spur	−57dBc
phase noise	−90dBc/Hz @10kHz −128dBc/Hz @10MHz
supply voltage	1.5V–VCO & prescaler 2.0V–other blocks
power consumption	9mW–VCO, 3mW–prescaler 4mW–others, 16mW–total
process	TSMC 0.35μm CMOS (2P4M)
active area	0.5mm^2–SDM, 0.15 mm^2–VCO, 0.05 mm^2–LF 0.04mm^2–prescaler, 0.85mm^2–total

A comparison of some frequency synthesizers recently reported in the literature and this work is summarized in Table 8-3. It is worthwhile to mention that the frequency synthesizer designed in 0.25μm CMOS in [8] failed to work beyond 2.41GHz due to the prescaler. Based on the low-power and robust phase-switching prescaler and loop capacitance multiplier, the proposed topology saves considerable power and area while improving the circuit robustness.

Table 8-3. PLL performance comparison

ref#	[10]	[7]	[11]	[12]	[8]	ours
output [GHz]	5.17~5.29 2.3%	4.84~5 3.2%	2.4~2.5 4%	2.4~2.53 5.2%	2.24~2.5 11%	2.23~2.45 9.4%
topology	Int.-N	Int.-N	ΣΔFN	Int.-N	ΣΔFN	ΣΔFN
process	0.4μm	0.24μm	0.5μm	0.25μm	0.25μm	0.35μm
f_{ref} [MHz]	11.75	11	48	1	13	50
ω_c[kHz]	800 (est.)	280	700	NA	NA	270
off-chip part	none	none	VCO LF	none	SDM LF	none
ref. spur	−53	≤−45	NA	−58.7	−64.7	−57
phase noise [dBc/Hz]	−115@ 10MHz	−101@ 1MHz	−123@ 10MHz	−112@ 1MHz	−133@ 3MHz	−128@ 10MHz
power	47	25	135.3	20	55	16
area	2.0	1.6*	3.5	0.29	2.0*	0.85

* including pads

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Chapter 9

CONCLUSIONS

The PLL frequency synthesizer is a critical building block of communication circuits. It is often used for frequency translation and channel selection. This book covers both fundamental and advanced knowledge of PLL synthesizers, from basic concepts of timing jitter and phase noise to the state-of-the-art analysis and design techniques. The contributions in this book are briefly listed in the following.

A. Analysis of the third-order PLL settling time

The frequency and time domain analysis of the PLL available in the literature is only based on the second-order approximation, which gives formulas for parameters like the damping factor and locking time. But in practice the charge-pump PLL are almost all of third- or fourth-order. The closed-form frequency and time domain analysis of the third-order PLL is presented in Chapter 3. It produces more accurate formulas for practical high-order PLL's. These new formulas provide not only profound insights on real PLL's, but also more enlightening design guidelines.

B. Comparative study of digital ΣΔ modulators for fractional-N PLL

Fractional-N PLL synthesizers with a digital ΣΔ modulator to control the instantaneous frequency divide ratio has been popular for more than a decade. This revolutionary fractional-N synthesizer architecture compensates fractional spurs elegantly in the digital domain and enables arbitrarily fine frequency resolution. However, the design considerations of the ΣΔ

modulator are not well discussed before. A comparative study of digital ΣΔ modulators for fractional-N PLL synthesizers is conducted in Chapter 4. Four modulator topologies are compared in terms of noise shaping, spurs, histogram of ΣΔ introduced phase errors, and noise folding due to PLL nonlinearities. It provides deep insights and informative design guidelines of digital ΣΔ modulators in fractional-N PLL's.

C. Low-power and robust phase-switching prescaler

The prescaler is often the speed bottleneck of high-frequency PLL synthesizers. The phase-switching prescaler exploits the toggling speed of a flip-flop or even an analog frequency divider, like the injection-locked architecture. The existing phase-switching prescaler topologies are based on four 90°-spaced phases and a multiplexer. They either suffer from potential glitches or use power-hungry glitch-removing techniques. Moreover, the high-speed 4-to-1 multiplexer imposes additional design challenges. A high-speed, low-power, and robust phase-switching prescaler is covered in Chapter 5. It is based on eight lower-frequency 45°-spaced phases and a reversed switching sequence. The phase pattern is detected to automatically adjust the switching sequence without introducing extra phase mismatches. The 8-to-1 multiplexer is carefully designed to avoid potential glitches and delay mismatches. Furthermore, the timing analysis of the delay budget in the phase-switching control loop provides helpful insights into the analysis and design of this phase switching prescaler.

D. Spurs due to delay mismatch in phase-switching prescaler

A group of multi-phase signals can be generated from either a multi-stage VCO, a multi-stage delay-line, a phase interpolator, or a frequency divider. They are used to produce a new signal by means of multiplexing. However, the delay/phase mismatches of the multi-phase signals will introduce spurs in the synthesized signal. A mathematical model of the spurs due to delay/phase mismatches in the phase-switching prescaler is derived in Chapter 5. Although it is based on a simplified statistical mismatch model, it does provide quantitative insights of the spur level. This spur analysis approach can be extended to model other multi-phase and multiplexing systems.

E. Loop filter with capacitance multiplier

The PLL loop filter often consists of a big capacitor, which either dominates the PLL area or has to be off-chip. The dual-path loop filter,

which equivalently scales down the capacitance by the current ratio of dual charge-pumps, is a popular solution to reducing the area of an on-chip loop filter. However, as mentioned in Chapter 1, this architecture has several disadvantages, such as big power and high complexity. A simple area-efficient loop filter solution based on a capacitance multiplier is elaborated in Chapter 6. It introduces negligible noise and consumes little power.

F. Complete derivation of PLL reference spur

Compared to phase noise, the reference spur of the charge-pump PLL is even more difficult to quantitatively analyze. Given the lack of a thorough study on this topic in the literature, a complete quantitative analysis of the reference spur is given in Chapter 7. Several mechanisms behind the reference spur are investigated, and their contributions are analyzed independently. The resulting formulas give designers a better estimation of the reference spur level during practical PLL circuit design.

G. Behavioral-level verification of PLL stability limit

The charge-pump PLL is an essentially discrete-time nonlinear system. However, the closed-loop phase margin, which is used as a stability criterion, is based on the continuous-time linear analysis. Gardner derived its stability limit using the z-domain analysis based on differential equations in 1980. A behavioral-level simulation of the third-order charge-pump PLL is made in the Appendix to verify its theoretical stability limit. The plot of the maximum bandwidth to reference frequency ratio versus the optimal phase margin shows that the simulation result agrees well with Gardner's formula. This verification further clarifies the confusion about the stability limit in the literature.

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APPENDIX

Behavioral Modeling of Charge-pump PLL

A. Behavioral model of charge-pump PLL

In a PLL, the loop bandwidth is at least ten times smaller than the reference frequency, while the VCO oscillating frequency can be as large as thousands of times of the reference frequency. Due to these vastly different time constants, the transistor-level transient simulation of PLL takes anywhere from a few hours to several days. Behavioral modeling is widely used to speed-up the simulation of the PLL. Figure A-1 shows the behavioral model of charge-pump PLL using Simulink. Basic parameters in this model include reference frequency f_{ref}, charge-pump current I_{cp}, loop filter values R_1, C_1 and C_2, VCO free-running frequency f_0 and conversion gain K_{vco}, and divide ratio N.

B. Stability limit of charge-pump PLL

As mentioned in Chapter 3, the stability limit of the third-order charge-pump PLL was derived by Gardner in [1] (see 3.37). It is based on linearized approximate difference equations. With $K = \omega_c b/(b-1)$ (see 3.23) and $\omega_z = \omega_c/\sqrt{b}$ (see 3.21), (3.73) becomes [2]

$$\frac{\omega_c}{\omega_{ref}} < \frac{4(1+a)}{\frac{4\pi^2(1+a)}{\sqrt{b}}\frac{\omega_c}{\omega_{ref}} + \frac{4\pi(1-a)(b-1)}{b}} \qquad \text{(A.1)}$$

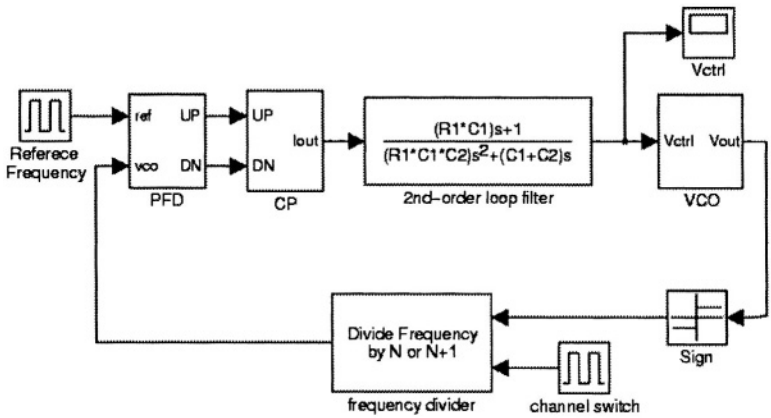


Figure A-1. Behavioral model of CP-PLL in Matlab (Simulink)

where $a = \exp\left(-2\sqrt{b}\pi \frac{\omega_c}{\omega_{ref}}\right)$.

Since the optimal phase margin ϕ_m is exclusively determined by b (see 3.22), we can plot the maximum ω_c / ω_{ref} ratio, that is, the stability limit, against ϕ_m [2]. The Matlab behavioral model of the third-order charge-pump PLL is used to verify this theoretical stability limit. The fixed part of loop parameters includes: $I_{cp} = 100\mu A$, $f_c = 100kHz$, $f_0 = 10MHz$, and $K_{vco} / N = 400kHz / V$. We sweep the phase margin ϕ_m by varying the value of b and calculate the corresponding loop filter values as listed in Table A-1. Then we check the loop stability limit by changing the value of f_{ref} and doing behavioral simulation. The theoretical stability limit is obtained by plotting both the left- and right-hand side of inequality (A.1) using Matlab to find the cross point value of ω_c / ω_{ref} .

As shown in Fig. A-2, the theoretical prediction of the maximum ω_c / ω_{ref} ratio agrees well with the behavioral simulation results. It proves that the discrete-time linear analysis in [1] is very accurate for the charge-pump PLL in its steady-state. Notice that the stability limit is non-monotonic with respect to the phase margin obtained from the continuous-time linear analysis. The commonly used rule-of-thumb, $\omega_c < \omega_{ref} / 10$, provides a safety margin factor of more than 2.7 to tolerate variations of PLL parameters and any additional loop delay. Note that, when a PLL has a very

wide frequency range, the charge-pump current and/or the loop filter values need to be adjusted adaptively to ensure loop stability [3]-[6].

Table A-1. Loop filter values for different phase margins

b	ϕ_m	R_1 $k\Omega$	C_1 pF	C_2 pF	b	ϕ_m	R_1 $k\Omega$	C_1 pF	C_2 pF
2	19.5°	31.4	71.7	71.7	12	57.8°	17.1	279	25.3
2.5	25.4°	26.2	96.1	64.1	16	61.9°	16.8	380	25.3
3	30.0°	23.6	117	58.5	25	67.4°	16.4	486	20.3
4	36.9°	20.9	152	50.7	36	71.1°	16.2	591	16.9
5	41.8°	19.6	181	45.3	49	73.7°	16.0	695	14.5
6	45.6°	18.8	207	41.4	81	77.3°	15.9	901	11.3
7	48.6°	18.3	230	38.3	100	78.6°	15.9	1003	10.1
8	51.1°	17.9	251	35.8	225	82.4°	15.8	1513	6.76
9	53.1°	17.7	270	33.8					

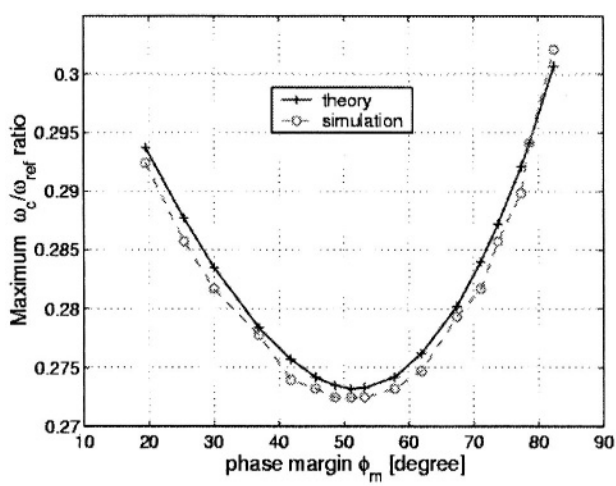
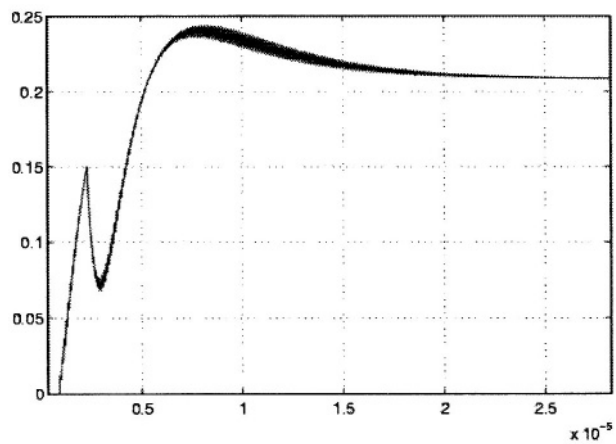


Figure A-2. Maximum stable ω_c/ω_{ref} ratio versus optimal phase margin

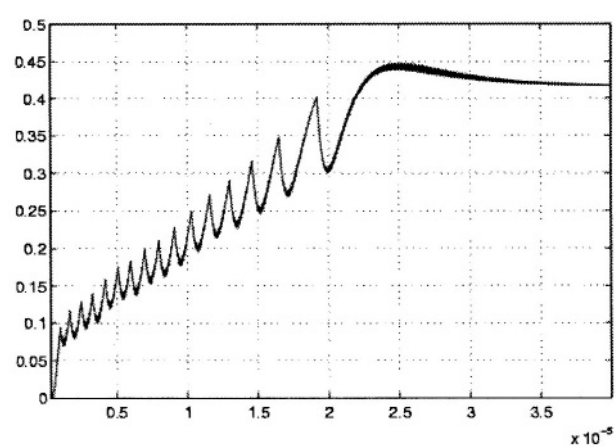
C. Nonlinear frequency pulling and linear phase locking

As shown in Fig. 3-5, the linear PFD detection range is $-2\pi < \theta_e < 2\pi$. When $\theta_e > 2\pi$ or $\theta_e < -2\pi$, a 'cycle slip' occurs. This nonlinear behavior can be simulated using the model in Fig. A-1. The loop parameters for PLL dynamic behavior simulation are: $f_{ref} = 10MHz$, $I_{cp} = 10\mu A$, $f_c = 100kHz$,

$K_{vco} = 120MHz/V$, N = 30, and loop filter values can be found in Table A-1 for $b = 16$ ($\phi_m = 62°$). The VCO control voltage V_c is shown in Fig. A-3 (a) and (b) to illustrate the nonlinear frequency pulling behavior with initial VCO frequency $f_0 = 275MHz$ and $250MHz$, respectively. It indicates that when $f_0 = 275MHz$, the 'cycle slip' occurs once where the VCO control voltage goes down. The 'cycle slip' happens frequently when $f_0 = 250MHz$, where the initial frequency error is even bigger. As mentioned in Chapter III, the average duty cycle of the charge-pump output current pulse is about 50% during nonlinear frequency pulling. The pull-in time can be calculated as in (A.2).



(a) f_0=275MHz



(b) f_0=250MHz

Figure A-3. Nonlinear frequency pulling simulation

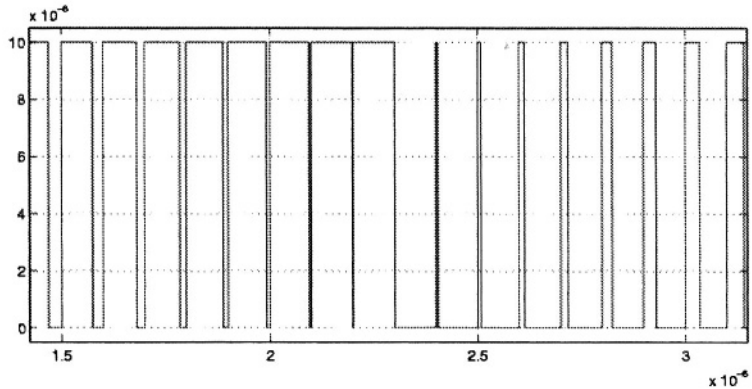


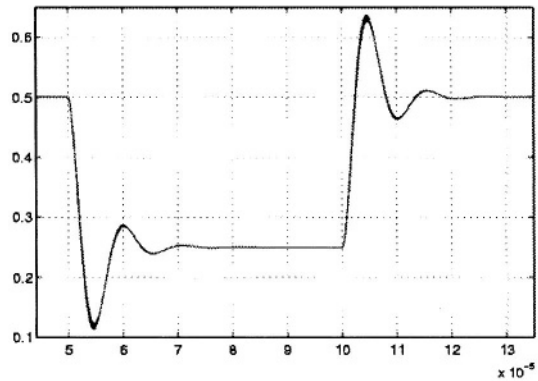
Figure A-4. Charge-pump output current pulses

$$T_P \approx \frac{(C_1 + C_2)\cdot \Delta V_c}{0.5 I_{cp}} = \frac{2(C_1 + C_2)\cdot \Delta f}{I_{cp} K_{vco}} \approx 34\mu s \qquad \text{(A.2)}$$

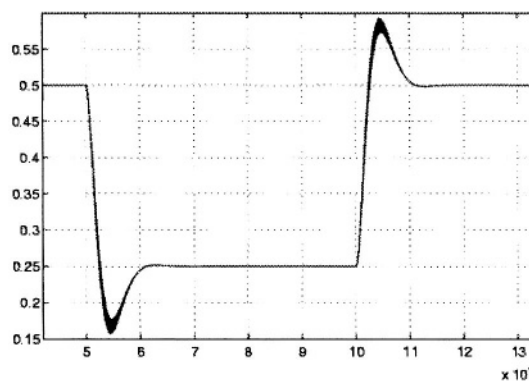
This estimated pull-in time roughly agrees with the plot shown in Fig. A-3 (b).

The 'cycle slip' in Fig. A-3 (a) is rechecked in by plotting current pulses at the charge-pump output shown in Fig. A-4. It indicates that when the divider's output frequency is less than the reference frequency, the phase error increases with time. Around time instant $t = 2.4\mu s$, the phase error θ_e is greater than 2π, that is, beyond the linear PFD detection range. Thus, the duty-cycle of the charge-pump output current pulse "falls down" from nearly 100% to almost 0%, which causes the falling down of the VCO control voltage in Fig. A-3 (a).

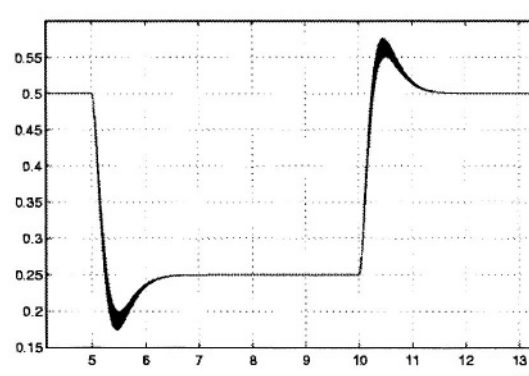
The phase error θ_e is within the linear PFD detection range of $\pm 2\pi$ during the linear phase locking. The channel switching operation in a PLL synthesizer involves a linear phase locking process. For phase-locking simulation, the PLL parameters are: $f_{ref} = 10MHz$, $I_{cp} = 100\mu A$, $f_c = 100kHz$, $K_{vco} = 40MHz/V$, $N = 100$, and $f_0 = 990MHz$. The division ratio changes between N and $N+1$. The simulated V_c for different ϕ_m values is shown in Fig. A-5. It reveals that the locking time is the minimum when ϕ_m is around 50°.



(a) ϕ_m=30° (b=3)

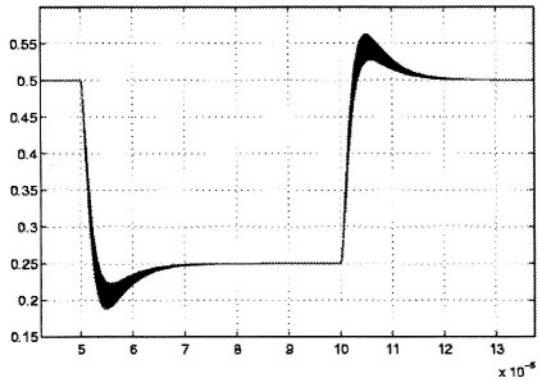


(b) ϕ_m=46° (b=6)

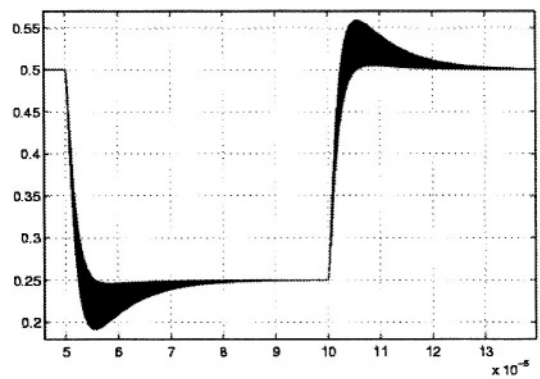


(c) ϕ_m=53° (b=9)

Figure A-5. Linear phase locking with f_{ref}/f_c=100



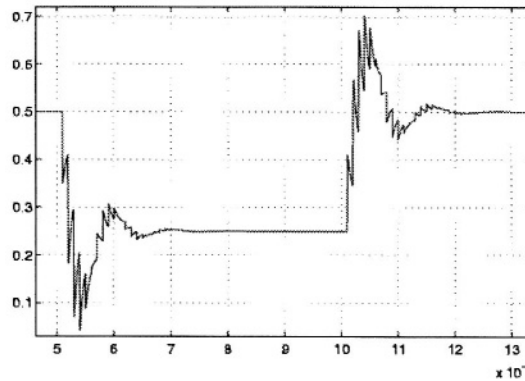
(d) ϕ_m=62° (b=16)



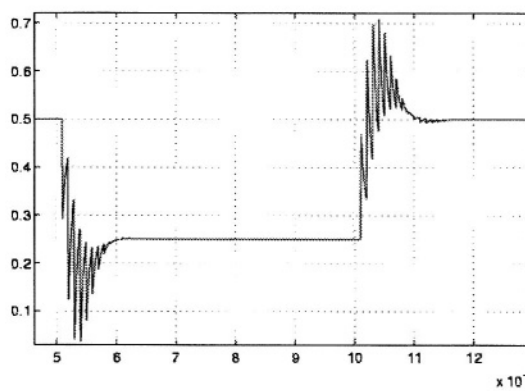
(e) ϕ_m=71° (b=36)

Figure A-5. Linear phase locking with f_{ref}/f_c=100 (continued)

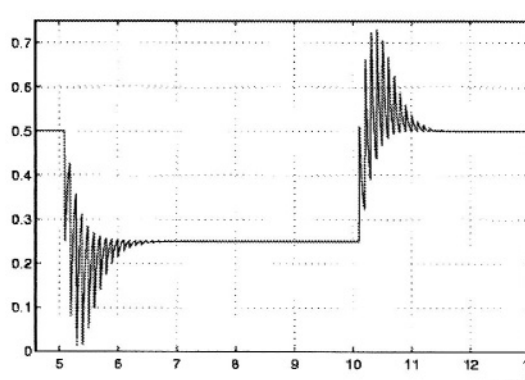
To further investigate the effect of sampling delay on the locking behavior of a PLL, the channel switching simulation is undertaken with $f_{ref}/f_c = 10$. The PLL parameters are: $f_{ref} = 1MHz$, $I_{cp} = 100\mu A$, $f_c = 100kHz$, $K_{vco} = 4MHz/V$, $N = 10$, and $f_0 = 9MHz$. As in the previous simulation, the division ratio varies between N and $N+1$. The simulated VCO control voltage with different phase margin values is shown in Fig. A-6. Comparing Fig. A-6 with Fig. A-5, we conclude that the continuous-time approximation is valid for $f_{ref}/f_c > 10$. For $f_{ref}/f_c = 10$, the locking time is the minimum when ϕ_m is around 45° [2].



(a) ϕ_m=30° (b=3)

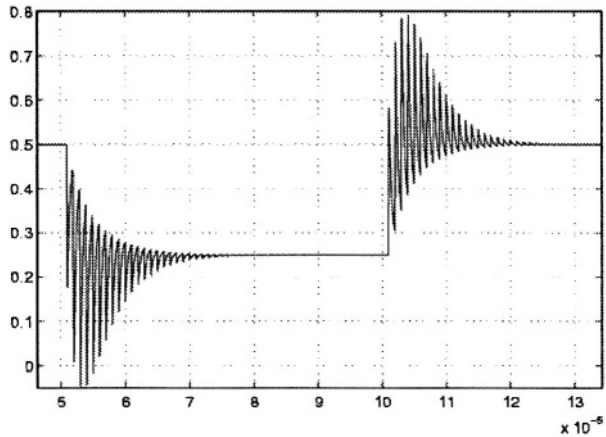


(b) ϕ_m=46° (b=6)

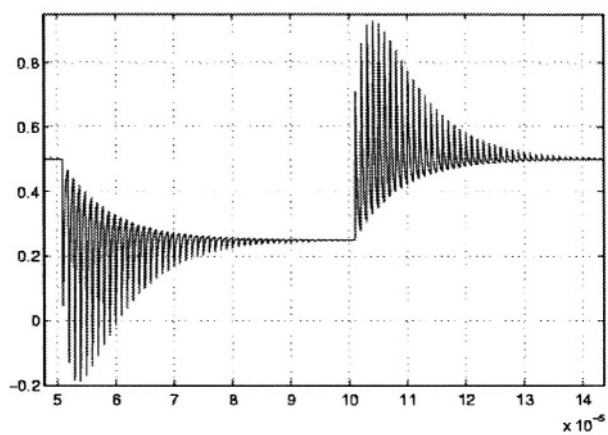


(c) ϕ_m=53° (b=9)

Figure A-6. Linear phase locking with f_{ref}/f_c=10



(d) ϕ_m=62° (b=16)



(e) ϕ_m=71° (b=36)

Figure A-6. Linear phase locking with f_{ref}/f_c=10 (continued)

D. Loop delay effect on locking behavior

To investigate the effect of loop delay on the PLL locking behavior, a delay block is added in the Simulink model as shown in Fig. A-7.

With b =16, the phase margins calculated from (3.39) for $t_d = 0.05/f_c$ and $t_d = 0.1/f_c$ are given in (A.3) and (A.4), respectively.

$$\phi_m' = \phi_m - \omega_c t_d = 62° - 18° = 44° \qquad \text{(A.3)}$$

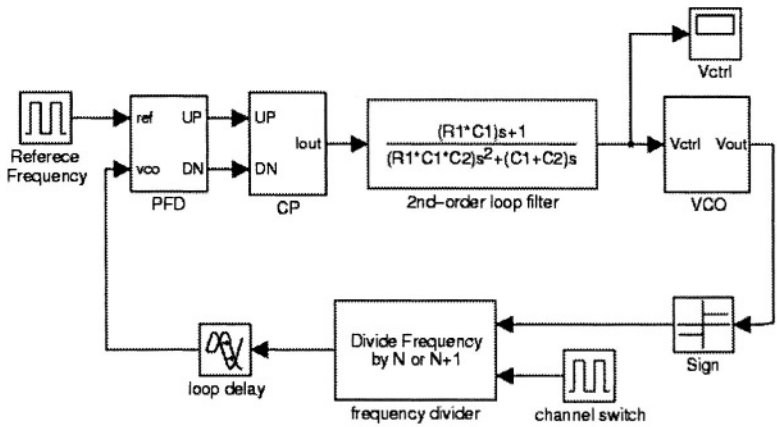
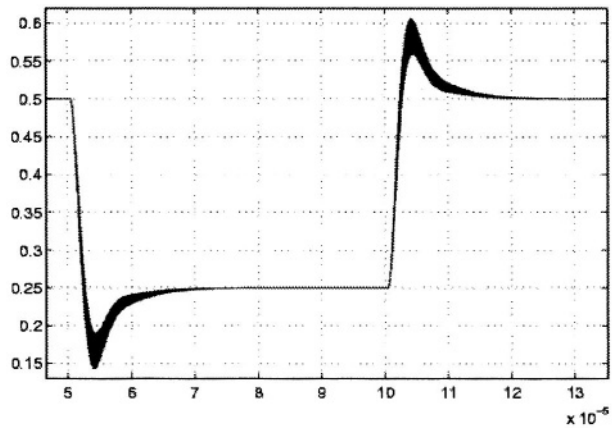


Figure A-7. Behavioral model of CP-PLL with loop delay

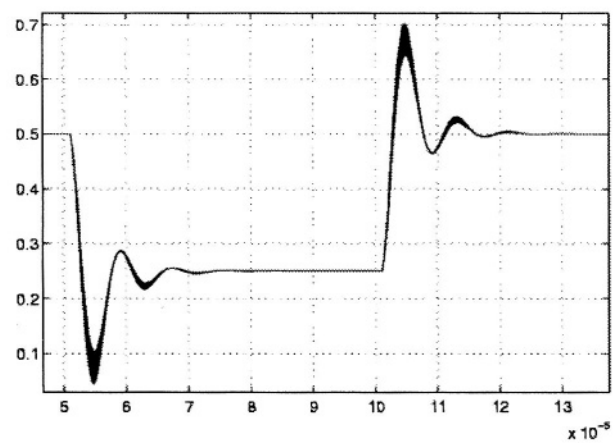
$$\phi_m^{'} = \phi_m - \omega_c t_d = 62° - 36° = 26° \tag{A.4}$$

For $f_{ref} / f_c = 100$, redo the simulation as shown in Fig. A-5 (d), which corresponds to $b = 16$. The VCO control voltage with loop delay $t_d = 0.05 / f_c$ and $t_d = 0.1 / f_c$ is shown in Fig. A-8 (a) and Fig. A-8 (b), respectively. It shows that the loop delay does reduce phase margin.

Similarly, repeat the simulation with loop delay for $f_{ref} / f_c = 10$. The VCO control voltage for $t_d = 0.05 / f_c$ and $t_d = 0.1 / f_c$ is depicted in Fig. A-9 (a) and Fig. A-9 (b), respectively.

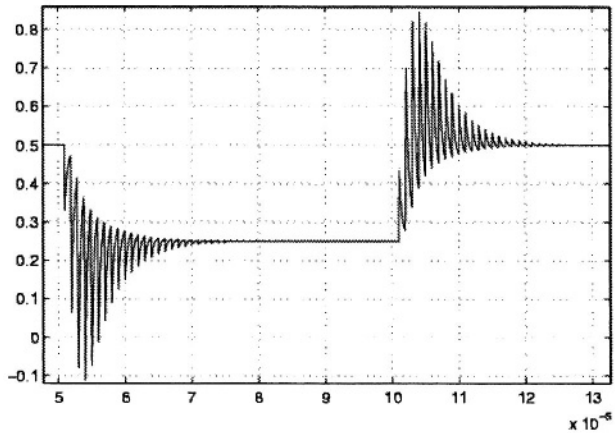


(a) t_d=0.05/ f_c (ϕ'_m=44°)

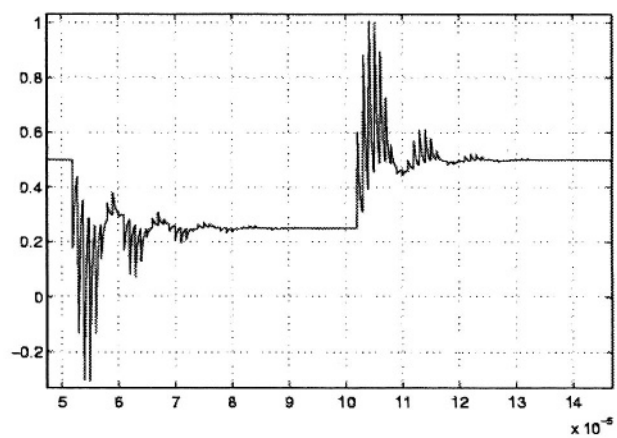


(b) t_d=0.1/ f_c (ϕ'_m=26°)

Figure A-8. Linear phase locking with f_{ref}/f_c=100 and loop delay



(a) t_d=0.05/ f_c (ϕ'_m=44°)



(b) t_d=0.1/ f_c (ϕ'_m=26°)

Figure A-9. Linear phase locking with f_{ref}/f_c=10 and loop delay

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