

11

Feedback Amplifier Theory

11.1	Introduction	11-1
11.2	Methods of Analysis	11-2
11.3	Signal Flow Analysis	11-3
11.4	Global Single-Loop Feedback	11-5
	Driving-Point I/O Resistance • Diminished Closed-Loop Damping Factor • Frequency Invariant Feedback Factor • Frequency Variant Feedback Factor (Compensation)	
11.5	Pole Splitting Open-Loop Compensation	11-11
	The Open-Loop Amplifier • Pole Splitting Analysis	
11.6	Summary	11-17

John Choma, Jr.

University of Southern California

11.1 Introduction

Feedback, whether intentional or parasitic, is pervasive of all electronic circuits and systems. In general, feedback is comprised of a subcircuit that allows a fraction of the output signal of an overall network to modify the effective input signal in such a way as to produce a circuit response that can differ substantially from the response produced in the absence of such feedback. If the magnitude and relative phase angle of the fed back signal decreases the magnitude of the signal applied to the input port of an amplifier, the feedback is said to be *negative* or **degenerative**. On the other hand, *positive* (or **regenerative**) feedback, which gives rise to oscillatory circuit responses, is the upshot of a feedback signal that increases the magnitude of the effective input signal. Because negative feedback produces stable circuit responses, the majority of all intentional feedback architectures is degenerative [1], [2]. However, parasitic feedback incurred by the energy storage elements associated with circuit layout, circuit packaging, and second-order high-frequency device phenomena often degrades an otherwise degenerative feedback circuit into either a potentially regenerative or severely underdamped network.

Intentional degenerative feedback applied around an analog network produces four circuit performance benefits. First, negative feedback desensitizes the gain of an **open-loop amplifier** (an amplifier implemented without feedback) with respect to variations in circuit element and active device model parameters. This desensitization property is crucial in view of parametric uncertainties caused by aging phenomena, temperature variations, biasing perturbations, and nonzero fabrication and manufacturing tolerances. Second, and principally because of the foregoing desensitization property, degenerative feedback reduces the dependence of circuit responses on the parameters of inherently nonlinear active devices, thereby reducing the total harmonic distortion evidenced in open loops. Third, negative feedback broadbands the dominant pole of an open-loop amplifier, thereby affording at least the possibility of a closed-loop network with improved high-frequency performance. Finally, by modifying the driving-point input and output impedances of the open-loop circuit, negative feedback provides a convenient vehicle for implementing voltage buffers, current buffers, and matched interstage impedances.

The disadvantages of negative feedback include gain attenuation, a closed-loop configuration that is disposed to potential instability, and, in the absence of suitable frequency compensation, a reduction in the open-loop gain-bandwidth product. In uncompensated feedback networks, open-loop amplifier gains are reduced in almost direct proportion to the amount by which closed-loop amplifier gains are desensitized with respect to open-loop gains. Although the 3-dB bandwidth of the open-loop circuit is increased by a factor comparable to that by which the open-loop gain is decreased, the closed-loop gain-bandwidth product resulting from uncompensated degenerative feedback is never greater than that of the open-loop configuration [3]. Finally, if feedback is incorporated around an open-loop amplifier that does not have a dominant pole [4], complex conjugate closed-loop poles yielding nonmonotonic frequency responses are likely. Even positive feedback is possible if substantive negative feedback is applied around an open-loop amplifier for which more than two poles significantly influence its frequency response.

Although the foregoing detail is common knowledge deriving from Bode's pathfinding disclosures [5], most circuit designers remain uncomfortable with analytical procedures for estimating the frequency responses, I/O impedances, and other performance indices of practical feedback circuits. The purposes of this section are to formulate systematic feedback circuit analysis procedures and ultimately, to demonstrate their applicability to six specific types of commonly used feedback architectures. Four of these feedback types, the series-shunt, shunt-series, shunt-shunt, and series-series configurations, are single-loop architectures, while the remaining two types are the series-series/shunt-shunt and series-shunt/shunt-series dual-loop configurations.

11.2 Methods of Analysis

Several standard techniques are used for analyzing linear feedback circuits [6]. The most straightforward of these entails writing the Kirchhoff equilibrium equations for the small-signal model of the entire feedback system. This analytical tack presumably leads to the idealized feedback circuit block diagram abstracted in Figure 11.1. In this model, the circuit voltage or current response, X_R , is related to the source current or voltage excitation, X_S , by

$$G_d \triangleq \frac{X_R}{X_S} = \frac{G_o}{1 + f G_o} \equiv \frac{G_o}{1 + T} \quad (11.1)$$

where G_d is the closed-loop gain of the feedback circuit, the feedback factor f is the proportion of circuit response fed back for antiphase superposition with the source signal, and G_o represents the open-loop gain. The product $f G_o$ is termed the loop gain T .

Equation (11.1) demonstrates that, for loop gains with magnitudes that are much larger than one, the closed-loop gain collapses to $1/f$, which is independent of the open-loop gain. To the extent that the

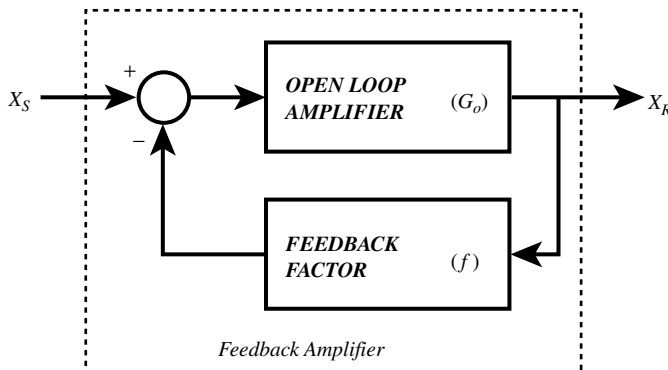


FIGURE 11.1 Block diagram model of a feedback network.

open-loop amplifier, and not the feedback subcircuit, contains circuit elements and other parameters that are susceptible to modeling uncertainties, variations in the fabrication of active and passive elements, and nonzero manufacturing tolerances, large loop gain achieves a desirable parametric desensitization. Unfortunately, the determination of G_o and f directly from the Kirchhoff relationships is a nontrivial task, especially because G_o is rarely independent of f in practical electronics. Moreover, (11.1) does not illuminate the manner in which the loop gain modifies the driving-point input and output impedances of the open-loop amplifier.

A second approach to feedback network analysis involves modeling the open-loop, feedback, and overall closed-loop networks by a homogeneous set of two-port parameters [7]. When the two-port parameter model is selected judiciously, the two-port parameters for the closed-loop network derive from a superposition of the respective two-port parameters of the open-loop and feedback subcircuits. Given the resultant parameters of the closed-loop circuit, standard formulas can then be exploited to evaluate closed-loop values of the circuit gain and the driving-point input and output impedances.

Unfortunately, several limitations plague the utility of feedback network analysis predicated on two-port parameters. First, the computation of closed-loop two-port parameters is tedious if the open-loop configuration is a multistage amplifier, or if multiloop feedback is utilized. Second, the two-loop method of feedback circuit analysis is straightforwardly applicable to only those circuits that implement **global feedback** (feedback applied from output port to input port). Many single-ended feedback amplifiers exploit only **local feedback**, wherein a fraction of the signal developed at the output port is fed back to a terminal pair other than that associated with the input port. Finally, the appropriate two-port parameters of the open-loop amplifier can be superimposed with the corresponding parameter set of the feedback subcircuit if and only if the Brune condition is satisfied [8]. This requirement mandates equality between the preconnection and postconnection values of the two-port parameters of open-loop and feedback cells, respectively. The subject condition is often not satisfied when the open-loop amplifier is not a simple three-terminal two-port configuration.

The third method of feedback circuit analysis exploits Mason's signal flow theory [9–11]. The circuit level application of this theory suffers few of the shortcomings indigenous to block diagram and two-port methods of feedback circuit analysis [12]. Signal flow analyses applied to feedback networks efficiently express I/O transfer functions, driving-point input impedances, and driving-point output impedances in terms of an arbitrarily selected critical or reference circuit parameters, say P .

An implicit drawback of signal flow methods is the fact that unless P is selected to be the feedback factor f , which is not always transparent in feedback architectures, expressions for the loop gain and the open-loop gain of feedback amplifiers are obscure. However, by applying signal flow theory to a feedback circuit model engineered from insights that derive from the results of two-port network analyses, the feedback factor can be isolated. The payoff of this hybrid analytical approach includes a conventional block diagram model of the I/O transfer function, as well as convenient mathematical models for evaluating the closed-loop driving-point input and output impedances. Yet, another attribute of hybrid methods of feedback circuit analysis is its ability to delineate the cause, nature, and magnitude of the feedforward transmittance produced by interconnecting a certain feedback subcircuit to a given open-loop amplifier. This information is crucial in feedback network design because feedforward invariably decreases gain and often causes undesirable phase shifts that can lead to significantly underdamped or unstable closed-loop responses.

11.3 Signal Flow Analysis

Guidelines for feedback circuit analysis by hybrid signal flow methods can be established with the aid of [Figure 11.2](#) [13]. [Figure 11.2\(a\)](#) depicts a linear network whose output port is terminated in a resistance, R_L . The output signal variable is the voltage V_O , which is generated in response to an input port signal whose Thévenin voltage and resistance are respectively, V_S and R_S . Implicit to the linear network is a current-controlled voltage source (CCVS) Pi_b , with a value that is directly proportional to the indicated network branch current i_b . The problem at hand is the deduction of the voltage gain $G_v(R_S, R_L) = V_O/V_S$,

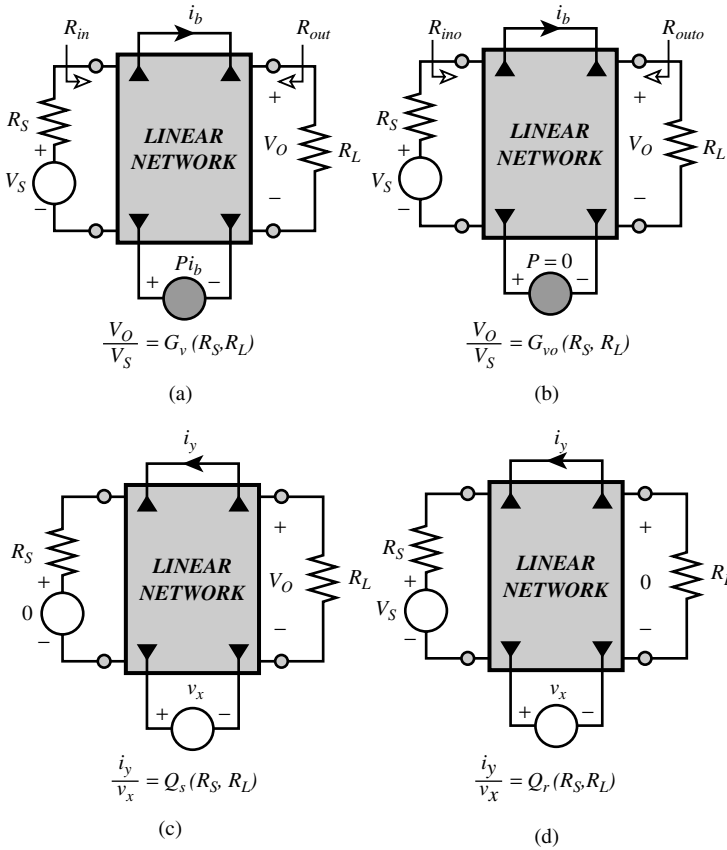


FIGURE 11.2 (a) Linear network with an identified critical parameter P . (b) Model for calculating the $P = 0$ value of voltage gain. (c) The return ratio with respect to P is $PQ_s(R_S, R_L)$. (d) The null return ratio with respect to P is $PQ_r(R_S, R_L)$.

the driving-point input resistance (or impedance) R_{in} , and the driving-point output resistance (or impedance) R_{out} , as explicit functions of the critical transimpedance parameter P . Although the following systematic procedure is developed in conjunction with the diagram in Figure 11.2, with obvious changes in notation, it is applicable to determining any type of transfer relationship for any linear network in terms of any type of reference parameter [14].

1. Set $P = 0$, as depicted in Figure 11.2(b), and compute the resultant voltage gain $G_{vo}(R_S, R_L)$, where the indicated notation suggests an anticipated dependence of gain on source and load resistances. Also, compute the corresponding driving-point input and output resistances R_{in} , and R_{out} , respectively. In this case, the “critical” parameter P is associated with a controlled voltage source. Accordingly, $P = 0$ requires that the branch containing the controlled source be supplanted by a short circuit. If, for example, P is associated with a controlled current source, $P = 0$ mandates the replacement of the controlled source by an open circuit.
2. Set the Thévenin source voltage V_S to zero, and replace the original controlled voltage source Pi_b by an independent voltage source of symbolic value, v_x . Then, calculate the ratio, i_y/v_x , where, as illustrated in Figure 11.2(c), i_y flows in the branch that originally conducts the controlling current i_b . Note, however, that the reference polarity of i_y is opposite to that of i_b . The computed transfer function i_y/v_x is denoted by $Q_s(R_S, R_L)$. This transfer relationship, which is a function of the source and load resistances, is used to determine the *return ratio* $T_s(P, R_S, R_L)$ with respect to parameter P of the original network. In particular,

$$T_s(P, R_S, R_L) = PQ_s(R_S, R_L) \tag{11.2}$$

If P is associated with a controlled current source, the controlled generator Pi_b is replaced by a current source of value i_x . If the controlling variable is a voltage, instead of a current, the ratio v_y/v_x , is computed, where v_y , where the polarity is opposite to that of the original controlling voltage, is the voltage developed across the controlling branch.

3. The preceding computational step is repeated, but instead of setting V_S to zero, the output variable, which is the voltage V_O in the present case, is nulled, as indicated in Figure 11.2(d). Let the computed ratio i_y/v_x , be symbolized as $Q_r(R_S, R_L)$. In turn, the null return ratio $T_r(P, R_S, R_L)$, with respect to parameter P is

$$T_r(P, R_S, R_L) = PQ_r(R_S, R_L) \tag{11.3}$$

4. The desired voltage gain $G_v(R_S, R_L)$, of the linear network undergoing study can be shown to be [5, 12]

$$G_v(R_S, R_L) = \frac{V_O}{V_S} = G_{vo}(R_S, R_L) \left[\frac{1 + PQ_r(R_S, R_L)}{1 + PQ_s(R_S, R_L)} \right] \tag{11.4}$$

5. Given the function $Q_s(R_S, R_L)$, the driving-point input and output resistances follow straightforwardly from [12]

$$R_{in} = R_{ino} \left[\frac{1 + PQ_s(0, R_L)}{1 + PQ_s(\infty, R_L)} \right] \tag{11.5}$$

$$R_{out} = R_{outo} \left[\frac{1 + PQ_s(R_S, 0)}{1 + PQ_s(R_S, \infty)} \right] \tag{11.6}$$

An important special case entails a controlling electrical variable i_b associated with the selected parameter P that is coincidentally the voltage or current output of the circuit under investigation. In this situation, a factor P of the circuit response is fed back to the port (not necessarily the input port) defined by the terminal pair across which the controlled source is incident. When the controlling variable i_b is the output voltage or current of the subject circuit $Q_r(R_S, R_L)$, which is evaluated under the condition of a nulled network response, is necessarily zero. With $Q_r(R_S, R_L) = 0$, the algebraic form of (11.4) is identical to that of (11.1), where the loop gain T is the return ratio with respect to parameter P ; that is,

$$PQ_s(R_S, R_L) \Big|_{Q_r(R_S, R_L)=0} = T \tag{11.7}$$

Moreover, a comparison of (11.4) to (11.1) suggests that $G_v(R_S, R_L)$ symbolizes the closed-loop gain of the circuit, $G_{vo}(R_S, R_L)$ represents the corresponding open-loop gain, and the circuit feedback factor f is

$$f = \frac{PQ_s(R_S, R_L)}{G_{vo}(R_S, R_L)} \tag{11.8}$$

11.4 Global Single-Loop Feedback

Consider the global feedback scenario illustrated in Figure 11.3(a), in which a fraction P of the output voltage V_O is fed back to the voltage-driven input port. Figure 11.3(b) depicts the model used to calculate

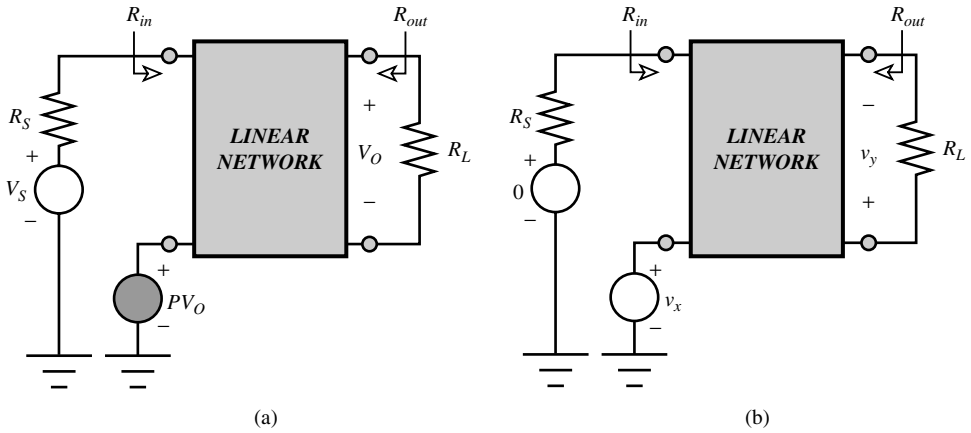


FIGURE 11.3 (a) Voltage-driven linear network with global voltage feedback. (b) Model for the calculation of loop gain.

the return ratio $Q_s(R_S, R_L)$, where, in terms of the branch variables in the schematic diagram, $Q_s(R_S, R_L) = v_y/v_x$. An inspection of this diagram confirms that the transfer function v_y/v_x is identical to the $P = 0$ value of the gain V_O/V_S , which derives from an analysis of the structure in Figure 11.3(a). Thus, for global voltage feedback in which a fraction of the output voltage is fed back to a voltage-driven input port, $Q_s(R_S, R_L)$ is the open-loop voltage gain; that is, $Q_s(R_S, R_L) \equiv G_{v_o}(R_S, R_L)$. It follows from (11.8) that the feedback factor f is identical to the selected critical parameter P . Similarly, for the global current feedback architecture of Figure 11.4(a), in which a fraction P of the output current, I_O , is fed back to the current-driven input port $f = P$. As implied by the model of Figure 11.4(b), $Q_s(R_S, R_L) \equiv G_{i_o}(R_S, R_L)$, the open-loop current gain.

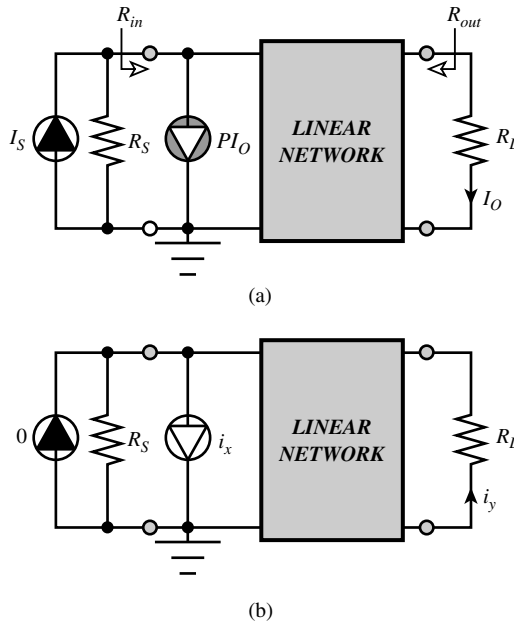


FIGURE 11.4 (a) Current-driven linear network with global current feedback. (b) Model for the calculation of loop gain.

Driving-Point I/O Resistances

Each of the two foregoing circuit architectures has a closed-loop gain where the algebraic form mirrors (11.1). It follows that for sufficiently large loop gain [equal to either $PG_{vo}(R_S, R_L)$ or $PG_{io}(R_S, R_L)$], the closed-loop gain approaches $(1/P)$ and is therefore desensitized with respect to open-loop gain parameters. However, such a desensitization with respect to the driving-point input and output resistances (or impedances) cannot be achieved. For the voltage feedback circuit in Figure 11.3(a), $Q_s(\infty, R_L)$ is the $R_S = \infty$ value, $G_{vo}(R_S, R_L)$, of the open-loop voltage gain. This particular open-loop gain is zero, because $R_S = \infty$ decouples the source voltage from the input port of the amplifier. On the other hand, $Q_s(0, R_L)$ is the $R_S = 0$ value, $G_{vo}(0, R_L)$, of the open-loop voltage gain. This gain is at least as large as $G_{vo}(R_S, R_L)$, since a short circuited Thévenin source resistance implies lossless coupling of the Thévenin signal to the amplifier input port. Recalling (11.5), the resultant driving-point input resistance of the voltage feedback amplifier is

$$R_{in} = R_{ino} \left[1 + PG_{vo}(0, R_L) \right] \geq R_{ino} \left[1 + PG_{vo}(R_S, R_L) \right] \quad (11.9)$$

which shows that the closed-loop driving-point input resistance is larger than its open-loop counterpart and is dependent on open-loop voltage gain parameters.

Conversely, the corresponding driving-point output resistance in Figure 11.3(a) is smaller than the open-loop output resistance and approximately inversely proportional to the open-loop voltage gain. These assertions derive from the facts that $Q_s(R_S, 0)$ is the $R_L = 0$ value of the open-loop voltage gain $G_{vo}(R_S, R_L)$. Because $R_L = 0$ corresponds to the short-circuited load resistance, $G_{vo}(R_S, 0) = 0$. In contrast, $Q_s(R_S, \infty)$ is the $R_L = \infty$ value, $G_{vo}(R_S, \infty)$, of the open-loop gain, which is at least as large as $G_{vo}(R_S, R_L)$. By (11.6),

$$R_{out} = \frac{R_{outo}}{1 + PG_{vo}(R_S, \infty)} \leq \frac{R_{outo}}{1 + PG_{vo}(R_S, R_L)} \quad (11.10)$$

Similarly, the driving-point input and output resistances of the global current feedback configuration of Figure 11.4(a) are sensitive to open-loop gain parameters. In contrast to the voltage amplifier of Figure 11.3(a), the closed-loop, driving-point input resistance of current amplifier is smaller than its open-loop value, while the driving-point output resistance is larger than its open-loop counterpart. Noting that the open-loop current gain $G_{io}(R_S, R_L)$ is zero for both $R_S = 0$ (which short circuits the input port), and $R_L = \infty$ (which open circuits the load port), (11.5) and (11.6) give

$$R_{in} = \frac{R_{ino}}{1 + PG_{io}(\infty, R_L)} \quad (11.11)$$

$$R_{out} = R_{outo} \left[1 + PG_{io}(R_S, 0) \right] \quad (11.12)$$

Diminished Closed-Loop Damping Factor

In addition to illuminating the driving-point and forward transfer characteristics of single-loop feedback architectures, the special case of global single-loop feedback illustrates the potential instability problems pervasive of almost all feedback circuits. An examination of these problems begins by returning to (11.1) and letting the open-loop gain, G_o , be replaced by the two-pole frequency-domain function,

$$G_o(s) = \frac{G_o(0)}{\left(1 + \frac{s}{p_1}\right) \left(1 + \frac{s}{p_2}\right)} \quad (11.13)$$

where $G_o(0)$ symbolizes the zero-frequency open-loop gain. The pole frequencies p_1 and p_2 in (11.13) are either real numbers or complex conjugate pairs. Alternatively, (11.13) is expressible as

$$G_o(s) = \frac{G_o(0)}{1 + \frac{2\zeta_{ol}}{\omega_{nol}}s + \frac{s^2}{\omega_{nol}^2}} \quad (11.14)$$

where

$$\omega_{nol} = \sqrt{p_1 p_2} \quad (11.15)$$

represents the *undamped natural frequency* of oscillation of the open-loop configuration, and

$$\zeta_{ol} = \frac{1}{2} \left[\sqrt{\frac{p_2}{p_1}} + \sqrt{\frac{p_1}{p_2}} \right] \quad (11.16)$$

is the *damping factor* of the open-loop circuit.

In (11.1), let the feedback factor f be the single left-half-plane zero function,

$$f(s) = f_o \left(1 + \frac{s}{z} \right) \quad (11.17)$$

where z is the frequency of the real zero introduced by feedback, and f_o is the zero-frequency value of the feedback factor. The resultant loop gain is

$$T(s) = f_o \left(1 + \frac{s}{z} \right) G_o(s) \quad (11.18)$$

the zero-frequency value of the loop gain is

$$T(0) = f_o G_o(0) \quad (11.19)$$

and the zero frequency closed-loop gain $G_{cl}(0)$, is

$$G_{cl}(0) = \frac{G_o(0)}{1 + f_o G_o(0)} = \frac{G_o(0)}{1 + T(0)} \quad (11.20)$$

Upon inserting (11.14) and (11.17) into (11.1), the closed-loop transfer function is determined to be

$$G_{cl}(s) = \frac{G_{cl}(0)}{1 + \frac{2\zeta_{cl}}{\omega_{ncl}}s + \frac{s^2}{\omega_{ncl}^2}} \quad (11.21)$$

where the closed-loop undamped natural frequency of oscillation ω_{ncl} relates to its open-loop counterpart ω_{nol} , in accordance with

$$\omega_{ncl} = \omega_{nol} \sqrt{1 + T(0)} \quad (11.22)$$

Moreover, the closed-loop damping factor ζ_{cl} is

$$\zeta_{cl} = \frac{\zeta_{ol}}{\sqrt{1+T(0)}} + \left[\frac{T(0)}{1+T(0)} \right] \frac{\omega_{ncl}}{2z} = \frac{\zeta_{ol}}{\sqrt{1+T(0)}} + \left[\frac{T(0)}{\sqrt{1+T(0)}} \right] \frac{\omega_{nol}}{2z} \quad (11.23)$$

A frequency invariant feedback factor $f(s)$ applied to the open-loop configuration whose transfer function is given by (11.13) implies an infinitely large frequency, z , of the feedback zero. For this case, (11.23) confirms a closed-loop damping factor that is always less than the open-loop damping factor. Indeed, for a smaller than unity open-loop damping factor (which corresponds to complex conjugate open-loop poles) and reasonable values of the zero-frequency loop gain $T(0)$, $\zeta_{cl} \ll 1$. Thus, constant feedback applied around an underdamped two-pole open-loop amplifier yields a severely underdamped closed-loop configuration. It follows that the closed-loop circuit has a transient step response plagued by overshoot and a frequency response that displays response peaking within the closed-loop passband. Observe that underdamping is likely even in critically damped (identical real open-loop poles) or overdamped (distinct real poles) open-loop amplifiers, which, respectively, correspond to $\zeta_{ol} = 1$ and $\zeta_{ol} > 1$, when a large zero-frequency loop gain is exploited.

Underdamped closed-loop amplifiers are not unstable systems, but they are nonetheless unacceptable. From a practical design perspective, closed-loop underdamping predicted by relatively simple mathematical models of the loop gain portend undesirable amplifier responses or even closed-loop instability. The problem is that simple transfer function models invoked in a manual circuit analysis are oblivious to presumably second-order parasitic circuit layout and device model energy storage elements with effects that include a deterioration of phase and gain margins.

Frequency Invariant Feedback Factor

Let the open-loop amplifier be overdamped, such that its real satisfy the relationship

$$p_2 = \kappa^2 p_1 \quad (11.24)$$

If the open-loop amplifier pole p_1 is dominant, κ^2 is a real number that is greater than the magnitude, $|G_o(0)|$, of the open-loop zero frequency gain, which is presumed to be much larger than one. The open-loop damping factor in (11.16) resultantly reduces to $\zeta_{ol} \approx \kappa/2$. With $\kappa^2 > |G_o(0)| \gg 1$, which formally reflects the *dominant pole approximation*, the 3-dB bandwidth B_{ol} of the open-loop amplifier is given approximately by [15]

$$B_{ol} \approx \frac{\omega_{nol}}{2\zeta_{ol}} = \frac{1}{\frac{1}{p_1} + \frac{1}{p_2}} = \left(\frac{\kappa^2}{\kappa^2 + 1} \right) p_1 \quad (11.25)$$

As expected, (11.25) predicts an open-loop 3-dB bandwidth that is only slightly smaller than the frequency of the open-loop dominant pole.

The frequency, z , in (11.23) is infinitely large if frequency invariant degenerative feedback is applied around on open-loop amplifier. For a critically damped or overdamped closed-loop amplifier, $\zeta_{cl} > 1$. Assuming open-loop pole dominance, this constraint imposes the open-loop pole requirement,

$$\frac{p_2}{p_1} \geq 4[1+T(0)] \quad (11.26)$$

Thus, for large zero-frequency loop gain, $T(0)$, an underdamped closed-loop response is avoided if and only if the frequency of the nondominant open-loop pole is substantially larger than that of the dominant open-loop pole. Unless frequency compensation measures are exploited in the open loop, (11.26) is

difficult to satisfy, especially if feedback is implemented expressly to realize a substantive desensitization of response with respect to open-loop parameters. On the chance that (11.26) can be satisfied, and if the closed-loop amplifier emulates a dominant pole response, the closed-loop bandwidth is, using (11.22), (11.23), and (11.25),

$$B_{cl} \approx \frac{\omega_{ncl}}{2\zeta_{cl}} \approx [1 + T(0)]B_{ol} \approx [1 + T(0)]p_1 \quad (11.27)$$

Observe from (11.27) and (11.26) that the maximum possible closed-loop 3-dB bandwidth is 2 octaves below the minimum acceptable frequency of the nondominant open-loop pole.

Although (11.27) theoretically confirms the broadbanding property of negative feedback amplifiers, the attainment of very large closed-loop 3-dB bandwidths is nevertheless a challenging undertaking. The problem is that (11.26) is rarely satisfied. As a result, the open-loop configuration must be suitably compensated, usually by pole splitting methodology [16–18], to force the validity of (11.26). However, the open-loop poles are not mutually independent, so any compensation that increases p_2 is accompanied by decreases in p_1 . The pragmatic upshot of the matter is that the closed-loop 3-dB bandwidth is not directly proportional to the uncompensated value of p_1 but instead, it is proportional to the smaller, compensated value of p_1 .

Frequency Variant Feedback Factor (Compensation)

Consider now the case where the frequency, z , of the compensating feedback zero is finite and positive. Equation (11.23) underscores the stabilizing property of a left-half-plane feedback zero in that a sufficiently small positive z renders a closed-loop damping factor ζ_{cl} that can be made acceptably large, regardless of the value of the open-loop damping factor ζ_{ol} . To this end, $\zeta_{cl} > 1/\sqrt{2}$ is a desirable design objective in that it ensures a monotonically decreasing closed-loop frequency response. If, as is usually a design goal, the open-loop amplifier subscribes to pole dominance, (11.23) translates the objective, $\zeta_{cl} > 1/\sqrt{2}$, into the design constraint

$$z \leq \frac{\left[\frac{T(0)}{1 + T(0)} \right] \omega_{ncl}}{\sqrt{2} - \frac{\omega_{ncl}}{[1 + T(0)]B_{ol}}} \quad (11.28)$$

where use is made of (11.25) to cast ζ in terms of the open-loop bandwidth B_{ol} . When the closed-loop damping factor is precisely equal to $1/\sqrt{2}$ a maximally flat magnitude closed-loop response results for which the 3-dB bandwidth is ω_{ncl} . Equation (11.28) can then be cast into the more useful form

$$zG_{cl}(0) = \frac{GBP_{ol}}{\sqrt{2} \left(\frac{GBP_{ol}}{GBP_{cl}} \right) - 1} \quad (11.29)$$

where (11.20) is exploited, GBP_{ol} is the *gain-bandwidth product* of the open-loop circuit, and GBP_{cl} is the gain-bandwidth product of the resultant closed-loop network.

For a given open-loop gain-bandwidth product GBP_{ol} , a desired low-frequency closed-loop gain, $G_{cl}(0)$, and a desired closed-loop gain-bandwidth product, GBP_{cl} , (11.29) provides a first-order estimate of the requisite feedback compensation zero. Additionally, note that (11.29) imposes an upper limit on the achievable high-frequency performance of the closed-loop configuration. In particular, because z must be positive to ensure acceptable closed-loop damping, (11.29) implies

$$\text{GBP}_{\text{ol}} > \frac{\text{GBP}_{\text{cl}}}{\sqrt{2}} \quad (11.30)$$

In effect, (11.30) imposes a lower limit on the required open-loop gain-bandwidth product commensurate with feedback compensation implemented to achieve a maximally flat, closed-loop frequency response.

11.5 Pole Splitting Open-Loop Compensation

Equation (11.26) underscores the desirability of achieving an open-loop dominant pole frequency response in the design of a feedback network. In particular, (11.26) shows that if the ultimate design goal is a closed-loop dominant pole frequency response, the frequency, p_2 , of the nondominant open-loop amplifier pole must be substantially larger than its dominant pole counterpart, p_1 . Even if closed-loop pole dominance is sacrificed as a trade-off for other performance merits, open-loop pole dominance is nonetheless a laudable design objective. This contention follows from (11.23) and (11.16), which combine to suggest that the larger p_2 is in comparison to p_1 , the larger is the open-loop damping factor. In turn, the unacceptably underdamped closed-loop responses that are indicative of small, closed-loop damping factors are thereby eliminated. Moreover, (11.23) indicates that larger, open-loop damping factors impose progressively less demanding restrictions on the feedback compensation zero that may be required to achieve acceptable closed-loop damping. This observation is important because in an actual circuit design setting, small z in (11.23) generally translates into a requirement of a correspondingly large RC time constant, where implementation may prove difficult in monolithic circuit applications.

Unfortunately, many amplifiers, and particularly broadbanded amplifiers, earmarked for use as open-loop cells in degenerative feedback networks, are not characterized by dominant pole frequency responses. The frequency response of these amplifiers is therefore optimized in accordance with a standard design practice known as **pole splitting compensation**. Such compensation entails the connection of a small capacitor between two high impedance, phase inverting nodes of the open-loop topology [17, 19–21]. Pole splitting techniques increase the frequency p_2 of the uncompensated nondominant open-loop pole to a compensated value, say p_{2c} . The frequency, p_1 , of the uncompensated dominant open-loop pole is simultaneously reduced to a smaller frequency, say p_{1c} . Although these pole frequency translations complement the design requirement implicit to (11.26) and (11.23), they do serve to limit the resultant closed-loop bandwidth, as discussed earlier. As highlighted next, they also impose other performance limitations on the open loop.

The Open-Loop Amplifier

The engineering methods, associated mathematics, and engineering trade-offs underlying pole splitting compensation are best revealed in terms of the generalized, phase inverting linear network abstracted in [Figure 11.5](#). Although this amplifier may comprise the entire open-loop configuration, in the most general case, it is an interstage of the open loop. Accordingly, R_{st} in this diagram is viewed as the Thévenin equivalent resistance of either an input signal source or a preceding amplification stage. The response to the Thévenin driver, V_{st} , is the indicated output voltage, V_i , which is developed across the Thévenin load resistance, R_i , seen by the stage under investigation. Note that the input current conducted by the amplifier is I_s , while the current flowing into the output port of the unit is denoted as I_i . The dashed branch containing the capacitor C_c , which is addressed later, is the pole splitting compensation element.

Because the amplifier under consideration is linear, any convenient set of two-port parameters can be used to model its terminal volt-ampere characteristics. Assuming the existence of the short circuit admittance, or y parameters,

$$\begin{bmatrix} I_s \\ I_i \end{bmatrix} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} \begin{bmatrix} V_i \\ V_i \end{bmatrix} \quad (11.31)$$

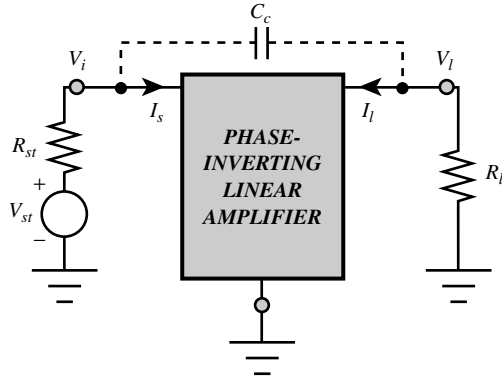


FIGURE 11.5 A linear amplifier for which a pole splitting compensation capacitance C_c is incorporated.

Defining

$$\begin{aligned}
 y_o &\triangleq y_{11} + y_{12} \\
 y_o &\triangleq y_{22} + y_{12} \\
 y_f &\triangleq y_{21} + y_{12} \\
 y_r &\triangleq -y_{12}
 \end{aligned}
 \tag{11.32}$$

(11.31) implies

$$I_s = y_i V_i + y_r (V_i - V_l) \tag{11.33}$$

$$I_l = y_f V_i + y_o V_l + y_r (V_l - V_i) \tag{11.34}$$

The last two expressions produce the y -parameter model depicted in Figure 7.6(a), in which y_i represents an effective shunt input admittance, y_o is a shunt output admittance, y_f is a forward transadmittance, and y_r reflects voltage feedback intrinsic to the amplifier.

Amplifiers amenable to pole splitting compensation have capacitive input and output admittances; that is, y_i and y_o are of the form

$$\begin{aligned}
 y_i &= \frac{1}{R_i} + sC_i \\
 y_o &= \frac{1}{R_o} + sC_o
 \end{aligned}
 \tag{11.35}$$

Similarly,

$$\begin{aligned}
 y_f &= G_f - sC_f \\
 y_r &= \frac{1}{R_r} + sC_r
 \end{aligned}
 \tag{11.36}$$

In (11.36), the conductance component G_f of the forward transadmittance y_f positive in a phase-inverting amplifier. Moreover, the reactive component $-sC_f$ of y_f produces an *excess phase angle*, and hence, a *group*

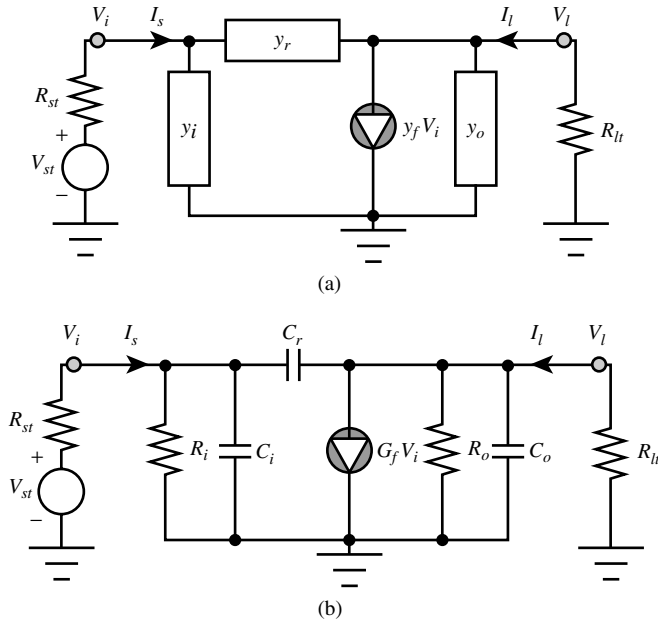


FIGURE 11.6 (a) The y -parameter equivalent circuit of the phase-inverting linear amplifier in Fig. 11.5. (b) An approximate form of the model in (a).

delay, in the forward gain function. This component, which deteriorates phase margin, can be ignored to first order if the signal frequencies of interest are not excessive in comparison to the upper-frequency limit of performance of the amplifier. Finally, the feedback internal to many practical amplifiers is predominantly capacitive so that the feedback resistance R_r can be ignored. These approximations allow the model in Figure 7.6(a) to be drawn in the form offered in Figure 11.6(b).

It is worthwhile interjecting that the six parameters indigenous to the model in Figure 11.6(b) need not be deduced analytically from the small-signal models of the active elements embedded in the subject interstage. Instead, SPICE can be exploited to evaluate the y parameters in (11.31) at the pertinent biasing level. Because these y parameters display dependencies on signal frequency, care should be exercised to evaluate their real and imaginary components in the neighborhood of the open-loop, 3-dB bandwidth to ensure acceptable computational accuracy at high frequencies. Once the y parameters in (11.31) are deduced by computer-aided analysis, the alternate admittance parameters in (11.23), as well as numerical estimates for the parameters, R_i , C_i , R_o , C_o , C_r , and G_f , in (11.35) and (11.36) follow straightforwardly.

Pole Splitting Analysis

An analysis of the circuit in Figure 11.6(b) produces a voltage transfer function $A_v(s)$ of the form

$$A_v(s) = \frac{V_l(s)}{V_{st}(s)} = A_v(0) \left[\frac{1 - \frac{s}{z_r}}{\left(1 + \frac{s}{p_1}\right) \left(1 + \frac{s}{p_2}\right)} \right] \tag{11.37}$$

Letting

$$R_{lt} = R_{lt} \parallel R_o \tag{11.38}$$

an inspection of the circuit in Figure 11.6(b) confirms that

$$A_v(0) = -G_f R_{ll} \left(\frac{R_i}{R_i + R_{st}} \right) \quad (11.39)$$

is the zero frequency voltage gain. Moreover, the frequency, z_r , of the right-half-plane zero is

$$z_r = \frac{G_f}{C_r} \quad (11.40)$$

The lower pole frequency, p_1 , and the higher pole frequency, p_2 , derive implicitly from

$$\frac{1}{p_1} + \frac{1}{p_2} = R_{ll}(C_o + C_r) + R_{ss} \left[C_i + (1 + G_f R_{ll}) C_r \right] \quad (11.41)$$

and

$$\frac{1}{p_1 p_2} = R_{ss} R_{ll} C_o \left[C_i + \left(\frac{C_o + C_i}{C_o} \right) C_r \right] \quad (11.42)$$

where

$$R_{ss} = R_{st} \stackrel{\Delta}{=} R_i \quad (11.43)$$

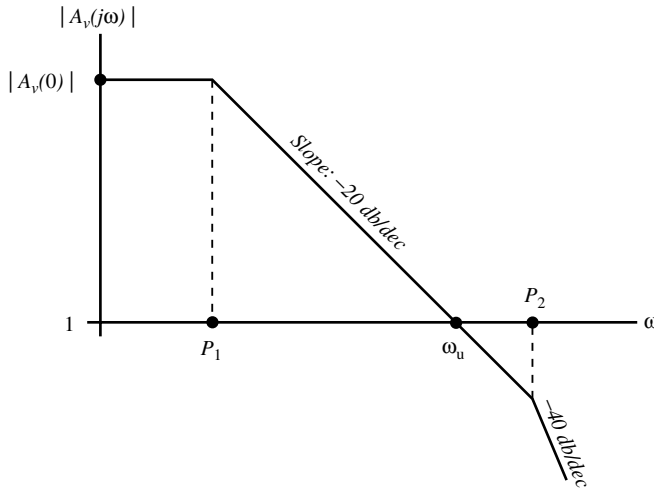
Most practical amplifiers, and particularly amplifiers realized in bipolar junction transistor technology, have very large forward transconductance, G_f , and small internal feedback capacitance, C_r . The combination of large G_f and small C_r renders the frequency in (11.40) so large as to be inconsequential to the passband of interest. When utilized in a high-gain application, such as the open-loop signal path of a feedback amplifier, these amplifiers also operate with a large effective load resistance, R_{ll} . Accordingly, (11.41) can be used to approximate the pole frequency p_1 as

$$p_1 \approx \frac{1}{R_{ss} \left[C_i + (1 + G_f R_{ll}) C_r \right]} \quad (11.44)$$

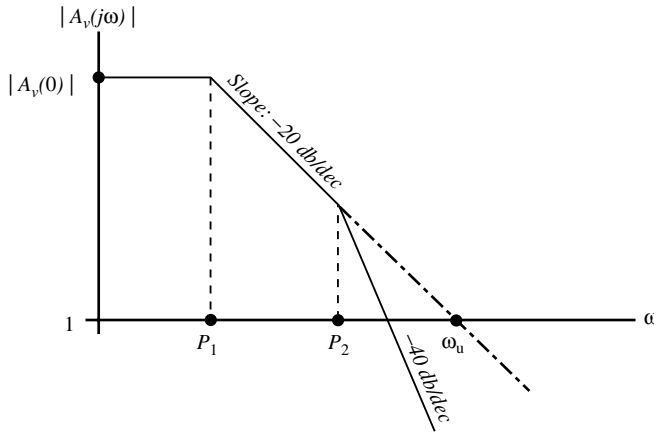
Substituting this result into (11.42), the approximate frequency p_2 of the high-frequency pole is

$$p_2 \approx \frac{C_i + (1 + G_f R_{ll}) C_r}{R_{ll} C_o \left[C_i + \left(\frac{C_o + C_i}{C_o} \right) C_r \right]} \quad (11.45)$$

Figure 11.7 illustrates asymptotic frequency responses corresponding to pole dominance and to a two-pole response. Figure 11.7(a) depicts the frequency response of a dominant pole amplifier, which does not require pole splitting compensation. Observe that its high-frequency response is determined by a single pole (p_1 in this case) through the signal frequency at which the gain ultimately degrades to unity. In this interpretation of a dominant pole amplifier, p_2 is not only much larger than p_1 , but is in fact larger than the unity gain frequency, which is indicated as ω_u in the figure. This unity gain frequency, which can be viewed as an upper limit to the useful passband of the amplifier, is approximately, $|A_v(0)|p_1$. To the extent that p_1 is essentially the 3-dB bandwidth when $p_2 \gg p_1$, the unity gain frequency is also the



(a)



(b)

FIGURE 11.7 (a) Asymptotic frequency response for a dominant pole amplifier. Such an amplifier does not require pole splitting compensation because the two lowest frequency amplifier poles, p_1 and p_2 , are already widely separated. (b) The frequency response of an amplifier with high-frequency response that is strongly influenced by both of its lowest frequency poles. The basic objective of pole splitting compensation is to transform the indicated frequency response to a form that emulates that depicted in (a).

gain-bandwidth product (GBP) of the subject amplifier. In short, with $|A_v(j\omega_u)| \triangleq 1$, $p_2 \gg p_1$ in (11.37) implies

$$\omega_u \approx |A_v(0)|p_1 \approx \text{GBP} \tag{11.46}$$

The contrasting situation of a response indigenous to the presence of two significant open-loop poles is illustrated in Figure 11.7(b). In this case, the higher pole frequency p_2 is smaller than ω_u and hence, the amplifier does not emulate a single-pole response throughout its theoretically useful frequency range. The two critical frequencies, p_1 and p_2 , remain real numbers, and as long as $p_2 \neq p_1$, the corresponding damping factor, is greater than one. However, the damping factor of the two-pole amplifier (its response is plotted in Figure 11.7(b)) is nonetheless smaller than that of the dominant pole amplifier. It follows that, for reasonable loop gains, unacceptable underdamping is more likely when feedback is invoked around the

two-pole amplifier, as opposed to the same amount of feedback applied around a dominant pole amplifier. Pole splitting attempts to circumvent this problem by transforming the pole conglomeration of the two pole amplifier into one that emulates the dominant pole situation inferred by Figure 11.7(a).

To the foregoing end, append the compensation capacitance C_c between the input and the output ports of the phase-inverting linear amplifier, as suggested in Figure 11.5. With reference to the equivalent circuit in Figure 11.6(b), the electrical impact of this additional element is the effective replacement of the internal feedback capacitance C_r by the capacitance sum $(C_r + C_c)$. Letting

$$C_p \triangleq C_r + C_c \quad (11.47)$$

it is apparent that (11.40)–(11.42) remain applicable, provided that C_r in these relationships is supplanted by C_p . Because C_p is conceivably significantly larger than C_c , however, the approximate expressions for the resultant pole locations differ from those of (11.44) and (11.45). In particular, a reasonable approximation for the compensated value, say p_{1c} , of the lower pole frequency is now

$$p_{1c} \approx \frac{1}{\left[R_{ll} + (1 + G_f R_{ll}) R_{ss} \right] C_p} \quad (11.48)$$

while the higher pole frequency, p_{2c} , becomes

$$p_{2c} \approx \frac{1}{\left(R_{ss} \parallel R_{ll} \parallel \frac{1}{G_f} \right) (C_o + C_i)} \quad (11.49)$$

Clearly, $p_{1c} < p_1$ and $p_{2c} > p_2$. Moreover, for large G_f , p_{2c} is potentially much larger than p_{1c} . It should also be noted that the compensated value, say z_{rc} , of the right-half-plane zero is smaller than its uncompensated value, z_r , because (11.40) demonstrates that

$$z_{rc} = \frac{G_f}{C_p} = z_r \left(\frac{C_r}{C_r + C_c} \right) \quad (11.50)$$

Although z_{rc} can conceivably exert a significant influence on the high-frequency response of the compensated amplifier, the following discussion presumes tacitly that $z_{rc} > p_{2c}$ [2].

Assuming a dominant pole frequency response, the compensated unity gain frequency, ω_{uc} , is, using (11.39), (11.46), and (11.48),

$$\omega_{uc} \approx |A_v(0)| p_{1c} \approx \left(\frac{1}{R_{st} C_p} \right) \left[G_f \left(R_{ss} \parallel R_{ll} \parallel \frac{1}{G_f} \right) \right] \quad (11.51)$$

It is interesting to note that

$$\omega_{uc} < \left(\frac{1}{R_{st} C_p} \right) \quad (11.52)$$

that is, the unity gain frequency is limited by the inverse of the RC time constant formed by the Thévenin source resistance R_{st} and the net capacitance C_p appearing between the input port and the phase inverted output port. The subject inequality comprises a significant performance limitation, for if p_{2c} is indeed

much larger than p_{ic} , ω_{uc} is approximately the GBP of the compensated cell. Accordingly, for a given source resistance, a required open-loop gain, and a desired open-loop bandwidth, (11.52) imposes an upper limit on the compensation capacitance that can be exploited for pole splitting purposes.

In order for the compensated amplifier to behave as a dominant pole configuration, p_{2c} must exceed ω_{uc} , as defined by (11.51). Recalling (11.49), the requisite constraint is found to be

$$R_{st}C_p > G_f \left(R_{ss} \| R_{ll} \left\| \frac{1}{G_f} \right. \right)^2 (C_o + C_i) \tag{11.53}$$

Assuming $G_f(R_{ss}/R_{ll}) \ll 1$, (11.53) reduces to the useful simple form

$$C_f R_{st} > \frac{C_o + C_i}{C_p} \tag{11.54}$$

which confirms the need for large forward transconductance G_f if pole splitting is to be an effective compensation technique.

11.6 Summary

The use of negative feedback is fundamental to the design of reliable and reproducible analog electronic networks. Accordingly, this chapter documents the salient features of the theory that underlies the efficient analysis and design of commonly used feedback networks. Four especially significant points are postulated in this section.

1. By judiciously exploiting signal flow theory, the classical expression, (11.1), for the I/O transfer relationship of a linear feedback system is rendered applicable to a broad range of electronic feedback circuits. This expression is convenient for design-oriented analysis because it clearly identifies the open-loop gain, G_o , and the loop gain, T . The successful application of signal flow theory is predicated on the requirement that the feedback factor, to which T is proportional and that appears in the signal flow literature as a “critical” or “reference” parameter, can be identified in a given feedback circuit.
2. Signal flow theory, as applied to electronic feedback architectures, proves to be an especially expedient analytical tool because once the loop gain T is identified, the driving-point input and output impedances follow with minimal additional calculations. Moreover, the functional dependence of T on the Thévenin source and terminating load impedances unambiguously brackets the magnitudes of the driving point I/O impedances attainable in particular types of feedback arrangements.
3. The damping factor concept is advanced herewith as a simple way of assessing the relative stability of both the open and closed loops of a feedback circuit. The open-loop damping factor derives directly from the critical frequencies of the open-loop gain, while these frequencies and any zeros appearing in the loop gain unambiguously define the corresponding closed-loop damping factor. Signal flow theory is once again used to confirm the propensity of closed loops toward instability unless the open-loop subcircuit functions as a dominant pole network. Also confirmed is the propriety of the common practice of implementing a feedback zero as a means of stabilizing an otherwise potentially unstable closed loop.
4. Pole splitting as a means to achieve dominant pole open-loop responses is definitively discussed. Generalized design criteria are formulated for this compensation scheme, and limits of performance are established. Of particular interest is the fact that pole splitting limits the GBP of the compensated amplifier to a value that is determined by a source resistance-compensation capacitance time constant.

References

- [1] J. A. Mataya, G. W. Haines, and S. B. Marshall, "IF amplifier using C_c -compensated transistors," *IEEE J. Solid-State Circuits*, vol. SC-3, pp. 401–407, Dec. 1968.
- [2] W. G. Beall and J. Choma, Jr., "Charge-neutralized differential amplifiers," *J. Analog Integrat. Circuits Signal Process.*, vol. 1, pp. 33–44, Sep. 1991.
- [3] J. Choma, Jr., "A generalized bandwidth estimation theory for feedback amplifiers," *IEEE Trans. Circuits Syst.*, vol. CAS-31, pp. 861–865, Oct. 1984.
- [4] R. D. Thornton, C. L. Searle, D. O. Pederson, R. B. Adler, and E. J. Angelo, Jr., *Multistage Transistor Circuits*, New York: John Wiley & Sons, 1965, chaps. 1, 8.
- [5] H. W. Bode, *Network Analysis and Feedback Amplifier Design*, New York: Van Nostrand, 1945.
- [6] P. J. Hurst, "A comparison of two approaches to feedback circuit analysis," *IEEE Trans Education*, vol. 35, pp. 253–261, Aug. 1992.
- [7] M. S. Ghauri, *Principles and Design of Linear Active Networks*, New York: McGraw-Hill, 1965, pp. 40–56.
- [8] A. J. Cote, Jr. and J. B. Oakes, *Linear Vacuum-Tube and Transistor Circuits*, New York: McGraw-Hill, 1961, pp. 40–46.
- [9] S. J. Mason, "Feedback theory — Some properties of signal flow graphs," *Proc. IRE*, vol. 41, pp. 1144–1156, Sep. 1953.
- [10] S. J. Mason, "Feedback theory — Further properties of signal flow graphs," *Proc. IRE*, vol. 44, pp. 920–926, July 1956.
- [11] N. Balabanian and T. A. Bickart, *Electrical Network Theory*, New York: John Wiley & Sons, 1969, pp. 639–669.
- [12] J. Choma, Jr., "Signal flow analysis of feedback networks," *IEEE Trans. Circuits Syst.*, vol. 37, pp. 455–463, April 1990.
- [13] J. Choma, Jr., *Electrical Networks: Theory and Analysis*, New York: Wiley Interscience, 1985, pp. 589–605.
- [14] P. J. Hurst, "Exact simulation of feedback circuit parameters," *IEEE Trans. Circuits Syst.*, vol. 38, pp. 1382–1389, Nov. 1991.
- [15] J. Choma, Jr. and S. A. Witherspoon, "Computationally efficient estimation of frequency response and driving point impedance in wideband analog amplifiers," *IEEE Trans. Circuits Syst.*, vol. 37, pp. 720–728, June 1990.
- [16] R. G. Meyer and R. A. Blauschild, "A wide-band low-noise monolithic transimpedance amplifier," *IEEE J. Solid-State Circuits*, vol. SC-21, pp. 530–533, Aug. 1986.
- [17] Y. P. Tsividis, "Design considerations in single-channel MOS analog integrated circuits," *IEEE J. Solid-State Circuits*, vol. SC-13, pp. 383–391, June 1978.
- [18] J. J. D'Azzo and C. H. Houppis, *Feedback Control System Analysis and Synthesis*, New York: McGraw-Hill, 1960, pp. 230–234.
- [19] P. R. Gray and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, New York: John Wiley & Sons, 1977, pp. 512–521.
- [20] P. R. Gray, "Basic MOS operational amplifier design — An overview," in *Analog MOS Integrated Circuits*, P. R. Gray, D. A. Hodges, and R. W. Brodersen, Eds., New York: IEEE, 1980, pp. 28–49.
- [21] J. E. Solomon, "The monolithic op-amp: A tutorial study," *IEEE J. Solid-State Circuits*, vol. SC-9, pp. 314–332, Dec. 1974.