2

Network Laws and Theorems

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2.1 Kirchhoff's Voltage and Current Laws

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Circuit analysis, like Euclidean geometry, can be treated as a mathematical system; that is, the entire theory can be constructed upon a foundation consisting of a few fundamental concepts and several axioms relating these concepts. As it happens, important advantages accrue from this approach — it is not simply a desire for mathematical rigor, but a pragmatic need for simplification that prompts us to adopt such a mathematical attitude.

The basic concepts are conductor, element, time, voltage, and current. Conductor and element are axiomatic; thus, they cannot be defined, only explained. A conductor is the idealization of a piece of copper wire; an element is a region of space penetrated by two conductors of finite length termed **leads** and pronounced "leeds". The ends of these leads are called **terminals** and are often drawn with small circles as in Figure 2.1.

Conductors and elements are the basic objects of circuit theory; we will take time, voltage, and current as the basic variables. The time variable is measured with a clock (or, in more picturesque language, a chronometer). Its unit is the second, *s*. Thus, we will say that time, like voltage and current, is defined **operationally**, that is, by means of a measuring instrument and a procedure for measurement. Our view of reality in this context is consonant with that branch of philosophy termed **operationalism** [1].

Voltage is measured with an instrument called a *voltmeter,* as illustrated in Figure 2.2. In Figure 2.2, a voltmeter consists of a readout device and two long, flexible conductors terminated in points called **probes** that can be held against other conductors, thereby making electrical contact with them. These conductors are usually covered with an insulating material. One is often colored red and the other black. The one colored red defines the positive polarity of voltage, and the other the negative polarity. Thus, voltage is always measured between two conductors. If these two conductors are element leads, the voltage is that across the corresponding element. Figure 2.3 is the symbolic description of such a measurement; the variable v, along with the corresponding plus and minus signs, means exactly the experimental procedure depicted in Figure 2.2, neither more nor less. The outcome of the measurement, incidentally, can be either positive or negative. Thus, a reading of $v = -12$ V, for example, has meaning only when

FIGURE 2.1 Conductors and elements.

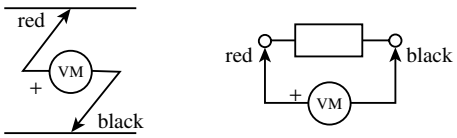

FIGURE 2.2 The operational definition of voltage.

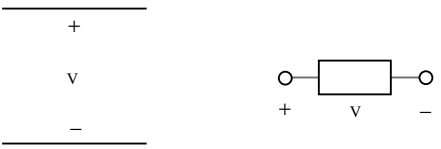

FIGURE 2.3 The symbolic description of the voltage measurement.

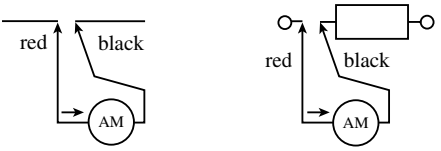

FIGURE 2.4 The operational definition of current.

FIGURE 2.5 The symbolic representation of a current measurement.

viewed within the context of the measurement. If the meter leads are simply reversed after the measurement just described, a reading of $v' = +12$ V will result. The latter, however, is a different variable; hence, we have changed the symbol to v'. The V after the numerical value is the unit of voltage, the volt, V.

Although voltage is measured across an element (or between conductors), current is measured through a conductor or element. Figure 2.4 provides an operational definition of current. One cuts the conductor or element lead and touches one meter lead against one terminal thus formed and the other against the second. A shorthand symbol for the meter connection is an arrow close to one lead of the ammeter. This arrow, along with the meter reading, defines the current. We show the shorthand symbol for a current in Figure 2.5. The reference arrow and the symbol i are shorthand for the complete measurement in Figure 2.4 — merely this and nothing more. The variable i can be either positive or negative; for example, one possible outcome of the measurement might be $i = -5$ A. The A signifies the unit of current, the ampere. If the red and black leads in Figure 2.4 were reversed, the reading sign would change.

Table 2.1 provides a summary of the basic concepts of circuit theory: the two basic objects and the three fundamental variables. Notice that we are a bit at variance with the SI system here because although time and current are considered fundamental in that system, voltage is not. Our approach simplifies things, however, for one does not require any of the other SI units or dimensions. All other quantities

TABLE 2.1 Summary of the Basic Concepts of Circuit Theory

Objects		Variables		
Conductor	Element	Time	Voltage	Current
—	—	Seconds, s	Volt, V	Ampere, A

are derived. For instance, charge is the integral of current and its unit is the ampere-second, or the coulomb, C. Power is the product of voltage and current. Its unit is the watt, W. Energy is the integral power, and has the unit of the watt-second, or joule, J. In this manner one avoids the necessity of introducing mechanical concepts, such as mechanical work, as being the product of force and distance.

In the applications of circuit theory, of course, one has need of the other concepts of physics. If one is to use circuit analysis to determine the efficiency of an electric motor, for example, the concept of mechanical work is necessary. However — and this is the main point of our approach — the introduction of such concepts is not essential in the analysis of a circuit itself. This idea is tied in to the concept of modeling. The basic catalog of elements used here does not include such things as temperature effects or radiation of electromagnetic energy. Furthermore, a "real" element such as resistor is not "pure." A real resistor is more accurately modeled, for many purposes, as a resistor plus series inductance and shunt capacitance. The point is this: In order to adequately model the "real world" one must often use complicated combinations of the basic elements. Additionally, to incorporate the influence of variables such as temperature, one must assume that certain parameters (such as resistance or capacitance) are functions of that variable. It is the determination of the more complicated model or the functional relationship of a given parameter to, for example, temperatures that fall within the realm of the practitioner. Such ideas were discussed more fully in Chapter 1. Circuit analysis merely provides the tools for analyzing the end result.

The radiation of electromagnetic energy is, on the other hand, a quite different aspect of circuit theory. As will be seen, circuit analysis falls within a regime in which such behavior can be neglected. Thus, the theory of circuit analysis we will expound has a limited range of application: to low frequencies or, what is the same in the light of Fourier analysis, to waveforms that do not vary too rapidly.

We are now in a position to state two basic axioms, which we will assume all circuits obey:

Axiom 1: The behavior of an element is completely determined by its *v–i* characteristic, which can be determined by tests made on the element in isolation from the other elements in the circuit in which it is connected.

Axiom 2: The behavior of a circuit is independent of the size or the shape or the orientation of its elements, the conductors that interconnect them, and the element leads.

At this point, we loosely consider a circuit to be any collection of elements and conductors, although we will sharpen our definition a bit later. Axiom 1 means that we can run tests on an element in the laboratory, then wire it into a circuit and have the assurance that it will not exhibit any new and different behavior. Axiom 2 means that it is only the *topology* of a circuit that matters, not the way the circuit is stretched or bent or rearranged, so long as we do not change the listing of which element leads are connected to which others or to which conductors.

The remaining two axioms are somewhat more involved and require some discussion of circuit topology. Consider, for a moment, the collection of elements in Figure 2.6. We labeled each element with a letter to distinguish it from the others. First, notice the two solid dots. We refer to them as **joints**. The idea is that they represent "solder joints," where the ends of two or more leads or conductors were connected. If only two ends are connected we do not show the joints explicitly; where three or more are connected, however, they are drawn. We temporarily (as a test) erase all of the element bodies and replace them with open space. The result is given in Figure 2.7. We refer to each of the interconnected "islands" of a conductor as a **node**. This example circuit has six nodes, and we labeled them with the numbers one through six for identification purposes.

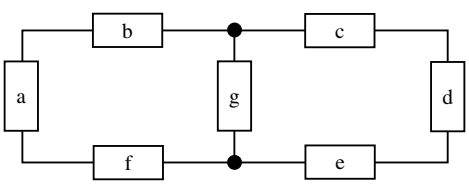

FIGURE 2.6 An example circuit.

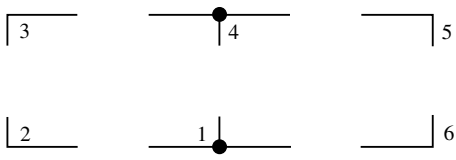

FIGURE 2.7 The nodes of the example circuit.

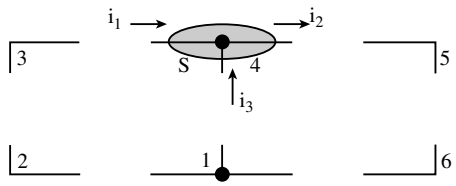

FIGURE 2.8 Illustration of Kirchhoff's current law.

Axiom 3 (Kirchhoff's Current Law): The charge on a node or in an element is identically zero at all instants of time.

Kirchhoff's current law (KCL) is not usually phrased in quite this manner. Thus, let us consider the closed (or "Gaussian") surface S in Figure 2.8. We assume that it is penetrated only by conductors. The elements, of course, are there; we simply do not show them so that we can concentrate on the conductors. We have arbitrarily defined the currents in the conductors penetrating *S*. Now, recalling that charge is the time integral of the current and thus has the same direction as the current from which it is derived, one can phrase Axiom 3 as follows:

$$\sum_s q_{\text{in}} = q_{\text{enclosed}} = 0 \tag{2.1}$$

at each instant of time. This equation is simply one form of conservation of charge. Because current is the time derivative of voltage, one can also state that

$$\sum_s i_{\text{in}} = 0 \tag{2.2}$$

at each and every time instant. This last equation is the usual phrasing of KCL. The subscript "in" means that a current reference pointed inward is to be considered positive; by default, therefore, a current with its reference pointed outward is to have a negative sign affixed. This sign is in addition to any negative sign that might be present in the value of each variable. For node 4 in Figure 2.8, KCL in its current form, therefore, reads

$$i_1 - i_2 + i_3 = 0 \tag{2.3}$$

Two other ways of expressing KCL (in current form) are

$$\sum_s i_{\text{out}} = 0 \tag{2.4}$$

and

$$\sum_s i_{\text{in}} = \sum_s i_{\text{out}} \tag{2.5}$$

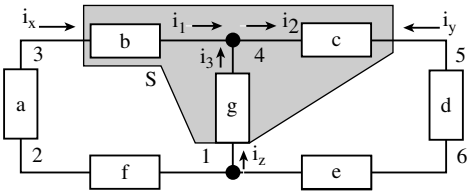

FIGURE 2.9 KCL for a more general surface.

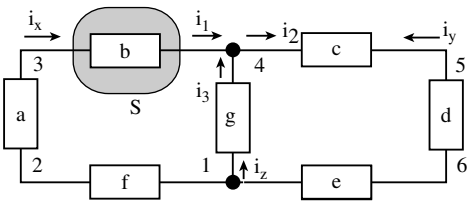

FIGURE 2.10 KCL for a single element.

The equivalent charge forms are also clearly valid. We emphasize the latter to a greater extent than is usual in the classical treatment because of the current interest in charge distribution and transfer circuits.

The Gaussian surface used to express KCL is not constrained to enclose only conductors. It can enclose elements as well, although it still can be penetrated by only conductors (which can be element leads). Thus, consider Figure 2.9, which illustrates the same circuit with which we have been working. Now, however, the elements are given and the Gaussian surface encloses three elements, as well as conductors carrying the currents previously defined. Because these currents are not carried in the conductors penetrating the surface under consideration, they do not enter into KCL for that surface. Instead, KCL becomes

$$i_x + i_y + i_z = 0 \tag{2.6}$$

As a special case let us look once more at the preceding figure, but use a different surface, one enclosing only the element *b*. This is depicted in Figure 2.10. If we refer to Axiom 3, which notes that charge cannot accumulate inside an element, and apply charge conservation, we find that

$$i_x = i_1 \tag{2.7}$$

This states that the current into any element in one of its leads is the same as the current leaving in the other lead. In addition, we see that KCL for nodes and KCL for elements (both of which are implied by Axiom 3) imply that KCL holds for any general closed surface penetrated only by conductors such as the one used in connection with Figure 2.9.

In order to phrase our last axiom, we must discuss circuit topology a bit more, and we will continue to use the circuit just considered previously. We define a **path** to be an ordered sequence of elements having the property that any two consecutive elements in the sequence share a common node. Thus, referring for convenience back to Figure 2.10, we see that {*f, a, b*} is a path. The elements *f* and *a* share node 2 and *a* and *b* share node 3. One lead of the last element in a path is connected to a node that is not shared with the preceding element. Such a node is called the **terminal** node of the path. Similarly, one lead of the first element in the sequence is connected to a node that is not shared with the preceding element.[1] It is called the *initial* node of the path. Thus, in the example just cited, node 1 is the initial node and node 4 is the final node. Thus, a direction is associated with a path, and we can indicate it diagram-

[1]We assume that no element has its two leads connected together and that more than two elements are in the path in this definition.

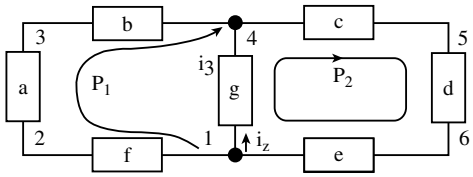

FIGURE 2.11 Circuit paths.

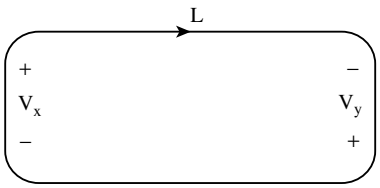

FIGURE 2.12 Voltage rise and drop.

matically by means of an arrow on the circuit. This is illustrated in Figure 2.11 for the path $P_1 = \{f, a, b\}$ and $P_2 = \{g, c, d, e\}$.

If the initial node is identical to the terminal node, then the corresponding path is called a *loop*. An example is $\{f, a, b, g\}$. The patch P_2 is a loop. An alternate definition of a loop is as a collection of branches having the property that each node connected to a patch branch is connected to precisely two path branches; that is, it has **degree two** relative to the path branches.

We can define the voltage across each element in our circuit in exactly two ways, corresponding to the choices of which lead is designated plus and which is designated minus. Figure 2.12 presents two voltages and a loop L in a highly stylized manner. We have purposely not drawn the circuit itself so that we can concentrate on the essentials in our discussion. If the path enters the given element on the lead carrying the minus and exits on the one carrying the positive, its voltage will be called a **voltage rise**; however, if it enters on the positive and exits on the minus, the voltage will be called a **voltage drop**. If the signs of a voltage are reversed and a negative sign is affixed to the voltage variable, the value of that variable remains unchanged; thus, note that a negative rise is a drop, and vice versa.

We are now in a position to state our fourth and final axiom:

Axiom 4 (Kirchhoff's Voltage Law): The sum of the voltage rises around any loop is identically zero at all instants of time.

We refer to this law as KVL for the sake of economy of space. Just as KCL was phrased in terms of charge, KVL could just as well be phrased in terms of **flux linkage**. Flux linkage is the time integral of voltage, so it can be said that the sum of the flux linkages around a loop is zero. In voltage form, we write

$$\sum_{\text{loop}} v_{\text{rises}} = 0 \tag{2.8}$$

We observed that a negative rise is a drop, so

$$\sum_{\text{loop}} v_{\text{drops}} = 0 \tag{2.9}$$

or

$$\sum_{\text{loop}} v_{\text{rises}} = \sum_{\text{loop}} v_{\text{drops}} \tag{2.10}$$

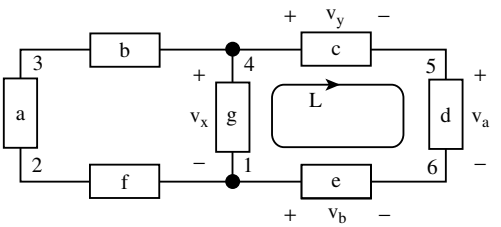

FIGURE 2.13 Illustration of Kirchhoff's voltage law.

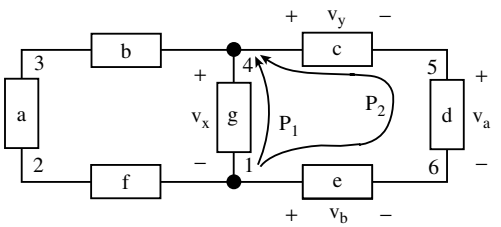

FIGURE 2.14 Path form of KVL.

Thus, in Figure 2.13, we could write [should we choose to use the form of (2.8)]

$$v_x - v_y - v_a + v_b = 0 \tag{2.11}$$

Clearly, one can rearrange KVL into many different algebraic forms that are equivalent to those just stated; one form, however, is more useful in circuit computations than many others. It is known as the **path form** of KVL. To better appreciate this form, review Figure 2.13. This time, however, the paths are defined a bit differently. As illustrated in Figure 2.14, we consider two paths, P_1 and P_2, having the same initial and terminal nodes, 1 and 4, respectively.[2] We can rearrange (2.11) into the form

$$v_x = -v_b + v_a + v_y \tag{2.12}$$

This form is often useful for finding one unknown voltage in terms of known voltages along some given path. In general, if P_1 and P_2 are two paths having the same initial and final nodes,

$$\sum_{P_1} v_{\text{rises}} = \sum_{P_2} v_{\text{rises}} = 0 \tag{2.13}$$

Be careful to distinguish this equation from (2.10). In the present case two paths are involved; in the former we find only a single loop, and drops are located on one side of the equation and rises on the other. One might call the path form the "all roads lead to Rome" form.

We covered four basic axioms, and these are all that are needed to construct a mathematical theory of circuit analysis. The first axiom is often referred to by means of the phrase "lumped circuit analysis", for we assume that all the physics of a given element are internal to that element and are of no concern to us; we are only interested in the *v–i* characteristic. That is, we are treating all the elements as lumps of matter that interact with the other elements in a circuit by means of the voltage and current at their leads. The second axiom says that the physical construction is irrelevant and that the interconnections are completely described by means of the circuit graph. Kirchhoff's current law is an expression of conservation of charge, plus the assumption that neither conductors nor elements can maintain a net

[2]If one defines the **negative** of a path as a listing of the same elements as the original path in the reverse order and summation of two paths as a concatenation of the two listings, one sees that $P_1 - P_2 = L$, the loop in Figure 2.13.

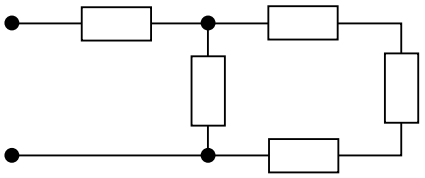

FIGURE 2.15 A "noncircuit."

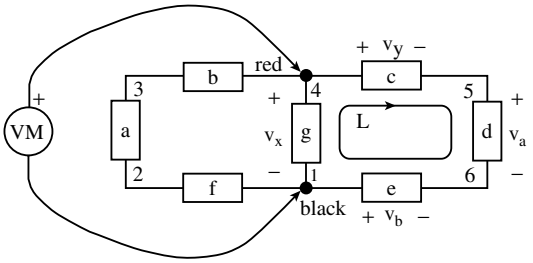

FIGURE 2.16 Node voltages.

charge. In this connection, observe that a capacitor maintains a charge separation internally, but it is a separation of two charges of opposite sign; thus, the total algebraic charge within it is zero. Finally, KVL is an expression of conservation of flux linkage. If $\mathrm{l}(t) = \int_{-\infty}^{t} v(\alpha)d\alpha$ is the flux linkage, then one can write[3] (using one form of KVL)

$$\sum_{\text{loop}} \lambda_{\text{rises}}^{(t)} = 0 \tag{2.14}$$

In the theory of electromagnetics, one finds that this equation does not hold exactly; in fact, the right-hand side is equal to the negative of the derivative of the magnetic flux contained within the loop (this is the Faraday–Lenz law). If, however, the time variation of all signals in the circuit are slow, then the right-hand side is approximately zero and KVL can be assumed to hold. A similar result holds also for KCL. For extremely short instants of time, a conductor can support an unbalanced charge. One finds, however, that the "relaxation" time of such unbalanced charge is quite short in comparison with the time variations of interest in the circuits considered in this text.

Finally, we tie up a loose end left hanging at the beginning of this subsection. We consider a circuit to be, not just any collection of elements that are interconnected, but a collection having the property that each element is contained in at least one loop. Thus, the circuit in Figure 2.15 is not a circuit; instead, it must be treated as a *subcircuit*, that is, as part of a larger circuit in which it is to be imbedded.

The remainder of this section develops the application of the axioms presented here to the analysis of circuits. The reader is referred to [2, 3, 4] for a more detailed treatment.

Nodal Analysis

Nodal analysis of electric circuits, although using all four of the fundamental axioms presented in the introduction, concentrates upon KCL explicitly. Kirchhoff's voltage law is also satisfied automatically in view of the way the basic equations are formulated. This effective method uses the concept of a **node voltage**. Figure 2.16 illustrates the concept. Observe a voltmeter, with its black probe attached to a single node, called the **reference node**, which remains fixed during the course of the investigation. In the case

[3]One might anticipate a constant on the right side of (2.14); however, a closer investigation reveals that it is more realistic and pragmatic to assume that all signals are one-sided and that all elements are causal. This implies that the constant is zero. Two-sided signals only arise legitimately within the context of steady-state behavior of stable circuits and systems.

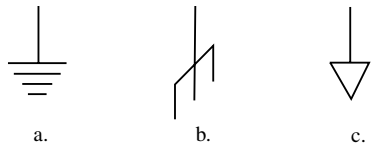

FIGURE 2.17 Reference node symbols.

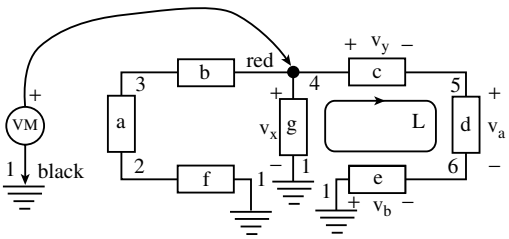

FIGURE 2.18 An alternate drawing.

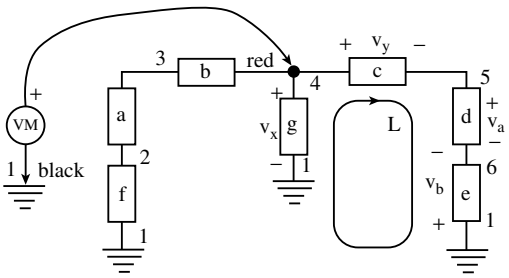

FIGURE 2.19 An equivalent drawing.

shown node 1 is the reference node. The red probe is shown being touched to node 4; therefore, we call the resulting voltage v_4. The subscript denotes the node and the result is always assumed to have its positive reference on the given node. In the present instance v_4 is identical to the element voltage because element g (across which v_g is defined) is connected between node 4 and the reference node. Note that the voltage of such an element is always either the node voltage or its negative, depending upon the reference polarities of its associated element voltage. If we were to touch the red probe to node 5, however, no element voltage would have this relationship to the resulting node voltage v_5 because no elements are connected directly between nodes 5 and 1.

The concept of reference node is used so often that a special symbol is used for it [see Figure 2.17(a)]; alternate symbols often seen on circuit diagrams are shown in the figure as well. Often one hears the terms "ground" or "ground reference" used. This is commonly accepted argot for the reference node; however, one should be aware that a safety issue is involved in the *process* of grounding a circuit or appliance. In such cases, sometimes one symbol specifically means "earth ground" and one or more other symbols are used for such things as "signal ground" or "floating ground", although the last term is something of an oxymoron. Here, we use the terms "reference" or "reference node." The reference symbol is quite often used to simplify the drawing of a circuit. The circuit in Figure 2.16, for instance, can be redrawn as in Figure 2.18; circuit operation will be unaffected. Note that all four of the reference symbols refer to a single node, node 1, although they are shown separated from one another. In fact, the circuit is not changed electrically if one bends the elements around and thereby separates the ground symbols even more, as we have done in Figure 2.19. Notice that the loop L shown in the original figure, Figure 2.16, remains a loop, as in Figures 2.18 and 2.19. Redrawing a circuit using ground reference symbols does not alter the circuit topology, the circuit graph.

Suppose the red probe were moved to node 5. As described previously, no element is directly connected between nodes 5 and 1; hence, node voltage v_5 is not an element voltage. However, the element voltages

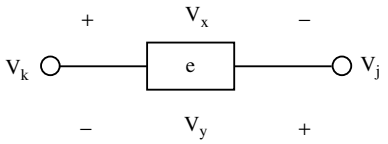

FIGURE 2.20 A floating element and its voltage.

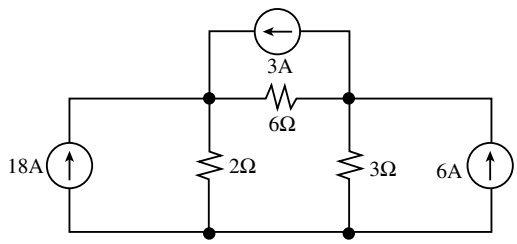

FIGURE 2.21 An example circuit.

and the node voltages are directly related in a one-to-one fashion. To see how, look at Figure 2.20. This figure shows a "floating element," *e*, which is connected between two nodes, *k* and *j*, neither of which is the reference node. It is vital here to remember that all node voltages are assumed to have their positive reference polarities on the nodes themselves and their negative reference on the reference node. Now, we can define the element voltage in either of two possible ways, as illustrated in the figure. Kirchhoff's voltage law (the simplest form perhaps being the path form) shows at once that

$$v_x = v_k - v_j \tag{2.15}$$

and

$$v_y = v_j - v_k \tag{2.16}$$

An easy mnemonic for this result is the following:

$$v_{\text{floatingelement}} = v_+ - v_- \tag{2.17}$$

where v_+ is the node voltage of the node to which the element lead associated with the positive reference for the element voltage is connected, and v_- is the node voltage of the node to which the lead carrying the negative reference for the element voltage is connected. We refer to an element that is not floating, by the way, as being "grounded."

It is easy to see that a circuit having N nodes has $N-1$ node voltages; further, if one uses (2.17), any element voltage can be expressed in terms of these $N-1$ node voltages. Then, for any invertible element,[4] one can determine the element current. The nodal analysis method uses this fact and considers the node voltages to be the unknown variables.

To illustrate the method, first consider a resistive circuit that contains only resistors and/or independent sources. Furthermore, we initially limit our investigation to circuits whose only independent sources (if any) are current sources. Such a circuit is depicted in Figure 2.21. Because nodal analysis relies upon the node voltages as unknowns, one must first select an arbitrary node for the reference. For circuits that contain voltage sources, one can achieve some simplification for hand analysis by choosing the reference wisely; however, if current sources are the only type of independent source present, one can choose it arbitrarily. As it happens, physical intuition is almost always better served if one chooses the bottom

[4]For instance, resistors, capacitors, and inductors are invertible in the sense that one can determine their element currents if their element voltages are known.

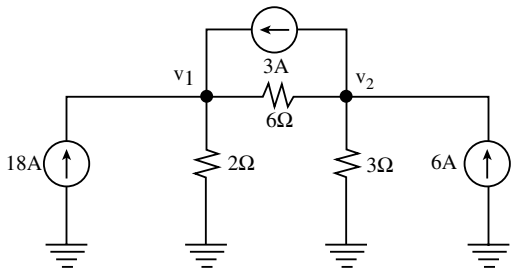

FIGURE 2.22 The example circuit prepared for nodal analysis.

node. Such is done here and the circuit is redrawn using reference symbols as in Figure 2.22. Here, we have arbitrarily assigned node voltages to the $N - 1 = 2$ nonreference nodes. In performing these two steps, we have "prepared the circuit for nodal analysis." The next step involves writing one KCL equation at each of the nonreference nodes. As it happens, the resulting equations are nice and compact if the form

$$\sum_{\text{node}} i_{\text{out}}\left(R's\right) = \sum_{\text{node}} i_{\text{in}}\left(I - \text{sources}\right) \tag{2.18}$$

is used. Here, we mean that the currents leaving a node through the resistors must sum up to be equal to the current being supplied to that node from current sources. Because these two types of elements are exhaustive for the circuits we are considering, this form is exactly equivalent to the other forms presented in the introduction. Furthermore, for a current leaving a node through a resistor, the floating element KVL result in (2.17) is used along with Ohm's law:

$$\sum_{j=1}^{N-1} \frac{v_k - v_j}{R_{kj}} = \sum_{q=1}^{M_k} i_{sq}\left(\text{node } k\right). \tag{2.19}$$

In this equation for node k, R_{kj} is the resistance between nodes k and j (or the equivalent resistance of the parallel combination if more than one are found), i_{sq} is the value of the qth current source connected to node k (positive if its reference is toward node k), and M_k is the number of such sources. Clearly, one can simply omit the $j = k$ term on the left side because $v_k - v_k = 0$.

The nodal equations for our example circuit are

$$\frac{v_1}{2} + \frac{v_1 - v_2}{6} = 18 + 3 \tag{2.20}$$

and

$$\frac{v_2 - v_1}{6} + \frac{v_2}{3} = 6 - 3 \tag{2.21}$$

Notice, by the way, that we are using units of A, Ω, and *V*. It is a simple matter to show that KVL, KCL, and Ohm's law remain invariant if we use the consistent units of mA, kΩ, and V. The latter is often a more practical system of units for filter design work. In the present case the matrix form of these equations is

$$\begin{bmatrix} \frac{2}{3} & -\frac{1}{6} \\ -\frac{1}{6} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} 21 \\ 3 \end{bmatrix} \tag{2.22}$$

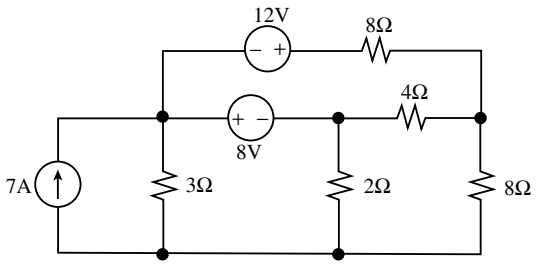

FIGURE 2.23 An example circuit.

It can be verified easily that the solution is $v_1 = 36$ V and $v_2 = 18$ V. To see that one can compute the value of any desired variable from these two voltages, consider the problem of determining the current i_6 (let us call it) through the horizontal 6 Ω resistor from right to left. One can simply use the equation

$$i_6 = \frac{v_2 - v_1}{6} = \frac{18 - 36}{6} = -3\text{A} \tag{2.23}$$

The previous procedure works for essentially all circuits encountered in practice. If the coefficient matrix on the left in (2.22) (which will always be symmetric for circuits of the type we are considering) is nonsingular, a solution is always possible. It is surprisingly difficult, however, to determine conditions on the circuit under which solutions do not exist, although this is discussed at greater length in a later subsection.

Suppose, now, that our circuit to be solved contains one or more independent voltage sources in addition to resistors and/or current sources. This constrains the node voltages because a given voltage source value must be equal to the difference between two node voltages if it is floating and to a node voltage or its negative if it is grounded. One might expect that this complicates matters, but fortunately the converse is true.

To explore this more fully, examine the example circuit in Figure 2.23. The algorithm just presented will not work as is because it relies upon balancing the current between resistors and current sources. Thus, it seems that we must account in some fashion for the currents in the voltage sources. In fact, we do not, as the following analysis shows. The key step in our reasoning is this: the analysis *procedure* should not depend upon the values of the independent circuit variables, that is, on the values of the currents in the current sources and voltages across the voltage sources. This is almost inherent in the definition of an independent source, for it can be adjusted to any value whatsoever. What we are assuming in addition to this is simply that we would not write one given set of equations for a specific set of source values, then change to another set of equations when these values are altered. Thus, let us test the circuit by temporarily deactivating all the independent sources (i.e., by making their values zero). Recalling that a deactivated voltage source is equivalent to a short circuit and a deactivated current source to an open circuit, we have the resulting configuration of Figure 2.24. The resulting nodes are shaded for convenience. Note carefully, however, that the nodes in the circuit under test are not the same as those in the original

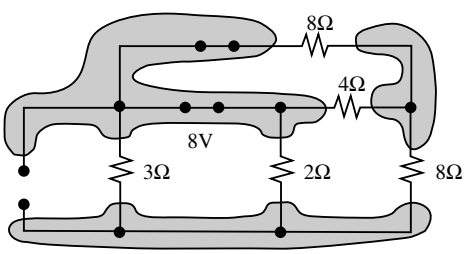

FIGURE 2.24 The example circuit deactivated.

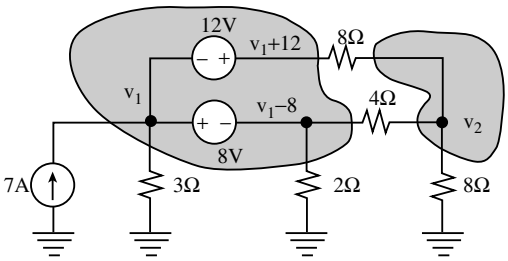

FIGURE 2.25 The example circuit prepared for nodal analysis.

circuit, although they are related. Notice that, for the circuit under test, all the resistor voltages would be determined by the node voltages as expected; however, *the number of nodes has been reduced by one for each voltage source*. Hence, we suspect that the required number of KCL equations N_{ne} (and the number of independent node voltages) is

$$N_{ne} = N - 1 - N_v \tag{2.24}$$

where N_v is the number of voltage sources. In the example circuit one can easily compute this required number to be 5 –1 –2 = 2. This is compatible with the fact that clearly three nodes (3 – 1 = 2 nonreference nodes) are clearly found in Figure 2.24.

It should also be rather clear that there is only one independent voltage within each of the shaded regions shown in Figure 2.24. We can use KVL to express any other in terms of that one. For example, in Figure 2.25 we have redrawn our example circuit with the bottom node arbitrarily chosen as the reference. We have also arbitrarily chosen a node voltage within the top left surface as the unknown v_1. Note how we have used KVL (the path form, again, is perhaps the most effective) to determine the node voltages of all the other nodes within the top left surface. Any set of connected conductors, leads, and voltage sources to which only one independent voltage can be assigned is called a **generalized node**. If that generalized node does not include the reference node, it is termed a **supernode**. The node within the shaded surface at the top left in Figure 2.25, however, has no voltage sources; hence, it is called an **essential node**.

As pointed out earlier, the equations that one writes should not depend upon the values of the independent sources. If one were to reduce all the independent sources to zero, each generalized node would reduce to a single node; hence, only one equation should be written for each supernode. One equation should be written for essential node also; it is unaffected by deactivation of the independent sources. Observe that deactivation of the current sources does not reduce the number of nodes in a circuit.

Writing one KCL equation for the supernode and one for the essential node in Figure 2.25 results in

$$\frac{v_1}{3} + \frac{v_1 - 8}{2} + \frac{v_1 - 8 - v_2}{4} + \frac{v_1 + 12 - v_2}{8} = 7 \tag{2.25}$$

and

$$\frac{v_2}{8} + \frac{v_2 - (v_1 - 8)}{4} + \frac{v_2 - (v_1 + 12)}{8} = 0 \tag{2.26}$$

In matrix form, one has

$$\begin{bmatrix} \frac{29}{24} & -\frac{3}{8} \\ -\frac{3}{8} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} \frac{23}{2} \\ -\frac{1}{2} \end{bmatrix} \tag{2.27}$$

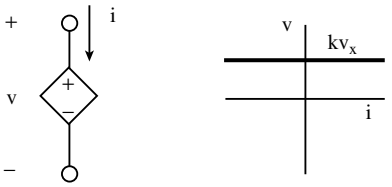

FIGURE 2.26 A dependent source.

The solution is $v_1 = 12$ V and $v_2 = 8$. Notice once again that the coefficient matrix on the left-hand side is symmetric. This actually follows from our earlier observation about this property for circuits containing only current sources and resistors because the voltage sources only introduce knowns into the nodal equations, thus modifying the right-hand side of (2.27).

The general form for nodal equations in any circuit containing only independent sources and resistors, based upon our foregoing development, is

$$A\bar{v}_n = F_v\bar{v}_s + F_I\bar{i}_s \tag{2.28}$$

where A is a symmetric square matrix of constant coefficients, F_v and F_I are rectangular matrices of constants, and $\bar{v}_n$ is the column matrix of independent mode voltages. The vectors $\bar{v}_s$ and $\bar{i}_s$ are column matrices of independent source values. Clearly, if A is a nonsingular matrix, (2.28) can be solved for the node voltages. Then, using KVL and/or Ohm's law, one can solve for any element current or voltage desired. Equally clearly, if a solution exists, it is a multilinear function of the independent source values.[5]

Now suppose that the circuit under consideration contains one or more dependent sources. Recall that the two-terminal characteristics of such elements are indistinguishable from those of the corresponding independent sources except for the fact that their value depends upon some other circuit variable. For instance, in Figure 2.26 a voltage-controlled voltage source (VCVS) is shown. Its v–i characteristic is identical to that of an independent source except for the fact that its voltage (the controlled variable) is a constant multiple[6] of another circuit variable (the controlling variable), in this case another voltage. This fact will be relied upon to develop a modification to the nodal analysis procedure.

We will adopt the following attitude: We will imagine that the dependent relationship, kv_x in Figure 2.26, is a label pasted to the surface of the source in much the same way that a battery is labeled with its voltage. We will imagine ourselves to take a small piece of opaque masking tape and apply it over this label; we will call this process **taping the dependent source**. This means that we are — temporarily — treating it as an independent source. The usual nodal analysis procedure is then followed, which results in (2.28). Then, we imagine ourselves to remove the tape from the dependent source(s) and note that the relationship is linear, with the controlling variables as the independent ones and the controlled variables the dependent ones. We next express the controlling variables — and thereby the controlled ones as well — in terms of the node voltages using KVL, KCL, and Ohm's law. The resulting relationships have the forms

$$\bar{v}_c = B'\bar{v}_n + C'\bar{y}_{si} + D'\bar{i}_{si} \tag{2.29}$$

and

$$\bar{i}_c = B''\bar{v}_n + C''\bar{v}_{si} + D''\bar{i}_{si} \tag{2.30}$$

Here, the subscript i refers to the fact that the corresponding sources are the independent ones. Noting that $\bar{v}_c$ and $\bar{i}_c$ appear on the right-hand side of (2.28) because they are source values, one can use the last two results to express the vectors of all source voltages and all source currents in that equation in the form

[5]That is, it is a linear function of the vector consisting of all of the independent source values.

[6]Thus, one should actually refer to such a device as a *linear* dependent source.

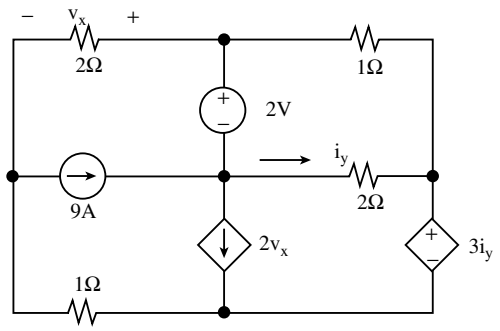

FIGURE 2.27 An example circuit.

$$\bar{v}_c = B'''\bar{v}_{si} + C'''\bar{i}_{si} + D'''\bar{v}_n \tag{2.31}$$

and

$$\bar{i}_c = B''''\,\bar{v}_{si} + C''''\,\bar{i}8_{si} + D''''\,\bar{v}_n \tag{2.32}$$

Finally, using the last two equations in (2.28), one has

$$A\bar{v}_n = F_v'\bar{v}_s + F_I'\bar{i}_s + B\bar{v}_n \tag{2.33}$$

Now,

$$(A - B)\bar{v}_n = F_v'\bar{v}_s + F_I'\bar{i}_s \tag{2.34}$$

This equation can be solved for the node voltages, provided that $A - B$ is nonsingular. This is even more problematic than for the case without dependent sources because the matrix B is a function of the gain coefficients of the dependent sources; for some set of such values the solution might exist and for others it might not. In any event if $A - B$ is nonsingular, one obtains once more a response that is linear with respect to the vector of independent source values.

Figure 2.27 shows a rather complex example circuit with dependent sources. As pointed out earlier, there are often reasons for preferring one reference node to another. Here, notice that if we choose one of the nodes to which a voltage source is attached it is not necessary to write a nodal equation for the nonreference node because, when the circuit is tested by deactivation of *all* the sources, the node disappears into the ground reference; thus, it is part of a generalized node including the reference called a **nonessential node**. For this circuit, choose the node at the bottom of the 2*V* independent source. The resulting circuit, prepared for nodal analysis, is shown in Figure 2.28. Surfaces have been drawn around both generalized nodes and the one essential node and they have been shaded for emphasis. Note that we have chosen one node voltage within the one supernode arbitrarily and have expressed the other node

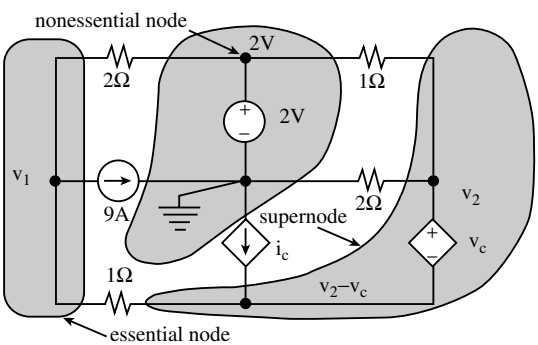

FIGURE 2.28 The example circuit prepared for nodal analysis.

voltage within that supernode in terms of the first and the voltage source value; furthermore, we have taped both dependent sources and written in the known value at the one nonessential node.

The nodal equations for the supernode and for the essential node are

$$\frac{v_1 - 2}{2} + \frac{v_1 - (v_2 - v_c)}{1} = -9 \quad \text{(essential node)} \tag{2.35}$$

and

$$\frac{v_2}{2} + \frac{v_2 - 2}{1} + \frac{v_2 - v_c - v_1}{1} = i_c \quad \text{(supernode)} \tag{2.36}$$

Now, the two dependent sources are untaped and their values expressed in terms of the unknown node voltages and known values using KVL, KCL, and Ohm's law. This results in (referring to the original circuit for the definitions)

$$v_c = -\frac{3}{2} v_2 \tag{2.37}$$

and

$$i_c = 4 - 2v_2 \cdot \tag{2.38}$$

Solving these four equations simultaneously gives $v_1 = -2$ V and $v_2 = 2$ V.

If the circuit under consideration contains op amps, one can first replace each op amp by a VCVS, using the above procedure, and then allow the voltage gain to go to infinity. This is a bit unwieldy, so one often models the op amp in a different way as a circuit element called a **nullor**. This is explored in more detail elsewhere in the book and is not discussed here.

Thus far, this chapter has considered only nondynamic circuits whose independent sources were all constants (DC). If these independent sources are assumed to possess time-varying waveforms, no essential modification ensues. The only difference is that each node voltage, and hence each circuit variable, becomes a time-varying function. If the circuit considered contains capacitors and/or inductors, however, the nodal equations are no longer algebraic; they become differential equations. The method developed above remains applicable, however. We will now show why.

Capacitors and inductors have the *v–i* relationships given in Figure 2.29. The symbols p and $1/p$ are referred to as **operators**, **differential operators**, or **Heaviside operators**. The last term is in honor of Oliver Heaviside, who first used them in circuit analysis. They are defined by

$$p = \frac{d}{dt} \tag{2.39}$$

$$\frac{1}{p} = \int_{-\infty}^{t} (\,)\, da \tag{2.40}$$

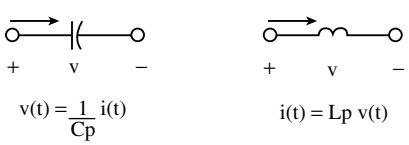

FIGURE 2.29 The dynamic element relationships.

The notation suggests that they are inverses of each other, and this is true; however, one must suitably restrict the signal space in order for this to hold. The most realistic assumption is that the signal space consists of all piecewise continuous functions whose derivatives of all orders exist except on a countable set of points that does not have any finite points of accumulation — *plus all generalized derivatives of such functions*. In fact, Laurent Schwartz, on the first page of the preface of his important work on the theory of distributions, acknowledges that this work was motivated by that of Heaviside. Thus, we will simply assume that all derivatives of all orders of any waveform under consideration exists in a generalized function sense. Higher order differentiation and integration operators are defined in power notation, as expected:

$$p^n = p \cdot p \cdots p = \frac{d^n}{dt^n} \tag{2.41}$$

and

$$\frac{1}{p^n} = \frac{1}{p} \cdot \frac{1}{p} \cdots \frac{1}{p} = \int_{-\infty}^{t} \int_{-\infty}^{b} \cdots \int_{-\infty}^{g} (\,)\, da \tag{2.42}$$

Another fact of the preceding issue often escapes notice, however. Look at any arbitrary function in the above-mentioned signal set, compute its running integral, and differentiate it. This action results in:

$$p\left[\frac{1}{p}x(t)\right] = \frac{d}{dt}\int_{-\infty}^{t} x(\alpha)d\alpha = x(t) \tag{2.43}$$

In fact, it is precisely this property that characterizes the set of all generalized functions. It is closed under differentiation. However, suppose the computation is done in the reverse order:

$$\frac{1}{p}\left[px(t)\right] = \int_{-\infty}^{t} x'(a)\,da = x(t) = x(t) - x(\infty) \tag{2.44}$$

We have assumed here that the Fundamental Theorem of Calculus holds. This is permissible within the framework of generalized functions, provided that the waveform $x(t)$ has a value in the conventional sense at time t. The problem with the previous result is that one does not regain $x(t)$. If it is assumed, however, that $x(t)$ is one sided (that is, $x(t)$ is identically zero for sufficiently large negative values of (t), $x(t)$ will be regained and p and $1/p$ will be inverses of one another. Thus, in the following, we will assume that all independent waveforms are one sided. We will, in fact, interpret this as meaning that they are all zero for $t < 0$. We will also assume that all circuit elements possess one property in addition to their defining *v–i* relationship, namely, that they are causal. Thus, all waveforms in any circuit under consideration will be zero for $t \leq 0$ and the previous two operators are inverses of one another. The only physically reasonable situation in which two-sided waveforms can occur is that of a stable circuit operating in the steady state, which we recognize as being an approximate mode of behavior derived from the previous considerations in the limit as time becomes large.

Referring to Figure 2.29 once more, we define

$$Z_c(p) = \frac{1}{Cp} \tag{2.45}$$

$$Z_L(p) = Lp \tag{2.46}$$

to be the **impedance operators** (or **operator impedances**) for the capacitor and the inductor, respectively. With our one-sidedness causality assumptions, we can manipulate these qualities just as we would manipulate algebraic functions of a real or complex variable.

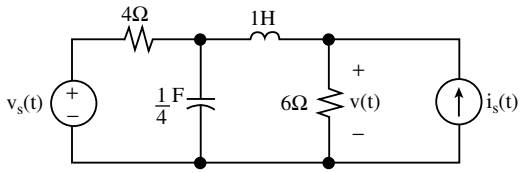

FIGURE 2.30 An example circuit.

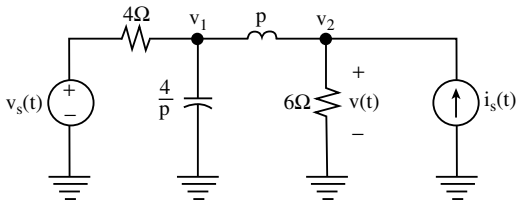

FIGURE 2.31 The example circuit prepared for nodal analysis.

The analysis of a dynamic circuit is illustrated by Figure 2.30. The circuit is shown prepared for nodal analysis, with the reference node at the bottom of the circuit and the dynamic elements expressed in terms of their impedance operators, in Figure 2.31. Note that if the circuit were to contain dependent sources, we would have taped them at this step. The nodal equations at the two essential nodes are

$$\frac{v_1 - v_2}{4} + \frac{v_1}{4/p} + \frac{v_1 - v_2}{p} = 0 \tag{2.47}$$

and

$$\frac{v_2}{6} + \frac{v_2 - v_1}{p} = i_s \tag{2.48}$$

In matrix form, merely rationalizing and collecting terms,

$$\begin{bmatrix} \frac{1}{4} + \frac{p}{4} + \frac{1}{p} & -\frac{1}{p} \\ -\frac{1}{p} & \frac{1}{6} + \frac{1}{p} \end{bmatrix} \begin{bmatrix} v_1(t) \\ v_2(t) \end{bmatrix} = \begin{bmatrix} \frac{1}{4} v_s(t) \\ i_s(t) \end{bmatrix} \tag{2.49}$$

Notice that the coefficient matrix is once again symmetric because no dependent sources exist. Multiplying the first row of each side by $4p$ and the second by $6p$, thus clearing fractions, one obtains

$$\begin{bmatrix} p^2 + p + 4 & -4 \\ -6 & p + 6 \end{bmatrix} \begin{bmatrix} v_1(t) \\ v_2(t) \end{bmatrix} = \begin{bmatrix} p v_s(t) \\ 6 p i_s(t) \end{bmatrix} \tag{2.50}$$

Now, multiply both sides by the inverse of the 2×2 coefficient matrix to get

$$\begin{bmatrix} v_1(t) \\ v_2(t) \end{bmatrix} = \frac{1}{p(p^2 + 7p + 10)} \begin{bmatrix} p + 6 & 4 \\ 6 & p^2 + p + 4 \end{bmatrix} \begin{bmatrix} p v_s(t) \\ 6 p i_s(t) \end{bmatrix} \tag{2.51}$$

Multiplying the two matrices on the right and cancelling the common p factor (legitimate under our assumptions), we finally have

$$v(t) = v_2(t) = \frac{6v_s(t) + 6\left(p^2 + p + 4\right)i_s(t)}{p^2 + 7p + 10} \tag{2.52}$$

We can, on the one hand, consider the result of our nodal analysis process to be a differential equation which we obtain by cross-multiplication:

$$\left[p^2 + 7p + 10\right]v(t) = 6v_s(t) + 6\left(p^2 + p + 4\right)i_s(t) \tag{2.53}$$

In conventional notation, using the distributive properties of the p operators, one has

$$\frac{d^2v(t)}{dt^2} + 7\frac{dv(t)}{dt} + 10v(t) = 6v_s(t) + 6\frac{d^2i_s(t)}{dt^2} + 6\frac{di_s(t)}{dt} + 24i_s(t). \tag{2.54}$$

On the other hand, it is possible to interpret (2.52) directly as a solution operator equation. We simply note that the denominator factors, then do a partial fraction expansion to get

$$\begin{aligned} v(t) &= \frac{6}{(p+2)(p+5)}v_s(t) + \frac{6\left(p^2 + p + 4\right)}{(p+2)(p+5)}i_s(t) \\ &= \frac{2}{p+2}v_s(t) - \frac{2}{p+2}v_s(t) + 6i_s(t) + \frac{2}{p+2}i_s(t) - \frac{8}{p+2}i_s(t). \end{aligned} \tag{2.55}$$

Thus, we have expressed the two second-order operators in terms of operators of order one. It is quite easy to show that the first-order operator has the following simple form:

$$\frac{1}{p+a}x(t) = e^{-at}\frac{1}{p}\left[e^{at}x(t)\right] \tag{2.56}$$

Using this result, one can quickly show that the impulse and step responses of the first-order operator are

$$h(t) = \frac{1}{p+a}\delta(t) = e^{-at}u(t) \tag{2.57}$$

and

$$s(t) = \frac{1}{p+a}u(t) = \left[1 - e^{-at}\right]u(t) \tag{2.58}$$

respectively. Thus, if $i_s(t) = \delta(t)$ and $v_s(t) = u(t)$, one has

$$v(t) = 6\delta(t) + \frac{1}{5}\left[3 + 5e^{-2t} - 38e^{-5t}\right]u(t) \tag{2.59}$$

References [5, 6] demonstrate that all the usual algebraic results valid for the Laplace transform are also valid for Heaviside operators.

Mesh Analysis

The central concept in nodal analysis is, of course, the node. The central idea in the method we will discuss here is the loop. Just as KCL formed the primary set of equations for nodal analysis, KVL will serve a similar function here. We will begin with the idea of a **mesh**. A mesh is a special kind of loop in

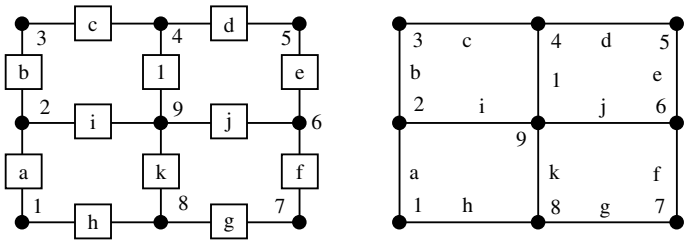

FIGURE 2.32 A circuit and its graph.

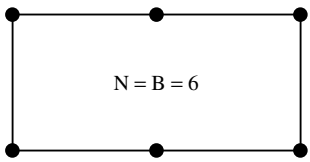

FIGURE 2.33 A one-mesh (series) circuit.

a planar circuit (one that can be drawn on a plane) a loop that does not contain any other loop inside it. If one reflects on this definition a bit, one will see that it depends upon how the circuit is drawn. Figure 2.32 illustrates the idea of a mesh. The nodes have been numbered and the elements labeled with letters for clarity. The circuit graph in Figure 2.32 abstracts all of the information about how the elements are connected, but does not show them explicitly. The lines represent the elements and the solid dots represent the nodes. If we apply the definition given in the introduction to this section, we can quickly verify that {*h, a, i, k*} is a loop. It is a simple loop because each of its elements share only one node with any of the other path elements. It is a mesh because no other loops are inside it.

It is an important fact that the number of meshes in a circuit is given by

$$N_m = B - N + 1 \tag{2.60}$$

where B is the number of branches (elements) and, as usual, N is the number of nodes. To see this, just look at the simple one-mesh graph in Figure 2.33. The number of branches is the same as the number of nodes for such a graph (or circuit). Imagine constructing the graph by placing an element on a planar surface, thereby forming two nodes with the one element. $B - N + 1 = 1 - 2 + 1 = 0$ in this case, and no meshes exist. Now, add another element by connecting one of its leads to one of the leads of the first element. Now, $B - N + 1 = 2 - 3 + 1 = 0$. This can be done indefinitely (or until you tire). At this point, connect one lead of the last element to the free lead of the one immediately preceding and the other lead of the last element to a node already placed. N nodes and $N - 1$ branches will have been put down, and exactly one mesh will have been formed. Thus, it is true that $B - N + 1 = N - (N - 1) + 1 = 1$ mesh and the formula is verified. Now connect a new element to one of the old nodes; the result is that one new element and one new node have been added. A glance at the formula verifies that it remains valid. Again, continue indefinitely, and then connect one new element and no new nodes by connecting the free lead of the last element with one of the nodes in the original one-loop circuit. Clearly, the number of added branches exceeds the number of added nodes by one; once again, the formula is verified. Figure 2.34 shows the new circuit. For the graph shown in the figure, $B = 13$ and $N = 12$, so $B - N + 1 = 2$, as expected. Induction generalizes the result, and (2.60) has been proved.

We now define a fictitious set of currents circulating around the meshes of a circuit. Figure 2.35 illustrates this idea with a circuit graph. All mesh currents are assumed to be circulating in a clockwise direction, although this is not necessary. We see that i_1 is the only current flowing in the branch in which the element current i_a is defined, therefore, $i_a = i_1$; similarly, i_3 is the only mesh current flowing in the element carrying element current i_b, but the two are defined in opposite directions. Thus, one sees that

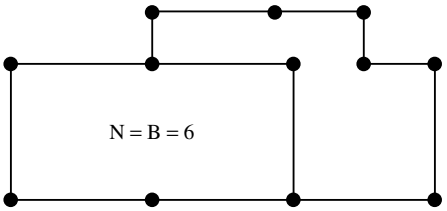

FIGURE 2.34 A two-mesh (series) circuit.

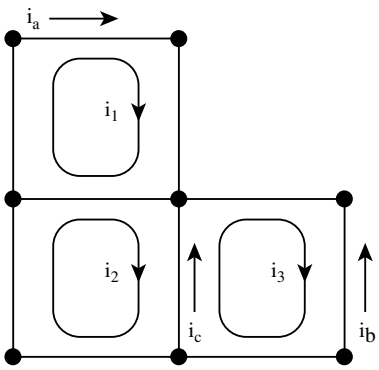

FIGURE 2.35 Mesh currents.

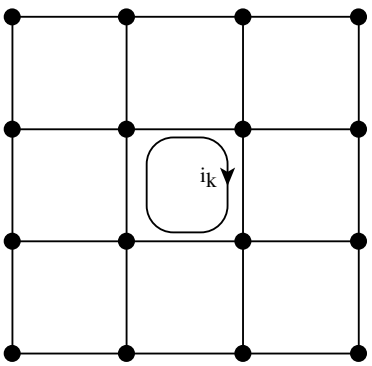

FIGURE 2.36 A fictitious mesh current.

$i_b = -i_3$. The third element where the current is indicated, however, is seen to carry two mesh currents in opposite directions. Hence, its element current is $i_c = i_3 - i_2$. In general, an element that is shared between two meshes has an element current which is the algebraic sum or difference[7] of the two adjacent mesh currents.

We used the term "fictitious" in our definition of mesh current. In the last example, however, we see that it is possible to make a physical measurement of each mesh current because each flows in an element that is not shared with any other mesh. Thus, one need only insert an ammeter in that element to measure the associated mesh current. Circuits exist, however, in which one or more mesh currents are impossible to measure. Figure 2.36 plots the graph of such a circuit. Each of the meshes is assumed to be carrying a mesh current, although only one has been drawn explicitly, i_k. As readily observed, each of the other mesh currents appears in a nonshared branch. For the mesh where the current is shown, however, it is impossible to find an element or a conductor carrying only that current. For this reason, i_k is merely a fiction, though a useful one.

[7]Always the difference if all mesh currents are defined in the same direction: clockwise or counterclockwise.

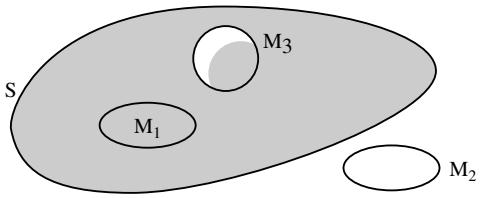

FIGURE 2.37 Illustration of KCL for mesh currents.

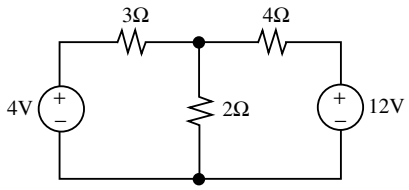

FIGURE 2.38 An example circuit.

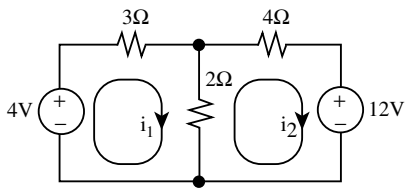

FIGURE 2.39 The example circuit prepared for mesh analysis.

It is easy to see that mesh currents automatically satisfy KCL because they form a complete loop. Observe the stylized picture in Figure 2.37, which shows three meshes represented for simplicity as small, closed ovals. M_1 lies entirely within the arbitrary closed surface S; thus, its current does not appear in KCL for that surface. M_2 lies entirely outside S, so the same thing is true for its current. Finally, we note that, regardless of the shape of S, M_3 penetrates it an even number of times. Thus, its current will appear in KCL for S an even number of times, and half of its appearances will carry a positive sign and half a negative sign. Thus, we have shown that any mesh current automatically satisfies KCL for any closed surface.

Because KCL is automatically satisfied, we must turn to KVL for the solution of a network in terms of its mesh currents. Figure 2.38 is an example circuit. Just as we assumed at the outset of the last subsection that any circuit under consideration contained only resistors and current sources, we will assume at first that any circuit under consideration contains only resistors and voltage sources. The one shown in Figure 2.38 has this property.

The first step is to identify the meshes and assign a mesh current to each. Identification of the meshes is easy, and this is the primary reason for its effectiveness in hand analysis of circuits. The mesh currents can be assigned in arbitrary directions, but for circuits of the sort considered here, it is more convenient to assign them all in the same direction, as in Figure 2.39. Writing one KVL equation for each mesh results in

$$3i_1 + 2(i_1 - i_2) = 4 \tag{2.61}$$

and

$$2(i_2 - i_1) + 4i_2 = -12 \tag{2.62}$$

In matrix form,

$$\begin{bmatrix} 5 & -2 \\ -2 & 6 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} 4 \\ -12 \end{bmatrix} \tag{2.63}$$

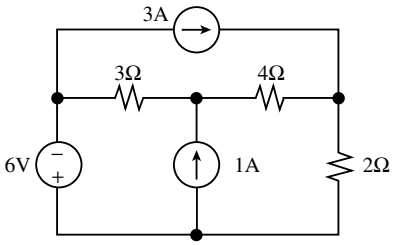

FIGURE 2.40 An example with current sources.

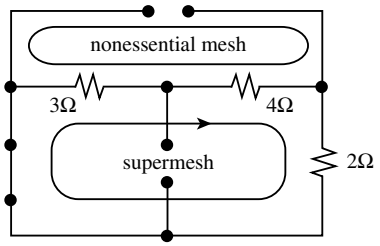

FIGURE 2.41 The deactivated current.

The solution is $i_1 = 0$ A and $i_2 = 2$ A. The same procedure holds for any planar circuit of an arbitrary number of meshes.

Suppose, now, that the circuit being considered has one or more current sources, such as the one in Figure 2.40. The meshes are readily determined; one need only to look for the "window panes", as meshes have been called. The only problem is this: When we write our mesh equations, what values do we use for the voltages across the current sources? These voltages are not known.

Thus, we could ascribe their voltages as unknowns, but this would lead to a hybrid form of analysis in which the unknowns are both element voltages and mesh currents; however, a more straightforward way is available. Consider this question: should the variables we use or the loops around which we decide to write KVL change if we alter the *values* of any of the independent sources? The answer, of course, is no. Thus, let us test the circuit by deactivating it-that is, by reducing all sources to zero. Recalling that a zero-valued voltage source is a short circuit and a zero-valued current source is an open circuit, we obtain the test circuit in Figure 2.41.

Notice what has happened. The two bottom meshes merge, thus forming one larger mesh in the deactivated circuit. The top mesh disappears (as a mesh or loop). For this reason, we refer to the former as a **supermesh** and the latter as a **nonessential mesh**. Observe also that it was the deactivation of the current sources that altered the topology; in fact, deactivation of the voltage sources has no effect on the mesh structure at all. Thus, we see that only one KVL equation is required to solve the deactivated circuit. (Reactivation of the source(s) is necessary, otherwise all voltage and currents will have zero values.) The conclusion relative to our example circuit is this: To solve the original circuit in terms of mesh currents, only one equation (KVL around the supermesh) is necessary.

The original circuit, with its three mesh currents arbitrarily defined, is redrawn in Figure 2.42. Notice that the isolated (nonshared) current source in the top (nonessential) mesh defines the associated mesh current as having the same value as the source itself. On the other hand, the 1 A current source shared by the bottom two meshes introduces a more general constraint: the difference between the two mesh currents must be the same as the source current. This constraint has been used to label the mesh current in the right-hand mesh with a value such that it, minus the left-hand mesh current, is equal to the source current. The nice feature of this approach is that one can clearly see which mesh currents are unknown and which are dependent upon the unknowns. Exactly one independent mesh current is always associated with a supermesh. Recalling our test circuit in Figure 2.41, we see that we need to write only one KVL equation around the supermesh. It is

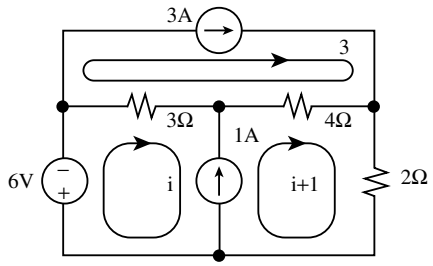

FIGURE 2.42 Assigning the mesh currents.

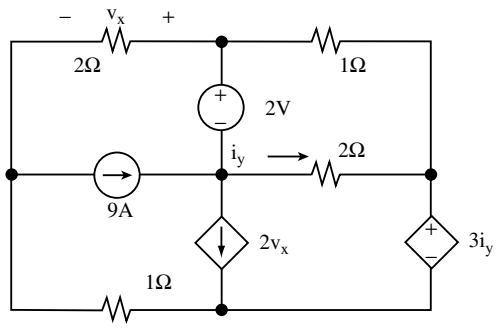

FIGURE 2.43 An example circuit.

$$3(i-3)+4(i+1-3)+2(i+1)=-6 \tag{2.64}$$

or

$$9i-9-8+2=-6 \tag{2.65}$$

The solution is $i = 1$ A. From this, one can compute the mesh current on the bottom right to be $i + 1 = 2$ A and the one in the top loop is already known to be 3 A. With these known mesh currents, we can solve for any circuit variable desired.

The development of mesh analysis seems at first glance to be the complete analog of nodal. This is not quite the case, however, because nodal will work for nonplanar circuits, while mesh works only for planar circuits; furthermore, no global reference exists for mesh currents as it does for node voltages.

Analyzing the problem, we observe that each current source, when deactivated, reduces the number of meshes by one. (A given element can be shared only by two meshes). Combining this fact with (2.60), we see that the required number of mesh equations is

$$N_{me} = B - N + 1 - N_I, \tag{2.66}$$

where, as usual, B is the number of branches, N is the number of nodes, and (in this equation) N_I is the number of current sources.

Note that mesh analysis is undertaken for circuits containing dependent sources in exactly the same manner as in nodal analysis — that is, by first taping the dependent sources, writing the mesh equations as above, and then untaping the dependent sources and expressing their controlled variables in terms of the unknown mesh currents. Figure 2.43 shows an example of such a circuit; in fact, it is the same figure investigated with nodal analysis in the preceding subsection.

The first step is to tape the dependent sources, thus placing them on the same footing as their more independent relatives. Then the circuit is tested for complexity by deactivating it as shown in Figure 2.44. All element labels have been removed merely to avoid obscuring the ideas being discussed. We see one supermesh, one essential mesh, and no nonessential mesh. Therefore, two KVL equations must be written in the original circuit, which is shown with the dependent sources taped in Figure 2.45. Notice that only

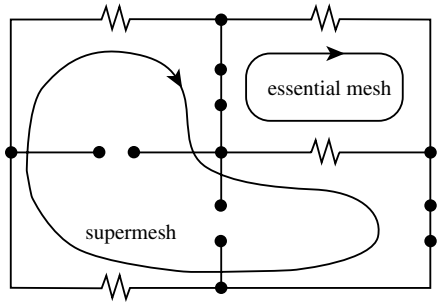

FIGURE 2.44 Testing the example circuit.

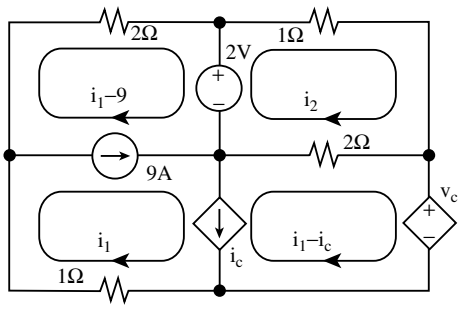

FIGURE 2.45 The example circuit prepared for mesh analysis.

two unknowns exist, and also that the dependent sources have been taped. For the moment, we have turned them into independent sources (albeit with unknown values).

We are now in a position to write KVL equations:

$$2(i_1 - 9) + 2(i_1 - i_c - i_2) + 1i_1 = -2 - v_c \qquad \text{(supermesh)} \tag{2.67}$$

and

$$1i_2 + 2(i_2 - i_1 + i_c) = 2 \qquad \text{(essential mesh)} \tag{2.68}$$

Observe that i_c and v_c are not known quantities, as would be the case were they the values of independent sources. Thus, at this point, we must untape the dependent sources and express their values in terms of the mesh currents. We find that

$$i_c = 2v_x = 2x2x(-i_1 + 9) = -4i_1 + 36 \tag{2.69}$$

and

$$v_c = 3i_y = 3(i_1 - i_c - i_2) = 15i_1 - 3i_2 + 36 \tag{2.70}$$

Inserting the last two results in (2.67) and (2.68) results in the matrix equation

$$\begin{bmatrix} 28 & -5 \\ -10 & 3 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} 196 \\ -70 \end{bmatrix} \tag{2.71}$$

The coefficient matrix is no longer symmetric now that dependent sources have been introduced. (This is also the case with nodal analysis. The example treating this same circuit is found in the last subsection and should be checked to verify this point.) However, the solution is found, as usual, to be $i_1 = 7$ A and $i_2 = 0$ A.

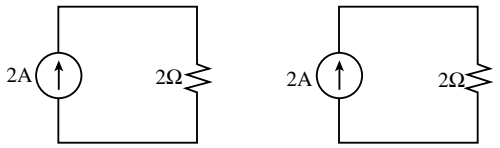

FIGURE 2.46 An example circuit.

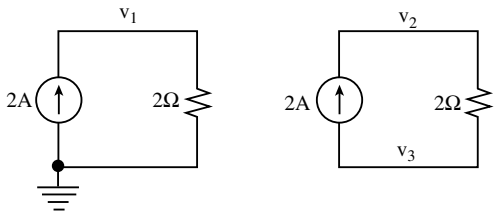

FIGURE 2.47 The example circuit prepared for nodal analysis.

A careful consideration of what we have done up to this point reveals that the mesh equations can be written in the form

$$A\bar{i}_M = B\bar{i}_s + C\bar{v}_s \tag{2.72}$$

In this general formulation, A is a square $n_M \times n_M$ matrix, where m is the number of meshes, and B and C are rectangular matrices whose dimensions depend upon the number of independent voltage and current sources, respectively. The variables $\bar{v}_s$ and $\bar{i}_s$ are the column matrices of independent voltage and current source values, respectively. A is symmetric if the circuit contains only resistors and independent sources. As was the case for nodal analysis, the elucidation of conditions under which the A matrix is nonsingular is difficult. Certainly, it can be singular for circuits with dependent sources; surprisingly, circuits also exist with only resistors and independent sources for which A is singular as well.

Finally, the mesh analysis procedure for circuits with dynamic elements should be clear. The algebraic process closely follows that for nodal analysis. For this reason, that topic is not discussed here.

Fundamental Cutset-Loop Circuit Analysis

As effective as nodal and mesh analysis are in treating circuits by hand, particular circuits exist for which they fail. Consider, for example, the circuit in Figure 2.46. If we were to blindly perform nodal analysis on this circuit, we would perhaps prepare it for analysis as shown in Figure 2.47. We have three nonreference nodes, hence, we have three nodal equations:

$$\frac{v_1}{2} = 2 \tag{2.73}$$

$$\frac{v_2 - v_3}{2} = 2 \tag{2.74}$$

$$\frac{v_3 - v_2}{2} = -2 \tag{2.75}$$

The third equation is simply the negative of the second; hence, the set of equations is linearly dependent and does not have a unique solution. The reason is quite obvious: the circuit is not connected.[8] It actually consists of two circuits considered as one. Therefore, one should actually select two reference nodes rather than one. A bit of reasoning along this line indicates that the number of nodal equations should be

[8]A circuit is connected if at least one path exists between each pair of nodes.

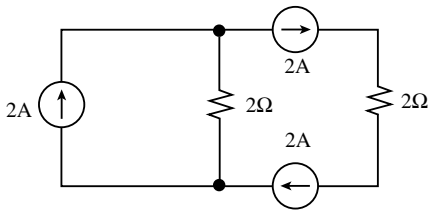

FIGURE 2.48 Another example circuit.

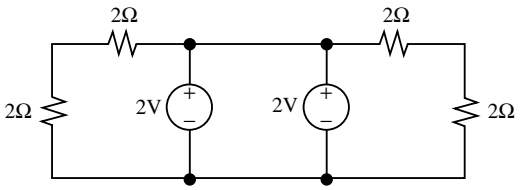

FIGURE 2.49 Another example of a singular circuit.

$$N_{ne} = N - 1 - P \tag{2.76}$$

where P is the number of separate parts, and hence the number of reference nodes required.

Another way nodal analysis can fail is not quite as obvious. Figure 2.48 illustrates the situation. In this case, we have a cutset of current sources. Therefore, in reality, at least one of the current sources cannot be independent for it must have the same value as the other in the cutset. We will leave the writing of the nodal equations as an exercise for the reader. They are, however, linearly dependent. The problem here clearly becomes evident if one deactivates the circuit, because the resulting test circuit is not connected.

Analogous problems can occur with mesh analysis, as the circuit in Figure 2.49 demonstrates. We find a loop of voltage sources and, when the circuit is deactivated, one mesh disappears. Again, it is left as an exercise for the reader to write the mesh equations and show that they are linearly independent (the coefficients of all currents in the KVL equation for the central mesh are zero).

One might question the practically of such circuits because clearly no one would design such networks to perform a useful function. In the computer automation of circuit analysis, however, dynamic elements are often modeled over a small time increment in terms of independent sources, and singular behavior can result. Furthermore, one would like to be able to include more general elements than R, L, C, and voltage and current sources. For such reasons, a general method that does not fail is desirable. We develop this method next. It is related to the modified nodal analysis technique that is described elsewhere in the book.

To develop this technique, we will examine the graph of a specific circuit: the one in Figure 2.50. Graph theory is covered elsewhere in the book, but salient points will be reviewed here [7, 8]. The graph, of course, is not concerned at all with the *v–i* characteristics of the elements themselves — only with how they are interconnected. The lines (or edges or branches) represent the elements and the dots represent the nodes. The arrows represent the assumed references for voltage and current, the positive voltage at the "upstream" end of the arrow and the current reference in the direction of the arrow. We also recall the definition of a tree: for a connected graph of N nodes, a **tree** is any subset of edges of the graph that connects all the nodes, but which contains no loops. Such a tree is shown by means of the darkened edges in the figure: *a, b,* and *c.* The complement of a tree is called a **cotree**. Thus, edges *d, e, f, g,* and *h* form a cotree in Figure 2.50. If a graph consists of separate parts (that is, it is not connected), then one calls a subset of edges that connects all N nodes, but forms no loops, a **forest**. The complement of a forest is a **coforest**. The analysis method presented here is applicable to either connected or nonconnected circuits. However, we will use the terms for a graph that is connected for ease of comprehension; one

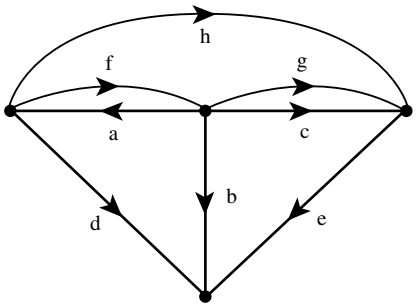

FIGURE 2.50 An example of a circuit graph.

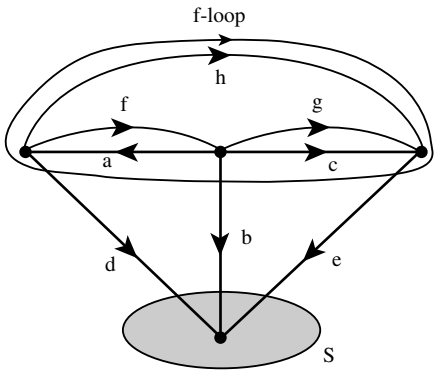

FIGURE 2.51 Fundamental cutsets and loops.

should go through a parallel development for nonconnected circuits to assure oneself that the generalization holds.

Each edge contained in a tree is called a **twig**, and each edge contained in a cotree is called a **link**. (Remember that the set of all nodes in a connected graph is split into exactly two sets of nodes, each of which is individually connected by twigs, when a tree edge is removed). The set of links having one of its nodes in one set and another in the second, together with the associated twig defining the two sets of nodes, is called a **fundamental cutset**, or ***f*-cutset**. If all links associated with a given tree are removed, then the links replaced one at a time, it can be seen that each link defines a loop called a **fundamental loop** or ***f*-loop**. Figure 2.51 is a fundamental cutset and a fundamental loop for the graph shown in Figure 2.50. The closed surface *S* is placed around one of the two sets of nodes so defined (in this case consisting of a single node) and is penetrated by the edges in the cutset *b*, *d*, and *e*. A natural orientation of the cutset is provided by the direction of the defining twig, in this case edge *b*. Thus, a positive sign is assigned to *b*; then, any link in the fundamental cutset with a direction relative to *S* agrees with that of the twig receives a positive sign, and each with a direction that is opposite receives a negative sign. Similarly, the fundamental loop is given a positive sense by the direction of the defining link, in the case edge *h*. It is assigned a positive sign; then, each twig in the *f*-loop is given a positive sign if its direction coincides in the loop with the defining link, and a negative sign if it does not.

The positive and negative signs just defined can be used to write one KCL equation for each *f*-cutset and one KVL equation for each *f*-loop, as follows. Consider the example graph with which we are working. The *f*-cutsets are $\{d, b, e\}$, $\{d, a, f, h\}$, and $\{e, c, g, h\}$. In general, $N - 1$ *f*-cutsets are associated with each tree — exactly the same as the number of twigs in the tree. Using surfaces similar to *S* in Figure 2.51 for each of the *f*-cutsets, we have the following set of KCL equations:

$$i_a - i_d - i_f - i_h = 0 \tag{2.77}$$

$$i_b + i_d + i_e = 0 \tag{2.78}$$

$$i_c - i_e + i_g + i_h = 0 \tag{2.79}$$

In matrix form, these equations become

$$\begin{bmatrix} 1 & 0 & 0 & -1 & 0 & -1 & 0 & -1 \\ 0 & 1 & 0 & 1 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & -1 & 0 & 1 & 1 \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \\ i_d \\ i_e \\ i_f \\ i_g \\ i_h \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 0 \end{bmatrix}. \tag{2.80}$$

The coefficient matrix consists of zeroes, and positive and negative ones. It is called the ***f*-cutset matrix**. Each row corresponds to the KCL equation for one of the *f*-cutsets, and has a zero entry for each edge not in that cutset, $a + 1$ for any edge in the cutset with the same orientation as the defining twig, and $a - 1$ for each edge in the cutset whose orientation is opposite to the defining twig, and $a - 1$ for each edge in the cutset whose orientation is opposite to the defining twig. One often labels the rows and columns,

$$Q = \begin{matrix} \\ a \\ b \\ c \end{matrix} \begin{bmatrix} a & b & c & d & e & f & g & h \\ 1 & 0 & 0 & -1 & 0 & -1 & 0 & -1 \\ 0 & 1 & 0 & 1 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & -1 & 0 & 1 & 1 \end{bmatrix}. \tag{2.81}$$

to emphasize the relation between the matrix and the graph. Thus, the first row corresponds to KCL for the *f*-cutset defined by twig *a*, the second to that defined by twig *b*, and the last to the cutset defined by twig *c*. The columns correspond to each of the edges in the graph, with the twigs occupying the first $N - 1$ columns in the same order as that in which they appear in the rows. Notice that a unit matrix of order $N - 1 \times N - 1$ is located in the leftmost $N - 1$ columns. Furthermore, Q has dimensions $(N - 1) \times B$, where B is the number of branches (edges). Clearly, Q has maximum rank because of the leading unit matrix. More succinctly, one writes KCL in terms of the *f*-cutset matrix as

$$Q\bar{i} = \left[U \vdots H\right]\bar{i} = 0, \tag{2.82}$$

where $\bar{i}$ is the column matrix of all the branch currents. Here, the structure of Q appears explicitly with the unit matrix in the first $N - 1$ columns and, for our example,

$$H = \begin{bmatrix} -1 & 0 & -1 & 0 & -1 \\ 1 & 1 & 0 & 0 & 0 \\ 0 & -1 & 0 & 1 & 1 \end{bmatrix} \tag{2.83}$$

In general, H will have dimensions $(N - 1) \times (b - N + 1)$.

Each of the links, all $B - N + 1$ of them, have an associated KVL equation. In our example, using the same order for these links and equations that occurs in the KCL equations,

$$\begin{bmatrix} 1 & -1 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & -1 & 1 & 0 & 1 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 & 0 & 1 & 0 \\ 1 & 0 & -1 & 0 & 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \\ v_d \\ v_e \\ v_f \\ v_g \\ v_h \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{2.84}$$

We have one row for each link and, therefore, one for each *f*-loop. If a given edge is in the given loop, $a + 1$ is in the corresponding column if its direction agrees with that of the defining link, and $a - 1$ if it disagrees. Notice that a unit matrix of dimensions $(B - N + 1) \times (B - N + 1)$ is located in the last $B - N + 1$ columns. Even more important, observe that the matrix in the first $N - 1$ columns has a familiar form; in fact, it is $-H'$, the negative transpose of the matrix in (2.83).

This is no accident. In fact, the entries in this matrix are strictly due to twigs in the tree. Focus on a given twig and a given link. The twig defines two twig-connected sets of nodes, as mentioned above. If the given link has both its terminal nodes in only one of these sets, the given twig voltage does not appear in the KVL equation for that *f*-loop. If, on the other hand, one of the link nodes is in one of those sets and the other in the alternate set, the given twig voltage will appear in the KVL equation for the given link, with $a + 1$ multiplier if the directions of the twig agree relative to the *f*-loop and $a - 1$ if they do not. However, a little thought shows that the same result holds for the *f*-cutset equation defined by the twig, except that the signs are reversed. If the link and twig directions agree for the *f*-loop, they disagree for the *f*-cutset, and vice versa. Thus, we can write KVL for the *f*-loops, in general, as

$$B_f \bar{v} = \left[-H' \vdots U\right] \bar{v} = 0 \tag{2.85}$$

B_f is called the fundamental loop matrix, and $\bar{v}$ is the column matrix of all branch voltages.

Suppose that we partition the branch voltages and branch currents according to whether they are associated with twigs or links. Thus, we write

$$\bar{v} = \left[\bar{v}_T' \; \bar{v}_C'\right]' \tag{2.86}$$

and

$$\bar{i} = \left[\bar{i}_T' \; \bar{i}_C'\right]'. \tag{2.87}$$

We use transpose notation to conserve space, and the subscripts *T* and *C* represent tree and cotree voltages and currents, respectively. We cannot use (2.82) and (2.85) to write the composite circuit variable vector as

$$\bar{u} = \begin{bmatrix} \bar{v} \\ \bar{i} \end{bmatrix} = \begin{bmatrix} U & 0 \\ H' & 0 \\ 0 & -H \\ 0 & U \end{bmatrix} \begin{bmatrix} \bar{v}_T \\ \bar{i}_C \end{bmatrix} \tag{2.88}$$

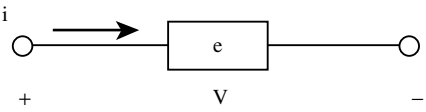

FIGURE 2.52 A two-terminal element.

The coefficient matrix is of dimensions $2B \times B$ and has rank B because of the two unit matrices. What we have accomplished is a direct sum decomposition of the $2B$-dimensional vector space consisting of all circuit variables in terms of the $N - 1$ dimensional vector space of tree voltages and the $B - N + 1$ dimensional vector space of link currents. Furthermore, the tree voltages and link currents form a basis for the vector space of all circuit variables.

We have discussed topology enough for our purposes. We now treat the elements. We are looking for a generalized method of circuit analysis that will succeed, not only for circuits containing *R, L, C,* and source elements, but ideal transformers, gyrators, nullators, and norators (among others) as well. Thus, we turn to a discussion of elements. [9].

Consider elements having two terminals only, as shown in Figure 2.52. The most general assumption we can make, assuming that we are ruling out "nonlinear" elements, is that the *v–i* characteristic of each such element be *affine;* that is, it is defined by an operator equation of the form

$$\begin{bmatrix} a & b \\ 0 & c \end{bmatrix} \begin{bmatrix} v \\ \bar{i} \end{bmatrix} = \begin{bmatrix} f(t) \\ g(t) \end{bmatrix} \tag{2.89}$$

where the parameters a, b, and c are operators. It is more classical to assume a scalar form of this equation; that is, with c and $g(t)$ both zero. In a series of papers in the 1960s, however, Carlin and Youla, Belevitch, and Tellegen [10–12] proposed that the *v–i* characteristic be interpreted as a multidimensional relationship. Among other things to come out of the approach was the definition of the nullator and the norator. Now, assuming that this defining characteristic is indeed multidimensional, we see at once that it is not necessary to consider operator matrices of a dimension larger than 2×2. There must be two columns because there are only two scalar terminal variables. If more than two rows were found, the additional equations would be either redundant or inconsistent, depending upon whether row reductions resulted in additional rows of all zeroes or in an inconsistent equation. Finally, the (2, 1) element in the operator matrix clearly can be chosen to be zero as shown, because otherwise it could be reduced to zero with elementary row operations. That is, one could, unless $a = 0$; but here, an exchange of rows produces the desired result shown. Note that any or all of *a, b,* and *c* can be the zero operator.

We pause here to remark that *a* and *b* can be rather general operators. If they are differential, or Heaviside, operators, (that is, they are real, rational functions of p), a theory of lumped circuits (differential systems) is obtained. On the other hand, they could be rational functions of the delay operator E.[9] In this case, one would obtain the theory of distributed (transmission line) circuits. Then, if a common delay parameter is used, one obtains a theory of commensurate transmission line circuits; if not, an incommensurate theory results. If the parameters are functions of both p and d, a mixed theory results. We will assume here that *a, b*, and *c* are rational functions of p.

Let us suppose that c is the zero operator and that $g(t) = 0$ is the second equality resulting from the stipulation of existence (consistency). This gives the affine scalar relationship

$$av + bi = f(t) \tag{2.90}$$

[9] $Ex(t) = x(t - T)$ for all t and all waveforms $x(t)$.

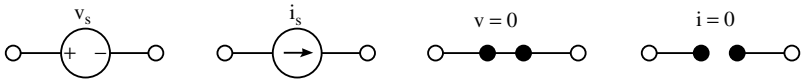

FIGURE 2.53 Conventional two-terminal elements.

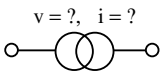

FIGURE 2.54 The norator.

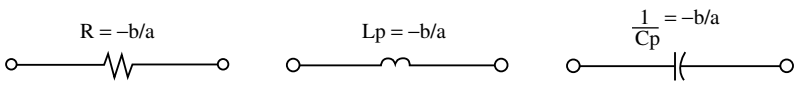

FIGURE 2.55 Passive elements.

Special cases are now examined. For instance, if $b = 0$ and $a \neq 0$, one has

$$v(t) = f(t)/a = v_s(t) \tag{2.91}$$

This, of course, is the *v–i* characteristic for an independent voltage source. If, on the other hand, $a = 0$ and $b \neq 0$, one has

$$i(t) = f(t)/b = i_s(t) \tag{2.92}$$

This is an ideal current source. If, in addition $f(t)$ is identically zero, one obtains a short circuit and an open circuit, respectively. These results are shown in Figure 2.53. Now suppose that a and b are both zero. Then, $f(t)$ must be identically zero as well; otherwise, the element does not exist. In this case any arbitrary voltage and current are possible. The resulting element, a "singular one" to be sure, is called a **norator**. Its symbol is shown in Figure 2.54.

Remaining with the same general case, that is, with $c = 0$ and $g(t) = 0$, we ask what element results if we also assume that neither a nor b are zero, but that $f(t)$ is identically zero. We can solve for either the voltage or the current. In either case, one obtains a passive element, as shown in Figure 2.55. If $-b/a$ is constant, a resistor will result; if $-b/a$ is a constant times the differential operator p, an inductor will result; and if $-b/a$ is reciprocal in p, a capacitor will result. In case the ratio is a more complicated function of p, one would consider the two-terminal object to be a subcircuit, that is, a two-terminal object decomposable into other elements, with $-b/a$ being the driving point impedance operator.

One can, in fact, derive the Thévenin and Norton equivalents from these considerations. Staying with the general case of c and g (t) both zero, but allowing $f(t)$ to be nonzero, we first assume that $a \neq 0$. Then, we obtain

$$v(t) = \frac{f(t)}{a} - \frac{b}{a} i(t) = v_{oc}(t) + Z_{eq}(p) i(t) \tag{2.93}$$

which represents the Thévenin equivalent subcircuit shown in Figure 2.56a. Alternately, if $b \neq 0$ we can write

$$i(t) = \frac{f(t)}{b} - \frac{a}{b} i(t) = i_{sc}(t) + Y_{eq}(p) v(t) \tag{2.94}$$

The latter equation is descriptive of the Norton equivalent shown in Figure 2.56b. The basic assumption is that the two-terminal object has a *v–i* characteristic (i.e., an affine relationship); if this object contains

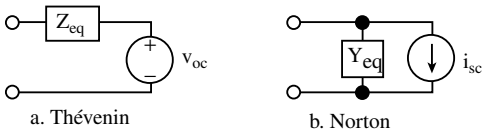

FIGURE 2.56 Two general equivalent subcircuits.

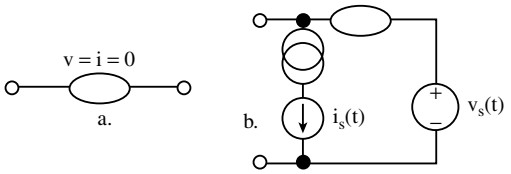

FIGURE 2.57 The nullator element and an equivalent subcircuit.

only elements characterized by affine relationships having a rank property to be given later, one can use the analysis method being presented here to prove that this assumption is true. At this point, however, we are merely assembling a catalog of elements, so we assume that the two-terminal object is, indeed, a single element (it cannot be decomposed farther).

We have only one other case to consider: that in which c is a nonzero operator. If this is the situation and if, in addition, a $\neq 0$ as well, one can solve (2.90) by inverting the coefficient matrix to obtain

$$\begin{bmatrix} v \\ i \end{bmatrix} = \begin{bmatrix} 1/c & -b/ac \\ 0 & 1/a \end{bmatrix} \begin{bmatrix} f(t) \\ g(t) \end{bmatrix} = \begin{bmatrix} v_s(t) \\ i_s(t) \end{bmatrix} \tag{2.95}$$

Therefore, the voltage and current are independently specified. First, suppose that both $v_s(t)$ and $i_s(t)$ are identically zero. Then, one has $v(t) = 0$ and $i(t) = 0$ for t. The associated element is called a **nullator**, and has the symbol shown in Figure 2.57(a). Finally, if $v_s(t)$ and $i_s(t)$ are nonzero, one can sketch the equivalent subcircuit as in Figure 2.57(b).

At this point, we have an exhaustive catalog of two-terminal circuit elements: the independent voltage and current sources, the resistor, the inductor, the capacitor, the norator, and the nullator. We would like to include more complex elements with more than two terminals as well. Figure 2.58(a) shows a three-terminal element and Figure 2.58(b) shows a two-port element. For the former, we see at once that only two voltages and two currents can be independently specified because KVL gives the voltage between the left and right terminals in terms of the two shown, while KCL gives the current in the third lead. As for the latter, it is a basic assumption that only the two-port voltages and the two-port currents are required to specify its operation. In fact, one assumes that the currents coming out of the bottom leads are identical to those going into the top leads. We also assume that the v–i characteristic is independent of the voltages between terminals in different ports. Each of the ports will be an edge in the circuit graph that results when such elements are interconnected.

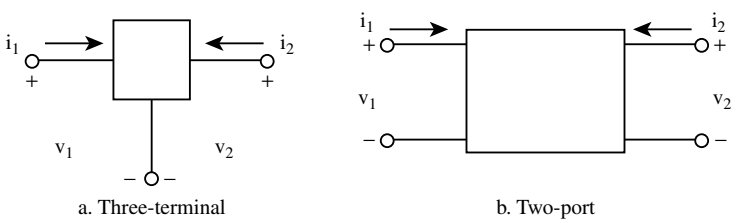

FIGURE 2.58 Three-terminal and two-port elements.

Because four variables are associated with a three-terminal or two-port element, the dimensionality of the resulting vector space is four; thus, we assume that the describing *v–i* characteristic is

$$\begin{bmatrix} a_{11} & a_{12} & a_{13} & a_{14} \\ 0 & a_{22} & a_{23} & a_{24} \\ 0 & 0 & a_{33} & a_{34} \\ 0 & 0 & 0 & a_{44} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} f_1(f) \\ f_2(f) \\ f_3(f) \\ f_4(f) \end{bmatrix} \tag{2.96}$$

We justify this form exactly as for the case of two-terminal elements. We will not exhaustively catalog all of the possible three-terminal/two-port elements for reasons of space; however, note that the usual case is that in which $a_{ij} = 0$ for $i \geq 3$. In this case one must insist that $f_3(t) = f_4(t) = 0$; then one has the 2×2 system of equations

$$\begin{bmatrix} a_{11} & a_{12} & a_{13} & a_{14} \\ 0 & a_{22} & a_{23} & a_{24} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} f_1(t) \\ f_2(t) \end{bmatrix} \tag{2.97}$$

If the two forcing functions on the right are not identically zero, a number of different two-port equivalent circuits can be generated — generalized Thévenin and Norton equivalents. If both of these forcing functions are identically zero and if at least one 2×2 submatrix of the coefficient operator matrix on the left side is nonsingular, one can derive a **hybrid matrix** and a **hybrid parameter equivalent circuit**. Specialized versions are the impedance parameters, the admittance parameters, and the transmission or chain parameters. Furthermore, one can accommodate controlled sources, transformers, gyrators, and all of the other known two-port elements.

To present just one example, assume that the operator (2.97) has the form

$$\begin{bmatrix} n & -1 & 0 & 0 \\ 0 & 0 & -1 & n \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \end{bmatrix} \tag{2.98}$$

The parameter n, assumed to be a real scalar multiplier, is called the **turns ratio**, and the element is the ideal transformer. The VCVS (voltage controlled voltage source) obeys

$$\begin{bmatrix} \mu & -1 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \end{bmatrix} \tag{2.99}$$

Thus, i_1 is identically zero and $v_2 = \mu v_1$. The quantity μ is the voltage gain.

Similarly, for each element with any number of ports,[10] we can write

[10]A two-terminal element is a one-port device.

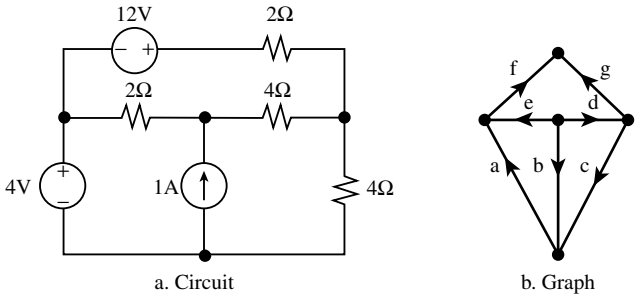

FIGURE 2.59 An example circuit and its graph.

$$A_0\bar{v} + B_0\bar{i} = \bar{C}_0 \tag{2.100}$$

where the voltage and current vectors are the terminal variables of the element. We can then represent the element equations for any circuit in the same form by forming A_0 and B_0 as quasidiagonal matrices, each of whose diagonal terms is the corresponding A_0 or B_0 for a given element, and stacking up the individual $\bar{C}_0$ column matrices to form the overall matrix. We then rewrite (2.100) in the form

$$\left[A_0 B_0\right]\begin{bmatrix}\bar{v}\\ \bar{i}\end{bmatrix} = \bar{C} \tag{2.101}$$

where the voltage and current vectors are each $B \times 1$ column matrices of the individual element voltages and currents. *We make the assumption that the matrix* $[A\ B]$, *which is of dimension* $B \times 2B$ *is of maximum rank b.* This is the only assumption required for the procedure to be outlined to succeed, as will later be demonstrated.

An example will clarify things. Figure 2.59 is an example circuit. The correspondence between the edge labels and the circuit elements is obvious; that is, for instance, *a* is the 4 V voltage source and its voltage is –4 V (minus, because of the definition of positive voltage on edge *a* in the graph). We have shown a tree on the graph. The *f*-cutset matrix is

$$Q = \begin{array}{c} \\ b \\ d \\ e \\ f \end{array}\begin{bmatrix} b & d & e & f & a & c & g \\ 1 & 0 & 0 & 0 & -1 & 1 & 0 \\ 0 & 1 & 0 & 0 & 0 & -1 & -1 \\ 0 & 0 & 1 & 0 & 1 & 0 & 1 \\ 0 & 0 & 0 & 1 & 0 & 0 & 1 \end{bmatrix} = \left[U \vdots H\right] \tag{2.102}$$

Thus,

$$H = \begin{bmatrix} -1 & 1 & 0 \\ 0 & -1 & -1 \\ 1 & 0 & 1 \\ 0 & 0 & 1 \end{bmatrix} \tag{2.103}$$

Although we could construct it from the *Q* matrix, we can just as easily read off the *f*-loop matrix from the graph:

$$B = \begin{matrix} a \\ c \\ g \end{matrix} \begin{bmatrix} b & d & e & f & a & c & g \\ 1 & 0 & -1 & 0 & 1 & 0 & 0 \\ -1 & 1 & 0 & 0 & 0 & 1 & 0 \\ 0 & 1 & -1 & -1 & 0 & 0 & 1 \end{bmatrix} = \left[-H' \vdots U\right] \tag{2.104}$$

The element constraint equations are

$$\begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & -4 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & -2 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & -4 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & -2 \end{bmatrix} \begin{bmatrix} v_b \\ v_d \\ v_e \\ v_f \\ v_a \\ v_c \\ v_g \\ i_b \\ i_d \\ i_e \\ i_f \\ i_a \\ i_c \\ i_g \end{bmatrix} = \begin{bmatrix} -1 \\ 0 \\ 0 \\ -12 \\ 4 \\ 0 \\ 0 \end{bmatrix} \tag{2.105}$$

In this case, both A_0 and B_0 are diagonal because all the elements are of the two-terminal variety.

The vector of all circuit variables is now expressed in terms of the basis in (2.88), the tree voltages and link currents. We then have

$$\left[AB\right] \begin{bmatrix} \bar{v} \\ \bar{i} \end{bmatrix} = \left[AB\right] \begin{bmatrix} U & 0 \\ H' & 0 \\ 0 & -H \\ 0 & U \end{bmatrix} \begin{bmatrix} \bar{v}_T \\ \bar{i}_C \end{bmatrix}$$

$$
= \begin{bmatrix}
0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & -4 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & -2 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & -4 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & -2
\end{bmatrix}
$$

$$
\times \begin{bmatrix}
1 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 1 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 1 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 1 & 0 & 0 & 0 \\
-1 & 0 & 1 & 0 & 0 & 0 & 0 \\
1 & -1 & 0 & 0 & 0 & 0 & 0 \\
0 & -1 & 1 & 1 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 1 & -1 & 0 \\
0 & 0 & 0 & 0 & 0 & 1 & 1 \\
0 & 0 & 0 & 0 & -1 & 0 & -1 \\
0 & 0 & 0 & 0 & 0 & 0 & 1 \\
0 & 0 & 0 & 0 & 1 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 1 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 1
\end{bmatrix}
\begin{bmatrix} v_b \\ v_d \\ v_e \\ v_f \\ v_a \\ i_c \\ i_g \end{bmatrix}
= \begin{bmatrix} -1 \\ 0 \\ 0 \\ -12 \\ 4 \\ 0 \\ 0 \end{bmatrix} \tag{2.106}
$$

After multiplying the two matrices, we have a more compact matrix

$$
\begin{bmatrix}
0 & 0 & 0 & 0 & 1 & -1 & 0 \\
0 & 1 & 0 & 0 & 0 & -4 & -4 \\
0 & 0 & 1 & 0 & 2 & 0 & 2 \\
0 & 0 & 0 & 1 & 0 & 0 & 0 \\
-1 & 0 & 1 & 0 & 0 & 0 & 0 \\
1 & -1 & 0 & 0 & 0 & -4 & 0 \\
0 & -1 & 1 & 1 & 0 & 0 & -2
\end{bmatrix}
\begin{bmatrix} v_b \\ v_d \\ v_e \\ v_f \\ i_a \\ i_c \\ i_g \end{bmatrix}
= \begin{bmatrix} -1 \\ 0 \\ 0 \\ -12 \\ 4 \\ 0 \\ 0 \end{bmatrix} \tag{2.107}
$$

We leave it to the reader to show that the solution is given by (in transpose notation):

$$\begin{bmatrix} v_b & v_d & v_e & v_f & i_a & i_c & i_g \end{bmatrix}' = \begin{bmatrix} 0 & -4 & 4 & -12 & 0 & 1 & -2 \end{bmatrix} \tag{2.108}$$

In general, one must solve the matrix equation

$$\begin{bmatrix} A\ B \end{bmatrix} = \begin{bmatrix} U & 0 \\ H' & 0 \\ 0 & -H \\ 0 & U \end{bmatrix} \begin{bmatrix} \bar{v}_T \\ \bar{i}_C \end{bmatrix} = C \tag{2.109}$$

where H is the nonunit submatrix in the f-cutset matrix and C_0 is the $B \times 1$ column matrix of constants (or independent functions of time). Here is the crucial result: $[A_0\ B_0]$ has dimensions $B \times 2B$; if it has rank B, then the product of it with the next matrix, which also has rank B, will be square (of dimensions $B \times B$) and of rank B by Sylvester's inequality [13]. In this case, the resulting coefficient matrix will be invertible, and a solution is possible.

The procedure just described, although involving more computation than, for example, nodal analysis, is general. If one solves for all element currents and voltages for a general circuit, however, one must anticipate additional complexity. Furthermore, the method outlined is algorithmic and can be computer automated. The element constraint matrices A_0 and B_0 consist of stylized submatrices corresponding to each type of element. These are referred to as **stamps** in the modified nodal technique described elsewhere in this volume, and the preceding method is quite similar. The major difference is that is uses node voltage as a basis for the branch voltage space of a circuit instead of the tree voltages described previously.

References

[1] P. W. Bridgman, *The Logic of Modern Physics,* New York: Macmillan, 1927.

[2] W.-K. Chen, *Linear Networks and Systems,* Monterey, CA: Brooks-Cole, 1983.

[3] J. Choma, *Electrical Networks: Theory and Analysis,* New York: Wiley, 1985.

[4] L. P. Huelsman, *Basic Circuit Theory,* Englewood Cliffs, NJ: Prentice Hall, 1927.

[5] A. M. Davis, "A unified theory of lumped circuits and differential system based on Heaviside operators and causality," *IEEE Trans. Circuits Syst.,* vol. 41, no. 11, pp. 712–727, November, 1990.

[6] A. M. Davis, *Linear Circuit Analysis*, text in preparation.

[7] W.-K. Chen, *Applied Graph Theory: Graphs and Electrical Networks,* New York: North-Holland, 1976.

[8] Chan, Shu-Park, *Introductory Topological Analysis of Electrical Networks,* New York: Holt, Rinehart, & Winston, 1969.

[9] A. M. Davis, unpublished notes.

[10] H. J. Carlin and D. C. Youla, "Network synthesis with negative resistors," *Proc. IEEE,* vol. 49, pp. 907–920, May 1961.

[11] V. Belevitch, "Four dimensional transformations of 4-pole matrices with applications to the synthesis of reactance 4-poles," *IRE Trans. Circuit Theory,* vol. CT-3, pp. 105–111, June 1956.

[12] B. D. H. Tellegen, "La Recherche pour une Serie Complete d'Elements de Circuit Ideaux Non-Lineaires," *Rendiconti Del Seminario Mathematico e Fisico di Milano,* vol. 25, pp. 134–144, April 1954.

[13] F. R. Gantmacher, *Theory of Matrices*, New York: Chelsea, 1959.

2.2 Network Theorems

Marwan A. Simaan

In Section 2.1, we learned how to determine currents and voltages in a resistive circuit. Methods have been developed, which are based on applying Kirchhoff's voltage law (KVL) and current law (KCL), to derive a set of mesh or node equations which, when solved, will yield mesh currents or node voltages, respectively. Frequently, and especially if the circuit is complex with many elements, the application of these methods may be considerably simplified if the circuit itself is simplified. For example, we may wish to replace a portion of the circuit consisting of resistors and sources by an equivalent circuit that has fewer elements in order to write fewer mesh or node equations.

In this context, we introduce three important and related theorems known as the **superposition**, the **Thévenin** and the **Norton theorems**. The superposition theorem shows how to solve for a variable in a circuit that has many independent sources, by solving simpler circuits, each excited by only one source. The Thévenin and Norton theorems can be used to replace a portion of a circuit at any two terminals by an equivalent circuit which consists of a voltage source in series with a resistor (i.e., a nonideal voltage source) or a current source in parallel with a resistor (i.e., a nonideal current source). Another important result derived in this section concerns the calculation of power dissipated in a load resistor connected to a circuit. This result is known as the **maximum power transfer theorem**, and is frequently used in circuit design problems. Finally, a result known as the **reciprocity theorem** is also discussed.

An important property of linear resistive circuits is the type of relationship that exists between any variable in the circuit and the independent sources. For linear resistive circuits the solution for a voltage or current variable can always be expressed as a *linear combination of the independent sources*. Let us elaborate on what we mean by this statement through an example.

Consider the circuit in Figure 2.60 and assume that we are interested in the voltage v across R_2. We can solve for v by first applying KCL at node a to get the equation

$$-\frac{v-v_1}{R_1}+\beta i_x+i_1-\frac{v}{R_2}=0 \tag{2.110}$$

and then by making use of the fact that

$$i_x=\frac{v_1-v}{R_1} \tag{2.111}$$

This gives

$$v=\frac{(1+\beta)R_2}{R_1+(1+\beta)R_2}v_1+\frac{R_1R_2}{R_1+(1+\beta)R_2}i_1 \tag{2.112}$$

Here, the voltage v is a linear combination of the independent sources v_1 and i_1.

The preceding observation indeed applies to every **linear circuit**. In general, if we let y denote a voltage across, or a current in, any element in a linear circuit and if we let $\{x_1, x_2, \ldots, x_N\}$ denote the independent voltage and current sources in that circuit (assuming there is a total of N such sources), then we can write

$$y=\sum_{k=1}^{N}a_kx_k \tag{2.113}$$

where $a_1, a_2, \ldots, a_N$ are constants which depend on the circuit parameters. Thus, in the circuit of Figure 2.60, every current or voltage variable can be expressed as a linear combination of the form

$$y = a_1V_1 + a_2 i_1$$

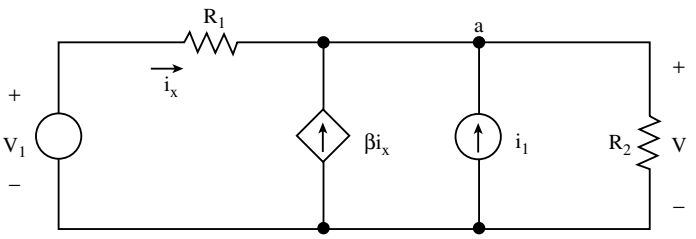

FIGURE 2.60 An example of a linear circuit.

where a_1 and a_2 are constants that depend on R_1, R_2, and β. For the voltage v across R_2, this relationship is given by expression (2.112).

Mathematically, the relationship between y and $\{x_1, x_2, \ldots, x_N\}$ expressed in (2.113) is said to be *linear* because it satisfies the following two conditions:

1. The *superposition condition,* which requires that:

$$\text{if} \qquad \hat{y} = \sum_{k=1}^{N} a_k \hat{x}_k$$

$$\text{and} \qquad \tilde{y} = \sum_{k=1}^{N} a_k \tilde{x}_k$$

$$\text{then} \qquad \hat{y} + \tilde{y} = \sum_{k=1}^{N} a_k \left(\hat{x}_k + \tilde{x}_k\right)$$

2. The *homogeneity condition,* which requires that:

$$\text{if} \qquad \hat{y} = \sum_{k=1}^{N} a_k \hat{x}_k$$

$$\text{then} \qquad c\hat{y}(t) = \sum_{k=1}^{N} a_k \{c\hat{x}_k\}$$

for any constant c.

The following example illustrates how these two conditions are satisfied for the circuit of Figure 2.60.

Example 2.1. For the circuit of Figure 2.60, let $R_1 = 2\ \Omega$, $R_2 = 1\ \Omega$, and $\beta = 2$. Show that the expression for v in terms of v_1 and i_1 satisfies the superposition and homogeneity conditions.

Substituting the values of R_1, R_2, and β in (2.112), the expression for v becomes

$$v = \frac{3}{5} v_1 + \frac{2}{5} i_1 \tag{2.114}$$

To check the superposition property, let $v_1 = \hat{v}_1$ and $i_1 = \hat{i}_1$. Then, the voltage $\hat{v}$ across R_2 is

$$\hat{v} = \frac{3}{5} \hat{v}_1 + \frac{2}{5} \hat{i}_1$$

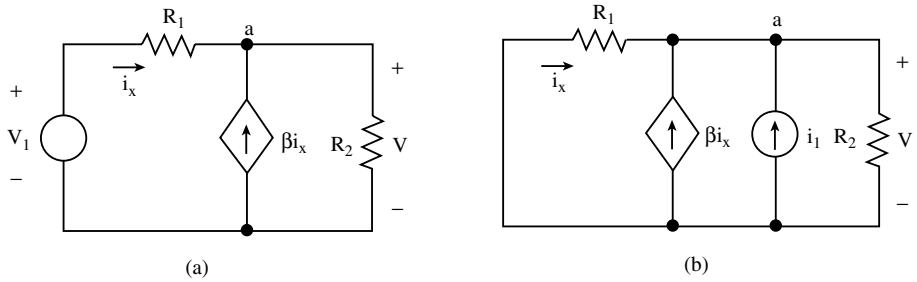

FIGURE 2.61 Circuit of Figure 2.60 with (a) the current source deactivated and with (b) the voltage source deactivated.

Similarly, let $V_1 = \tilde{V}_1$ and $i_1 = \tilde{i}_1$. Then, the voltage $\tilde{V}$ across R_2 is

$$\tilde{v} = \frac{3}{5}\tilde{v}_1 + \frac{2}{5}\tilde{i}_1$$

Now, assume that $V_1 = \hat{V}_1 + \tilde{V}_1$ and that $i_1 = \hat{i}_1 + \tilde{i}_1$. Then, according to (2.114) the corresponding voltage V across R_2 is

$$\begin{aligned} V &= \frac{3}{5}\left(\hat{V}_1 + \tilde{V}_1\right) + \frac{2}{5}\left(\hat{i}_1 + \tilde{i}_1\right) \\ &= \left(\frac{3}{5}\hat{V}_1 + \frac{2}{5}\hat{i}_1\right) + \left(\frac{3}{5}\tilde{V}_1 + \frac{2}{5}\tilde{i}_1\right) \\ &= \hat{V} + \tilde{V} \end{aligned}$$

Hence, the superposition condition is satisfied.

To check the homogeneity condition, let $V_1 = c\hat{V}_1$ and $i_1 = c\hat{i}_1$, where c is an arbitrary constant. Then, according to (2.114) the corresponding voltage v across R_2 is

$$\begin{aligned} V &= \frac{3}{5}\left(c\hat{V}_1\right) + \frac{2}{5}\left(c\hat{i}_1\right) \\ &= c\left(\frac{3}{5}\hat{V}_1 + \frac{3}{5}\hat{i}_1\right) \\ &= c\hat{V} \end{aligned}$$

The homogeneity condition is also satisfied.

The Superposition Theorem

Let us reexamine expression (2.112) for the voltage v in the circuit of Figure 2.60. To be more specific, let us use this expression to calculate the voltage across R_2 for the two circuits shown in Figures 2.61(a) and 2.61(b), respectively. Observe that the first circuit is obtained from the original circuit *by deactivating* the current source (i.e., setting $i_1 = 0$) and leaving the voltage source to act alone. The second is obtained by *deactivating* the voltage source (i.e., setting $V_1 = 0$) and leaving the current source to act alone. If we label the voltages across R_2 in these two circuits as v_a and v_b, respectively, then

$$v_a = v\Big|_{\substack{\text{when} \\ i_1=0}} = \frac{(1+\beta)R_2}{R_1 + (1+\beta)R_2}v_1$$

and

$$v_b = v\Big|_{\substack{\text{when}\\ v_1=0}} = \frac{R_1R_2}{R_1+(1+\beta)R_2}i_1$$

In other words, expression (2.112), which was used to derive the above two expressions, can itself be written as:

$$v = v\Big|_{\substack{\text{when}\\ i_1=0}} + v\Big|_{\substack{\text{when}\\ v_1=0}}$$

or

$$v = v_a + v_b$$

Thus, we conclude that the voltage across R_2 in Figure 2.60 is actually equal to the sum of two voltages across R_2 due to two independent sources in the circuit acting individually.

The preceding result is in fact a direct consequence of the linearity property

$$y = a_1x_1 + a_2x_2 + \ldots + a_Nx_N$$

expressed in (2.113). Note that, from this expression, we can write

$$a_1x_1 = y\Big|_{\text{when } x_1\neq 0, x_2=0, x_3=0,\ldots,x_N=0},$$

$$a_2x_2 = y\Big|_{\text{when } x_1=0, x_2\neq 0, x_3=0,\ldots,x_N=0},$$

$$\vdots \quad \vdots$$

$$a_Nx_N = y\Big|_{\text{when } x_1=0, x_2=0, x_3=0,\ldots,x_N\neq 0}$$

This means (2.113) can be rewritten as

$$y = y\Big|_{\text{when } x_1\neq 0, x_2=0, x_3=0,\ldots,x_N=0} + y\Big|_{\text{when } x_1=0, x_2\neq 0, x_3=0,\ldots,x_N=0} + \vdots + y\Big|_{\text{when } x_1=0, x_2=0, x_3=0,\ldots,x_N\neq 0}$$

The following theorem, known as the **superposition theorem**, is therefore directly implied from the previous expression:

> *The voltage across any element (or current through any element) in a linear circuit may be calculated by adding algebraically the individual voltages across that element (or currents through that element) due to each independent source acting alone with all other independent sources deactivated.*

In this statement, the word *deactivated* is used to imply that the source is set to zero. In this context, we refer to a **deactivated current source** as one that is replaced by an open circuit and a **deactivated**

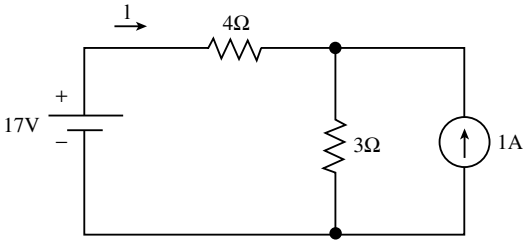

FIGURE 2.62 Circuit for Example 2.2.

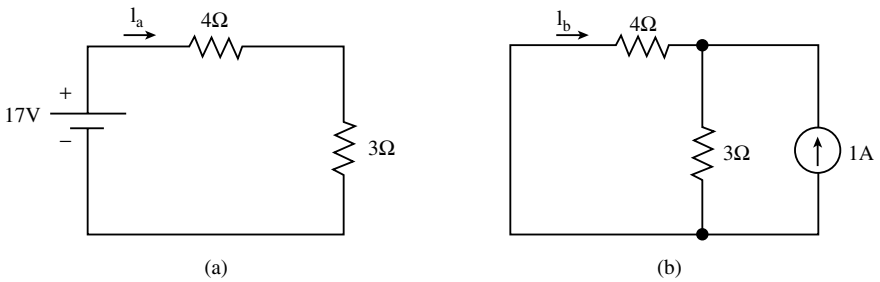

FIGURE 2.63 Circuit for Example 2.2 with (a) the current source deactivated and with (b) the voltage source deactivated.

voltage source as one that is replaced by a short circuit. Note that the action of deactivating a source refers only to independent sources. The following example illustrates how the superposition theorem can be used to solve for a variable in a circuit with more than one independent source.

Example 2.2. For the circuit shown in Figure 2.62, apply superposition to calculate the current I in the 4 Ω resistor.

Because we are interested in calculating I using the superposition theorem, we need to consider the two circuits shown in Figures 2.63(a) and (b). The first is obtained by deactivating the current source and the second is obtained by deactivating the voltage source. Let I_a be the current in the 4 Ω resistor in the first circuit and I_b be the current in the same resistor in the second. Then, by superposition

$$I = I_a + I_b$$

We can solve for I_a and I_b independently as follows. From Figure 2.63(a):

$$I_a = \frac{17}{7} A$$

and from Figure 2.63(b), applying the current divider rule,

$$I_b = -1 \cdot \frac{3}{7} A$$

Thus,

$$I = \frac{17}{7} - \frac{3}{7}$$

$$= 2A$$

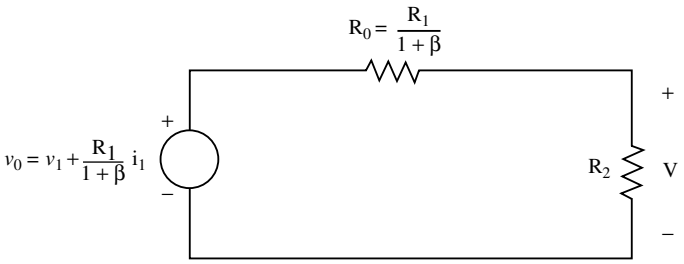

FIGURE 2.64 Voltage divider circuit representing (2.118).

The Thévenin Theorem

In the discussion on the superposition theorem, we interpreted (2.112) for the voltage V in the circuit of Figure 2.60 as a superposition of two terms. Let us now examine a different interpretation of this expression.

Suppose we factor the common term in expression (2.112), so that it can be written as

$$v = \frac{(1+\beta)R_2}{R_1+(1+\beta)R_2}\left\{v_1 + \frac{R_1}{1+\beta} i_1\right\} \tag{2.115a}$$

or

$$v = \frac{R_2}{\left(R_1/(1+\beta)\right)+R_2}\left\{v_1 + \left(\frac{R_1}{1+\beta}\right) i_1\right\} \tag{2.115b}$$

Now, suppose we define

$$v_0 = v_1 + \frac{R_1}{1+\beta} i_1 \tag{2.116}$$

and

$$R_0 = \frac{R_1}{1+\beta} \tag{2.117}$$

Then, we can write (2.112) in the simple form

$$v = \frac{R_2}{R_0+R_2} v_0 \tag{2.118}$$

This expression can be interpreted as a voltage divider equation for a two-resistor circuit as shown in Figure 2.64. This circuit has a voltage source v_0 in series with two resistors R_0 and R_2. When this circuit is compared with Figure 2.60, the combination of voltage source v_0 in series with R_0 can be interpreted as an equivalent replacement of all the elements in the circuit connected to R_2. That is, we could remove that portion of the circuit of Figure 2.60 consisting of v_1, R_1, βi_x, and i_1 and replace it with the voltage source v_0 in series with the resistor R_0.

The fact that a portion of a circuit can be replaced by an equivalent circuit consisting of a voltage source in series with a resistor is actually a direct result of the linearity property, and hence is true for linear circuits in general. It is known as **Thévenin's theorem**[11] and is stated as follows:

[11]For an interesting, brief discussion on the history of Thévenin's theorem, see an article by James E. Brittain, in *IEEE Spectrum,* p. 42, March 1990.

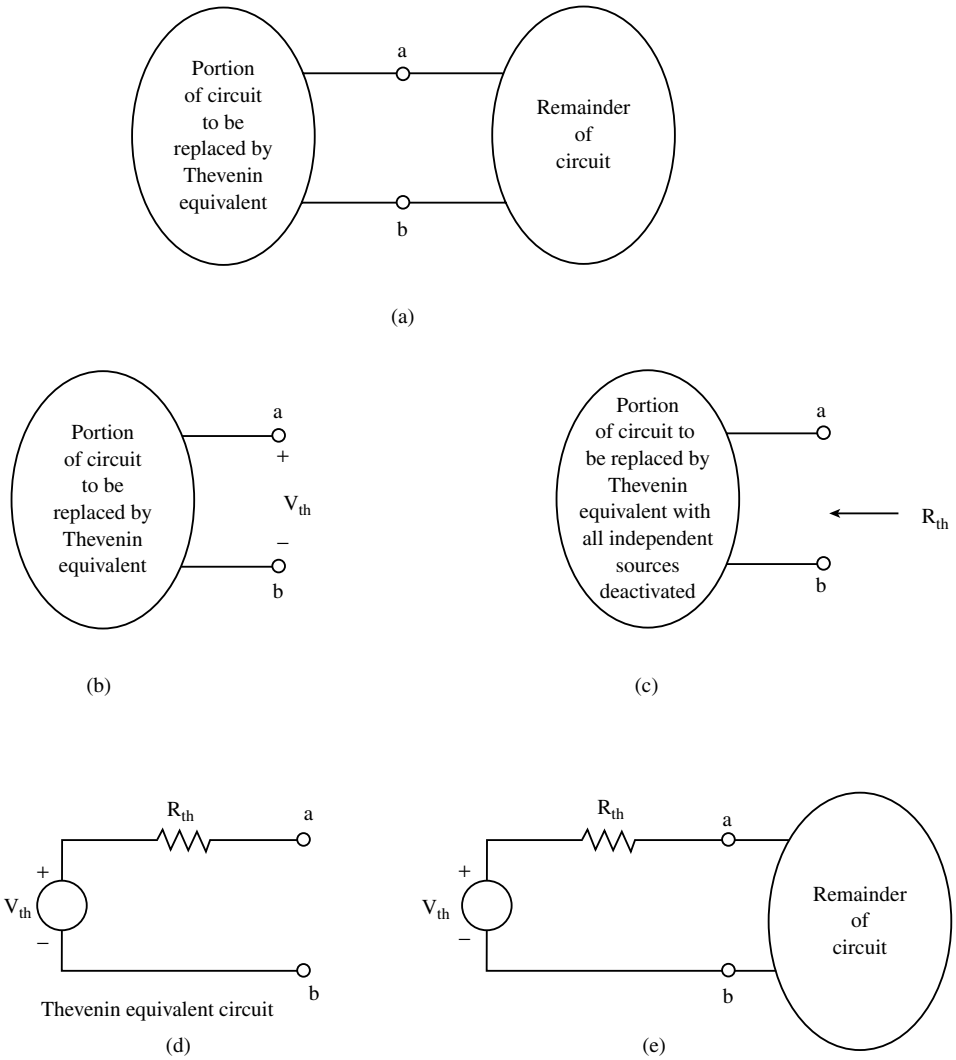

FIGURE 2.65 Steps in determining the Thévenin equivalent circuit.

Any portion of a linear circuit between two terminals a and b can be replaced by an equivalent circuit consisting of a voltage source V_{th} in series with a resistor R_{th}. The voltage V_{th} is determined as the open circuit voltage at terminals a-b. The resistor R_{th} is equal to the input resistance at terminals a-b with all the independent sources deactivated.

The various steps involved in the derivation of the Thévenin equivalent circuit are illustrated in Figure 2.65. The Thévenin voltage v_{th} is determined by solving for the voltage at terminals a-b when open circuited, and the Thévenin resistance R_{th} is determined by calculating the input resistance of the circuit at terminals a-b when all the independent sources have been deactivated. The following two examples illustrate the application of this important theorem.

Example 2.3. For the circuit in Figure 2.66, determine the Thévenin equivalent of the portion of the circuit to the left of terminals a-b; use it to calculate the current I in the 2 Ω resistor.

First, we determine V_{th} from the circuit of Figure 2.67(a). Note that because terminals a-b are open circuited the current in the branch containing the 2 Ω resistor and 9 V source is equal to 3 A in the direction shown. Applying KCL at the upper node of the 1 Ω resistor, we can calculate the current in

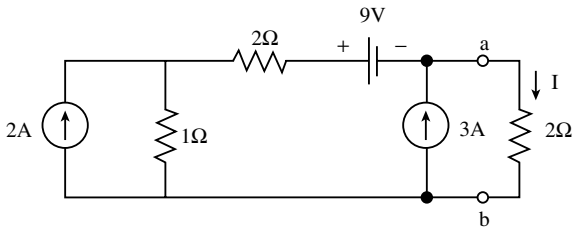

FIGURE 2.66 Circuit for Example 2.3.

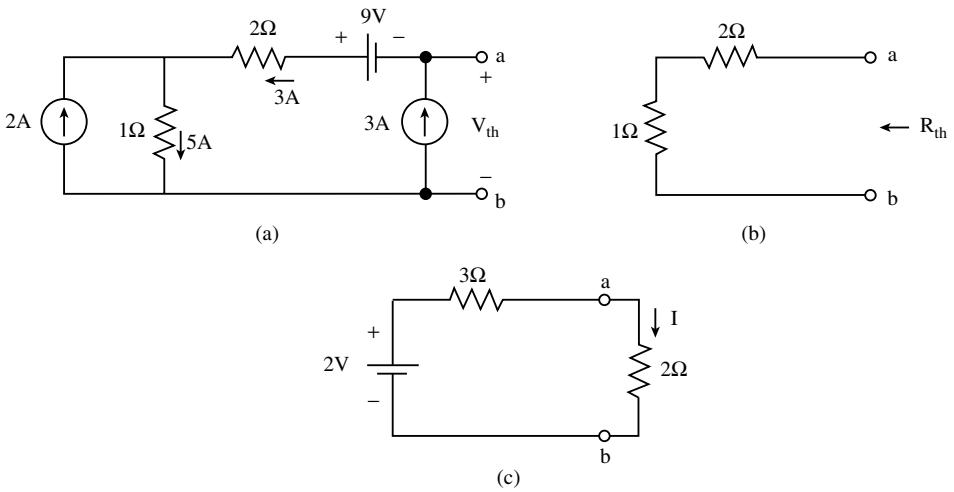

FIGURE 2.67 (a) Calculation of V_{th}, (b) calculation of R_{th}, and (c) the equivalent circuit for Example 2.3.

this resistor to be 3 + 2 = 5 A as shown. Writing a KVL equation around the inner loop (counterclockwise at terminal b) we have

$$V_{th} + 9 - (2 \times 3) - (1 \times 5) = 0$$

which yields

$$V_{th} = 2 \text{ V}$$

Now, for R_{th} the three sources are deactivated to obtain the circuit shown in Figure 2.67(b). From this circuit, it is clear that

$$R_{th} = 3\Omega$$

The circuit obtained by replacing the portion to the left of terminals a-b with its Thévenin equivalent is shown in Figure 2.67(c). The current I is now easily computed as

$$I = \frac{2}{2+3} = 0.4A$$

Example 2.4. For the circuit shown in Figure 2.60, determine the Thévenin equivalent circuit for the portion of the circuit to the left of resistor R_2.

In deriving (2.118) from (2.110), we actually already determined the Thévenin equivalent for the portion of the circuit to the left of R_2. This was shown in Figure 2.64. Of course, this procedure is *not* the most efficient way to determine the Thévenin equivalent. Let us now illustrate how the equivalent

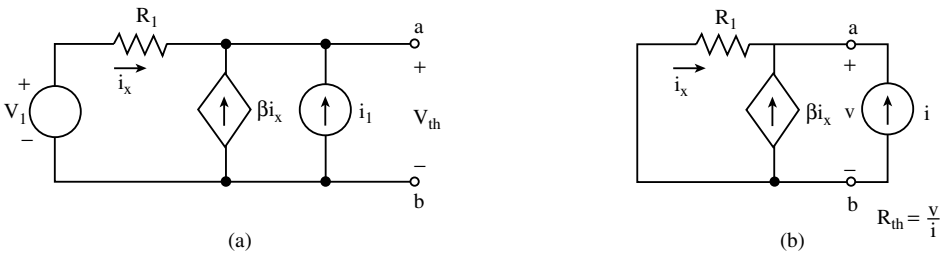

FIGURE 2.68 Calculation of (a) v_{th} and (b) R_{th} for the circuit of Figure 2.60 (Example 2.4).

circuit is obtained using the procedure described in Thévenin's theorem. First, we determine v_{th} from the circuit of Figure 2.68(a) with R_2 removed and terminals a-b left open. Applying KCL at node a, we have

$$i_x + \beta i_x + i_1 = 0$$

or

$$i_x = -\frac{i_1}{1+\beta}$$

Hence,

$$v_{th} = v_1 - R_1 i_x$$
$$= v_1 + \frac{R_1}{1+\beta} i_1$$

As for R_{th}, we need to consider the circuit shown in Figure 2.68(b), in which the two independent sources were deactivated. Because of the presence of the dependent source βi_x, we determine R_{th} by exciting the circuit with an external source. Let us use a current source i for this purpose and determine the voltage v across it as shown in Figure 2.68(b). We stress that i is an arbitrary and completely independent source and is in no way related to i_1, which was deactivated. Applying KCL at node a, we have

$$i_x + \beta i_x + i = 0$$

or

$$i_x = -\frac{1}{1+\beta} i$$

Also, applying Ohm's law to R_1,

$$v = -R_1 i_x$$

or

$$v = \frac{R_1}{1+\beta} i$$

Hence,

$$R_{th} = \frac{v}{i}$$
$$= \frac{R_1}{1+\beta}$$

Note that v_{th} and R_{th} determined previously are the same as v_0 and R_0 of (2.116) and (2.117).

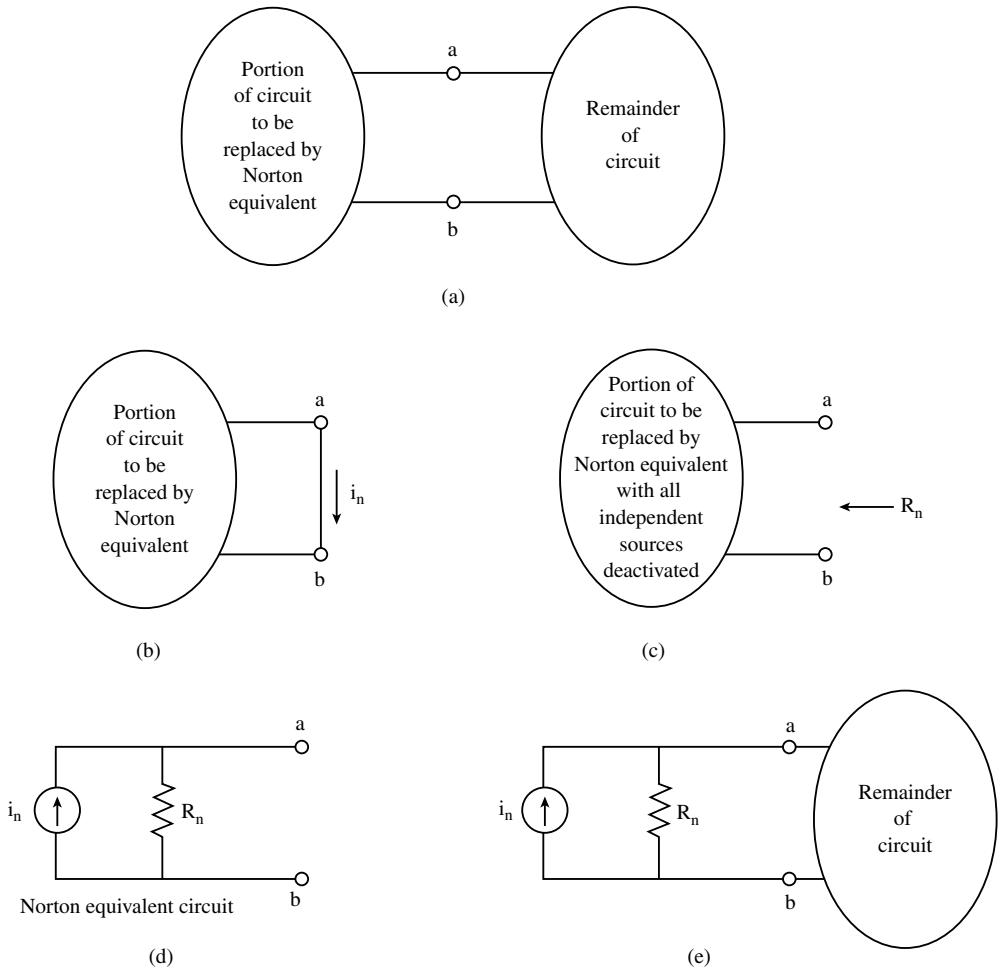

FIGURE 2.69 Steps in determining the Norton equivalent circuit.

The Norton Theorem

Instead of a voltage source in series with a resistor, it is possible to replace a portion of a circuit by an equivalent current source in parallel with a resistor. This result is formally known as *Norton's theorem* and is stated as follows:

> *Any portion of linear circuit between two terminals a and b can be replaced by an equivalent circuit consisting of a current source i_n in parallel with a resistor R_n. The current i_n is determined as the current that flows from a to b in a short circuit at terminals a-b. The resistor R_n is equal to the input resistance at terminals a-b with all the independent sources deactivated.*

As in the case of Thévenin's, the preceding theorem provides a procedure for determining the "Norton" current source and "Norton" resistance in the **Norton equivalent circuit**. The various steps in this procedure are illustrated in Figure 2.69. The Norton current is determined by solving for the current in a short circuit at terminals a-b and the Norton resistance is determined by calculating the input resistance to the circuit at terminals a-b when all independent sources have been deactivated. The Norton's equivalent of a portion of a circuit is, in effect, a nonideal current source representation of that portion. It should be noted that the procedure to determine R_n is exactly the same as that for R_{th}. In other words,

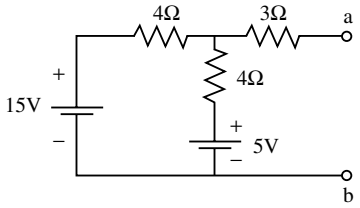

FIGURE 2.70 Circuit for Example 2.5.

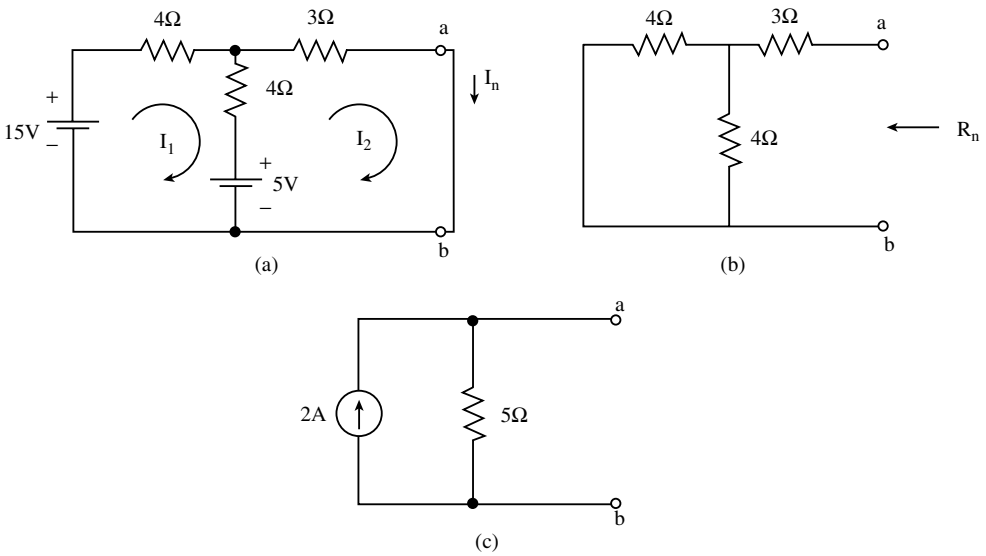

FIGURE 2.71 (a) Calculation of I_n, (b) calculation of R_n and (c) Norton's equivalent for the circuit of Example 2.5.

$$R_n = R_{th}$$

Also, if we compare Thévenin's and Norton's equivalent circuits, we see that these are indeed related by the voltage–current source transformation rule discussed earlier in this chapter. Each circuit is a source transformation of the other. For this reason, the Thévenin and Norton equivalent circuits are often referred to as **dual circuits**, and the two resistance R_{th} and R_n are frequently referred to as the source resistance and denoted by R_s. Clearly, v_{th} and i_n are related by

$$v_{th} = R_s i_n$$

Example 2.5. For the circuit shown in Figure 2.70, determine the Norton equivalent circuit at terminals a-b.

We determine Norton's current I_n by placing a short circuit between a and b, as shown in Figure 2.71(a), and solving for the current in it with a reference direction going from a to b. For this circuit, we could use the mesh equation method. In matrix form, the mesh equations are

$$\begin{bmatrix} 8 & -4 \\ -4 & 7 \end{bmatrix} \cdot \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} 10 \\ 5 \end{bmatrix}$$

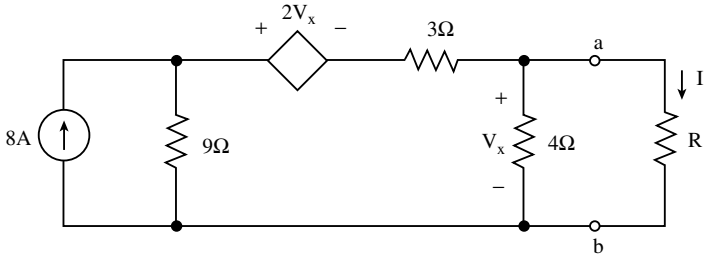

FIGURE 2.72 Circuit for Example 2.6.

and the solution for the mesh currents is

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \frac{1}{56-16}\begin{bmatrix} 7 & 4 \\ 4 & 8 \end{bmatrix}\cdot\begin{bmatrix} 10 \\ 5 \end{bmatrix}$$

From this, we extract I_n as

$$I_n = I_2 = \frac{40+40}{40} = 2A$$

Norton's resistance R_n is determined by deactivating the two voltage sources, as shown in Figure 2.71(b), and calculating the input resistance at terminals a-b. Clearly,

$$R_n = \left(4\|4\right)+3 = 5\Omega$$

Thus, the Norton equivalent for the circuit of Figure 2.70 is shown in Figure 2.71(c).

Example 2.6. For the circuit shown in Figure 2.72 determine the Norton equivalent circuit at terminals a-b and use it to calculate the current and power dissipated in *R*.

With a short circuit placed at terminals a-b, as shown in Figure 2.73(a), the voltage $V_x = 0$. Hence, the dependent source in this circuit is equal to zero. This means that the 8 A current source has the 9 Ω and 3 Ω resistors in parallel across it, and I_n is the current in the 3 Ω resistor. Using the current divider rule we have

$$I_n = 8\frac{9}{12} = 6A$$

Now, deactivating the independent source to determine R_n,we excite the circuit with a voltage source *V* at terminals a-b. Let *I* be the current in this source as shown in Figure 2.73(b). Applying KCL at node a yields the current in the 3 Ω resistor to be I – (V/4) from right to left. Applying KVL around the outer loop and making use of the fact that in this circuit $V_x = V$, we get

$$V - 3\left(I - \frac{V}{4}\right) + 2V - 9\left(I - \frac{V}{4}\right) = 0$$

Solution of this equation yields

$$R_n = \frac{V}{I} = 2\Omega.$$

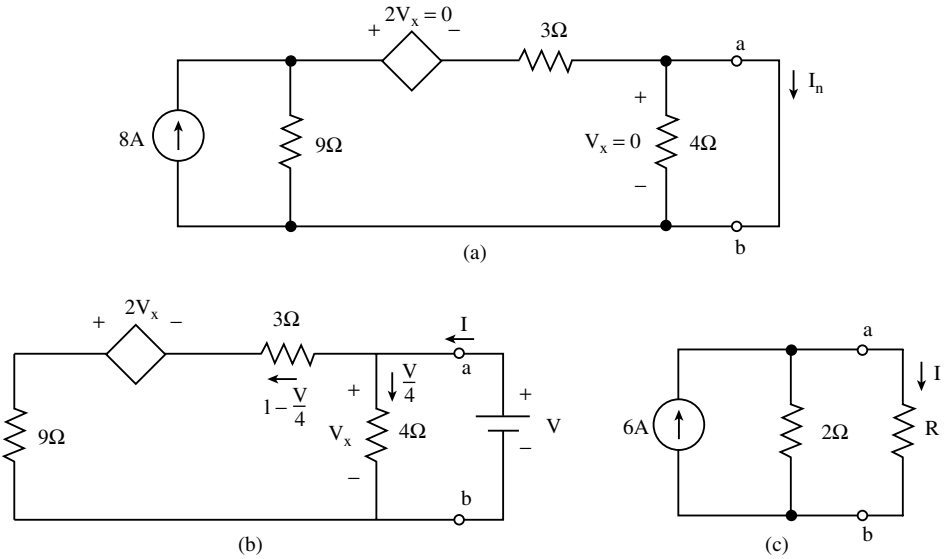

FIGURE 2.73 (a) Calculation of I_n, (b) calculation of R_n, and (c) Norton's equivalent for the circuit of Example 2.6.

The Norton equivalent of the portion of the circuit to the left of terminals a–b, connected to the resistor R is shown in Figure 2.73(c). Applying the current divider rule gives

$$I = 6\frac{2}{2+R}$$

$$= \frac{12}{2+R}\text{A}$$

and the power dissipated in R is

$$P = RI^2$$

$$P = \frac{144R}{(2+R)^2}\text{W} \tag{2.119}$$

The Maximum Power Transfer Theorem

In the previous example, we replaced the entire circuit connected to the resistor R at terminals a-b by its Norton equivalent in order to calculate the power P dissipated in R. Because R did not have a fixed value, we determined an expression for P in terms of R. Suppose we are now interested in examining how P varies as a function of R. A plot of P versus R as given by (2.119) is given in Figure 2.74.

The first noticeable characteristic of this plot is that it has a *maximum*. Naturally, we would be interested in the value of R that results in maximum power delivered to it. This information is directly available from the plot in Figure 2.74. To maximize P the value of R should be 2 **Ω** and the maximum power is P_{max} = 18 W. That is, 18 W is the most that this circuit can deliver at terminals a-b, and that occurs when R = 2 **Ω**. Any other value of R will result in less power delivered to it.

The problem of finding the value of a load resistor R_L such that maximum power is delivered to it is obviously an important circuit design problem. Because it is possible to reduce any linear circuit connected to R_L into either its Thévenin or Norton equivalent, as illustrated in Figure 2.75, the problem becomes quite simple. We need to consider only either the circuit of Figure 2.75(b) or that of 2.75(c).

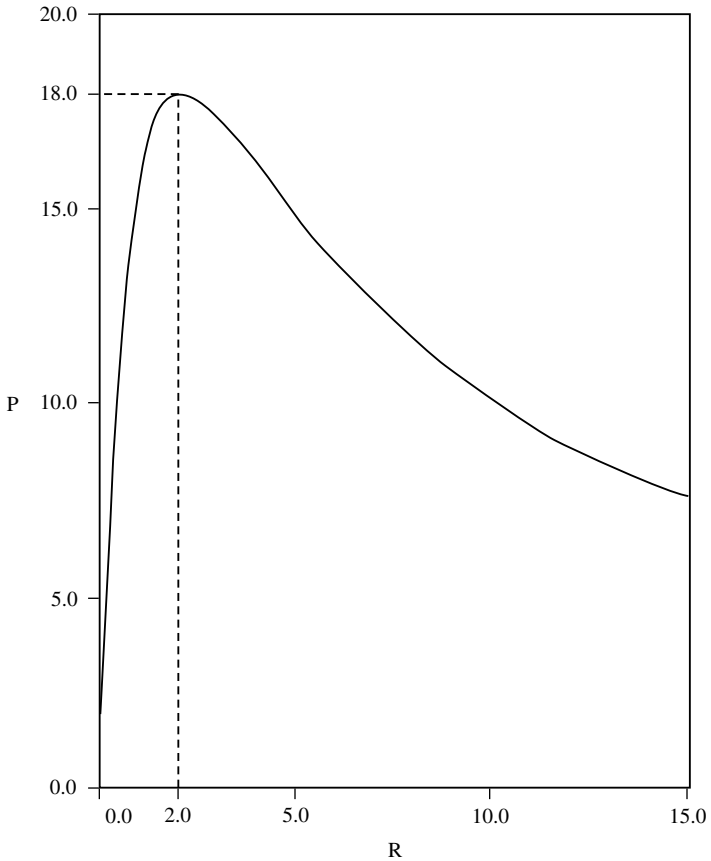

FIGURE 2.74 Plot of P vs. R for the circuit of Example 2.6.

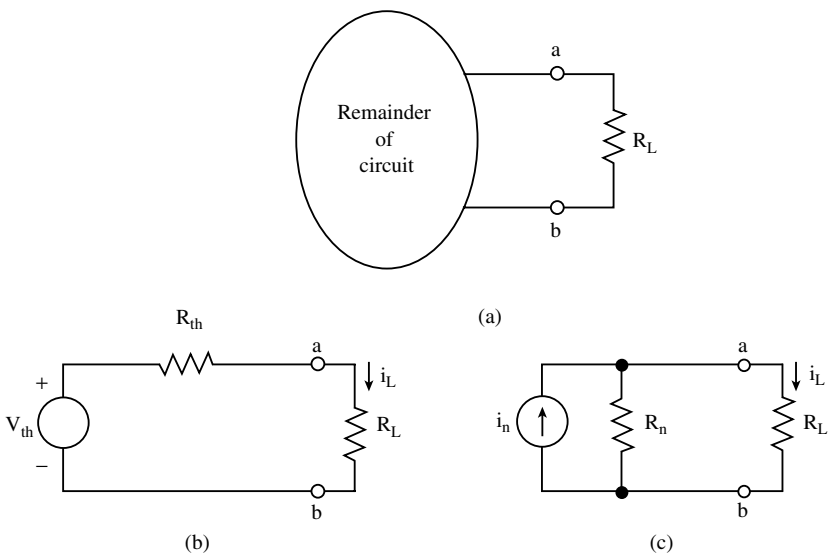

FIGURE 2.75 (a) A load resistance R_L in a circuit. (b) R_L with the remainder of the circuit reduced to a Thévenin equivalent. (c) R_L with the remainder of the circuit reduced to a Norton equivalent.

Let us first consider the circuit that uses the Thévenin equivalent. In this case, the power P delivered to R_L is given by

$$P = \left(\frac{v_{th}}{R_{th} + R_L} \right)^2 R_L \tag{2.120}$$

In general, we may not always be able to plot P vs. R_L, as we did earlier, therefore, we need to maximize P mathematically. We do this by solving the necessary condition

$$\frac{dP}{dR_L} = 0 \tag{2.121}$$

for R_L. To guarantee that R_L maximizes P, it must also satisfy the sufficiency condition

$$\left. \frac{d^2P}{dR_L^2} \right|_{R_L} < 0 \tag{2.122}$$

Thus, applying these conditions to (2.120), we have

$$\begin{aligned} \frac{dP}{dR_L} &= v_{th}^2 \left[\frac{\left(R_h + R_L\right)^2 - 2R_L\left(R_{th} + R_L\right)}{\left(R_{th} + R_L\right)^4} \right], \\ &= v_{th}^2 \frac{\left(R_{th} - R_L\right)}{\left(R_{th} + R_L\right)^3} \end{aligned} \tag{2.123}$$

Equating the right-hand side of (2.123) to zero and solving for R_L yields

$$R_L = R_{th}$$

The sufficiency condition (2.122) yields

$$\frac{d^2P}{dR_L^2} = v_{th}^2 \frac{2R_{th} - 4R_L}{\left(R_{th} + R_L\right)^4}$$

When R_L is replaced with R_{th}, we get

$$\left. \frac{d^2P}{dR_L^2} \right|_{R_L = R_{th}} = -\frac{v_{th}^2}{8R_{th}^3} < 0$$

Thus, $R_L = R_{th}$ satisfies both conditions (2.121) and (2.122), and hence is the maximizing value. This result is often referred to as the **maximum power transfer theorem**. It says

The maximum power that can be transferred to a load resistance R_L by a circuit represented by its Thévenin equivalent is attained when R_L is equal to R_{th}.

The corresponding value of $P_{\max}$ is obtained from (2.120) as

$$P_{\max} = \frac{v_{th}^2}{4R_{th}} \tag{2.124}$$

In the case of Norton's equivalent circuit of Figure 2.75(b), a similar derivation can be carried out. The power P delivered to R_L is given by

$$P = \left(\frac{R_n i_n}{R_n + R_L} \right)^2 R_L \tag{2.125}$$

This expression has exactly the same form as (2.120). Consequently, its maximum is achieved when

$$R_L = R_n$$

and the corresponding maximum power is

$$P_{\max} = \frac{R_n i_n^2}{4} \tag{2.126}$$

This leads to the following alternate statement of the **maximum power transfer theorem**:

> *The maximum power that can be transferred to a load resistance R_L by a circuit represented by its Norton equivalent is attained when R_L is equal to R_n.*

Example 2.7. Consider the circuit of Example 2.3 in Figure 2.66. Determine the value of a load resistor R_L connected in place of the 2 Ω resistor at terminals a-b in order to achieve maximum power transfer to the load.

Solution. The Thévenin equivalent for the circuit of Figure 2.66 already was determined and is shown in Figure 2.67 (c). Using the results of the maximum power transfer theorem, we should have

$$R_L = 3\ \Omega$$

The corresponding value of maximum power is

$$P_{\max} = \frac{2^2}{4 \times 3}$$

$$= \frac{1}{3} \text{W}$$

The Reciprocity Theorem

The reciprocity theorem is an important result that applies to circuits consisting of linear resistors and one independent source (either a current source or a voltage source). It does not apply to nonlinear circuits, and, in general, it does not apply to circuits containing dependent sources. The reciprocity theorem is stated as follows:

> *The ratio of a voltage (or current) response in one part of the circuit to the current (or voltage)* source is the same if the locations of the response and the source are interchanged.

It is important to note that the reciprocity theorem applies only to circuits in which the source and response are voltage and current or current and voltage, respectively. It does not apply to circuits in which the source and response are of the same type (i.e., voltage and voltage or current and current).

Example 2.8. Verify the reciprocity theorem for the circuit shown in Figure 2.76(a).

Solution. If we interchange the location of the 40 V voltage source and current response I, we obtain the circuit shown in Figure 2.76(b). The reciprocity theorem implies that I should be the same in both circuits.

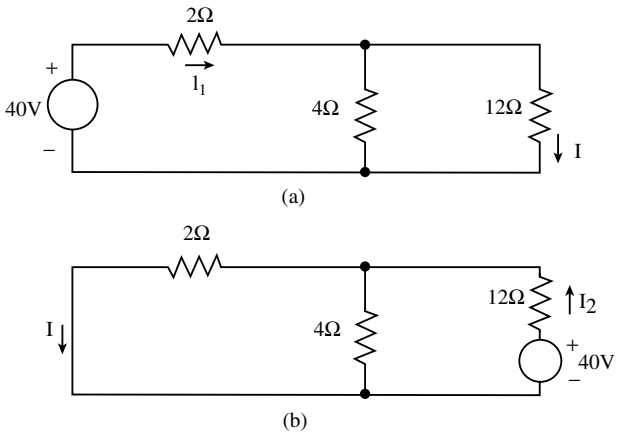

FIGURE 2.76 (a) Circuit for Example 2.8. (b) Circuit with location of voltage source and current response interchanged.

For the circuit in Figure 2.76(a), the current I_1 in the 2 Ω resistor is equal to:

$$I_1 = \frac{40}{2 + 4\|12}$$

$$= \frac{40}{2+3}$$

$$= 8\text{A}$$

and the response I can be easily determined, using the current divider rule, as:

$$I = 8 \times \frac{4}{4+12}$$

$$= 2\text{A}$$

For the circuit in Figure 2.76(b), the current I_2 in the 12 Ω resistor is equal to:

$$I_2 = \frac{40}{12 + 2\|4}$$

$$= \frac{40}{12 + \frac{4}{3}}$$

$$= 3\text{ A}$$

and the response I can be determined easily, using the current divider rule, as

$$I = 3 \times \frac{4}{2+4}$$

$$= 2\text{ A}$$

Thus, the reciprocity theorem is satisfied.