which is substantially smaller than $(V_{GS} - V_{TN})$. Thus, a MOSFET diff-amp inherently displays a higher input offset voltage than a bipolar pair for the same level of mismatch.

Partial data sheets showing some of the nonideal characteristics for the op-amps considered in the last chapter are in Table 14.1. The 741 op-amp, an all-bipolar circuit, has a maximum input offset voltage of 3 mV. The CA3140, which has a MOSFET input differential pair, has a maximum input offset voltage of 15 mV; and the LH0042C, which has a JFET input differential pair, has a maximum input offset voltage of 20 mV. This supports our conclusion that op-amps with FET input transistors have substantially larger input offset voltages than the all-bipolar circuit discussed.

14.4.2 Offset Voltage Compensation

In many applications, especially those for which the input signal is large compared to the offset voltage V_{OS}, the effect of the offset voltage is negligible. However, there are situations in which it is necessary to compensate for, or "null out," the offset voltage. Two such methods are: (a) an externally connected **offset compensation network**, and (2) an operational amplifier with **offset-null terminals**.

External Offset Compensation Network

Figure 14.20 shows a simple network for offset voltage compensation in an inverting amplifier. The resistive voltage divider of R_4 and R_5, in conjunction with potentiometer R_3, is used to make voltage adjustments of either polarity at the noninverting terminal to cancel the effects of V_{OS}. If $R_5 \ll R_4$, then the compensating voltage applied to the noninverting terminal can be in the millivolt range, which is typical of offset voltage values.

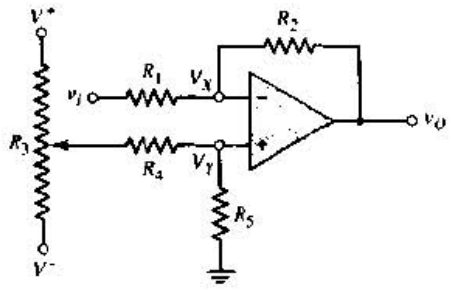

Figure 14.20 Offset voltage compensation circuit for inverting amplifier

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Example 14.11 **Objective:** Determine the range of voltage produced by an offset voltage compensation network.

Consider the compensation network in Figure 14.20 with $R_5 = 100\,\Omega$, $R_4 = 100\,\text{k}\Omega$, and a 100 kΩ potentiometer R_3. Let $V^+ = 15$ V and $V^- = -15$ V. Determine the voltage range at V_Y.

Solution: Assume the potentiometer wiper arm is connected to the V^+ supply voltage. The voltage V_Y is then

$$V_Y = \left(\frac{R_5}{R_5 + R_4}\right)V^+ = \left(\frac{0.1}{0.1 + 100}\right)(15) \Rightarrow 15\,\text{mV}$$

Comment: For this particular circuit, the compensation voltage range is -15 mV to $+15$ mV. A larger resistance R_5 will increase the offset voltage compensation range, and a smaller resistance R_5 will increase the sensitivity of offset voltage compensation.

Test Your Understanding

D14.19 Consider the compensation network in Figure 14.20. Assume $V^+ = 10$ V, $V^- = -10$ V, $R_3 = 100\,\text{k}\Omega$, and $R_4 = 100\,\text{k}\Omega$. Design R_5 such that the circuit can compensate for an offset voltage of $V_{OS} = 5$ mV. (Ans. 50 Ω)

Figure 14.21 shows a compensation network that can be used with a noninverting op-amp circuit. The same R_4–R_5 voltage divider is used with the potentiometer R_3. Typically, R_5 is on the order of 100 Ω and R_4 on the order of 100 kΩ. If $V^+ = 15$ V and $V^- = -15$ V, then the compensation voltage is again in the range of -15 mV to $+15$ mV.

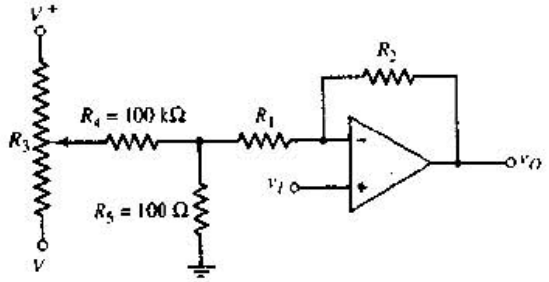


Figure 14.21 Offset voltage compensation circuit for noninverting amplifier

The voltage gain of the noninverting amplifier becomes a function of the compensation network. Since $R_5 \ll R_4$, then the gain of the amplifier, to a good approximation, is

$$A_v = \frac{v_O}{v_I} = \left(1 + \frac{R_2}{R_1 + R_5}\right) \tag{14.72}$$

Since R_5 is small, Equation (14.72) shows that the gain is not a strong function of the compensation network; however, it may still need to be taken into account.

Offset-Null Terminals

Many op-amps, including the 741 bipolar and the CA3140 BiCMOS circuits studied in Chapter 13, include a pair of external offset-null terminals, which are used to compensate for the offset voltage. Figure 14.22 shows a basic bipolar

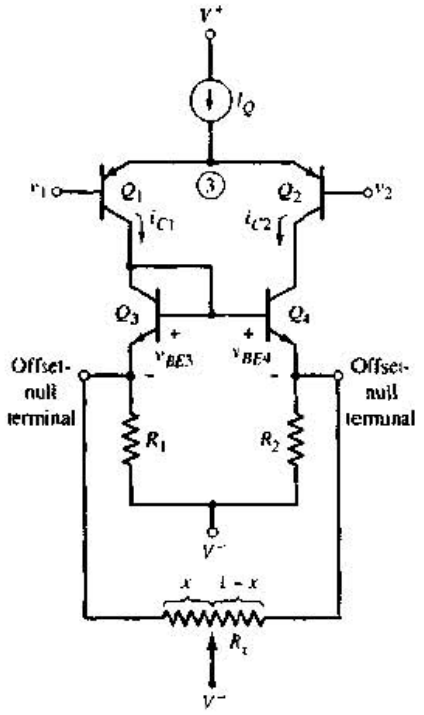


Figure 14.22 Basic bipolar input diff-amp stage, including a pair of offset-null terminals connected to a potentiometer

input diff-amp stage, including a pair of offset-null terminals. An external potentiometer R_x is connected between these terminals, and the wiper arm is connected to supply voltage V^-.

If the wiper arm of R_x is centered, then R_1 and R_2 will each have a resistance $R_x/2$ connected in parallel. When the wiper arm is moved off center, then R_1 and R_2 will each have a different resistance connected in parallel, and an asymmetry will be introduced into the circuit. This asymmetry in turn introduces an offset voltage, which cancels the input offset voltage effects. In practice, to adjust for offset voltage effects, the op-amp is connected in a feedback configuration with the input differential voltage set equal to zero. The wiper arm of potentiometer R_x is then adjusted until the output voltage becomes zero.

To demonstrate the offset-null technique, we first write a KVL equation between the base terminals of Q_3 and Q_4 and voltage V^- in Figure 14.22, as follows:

$$v_{BE3} + i_{C1}R_1' = v_{BE4} + i_{C2}R_2' \tag{14.73}$$

where R_1' and R_2' are the effective resistances in the emitters of Q_3 and Q_4, including the parallel effects of potentiometer R_x. We have that

$$R_1' = R_1 \| xR_x \qquad \text{and} \qquad R_2' = R_2 \| (1-x)R_x$$

The base–emitter voltages are

$$v_{BE3} = V_T \ln\left(\frac{i_{C1}}{I_{S3}}\right) \tag{14.74(a)}$$

and

$$v_{BE4} = V_T \ln\left(\frac{i_{C2}}{I_{S4}}\right) \tag{14.74(b)}$$

Substituting Equations (14.74(a)) and (14.74(b)) into Equation (14.73) yields

$$V_T \ln\left(\frac{i_{C1}}{I_{S3}}\right) + i_{C1}R_1' = V_T \ln\left(\frac{i_{C2}}{I_{S4}}\right) + i_{C2}R_2' \tag{14.75}$$

If a mismatch occurs between Q_3 and Q_4, meaning $I_{S3} \neq I_{S4}$, then a deliberate mismatch between R_1' and R_2' can be introduced to compensate for the transistor mismatch and the adjustment can make $i_{C1} = i_{C2}$. Similarly, a deliberate mismatch between R_1' and R_2' can be used to compensate for a mismatch between Q_1 and Q_2.

Example 14.12 **Objective:** Determine the required difference between R_1' and R_2', and the value of x in the potentiometer to compensate for a mismatch between active load transistors Q_3 and Q_4 in the diff-amp in Figure 14.22.

Assume that $I_Q = 200\,\mu\text{A}$, which means that we want $i_{C1} = i_{C2} = 100\,\mu\text{A}$. Let $I_{S3} = 10^{-14}\,\text{A}$ and $I_{S4} = 1.05 \times 10^{-14}\,\text{A}$. Also assume $R_1 = R_2 = 1\,\text{k}\Omega$ and $R_x = 100\,\text{k}\Omega$.

Solution: The difference between R_2' and R_1' is determined from Equation (14.75), as follows:

$$V_T \ln\left(\frac{i_{C1}}{I_{S3}}\right) + i_{C1}R_1' = V_T \ln\left(\frac{i_{C2}}{I_{S4}}\right) + i_{C2}R_2'$$

or

$$(0.026)\ln\left(\frac{100 \times 10^{-6}}{10^{-14}}\right) + (0.10)R_1' = (0.026)\ln\left(\frac{100 \times 10^{-6}}{1.05 \times 10^{-14}}\right) + (0.10)R_2'$$

which yields

$$R_2' - R_1' = 0.0127\,\text{k}\Omega \Rightarrow 12.7\,\Omega$$

We can also write the difference between R_2' and R_1' as

$$\frac{R_2(1-x)R_x}{R_2 + (1-x)R_x} - \frac{R_1 x R_x}{R_1 + xR_x} = 0.0127\,\text{k}\Omega$$

Substituting the values for R_1, R_2, and R_x, we find that

$$x = 0.349$$

Comment: On the basis of this analysis, the value of R_1' is $1\|34.9 = 0.9721\,\text{k}\Omega$, and the value of R_2' is $1\|(100 - 34.9) = 0.9849\,\text{k}\Omega$.

Computer Simulation Verification: Figure 14.23 is the circuit used in PSpice simulation. The values of R_X and R_Y were varied to simulate a change in the variable x in the potentiometer in the circuit in Figure 14.22. The output voltage v_O is taken off the common collectors of Q_1 and Q_3. This voltage would correspond to the input voltage of a second stage.

A change in the values of R_X and R_Y causes a slight change in the currents in the two sides of the circuit. A change in current causes a change in the collector–emitter

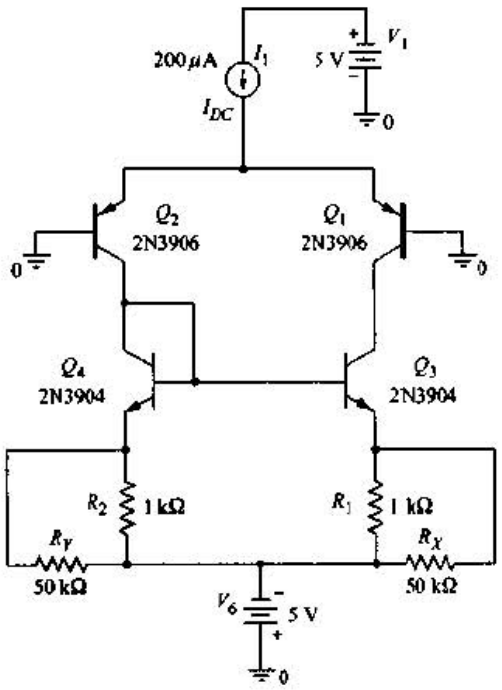


Figure 14.23 Circuit used in the computer simulation analysis for Example 14.12

voltages of Q_1 and Q_3, or a change in the output voltage. Figure 14.24 shows the output voltage as a function of x, or as a function of the position of the potentiometer. The results show that a change of approximately 0.7 V is possible for this range in potentiometer setting. This change in voltage would represent a large change in input voltage for the second stage, which in turn would cause a large change in the dc value of the output voltage. The dc output voltage could therefore be set to zero by adjusting the potentiometer setting.

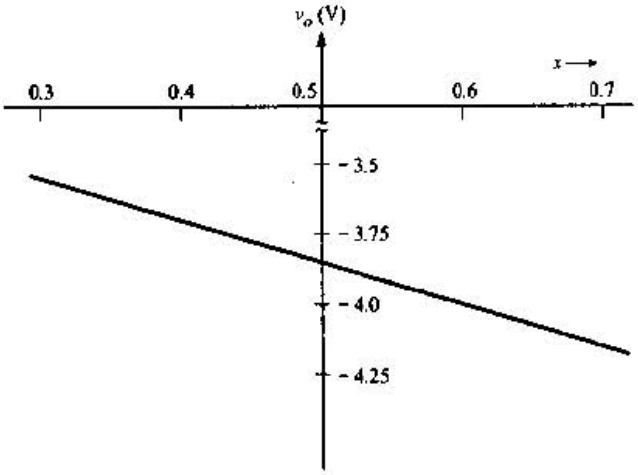


Figure 14.24 Output voltage versus potentiometer setting

Test Your Understanding

***14.20** Consider the diff-amp in Figure 14.22 with a pair of offset-null terminals. Let $R_1 = R_2 = 1\,\text{k}\Omega$. Let R_x be a $100\,\text{k}\Omega$ potentiometer. Assume $I_Q = 100\,\mu\text{A}$ and $I_{S3} = 10^{-14}\,\text{A}$. If the wiper arm on the potentiometer is adjusted such that $25\,\text{k}\Omega$ is in parallel with R_1 and $75\,\text{k}\Omega$ is in parallel with R_2, determine the value of I_{S4} for $i_{C1} = i_{C2}$. (Ans. $1.05 \times 10^{-14}\,\text{A}$)

14.5 INPUT BIAS CURRENT

The input currents to an ideal op-amp are zero. In actual operational amplifiers, however, the input bias currents are not zero. If the input stage consists of a pair of npn transistors, as shown in Figure 14.25(a), the bias currents enter the input terminals. However, if the input state consists of a pair of pnp transistors, as shown in Figure 14.25(b), the bias currents leave the input terminals.

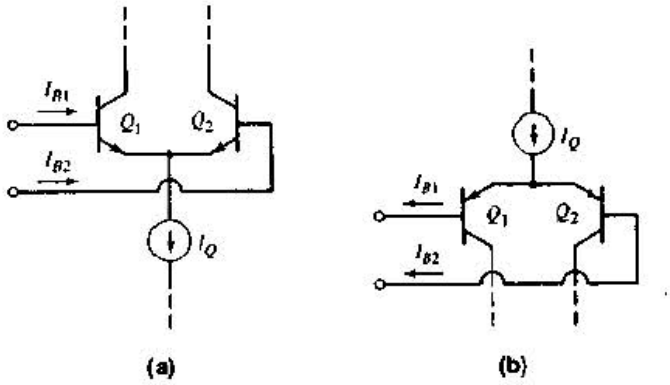


Figure 14.25 (a) Pair of npn transistors, showing input bias currents, and (b) pair of pnp transistors, showing input bias currents

If the input diff-amp consists of a pair of JFETs, the input bias currents are normally much smaller than those in a bipolar differential pair. A MOSFET input differential pair, generally, must include protection devices as discussed in Chapter 13, so the input bias currents are also not zero even in this case.

For op-amps with a bipolar input stage, the input bias currents may be as high as $10\,\mu\text{A}$ and as low as a few nanoamperes. For op-amps with an FET input stage, the bias currents may be as low as a few picoamperes. Table 14.1 lists the typical input bias current. For the 741 op-amp it is 30 nA, and for the FET input op-amps it is in the low picoampere range.

14.5.1 Bias Current Effects

Figure 14.26 schematically shows an op-amp with input bias currents. If the input stage is symmetrical, with all corresponding elements matched, then

$I_{B1} = I_{B2}$. However, if the input transistors are not exactly identical, then $I_{B1} \neq I_{B2}$. The **input bias current** is then defined as the average of the two input currents, or

$$I_B = \frac{I_{B1} + I_{B2}}{2} \tag{14.76}$$

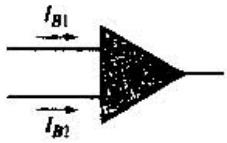


Figure 14.26 Op-amp with input bias currents

The difference between the two input currents is called the **input offset current** I_{OS} and is given by

$$I_{OS} = |I_{B1} - I_{B2}| \tag{14.77}$$

The algebraic sign of the offset current is usually not important, just as the offset voltage polarity is not critical. The typical input offset current is on the order of 10 percent of the input bias current, although data sheets may list larger values. The typical and maximum input offset currents for the three op-amps analyzed in the last chapter are given in Table 14.1.

Figure 14.27 shows an op-amp and associated resistors for a zero input voltage. Even if $I_{B2} \neq 0$, the noninverting terminal is still at zero volts, or $V_Y = 0$. From the virtual ground concept, we have $V_X = 0$, which means that the current in R_1 must be zero. Bias current I_{B1} is therefore supplied by the output of the op-amp and flows through R_2, producing an output voltage. If, for example, $I_{B1} = 5\,\mu A$ and $R_2 = 100\,k\Omega$, then $v_O = 0.5\,V$, which is unacceptable in most applications. Smaller input bias currents and a smaller feedback resistor will reduce the bias current effects.

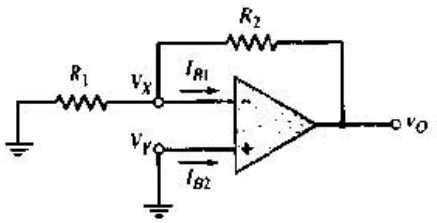


Figure 14.27 Op-amp with grounded noninverting terminal

14.5.2 Bias Current Compensation

The effect of bias currents in op-amp circuits can be minimized with a simple compensation technique. Consider the circuit in Figure 14.28. We determine v_O as a function of I_{B1} and I_{B2} using superposition. For $I_{B2} = 0$, then $V_Y = V_X = 0$, and the output voltage due to I_{B1} is

$$v_O(I_{B1}) = I_{B1} R_2 \tag{14.78(a)}$$

For $I_{B1} = 0$, we find

$$V_Y = -I_{B2} R_3 = V_X$$

Since

$$v_O = (1 + R_2/R_1) V_X$$

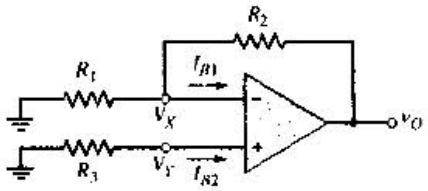


Figure 14.28 Op-amp circuit with resistor connected to noninverting terminal, for input bias current compensation

the output voltage due to I_{B2} is

$$v_O(I_{B2}) = -I_{B2}R_3\left(1 + \frac{R_2}{R_1}\right) \tag{14.78(b)}$$

The net output voltage due to both I_{B1} and I_{B2} is the sum of Equations (14.78(a)) and (14.78(b)), or

$$v_O = I_{B1}R_2 - I_{B2}R_3\left(1 + \frac{R_2}{R_1}\right) \tag{14.79}$$

If $I_{B1} = I_{B2} \equiv I_B$ and if the combination of the three resistances can be adjusted to produce $v_O = 0$, then Equation (14.79) becomes

$$0 = I_B\left[R_2 - R_3\left(1 + \frac{R_2}{R_1}\right)\right] \tag{14.80}$$

which means that

$$R_2 = R_3\left(1 + \frac{R_2}{R_1}\right) \tag{14.81}$$

Equation (14.81) can be rearranged as follows:

$$R_3 = \frac{R_1R_2}{R_1 + R_2} = R_1 \| R_2 \tag{14.82}$$

Equation (14.82) shows that R_3 should be made equal to the parallel combination of R_1 and R_2, to eliminate the effect of equal input bias currents.

If $R_3 = R_1 \| R_2$ and if the bias currents are not equal, then from Equation (14.79), we have

$$v_O = R_2(I_{B1} - I_{B2}) = R_2I_{OS} \tag{14.83}$$

Since the input offset current is normally a fraction of the input bias current, Equation (14.83) shows that the bias current effect can be reduced by making $R_3 = R_1 \| R_2$.

Example 14.13 **Objective:** Determine the bias current effect in an op-amp circuit, with and without bias current compensation.

Consider the op-amp circuits in Figures 14.27 and 14.28. Let $R_1 = 10\,\text{k}\Omega$ and $R_2 = 100\,\text{k}\Omega$. Assume $I_{B1} = 1.1\,\mu\text{A}$ and $I_{B2} = 1.0\,\mu\text{A}$.

Solution: For the op-amp circuit in Figure 14.27, the output voltage due to the bias currents is

$$v_O = I_{B1}R_2 = (1.1 \times 10^{-6})(100 \times 10^3) = 0.11\,\text{V}$$

For the circuit in Figure 14.28, we design R_3 such that

$$R_3 = R_1 \| R_2 = 10 \| 100 = 9.09\,\text{k}\Omega$$

Then, from Equation (14.83), we find

$$v_O = R_2(I_{B1} - I_{B2}) = (100 \times 10^3)(1.1 - 1.0) \times 10^{-6} = 0.010\,\text{V}$$

Comment: Even if the input offset current is not zero, the effect of the input bias currents can be reduced substantially by incorporating resistor R_3.

Usually the effect of bias currents in op-amp circuits is significant only for circuits with large resistor values. For these situations, an op-amp with an FET input stage may be necessary.

Test Your Understanding

14.21 For the op-amp in Figure 14.28, the parameters are: $R_1 = 10\,\text{k}\Omega$ and $R_2 = 100\,\text{k}\Omega$. If $I_{B1} = 1.1\,\mu\text{A}$ and $I_{B2} = 1.0\,\mu\text{A}$, can R_3 be adjusted such that $v_O = 0$? If so, what is the value of R_3? (Ans. $R_3 = 10\,\text{k}\Omega$)

14.22 Consider the inverting summing amplifier in Figure 14.29. Assume input bias currents of $I_{B1} = I_{B2} = 1\,\mu\text{A}$. (a) For $v_{i1} = v_{i2} = 0$ and $R_4 = 0$, determine v_O due to the bias currents. (b) Find the value of R_4 that compensates for the effects of the bias currents. (Ans. (a) $v_O = 0.20\,\text{V}$ (b) $R_4 = 28.6\,\text{k}\Omega$)

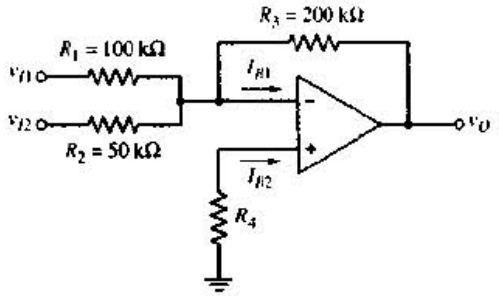


Figure 14.29 Figure for Exercise 14.22

14.6 ADDITIONAL NONIDEAL EFFECTS

Two additional nonideal effects in op-amps are: temperature effects and common-mode rejection ratio. We will look at each of these in this section.

14.6.1 Temperature Effects

Individual transistor parameters are functions of temperature. For bipolar transistors, the collector current is

$$i_C = I_S e^{v_{BE}/V_T} \tag{14.84}$$

where both I_S and V_T are functions of temperature. We expect the open-loop gain to vary with temperature, but as we saw in Section 14.2, the fractional change in the closed-loop gain is orders of magnitude less than the fractional change in the open-loop gain. This then makes the closed-loop gain very insensitive to temperature variations.

Offset Voltage Temperature Coefficient

The electrical properties of transistors are functions of temperature, which means that the input offset voltage is a function of temperature. The rate of change of offset voltage with temperature is defined as the **temperature coefficient of offset voltage**, or **input offset voltage drift**, and is given by

$$\mathrm{TC}v_{OS} = \frac{dV_{OS}}{dT} \tag{14.85}$$

For a bipolar diff-amp input stage, the offset voltage, from Equation (14.59(b)), is

$$V_{OS} = V_T \ln(I_{S2}/I_{S1})$$

The temperature variations of the I_S parameters cancel; therefore, the offset voltage is directly proportional to the thermal voltage V_T, which in turn is directly proportional to temperature. From Equation (14.59(b)), the temperature coefficient is then

$$\mathrm{TC}v_{OS} = \frac{V_{OS}}{T} \tag{14.86}$$

where T is the absolute temperature. Thus, for $V_{OS} = 1\,\mathrm{mV}$, the temperature coefficient is $\mathrm{TC}v_{OS} = 1\,\mathrm{mV}/300\,^{\circ}\mathrm{K} \Rightarrow 3.3\,\mu\mathrm{V}/^{\circ}\mathrm{C}$. A change of 10 °C will therefore result in an offset voltage change of approximately $33\,\mu\mathrm{V}$. The temperature coefficients of offset voltage listed in Table 14.1 are in the range of 10 $15\,\mu\mathrm{V}/^{\circ}\mathrm{C}$.

Consequently, the offset voltage compensation techniques discussed previously are completely effective at only one temperature. As the device temperature drifts in either direction from the temperature at which the compensation network was designed, the offset voltage effect is not completely compensated. However, the offset voltage drift is substantially less than the initial offset voltage, so offset voltage compensation is still desirable.

Input Offset Current Temperature Coefficient

The input bias currents are functions of temperature. For example, the input bias current of a bipolar input stage has the same functional dependence as the collector current, as given by Equation (14.84). If the input devices are not matched, then an input offset current I_{OS} exists, which is also a function of temperature. The input offset current temperature coefficient is dI_{OS}/dT. For the 741 op-amp, the maximum value given in Table 14.1 is $0.5\,\mathrm{nA}/^{\circ}\mathrm{C}$. If the input offset current becomes a problem in a particular design, then a JFET or MOSFET input stage of-amp may be required.

14.6.2 Common-Mode Rejection Ratio

We considered the common-mode gain (A_{cm}) and common-mode rejection ratio (CMRR) of the difference amplifier in Chapter 11. Since a diff-amp is the op-amp input stage, any common-mode signal produced at the input stage will propagate through the op-amp to the output. Therefore, the CMRR of the op-amp is essentially the same as the CMRR of the input diff-amp.

Figure 14.30(a) shows the open-loop op-amp with a pure differential-mode input signal. The differential-mode gain A_d is the same as the open-loop gain A_{OL}. Figure 14.30(b) shows the open-loop op-amp with a pure common-mode input signal. The common-mode rejection ratio, in dB, is

$$\text{CMRR}_{\text{dB}} = 20\log_{10}\left|\frac{A_d}{A_{cm}}\right| \tag{14.87}$$

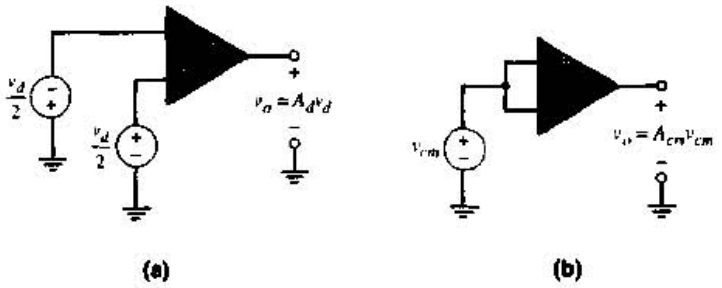


Figure 14.30 *Open-loop op-amp (a) with pure differential-mode input signal and (b) with pure common-mode input signal*

Typical values of CMRR_{dB} range from 80 to 100 dB. Table 14.1 lists typical CMRR_{dB} values for three op-amps.

14.7 SUMMARY

- A finite open-loop amplifier gain results in the magnitudes of the inverting amplifier and noninverting amplifier gains being smaller than the ideal values.
- A finite open-loop amplifier gain plus finite input amplifier resistance and nonzero output resistance results in nonideal op-amp input and output resistance values. In the case of a shunt input feedback connection (e.g., inverting op-amp), the input resistance is small but not ideally zero. In the case of a series input feedback connection (e.g., noninverting op-amp), the input resistance is large but not ideally infinite. For a shunt output feedback connection, the output resistance is small (may be in the milliohm range) but not zero.
- The practical op-amp circuit has a finite bandwidth. With negative feedback, the gain–bandwidth product is essentially constant, so an op-amp circuit with negative feedback has a reduced gain magnitude but an increased small-signal bandwidth.
- Slew rate is defined as the maximum rate at which the op-amp output signal can change per unit time. In general, the slew rate is limited by the internal frequency compensation capacitor. The slew rate is also a function of the bias current in the input diff-amp stage. Slew rates are typically in the 0.5–3 V/μs range. Full-power bandwidth is the maximum frequency at which an op-amp circuit can operate without being slew-rate limited. This frequency is a function of both the slew rate and the peak value of output voltage.

- An input offset voltage means that the output voltage is not zero when the input signal voltages are zero. One source of an offset voltage is a mismatch in the differential pair transistor parameters and/or mismatches in active load transistor parameters. Typically, an offset voltage of a few millivolts may occur in a bipolar circuit, whereas an offset voltage of tens of millivolts may occur in a MOSFET circuit.
- Two techniques of offset voltage compensation were analyzed. The first technique involves using an external potentiometer network at the input to the amplifier to null out the offset voltage. The second technique uses a potentiometer connected to a pair of offset-null terminals connected to the input diff-amp circuit.
- Input bias currents of an ideal op-amp are zero. However, actual bias currents may range from a few picoamperes for FET input stages to as high as a few microamperes for some bipolar input stages. The input bias currents can produce an unwanted component of output voltage. We analyzed the design of input bias current compensation circuits that eliminate or at least minimize these bias current effects.
- Variations in temperature produce variations in offset voltage and input bias currents. Therefore, the offset voltage and input bias current compensation circuits are completely effective only at one temperature. Typical offset voltage temperature coefficients are in the range of a few $\mu V/°C$ and input bias current temperature coefficients may be in the range of a few $nA/°C$.

CHECKPOINT

After studying this chapter the reader should have the ability to:

✔ Understand differences between ideal and practical values of various parameters of the operational amplifier circuit. (Section 14.1)

✔ Understand the effect of a finite open-loop amplifier gain on the characteristics of the op-amp. (Section 14.2)

✔ Understand the small-signal frequency response and the large-signal slew-rate response of op-amps. (Section 14.3)

✔ Understand offset voltage characteristics and design offset voltage compensation circuits for an op-amp. (Section 14.4)

✔ Understand input bias current effects and design input bias current compensation circuits for an op-amp. (Section 14.5)

REVIEW QUESTIONS

1. List and describe five practical op-amp parameters and discuss the effect they have on op-amp circuit characteristics.
2. What is a typical value of open-loop, low-frequency gain of an op-amp circuit? How does this compare to the ideal value?
3. How does a finite open-loop gain affect the closed-loop gains of the inverting and noninverting amplifiers?
4. How does a finite open-loop gain affect the (a) input resistance of an op-amp circuit and (b) the output resistance of an op-amp circuit? Consider the inverting and noninverting amplifiers.
5. Describe the open-loop amplifier frequency response and define the unity-gain bandwidth.
6. What is a typical corner frequency value, or dominant-pole frequency, in an open-loop frequency characteristic?
7. Describe the gain–bandwidth product property on a closed-loop amplifier response.

8. Define slew rate.
9. What is meant by full-power bandwidth?
10. What is the primary source of slew-rate limitation in an op-amp circuit?
11. What is one cause of an offset voltage in the input stage of a BJT op-amp?
12. What is one cause of an offset voltage in the input stage of a CMOS op-amp?
13. Describe an offset voltage compensation technique.
14. What is the source of input bias current in the 741 op-amp?
15. What can be the effect of an input bias current?
16. Describe any difference in input bias current effects between a pnp BJT input differential pair and an npn BJT input differential pair.
17. Describe the effect of input bias currents on an integrator.
18. Describe an input bias current compensation technique.
19. Define and explain common-mode rejection ratio.

PROBLEMS

Section 14.2 Finite Open-Loop Gain

14.1 For the op-amp used in the inverting amplifier configuration in Figure P14.1, the open-loop parameters are $A_{OL} = 10^3$ and $R_o = 0$. Determine the closed-loop gain $A_{CL} = v_O/v_I$ and input resistance R_{if} for an open-loop input differential-mode resistance of: (a) $R_i = 1\,\text{k}\Omega$, (b) $R_i = 10\,\text{k}\Omega$, and (c) $R_i = 100\,\text{k}\Omega$.

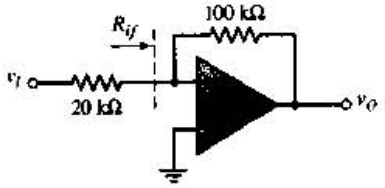


Figure P14.1

14.2 A pressure transducer, as described in Example 14.1, is to be used in conjunction with a noninverting op-amp circuit. The ideal output voltage is to be +0.10 V for a transducer voltage of 2 mV. Determine the minimum open-loop gain required so that the actual output voltage is within 0.1 percent of the ideal.

14.3 Consider the two inverting amplifiers in cascade in Figure P14.3. The op-amp parameters are $A_{OL} = 5 \times 10^3$, $R_i = 10\,\text{k}\Omega$, and $R_o = 1\,\text{k}\Omega$. Determine the actual

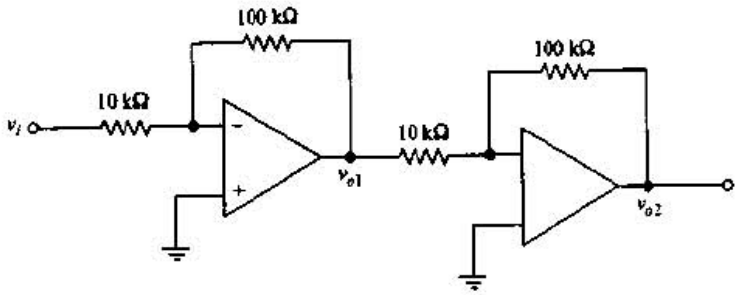


Figure P14.3

closed-loop gains $A_{vf1} = v_{o1}/v_i$ and $A_{vf} = v_{o2}/v_i$. What is the percent error from the ideal values?

14.4 The noninverting amplifier in Figure P14.4 has an op-amp with open-loop properties: $A_{OL} = 10^3$, $R_i = 20\,\text{k}\Omega$, and $R_o = 0.5\,\text{k}\Omega$. (a) Determine the closed-loop values of $A_{CL} = v_O/v_I$, R_{if}, and R_{of}. (b) If A_{OL} decreases by 10 percent, determine the percentage change in A_{CL}.

14.5 For the op-amp in the voltage follower circuit in Figure P14.5, the open-loop parameters are: $A_{OL} = 10^4$, $R_i = 100\,\text{k}\Omega$, and $R_o = 200\,\Omega$. Determine: (a) the closed-loop voltage gain $A_v = v_O/v_I$, and (b) the output resistance R_{of}.

14.6 The summing amplifier in Figure P14.6 has an op-amp with open-loop parameters: $A_{OL} = 2 \times 10^5$, $R_i = \infty$, and $R_o = 0$. Determine the actual output voltage as a function of v_{I1} and v_{I2}. What is the percent error from the ideal value?

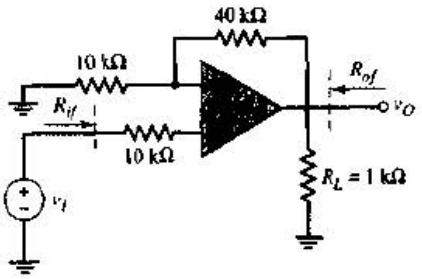


Figure P14.4

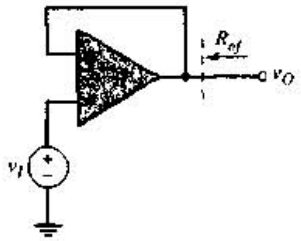


Figure P14.5

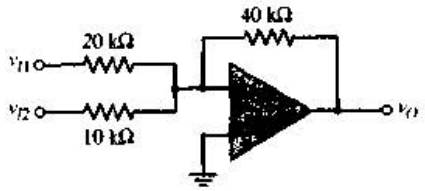


Figure P14.6

14.7 For the op-amp in the differential amplifier in Figure P14.7, the open-loop parameters are: $A_{OL} = 10^3$, $R_i = \infty$, and $R_o = 0$. Determine the actual differential voltage gain $A_d = v_O/(v_{I2} - v_{I1})$. What is the percentage error from the ideal value?

14.8 Because of a manufacturing error, the open-loop gain of each op-amp in the circuit in Figure P14.8 is only $A_{OL} = 100$. The open-loop input and output resistances are $R_i = 10\,\text{k}\Omega$ and $R_o = 1\,\text{k}\Omega$, respectively. Determine the closed-loop parameters: (a) R_{if}, (b) R_{of}, and (c) $A_{CL} = v_{O2}/v_I$. (d) What is the ratio of the actual closed-loop gain to the ideal value?

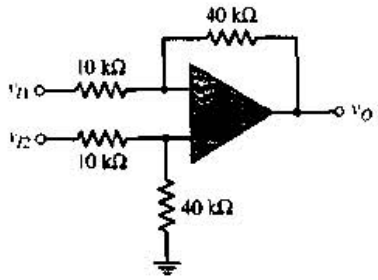


Figure P14.7

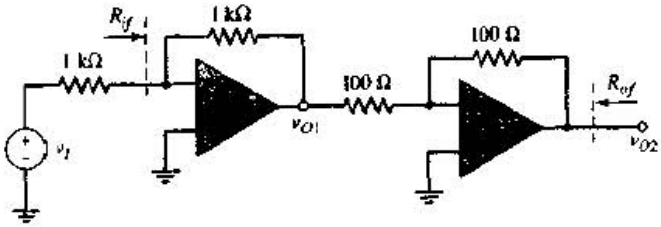


Figure P14.8

Section 14.3 Frequency Response

14.9 The low-frequency open-loop gain of an op-amp is 2×10^5 and the second pole occurs at a frequency of 5 MHz. An amplifier using this op-amp has a low-frequency closed-loop gain of 100 and a phase margin of 80 degrees. Determine the dominant-pole frequency.

14.10 Two inverting amplifiers are connected in cascade to provide an overall voltage gain of 500. The gain of the first amplifier is -10 and the gain of the second amplifier is -50. The unity-gain bandwidth of each op-amp is 1 MHz. (a) What is the bandwidth of the overall amplifier system? (b) Redesign the system to achieve the maximum bandwidth. What is the maximum bandwidth?

14.11 The open-loop low-frequency gain of an op-amp is found to be $A_o = 5 \times 10^4$. At a frequency of $f = 10^4$ Hz, the open-loop gain is 200. Determine the dominant-pole frequency and the unity-gain bandwidth.

14.12 An inverting amplifier circuit has a voltage gain of -25. The op-amp used in the circuit has a low-frequency voltage gain of 5×10^4 and a unity-gain bandwidth of 1 MHz. Determine the dominant pole frequency of the op-amp and the small-signal bandwidth, $f_{3\text{-dB}}$, of the inverting amplifier. What is the magnitude of the closed-loop voltage gain at $0.5f_{3\text{-dB}}$ and at $2f_{3\text{-dB}}$?

14.13 An audio amplifier system, using a noninverting op-amp circuit, needs to have a small-signal bandwidth of 20 kHz. The open-loop low-frequency voltage gain of the op-amp is 10^5 and the unity-gain bandwidth is 1 MHz. What is the maximum closed-loop voltage gain that can be obtained for these specifications?

14.14 If an op-amp has a slew rate of 10 V/μs, find the full-power bandwidth for a peak output voltage of 10 V.

14.15 (a) An op-amp with a slew rate of 8 V/μs is driven by a 250 kHz sine wave. What is the maximum output amplitude at which slew-rate limiting is reached? (b) Repeat part (a) for a 250 kHz zero time-average triangular wave.

14.16 The op-amp in the noninverting amplifier configuration in Figure P14.16 has a slew rate of 1 V/μs. Sketch the output voltage versus time for each of the three inputs shown. The op-amp is biased at ±10 V.

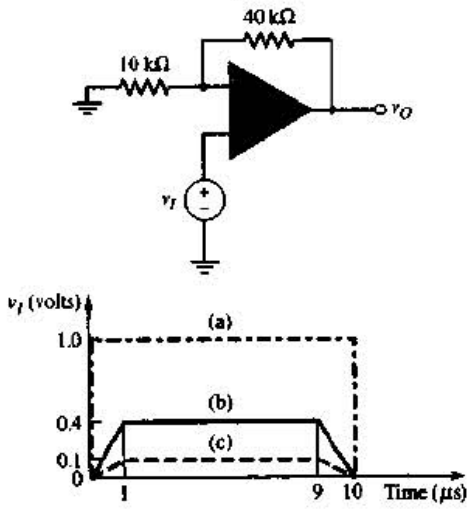


Figure P14.16

14.17 For each op-amp in the circuit shown in Figure P14.17, the bias is ±15 V and the slew rate is 3 V/μs. Sketch the output voltages v_{O1} and v_{O2} versus time for each input shown.

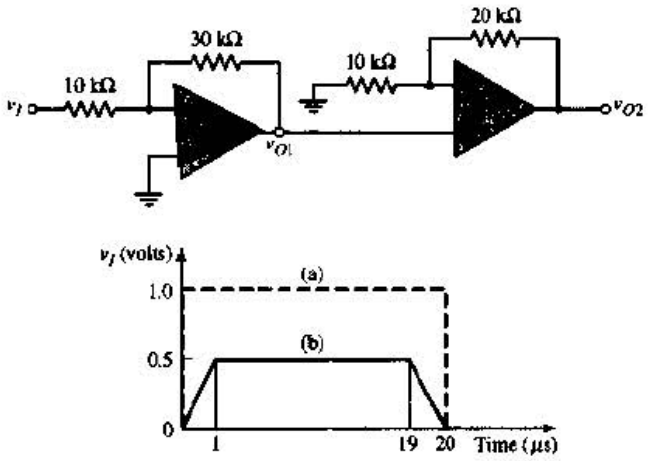


Figure P14.17

14.18 The op-amp to be used in the audio amplifier system in Problem 14.13 has a slew rate of 0.8 V/μs. Determine the maximum peak value of output voltage that can be obtained for these specifications.

Section 14.4 Offset Voltage

14.19 For the transistors in the diff-amp in Figure 14.16 in the text, the current parameters I_{S1} and I_{S2} can be written as $5 \times 10^{-14}(1 + x)$ A, where x represents the deviation from the ideal due to variations in electrical and geometric characteristics. (The value of x is positive for one transistor and negative for the other transistor.) Determine the maximum value of x such that the maximum offset voltage is limited to $V_{OS} = 2.5$ mV.

14.20 The bipolar active load diff-amp in Figure 14.18 in the text is biased at $V^+ = 5$ V. The transistor parameters are: $v_{BE}(\text{npn}) = v_{EB}(\text{pnp}) = 0.6$ V, $V_{AN} = V_{AP} = 80$ V, $I_{S1} = I_{S2}$, and $I_{S4} = 10^{-14}$ A. Determine the value of I_{S3} for which Q_2 has a C–E voltage of $v_{CE2} = 0.6$ V.

14.21 An inverting op-amp circuit has a gain of −50. The op-amp used in the circuit has an offset voltage of ±2.5 mV. If the input signal voltage to the circuit is 20 mV, determine the possible range in the output voltage.

14.22 Consider the integrator circuit in Figure P14.22. The circuit parameters are $R = 10$ kΩ and $C = 10$ μF. The op-amp offset voltage is ±5 mV. For $v_i = 0$, determine the output voltage versus time. For the worst-case offset voltage, determine the time that it would take for the output voltage to reach ±5 V.

D14.23 In the circuit in Figure P14.23, the offset voltage of each op-amp is $V_{OS} = 10$ mV. (a) Find the worst-case output voltages v_{O1} and v_{O2} for $v_I = 0$. (b) Design offset voltage compensation circuit(s) to adjust both v_{O1} and v_{O2} to zero when $v_I = 0$.

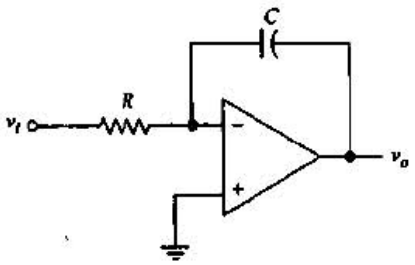


Figure P14.22

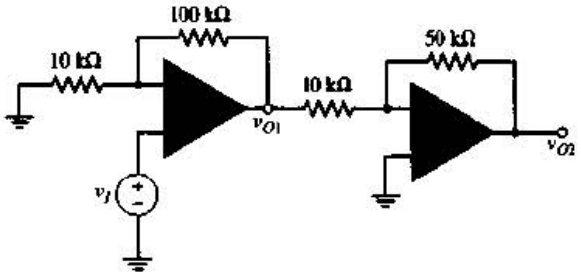


Figure P14.23

14.24 In the circuit shown in Figure P14.24, the op-amp is ideal. For $v_I = 0.5\,\text{V}$, determine v_O when the wiper arm of the potentiometer is at the V^+ node, in the center, and at the V^- node.

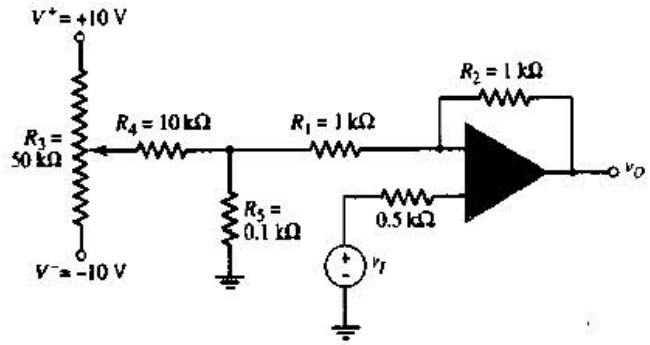


Figure P14.24

14.25 Consider the bipolar diff-amp with an active load and a pair of offset-null terminals as shown in Figure 14.22 in the text. Let $R_1 = R_2 = 500\,\Omega$ and let R_x be a $50\,\text{k}\Omega$ potentiometer. (a) If the wiper arm of the potentiometer is exactly in the center, determine the effective resistances R_1' and R_2'. (b) Assume $I_Q = 250\,\mu\text{A}$ meaning that $i_{C1} = i_{C2} = 125\,\mu\text{A}$. Let $I_{S3} = 2 \times 10^{-14}\,\text{A}$ and $I_{S4} = 2.2 \times 10^{-14}\,\text{A}$. Determine the required values of x and $(1 - x)$ of the potentiometer to compensate for the transistor mismatches.

14.26 The bipolar diff-amp in Figure 14.22 in the text is biased at $I_Q = 500\,\mu\text{A}$. Assume all transistors are matched, with $I_S = 10^{-14}\,\text{A}$. Let $R_1 = R_2 = 500\,\Omega$, and assume R_x is a $50\,\text{k}\Omega$ potentiometer. If the wiper arm of the potentiometer is off center such that $x = 15\,\text{k}\Omega$ and $(1 - x) = 35\,\text{k}\Omega$, determine the ratio of i_{C1}/i_{C2}. What is the corresponding offset voltage?

Section 14.5 Input Bias Current

D14.27 An op-amp used in a voltage follower configuration is ideal except that the input bias currents are $I_{B1} = I_{B2} = 1\,\mu\text{A}$. The source driving the voltage follower has an output resistance of $10\,\text{k}\Omega$. (a) Find the output voltage due to the bias current effects when $v_I = 0$. (b) Can the circuit be designed to compensate for the input bias currents? If so, how?

14.28 In the differential amplifier in Figure P14.7, the op-amp is ideal except that the average input bias current is $I_B = 10\,\mu A$ and the input offset current is $I_{OS} = 3\,\mu A$. If $v_{i1} = v_{i2} = 0$, determine the worst-case output voltage v_O due to the input bias current effects.

D14.29 The op-amp bias currents for the circuit in Figure P14.23 are equal at $I_{B1} = I_{B2} = 1\,\mu A$. (a) Find the worst-case output voltages v_{O1} and v_{O2} for $v_I = 0$. (b) Design input bias current compensation circuit(s) to adjust both v_{O1} and v_{O2} to zero when $v_I = 0$.

14.30 (a) For the integrator circuit in Figure P14.30, let the input bias currents be $I_{B1} = I_{B2} = 0.1\,\mu A$. Assume that switch S opens at $t = 0$. Derive an expression for the output voltage versus time for $v_I = 0$. (b) Plot v_O versus time for $0 \le t \le 10\,s$. (c) Repeat part (b) for $I_{B1} = I_{B2} = 100\,pA$.

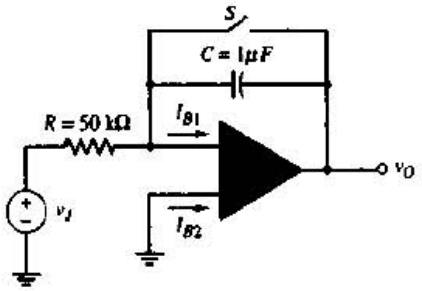


Figure P14.30

14.31 For the circuit in Figure P14.31, the op-amps are ideal except that each op-amp has input bias currents $I_{B1} = I_{B2} = 10\,\mu A$. (a) For $v_I = 0$ and $R_A = R_B = 0$, determine the worst-case values of v_{O1}, v_{O2}, and v_{O3} due to bias currents. (b) Determine the values of R_A and R_B for input bias current compensation. (c) If the average input bias current is $I_B = 10\,\mu A$ and the input offset current is $I_{OS} = 2\,\mu A$, determine the worst-case output values of v_{O1}, v_{O2}, and v_{O3} using the results of part (b).

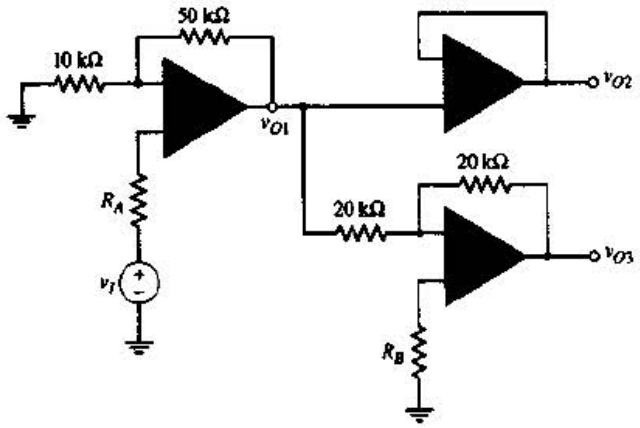


Figure P14.31

14.32 For each circuit in Figure P14.32, the input bias current is $I_B = 0.8\,\mu A$ the input offset current is $I_{OS} = 0.2\,\mu A$. (a) Determine the output voltage due to the average bias current I_B. (b) Determine the worst-case output voltage, including the effect of the input offset current.

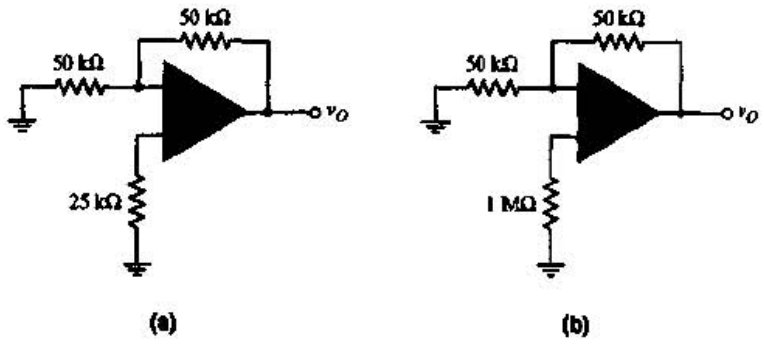


Figure P14.32

Sections 14.4 and 14.5 Offset Voltage and Input Bias Current: Total Effects

D14.33 For the op-amp in Figure P14.33, the input offset voltage is $V_{OS} = 10\,\text{mV}$, the input bias current is $I_B = 2\,\mu\text{A}$, and the input offset current is $I_{OS} = 0.2\,\mu\text{A}$. (a) Determine the worst-case, or maximum, output voltage when $v_I = 0$. (b) Design compensation circuit(s) to minimize v_O when $v_I = 0$.

D14.34 Consider the op-amp circuit in Figure P14.34. (a) Find the value of R_2 needed for a $\pm 10\,\text{mV}$ offset voltage adjustment. (b) Determine R_1 to minimize bias current effects. (Assume $R_2 \gg R_1$.)

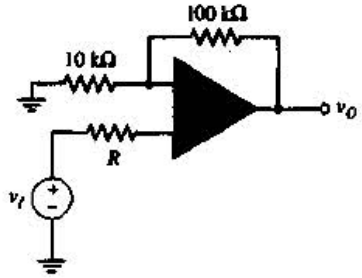


Figure P14.33

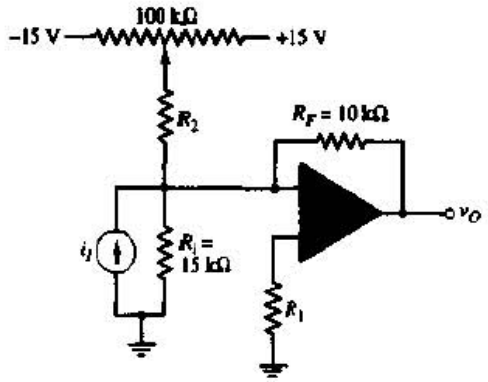


Figure P14.34

D14.35 For each op-amp in the circuit in Figure P14.23, the offset voltage is $V_{OS} = 10\,\text{mV}$ and the input bias currents are $I_{B1} = I_{B2} = 2\,\mu\text{A}$. (a) Find the worst-case output voltages v_{O1} and v_{O2} for $v_I = 0$. (b) Design compensation circuits to adjust both v_{O1} and v_{O2} to zero when $v_I = 0$.

D14.36 The op-amps in the circuit in Figure P14.31 have an offset voltage of $V_{OS} = 5\,\text{mV}$, and average input bias current of $I_B = 5\,\mu\text{A}$, and an input offset current of $I_{OS} = 1\,\mu\text{A}$. (a) For $v_I = 0$ and $R_A = R_B = 0$, determine the worst-case output voltages v_{O1}, v_{O2}, and v_{O3}. (b) Design compensation circuits to minimize the effects of the offset voltage and input bias current.

14.37 Each op-amp in Figure P14.32 has an offset voltage of $V_{OS} = 2\,\text{mV}$, an average input bias current of $I_B = 500\,\text{nA}$, and an input offset current of $I_{OS} = 100\,\text{nA}$. Determine the worst-case output voltage for each circuit.

Section 14.6 Additional Nonideal Effects

14.38 For each op-amp in Figure P14.32, the input offset voltage is $V_{OS} = 2\,\text{mV}$ at $T = 25\,^\circ\text{C}$ and the input offset voltage temperature coefficient is $\text{TC}v_{OS} = 6.7\,\mu\text{V}/^\circ\text{C}$. Find the output voltage v_O due to the input offset voltage effects at: (a) $T = 25\,^\circ\text{C}$ and (b) $T = 50\,^\circ\text{C}$.

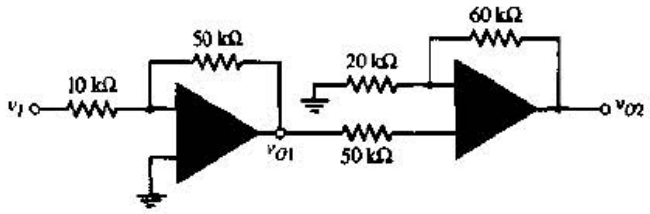


Figure P14.39

14.39 The input offset voltage in each op-amp in Figure P14.39 is $V_{OS} = 1\,\text{mV}$ at $T = 25\,^\circ\text{C}$ and the input offset voltage coefficient is $\text{TC}v_{OS} = 3.3\,\mu\text{V}/^\circ\text{C}$. Find the worst-case output voltages v_{O1} and v_{O2} at: (a) $T = 25\,^\circ\text{C}$ and (b) $T = 50\,^\circ\text{C}$.

14.40 For each op-amp in Figure P14.32, the input bias current is $I_B = 500\,\text{nA}$ at $T = 25\,^\circ\text{C}$, the input offset current is $I_{OS} = 200\,\text{nA}$ at $T = 25\,^\circ\text{C}$, the input bias current temperature coefficent is $8\,\text{nA}/^\circ\text{C}$, and the input offset current temperature coefficient is $2\,\text{nA}/^\circ\text{C}$. (a) Find the output voltage due to the average input bias currents at $T = 25\,^\circ\text{C}$. (b) Find the worst-case output voltage due to the input bias current and input offset current at $T = 25\,^\circ\text{C}$. (c) Repeat parts (a) and (b) for $T = 50\,^\circ\text{C}$.

14.41 For each op-amp in Figure P14.39, the input bias current is $I_B = 2\,\mu\text{A}$ at $T = 25\,^\circ\text{C}$, the input offset current is $I_{OS} = 0.2\,\mu\text{A}$ at $T = 25\,^\circ\text{C}$, the input bias current temperature coefficient is $20\,\text{nA}/^\circ\text{C}$, and the input offset current temperature coefficient is $5\,\text{nA}/^\circ\text{C}$. (a) Find the worst-case output voltages v_{O1} and v_{O2} due to the average input bias currents at $T = 25\,^\circ\text{C}$. (b) Find the worst-case output voltages v_{O1} and v_{O2} due to the input bias currents and input offset current at $T = 25\,^\circ\text{C}$. (c) Repeat parts (a) and (b) for $T = 50\,^\circ\text{C}$.

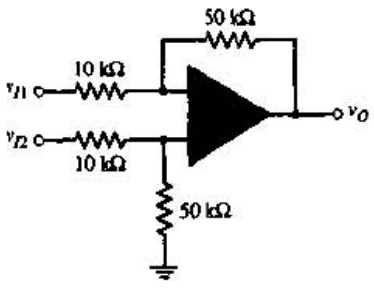


Figure P14.42

14.42 The op-amp in the diff-amp in Figure P14.42 is ideal. If the tolerance of each resistor is ±2%, determine the minimum value of CMRR_{dB}.

14.43 If the tolerances of each resistor in the diff-amp in Figure P14.42 are ±x%, what is the maximum value of x if the minimum CMRR_{dB} is: (a) 90 dB and (b) 60 dB.

COMPUTER SIMULATION PROBLEMS

14.44 Consider the reference circuit and gain stage of the 741 op-amp in Figure 13.7. Using a computer analysis, determine the slew rate of the gain stage.

14.45 The equivalent circuit of the all-CMOS MC14573 op-amp was given in Figure 13.14. Using a computer analysis, determine the slew rate of the op-amp, assuming $C_1 = 12\,\text{pF}$. Use the transistor and circuit parameters given in Example 13.8 and 13.9.

14.46 A basic bipolar input diff-amp stage is shown in Figure 14.22. Assume the circuit parameters are: $I_Q = 0.2\,\text{mA}$, $V^+ = 10\,\text{V}$, $V^- = -10\,\text{V}$, and $R_1 = R_2 = 500\,\Omega$. Let R_x be a $100\,\text{k}\Omega$ potentiometer and assume transistor Early voltages of 80 V. (a) Plot the collector voltage at Q_4 as a function of the wiper arm position. (b) Assume the I_S parameters of Q_1 and Q_2 vary such that Q_1 and Q_2 are mismatched by ±5%. Repeat part (a). (c) Repeat part (b) for a ±5% mismatch in Q_3 and Q_4.

14.47 Consider the input stage and bias circuit of the 741 op-amp in Figure 13.5. Assume the transistor Early voltages are 50 V. Using a computer analysis, determine the diff-amp common-mode rejection ratio.

CHAPTER

15

Applications and Design of Integrated Circuits

15.0 PREVIEW

In Chapter 9, we introduced the ideal operational amplifier and analyzed and designed basic op-amp circuits. In this chapter, we consider additional applications and designs of op-amp and comparator circuits that may be fabricated as integrated circuits. A comparator is essentially an op-amp operated in an open-loop configuration with either a high or low saturated output signal.

A general goal of this chapter is to increase our skill at designing electronic circuits to meet particular specifications and to perform particular functions.

Five types of circuits are considered. These circuits and their purpose are as follows:

1. *Active filters.* The primary functions of a filter are transmission of the desired frequency components of an input signal and attenuation of any undesired frequency components.
2. *Oscillators.* These circuits provide sinusoidal signals at a specified frequency for communication systems, for example.
3. *Multivibrator circuits.* Some electronic systems, for example, digital systems, require signals with particular waveforms, such as square-wave, triangular-wave, or single-pulse signals. Multivibrator circuits generate these types of signals.
4. *Power amplifiers.* An IC power amplifier usually consists of a high-gain small-signal amplifier in cascade with a class-AB output stage.
5. *Voltage regulators.* This circuit establishes a relatively constant dc voltage from an ac signal source.

We present three examples of integrated circuit power amplifiers. The IC power amplifier usually consists of a high-gain small-signal amplifier in cascade with a class-AB output stage. The output stage and feedback may be part of the integrated circuit, or may be external to the chip.

In the last section, we discuss the basis of voltage regulator circuits. The voltage regulator generally consists of an amplifier and other basic circuits and it uses feedback techniques. We will discuss one example of a basic voltage regulator IC.

15.1 ACTIVE FILTERS

An important application of op-amp is the **active filter**. The word filter refers to the process of removing undesired portions of the frequency spectrum. The word *active* implies the use of one or more active devices, usually an operational amplifier, in the filter circuit. As an example of the application of op-amps in the area of active filters, we will discuss the Butterworth filter. The discussion is only an introduction to the subject of filter theory design.

Two advantages of active filters over passive filters are:

1. The maximum gain or the maximum value of the transfer function may be greater than unity.
2. The loading effect is minimal, which means that the output response of the filter is essentially independent of the load driven by the filter.

15.1.1 Active Network Design

From our discussions of frequency response in Chapter 7, we know that *RC* networks form filters. Figure 15.1(a) is a simple example of a coupling-capacitor circuit. The voltage transfer function for this circuit is

$$T(s) = \frac{V_o(s)}{V_i(s)} = \frac{R}{R + \frac{1}{sC}} = \frac{sRC}{1 + sRC} \tag{15.1}$$

The Bode plot of the voltage gain magnitude $|T(j\omega)|$ is shown in Figure 15.1(b). The circuit is called a **high-pass filter**.

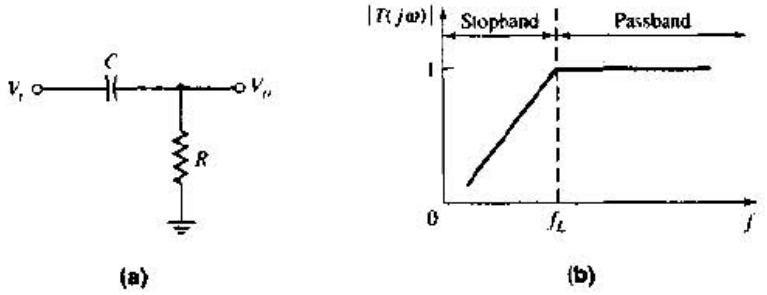


Figure 15.1 (a) Simple high-pass filter and (b) Bode plot of transfer function magnitude

Figure 15.2(a) is another example of a simple RC network. Here, the voltage transfer function is

$$T(s) = \frac{V_o(s)}{V_i(s)} = \frac{\frac{1}{sC}}{\frac{1}{sC} + R} = \frac{1}{1 + sRC} \tag{15.2}$$

The Bode plot of the voltage gain magnitude $|T(j\omega)|$ for this circuit is shown in Figure 15.2(b). This circuit is called a **low-pass filter**.

Although these circuits both perform a basic filtering function, they may suffer from loading effects, substantially reducing the maximum gain from the

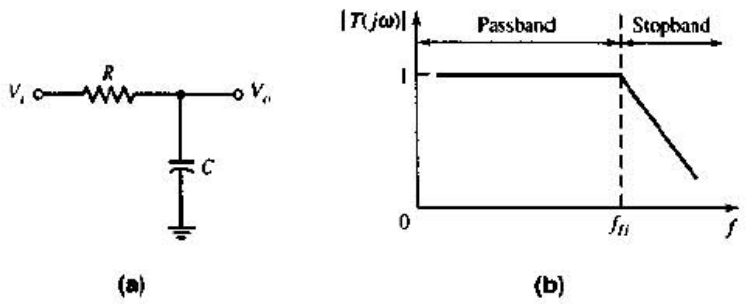


Figure 15.2 (a) Simple low-pass filter and (b) Bode plot of transfer function magnitude

unity value shown in Figures 15.1(b) and 15.2(b). Also, the cutoff frequencies f_L and f_H may change when a load is connected to the output. The loading effect can essentially be eliminated by using a voltage follower as shown in Figure 15.3. In addition, a noninverting amplifier configuration can be incorporated to increase the gain, as well as eliminate the loading effects.

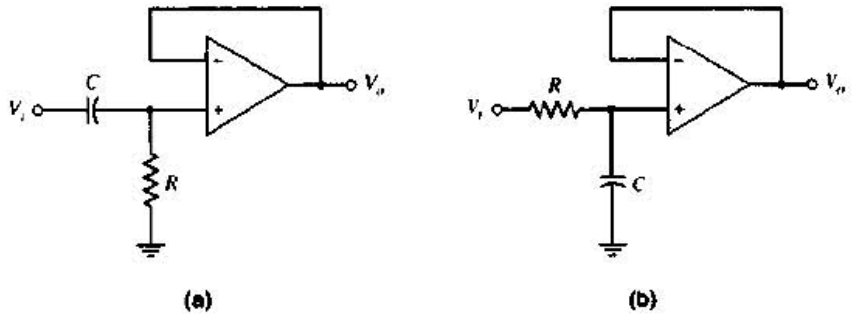


Figure 15.3 (a) High-pass filter with voltage follower and (b) low-pass filter with voltage follower

These two filter circuits are called one-pole filters; the slope of the voltage gain magnitude curve outside the passband is 6 dB/octave or 20 dB/decade. This characteristic is called the rolloff. The rolloff becomes sharper or steeper with higher-order filters and is usually one of the specifications given for active filters.

Two other categories of filters are **bandpass** and **band-reject**. The desired ideal frequency characteristics are shown in Figure 15.4.

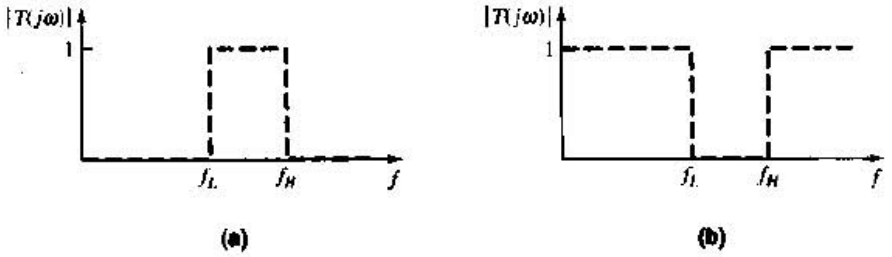


Figure 15.4 Ideal frequency characteristics: (a) bandpass filter and (b) band-reject filter

15.1.2 General Two-Pole Active Filter

Consider Figure 15.5 with admittances Y_1 through Y_4 and an ideal voltage follower. We will derive the transfer function for the general network and will then apply specific admittances to obtain particular filter characteristics.

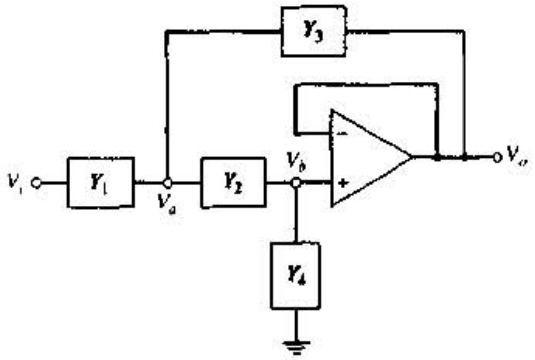


Figure 15.5 General two-pole active filter

A KCL equation at node V_a yields

$$(V_i - V_a)Y_1 = (V_a - V_b)Y_2 + (V_a - V_o)Y_3 \tag{15.3}$$

A KCL equation at node V_b produces

$$(V_a - V_b)Y_2 = V_b Y_4 \tag{15.4}$$

From the voltage follower characteristics, we have $V_b = V_o$. Therefore, Equation (15.4) becomes

$$V_a = V_b\left(\frac{Y_2 + Y_4}{Y_2}\right) = V_o\left(\frac{Y_2 + Y_4}{Y_2}\right) \tag{15.5}$$

Substituting Equation (15.5) into (15.3) and again noting that $V_b = V_o$, we have

$$\begin{aligned} V_i Y_1 + V_o(Y_2 + Y_3) &= V_a(Y_1 + Y_2 + Y_3) \\ &= V_o\left(\frac{Y_2 + Y_4}{Y_2}\right)(Y_1 + Y_2 + Y_3) \end{aligned} \tag{15.6}$$

Multiplying Equation (15.6) by Y_2 and rearranging terms, we get the following expression for the transfer function:

$$T(s) = \frac{V_o(s)}{V_i(s)} = \frac{Y_1 Y_2}{Y_1 Y_2 + Y_4(Y_1 + Y_2 + Y_3)} \tag{15.7}$$

To obtain a low-pass filter, both Y_1 and Y_2 must be conductances, allowing the signal to pass into the voltage follower at low frequencies. If element Y_4 is a capacitor, then the output rolls off at high frequencies.

To produce a two-pole function, element Y_3 must also be a capacitor. On the other hand, if elements Y_1 and Y_2 are capacitors, then the signal will be blocked at low frequencies but will be passed into the voltage follower at high frequencies, resulting in a high-pass filter. Therefore, admittances Y_3 and Y_4 must both be conductances to produce a two-pole high-pass transfer function.

15.1.3 Two-Pole Low-Pass Butterworth Filter

To form a low-pass filter, we set $Y_1 = G_1 = 1/R_1$, $Y_2 = G_2 = 1/R_2$, $Y_3 = sC_3$, and $Y_4 = sC_4$, as shown in Figure 15.6. The transfer function, from Equation (15.7), becomes

$$T(s) = \frac{V_o(s)}{V_i(s)} = \frac{G_1 G_2}{G_1 G_2 + sC_4(G_1 + G_2 + sC_3)} \tag{15.8}$$

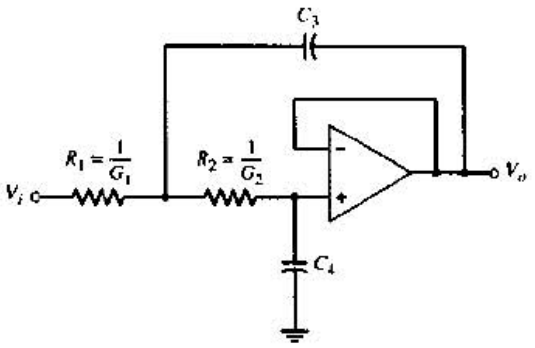


Figure 15.6 General two-pole low-pass filter

At zero frequency, $s = j\omega = 0$ and the transfer function is

$$T(s = 0) = \frac{G_1 G_2}{G_1 G_2} = 1 \tag{15.9}$$

In the high-frequency limit, $s = j\omega \to \infty$ and the transfer function approaches zero. This circuit therefore acts as a low-pass filter.

A **Butterworth filter** is a **maximally flat magnitude filter**. The transfer function is designed such that the magnitude of the transfer function is as flat as possible within the passband of the filter. This objective is achieved by taking the derivatives of the transfer function with respect to frequency and setting as many as possible equal to zero at the center of the passband, which is at zero frequency for the low-pass filter.

Let $G_1 = G_2 \equiv G = 1/R$. The transfer function is then

$$T(s) = \frac{\frac{1}{R^2}}{\frac{1}{R^2} + sC_4\left(\frac{2}{R} + sC_3\right)} = \frac{1}{1 + sRC_4(2 + sRC_3)} \tag{15.10}$$

We define time constants at $\tau_3 = RC_3$ and $\tau_4 = RC_4$. If we then set $s = j\omega$, we obtain

$$T(j\omega) = \frac{1}{1 + j\omega\tau_4(2 + j\omega\tau_3)} = \frac{1}{(1 - \omega^2\tau_3\tau_4) + j(2\omega\tau_4)} \tag{15.11}$$

The magnitude of the transfer function is therefore

$$|T(j\omega)| = \left[(1 - \omega^2\tau_3\tau_4)^2 + (2\omega\tau_4)^2\right]^{-1/2} \tag{15.12}$$

For a maximally flat filter (that is, a filter with a minimum rate of change), which defines a Butterworth filter, we set

$$\left.\frac{d|T|}{d\omega}\right|_{\omega=0} = 0 \tag{15.13}$$

Taking the derivative, we find

$$\frac{d|T|}{d\omega} = -\frac{1}{2}[(1-\omega^2\tau_3\tau_4)^2 + (2\omega\tau_4)^2]^{-3/2}[-4\omega\tau_3\tau_4(1-\omega^2\tau_3\tau_4) + 8\omega\tau_4^2] \tag{15.14}$$

Setting the derivative equal to zero at $\omega = 0$ yields

$$\begin{aligned}\left.\frac{d|T|}{d\omega}\right|_{\omega=0} &= \left[-4\omega\tau_3\tau_4(1-\omega^2\tau_3\tau_4) + 8\omega\tau_4^2\right] \\ &= 4\omega\tau_4\left[-\tau_3(1-\omega^2\tau_3\tau_4) + 2\tau_4\right]\end{aligned} \tag{15.15}$$

Equation (15.15) is satisfied when $2\tau_4 = \tau_3$, or

$$C_3 = 2C_4 \tag{15.16}$$

For this condition, the transfer magnitude is, from Equation (15.12),

$$|T| = \frac{1}{\left[1 + 4(\omega\tau_4)^4\right]^{1/2}} \tag{15.17}$$

The 3 dB, or cutoff, frequency occurs when $|T| = 1/\sqrt{2}$, or when $4(\omega_{3\,\text{dB}}\tau_4)^4 = 1$. We then find that

$$\omega_{3\,\text{dB}} = 2\pi f_{3\,\text{dB}} = \frac{1}{\tau_4\sqrt{2}} = \frac{1}{\sqrt{2}RC_4} \tag{15.18}$$

In general, we can write the cutoff frequency in the form

$$\omega_{3\,\text{dB}} = \frac{1}{RC} \tag{15.19}$$

Finally, comparing Equations (15.19), (15.18), and (15.16) yields

$$C_4 = 0.707C \tag{15.20(a)}$$

and

$$C_3 = 1.414C \tag{15.20(b)}$$

The two-pole low-pass Butterworth filter is shown in Figure 15.7(a). The Bode plot of the transfer function magnitude is shown in Figure 15.7(b). From Equation (15.17), the magnitude of the voltage transfer function for the two-pole low-pass Butterworth filter can be written as

$$|T| = \frac{1}{\sqrt{1 + \left(\dfrac{f}{f_{3\,\text{dB}}}\right)^4}} \tag{15.21}$$

Equation (15.15) shows that the derivative of the voltage transfer function magnitude at $\omega = 0$ is zero even without setting $2\tau_4 = \tau_3$. However, the added condition of $2\tau_4 = \tau_3$ produces the maximally flat transfer characteristics of the Butterworth filter.

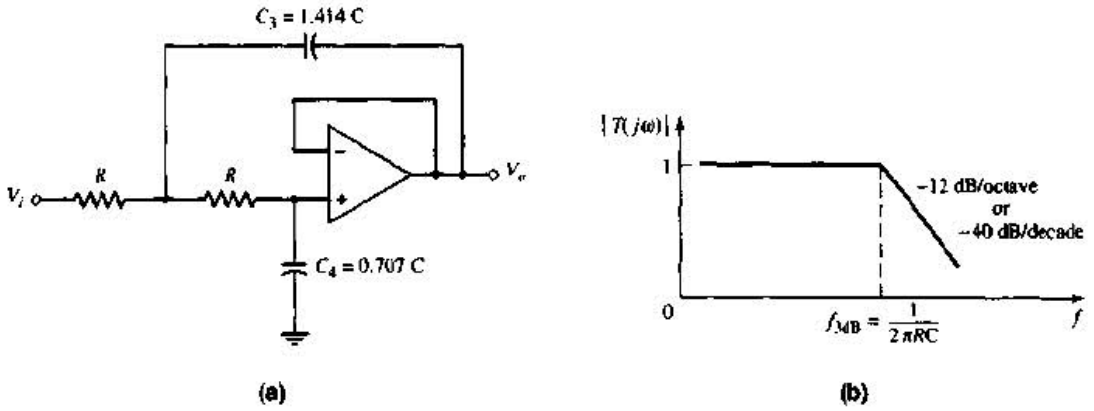


Figure 15.7 (a) Two-pole low-pass Butterworth filter and (b) Bode plot, transfer function magnitude

Design Example 15.1 **Objective:** Design a two-pole low-pass Butterworth filter for an audio amplifier application.

Consider the circuit shown in Figure 15.7(a). Design the circuit such that the bandwidth is 20 kHz.

Solution: From Equation (15.19), we have

$$f_{3\,dB} = \frac{1}{2\pi RC}$$

or

$$RC = \frac{1}{2\pi f_{3\,dB}} = \frac{1}{2\pi(20 \times 10^3)} = 7.96 \times 10^{-6}$$

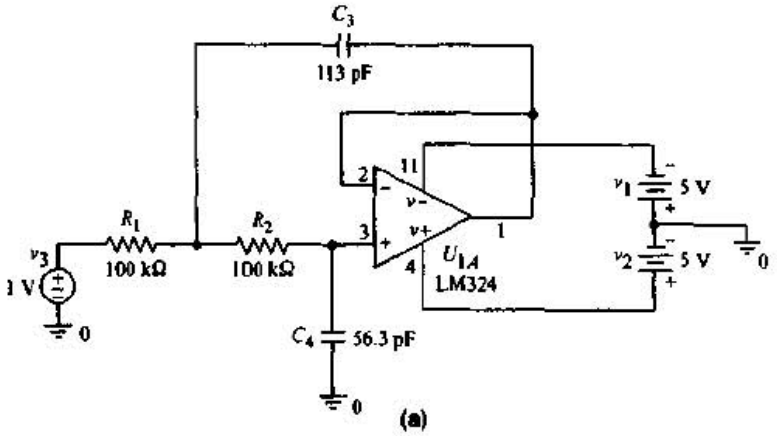
If we let $R = 100\,k\Omega$, then $C = 79.6\,pF$, which means tht $C_3 = 1.414C = 113\,pF$ and $C_4 = 0.707C = 56.3\,pF$.

Comment: These resistance and capacitance values are generally too large to be fabricated conveniently on an IC. Instead, discrete resistors and capacitors, in conjunction with the IC op-amp, would need to be used.

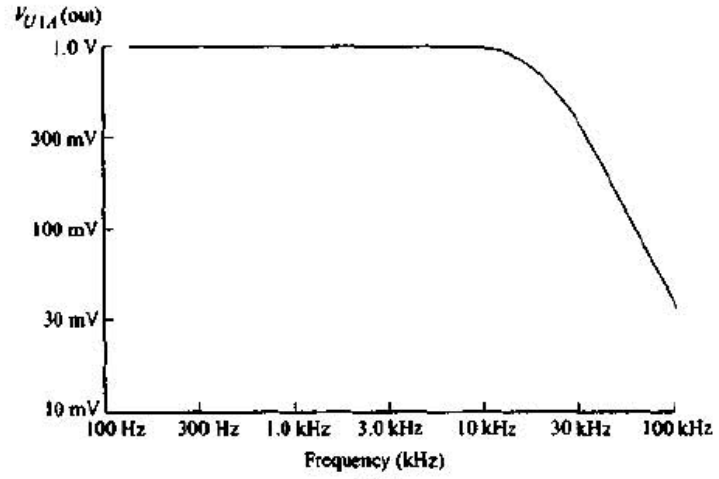
Computer Simulation Verification: Figure 15.8(a) shows the circuit used in the computer simulation. A standard LM324 op-amp is used. A 1 V sinusoidal input signal is applied. Figure 15.8(b) shows the output signal as a function of frequency. The 3 dB frequency, the frequency at which the output signal is 0.707 V, is 20 kHz, as designed. The slope of the rolloff at high frequency is also −12 dB/octave, as predicted from theory.

15.1.4 Two-Pole High-Pass Butterworth Filter

To form a high-pass filter, the resistors and capacitors are interchanged from those in the low-pass filter. A two-pole high-pass Butterworth filter is shown in Figure 15.9(a). The analysis proceeds exactly the same as in the last section,

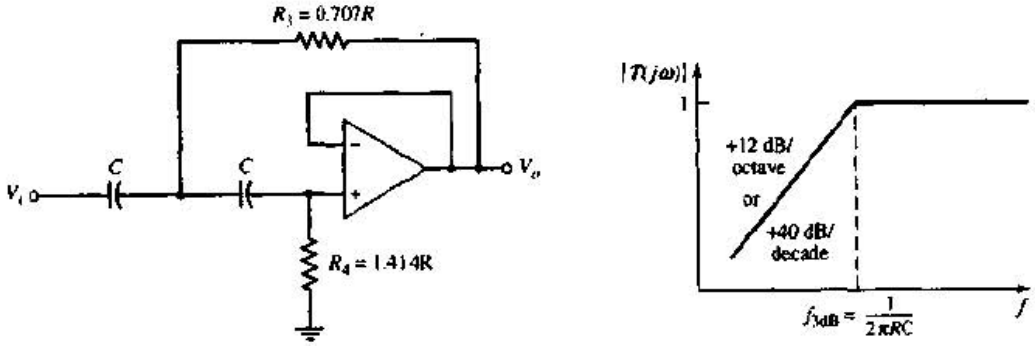


(a)



(b)

Figure 15.8 (a) Circuit used in the computer simulation of the design in Example 15.1; (b) output versus frequency



(a) (b)

Figure 15.9 (a) Two-pole high-pass Butterworth filter and (b) Bode plot, transfer function magnitude

except that the derivative is set equal to zero at $s = j\omega = \infty$. Also, the two capacitors are set equal to each other. The 3 dB or cutoff frequency can be written in the general form

$$\omega_{3\text{dB}} = 2\pi f_{3\text{dB}} = \frac{1}{RC} \tag{15.22}$$

We find that $R_3 = 0.707R$ and $R_4 = 1.414R$. The magnitude of the voltage transfer function for the two-pole high-pass Butterworth is

$$|T| = \frac{1}{\sqrt{1 + \left(\frac{f_{3\text{dB}}}{f}\right)^4}} \tag{15.23}$$

The Bode plot of the transfer function magnitude for the two-pole high-pass Butterworth filter is shown in Figure 15.9(b).

15.1.5 Higher-Order Butterworth Filters

The filter order is the number of poles and is usually dictated by the application requirements. An N-pole active low-pass filter has a high-frequency rolloff rate of $N \times 6$ dB/octave. Similarly, the response of an N-pole high-pass filter increases at a rate of $N \times 6$ dB/octave, up to the cutoff frequency. In each case, the 3 dB frequency is defined as

$$f_{3\text{dB}} = \frac{1}{2\pi RC} \tag{15.24}$$

The magnitude of the voltage transfer function for a Butterworth Nth-order low-pass filter is

$$|T| = \frac{1}{\sqrt{1 + \left(\frac{f}{f_{3\text{dB}}}\right)^{2N}}} \tag{15.25}$$

For a Butterworth Nth-order high-pass filter, the voltage transfer function magnitude is

$$|T| = \frac{1}{\sqrt{1 + \left(\frac{f_{3\text{dB}}}{f}\right)^{2N}}} \tag{15.26}$$

Figure 15.10(a) shows a three-pole low-pass Butterworth filter. The three resistors are equal, and the relationship between the capacitors is found by taking the first and second derivatives of the voltage gain magnitude with respect to frequency and setting those derivatives equal to zero at $s = j\omega = 0$. Figure 15.10(b) shows a three-pole high-pass Butterworth filter. In this case, the three capacitors are equal and the relationship between the resistors is also found through the derivatives.

Higher-order filters can be created by adding additional RC networks. However, the loading effect on each additional RC circuit becomes more severe. The usefulness of active filters is realized when two or more op-amp filter circuits are cascaded to produce one large higher-order active filter.

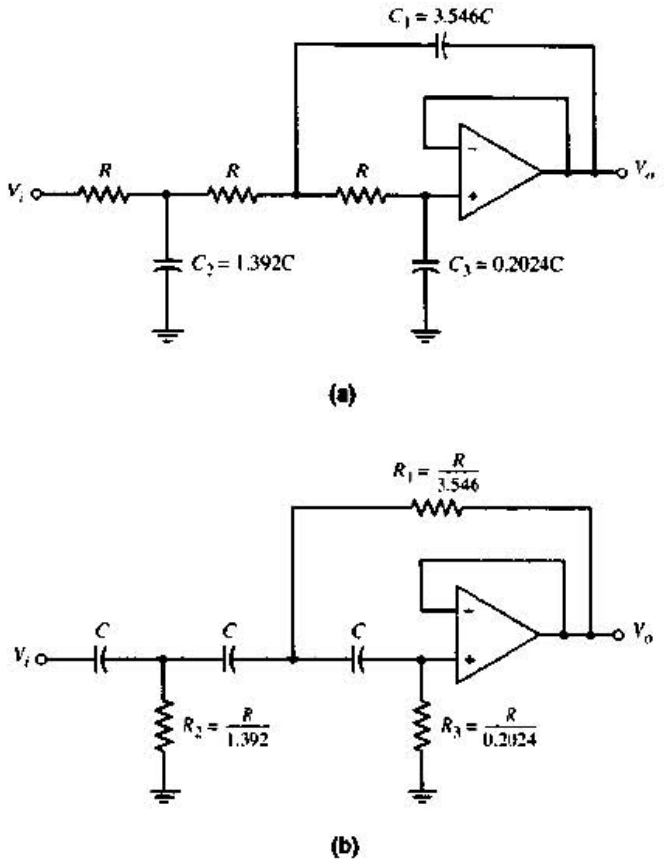


Figure 15.10 (a) Three-pole low-pass Butterworth filter and (b) three-pole high-pass Butterworth filter

Because of the low output impedance of the op-amp, there is virtually no loading effect between cascaded stages.

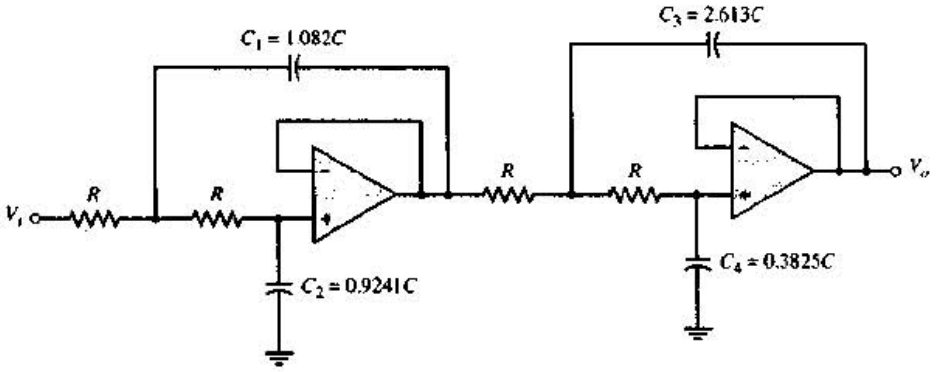
Figure 15.11(a) shows a four-pole low-pass Butterworth filter. The maximally flat response of this filter is *not* obtained by simply cascading two two-pole filters. The relationship between the capacitors is found through the first three derivatives of the transfer function. The four-pole high-pass Butterworth filter is shown in Figure 15.11(b).

Higher-order filters can be designed but are not considered here. Bandpass and band-reject filters use similar circuit configurations.

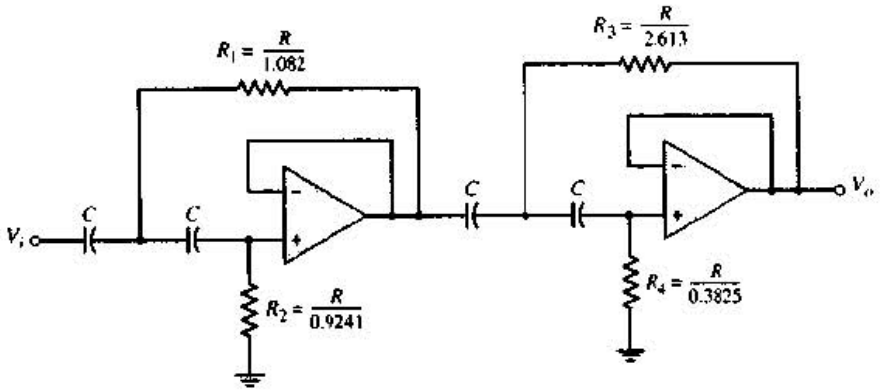
Test Your Understanding

D15.1 Design a three-pole low-pass Butterworth active filter with a cutoff frequency of 10 kHz and unity gain at low frequency. What is the magnitude of the voltage transfer function at 20 kHz? (Ans. For example, $R = 1.59\,\text{k}\Omega$, $C_1 = 0.03546\,\mu\text{F}$, $C_2 = 0.01392\,\mu\text{F}$, $C_3 = 0.002024\,\mu\text{F}$, $|T| = -18.1\,\text{dB}$)

D15.2 Design a four-pole high-pass Butterworth active filter with a 3 dB frequency of 50 kHz. Determine the frequency at which the voltage transfer function magnitude is 1 percent of its maximum value. (Ans. For example, $C = 0.001\,\mu\text{F}$, $R_1 = 2.94\,\text{k}\Omega$, $R_2 = 3.44\,\text{k}\Omega$, $R_3 = 1.22\,\text{k}\Omega$, $R_4 = 8.31\,\text{k}\Omega$, $f \cong 15.8\,\text{kHz}$)



(a)



(b)

Figure 15.11 (a) Four-pole low-pass Butterworth filter and (b) four-pole high-pass Butterworth filter

15.3 One-, two-, three-, and four-pole low-pass Butterworth active filters are all designed with a cutoff frequency of 10 kHz and unity gain at low frequency. Determine the voltage transfer function magnitude, in dB, at 12 kHz for each filter. (Ans. −3.87 dB, −4.88 dB, −6.0 dB, and −7.24 dB)

15.1.6 Switched-Capacitor Filter

The results of Example 15.1 demonstrated that discrete resistors and capacitors may be needed in active filters, since the required resistance and capacitance values are too large to be conveniently fabricated on a monolithic IC chip. Large-value resistors ($R > 10\,k\Omega$) require a large chip area, and the absolute-value tolerance is difficult to maintain. In addition, the maximum capacitance for a monolithic IC capacitor is approximately 100 pF, which is also limited by the large chip area required and the absolute-value tolerance. In these cases, accurate RC time constants may be difficult to maintain.

Conventional active filters usually combine an IC op-amp and discrete resistors and capacitors. However, even with discrete resistors and capacitors,

standard components may not be available for the design of a specific cutoff frequency. Design accuracy for a specific cutoff frequency may therefore have to be sacrificed.

Switched-capacitor filters have the advantage of an all-IC circuit. The filter uses small capacitance values and realizes large effective resistance values by using a combination of capacitors and MOS switching transistors.

The Basic Principle of the Switched Capacitor

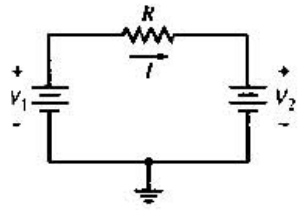


Figure 15.12 Voltages applied to resistor terminals, and the current

Figure 15.12 shows a simple circuit in which voltages V_1 and V_2 are applied at the terminals of a resistance R. The current in the resistor is

$$I = \frac{V_1 - V_2}{R} \tag{15.27(a)}$$

The resistance is therefore

$$R = \frac{V_1 - V_2}{I} \tag{15.27(b)}$$

Since the current is the rate of charge flow, Equation (15.27(b)) states that the resistance is a voltage difference divided by the rate of charge flow. We use this basic definition in switched-capacitor circuits.

The circuit in Figure 15.13(a) consists of two MOSFETs and a capacitor. A two-phase clock provides complementary but nonoverlapping ϕ_1 and ϕ_2 gate pulses, as shown in Figure 15.13(b). When a clock pulse is high, the corresponding transistor turns on; when the gate pulse is low, the transistor is off.

When ϕ_1 goes high, M_1 turns on and capacitor C charges up to V_1. When ϕ_2 goes high, M_2 turns on and capacitor C discharges to V_2 (assuming $V_1 > V_2$). The amount of charge transferred during this process is $Q = C(V_1 - V_2)$ and the transfer occurs during one clock period T_C. The equivalent current is then

$$I_{eq} = \frac{Q}{T_C} = \frac{C(V_1 - V_2)}{T_C} = f_C C(V_1 - V_2) = \frac{V_1 - V_2}{R_{eq}} \tag{15.28}$$

where f_C is the clock frequency and R_{eq} is the equivalent resistance given by

$$R_{eq} = \frac{1}{f_C C} \tag{15.29}$$

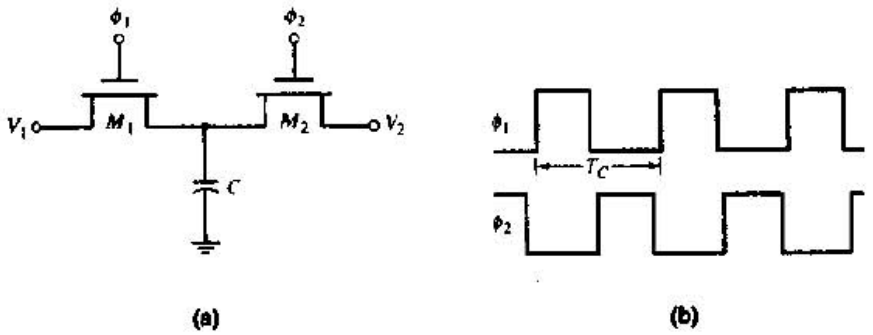


Figure 15.13 (a) Capacitor with two switching MOSFETs and (b) two-phase clock pulses

Using this technique, we can simulate an equivalent resistance by alternately charging and discharging a capacitor between two voltage levels. A large equivalent resistance can be simulated by using a small capacitance and an appropriate clock frequency. The circuit in Figure 15.13(a) is therefore called a switched-capacitor circuit.

Example 15.2 **Objective:** Determine the clock frequency required to simulate a specific resistance.

Consider the switched-capacitor circuit in Figure 15.13(a). Assume a capacitance of $C = 20\,\text{pF}$. Determine the clock frequency required to simulate a $1\,\text{M}\Omega$ resistance.

Solution: From Equation (15.29), we find that

$$f_C = \frac{1}{CR_{eq}} = \frac{1}{(20 \times 10^{-12})(10^6)} \Rightarrow 50\,\text{kHz}$$

Comment: A very large resistance can be readily simulated by a small capacitance and a reasonable clock frequency.

Various classes of active filters, such as low-pass, high-pass, bandpass, and band-reject circuits, can be implemented by the switched-capacitor technique, which then results in an all-capacitor filter circuit.

Example of Switched-Capacitor Filter

Consider the one-pole low-pass filter in Figure 15.14(a). The transfer function is

$$T(s) = \frac{V_o(s)}{V_{in}(s)} = -\frac{R_F}{R_1}\frac{1}{1 + sR_FC_F} \tag{15.30}$$

and the cutoff frequency is

$$f_{3\text{dB}} = \frac{1}{2\pi R_FC_F} \tag{15.31}$$

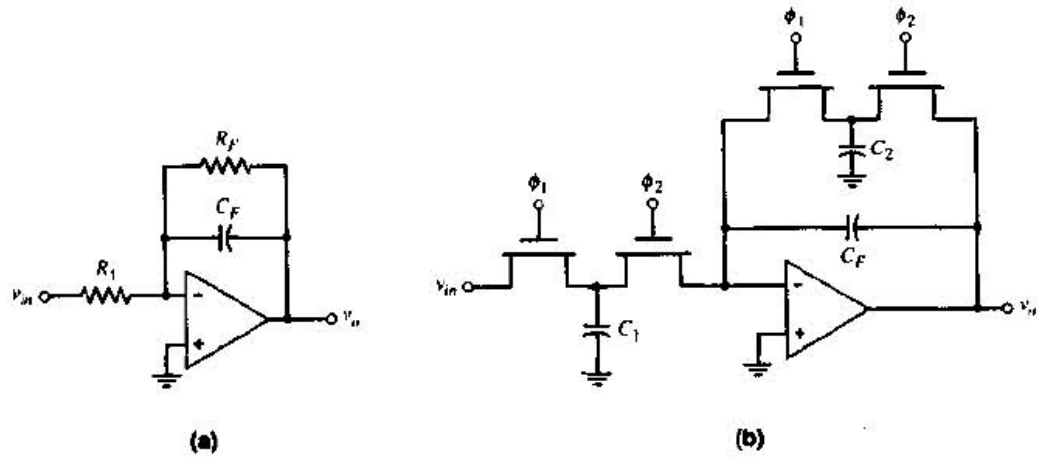


Figure 15.14 (a) One-pole low-pass filter and (b) equivalent switched-capacitor circuit

If a 10 kHz cutoff frequency is required and if $C_F = 10\,\text{pF}$, then the R_F resistance required is approximately 1.6 MΩ. In addition, if a gain of −10 is desired, then resistance R_1 must be 160 kΩ.

The equivalent switched-capacitor filter is shown in Figure 15.14(b). The transfer function is still given by Equation (15.30), where $R_{Feq} = 1/(f_C C_2)$ and $R_{1eq} = 1/(f_C C_1)$. The transfer function is then

$$T(j\omega) = -\frac{(1/f_C C_2)}{(1/f_C C_1)} \cdot \frac{1}{1 + j\dfrac{(2\pi f)C_F}{f_C C_2}} = -\frac{C_1}{C_2} \cdot \frac{1}{1 + j\dfrac{f}{f_{3\text{dB}}}} \tag{15.32}$$

The low-frequency gain is $-C_1/C_2$, which is just the ratio of two capacitances, and the 3 dB frequency is

$$f_{3\text{dB}} = (f_C C_2)/(2\pi C_F)$$

which is also proportional to the ratio of two other capacitances. For MOS IC capacitance values of approximately 10 pF, the ratio tolerance is on the order of 0.1 percent. This means that switched-capacitor filter characteristics can be precisely controlled.

Design Example 15.3 **Objective:** Design a one-pole low-pass switched-capacitor filter.

Design the circuit in Figure 15.14(b) such that the low-frequency gain is −1 and the cutoff frequency is 1 kHz.

Solution: From Equation (15.32), the low-frequency gain is $-(C_1/C_2)$, and the capacitance ratio must be $(C_1/C_2) = 1$. From Equation (15.32), the cutoff frequency is

$$f_{3\text{dB}} = \frac{f_C C_2}{2\pi C_F}$$

If we set the clock frequency to $f_C = 10\,\text{kHz}$, then

$$\frac{C_2}{C_F} = \frac{2\pi f_{3\text{dB}}}{f_C} = \frac{2\pi(10^3)}{10 \times 10^3} = 0.628$$

Comment: Since the low-frequency gain and cutoff frequency are both functions of capacitor ratios, the absolute capacitor values can be designed for compatibility with IC fabrication.

This discussion of switched-capacitor filters is a short introduction to the topic and is intended only to show another application of operational amplifiers. Switched-capacitor filters are "sampled-data systems"; that is, the analog input signal is not transmitted through the circuit as a continuous signal but passes through the system as a series of pulses. The equivalent resistance given by Equation (15.29) is valid only for clock frequencies much greater than the analog input signal frequency. Switched-capacitor systems can be analyzed and designed by z-transform techniques.

Test Your Understanding

15.4 Simulate a 5 MΩ resistance using the circuit in Figure 15.13(a). What capacitor value and clock frequency are required? (Ans. For example, $C = 10\,\text{pF}$, $f_C = 20\,\text{kHz}$)

15.5 For the switched-capacitor circuit in Figure 15.14(b), the parameters are: $C_1 = 30\,\text{pF}$, $C_2 = 5\,\text{pF}$, and $C_F = 12\,\text{pF}$. The clock frequency is 100 kHz. Determine the low-frequency gain and the cutoff frequency. (Ans. $-C_1/C_2 = -6, f_{3\text{dB}} = 6.63\,\text{kHz}$)

15.2 OSCILLATORS

In this section, we will look at the basic principles of sine-wave oscillators. In our study of feedback in Chapter 12, we emphasized the need for negative feedback to provide a stable circuit. Oscillators, however, use positive feedback and, therefore, are actually nonlinear circuits in some cases. The analysis and design of oscillator circuits are divided into two parts. In the first part, the condition and frequency for oscillation are determined; in the second part, means for amplitude control is addressed. We consider only the first step in this section to gain insight into the basic operation of oscillators.

15.2.1 Basic Principles for Oscillation

The basic **oscillator** consists of an amplifier and a **frequency-selective network** connected in a feedback loop. Figure 15.15 shows a block diagram of the fundamental feedback circuit, in which we are implicitly assuming that negative feedback is employed. Although actual oscillator circuits do not have an input signal, we initially include one here to help in the analysis. In previous feedback circuits, we assumed the feedback transfer function β was independent of frequency. In oscillator circuits, however, β is the principal portion of the loop gain that is dependent on frequency.

For the circuit shown, the ideal closed-loop transfer function is given by

$$A_f(s) = \frac{A(s)}{1 + A(s)\beta(s)} \tag{15.33}$$

and the loop gain of the feedback circuit is

$$T(s) = A(s)\beta(s) \tag{15.34}$$

From our discussion of feedback in Chapter 12, we know that the loop gain $T(s)$ is positive for negative feedback, which means that the feedback

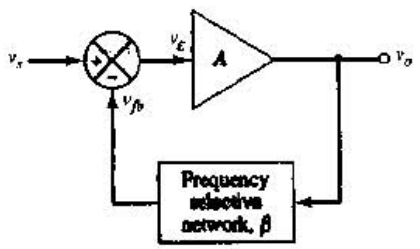


Figure 15.15 Block diagram of the fundamental feedback circuit

signal v_{fb} subtracts from the input signal v_s. If the loop gain $T(s)$ becomes negative, then the feedback signal phase causes v_{fb} to add to the input signal, increasing the error signal v_ε. If $T(s) = -1$, the closed-loop transfer function goes to infinity, which means that the circuit can have a finite output for a zero input signal.

As $T(s)$ approaches -1, an actual circuit becomes nonlinear, which means that the gain does not go to infinity. Assume that $T(s) \approx -1$ so that positive feedback exists over a particular frequency range. If a spontaneous signal (due to noise) is created at v_s in this frequency range, the resulting feedback signal v_{fb} is in phase with v_s, and the error signal v_ε is reinforced and increased. This reinforcement process continues at only those frequencies for which the total phase shift around the feedback loop is zero. Therefore, the condition for oscillation is that, at a specific frequency, we have

$$T(j\omega_o) = A(j\omega_o)\beta(j\omega_o) = -1 \tag{15.35}$$

The condition that $T(j\omega_o) = -1$ is called the **Barkhausen criterion**.

Equation (15.35) shows that two conditions must be satisfied to sustain oscillation:

1. The total phase shift through the amplifier and feedback network must be $N \times 360°$, where $N = 0, 1, 2, \ldots$.
2. The magnitude of the loop gain must be unity.

In the feedback circuit block diagram in Figure 15.15, we implicitly assume negative feedback. For an oscillator, the feedback transfer function, or the frequency-selective network, must introduce an additional 180 degree phase shift such that the net phase around the entire loop is zero. For the circuit to oscillate at a single frequency ω_o, the condition for oscillation, from Equation (15.35), should be satisfied at only that one frequency.

15.2.2 Phase-Shift Oscillator

An example of an op-amp oscillator is the **phase-shift oscillator**. One configuration of this oscillator circuit is shown in Figure 15.16. The basic amplifier of the circuit is the op-amp A_3, which is connected as an inverting amplifier with its output connected to a three-stage RC filter. The voltage followers in the circuit eliminate loading effects between each RC filter stage.

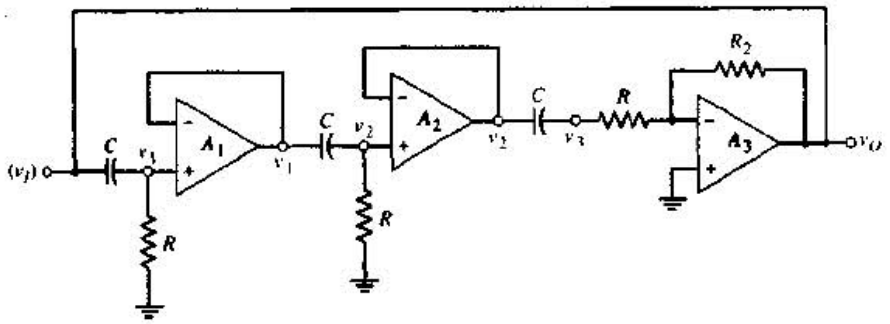


Figure 15.16 Phase-shift oscillator circuit with voltage-follower buffer stages

The inverting amplifier introduces a −180 degree phase shift, which means that each *RC* network must provide 60 degrees of phase shift to produce the 180 degrees required of the frequency-sensitive feedback network in order to produce positive feedback. Note that the inverting terminal of op-amp A_3 is at virtual ground; therefore, the *RC* network between op-amps A_2 and A_3 functions exactly as the other two *RC* networks. We assume that the frequency effects of the op-amps themselves occur at much higher frequencies than the response due to the *RC* networks. Also, to aid in the analysis, we assume an input signal (v_I) exists at one node as shown in the figure.

The transfer function of the first *RC* network is

$$v_1 = \left(\frac{sRC}{1 + sRC}\right)(v_I) \tag{15.36}$$

Since the *RC* networks are assumed to be identical, and since there is no loading effect of one *RC* stage on another, we have

$$\frac{v_3}{(v_I)} = \left(\frac{sRC}{1 + sRC}\right)^3 = \beta(s) \tag{15.37}$$

where $\beta(s)$ is the feedback transfer function. The amplifier gain $A(s)$ in Equation (15.33) and (15.34) is actually the magnitude of the gain, or

$$A(s) = \left|\frac{v_O}{v_3}\right| = \frac{R_2}{R}. \tag{15.38}$$

The loop gain is then

$$T(s) = A(s)\beta(s) = \left(\frac{R_2}{R}\right)\left(\frac{sRC}{1 + sRC}\right)^3 \tag{15.39}$$

From Equation (15.35), the condition for oscillation is that $|T(j\omega_o)| = 1$ and the phase of $T(j\omega_o)$ must be 180 degrees. When these requirements are satisfied, then v_O will equal (v_I) and a separate input signal will not be required.

If we set $s = j\omega$, Equation (15.39) becomes

$$\begin{aligned} T(j\omega) &= \left(\frac{R_2}{R}\right)\frac{(j\omega RC)^3}{(1 + j\omega RC)^3} \\ &= -\left(\frac{R_2}{R}\right)\frac{(j\omega RC)(\omega RC)^2}{\left[1 - 3\omega^2R^2C^2\right] + j\omega RC\left[3 - \omega^2R^2C^2\right]} \end{aligned} \tag{15.40}$$

To satisfy the condition $T(j\omega_o) = -1$, the imaginary component of Equation (15.40) must equal zero. Since the numerator is purely imaginary, the denominator must become purely imaginary, or

$$\left[1 - 3\omega_o^2R^2C^2\right] = 0$$

which yields

$$\omega_o = \frac{1}{\sqrt{3}\,RC} \tag{15.41}$$

where ω_o is the oscillation frequency. At this frequency, Equation (15.40) becomes

$$T(j\omega_o) = -\left(\frac{R_2}{R}\right)\frac{(j/\sqrt{3})(1/3)}{0 + (j/\sqrt{3})[3 - (1/3)]} = -\left(\frac{R_2}{R}\right)\left(\frac{1}{8}\right) \tag{15.42}$$

Consequently, the condition $T(j\omega_o) = -1$ is satisfied when

$$\frac{R_2}{R} = 8 \tag{15.43}$$

Equation (15.43) implies that if the magnitude of the inverting amplifier gain is greater than 8, the circuit will spontaneously begin oscillating and will sustain oscillation.

Example 15.4 **Objective:** Determine the oscillation frequency and required amplifier gain for a phase-shift oscillator.

Consider the phase-shift oscillator in Figure 15.16 with parameters $C = 0.1\,\mu F$ and $R = 1\,k\Omega$.

Solution: From Equation (15.41), the oscillation frequency is

$$f_o = \frac{1}{2\pi\sqrt{3}RC} = \frac{1}{2\pi\sqrt{3}(10^3)(0.1 \times 10^{-6})} = 919\,Hz$$

The minimum amplifier gain magnitude is 8 from Equation 15.43; therefore, the minimum value of R_2 is $8\,k\Omega$.

Comment: Higher oscillation frequencies can easily be obtained by using smaller capacitor values.

Using Equation (15.36), we can determine the effect of each RC network in the phase-shift oscillator. At the oscillation frequency ω_o, the transfer function of each RC network stage is

$$\frac{j\omega_o RC}{1 + j\omega_o RC} = \frac{(j/\sqrt{3})}{1 + (j/\sqrt{3})} = \frac{j}{\sqrt{3} + j} \tag{15.44}$$

which can be written in terms of the magnitude and phase, as follows:

$$\frac{1}{\sqrt{3} + 1} \times \frac{\angle 90^\circ}{\angle \tan^{-1}(1/\sqrt{3})} = \frac{1}{2} \times [\angle 90^\circ - \angle \tan^{-1}(0.577)] \tag{15.45(a)}$$

or

$$\frac{1}{2} \times (\angle 90^\circ - \angle 30^\circ) = \frac{1}{2} \times \angle 60^\circ \tag{15.45(b)}$$

As required, each RC network introduces a 60 degree phase shift, but they each also introduce an attenuation factor of $(\frac{1}{2})$ for which the amplifier must compensate.

Test Your Understanding

D15.6 Design the phase-shift oscillator shown in Figure 15.16 to oscillate at $f_o = 15\,\text{kHz}$. Choose appropriate component values. (Ans. For example, $C = 0.001\,\mu\text{F}$, $R = 6.13\,\text{k}\Omega$, $R_2 = 49\,\text{k}\Omega$)

The two voltage followers in the circuit in Figure 15.16 need not be included in a practical phase-shift oscillator. Figure 15.17 shows a phase-shift oscillator without the voltage-follower buffer stages. The three RC network stages and the inverting amplifier are still included. The loading effect of each successive RC network complicates the analysis, but the same principle of operation applies. The analysis shows that the oscillation frequency is

$$\omega_o = \frac{1}{\sqrt{6}RC} \tag{15.46}$$

and the amplifier resistor ratio must be

$$\frac{R_2}{R} = 29 \tag{15.47}$$

in order to sustain oscillation.

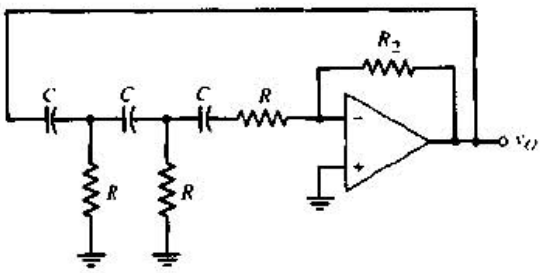


Figure 15.17 Phase-shift oscillator circuit

Test Your Understanding

15.7 For the phase-shift oscillator in Figure 15.17, the parameters are $R = 10\,\text{k}\Omega$ and $C = 100\,\text{pF}$. Determine the frequency of oscillation and the required value of R_2. (Ans. $f_o \cong 65\,\text{kHz}$, $R_2 = 290\,\text{k}\Omega$)

15.2.3 Wien-Bridge Oscillator

Another basic oscillator is the **Wien-bridge circuit**, shown in Figure 15.18. The circuit consists of an op-amp connected in a noninverting configuration and two RC networks connected as the frequency-selecting feedback circuit.

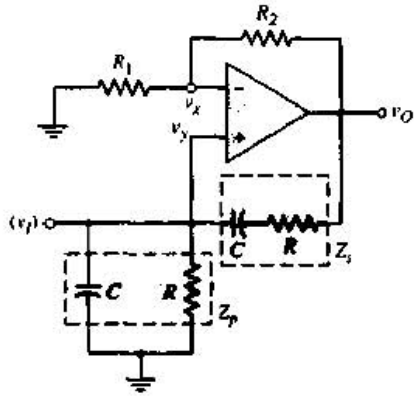


Figure 15.18 Wien-bridge oscillator

Again, we initially assume that an input signal exists at the noninverting terminals of the op-amp. Since the noninverting amplifier introduces zero phase shift, the frequency-selective feedback circuit must also introduce zero phase shift to create the positive feedback condition.

The loop gain is the product of the amplifier gain and the feedback transfer function, or

$$T(s) = \left(1 + \frac{R_2}{R_1}\right)\left(\frac{Z_p}{Z_p + Z_s}\right) \tag{15.48}$$

where Z_p and Z_s are the parallel and series RC network impedances, respectively. These impedances are

$$Z_p = \frac{R}{1 + sRC} \tag{15.49(a)}$$

and

$$Z_s = \frac{1 + sRC}{sC} \tag{15.49(b)}$$

Combining Equations (15.49(a)), (15.49(b)), and (15.48), we get an expression for the loop gain function,

$$T(s) = \left(1 + \frac{R_2}{R_1}\right)\left[\frac{1}{3 + sRC + (1/sRC)}\right] \tag{15.50}$$

Since this circuit has no explicit negative feedback, as was assumed in the general network shown in Figure 15.15, the condition for oscillation is given by

$$T(j\omega_o) = 1 = \left(1 + \frac{R_2}{R_1}\right)\left[\frac{1}{3 + j\omega_o RC + (1/j\omega_o RC)}\right] \tag{15.51}$$

Since $T(j\omega_o)$ must be real, the imaginary component of Equation (15.51) must be zero; therefore,

$$j\omega_o RC + \frac{1}{j\omega_o RC} = 0 \tag{15.52(a)}$$

which gives the frequency of oscillation as

$$\omega_o = \frac{1}{RC} \qquad \textbf{(15.52(b))}$$

The magnitude condition is then

$$1 = \left(1 + \frac{R_2}{R_1}\right)\left(\frac{1}{3}\right) \qquad \textbf{(15.53(a))}$$

or

$$\frac{R_2}{R_1} = 2 \qquad \textbf{(15.53(b))}$$

Equation (15.53(b)) states that to ensure the startup of oscillation, we must have $(R_2/R_1) > 2$.

Design Example 15.5 Objective: Design a Wien-bridge circuit to oscillate at a specified frequency.

Consider the Wien-bridge oscillator in Figure 15.18. Design the circuit to oscillate at $f_o = 20\,\text{kHz}$.

Solution: The oscillation frequency given by Equation (15.52(b)) yields

$$RC = \frac{1}{2\pi f_o} = \frac{1}{2\pi(20 \times 10^3)} = 7.96 \times 10^{-6}$$

a $10\,\text{k}\Omega$ resistor and 796 pF capacitor satisfy this requirement. Since the amplifier resistor ratio must be $R_2/R_1 = 2$, we could, for example, have $R_2 = 20\,\text{k}\Omega$ and $R_1 = 10\,\text{k}\Omega$, which would satisfy the requirement.

Comment: As usual in any electronic circuit design, there is no unique solution. Reasonably sized component values should be chosen whenever possible.

Computer Simulation Verification: A computer simulation was performed using the circuit in Figure 15.19(a). Figure 15.19(b) shows the output voltage versus time. Since the ratio of resistances is $R_2/R_1 = 22/10 = 2.2$, the overall gain is greater than unity so the output increases as a function of time. This increase shows the oscillation nature of the circuit. Another characteristic of the circuit is shown in Figure 15.19(c). A 1 mV sinusoidal signal was applied to the input of R_1 and the output voltage measured as the frequency was swept from 10 kHz to 30 kHz. The resonant nature of the circuit is observed. The oscillation frequency and the resonant frequency are both at approximately 18.2 kHz, which is below the design value of 20 kHz.

If the capacitor in the circuit is reduced from 796 pF to 720 pF, the resonant frequency is exactly 20 kHz. This example is one case, then, when the design parameters need to be changed slightly in order to meet the design specifications.

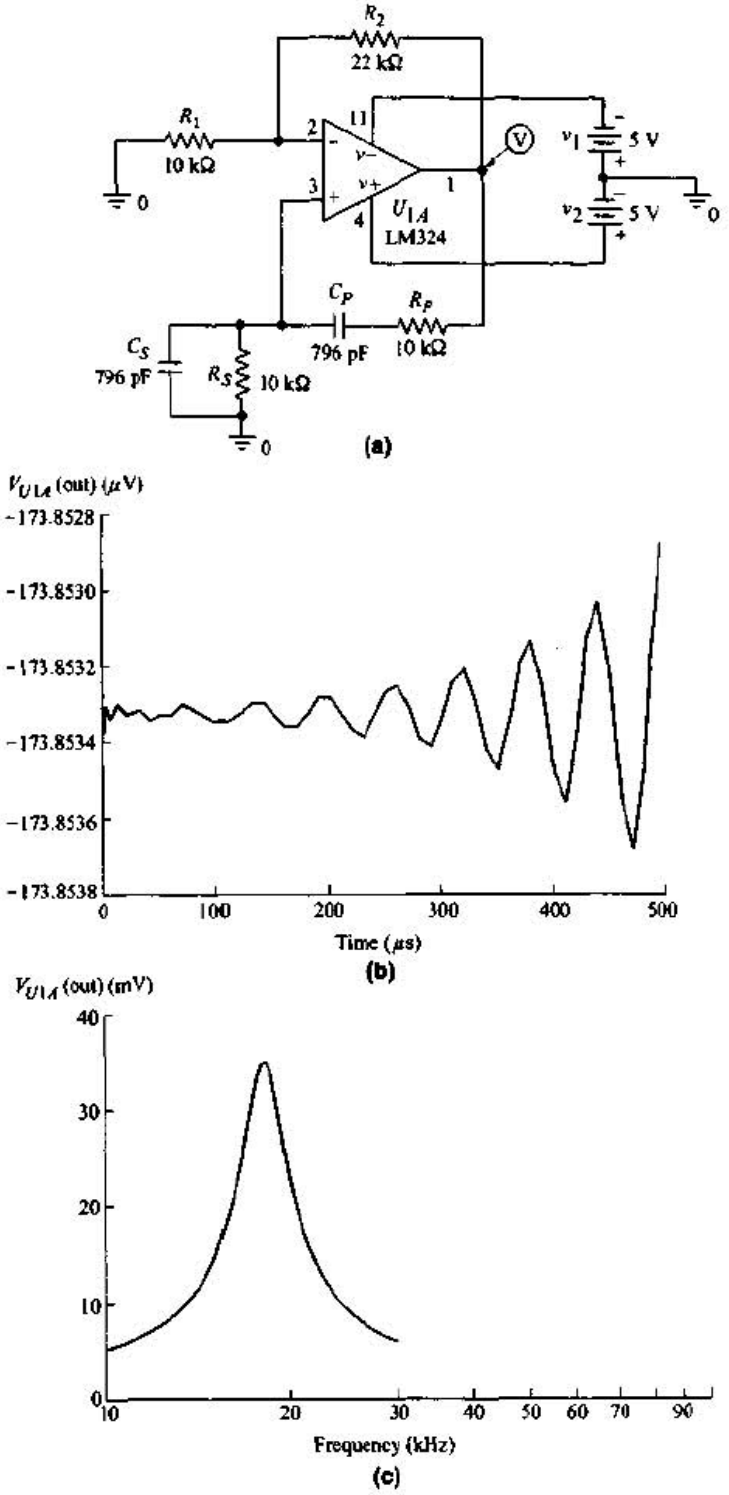


Figure 15.19 (a) Circuit used in the computer simulation for Example 15.5, (b) output voltage versus time, and (c) output voltage versus input frequency

Test Your Understanding

D15.8 Design the Wien-bridge circuit in Figure 15.18 to oscillate at $f_o = 800\,\text{Hz}$. Assume $R = R_1 = 10\,\text{k}\Omega$. (Ans. $C \cong 0.02\,\mu\text{F}$, $R_2 = 20\,\text{k}\Omega$)

15.2.4 Additional Oscillator Configurations

Oscillators that use transistors and *LC* tuned circuits or crystals in their feedback networks can be used in the hundreds of kHz to hundreds of MHz frequency range. Although these oscillators do not typically contain an op-amp, we include a brief discussion of such circuits for completeness. We will examine the Colpitts, Hartley, and crystal oscillators.

Colpitts Oscillator

The ac equivalent circuit of the **Colpitts oscillator** with an FET is shown in Figure 15.20. A circuit with a BJT can also be designed. A parallel *LC* resonant circuit is used to establish the oscillator frequency, and feedback is provided by a voltage divider between capacitors C_1 and C_2. Resistor R in conjunction with the transistor provides the necessary gain at resonance. We assume that the transistor frequency response occurs at a high enough frequency that the oscillation frequency is determined by the external elements only.

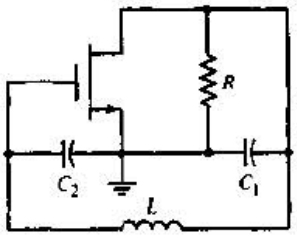


Figure 15.20 The ac equivalent circuit, MOSFET Colpitts oscillator

Figure 15.21 shows the small-signal equivalent circuit of the Colpitts oscillator. The transistor output resistance r_o can be included in R. A KCL equation at the output node yields

$$\frac{V_o}{\dfrac{1}{sC_1}} + \frac{V_o}{R} + g_m V_{gs} + \frac{V_o}{sL + \dfrac{1}{sC_2}} = 0 \tag{15.54}$$

and a voltage divider produces

$$V_{gs} = \left(\frac{\dfrac{1}{sC_2}}{\dfrac{1}{sC_2} + sL} \right) \cdot V_o \tag{15.55}$$

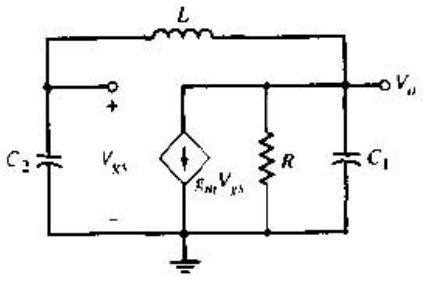


Figure 15.21 Small-signal equivalent circuit, MOSFET Colpitts oscillator

Substituting Equation (15.55) into Equation (15.54), we find that

$$V_o\left[g_m + sC_2 + (1 + s^2LC_2)\left(\frac{1}{R} + sC_1\right)\right] = 0 \tag{15.56}$$

If we assume that oscillation has started, then $V_o \neq 0$ and can be eliminated from Equation (15.56). We then have

$$s^3LC_1C_2 + \frac{s^2LC_2}{R} + s(C_1 + C_2) + \left(g_m + \frac{1}{R}\right) = 0 \tag{15.57}$$

Letting $s = j\omega$, we obtain

$$\left(g_m + \frac{1}{R} - \frac{\omega^2LC_2}{R}\right) + j\omega\left[(C_1 + C_2) - \omega^2LC_1C_2\right] = 0 \tag{15.58}$$

The condition for oscillation implies that both the real and imaginary components of Equation (15.58) must be zero. From the imaginary component, the oscillation frequency is

$$\omega_o = \frac{1}{\sqrt{L\left(\frac{C_1C_2}{C_1 + C_2}\right)}} \tag{15.59}$$

which is the resonant frequency of the LC circuit. From the real part of Equation (15.58), the condition for oscillation is

$$\frac{\omega_o^2LC_2}{R} = g_m + \frac{1}{R} \tag{15.60}$$

Combining Equations (15.59) and (15.60) yields

$$\frac{C_2}{C_1} = g_mR \tag{15.61}$$

where g_mR is the magnitude of the gain. Equation (15.61) states that to initiate oscillations spontaneously, we must have $g_mR > (C_2/C_1)$.

Hartley Oscillator

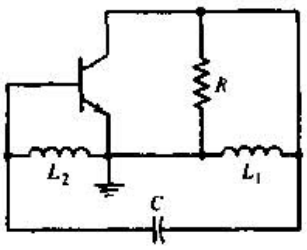


Figure 15.22 The ac equivalent, BJT Hartley oscillator

Figure 15.22 shows the ac equivalent circuit of the Hartley oscillator with a BJT. An FET can also be used. Again, a parallel LC resonant circuit establishes the oscillator frequency, and feedback is provided by a voltage divider between inductors L_1 and L_2.

The analysis of the Hartley oscillator is essentially identical to that of the Colpitts oscillator. The frequency of oscillation, neglecting transistor frequency effects, is

$$\omega_o = \frac{1}{\sqrt{(L_1 + L_2)C}} \tag{15.62}$$

Equation (15.62) also assumes that $r_\pi \gg 1/(\omega C_2)$.

Crystal Oscillator

A piezoelectric crystal, such as quartz, exhibits electromechanical resonance characteristics in response to a voltage applied across the crystal. The oscillations are very stable over time and temperature, with temperature coefficients on the order of 1 ppm per °C. The oscillation frequency is determined by the crystal dimensions. This means that crystal oscillators are fixed-frequency devices.

The circuit symbol for the piezoelectric crystal is shown in Figure 15.23(a), and the equivalent circuit is shown in Figure 15.23(b). The inductance L can be as high as a few hundred henrys, the capacitance C_s can be on the order of 0.001 pF, and the capacitance C_p can be on the order of a few pF. Also, the Q-factor can be on the order of 10^4, which means that the series resistance r can be neglected.

The impedance of the equivalent circuit in Figure 15.23(b) is

$$Z(s) = \frac{1}{sC_p} \cdot \frac{s^2 + (1/LC_s)}{s^2 + [(C_p + C_s)/(LC_sC_p)]} \tag{15.63}$$

Equation (15.63) indicates that the crystal has two resonant frequencies, which are very close together. At the series-resonant frequency f_s, the reactance of the series branch is zero; at the parallel-resonant frequency f_p, the reactance of the crystal approaches infinity.

Between the resonant frequencies f_s and f_p, the crystal reactance is inductive, so the crystal can be substituted for an inductance, such as that in a Colpitts oscillator. Figure 15.24 shows the ac equivalent circuit of a Pierce oscillator, which is similar to the Colpitts oscillator in Figure 15.20 but with the inductor replaced by the crystal. Since the crystal reactance is inductive over a very narrow frequency range, the frequency of oscillation is also confined to this narrow range and is quite constant relative to changes in bias current or temperature. Crystal oscillator frequencies are usually in the range of tens of kHz to tens of MHz.

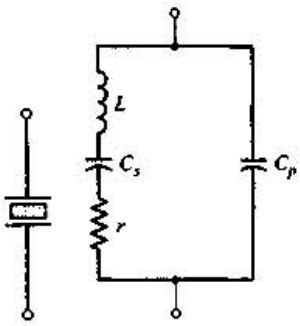


Figure 15.23 (a) Piezoelectric crystal circuit symbol and (b) piezoelectric crystal equivalent circuit

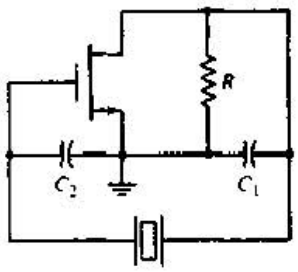


Figure 15.24 Pierce oscillator in which the inductor in a Colpitts oscillator is replaced by a crystal

Test Your Understanding

***15.9** For the Colpitts oscillator in Figure 15.20, assume parameters of $L = 1\,\mu H$, C_1 and $C_2 = 1\,nF$, and $R = 4\,k\Omega$. Determine the oscillator frequency and the required value of g_m. Is this value of g_m reasonable for a MOSFET? Why? (Ans. $f_o = 7.12\,MHz$, $g_m = 0.25\,mA/V$)

15.3 SCHMITT TRIGGER CIRCUITS

In this section, we will analyze another class of circuits that utilize positive feedback. The basic circuit is commonly called a **Schmitt trigger**, which can be used in the class of waveform generators called multivibrators. The three general types of multivibrators are: bistable, monostable, and astable. In this section, we will examine the bistable multivibrator, which has a comparator

with positive feedback and has two stable states. We will discuss the comparator first, and will then describe various applications of the Schmitt trigger.

15.3.1 Comparator

The comparator is essentially an op-amp operated in an open-loop configuration, as shown in Figure 15.25(a). As the name implies, a comparator compares two voltages to determine which is larger. The comparator is usually biased at voltages $+V_S$ and $-V_S$, although other biases are possible.

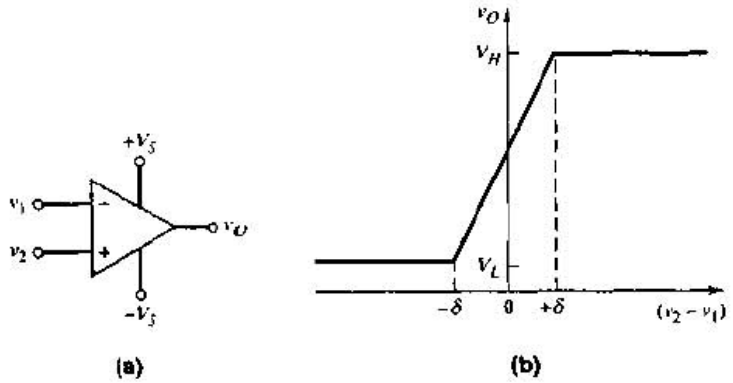


Figure 15.25 (a) Open-loop comparator and (b) voltage transfer characteristics, open-loop comparator

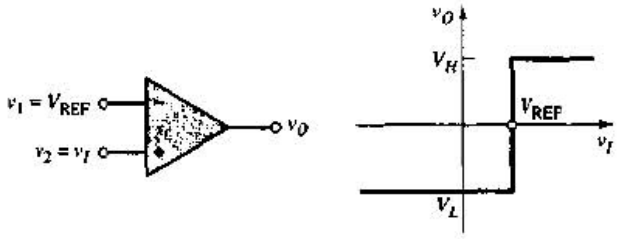
The voltage transfer characteristics, neglecting any offset voltage effects, are shown in Figure 15.25(b). When v_2 is slightly greater than v_1, the output is driven to a high saturated state V_H; when v_2 is slightly less than v_1, the output is driven to a low saturated state V_L. The saturated output voltages V_H and V_L may be close to the supply voltages $+V_S$ and $-V_S$, respectively, which means that V_L may be negative. The transition region is the region in which the output voltage is in neither of its saturation states. This region occurs when the input differential voltage is in the range $-\delta < (v_2 - v_1) < +\delta$. If, for example, the open-loop gain is 10^5 and the difference between the two output states is $(V_H - V_L) = 10\,\text{V}$, then

$$2\delta = 10/10^5 = 10^{-4}\,\text{V} = 0.1\,\text{mV}$$

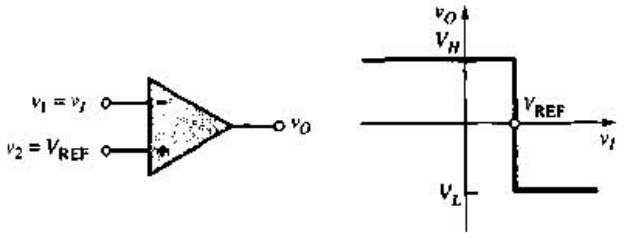
The range of input differential voltage in the transition region is normally very small.

One major difference between a comparator and op-amp is that a comparator need not be frequency compensated. Frequency stability is not a consideration since the comparator is being driven into one of two states. Since a comparator does not contain a frequency compensation capacitor, it is not slew-rate-limited by the compensation capacitor as is the op-amp. Typical response times for the comparator output to change states are in the range of 30 to 200 ns. An expected response time for a 741 op-amp with a slew rate of 0.7 V/μs would be on the order of 30 μs, which is a factor of 1000 times greater.

Figure 15.26 shows two comparator configurations along with their voltage transfer characteristics. In both, the input transition region width is assumed to be negligibly small. The reference voltage may be either positive or negative, and the output saturation voltages are assumed to be symmetrical about zero. The crossover voltage is defined as the input voltage at which the output changes states.



(a)



(b)

Figure 15.26 (a) Noninverting comparator circuit and (b) inverting comparator circuit

Two other comparator configurations, in which the crossover voltage is a function of resistor ratios, are shown in Figure 15.27. Input bias current compensation is also included in this figure. From Figure 15.27(a), we use superposition to obtain

$$v_+ = \left(\frac{R_2}{R_1 + R_2}\right) V_{REF} + \left(\frac{R_1}{R_1 + R_2}\right) v_I \tag{15.64}$$

The ideal crossover voltage occurs when $v_+ = 0$, or

$$R_2 V_{REF} + R_1 v_I = 0 \tag{15.65(a)}$$

which can be written as

$$v_I = -\frac{R_2}{R_1} V_{REF} \tag{15.65(b)}$$

The output goes high when $v_+ > 0$. From Equation (15.64), we see that v_o = High when v_I is greater than the crossover voltage. A similar analysis produces the characteristics shown in Figure 15.27(b).

Figure 15.28 shows one application of a comparator, to control street lights. The input signal is the output of a photodetector circuit. Voltage v_I is directly proportional to the amount of light incident on the photodetector.

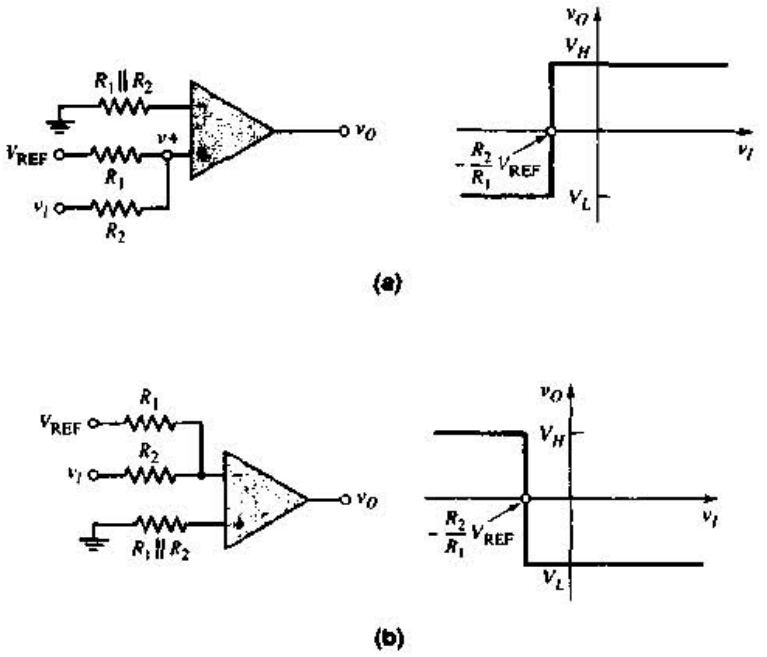


Figure 15.27 Other comparator circuits: (a) noninverting and (b) inverting

During the night, $v_I < V_{REF}$, and v_O is on the order of $V_S = +15\,V$; the transistor turns on. The current in the relay switch then turns the street lights on. During the day, the light incident on the photodetector produces an output signal such that $v_I > V_{REF}$. In this case, v_O is on the order of $-V_S = -15\,V$, and the transistor turns off.

Diode D_1 is used as a protection device, preventing reverse-bias breakdown in the B–E junction. With zero output current, the relay switch is open and the street lights are off. At dusk and dawn, $v_I = V_{REF}$.

The open-loop comparator circuit in Figure 15.28 may exhibit unacceptable behavior in response to noise in the system. Figure 15.29(a) shows the same comparator circuit, but with a variable light source, such as clouds causing the

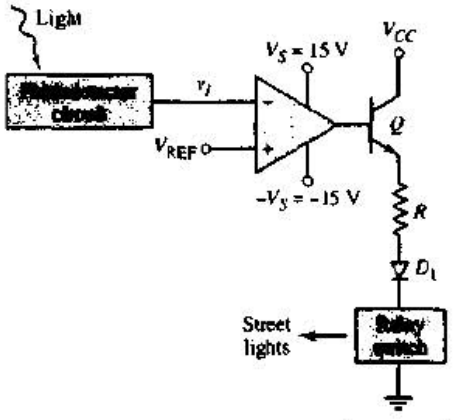


Figure 15.28 Comparator application

(a)

Figure 15.29 (a) Comparator circuit including input noise source, (b) input signal, and (c) output signal, showing chatter effect

light intensity to fluctuate over a short period of time. A variable light intensity would be equivalent to a noise source v_n in series with the signal source v_I. If we assume that v_I is increasing linearly with time (corresponding to dawn), then the total input signal v_I' versus time is shown in Figure 15.29(b). When $v_I' > V_{REF}$, the output switches low; when $v_I' < V_{REF}$, the output switches high, producing a chatter effect in the output signal as shown in Figure 14.29(c). This effect would turn the street lights off and on over a relatively short time period. If the amplitude of the noise signal increases, the chatter effect becomes more severe. This chatter can be eliminated by using a Schmitt trigger.

15.3.2 Basic Inverting Schmitt Trigger

The Schmitt trigger or **bistable multivibrator** uses positive feedback with a loop-gain greater than unity to produce a bistable characteristic. Figure 15.30(a) shows one configuration of a Schmitt trigger. Positive feedback occurs because the feedback resistor is connected between the output and noninverting input terminals. Voltage v_+, in terms of the output voltage, can be found by using a voltage divider equation to yield

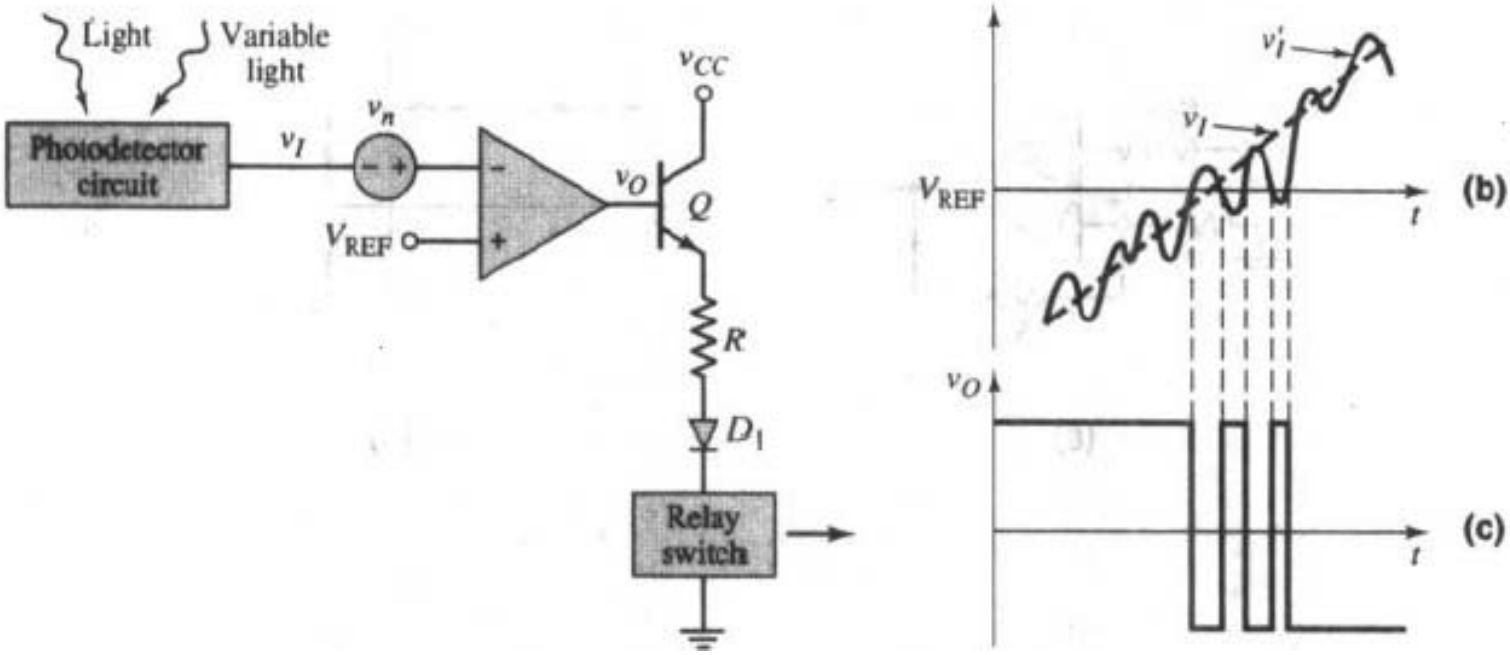
$$v_+ = \left(\frac{R_1}{R_1 + R_2}\right) v_O \tag{15.66}$$

Voltage v_+ does not remain constant; rather, it is a function of the output voltage. Input signal v_I is applied to the inverting terminal.

Voltage Transfer Characteristics

To determine the voltage transfer characteristics, we assume that the output of the comparator is in one state, namely $v_O = V_H$, which is the high state. Then

$$v_+ = \left(\frac{R_1}{R_1 + R_2}\right) V_H \tag{15.67}$$


Light
Variable light
Photodetector circuit
v_I
v_n
V_{REF}
v_{CC}
v_O
Q
R
D_1
Relay switch
v_I'
v_I
V_{REF}
t
(b)
v_O
t
(c)

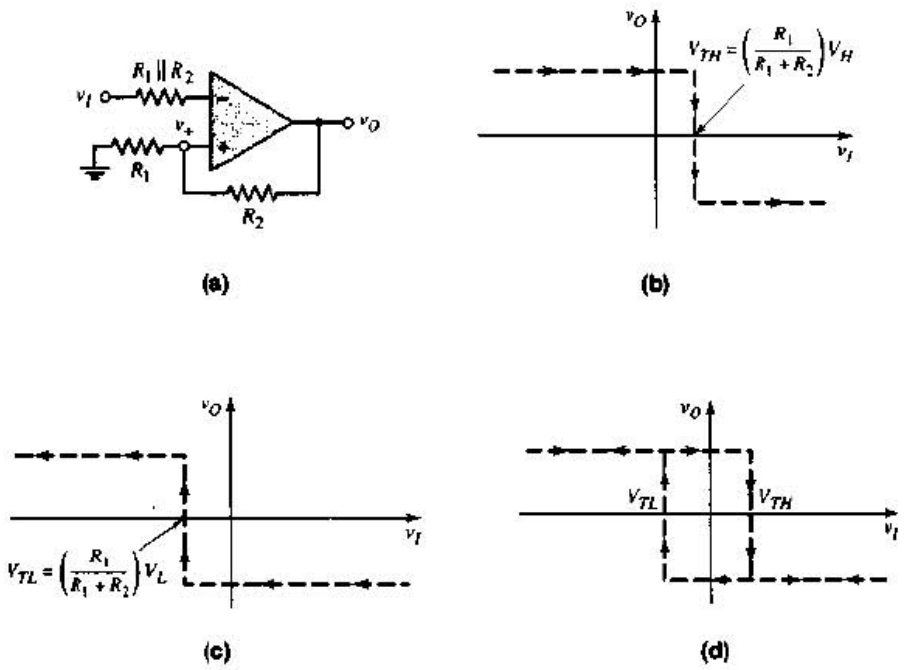


Figure 15.30 (a) Schmitt trigger circuit, (b) voltage transfer characteristic as input voltage increases, (c) voltage transfer characteristic as input voltage decreases, and (d) net voltage transfer characteristics, showing hysteresis effect

As long as the input signal is less than v_+, the output remains in its high state. The crossover voltage occurs when $v_I = v_+$ and is defined as V_{TH}. We have

$$V_{TH} = \left(\frac{R_1}{R_1 + R_2}\right) V_H \tag{15.68}$$

When v_I is greater than V_{TH}, the voltage at the inverting terminal is greater than that at the noninverting terminal. The differential input voltage $(v_I - V_{TH})$ is amplified by the open-loop gain of the comparator, and the output switches to its low state, or $v_O = V_L$. Voltage v_+ then becomes

$$v_+ = \left(\frac{R_1}{R_1 + R_2}\right) V_L \tag{15.69}$$

Since $V_L < V_H$, the input voltage v_I is still greater than v_+, and the output remains in its low state as v_I continues to increase. This voltage transfer characteristic is shown in Figure 15.30(b). Implicit in these transfer characteristics is the assumption that V_H is positive and V_L is negative.

Now consider the transfer characteristic as v_I decreases. As long as v_I is larger than $v_+ = [R_1/(R_1 + R_2)]V_L$, the output remains in its low saturation state. The crossover voltage now occurs when $v_I = v_+$ and is defined as V_{TL}. We have

$$V_{TL} = \left(\frac{R_1}{R_1 + R_2}\right) V_L \tag{15.70}$$

As v_I drops below this value, the voltage at the noninverting terminal is greater than that at the inverting terminal. The differential voltage at the comparator terminals is amplified by the open-loop gain, and the output switches to its high

state, or $v_O = V_H$. As v_I continues to decrease, it remains less than v_+; therefore, v_O remains in its high state. This voltage transfer characteristic is shown in Figure 15.30(c).

Complete Voltage Transfer and Bistable Characteristics

The complete voltage transfer characteristics of the Schmitt trigger in Figure 15.30(a) combine the characteristics in Figures 15.30(b) and 15.30(c). These complete characteristics are shown in Figure 15.30(d). As shown, the crossover voltages depend on whether the input voltage is increasing or decreasing. The complete transfer characteristics therefore show a **hysteresis effect**. The width of the hysteresis is the difference between the two crossover voltages V_{TH} and V_{TL}.

The bistable characteristic of the circuit occurs around the point $v_I = 0$, at which the output may be in either its high or low state. The output remains in either state as long as v_I remains in the range $V_{TL} < v_I < V_{TH}$. The output switches states only if the input increases above V_{TH} or decreases below V_{TL}.

Example 15.6 **Objective:** Determine the hysteresis width of a particular Schmitt trigger.

Consider the Schmitt trigger in Figure 15.30(a), with parameters $R_1 = 10\,\text{k}\Omega$ and $R_2 = 90\,\text{k}\Omega$. Let $V_H = 10\,\text{V}$ and $V_L = -10\,\text{V}$.

Solution: From Equation (15.68), the upper crossover voltage is

$$V_{TH} = \left(\frac{R_1}{R_1 + R_2}\right)V_H = \left(\frac{10}{10 + 90}\right)(10) = 1\,\text{V}$$

and from Equation (15.70), the lower crossover voltage is

$$V_{TL} = \left(\frac{R_1}{R_1 + R_2}\right)V_L = \left(\frac{10}{10 + 90}\right)(-10) = -1\,\text{V}$$

The hysteresis width is therefore $(V_{TH} - V_{TL}) = 2\,\text{V}$.

Comment: The hysteresis width can be designed to be larger or smaller for specific applications by adjusting the voltage divider ratio of R_1 and R_2.

The complete voltage transfer characteristics in Figure 15.30(d) show the inverting characteristics of this particular Schmitt trigger. When the input signal becomes sufficiently positive, the output is in its low state; when the input signal is sufficiently negative, the output is in its high state. Since the input signal is applied to the inverting terminal of the comparator, this characteristic is as expected.

Test Your Understanding

15.10 For the comparator in Figure 15.30(a), the high and low saturated output states are $+12\,\text{V}$ and $-12\,\text{V}$, respectively. If $R_2 = 20\,\text{k}\Omega$, find R_1 such that the crossover voltages are $\pm 2\,\text{V}$. (Ans. $R_1 = 4\,\text{k}\Omega$)

15.3.3 Additional Schmitt Trigger Configurations

A noninverting Schmitt trigger can be designed by applying the input signal to the network connected to the comparator noninverting terminal. Also, both crossover voltages of a Schmitt trigger circuit can be shifted in either a positive or negative direction by applying a reference voltage. We will study these general circuit configurations, the resulting voltage transfer characteristics, and an application of a Schmitt trigger circuit in this section.

Noninverting Schmitt Trigger Circuit

Consider the circuit in Figure 15.31(a). The inverting terminal is held essentially at ground potential, and the input signal is applied to resistor R_1, which is connected to the comparator noninverting terminal. Voltage v_+ at the noninverting terminal then becomes a function of both the input signal v_I and the output voltage v_O. Using superposition, we find that

$$v_+ = \left(\frac{R_2}{R_1 + R_2}\right)v_I + \left(\frac{R_1}{R_1 + R_2}\right)v_O \tag{15.71}$$

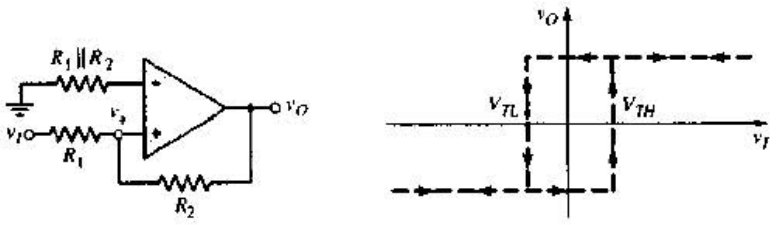


Figure 15.31 (a) Noninverting Schmitt trigger circuit and (b) voltage transfer characteristics

If v_I is negative, and the output is in its low state, then $v_O = V_L$ (assumed to be negative), v_+ is negative, and the output remains in its low saturation state. Crossover voltage $v_I = V_{TH}$ occurs when $v_+ = 0$ and $v_O = V_L$, or, from Equation (15.71),

$$0 = R_2 V_{TH} + R_1 V_L \tag{15.72(a)}$$

which can be written

$$V_{TH} = -\left(\frac{R_1}{R_2}\right)V_L \tag{15.72(b)}$$

Since V_L is negative, V_{TH} is positive.

If we let $v_I = V_{TH} + \delta$, where δ is a small positive voltage, the input voltage is just greater than the crossover voltage and Equation (15.71) becomes

$$v_+ = \left(\frac{R_2}{R_1 + R_2}\right)(V_{TH} + \delta) + \left(\frac{R_1}{R_1 + R_2}\right)V_L \tag{15.73}$$

Equation (15.73) then becomes

$$v_+ = \left(\frac{R_2}{R_1 + R_2}\right)\left(\frac{-R_1}{R_2}\right)V_L + \left(\frac{R_2}{R_1 + R_2}\right)\delta + \left(\frac{R_1}{R_1 + R_2}\right)V_L \qquad \textbf{(15.74(a))}$$

or

$$v_+ = \left(\frac{R_2}{R_1 + R_2}\right)\delta > 0 \qquad \textbf{(15.74(b))}$$

When $v_+ > 0$, the output switches to its high saturation state.

The lower crossover voltage $v_I = V_{TL}$ occurs when $v_+ = 0$ and $v_O = V_H$. From Equation (15.71), we have

$$0 = R_2 V_{TL} + R_1 V_H \qquad \textbf{(15.75(a))}$$

which can be written

$$V_{TL} = -\left(\frac{R_1}{R_2}\right)V_H \qquad \textbf{(15.75(b))}$$

Since $V_H > 0$, then $V_{TL} < 0$.

The complete voltage transfer characteristics are shown in Figure 15.31(b). We again note the hysteresis effect and the bistable characteristic around $v_I = 0$. With v_I sufficiently positive, the output is in its high state; with v_I sufficiently negative, the output is in its low state. The circuit thus exhibits the noninverting transfer characteristic.

Test Your Understanding

D15.11 A noninverting Schmitt trigger is shown in Figure 15.31(a). Its saturated output voltages are ±10V. Design the circuit to obtain ±100 mV crossover voltages. Choose suitable component values. (Ans. $R_1/R_2 = 0.010$)

Schmitt Trigger Circuits with Applied Reference Voltages

The switching voltage of a Schmitt trigger is defined as the average value of V_{TH} and V_{TL}. For the two circuits in Figure 15.30(a) and 15.31(a), the switching voltages are zero, assuming $V_{TL} = -V_{TH}$. In some applications, the switching voltage must be either positive or negative. Both crossover voltages can be shifted in either a positive or negative direction by applying a reference voltage.

Figure 15.32(a) shows an inverting Schmitt trigger with a reference voltage V_{REF}. The complete voltage transfer characteristics are shown in Figure 15.32(b). The switching voltage V_S, assuming V_H and V_L are symmetrical about zero, is given by

$$V_S = \left(\frac{R_2}{R_1 + R_2}\right)V_{REF} \qquad \textbf{(15.76)}$$

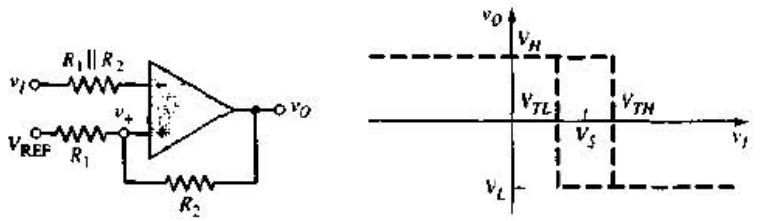


Figure 15.32 (a) Inverting Schmitt trigger circuit with applied reference voltage and (b) voltage transfer characteristics

Note that the switching voltage is not the same as the reference voltage. The upper and lower crossover voltages are

$$V_{TH} = V_S + \left(\frac{R_1}{R_1 + R_2}\right) V_H \tag{15.77(a)}$$

and

$$V_{TL} = V_S + \left(\frac{R_1}{R_1 + R_2}\right) V_L \tag{15.77(b)}$$

Test Your Understanding

15.12 For the Schmitt trigger in Figure 15.32(a), the parameters are: $V_{REF} = 2\,V$, $V_H = 10\,V$, $V_L = -10\,V$, $R_1 = 1\,k\Omega$, and $R_2 = 10\,k\Omega$: (a) Determine V_S, V_{TH}, and V_{TL}. (b) Let v_I be a triangular wave with a zero average voltage, a 10 V peak amplitude, and a 10 ms period. Sketch v_O versus time over two periods. Label the appropriate voltages and times. (Ans. (a) $V_S = 1.82\,V$, $V_{TH} = 2.73\,V$, $V_{TL} = 0.91\,V$)

A noninverting Schmitt trigger with a reference voltage is shown in Figure 15.33(a), and the complete voltage transfer characteristics are shown in Figure 15.33(b). The switching voltage V_s, again assuming V_H and V_L are symmetrical about zero, is given by

$$V_S = \left(1 + \frac{R_1}{R_2}\right) V_{REF} \tag{15.78}$$

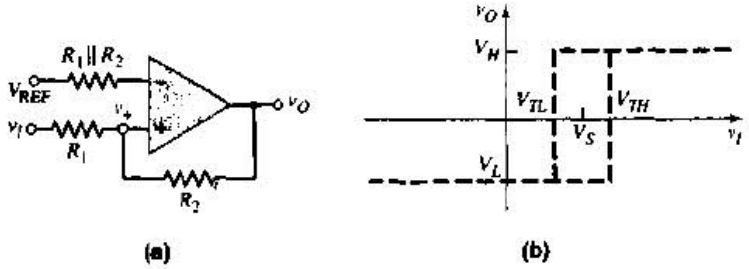


Figure 15.33 (a) Noninverting Schmitt trigger circuit with applied reference voltage and (b) voltage transfer characteristics

and the upper and lower crossover voltages are

$$V_{TH} = V_S - \left(\frac{R_1}{R_2}\right)V_L \qquad \textbf{(15.79(a))}$$

and

$$V_{TL} = V_S - \left(\frac{R_1}{R_2}\right)V_H \qquad \textbf{(15.79(b))}$$

If the output saturation voltages are symmetrical such that $V_L = -V_H$, then the crossover voltages are symmetrical about the switching voltage V_S.

Test Your Understanding

D15.13 Consider the Schmitt trigger in Figure 15.33(a). Let $V_H = 5\,\text{V}$ and $V_L = -5\,\text{V}$. Design the circuit such that $V_S = -1\,\text{V}$ and the hysteresis width is 2.5 V. What are the values of V_{TL} and V_{TH}? (Ans. $R_1/R_2 = 0.25$, $V_{\text{REF}} = -0.8\,\text{V}$, $V_{TH} = 0.25\,\text{V}$, $V_{TL} = -2.25\,\text{V}$)

Schmitt Trigger Application

Let us reconsider the street light control in Figure 15.29(a), which included a noise source. Figure 15.34(a) shows the same basic circuit, except that a Schmitt trigger is used instead of a simple comparator.

The input signal v_I is again assumed to increase linearly with time. The total input signal v_I' is v_I with the noise signal superimposed, as shown in Figure 15.34(b). At time t_1, the input signal becomes greater than the switching voltage V_S. The output, however, does not switch, since $v_I' < V_{TH}$. This means that the input signal is less than the upper crossover voltage. At time t_2, the input signal becomes larger than the crossover voltage, or $v_I' > V_{TH}$, and the

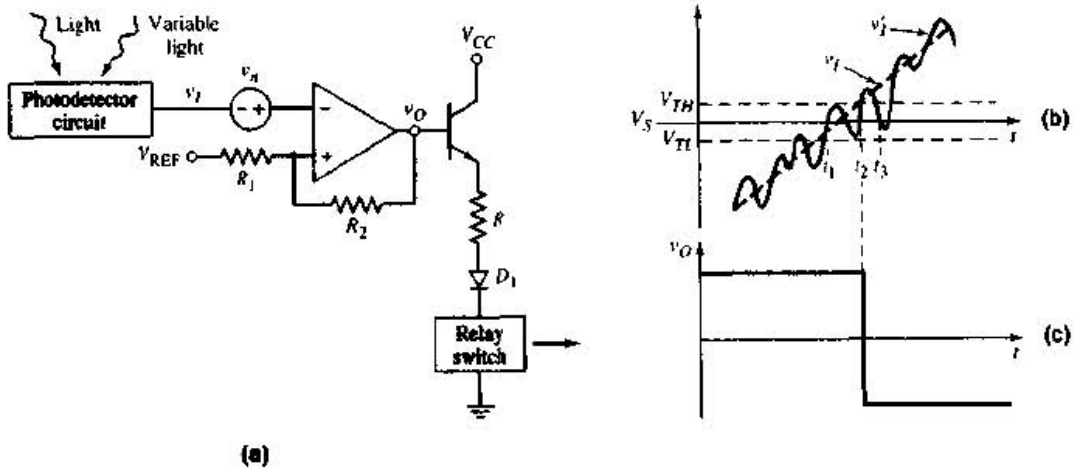


Figure 15.34 (a) Application of Schmitt trigger circuit including input noise source, (b) input signal, and (c) output signal, showing elimination of chatter effect

output signal switches from its high to its low state. At time t_3, the input signal drops below V_S, but the output does not switch states since $v_I' > V_{TL}$. This means that the input signal remains greater than the lower crossover voltage. The Schmitt trigger circuit thus eliminates the chatter effect that occurs in the output voltage in Figure 15.29(c). Elimination of the chatter in the output voltage response results directly from the hysteresis effect in the Schmitt trigger characteristics.

Design Example 15.7 **Objective:** Design a Schmitt trigger circuit for the photodetector switch circuit.

Consider the Schmitt trigger circuit in Figure 15.34(a). Design the circuit such that the switching voltage is $V_S = 2\,\text{V}$ and the hysteresis width is 60 mV. Assume $V_H = 15\,\text{V}$ and $V_L = -15\,\text{V}$.

Solution: The Schmitt trigger circuit is the inverting type, for which the voltage transfer characteristics are shown in Figure 15.32(b). From Equations (15.77(a)) and (15.77(b)), the hysteresis width is

$$V_{TH} - V_{TL} = \left(\frac{R_1}{R_1 + R_2}\right)(V_H - V_L)$$

so

$$0.060 = \left(\frac{R_1}{R_1 + R_2}\right)[15 - (-15)] = 30\left(\frac{R_1}{R_1 + R_2}\right)$$

which yields $R_2/R_1 = 499$. We can find the reference voltage from Equation (15.76), which can be rewritten to obtain

$$V_{\text{REF}} = \left(1 + \frac{R_1}{R_2}\right)V_S = \left(1 + \frac{1}{499}\right)(2) = 2.004\,\text{V}$$

Resistor values of $R_1 = 100\,\Omega$ and $R_2 = 49.9\,\text{k}\Omega$ will satisfy the requirements. The crossover voltages are thus $V_{TH} = 2.03\,\text{V}$ and $V_{TL} = 1.97\,\text{V}$.

Comment: In this case, the output chatter effect is eliminated for noise signals with amplitudes lower than 30 mV. The hysteresis width can be adjusted up or down to fit specific application requirements in which the noise signal is larger or smaller than that given in this example.

Test Your Understanding

D15.14 Redesign the street light control circuit shown in Figure 15.34(a) such that the switching voltage is $V_S = 1\,\text{V}$ and the hysteresis width is 100 mV. Assume $V_H = +10\,\text{V}$ and $V_L = -10\,\text{V}$. Also, find R such that $I = 200\,\text{mA}$ when $v_O = V_H$. Assume $V_{BE}(\text{on}) = 0.7\,\text{V}$ and $V_\gamma = 0.7\,\text{V}$, and assume the relay switch resistance is $100\,\Omega$. (Ans. $R_2/R_1 = 199$, $V_{\text{REF}} = 1.005\,\text{V}$, $R = 42.9\,\text{k}\Omega$)

15.3.4 Schmitt Triggers with Limiters

In the Schmitt trigger circuits we have thus far considered, the open-loop saturation voltages of the comparator may not be very precise and may also vary from one comparator to another. The output saturation voltages can be controlled and made more precise by adding limiter networks.

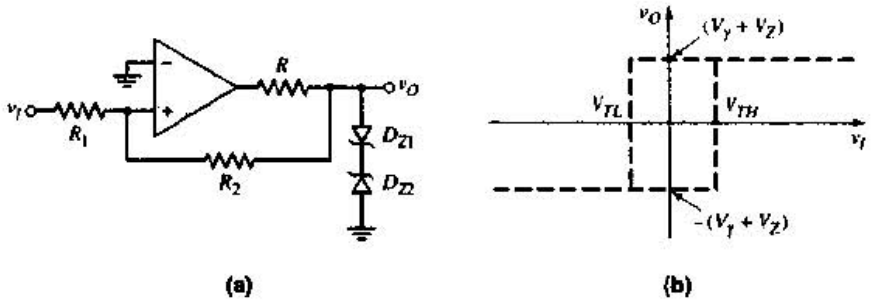


Figure 15.35 (a) Schmitt trigger with Zener diode limiters and (b) voltage transfer characteristics

A direct approach at limiting the output is shown in Figure 15.35. Two back-to-back Zener diodes are connected between the output and ground. Assuming the two diodes are matched, the output is limited to either the positive or negative value of $(V_\gamma + V_Z)$, where V_γ is the forward diode voltage and V_Z is the reverse Zener voltage. Resistor R is chosen to produce a specified current in the diodes.

Another Schmitt trigger with a limiter is shown in Figure 15.36(a). If we assume that $v_I = 0$ and v_O is in its high state, then D_2 is on and D_1 is off.

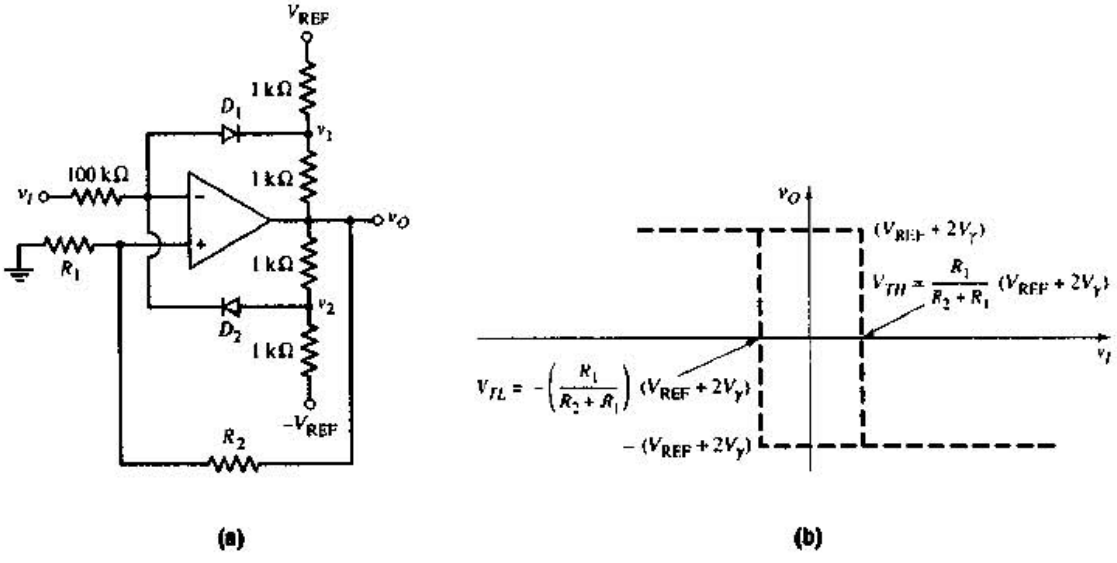


Figure 15.36 (a) Inverting Schmitt trigger with diode limiters and (b) voltage transfer characteristics

Neglecting currents in the 100 kΩ resistor, we have $v_2 = +V_\gamma$, where V_γ is the forward diode voltage. We can write

$$\frac{v_O - v_2}{1} = \frac{v_2 - (-V_{REF})}{1} \tag{15.80}$$

Solving for v_O yields

$$v_O = V_{REF} + 2V_\gamma \tag{15.81}$$

which means that the output voltage can be controlled and can be designed more accurately. The ideal hysteresis characteristics for this Schmitt trigger are shown in Figure 15.36(b). As v_I increases or decreases, a small current flows in the 100 kΩ resistor, producing a nonzero slope in the voltage transfer characteristics. The slope is on the order of 1/100, which is quite small.

A noninverting Schmitt trigger with a limiting network is shown in Figure 15.37(a), and the resulting voltage transfer characteristics are given in Figure 15.37(b).

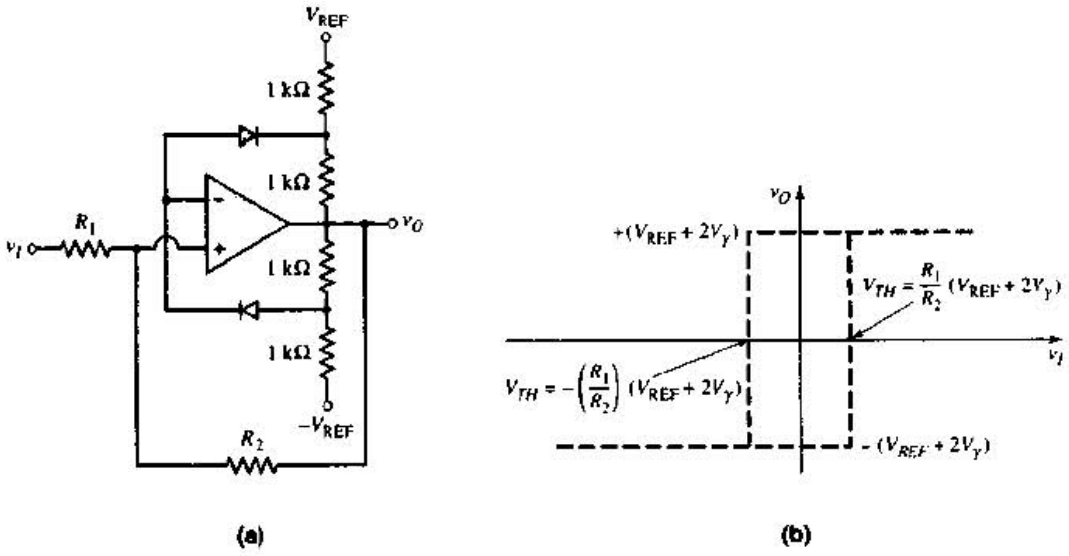


Figure 15.37 (a) Noninverting Schmitt trigger with diode limiters and (b) voltage transfer characteristics

15.4 NONSINUSOIDAL OSCILLATORS AND TIMING CIRCUITS

Many applications, especially digital electronic systems, use a nonsinusoidal square-wave oscillator to provide a clock signal for the system. This type of oscillator is called an astable multivibrator. In other applications, a single pulse of known height and width is used to initiate a particular set of functions. This type of oscillator is called a monostable multivibrator. First, we will examine the Schmitt trigger connected as an oscillator. Then we will analyze the 555 timer circuit. Although used extensively in digital electronic systems, these circuits are included here as comparator circuit applications.

15.4.1 Schmitt Trigger Oscillator

The Schmitt trigger can be used in an oscillator circuit to generate a square-wave output signal. This is accomplished by adding an RC network to the negative feedback loop of the Schmitt trigger as shown in Figure 15.38. As we will see, this circuit has no stable states. It is therefore called an **astable multivibrator**.

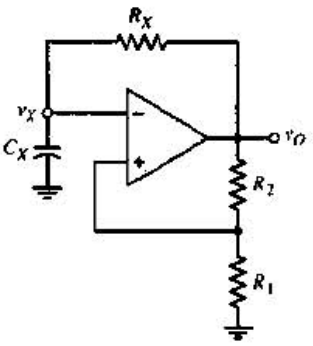


Figure 15.38 Schmitt trigger oscillator

Initially, we set R_1 and R_2 equal to the same value, or $R_1 = R_2 = R$. We assume that the output switches symmetrically about zero volts, with the high saturated output denoted by $V_H = V_P$ and the low saturated output denoted by $V_L = -V_P$. If v_O is low, or $v_O = -V_P$, then $v_+ = -(\frac{1}{2})V_P$. When v_X drops just slightly below v_+, the output switches high so that $v_O = +V_P$ and $v_+ = +(\frac{1}{2})V_P$. The R_XC_X network sees a positive step-increase in voltage, so capacitor C_X begins to charge and voltage v_X starts to increase toward a final value of V_P.

The general equation for the voltage across a capacitor in an RC network is

$$v_X = v_{\text{Final}} + (v_{\text{Initial}} - v_{\text{Final}})e^{-t/\tau} \tag{15.82}$$

where v_{Initial} is the initial capacitor voltage at $t = 0$, v_{Final} is the final capacitor voltage at $t = \infty$, and τ is the time constant. We can now write

$$v_X = V_P + \left(-\frac{V_P}{2} - V_P\right)e^{-t/\tau_x} \tag{15.83(a)}$$

or

$$v_X = V_P - \frac{3V_P}{2}e^{-t/\tau_x} \tag{15.83(b)}$$

where $\tau_x = R_XC_X$. Voltage v_X increases exponentially with time toward a final voltage V_P. However, when v_X becomes just slightly greater than $v_+ = +(1/2)V_P$, the output switches to its low state of $v_O = -V_P$ and $v_+ = -(\frac{1}{2})V_P$. The R_XC_X network sees a negative step change in voltage, so capacitor C_X now begins to discharge and voltage v_X starts to decrease toward a final value of $-V_P$. We can now write

$$v_X = -V_P + \left[+\frac{V_P}{2} - (-V_P)\right]e^{-(t-t_1)/\tau_x} \tag{15.84(a)}$$

or

$$v_X = -V_P + \frac{3V_P}{2}e^{-(t-t_1)/\tau_x} \tag{15.84(b)}$$

where t_1 is the time at which the output switches to its low state. The capacitor voltage then decreases exponentially with time. When v_X decreases to $v_+ = -(\frac{1}{2})V_P$, the output again switches to its high state. The process continues to repeat itself, which means that this positive-feedback circuit oscillates producing a square-wave output signal. Figure 15.39 shows the output voltage v_O and the capacitor voltage v_X versus time.

Time t_1 can be found from Equation (15.83(b)) by setting $t = t_1$ when $v_X = V_P/2$, or

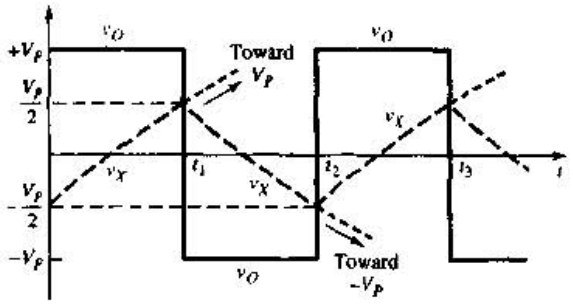


Figure 15.39 Output voltage and capacitor voltage versus time for Schmitt trigger oscillator

$$\frac{V_P}{2} = V_P - \frac{3V_P}{2}e^{-t_1/\tau_x} \tag{15.85}$$

Solving for t_1, we find that

$$t_1 = \tau_x \ln 3 = 1.1R_XC_X \tag{15.86}$$

From a similar analysis using Equation (15.84(b)), we find that the difference between t_2 and t_1 is also $1.1R_XC_X$; therefore, the period of oscillation T is

$$T = 2.2R_XC_X \tag{15.87}$$

and the frequency of oscillation is

$$f = \frac{1}{T} = \frac{1}{2.2R_XC_X} \tag{15.88}$$

As an example of an application of this circuit, a variable frequency oscillator is created by letting R_X be a variable resistor.

Design Example 15.8 Objective: Design a Schmitt trigger oscillator for a particular frequency.

Consider the oscillator in Figure 15.38. Design the circuit to oscillate at $f_o = 1$ kHz.

Solution: Using Equation (15.88), we can write

$$R_XC_X = \frac{1}{2.2f_o} = \frac{1}{2.2(10^3)} = 4.55 \times 10^{-4}$$

If $C_X = 0.1\,\mu$F, then $R_X = 4.55\,$kΩ.

Comment: A larger frequency of oscillation can easily be obtained by using a smaller capacitor value.

The **duty cycle** of the oscillator is defined as the percentage of time that the output voltage v_O is in its high state. For the circuit just considered, the duty cycle is 50 percent, as seen in Figure 15.39. This is a result of the symmetrical output voltages $+V_P$ and $-V_P$. If asymmetrical output voltages are used, then the duty cycle changes from the 50 percent value.

Test Your Understanding

***15.15** For the Schmitt trigger oscillator in Figure 15.38, the saturation output voltages are $+10\,V$ and $-5\,V$. $R_1 = R_2 = 20\,k\Omega$, $R_X = 50\,k\Omega$, and $C_X = 0.01\,\mu F$. Determine the frequency of oscillation and the duty cycle. Sketch v_O and v_X versus time over two periods of the oscillation. (Ans. $f = 866\,Hz$, duty cycle = 39.7%)

15.16 The Schmitt trigger oscillator is shown in Figure 15.38. The saturation output voltages are $\pm 10\,V$, and $R_1 = 10\,k\Omega$, $R_2 = 20\,k\Omega$, $R_X = 10\,k\Omega$, and $C_X = 0.1\,\mu F$. Determine the frequency of oscillation and the duty cycle. Sketch v_O and v_X versus time over two periods of oscillation. (Ans. $f = 722\,Hz$, duty cycle = 50%)

15.4.2 Monostable Multivibrator

A **monostable multivibrator** has one stable state, in which it can remain indefinitely if not disturbed. However, a trigger pulse can force the circuit into a quasi-stable state for a definite time, producing an output pulse with a particular height and width. The circuit then returns to its stable state until another trigger pulse is applied. The monostable multivibrator is also called a **one-shot**.

A monostable multivibrator is created by modifying the Schmitt trigger oscillator as shown in Figure 15.40. A clamping diode D_1 is connected in parallel with C_X. In the stable state, the output is high and voltage v_X is held low by the conducting diode D_1.

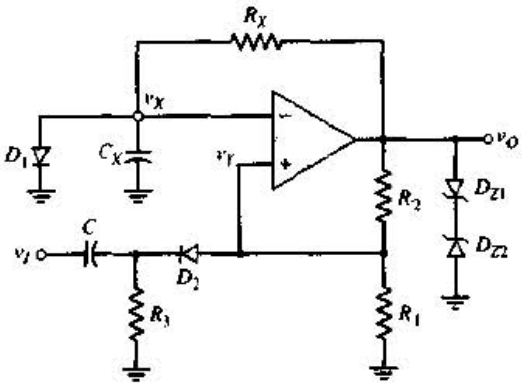


Figure 15.40 Schmitt trigger monostable multivibrator

The trigger circuit is composed of the capacitor C, resistor R_3, and diode D_2, and is connected to the noninverting terminal of the comparator. The value of R_3 is chosen to be much larger than R_1, so that voltage v_Y is determined primarily by a voltage divider of R_1 and R_2. We then have

$$v_Y \cong \left(\frac{R_1}{R_1 + R_2}\right) V_P \equiv \beta V_P \tag{15.89}$$

where V_P is the sum of the forward and breakdown voltages of D_{Z1} and D_{Z2}, or $V_P = (V_{\gamma 1} + V_{Z2})$. This voltage is the positive saturated output voltage.

The circuit is triggered by a negative-going step voltage applied to capacitor C. This action forward-biases diode D_2 and pulls the voltage v_γ below v_γ. Since the comparator then sees a larger voltage at the inverting terminal, the output switches to its low state of

$$v_O = -V_P = -(V_{\gamma 2} + V_{Z1})$$

Voltage v_γ then becomes

$$v_\gamma \cong -\left(\frac{R_1}{R_1 + R_2}\right) V_P \equiv -\beta V_P \tag{15.90}$$

causing D_2 to become reverse biased, thus isolating the oscillator circuit from the input triggering network. The negative-step change in v_O causes voltage v_X to decrease exponentially with a time constant of $\tau_x = R_X C_X$ toward a final value of $-V_P$. Diode D_1 is reverse biased during this time. When v_X drops just below the value of v_γ given by Equation (15.90), the output switches back to its positive saturated value of $+V_P$. The capacitor voltage v_X then starts to increase exponentially toward a final value of $+V_P$. When v_X reaches V_γ, diode D_1 again becomes forward biased, v_X is clamped at V_γ, and the output remains in its high state.

The waveforms of v_O and v_X versus time are shown in Figure 15.41. After the output has switched back to its high state, the capacitor voltage v_X must return to its quiescent value of $v_X = V_\gamma$. This implies that there is a **recovery time** of $(T' - T)$ during which the circuit should not be retriggered.

For $t > 0$, voltage v_X can be written in the same general form as Equation (15.82), as follows:

$$v_X = -V_P + (V_\gamma - (-V_P))e^{-t/\tau_x} \tag{15.91}$$

where $\tau_x = R_X C_X$. At $t = T$, $v_X = -\beta V_P$ and the output switches high. The pulse width is then

$$T = \tau_x \ln\left[\frac{1 + (V_\gamma / V_P)}{(1 - \beta)}\right] \tag{15.92}$$

If we assume $V_\gamma \ll V_P$ and if we let $R_1 = R_2$ such that $\beta = 1/2$, then the pulse width is $T = 0.69\tau_x$. We can show that for $V_\gamma \ll V_P$ and $\beta = 1/2$, the recovery time is $(T' - T) = 0.4\tau_x$. There are alternative circuits with shorter recovery times, but we will not consider them here.

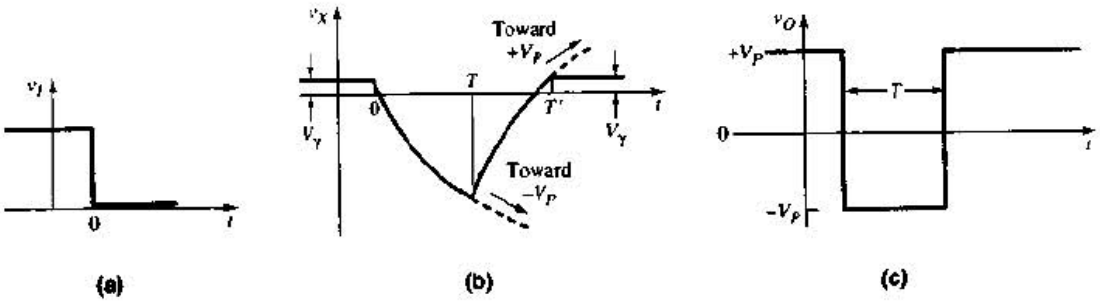


Figure 15.41 Schmitt trigger monostable multivibrator voltages versus time (a) input trigger pulse, (b) capacitor voltage, and (c) output pulse

Design Example 15.9 **Objective:** Design a monostable multivibrator to produce a given pulse width.

Consider the circuit in Figure 15.40 with parameters $V_P = 10\,\text{V}$, $V_\gamma = 0.7\,\text{V}$, and $R_1 = R_2 = 20\,\text{k}\Omega$. Design the circuit to produce a pulse that is 1 μs wide.

Solution: Since $V_\gamma \ll V_P$ and $R_1 = R_2$, then from Equation (15.92), we have

$$T = 0.69\tau_x$$

or

$$\tau_x = R_X C_X = \frac{T}{0.69} = \frac{1}{0.69} = 1.45\,\mu\text{s}$$

If $R_X = 10\,\text{k}\Omega$, then $C_X = 145\,\text{pF}$.

Comment: In actual monostable multivibrator ICs, R_X and C_X are external elements to allow for variable times.

Test Your Understanding

***15.17** For the monostable circuit shown in Figure 15.40, the parameters are: $V_P = 12\,\text{V}$, $V_\gamma = 0.7\,\text{V}$, $C_X = 0.1\,\mu\text{F}$, $R_1 = 10\,\text{k}\Omega$, and $R_2 = 90\,\text{k}\Omega$. (a) Find the value of R_X that will result in a 50 μs output pulse. (b) Using the results of part (a), find the recovery time. (Ans. (a) $R_X = 3.09\,\text{k}\Omega$ (b) 47.9 μs)

15.18 Consider the monostable multivibrator in Figure 15.40 with parameters: $V_P = 8\,\text{V}$, $V_\gamma = 0.7\,\text{V}$, $C_X = 0.01\,\mu\text{F}$, $R_X = 10\,\text{k}\Omega$, $R_1 = 20\,\text{k}\Omega$, and $R_2 = 40\,\text{k}\Omega$. Determine the output pulse width and recovery time. (Ans. $T = 48.9\,\mu\text{s}$, $t_2 = 37.8\,\mu\text{s}$)

15.4.3 The 555 Circuit

The **555 monolithic integrated circuit timer** was first introduced by Signetics Corporation in 1972 in bipolar technology. It quickly became an industry standard for timing and oscillation functions. Many manufacturers produce a version of a 555 IC, some in CMOS technology. The 555 is a general-purpose IC that can be used for precision timing, pulse generation, sequential timing, time delay generation, pulse width modulation, pulse position modulation, and linear ramp generation. The 555 can operate in both astable and monostable modes, with timing pulses ranging from microseconds to hours. It also has an adjustable duty cycle and can generally source or sink output currents up to 200 mA.

Basic Operation

The basic block diagram of the 555 IC is shown in Figure 15.42(a). The circuit consists of two comparators, which drive an RS flip-flop, an output buffer, and a transistor that discharges an external timing capacitor. The actual circuit of an LM555 timer is shown in Figure 15.42(b).

The **RS flip-flop** is a digital circuit that will be considered in detail in a later chapter. Here, we will describe only the basic digital function of the flip-flop, so

(a)

Figure 15.42 (a) Basic block diagram, 555 IC timer circuit and (b) circuit diagram, LM555 timer circuit

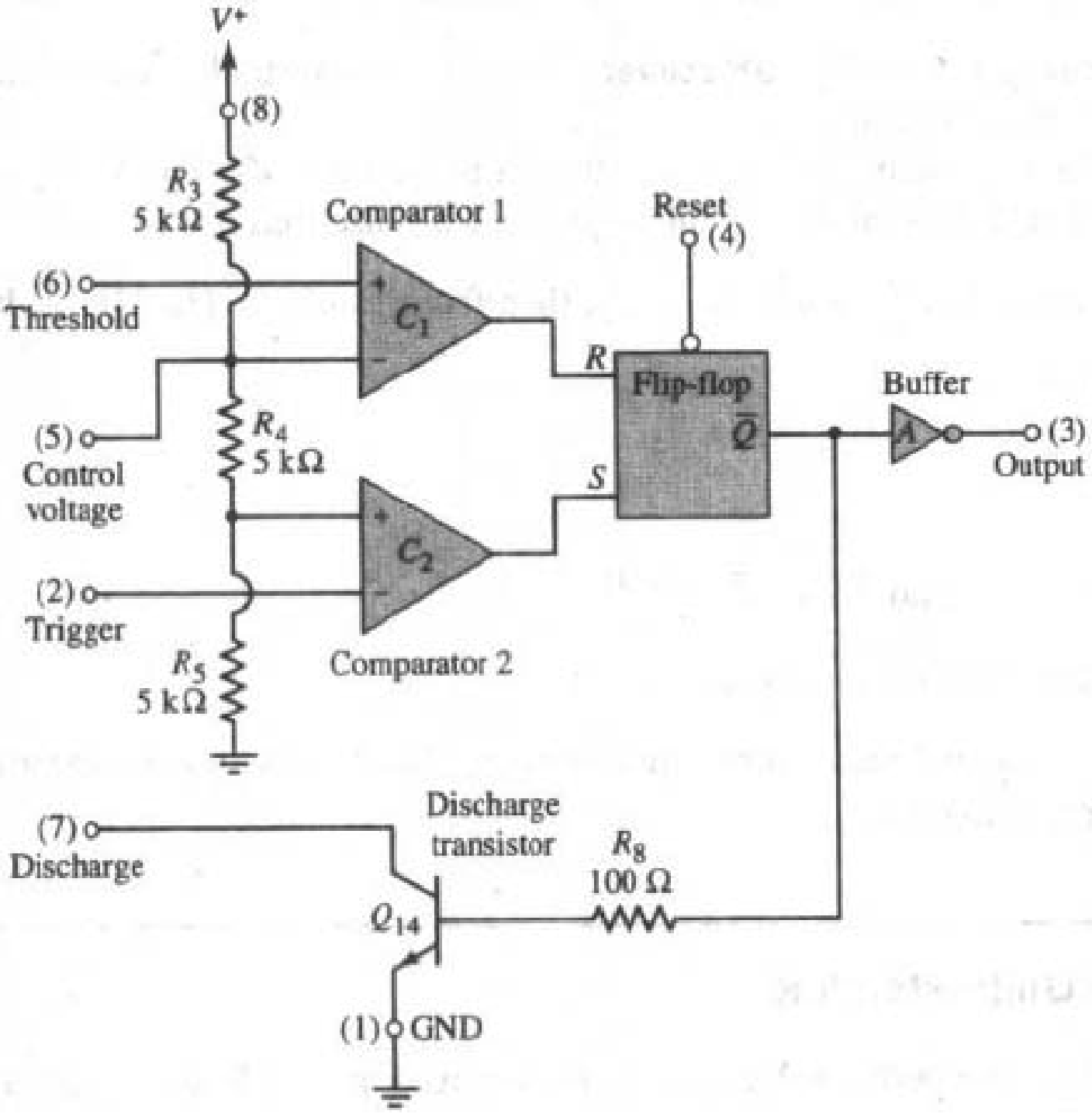
that the operation of the 555 timer can be explained. When the input R is high and input S is low, output $\overline{Q}$ is high. The complementary state occurs when R is low and S is high, producing a low $\overline{Q}$ output. If both R and S are low, then output $\overline{Q}$ remains in its previous state.

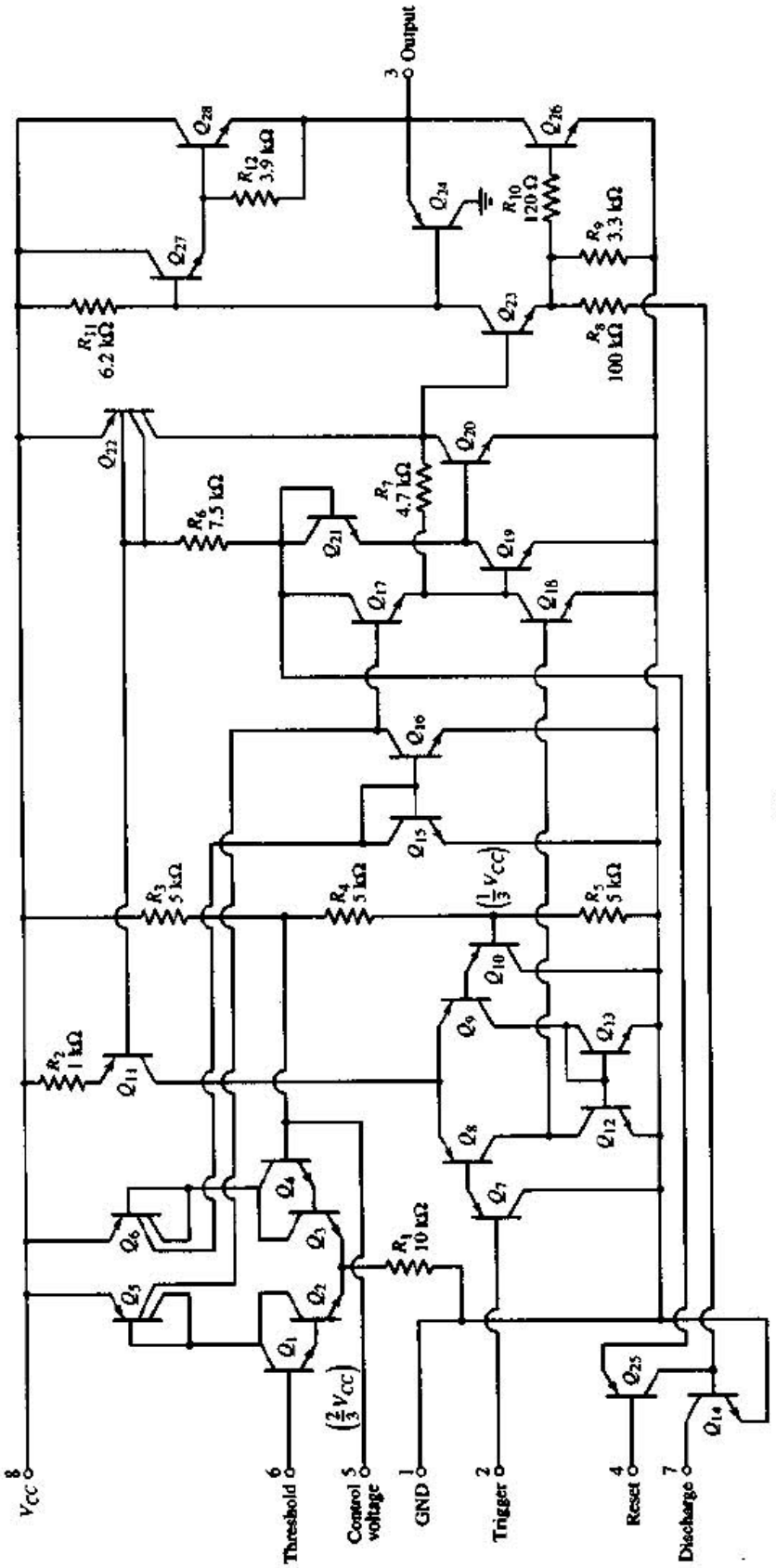
Comparator 1 is called the **threshold comparator**, which compares its input with an internal voltage reference set at $(\frac{2}{3})V^+$ by the voltage divider R_3, R_4, and R_5. When the input level exceeds this reference level, the threshold comparator output goes high, producing a high output at flip-flop terminal $\overline{Q}$. This turns the discharge transistor on and an external timing capacitor (not shown in this figure) starts to discharge.

The internal control voltage node is connected to an external terminal. This provides external control of the reference level, should the timing period need to be modified. When not in active use, this terminal should be bypassed to ground with a 0.01 μF capacitor, to improve the circuit's noise immunity.

Comparator 2, called the **trigger comparator**, compares its input trigger voltage to an internal voltage reference set to $(\frac{1}{3})V^+$ by the same voltage divider as before. When the output trigger level is reduced below this reference level, the trigger comparator output goes high, causing the RS flip-flop to reset. Output $\overline{Q}$ goes low and the discharge transistor turns off. This comparator triggers on the leading edge of a negative-going input pulse.

The output stage of the 555 IC is driven by output $\overline{Q}$ of the RS flip-flop. This output is usually a totem-pole push-pull circuit, or a simple buffer, and is generally capable of sourcing or sinking 200 mA.


V+
(8)
R3
5 kΩ
Comparator 1
Reset
(4)
(6)
Threshold
C1
R
Flip-flop
Q̄
Buffer
(5)
Control
voltage
R4
5 kΩ
S
(3)
Output
C2
(2)
Trigger
R5
5 kΩ
Comparator 2
(7)
Discharge
Discharge
transistor
R8
100 Ω
Q14
(1) GND



(b)

Figure 15.42 (continued)

An external reset input to the RS flip-flop overrides all other inputs and is used to initiate a new timing cycle by turning the discharge transistor on. The reset input must be less than 0.4 V to initiate a reset. When not actively in use, the reset terminal should be connected to V^+ to prevent a false reset.

Monostable Multivibrator

A monostable multivibrator, also called a one-shot, operates by charging a timing capacitor with a current set by an external resistance. When the one-shot is triggered, the charging network cycles only once during the timing interval. The total timing interval includes the recovery time needed for the capacitor to charge up to the threshold level.

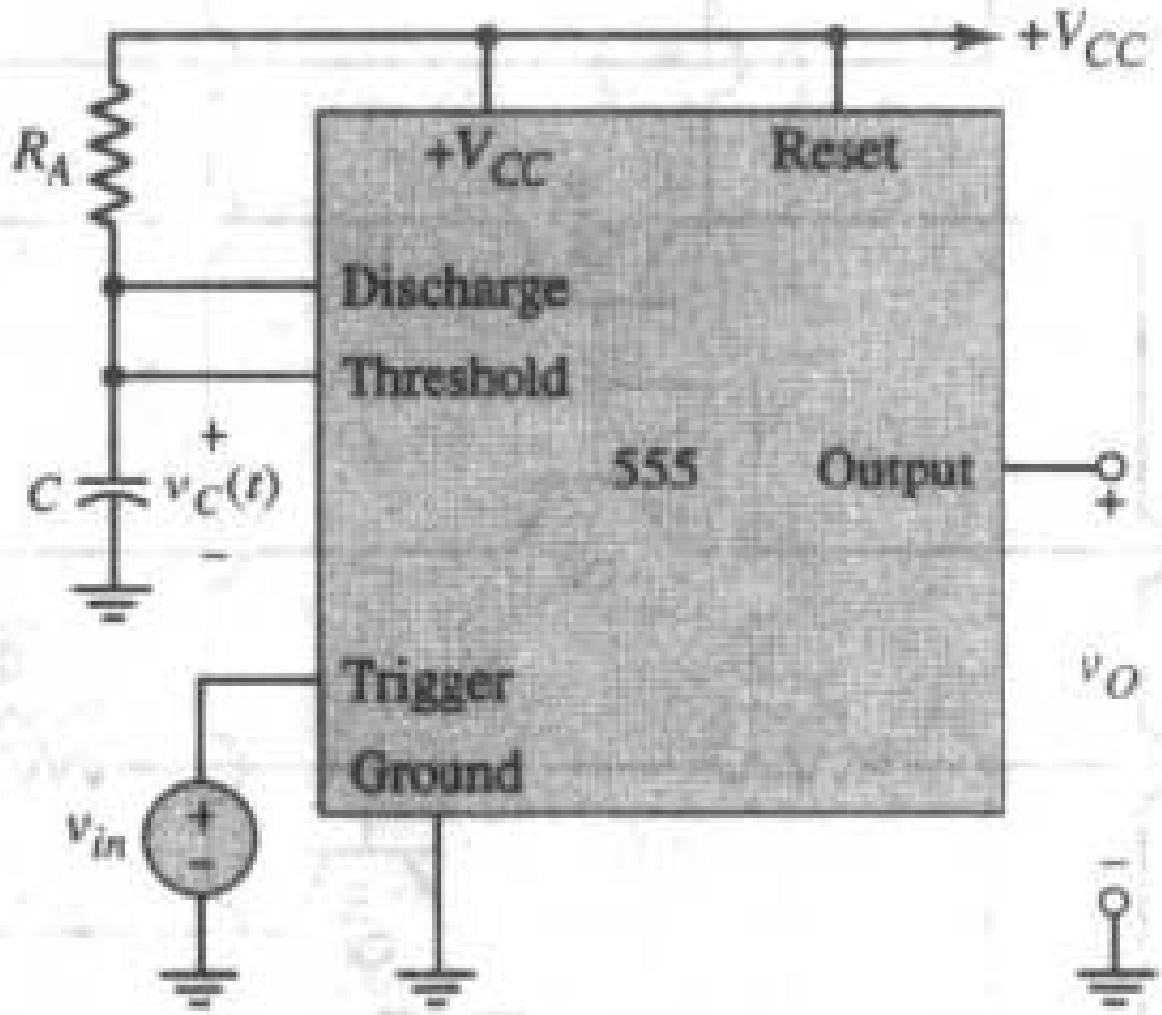
The external circuitry and connections for the 555 to be used as a one-shot multivibrator are shown in Figure 15.43. With a high voltage V^+ applied to the trigger input, the trigger comparator output is low, the flip-flop output $\overline{Q}$ is high, the discharge transistor is turned on, and the timing capacitor C is discharged to nearly ground potential. The output of the 555 circuit is then low, which is the quiescent state of the one-shot.

Figure 15.43 The 555 circuit connected as a monostable multivibrator

When a negative-going pulse is applied to the trigger input, the output of the trigger comparator goes high when the trigger pulse drops below $(\frac{1}{3})V^+$. Output $\overline{Q}$ goes low, which means that the output of the 555 goes high, and the discharge transistor turns off. The output of the 555 remains high even if the trigger pulse returns to its initial high value, because the reset input to the flip-flop is still low. The timing capacitor charges up exponentially toward a final value of V^+ through resistor R. The capacitor voltage is given by

$$v(t) = V^+\left(1 - e^{-t/RC}\right) \tag{15.93}$$

When $v(t) = (\frac{2}{3})V^+$, the threshold comparator output goes high, resetting the flip-flop. Output $\overline{Q}$ then goes high and the output of the 555 goes low. The high output at $\overline{Q}$ also turns on the discharge transistor, allowing the timing capacitor to discharge to near zero volts. The circuit thus returns to its quiescent state.


+V_{CC}
R_A
+V_{CC}
Reset
Discharge
Threshold
555
Output
C
$v_C(t)$
Trigger
Ground
v_{in}
v_O

The width of the output pulse is determined from Equation (15.93). If we set $v(t) = (\frac{2}{3})V^+$ and $t = T$, then

$$\left(\frac{2}{3}\right)V^+ = V^+\left(1 - e^{-T/RC}\right) \tag{15.94}$$

Solving for T, we have

$$T = RC\ln(3) = 1.1RC \tag{15.95}$$

The width of the output pulse is a function of only the external time constant RC; it is independent of the supply voltage V^+ and any internal circuit parameters. The triggering input pulse must be of a shorter duration than T. The output pulse height is a function of V^+ as well as of the internal circuitry. For a bipolar 555, the output pulse amplitude is approximately 1.7 V below supply voltage V^+.

When the output is high and the timing capacitor is charging, another trigger input pulse will have no effect on the circuit. If desired, the circuit can be reset during this period by applying a low input to the reset terminal. The output will return to zero and will remain in this quiescent state until another trigger pulse is applied.

Design Example 15.10 **Objective:** Design the 555 IC as a monostable multivibrator with a 100 μs output pulse.

Consider the circuit in Figure 15.43. Let $C = 15$ nF.

Solution: Using Equation (15.95), we find that

$$R = \frac{T}{1.1C} = \frac{100 \times 10^{-6}}{(1.1)(15 \times 10^{-9})} \Rightarrow 6.06\ \text{k}\Omega$$

Comment: To a very good approximation, the pulse width is a function of only the external resistor and capacitance values. A wide range of pulse widths can be obtained by changing these component values.

Astable Multivibrator

Figure 15.44 shows a typical external circuit connection for the 555 operating as an astable multivibrator, also called a timer circuit or clock. The threshold input and trigger input terminals are connected together. In the astable mode, the timing capacitor C charges through $R_A = R_B$ until $v(t)$ reaches $(\frac{2}{3})V^+$. The threshold comparator output then goes high, forcing the flip-flop output $\overline{Q}$ to go high. The discharge transistor turns on, and the timing capacitor C discharges through R_B and the discharge transistor. The capacitor voltage decreases until it reaches $(\frac{1}{3})V^+$, at which point the trigger comparator switches states and sends $\overline{Q}$ low. The discharge transistor turns off, and the timing capacitor begins to recharge. When $v(t)$ reaches the threshold level of $(\frac{2}{3})V^+$, the cycle repeats itself.

When the timing capacitor is charging, during the time $0 < t < T_C$, the capacitor voltage is

$$v(t) = \frac{1}{3}V^+ + \frac{2}{3}V^+\left(1 - e^{-t/\tau_A}\right) \tag{15.96}$$

where $\tau_A = (R_A + R_B)C$. At time $t = T_C$, the capacitor voltage reaches the threshold level, or

$$v(T_C) = \frac{2}{3}V^+ = \frac{1}{3}V^+ + \frac{2}{3}V^+\left(1 - e^{-T_C/\tau_A}\right) \tag{15.97}$$

Solving Equation (15.97) for the timing capacitor charging time T_C yields

$$T_C = \tau_A \ln(2) = 0.693(R_A + R_B)C \tag{15.98}$$

When the timing capacitor is discharging, during the time $0 < t' < T_D$, the capacitor voltage is

$$v(t') = \frac{2}{3}V^+ e^{-t'/\tau_B} \tag{15.99}$$

where $\tau_B = R_B C$. At time $t' = T_D$, the capacitor voltage reaches the trigger level and

$$v(T_D) = \frac{1}{3}V^+ = \frac{2}{3}V^+ e^{-T_D/\tau_B} \tag{15.100}$$

Solving Equation (15.100) for the timing capacitor discharge time T_D yields

$$T_D = \tau_B \ln(2) = 0.693 R_B C \tag{15.101}$$

The period T of the astable multivibrator cycle is the sum of the charging period T_C and the discharging period T_D. The frequency of oscillation is therefore

$$f = \frac{1}{T} = \frac{1}{T_C + T_D} = \frac{1}{0.693(R_A + 2R_B)C} \tag{15.102}$$

The duty cycle is defined as the percentage of time the output is high during one period of oscillation. During the charging time T_C, the output is high; during the discharging time, the output is low. The duty cycle is therefore

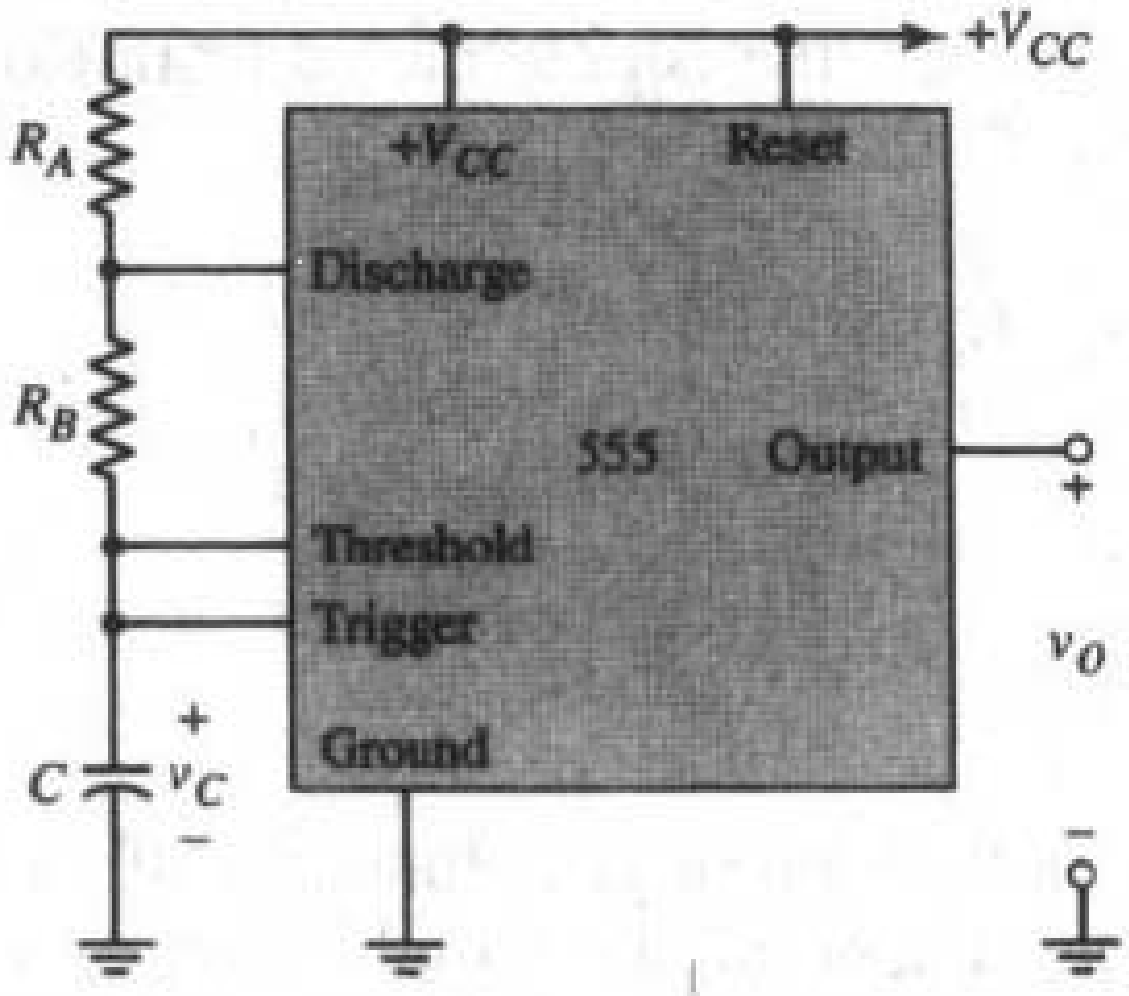


Figure 15.44 Astable multivibrator 555 circuit

$$\text{duty cycle} = \frac{T_C}{T} \times 100\% = \frac{R_A + R_B}{R_A + 2R_B} \times 100\% \tag{15.103}$$

Equation (15.103) shows that the duty cycle for this circuit is always greater than 50 percent. The duty cycle approaches 50 percent for $R_A \ll R_B$ and 100 percent for $R_B \ll R_A$. Alternative circuits can provide duty cycles of less than 50 percent.

Design Example 15.11 **Objective:** Design the 555 IC as an astable multivibrator for a specific frequency and duty cycle.

Consider the circuit in Figure 15.44. Design the circuit such that the frequency is 50 kHz and the duty cycle is 75 percent. Let $C = 1$ nF.

Solution: The frequency of oscillation, as given by Equation (15.102), is

$$f = \frac{1}{0.693(R_A + 2R_B)C}$$

Therefore,

$$R_A + 2R_B = \frac{1}{(0.693)fC} = \frac{1}{(0.693)(50 \times 10^3)(1 \times 10^{-9})} \Rightarrow 28.9\,\text{k}\Omega \tag{15.104}$$

The duty cycle, given by Equation (15.103), is

$$\text{Duty cycle} = 0.75 = \frac{R_A + R_B}{R_A + 2R_B}$$

which yields

$$R_A = 2R_B \tag{15.105}$$

Combining Equations (15.104) and (15.105), we find that

$$R_A = 14.5\,\text{k}\Omega \quad \text{and} \quad R_B = 7.23\,\text{k}\Omega$$

Comment: A wide range of oscillation frequencies can be obtained by changing the resistance and capacitance values.

Other Applications

When the 555 is connected in the monstable mode, an external signal applied to the control voltage terminal will change the charging time of the timing capacitor and the pulse width. If the one-shot is triggered with a continuous pulse train, the output pulse width will be modulated by the external signal. This circuit is known as a **pulse width modulator (PWM)**.

A **pulse position modulator** can also be developed using the astable mode. A modulating signal applied to the control voltage terminal will vary the pulse position, which will be controlled by the modulating signal in a manner similar to the PWM.

Finally, a **linear ramp generator** can be constructed, again using the 555 monostable mode. The normal charging pattern of the timing capacitor is exponential because of the RC circuit. If resistor R is replaced by a constant current source, a linear ramp will be generated.

Test Your Understanding

15.19 The 555 IC is connected as an astable multivibrator. Let $R_A = 20\,\text{k}\Omega$, $R_B = 80\,\text{k}\Omega$, and $C = 0.01\,\mu\text{F}$. Determine the frequency of oscillation and the duty cycle. (Ans. $f = 802\,\text{Hz}$, duty cycle = 55.6%)

D15.20 Design the 555 IC as an astable multivibrator to deliver a 1 kHz signal with a 55 percent duty cycle. (Ans. For example, $C = 0.01\,\mu\text{F}$, $R_A = 26\,\text{k}\Omega$, $R_B = 118\,\text{k}\Omega$)

15.5 INTEGRATED CIRCUIT POWER AMPLIFIERS

Most IC power amplifiers consist of a high-gain small-signal amplifier cascaded with a class-AB output stage. Some IC power amplifiers are a fixed-gain circuit with negative feedback incorporated on the chip, while others use a current gain output stage and negative feedback external to the chip. We consider three examples of IC power amplifiers in this section.

15.5.1 LM380 Power Amplifier

The LM380 is a popular fixed-gain power amplifier capable of an ac power output up to 5 W. Figure 15.45 is a simplified circuit diagram of the amplifier. The input stage is a Darlington pair configuration composed of Q_1 through Q_4 and an active load formed by Q_5 and Q_6.

The input stage is biased by currents through resistors R_{1A}, R_{1B}, and R_2. Transistor Q_3 is biased by a current from power supply V^+, through the diode-connected transistor Q_{10} and resistors R_{1A} and R_{1B}. Transistor Q_4 is biased by a current from the output terminal through R_2. For zero input voltages, the currents in Q_3 and Q_4 are nearly equal. Assuming matched input transistors and neglecting base currents, we find that

$$I_{C3} = \frac{V^+ - 3V_{EB}}{R_{1A} + R_{2A}} \tag{15.106}$$

and

$$I_{C4} = \frac{V_O - 2V_{EB}}{R_2} \tag{15.107}$$

Since $I_{C3} = I_{C4}$, we can find the quiescent output voltage by combining Equations (15.106) and (15.107), or

$$V_O = 2V_{EB} + \frac{R_2}{R_{1A} + R_{2B}}(V^+ - 3V_{EB}) = \frac{1}{2}V^+ + \frac{1}{2}V_{EB} \tag{15.108}$$

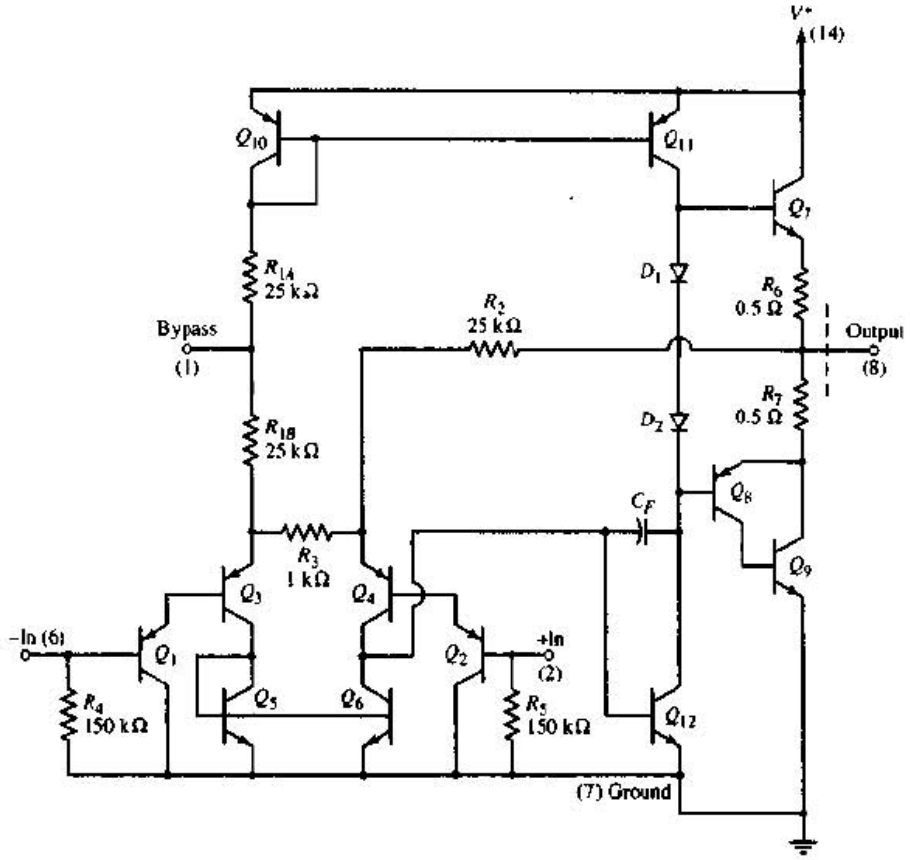


Figure 15.45 The LM380 power amplifier

The quiescent output voltage is approximately half the power supply voltage, which allows for a maximum output voltage swing and for maximum power to be delivered to a load. The feedback from the output to the emitter of Q_4, through R_2, stabilizes the quiescent output voltage at this value.

The output signal of the diff-amp is the input signal to the base of Q_{12}, which is connected in a common-emitter configuration in which Q_{11} acts as an active load. The output signal from the collector of Q_{12} is the input to the class-AB output stage, and capacitor C_F provides frequency compensation.

The class-AB complementary push-pull emitter-follower output stage comprises transistors Q_7, Q_8, and Q_9 and diodes D_1 and D_2. Transistor Q_7, which is the npn half of the push-pull output stage, sources current to the load. Transistors Q_8 and Q_9 operate as a composite pnp transistor, with the overall current gain equal to the product of the current gains of each transistor. This composite transistor is the pnp half of the push-pull output stage sinking current from the load. Diodes D_1 and D_2 provide the quiescent bias for class-AB operation.

The closed-loop gain is determined from the ac equivalent circuit in Figure 15.46. A differential-input voltage is applied at the input, with $V_{id}/2$ applied at the noninverting terminal and $-V_{id}/2$ applied at the inverting terminal. An external bypass capacitor is connected at the node between R_{1A} and R_{1B}, putting this node at signal ground. The second stage and output stage are

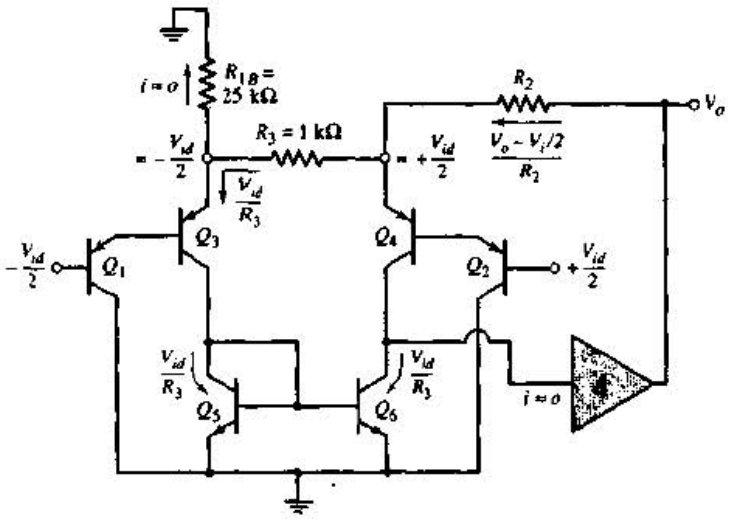


Figure 15.46 The ac equivalent circuit, LM380 power amplifier

represented by amplifier A. The input impedance is assumed to be large, which means that the input current is assumed to be negligible.

Since the input stage is an emitter-follower configuration, the signal voltage is approximately $+V_{id}/2$ at the emitter of Q_4 and is approximately $-V_{id}/2$ at the emitter of Q_3. Comparing the resistor values of R_3 and R_{1B}, we see the signal current in R_{1B} is negligible. The signal current in Q_3 is equal to that in R_3, and the current-mirror configuration of Q_5 and Q_6 implies that the current in Q_6 is also V_{id}/R_3. Summing the currents at the emitter of Q_4, we obtain

$$\frac{V_o - V_{id}/2}{R_2} = \frac{V_{id}}{R_3} + \frac{V_{id}}{R_3} \tag{15.109}$$

which yields the closed-loop voltage gain

$$\frac{V_o}{V_{id}} = \frac{1}{2} + \frac{2R_2}{R_3} \cong 50 \tag{15.110}$$

Equation (15.110) shows that the LM380 has a fixed gain of approximately 50.

The LM380 is designed to operate in the range of 12–22 V from a single supply V^+. The value of V^+ depends on the power requirements. Figure 15.47 shows the relationship between device dissipation, output power, and supply voltage for an 8 Ω load. As the output signal increases, harmonic distortion in the sinusoidal signal increases because the output transistor is approaching the saturation region. The lines marked 3% and 10% are the points at which harmonic distortion reaches 3% and 10%, respectively.

Example 15.12 **Objective:** Determine the output voltage and conversion efficiency for an LM380 power amplifier.

The required power for an 8 Ω is to be 4 W, with minimum distortion in the output signal.

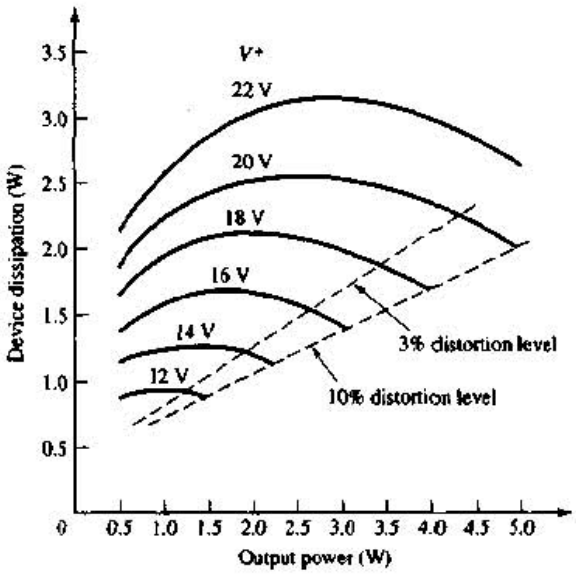


Figure 15.47 LM380 power amplifier characteristics

Solution: From the curves in Figure 15.47, for an output of 4 W, minimum distortion occurs when the supply voltage is a maximum, or $V^+ = 22\,\text{V}$. For 4 W to be delivered to the 8 Ω load, the peak output signal voltage is determined by

$$\overline{P}_L = 4 = \frac{V_P^2}{2R_L} = \frac{V_P^2}{2(8)}$$

which yields $V_P = 8\,\text{V}$.

The power dissipated in the device is 3 W, which means that the conversion efficiency is $4/(3+4) \rightarrow 57$ percent.

Comment: A reduction in the harmonic distortion means that the conversion efficiency is less than the theoretical value of 78.5 percent for the class-B output stages. However, a conversion efficiency of 57 percent is still substantially larger than would be obtained in any class-A amplifier.

Test Your Understanding

15.21 The supply voltage to an LM380 power amplifier, as shown in Figure 15.45, is 12 V. With a sinuosidal input signal, an average output power of 1 W must be delivered to an 8 Ω load. (a) Determine the peak output voltage and peak output current. (b) When the output voltage is at its peak value, calculate the instantaneous power being dissipated in Q_7. (Ans. (a) $V_p = 4\,\text{V}$, $I_p = 0.5\,\text{A}$ (b) $P_Q = 4\,\text{W}$)

15.5.2 PA12 Power Amplifier

The basic circuit diagram of the PA12 amplifier is shown in Figure 15.48. The input signal to the class-AB output stage is from a small-signal high-gain

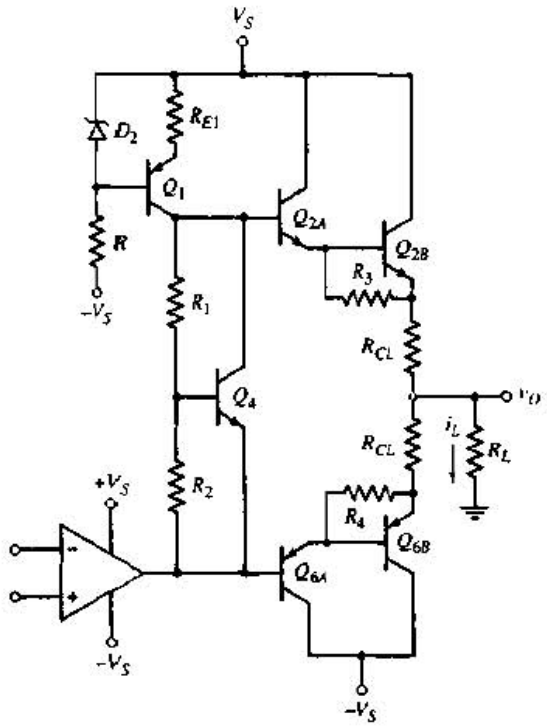


Figure 15.48 PA12 power amplifier

op-amp. The power supply voltages are in the range of $10 \leq V_S \leq 50\,\text{V}$, the peak output current is in the range $-15 \leq I_L \leq +15\,\text{A}$, and the maximum internal power dissipation is 125 W. The output stage is a class-AB configuration using npn and pnp Darlington pair transistors. The bias for the output transistors is established by the V_{BE} multiplier circuit composed of R_1, R_2, and Q_4. Also, external feedback is required.

Design Example 15.13 Objective: Design the supply voltage required to meet a specific conversion efficiency in the PA12 power amplifier.

Consider the power amplifier in Figure 15.48 with a load resistance of $10\,\Omega$. The required average power delivered to the load is 20 W. Determine the power supply voltage such that the conversion efficiency is 50 percent.

Solution: For an average of 20 W delivered to the load, the peak output voltage is

$$V_p = \sqrt{2R_L P_L} = \sqrt{2(10)(20)} = 20\,\text{V}$$

and the peak load current is

$$I_p = \frac{V_p}{R_L} = \frac{20}{10} = 2\,\text{A}$$

Assuming an ideal class-B condition, for a 50 percent conversion efficiency, the average power supplied by each V_S source must be 20 W. If we neglect power dissipation in the bias circuit, the average power supplied by each source is

$$P_S = V_S\left(\frac{V_p}{\pi R_L}\right)$$

and the required supply voltage is then

$$V_S = \frac{\pi R_L P_S}{V_p} = \frac{\pi(10)(20)}{20} = 31.4\,\text{V}$$

Comment: The actual conversion efficiency for class-AB operation is less than 50 percent. This reduced conversion efficiency ensures that harmonic distortion in the output signal is not severe.

Computer Simulation Verification: A computer simulation analysis of the circuit in Figure 15.48 was performed. The supply voltages were set at ±31.4 V and the input sinusoidal signal was adjusted so that the peak sinusoidal output voltage was 19.7 V across a 10 Ω load resistor. For these settings, the bias supply currents were 1.971 A. The average power delivered by the supply voltage sources is 39.4 W, so that the conversion efficiency is 49.25 percent, which is just slightly below the design value of 50 percent.

15.5.3 Bridge Power Amplifier

Figure 15.49 shows a bridge power amplifier that uses two op-amps. Amplifier A_1 is connected in a noninverting configuration; A_2 is connected in an inverting configuration. The magnitudes of the two gains are equal to each other. The load, such as an audio speaker, is connected between the two output terminals and is floating. A sinusoidal input signal produces output voltages v_{o1} and v_{o2}, which are equal in magnitude but 180 degrees out of phase. The voltage across the load is therefore twice as large as it would be if produced from a single op-amp.

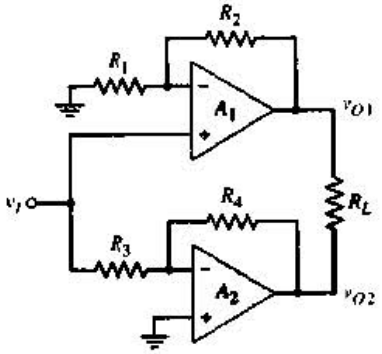


Figure 15.49 Bridge power amplifier

Test Your Understanding

15.22 Consider the bridge amplifier in Figure 15.49 with parameters $R_1 = R_3 = 20\,\text{k}\Omega$, $R_2 = 30\,\text{k}\Omega$, $R_4 = 50\,\text{k}\Omega$, and $R_L = 1.2\,\text{k}\Omega$. Assume the op-amps are biased at ±15 V, and the peak output voltage of each op-amp is limited to ±12 V. Determine: (a) the voltage gain of each op-amp circuit, (b) the average power that can be delivered to the load, and (c) the peak amplitude of the input voltage. (Ans. (a) $A_{v1} = 2.5$, $A_{v2} = -2.5$ (b) $\overline{P}_L = 0.24\,\text{W}$ (c) $V_{pi} = 4.8\,\text{V}$)

15.6 VOLTAGE REGULATORS

Another class of analog circuits that is used extensively in electronic systems is the voltage regulator. We briefly considered constant-voltage circuits, or voltage regulators, when we studied diode circuits and when we considered ideal op-amp circuits in Chapter 9. In this section, we will discuss examples of IC voltage regulators.

15.6.1 Basic Regulator Description

A **voltage regulator** is a circuit or device that provides a constant voltage to a load. The output voltage is controlled by the internal circuitry and is relatively independent of the load current supplied by the regulator.

A basic diagram of a voltage regulator is shown in Figure 15.50. It consists of three basic parts: a reference voltage circuit; an error amplifier, which is part of a feedback circuit; and a current amplifier, which supplies the required load current. The reference voltage circuit produces a voltage that is essentially independent of both supply voltage V^+ and temperature. As shown in the basic circuit of Figure 15.50, a fraction of the output voltage is fed back to the error amplifier which, through negative feedback, maintains the feedback voltage at a value equal to the reference voltage.

Figure 15.50 Basic circuit diagram of a voltage regulator

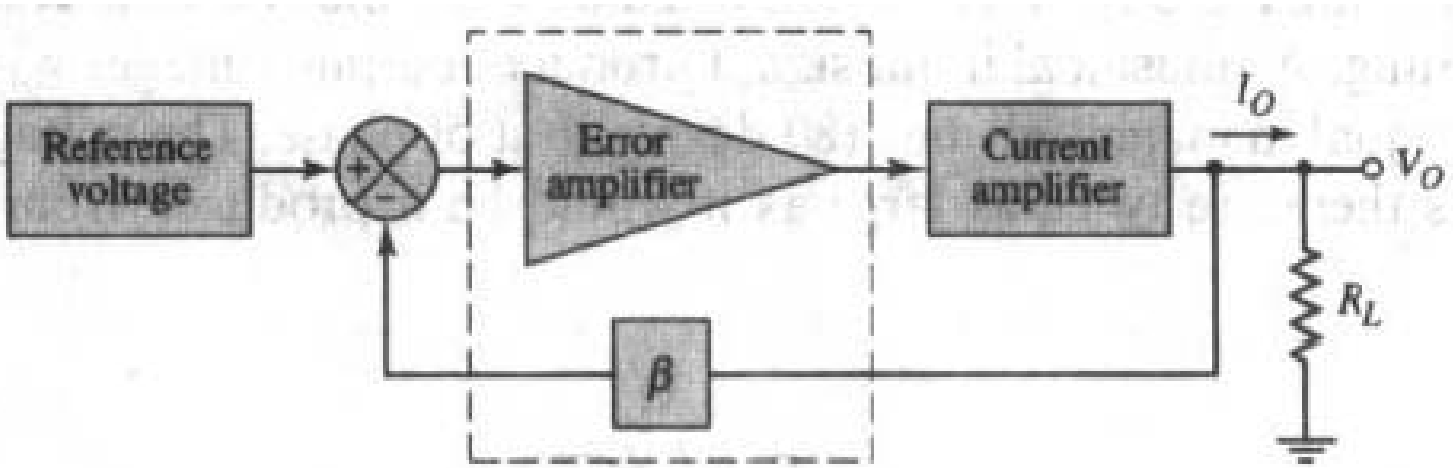
Since the regulator output voltage is derived from the reference voltage, any variation in that reference voltage, as the power supply voltage V^+ changes, also affects the output voltage. **Line regulation** is defined as the ratio of the change in output voltage to a given change in the input supply voltage, or

$$\text{Line regulation} = \frac{\Delta V_o}{\Delta V^+} \tag{15.111}$$

Line regulation is one figure of merit of voltage regulators. In many cases, the reference voltage circuit contains one or more Zener diodes. Line regulation is then a function of the Zener diode resistance and the effective resistance of the circuit biasing the diode.

15.6.2 Output Resistance and Load Regulation

The ideal voltage regulator is equivalent to an ideal voltage source in that the output voltage is independent of the output current and any output load impedance. In actual voltage regulators, however, the output voltage is a slight


Reference voltage
+
−
Error amplifier
Current amplifier
I_O
V_O
R_L
β

function of output current. This dependence is related to the output resistance of the regulator.

The output resistance is defined as the rate of change of output voltage with output current, or

$$R_{of} = -\frac{\Delta V_O}{\Delta I_O} \tag{15.112}$$

The change in V_O and I_O is caused by a change in the load resistance R_L. Everything else in the circuit remains constant. The negative sign in Equation (15.112) results from the voltage polarity and current direction, as shown in Figure 15.50. An increase in I_O produces a decrease in V_O; therefore, the output resistance R_{of} is positive. The output resistance of a voltage regulator should be small, so that a change in output current ΔI_O will result in only a small change in output voltage ΔV_O.

The notation R_{of} for the output resistance of the voltage regulator is the same as the term for the output resistance of a feedback circuit. This is appropriate since voltage regulators use feedback.

A second figure-of-merit for voltage regulators is load regulation. **Load regulation** is defined as the change in output voltage between a no-load current condition and a full-load current condition. Load regulation can be expressed as a percentage, or

$$\text{Load regulation} = \frac{V_O(\text{NL}) - V_O(\text{FL})}{V_O(\text{NL})} \times 100\% \tag{15.113}$$

where $V_O(\text{NL})$ is the output voltage for a zero-load current condition and $V_O(\text{FL})$ is the output voltage for a full-load or maximum load current condition.

In some applications, a zero-load current is impractical, and a load current that is approximately 1 percent of the full-load current is used as the no-load condition. In most cases, this condition provides an adequate definition for load regulation.

Example 15.14 **Objective:** Determine the output resistance and load regulation of a voltage regulator.

Assume the output voltage of a regulator is 5.0 V for a load current of 5 mA, and is 4.96 V for a load current of 1.5 A.

Solution: If we assume that the output voltage decreases linearly with load current, then the output resistance is

$$R_{of} = -\frac{\Delta V_O}{\Delta I_O} = -\left(\frac{5.0 - 4.96}{0.005 - 1.5}\right) \cong 0.0267\,\Omega$$

or

$$R_{of} \cong 27\,\text{m}\Omega$$

The load regulation is then

$$\text{Load regulation} = \frac{V_O(\text{NL}) - V_O(\text{FL})}{V_O(\text{NL})} \times 100\% = \frac{5.0 - 4.96}{5.0} \times 100\% = 0.80\%$$

Comment: The output resistance of a voltage regulator is usually not constant at all load currents, but the values are typically in the milliohm range. Also, a load regulation of 0.8% is typical of many voltage regulators.

15.6.3 Simple Series-Pass Regulator

Figure 15.51 shows a simple voltage regulator that includes an error amplifier (comparator) and series-pass transistors. The series-pass transistors, which are connected in a Darlington emitter-follower configuration, form the current amplifier. A resistive voltage divider allows a portion of the output voltage to be fed back to the error amplifier. The closed-loop feedback system acts to maintain this fraction of the output voltage at a value equal to the reference voltage.

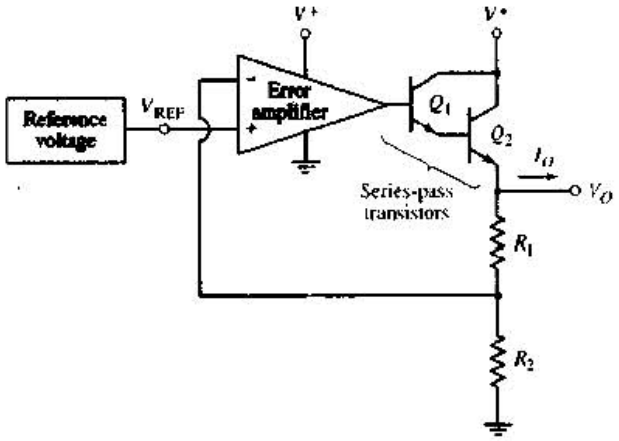


Figure 15.51 Basic series-pass voltage regulator

For an ideal system, we can write

$$\left(\frac{R_2}{R_1 + R_2}\right) V_O = V_{REF} \tag{15.114(a)}$$

or

$$V_O = V_{REF}\left(1 + \frac{R_1}{R_2}\right) \tag{15.114(b)}$$

Since the output of the feedback circuit is a shunt connection, the output resistance can be written, according to the results from Chapter 12, as

$$R_{of} = \frac{R_o}{1 + T} \tag{15.115}$$

where R_o is the output resistance of the open-loop system and T is the loop gain.

From feedback theory, the closed-loop and open-loop gains are related by

$$A_{CL} = \frac{A_{OL}}{1 + T} \tag{15.116}$$

Combining Equation (15.115) and (15.116), we can write the closed-loop output resistance of the voltage regulator in the form

$$R_{of} = R_o\left(\frac{A_{CL}}{A_{OL}}\right) \tag{15.117}$$

From the circuit in Figure 15.51, the closed-loop gain is

$$A_{CL} = \frac{V_O}{V_{REF}} \tag{15.118}$$

The open-loop output resistance is the output resistance of the series-pass transistors, which are operating in an emitter-follower configuration. From previous results, we can write

$$R_o = \frac{r_{\pi 2} + R_{o1}}{(1 + \beta_2)} \tag{15.119}$$

where

$$R_{o1} = \frac{r_{\pi 1} + R_{oa}}{(1 + \beta_1)} \tag{15.120}$$

in which R_{oa} is the output resistance of the error amplifier. If the current in Q_2 is essentially equal to I_O and if β_1 and β_2 are large, then combining Equations (15.119) and (15.120) yields

$$R_o \cong \frac{2V_T}{I_O} + \frac{R_{oa}}{\beta_1\beta_2} \tag{15.121}$$

Since the product $\beta_1\beta_2$ is large, the second term in Equation (15.121) is generally negligible.

The closed-loop output resistance, given by Equation (15.117), is then

$$R_{of} \cong \left(\frac{2V_T}{I_O}\right)\left(\frac{A_{CL}}{A_{OL}}\right) = \left(\frac{2V_T}{I_O}\right)\left(\frac{V_O}{V_{REF}}\right)\left(\frac{1}{A_{OL}}\right) \tag{15.122}$$

Equation (15.122) shows that the output resistance of the voltage regulator is not constant, but varies inversely with load current. Also, for very small values of load current, the output resistance may be unacceptably high.

The basic definition of output resistance is given in Equation (15.112). Using this definition and Equation (15.122), and rearranging terms, we obtain

$$\frac{\Delta V_O}{V_O} = -\left(\frac{\Delta I_O}{I_O}\right)\left(\frac{2V_T}{V_{REF}}\right)\left(\frac{1}{A_{OL}}\right) \tag{15.123}$$

Equation (15.123) relates the fractional change in output voltage to a fractional change in output current. Although valid for only small variations in voltage and current, this equation provides insight into the concept of load regulation.

Example 15.15 **Objective:** Determine the output resistance and the variation in output voltage of a series-pass regulator.

Assume an open-loop gain of $A_{OL} = 1000$, a reference voltage of $V_{REF} = 5\,\text{V}$, a nominal output voltage of $V_O = 10\,\text{V}$, and a nominal output current of $I_O = 100\,\text{mA}$.

Solution: From Equation (15.122), the output resistance is

$$R_{of} = \left(\frac{2V_T}{I_O}\right)\left(\frac{V_O}{V_{REF}}\right)\left(\frac{1}{A_{OL}}\right) = \left[\frac{2(0.026)(10)}{(0.10)(5)(1000)}\right] \Rightarrow 1.04\,\text{m}\Omega$$

From Equation (15.123), the relative change in output voltage is

$$\frac{\Delta V_O}{V_O} = -\left(\frac{\Delta I_O}{I_O}\right)\left(\frac{2V_T}{V_{REF}}\right)\left(\frac{1}{A_{OL}}\right) = -\left(\frac{\Delta I_O}{I_O}\right)\left[\frac{2(0.026)}{(5)(1000)}\right]$$

or

$$\frac{\Delta V_O}{V_O} = -\left(\frac{\Delta I_O}{I_O}\right)(1.04 \times 10^{-5})$$

A 10 percent change in output current results in only a 1.04×10^{-4} percent change in output voltage.

Comment: An output resistance in the mΩ range is typical of voltage regulators, and a change of only 10^{-4} percent in output for a 10 percent change in current is a good load regulation value.

15.6.4 Positive Voltage Regulator

In this section, we will analyze an example of a three-terminal positive voltage regulator fabricated as an IC. The equivalent circuit, shown in Figure 15.52, is part of the LM78LXX series, in which the XX designation indicates the output voltage of the regulator. For example, an LM78L08 is an 8 V regulator.

Basic Circuit Description

Once the bias current is established, Zener diode D_2 provides the basic reference voltage. Transistors Q_{15} and Q_{16} and diode D_1 form a start-up circuit that applies the initial bias to the reference voltage circuit. As the voltage across D_2 reaches the Zener voltage, transistor Q_{15} turns off, since the B–E voltage goes to zero (D_1 and D_2 are identical) and, the start-up circuit is then effectively disconnected from the reference voltage circuit.

The reference portion of the circuit is composed of Zener diode D_2 and transistors Q_3, Q_2, and Q_1, which are used for temperature compensation. The temperature compensation aspects of the circuit are discussed later in this section. Zener diode D_2 is biased by the current-source transistor Q_4. The temperature-compensated portion of the reference voltage at the node between R_1 and R_2 is applied to the base of Q_7, which is part of the error amplifier.

The bias current in Q_4 is established by the current in Q_5, which is a multiple-collector, multiple-emitter transistor. Transistor Q_5 is biased by the current in Q_3, which is controlled by the Zener voltage across D_2 and the B–E junction voltages of Q_3, Q_2, and Q_1. Consequently, the bias currents in the reference portion of the circuit become almost independent of the input supply

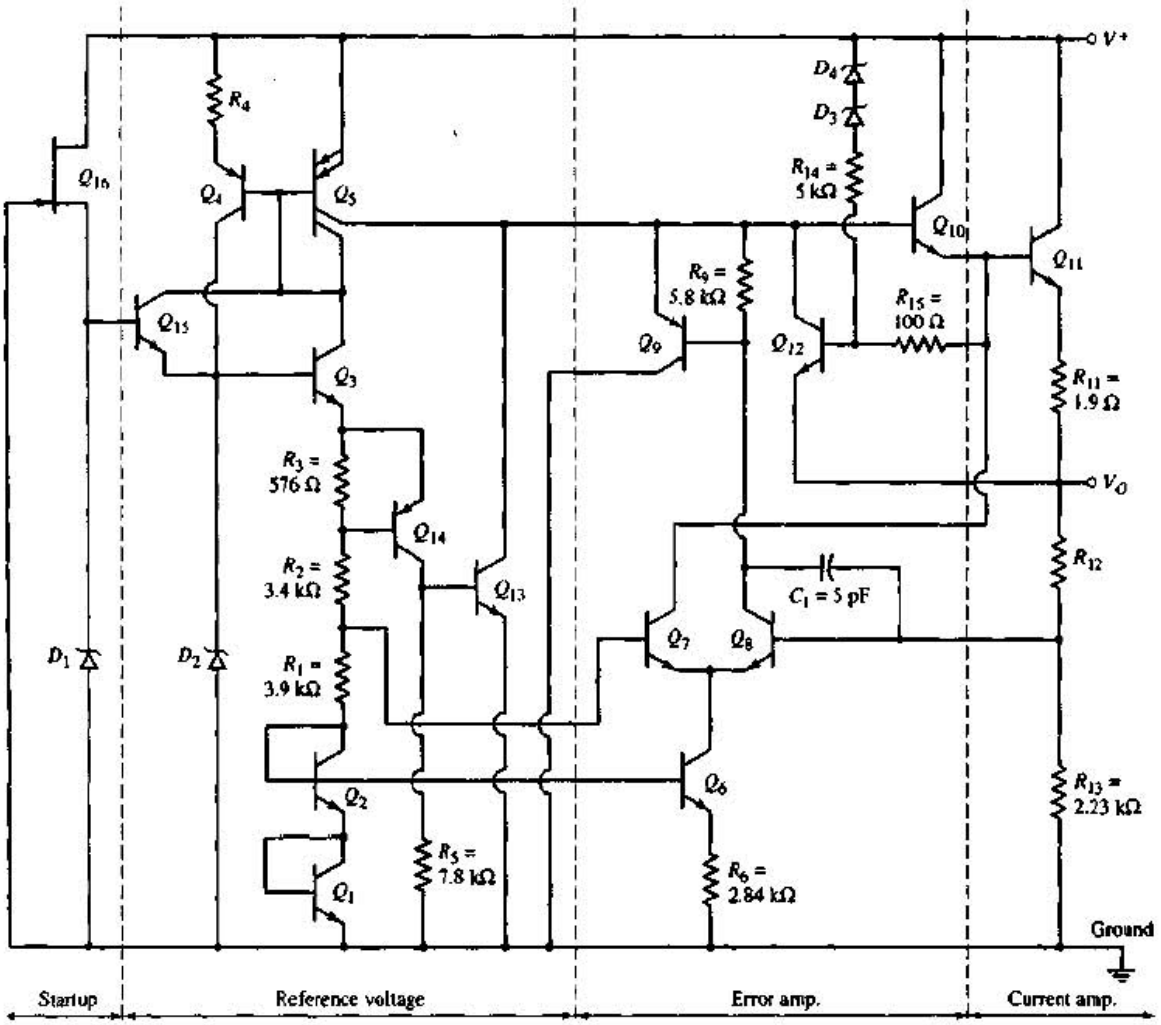


Figure 15.52 Equivalent circuit, LM78LXX series three-terminal positive voltage regulator

voltage. This in turn means that the reference voltage, and thus the output voltage are essentially independent of the power supply voltage. The overall result is very good line regulation.

The error amplifier is the differential pair Q_7 and Q_8, biased by Q_6 and R_6. The error amplifier output is the input to the base of Q_9, which is connected as an emitter follower and forms part of the drive for the series-pass transistors. The series-pass output transistors Q_{10} and Q_{11} are connected in a Darlington emitter-follower configuration.

A fraction of the output voltage, determined by the voltage divider R_{12} and R_{13}, is fed back to the base of Q_8, which is the error-amplifier inverting terminal. If the output voltage is slightly *below* its nominal value, then the base voltage at Q_8 is smaller than that at Q_7, and the current in Q_7 becomes a larger fraction of the total diff-amp bias current. The increased current in Q_7 induces a larger current in Q_{10}, which in turn produces a larger current in Q_{11} and increases the output voltage to the proper value. The opposite process occurs if the output voltage is *above* its nominal value.

Example 15.16 **Objective:** Determine the bias current, temperature-compensated reference voltage, and required resistor R_{12} in a particular LM78LXX voltage regulator.

Consider the voltage regulator circuit in Figure 15.52. Assume Zener diode voltages of $V_Z = 6.3\,\text{V}$ and transistor parameters of $V_{BE}(\text{npn}) = V_{EB}(\text{pnp}) = 0.6\,\text{V}$. Design R_{12} such that $V_O = 8\,\text{V}$.

Solution: The bias current, neglecting base currents, is found as

$$I_{C3} = I_{C5} = \frac{V_Z - 3V_{BE}(\text{npn})}{R_3 + R_2 + R_1} = \frac{6.3 - 3(0.6)}{0.576 + 3.4 + 3.9} = 0.571\,\text{mA}$$

The temperature-compensated portion of the reference voltage, which is the input to the base of Q_7, is

$$V_{B7} = I_{C3}R_1 + 2V_{BE}(\text{npn}) = (0.571)(3.9) + 2(0.6) = 3.43\,\text{V}$$

From the voltage divider network, we have

$$\left(\frac{R_{13}}{R_{12} + R_{13}}\right)V_O = V_{B8} = V_{B7}$$

or

$$\left(\frac{2.23}{R_{12} + 2.23}\right)(8) = 3.43$$

which yields

$$R_{12} = 2.97\,\text{k}\Omega$$

Comment: The voltage divider of R_{12} and R_{13} is internal to the IC. This means the output voltage of a voltage regulator is fixed.

Temperature Compensation

Zener diodes with breakdown voltages greater than approximately 5 V have positive temperature coefficients, and forward-biased pn junctions have negative temperature coefficients. The magnitude of the temperature coefficients in the two devices is nearly the same.

For a given increase in temperature, V_{Z2} increases by ΔV and each B–E voltage decreases by ΔV, which means that I_{C3} in Figure 15.52 increases by approximately

$$\Delta I_{C3} \cong \frac{4\Delta V}{R_1 + R_2 + R_3} \tag{15.124}$$

The total voltage across the B–E junctions of Q_1 and Q_2 decreases by approximately $2\Delta\text{V}$, and the change in voltage at the base of Q_7 is

$$\Delta V_{B7} \cong \Delta I_{C3}R_1 - 2\Delta V = 4\Delta V\left(\frac{R_1}{R_1 + R_2 + R_3}\right) - 2\Delta V \approx 0 \tag{15.125}$$

This indicates that the voltage divider across R_1 effectively cancels any temperature variation. The input signal to the error amplifier is thus temperature compensated.

Protection Devices

Transistors Q_{13} and Q_{14} and resistor R_3 in the regulator in Figure 15.52 provide thermal protection. From the results of Example 15.16, the B–E voltage of Q_{14} is approximately 330 mV, which means that both Q_{14} and Q_{13} are effectively cut off. As the temperature increases, the combination of a negative B–E temperature coefficient and an increase in I_{C3} causes Q_{14} to begin conducting, which in turn causes Q_{13} to conduct. The current in Q_{13} shunts current away from the output series-pass transistors and produces thermal shutdown.

Output current limiting is provided by transistor Q_{12} and resistor R_{11}, as we saw previously in op-amp output stages. The combination of resistors R_{14} and R_{15} and diodes D_3 and D_4 produces what is called a **foldback characteristic**. The vast majority of the power dissipated in the regulator is usually due to the output current, or

$$P_D \cong (V^+ - V_O)I_O \tag{15.126}$$

The output current limit, to prevent power dissipation from reaching its maximum value $P_D(\max)$, is given by

$$I_O(\max) = \frac{P_D(\max)}{V^+ - V_O} \tag{15.127}$$

A current-limiting characteristic of the type described by Equation (15.127) will protect the regulator and allow the maximum output current possible. This type of current limiting is called foldback current limiting.

Three-Terminal Regulator

The three-terminal voltage regulator is designed with an output voltage set at a predetermined value; external feedback elements and connections are not required. Figure 15.53 shows the basic circuit configuration of a three-terminal regulator. In some applications, capacitors may be inserted across the input and output terminals. The lead inductance between the voltage supply and regulator may cause stability problems. The capacitor across the input terminals is used only if the power supply and regulator are separated by a few centimeters. The load capacitor may improve the response of the regulator to transient changes in load current.

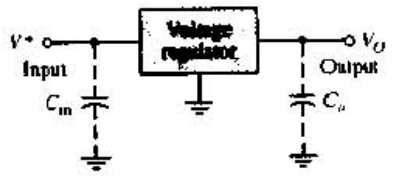


Figure 15.53 Basic circuit configuration of a three-terminal voltage regulator

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Test Your Understanding

15.23 The reference voltage for a constant-voltage source is established by the simple combination of V^+, R_1, and D_1, as shown in the regulator circuit in Figure

15.54. If the Zener diode resistance is $R_Z = 10\,\Omega$ and the zero-current diode voltage is $V_{Zo} = 5.6\,V$, determine the line regulation of the voltage regulator. Assume an ideal op-amp. (Ans. 0.454%)

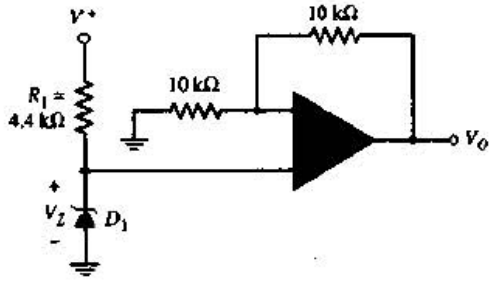


Figure 15.54 Figure for Exercise 15.23

***15.24** Consider the voltage regulator in Figure 15.55. The Zener diode is ideal, with $V_Z = 6.3\,V$, and the op-amp has a finite open-loop gain of $A_{OL} = 1000$. The no-load current is $I_O = 1\,mA$, and the full-load current is $I_O = 100\,mA$. Determine the load regulation. (Ans. 0.786%)

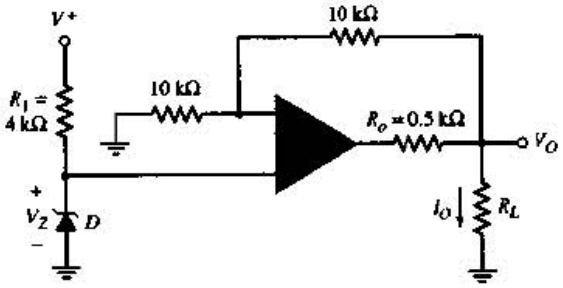


Figure 15.55 Figure for Exercise 15.24

15.25 Consider the voltage regulator circuit shown in Figure 15.52 with Zener diode voltages of $V_Z = 5.6\,V$. Assume transistor parameters of $V_{BE}(npn) = V_{EB}(pnp) = 0.6\,V$, neglect base currents, and let the resistor in the emitter of Q_4 be $R_4 = 100\,\Omega$. (a) Determine the bias currents I_{C3} and I_{C4}, and the temperature-compensated portion of the reference voltage V_{B7}. (b) Determine R_{12} such that $V_O = 5\,V$. (Ans. (a) $I_{C3} = 0.482\,mA$, $I_{C4} = 0.213\,mA$, $V_{B7} = 3.08\,V$ (b) $R_{12} = 1.39\,k\Omega$)

15.7 SUMMARY

- This chapter has presented several applications of op-amps and comparators that may be fabricated as integrated circuits.
- An active filter uses an active device, such as an op-amp, so as to minimize the effect of loading on the frequency characteristics of the filter.
- A Butterworth filter has a maximally flat response in the passband. The maximally flat response is obtained by setting the derivative of the transfer function with respect

to frequency equal to zero in the center of the passband. This procedure establishes the relationships between the various resistor and capacitor values.

- A switched-capacitor filter offers the advantage of an all-IC configuration, since this uses small capacitance values in conjunction with MOS switching transistors that simulate large resistance values.
- The basic principles of oscillation are: (1) the net phase through the amplifier and feedback network must be zero and (2) the magnitude of the loop gain must be unity. For an oscillator to function, the loop gain of a feedback network must provide sufficient phase shift to produce positive feedback.
- A phase shift oscillator consists of three *RC* networks, each providing a phase shift of 60 degrees, and an inverting op-amp, providing a phase shift of 180 degrees, for a total phase shift of 360 degrees.
- A Wien-bridge oscillator uses two *RC* networks as positive feedback in an op-amp circuit.
- The Colpitts, Harley, and crystal oscillator circuits use discrete transistors rather than op-amps, but have the potential of being very high frequency oscillators.
- A comparator is essentially an op-amp operated in an open-loop configuration. The output signal is either a high or low saturated voltage.
- A Schmitt trigger uses a comparator with positive feedback, which produces a hysteresis in the voltage transfer characteristics. This circuit, with its hysteresis characteristic, can eliminate the chatter effect in an output signal during switching applications in which noise is superimposed on the input signal.
- A square-wave generator or oscillator can be produced by incorporating an *RC* network in the negative feedback loop of a Schmitt trigger. This type of oscillator is called an astable multivibrator.
- The 555 IC timer uses two comparators and can operate in either astable or monostable modes. The frequency and duty cycle of the astable output signal, and the output pulse width of the monostable output signal, can be adjusted over a wide range by varying external resistor and capacitor values.
- Three examples of IC power amplifiers were discussed. The LM380 power amplifier is an all-IC device capable of delivering 5 W of ac power to a load. The PA12 power amplifier consists of a high-gain amplifier in conjunction with an external class-AB output stage and is capable of supplying peak output currents in the range of ± 15 A. The bridge power amplifier uses two op-amps connected to an external load.
- A simple series-pass voltage regulator was analyzed to determine the basic characteristics of a regulator. The line regulation and load regulation were defined for regulators. Finally, an all-IC LM78L08 voltage regulator was discussed.

CHECKPOINT

After studying this chapter, the reader should have the ability to:

✔ Design a basic active filter. (Section 15.1)

✔ Design a basic oscillator. (Section 15.2)

✔ Design a basic Schmitt trigger circuit. (Section 15.3)

✔ Design a Schmitt trigger square-wave oscillator and use a 555 timer circuit. (Section 15.4)

✔ Understand the operation and characteristics of examples of integrated circuit power amplifiers. (Section 15.5)

REVIEW QUESTIONS

1. Describe the difference between an active filter and a passive filter. What is the primary advantage of an active filter?
2. Sketch the general characteristics of a low-pass filter, a high-pass filter, and a band-pass filter.
3. Consider a low-pass filter. What is the slope of the roll-off with frequency for a (a) one-pole filter, (b) two-pole filter, (c) three-pole filter, and (d) four-pole filter?
4. What characteristic defines a Butterworth filter?
5. Describe how a capacitor in conjunction with two switching transistors can behave as a resistor.
6. Sketch a one-pole low-pass switched-capacitor filter circuit.
7. Describe the characterisics of an oscillator.
8. Describe and explain the operation of a phase-shift oscillator.
9. Describe and explain the operation of a Wien-bridge oscillator.
10. What is the advantage of a Colpitts oscillator or Hartley oscillator compared to a phase-shift oscillator.
11. Sketch the circuits and characteristics of inverting and noninverting comparators.
12. Sketch the circuit and characteristics of a basic inverting Schmitt trigger.
13. What is meant by a bistable circuit?
14. What is the primary advantage of a Schmitt trigger circuit.
15. Sketch the circuit and explain the operation of a Schmitt trigger oscillator.
16. Describe the characteristics of a monostable multivibrator.
17. Describe how an op-amp in conjunction with a class-AB output stage can be used as a power amplifier.
18. Sketch a bridge power amplifier and describe its operation.
19. Sketch the basic circuit block diagram of a voltage regulator and explain the principle of operation.
20. Define load regulation of a voltage regulator.
21. Sketch the basic circuit of a series-pass voltage regulator.

PROBLEMS

Section 15.1 Active Filters

D15.1 (a) Design a single-pole low-pass filter with a gain of 10 in the passband and a 3 dB frequency of 5 kHz. (b) Repeat part (a) for a gain of -15 in the passband and a 3 dB frequency of 10 kHz. The minimum input resistance in the passband for this filter is to be 10 kΩ.

15.2 Determine the reduction in gain at $f = 2f_{3dB}$ for a (a) one-pole, (b) two-pole, and (c) three-pole low-pass filter.

D15.3 Design a two-pole high-pass Butterworth active filter with a cutoff frequency of 10 kHz and a unity-gain magnitude at high frequency.

D15.4 Design a three-pole high-pass Butterworth active filter with a cutoff frequency of 50 kHz. What is the magnitude of the transfer function at frequencies of 30, 35, 40, and 45 kHz?

15.5 Starting with the general transfer function given by Equation (15.7), derive the relationship between R_1 and R_2 in the two-pole high-pass Butterworth active filter.

15.6 A low-pass filter is to have a cutoff frequency of 10 kHz and is to have a gain at 20 kHz, which is reduced by at least 25 dB from its maximum value. Find the minimum number of poles required for a Butterworth filter.

***D15.7** Design a special type of first-order filter (one capacitor) in which the gain magnitude is 25 for frequencies less than approximately 25 kHz and is 1 for frequencies greater than approximately 25 kHz.

***D15.8** An amplitude-modulated radio signal consists of an 80 Hz to 12 kHz audio signal superimposed on a 770 kHz carrier signal. A low-pass filter is to be designed in which the gain in the passband is unity and the carrier signal is attenuated by at least −100 dB. What order of filter is required?

D15.9 A band-reject filter may be designed by combining a low-pass filter and a high-pass filter with a summing amplifier. A 60 Hz signal is to be at least −50 dB below the maximum gain value of 0 dB with a two-pole low-pass Butterworth filter and a two-pole high-pass Butterworth filter. What is the bandwidth of the reject filter?

15.10 Consider the bandpass filter in Figure P15.10. (a) Show that the voltage transfer function is

$$A_v(s) = \frac{v_O}{v_I} = \frac{-1/R_4}{(1/R_1) + sC + 1/(sCR_2R_3)}$$

(b) For $C = 0.1\ \mu F$, $R_1 = 85\ k\Omega$, $R_2 = R_3 = 300\ \Omega$, $R_4 = 3\ k\Omega$, and $R_5 = 30\ k\Omega$, determine: (i) $|A_v(\max)|$; (ii) the frequency f_o at which $|A_v(\max)|$ occurs; and (iii) the two 3 dB frequencies.

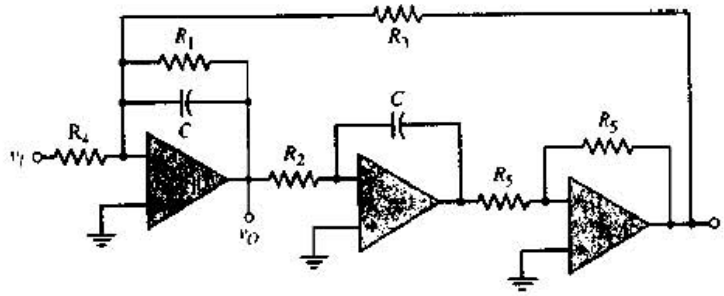


Figure P15.10

15.11 Consider the circuit in Figure P15.11. (a) Derive the expressions for the magnitude and phase of the voltage transfer function. (b) Plot the phase versus frequency for $R = 10\ k\Omega$ and $C = 15.9\ nF$. [Note: this filter is referred to as an all-pass filter in that the magnitude of the voltage gain is constant, but the phase of the output voltage changes with frequency.]

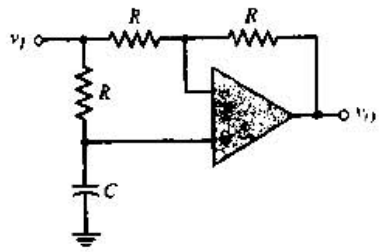


Figure P15.11

15.12 For each of the circuits in Figures P15.12, derive the expressions for the voltage transfer function $T(s) = V_o(s)/V_i(s)$ and the cutoff frequency f_{3dB}.

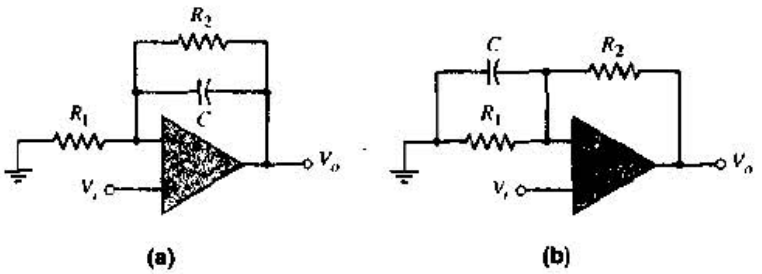


Figure P15.12

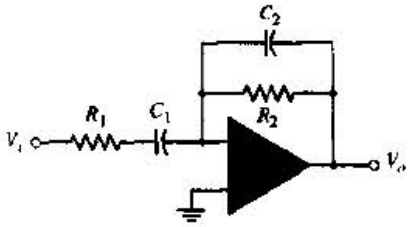


Figure P15.13

15.13 The circuit in Figure P15.13 is a bandpass filter. (a) Derive the expression for the voltage transfer function $T(s)$. (b) If $R_1 = 10\,\text{k}\Omega$, determine R_2, C_1, and C_2 such that the magnitude of the midband gain is 50 and the cutoff frequencies are 200 Hz and 5 kHz.

D15.14 A simple bandpass filter can be designed by cascading one-pole high-pass and one-pole low-pass filters. Using op-amp circuits similar to those in Figure 15.3, design a bandpass filter with cutoff frequencies of 200 Hz and 50 kHz and with a midband gain of 10 dB. Resistor values must be no larger than 200 kΩ, but the input resistance must be as large as possible.

15.15 The clock frequency in the switched-capacitor circuit in Figure 15.13(a) is 100 kHz. Find the equivalent resistance when: (a) $C = 1\,\text{pF}$, (b) $C = 10\,\text{pF}$, and (c) $C = 30\,\text{pF}$.

15.16 In the switched-capacitor circuit in Figure 15.13(a), the voltages are $V_1 = 2\,\text{V}$ and $V_2 = 1\,\text{V}$, the capacitor value is $C = 10\,\text{pF}$, and the clock frequency is $f_C = 100\,\text{kHz}$. (a) Determine the charge transferred from V_1 to V_2 during each clock pulse. (b) What is the average current that source V_1 supplies? (c) If the "on" resistance of each MOSFET is 1000 Ω, determine the time required to transfer 99 percent of the charge during each half-clock period.

D15.17 Consider the switched-capacitor filter in Figure 15.14(b). Design the circuit for a low-frequency gain of −10 and a cutoff frequency of 10 kHz. The clock frequency must be 10 times the cutoff frequency and the largest capacitance is to be 30 pF. Find the required values of C_1, C_2, and C_F.

15.18 The circuit in Figure P15.18 is a switched-capacitor integrator. Let $C_F = 30\,\text{pF}$ and $C_1 = 5\,\text{pF}$, and assume the clock frequency is 100 kHz. Also, let $v_I = 1\,\text{V}$. (a) Determine the integrating RC time constant. (b) Find the change in output voltage during each clock period. (c) If C_F is initially uncharged, how many clock pulses are required for v_O to change by 13 V?

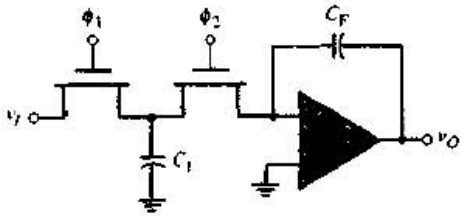


Figure P15.18

Section 15.2 Oscillators

15.19 Consider the phase-shift oscillator in Figure 15.16 with parameters $R = 4\,\text{k}\Omega$ and $C = 10\,\text{nF}$. Determine the frequency of oscillation and the required value of R_2.

15.20 In the phase-shift oscillator in Figure 15.16, the capacitor at the noninverting terminal of op-amp A_1 is replaced by a variable capacitor C_V. (a) Derive the expression for the frequency of oscillation. (b) If $C = 10\,\text{pF}$, $R = 10\,\text{k}\Omega$, and C_V is variable between 10 and 50 pF, determine the range of oscillation frequency.

D15.21 Design the phase-shift oscillator in Figure 15.17 to operate at $f_o = 80\,\text{kHz}$. Let $C = 100\,\text{pF}$.

15.22 Analyze the phase-shift oscillator in Figure 15.17. Show that the frequency of oscillation is given by Equation (15.46) and that the condition for oscillation is given by Equation (15.47).

15.23 The circuit in Figure P15.23 is an alternative configuration of a phase-shift oscillator. (a) Assume that $R_1 = R_2 = R_3 = R_{A_1} = R_{A_2} = R_{A_3} \equiv R$ and $C_1 = C_2 = C_3 \equiv C$. Show that the frequency of oscillation is $\omega_o = \sqrt{3}/RC$. (b) Assume equal magnitudes of gain in each amplifier stage. What is the minimum magnitude of gain required in each stage to sustain oscillation?

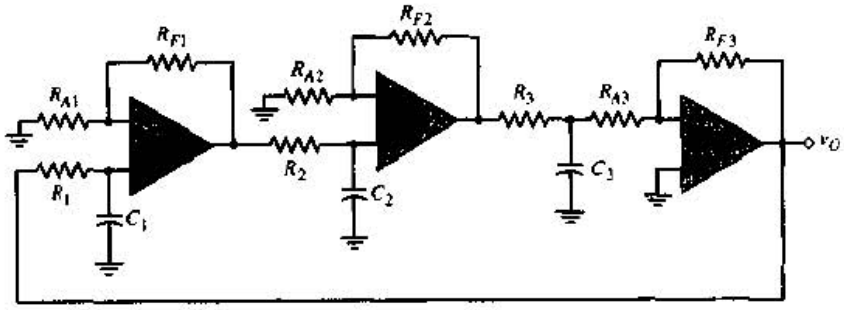


Figure P15.23

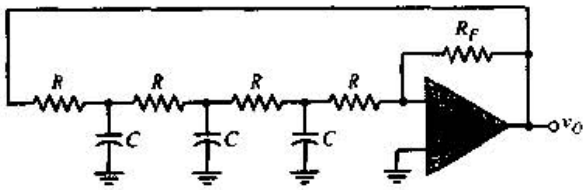


Figure P15.24

15.24 Consider the phase-shift oscillator in Figure P15.24. (a) Derive the expression for the frequency of oscillation. (b) If $R = 5\,\text{k}\Omega$, find the values of C and R_F that will produce sustained oscillations at 5 kHz.

15.25 A Wien-bridge oscillator is shown in Figure P15.25. (a) Derive the expression for the frequency of oscillation. (b) What is the condition for sustained oscillations?

15.26 Consider the oscillator circuit in Figure P15.26. (a) Derive the expression for the loop gain $T(s)$. (b) Determine the expression for the frequency of oscillation. (c) Find the condition for oscillation.

Figure P15.25

Figure P15.26

D15.27 Design the Wien-bridge oscillator in Figure 15.18 to oscillate at $f_o = 80\,\text{kHz}$. Choose appropriate component values.

D15.28 The Colpitts oscillator in Figure 15.20 is biased at $I_D = 1\,\text{mA}$. The transistor parameters are $V_{TN} = 1\,\text{V}$ and $K_n = 0.5\,\text{mA/V}^2$. Let $C_1 = 0.01\,\mu\text{F}$ and $R_L = 4\,\text{k}\Omega$. Design the circuit to oscillate at $f_o = 400\,\text{kHz}$.

15.29 Figure P15.29 shows a Colpitts oscillator with a BJT. Assume r_π and r_o are both very large. Derive the expressions for the frequency of oscillation and the condition of oscillation.

15.30 Consider the ac equivalent circuit of the Hartley oscillator in Figure 15.22. (a) Derive the expression for the frequency of oscillation. (b) Determine the condition for sustained oscillations.

D15.31 For the Hartley oscillator in Figure 15.22, assume $r_\pi \to \infty$ and let $g_m = 20\,\text{mA/V}$. Design the circuit to oscillate at $f_o = 800\,\text{kHz}$ and verify that the circuit will sustain oscillations.

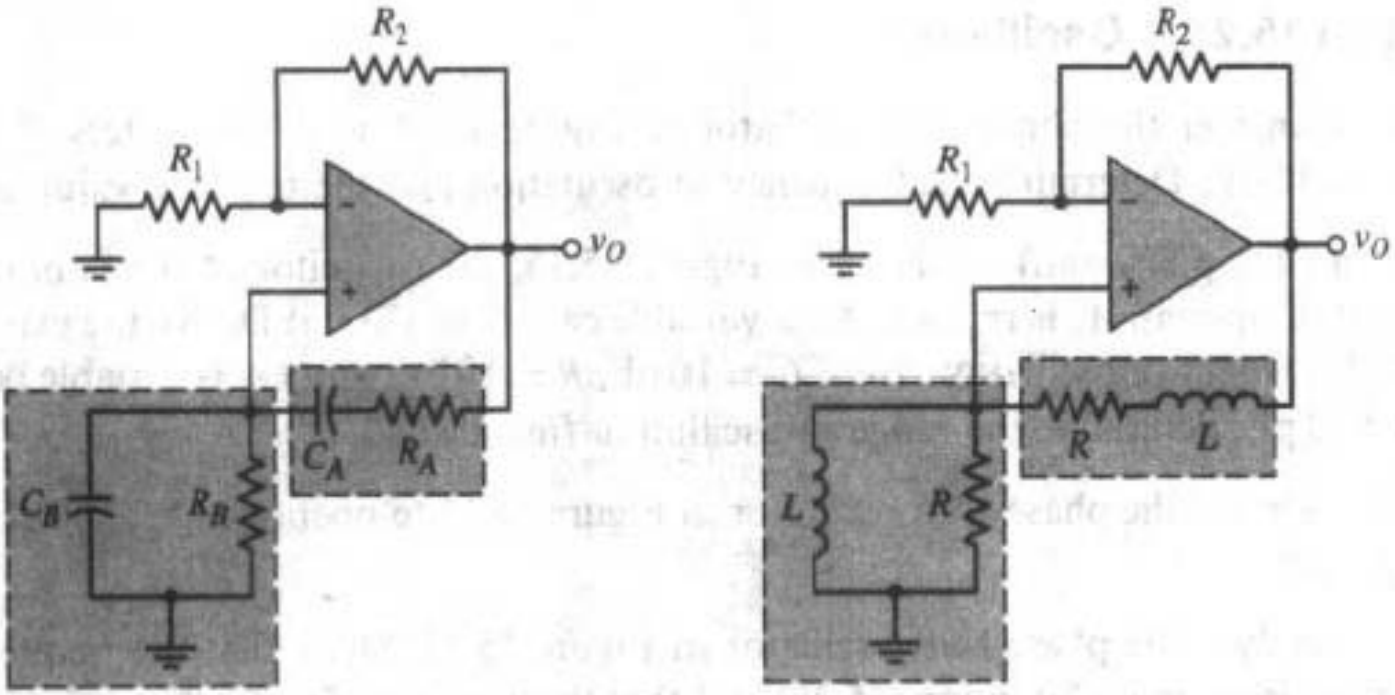
15.32 Find the loop gain functions $T(s)$ and $T(j\omega)$, the frequency of oscillation, and the R_2/R_1 required for oscillation for the circuit in Figure P15.32.

15.33 Repeat Problem 15.32 for the circuit in Figure P15.33.

Figure P15.29

Figure P15.32

Figure P15.33


R_2
R_1
v_O
C_A
R_A
C_B
R_B
R_2
R_1
v_O
R
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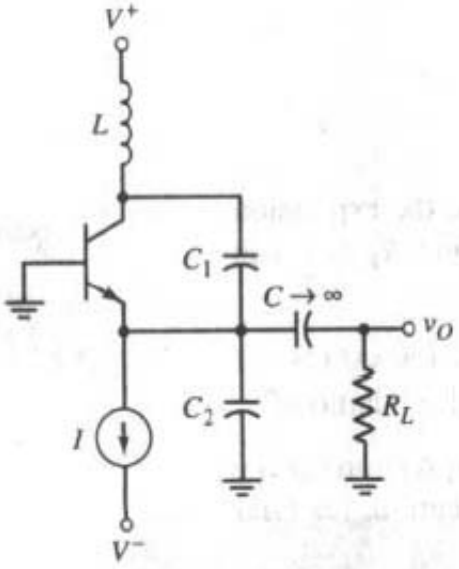
L
R


V+
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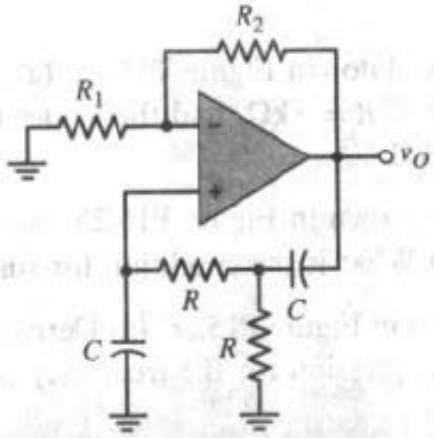
C → ∞
vO
C2
RL
I
V−


R2
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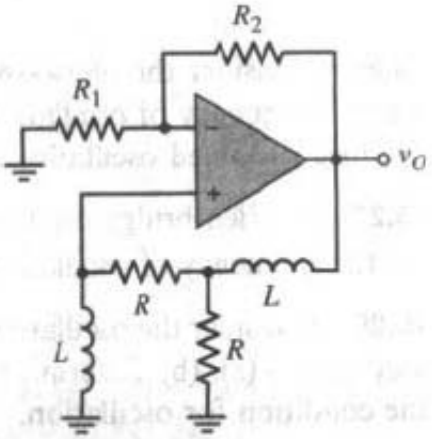
vO
R
C
C
R


R2
R1
vO
R
L
L
R

Section 15.3 Schmitt Trigger Circuits

D15.34 For the comparator in the circuit in Figure 15.27(a), the output saturation voltages are $\pm 10\,\text{V}$. Let $R_1 = 50\,\text{k}\Omega$. Design R_2 as a potentiometer in series with a fixed resistor, and find a reference voltage such that the crossover voltage can easily be varied over the range of 1 to 5 V.

D15.35 Consider the Schmitt trigger in Figure 15.30(a). Assume the saturated output voltages are $V_H = +10\,\text{V}$ and $V_L = -10\,\text{V}$. Neglecting input bias current effects, design the circuit such that the maximum current in R_1 and R_2 is $100\,\mu\text{A}$ and the hysteresis width is 0.1 V.

15.36 A Schmitt trigger is shown in Figure 15.30(a). The parametes are: $V_H = +10\,\text{V}$, $V_L = -10\,\text{V}$, $R_1 = 10\,\text{k}\Omega$, and $R_2 = 40\,\text{k}\Omega$. (a) Determine the crossover voltages V_{TH} and V_{TL}. (b) Assume a sinusoidal voltage $v_I = 5\sin[2\pi(60)t]\,\text{V}$ is applied at the input. Sketch the steady-state output voltage versus time over two periods of the waveform.

15.37 Consider the Schmitt trigger in Figure P15.37. Assume the saturated output voltages are $\pm V_P$. (a) Derive the expression for the crossover voltages V_{TH} and V_{TL}. (b) Let $R_A = 10\,\text{k}\Omega$, $R_B = 20\,\text{k}\Omega$, $R_1 = 5\,\text{k}\Omega$, $R_2 = 20\,\text{k}\Omega$, $V_P = 10\,\text{V}$, and $V_{\text{REF}} = 2\,\text{V}$. (a) Find V_{TH} and V_{TL}. (b) Sketch the voltage transfer characteristics.

15.38 The saturated output voltages are $\pm V_P$ for the Schmitt trigger in Figure P15.38. (a) Derive the expressions for the crossover voltages V_{TH} and V_{TL} (b) If $V_P = 12\,\text{V}$, $V_{\text{REF}} = -10\,\text{V}$, and $R_3 = 10\,\text{k}\Omega$, find R_1 and R_2 such that the switching point is $V_S = -5\,\text{V}$ and the hysteresis width is 0.2 V. (c) Sketch the voltage transfer characteristics.

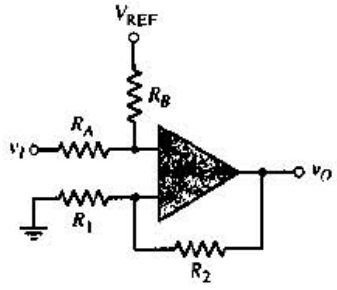


Figure P15.37

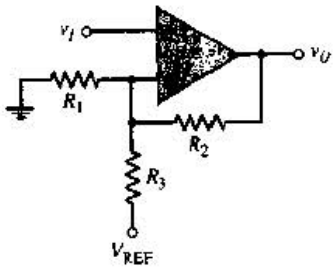


Figure P15.38

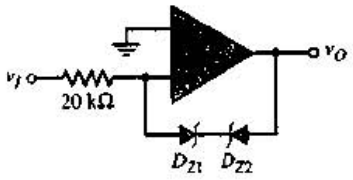


Figure P15.39

15.39 (a) Plot the voltage transfer characteristics of the comparator circuit in Figure P15.39 assuming the open-loop gain is infinite. Let the reverse Zener voltage be $V_Z = 5.6\,\text{V}$ and the forward diode voltage be $V_\gamma = 0.6\,\text{V}$. (b) Repeat part (a) for an open-loop gain of 10^3. (c) Repeat part (a) for 2.5 V applied to the inverting terminal of the comparator.

15.40 Consider the Schmitt trigger in Figure 15.32(a). (a) Derive the expressions for the switching point and crossover voltages, as given in Equations (15.76) and (15.77). (b) Let $V_H = +10\,\text{V}$, $V_L = -10\,\text{V}$, and $R_1 = 10\,\text{k}\Omega$. Determine R_2 and V_{REF} such that $V_{TH} = 2\,\text{V}$ and $V_{TL} = 1\,\text{V}$.

15.41 Consider the Schmitt trigger in Figure 15.33(a). (a) Derive the expressions for the switching point and crossover voltages, as given in Equations (15.78) and (15.79). (b) Let $V_H = 12\,\text{V}$, $V_L = -12\,\text{V}$, and $R_2 = 20\,\text{k}\Omega$. Determine R_1 and V_{REF} such that $V_{TH} = -1\,\text{V}$ and $V_{TL} = -2\,\text{V}$.

15.42 For the comparator in the circuit in Figure 15.35, the nominal output saturation voltages are ±12 V. Assume forward diode voltage drops of 0.7 V and reverse Zener voltages of 5.6 V. (a) If $R_1 = 1\,\text{k}\Omega$, find R_2 such that the hysteresis width is 1 V. (b) Find R such that the average diode current is 1 mA.

15.43 Consider the Schmitt trigger with limiter, as shown in Figure 15.36. Assume the forward diode turn-on voltage V_γ is 0.7 V. (a) Determine V_{REF} such that the bistable output voltages at $v_I = 0$ are ±5 V. (b) Find values of R_1 and R_2 such that the crossover voltages are ±0.5 V. (c) Taking R_1, R_2, and the 100 kΩ resistors into account, find v_O when $v_I = 10\,\text{V}$.

15.44 Consider the inverting Schmitt trigger with limiting network, as shown in Figure 15.36(a). Show that the crossover voltages are those given in Figure 15.36(b).

15.45 (a) For the Schmitt trigger with limiter in Figure 15.37(a), find the two output voltage values at $v_I = 0$ and the two crossover voltages. (b) Derive the expression for the slope of v_O versus v_I for $v_I > V_{TH}$.

Section 15.4 Nonsinusoidal Oscillators and Timing Circuits

D15.46 Using the Schmitt trigger circuit in Figure 15.38, design a square-wave oscillator with a frequency of $f_o = 5\,\text{kHz}$ and a 50 percent duty cycle. Choose reasonable component values.

15.47 For the Schmitt trigger oscillator in Figure 15.38, the parameters are: $C_x = 0.1\,\mu\text{F}$, $R_x = 10\,\text{k}\Omega$, $R_2 = 10\,\text{k}\Omega$, and $R_1 = 30\,\text{k}\Omega$. The saturated output voltages are ±10 V. (a) Plot v_o and v_x versus time over two periods of oscillation. (b) Find the frequency of oscillation and the duty cycle.

15.48 Repeat Problem 15.47 for saturated output voltages of $V_H = +15\,\text{V}$ and $V_L = -10\,\text{V}$.

15.49 Consider the circuit in Figure P15.49. The saturated output voltages of the Schmitt trigger comparator are ±10 V. Assume that at $t = 0$, output v_{o1} switches from its low state to its high state and C_γ is uncharged. Plot v_{o1} and v_o versus time over two periods of oscillation.

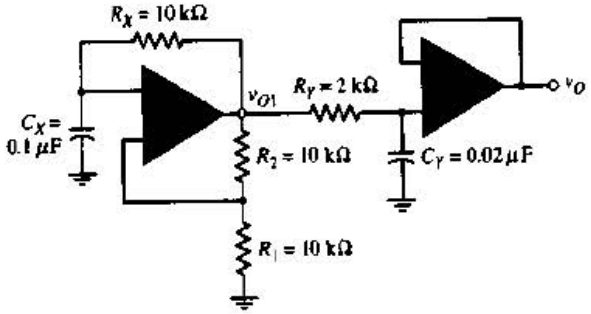


Figure P15.49

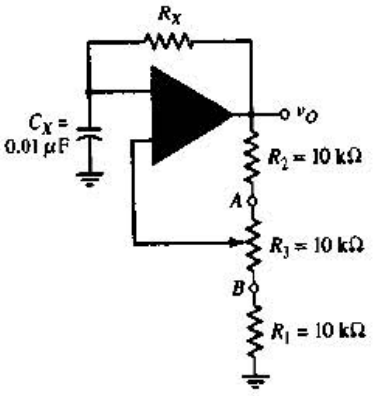


Figure P15.50

15.50 The saturated output voltages of the comparator in Figure P15.50 are ±10 V. (a) Find R_x such that the frequency of oscillation is 500 Hz when the potentiometer is connected to point A. (b) Using the results of part (a), determine the oscillator frequency when the potentiometer is connected to point B.

15.51 The monostable multivibrator in Figure 15.40 is to be designed to produce a 100μs pulse. Assume the saturated output voltages are ±5 V, and let $V_\gamma = 0.7$ V, $R_1 = 10\,\text{k}\Omega$, and $R_2 = 25\,\text{k}\Omega$. What is the minimum input triggering voltage required? What is the recovery time?

15.52 A monostable multivibrator is shown in Figure 15.40. The parameters are: $R_x = 50\,\text{k}\Omega$, $C_x = 01.\,\mu\text{F}$, and $R_1 = R_2 = 20\,\text{k}\Omega$. The saturated output voltages are ±10 V. Let $V_\gamma = 0.7$ V for D_1 and D_2. What is the width of the output pulse? What is the recovery time?

D15.53 Figure 15.43 shows the 555 timer connected in the monostable multivibrator mode. (a) Design the circuit to provide an output pulse 60 seconds wide. (b) Determine the recovery time.

D15.54 Design a 555 monostable multivibrator to provide a 5μs pulse. What is the recovery time?

15.55 A 555 timer is connected in the astable mode as shown in Figure 15.44. The parameters are $R_A = R_B = 20\,\text{k}\Omega$ and $C = 0.1\,\mu\text{F}$. Determine the frequency of oscillation and the duty cycle.

15.56 A 555 ICC is connected as shown in Figure P15.56. Determine the range of oscillation frequency and the duty cycle.

15.57 Repeat Problem 15.56 for the circuit in Figure P15.57.

Section 15.5 Integrated Circuit Power Amplifiers

15.58 The LM380 power amplifier in Figure 15.45 is biased at $V^+ = 22$ V. Let $\beta_n = 100$ and $\beta_p = 20$ for the npn and pnp transistors, respectively. (a) Determine the quiescent collector currents in transistors Q_1 through Q_6. (b) Assume that diodes D_1 and D_2 and transistors Q_7, Q_8, and Q_9 are all matched, with parameters $I_S = 10^{-13}$ A. For zero input voltages, determine the quiescent currents in D_1, D_2, Q_7, Q_8, and Q_9. (c) For no load, calculate the quiescent power dissipated in the amplifier.

15.59 An LM380 must deliver ac power to a 10 Ω load. The maximum power dissipated in the amplifier must be limited to 2 W and the maximum allowed distortion must

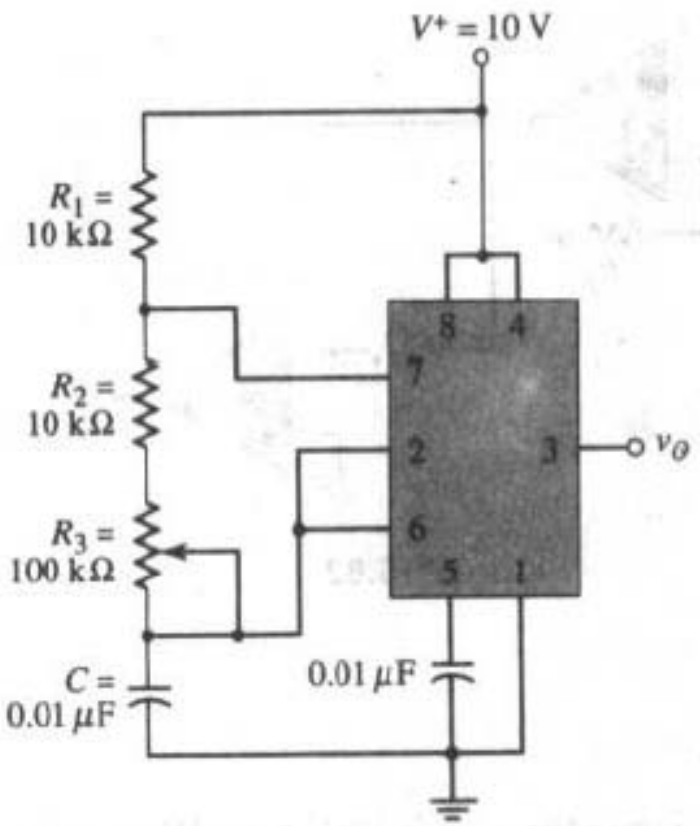


Figure P15.56

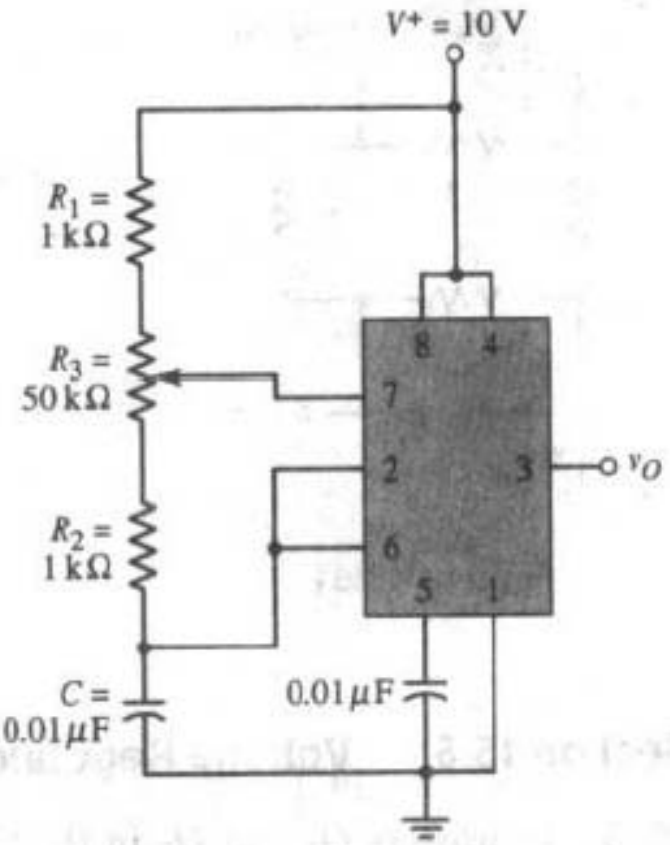


Figure P15.57

be limited to 3 percent. Determine: (a) the maximum power that can be delivered to the load, (b) the maximum supply voltage, and (c) the peak amplitude of the sinusoidal output voltage.

D15.60 Design the bridge circuit in Figure 15.49 such that it can deliver an average ac power of 20 W to a 10 Ω speaker. Design each op-amp to have a gain magnitude of 15. Each supply voltage must be approximately 20 percent larger than the peak amplitude of the output voltage. What is the peak amplitude of the output voltage and current for each op-amp?

D15.61 Another form of the bridge power amplifier is shown in Figure P15.61. This amplifier has a very high input resistance since the input is to the noninverting terminal of an op-amp. (a) Derive the expression for the voltage gain $A_v = v_L/v_I$. (b) Design the circuit to provide a gain of $A_v = 10$ so that the magnitudes of v_{o1} and v_{o2} are equal. Let $R_1 = 50\,\text{k}\Omega$. (c) If $R_L = 20\,\Omega$ and if the average power delivered to the load is 10 W, determine the peak amplitude of v_{o1} and v_{o2} and the peak load current.

D15.62 Figure P15.62 shows an audio power amplifier using two identical op-amps connected in a bridge configuration. (a) Derive the expression for the voltage gain $A_v = v_L/v_I$. (b) Design the circuit to provide a gain of $A_v = 15$ and so that the magnitudes of v_{o1} and v_{o2} are equal. (c) If $R_L = 8\,\Omega$ and if the average power delivered to the load is 50 W, determine the peak amplitudes of v_{o1} and v_{o2} and the peak load current.

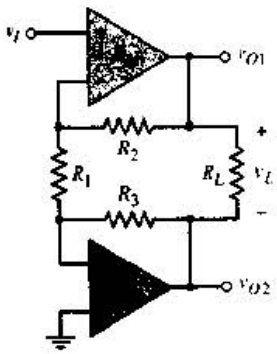


Figure P15.61

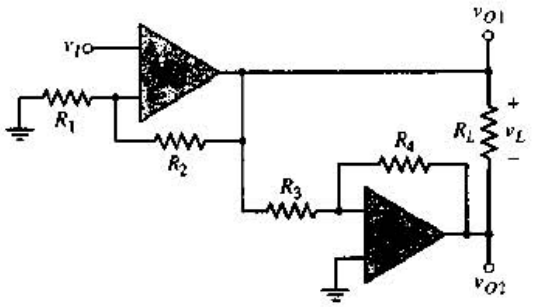


Figure P15.62

Section 15.6 Voltage Regulators

15.63 Transistors Q_1 and Q_2 in the voltage regulator circuit in Figure P15.63 have parameters $\beta = 200$, $V_{EB}(\text{on}) = 0.7\,\text{V}$, and $V_A = 100\,\text{V}$. The zero-current Zener voltage is $V_{ZO} = 6.3\,\text{V}$ and the Zener resistance is $r_z = 15\,\Omega$. Assuming an ideal op-amp, calculate the line regulation.

15.64 The output voltage of a voltage regulator decreases by 10 mV as the load current changes from a no-load current of zero to a full-load current of 1 A. If the output voltage changes linearly with load current, determine the output resistance of the regulator.

15.65 Consider the three-terminal voltage regulator in Figure 15.52, with parameters as given in Example 15.16. If the maximum load current is $I_O(\text{max}) = 100\,\text{mA}$, determine the minimum applied power supply voltage V^+ that will still maintain all transistors biased in the active region.

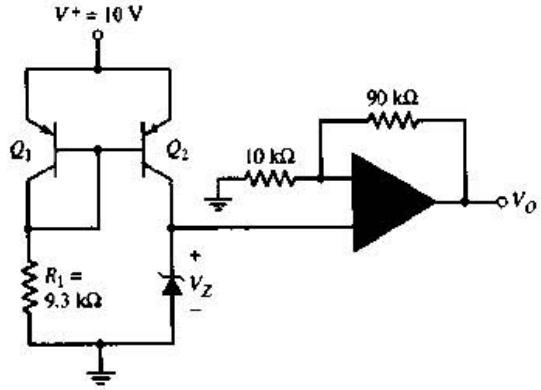


Figure P15.63

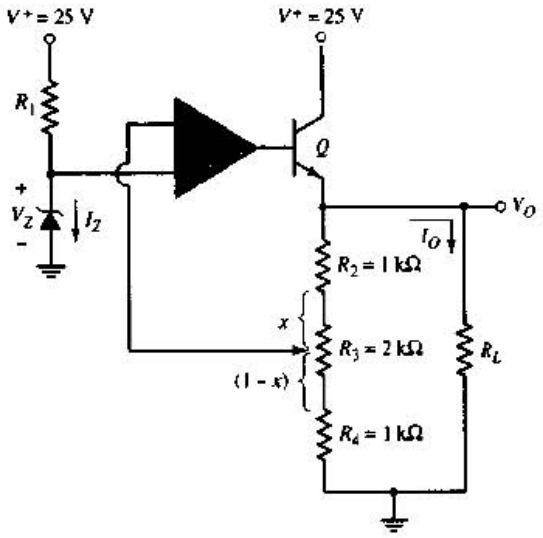


Figure P15.68

D15.66 Consider the three-terminal voltage regulator in Figure 15.52, with Zener diode voltages of $V_Z = 6.3\,\text{V}$. Assume transistor parameters of $V_{BE}(\text{npn}) = V_{EB}(\text{pnp}) = 0.6\,\text{V}$, and neglect base currents. (a) Determine resistance R_4 such that $I_{Z2} = 0.25\,\text{mA}$. (b) Determine R_{12} such that $V_O = 12\,\text{V}$.

15.67 The three-terminal voltage regulator in Figure 15.52 has parameters as described in Example 15.16. Assume $R_4 = 0$, $V_A = 50\,\text{V}$ for Q_4, and $r_z = 15\,\Omega$ for D_2. Determine the line regulation.

15.68 The voltage regulator in Figure P15.68. is a variable voltage, 0-to-1 A power supply. The transistor parameters are $\beta = 100$ and $V_{BE}(\text{on}) = 0.7\,\text{V}$. The op-amp has a finite open-loop gain of $A_{OL} = 10^4$. The zero-current Zener voltage is $V_{ZO} = 5\,\text{V}$ and the Zener resistance is $r_z = 10\,\Omega$. (a) For $I_Z = 10\,\text{mA}$, find R_1. (b) Determine the range of output voltage as the potentiometer R_3 is varied. (c) If the potentiometer is varied such that $x = 0$, determine the load regulation. Assume R_o of the op-amp is zero.

15.69 For the transistor in the circuit in Figure P15.69, the parameters are $\beta = 100$ and $V_{EB}(\text{on}) = 0.6\,\text{V}$. The diode is an idea Zener with $V_Z = 5.6\,\text{V}$, and the op-amp is ideal. Determine the range of load resistance R_L such that the load current is a constant. What is the value of that constant load current?

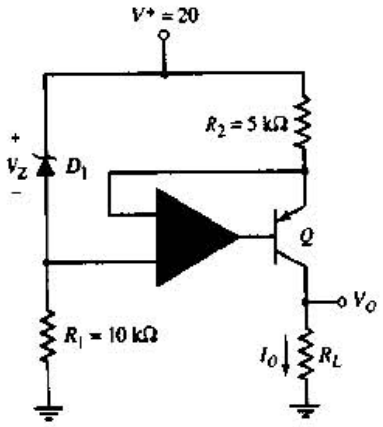


Figure P15.69

COMPUTER SIMULATION PROBLEMS

15.70 Simulate the three-pole low-pass Butterworth filter in Figure 15.10(a) using parameters $R = 1.59\,\text{k}\Omega$, $C_1 = 0.03546\,\mu\text{F}$, $C_2 = 0.01392\,\mu\text{F}$, and $C_3 = 0.002024\,\mu\text{F}$. Plot the magnitude of the voltage transfer function versus frequency and compare the computer results to the results obtained in Exercise 15.1.

15.71 Simulate the switched-capacitor filter in Figure 15.14(b) using parameters $C_1 = 30\,\text{pF}$, $C_2 = 5\,\text{pF}$, and $C_F = 12\,\text{pF}$. Assume a clock frequency of 100 kHz. Plot the magnitude of the voltage transfer function versus frequency. Determine the 3 dB frequency and low-frequency gain. Compare these results with those obtained in Exercise 15.3.

15.72 Simulate the phase-shift oscillator in Figure 15.17 using parameters $R = 10\,\text{k}\Omega$, $C = 100\,\text{pF}$, and $R_2 = 300\,\text{k}\Omega$. Plot the output voltage versus time. What is the frequency of oscillation?

15.73 Simulate the Schmitt trigger with limiters in Figure 15.36(a). Let $V_{REF} = 5\,\text{V}$. Plot v_O versus v_I as v_I increases from -5 to $+5\,\text{V}$, and then as v_I decreases from $+5$ to $-5\,\text{V}$.

15.74 Simulate the ac equivalent circuit of the LM380 power amplifier in Figure 15.46. Determine the small-signal differential voltage gain.

15.75 Consider the reference voltage and error amp sections of the LM78LXX voltage regulator in Figure 15.52. Use the parameters described in Example 15.16. From a PSpice analysis, determine the temperature sensitivity and load regulation.

DESIGN PROBLEMS

[Note: Each design should be correlated with a computer analysis.]

***D15.76** Design a low-pass Butterworth filter to have a cutoff frequency at 15 kHz and a gain at 20 kHz, which is reduced by at least 20 dB from its maximum value. Determine the minimum number of poles and specify all component values.

***D15.77** Consider the Colpitts oscillator in Figure P15.77. The capacitors C_E and C_C are very large bypass and coupling capacitors. Let $V_{CC} = 10\,\text{V}$. (a) Design the circuit such that the quiescent collector current is $I_{CQ} = 1\,\text{mA}$. (b) Design the circuit to oscillate at $f_o = 800\,\text{kHz}$.

***D15.78** Design a Schmitt trigger oscillator to produce a square-wave output at a frequency of $f_o = 5\,\text{kHz}$ with peak output voltages of $\pm 5\,\text{V}$.

***D15.79** Design a 555 timer as an astable multivibrator with an output signal frequency of 800 Hz and a 60 percent duty cycle.

***D15.80** Consider the power amplifier in Figure P15.80 with parameters $V^+ = 15\,\text{V}$, $V^- = -15\,\text{V}$, and $R_L = 20\,\Omega$. The closed-loop gain must be 10. Design the circuit such that the power delivered to the load is 5 W when $v_I = -1\,\text{V}$. If the four transistors are matched, determine the minimum β required such that the op-amp output current is limited to 2 mA when 5 W is delivered to the load.

***D15.81** Consider the simple series-pass regulator circuit in Figure P15.81. Assume an ideal Zener diode with $V_Z = V_{REF} = 4.7\,\text{V}$. Let $\beta = 100$ and $V_{BE}(\text{on}) = 0.7\,\text{V}$ for all transistors. (a) Design the circuit such that $V_O = 10\,\text{V}$ and $I_Z = 10\,\text{mA}$ for a nominal supply voltage of $V^+ = 20\,\text{V}$. (b) Determine the regulator output resistance R_{of}.

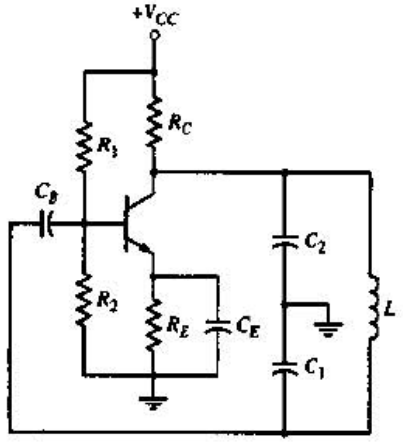


Figure P15.77

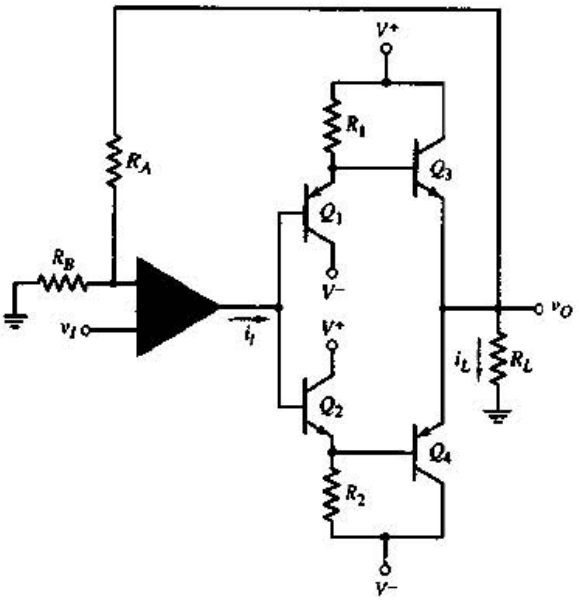


Figure P15.80

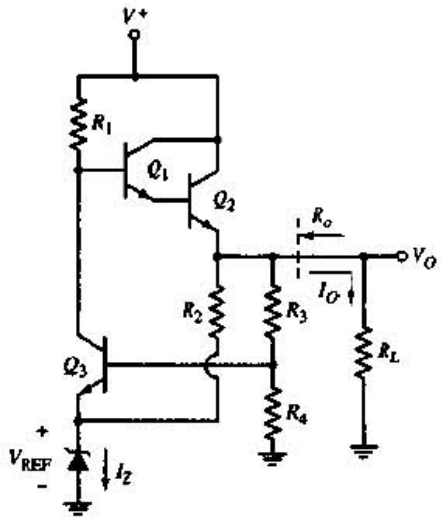


Figure P15.81

Industry Insight

PETER J. STARVASKI
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"The equations presented in the following chapters have found (and will continue to find) use throughout my career. Two examples come quickly to mind. The first stems from my involvement with a team whose goal was to improve the yield of one of our NMOS FET chips. This was an important project, needed to meet our customer's requirements. Engineers from a variety of disciplines were on the team. One hurdle everyone had to overcome was the fact that manufacturing engineers speak in terms of statistical process controls, product engineers speak in terms of specific failures for that product, design engineers speak in terms of their circuit models, etc.

The common language across all of these functions was the performance of the individual transistor. With only slight modifications, resulting from the idiosyncrasises of our manufacturing process, we used the FET equations in the following chapters. Everyone on the team needed to know these equations, as they dictate the parameters on the manufacturing floor, for the tester, in the circuit models, etc.

The second example occurred while I was designing the interrupt logic for a microprocessor. This was one of our early designs using CMOS FET technology. The input/output section of the chip was especially susceptible to a failure mechanism known as "latchup." Latchup is a bipolar phenomenon that occurs in a CMOS field effect transistor circuit (quite inadvertently—it's a result of the physical layout of the FET devices). None of our models correctly handled this effect, and we found ourselves using the BJT equations presented in the following chapters to understand and solve the problem. FET designers need to know bipolar theory!

Everything comes back to the basics. Whether you're working as part of a team with a variety of engineering disciplines, or tackling infant technologies, the equations and concepts you're about to study will be tools you'll need to call upon often. Treat each section with equal importance, for, as I've shown, being one type of designer does not preclude you from having to use another's equations.

Good luck with your studies."