(a) Design an NMOS logic circuit with depletion load to perform this function. Signals A, B, and C are available. (b) Assume $(W/L)_L = 1$, $V_{DD} = 5\,V$, $V_{TNL} = -1.5\,V$, and $V_{TND} = 0.8\,V$. Determine the W/L ratio of the other transistors such that the maximum logic 0 value in any part of the circuit is 0.2 V.

D16.27 Design an NMOS logic circuit with a depletion load that will sound an alarm in an automobile if the ignition is turned off while the headlights are still on and/or the parking brake has not been set. Separate indicator lights are also to be included showing whether the headlights are on or the parking brake needs to be set. State any assumptions that are made.

Section 16.3 CMOS Inverter

16.28 Consider the CMOS inverter in Figure 16.34. Let $K_p = K_n$, $V_{TN} = +0.8\,V$, $V_{TP} = -0.8\,V$, and $V_{DD} = 5\,V$. (a) Find the transition points for the p-channel and n-channel transistors. (b) Sketch the voltage transfer characteristic, including the appropriate voltage values at the transition points. (c) Find v_O for $v_I = 2\,V$ and for $v_I = 3\,V$.

16.29 For the CMOS inverter in Figure 16.34, let $V_{TN} = +0.4\,V$, $V_{TP} = -0.4\,V$, $k_n' = 80\,\mu a/V^2$, $k_p' = 40\,\mu A/V^2$, and $V_{DD} = 3.3\,V$. (a) Let $(W/L)_n = 2$ and $(W/L)_p = 4$. (i) Find the transition points for the p-channel and n-channel transistors. (ii) Sketch the voltage transfer characteristics including the appropriate voltage values at the transition points. (iii) Find v_I when $v_O = 0.4\,V$ and when $v_O = 2.9\,V$. (b) For $(W/L)_n = (W/L)_p = 2$, repeat part (a).

16.30 Consider the CMOS inverter pair in Figure P16.30. Let $V_{TN} = 0.8\,V$, $V_{TP} = -0.8\,V$, and $K_n = K_p$. (a) If $v_{O1} = 0.6\,V$, determine v_I and v_{O2}. (b) Determine the range of v_{O2} for which both N_2 and P_2 are biased in the saturation region.

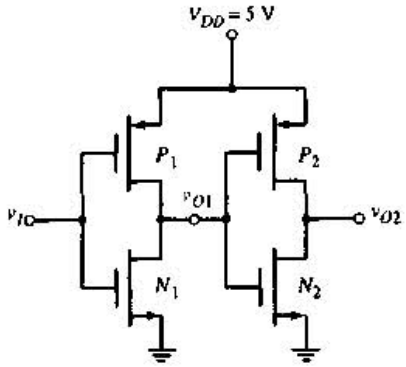


Figure P16.30

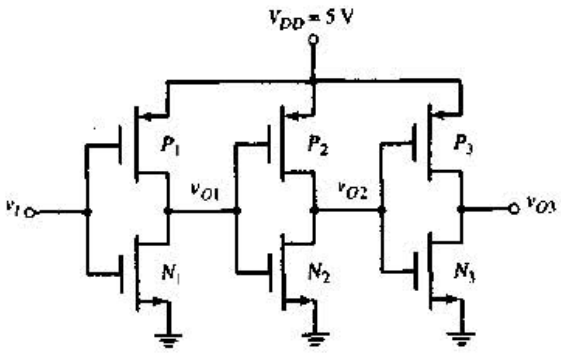


Figure P16.31

16.31 Consider the series of CMOS inverters in Figure P16.31. The threshold voltages of the n-channel transistors are $V_{TN} = 0.8\,V$, and the threshold voltages of the p-channel transistors are $V_{TP} = -0.8\,V$. The conduction parameters are all equal. (a) Determine the range of v_{O1} for which both N_1 and P_1 are biased in the saturation region. (b) If $v_{O2} = 0.6\,V$, determine the values of v_{O3}, v_{O1}, and v_I.

16.32 For the CMOS inverter in Figure 16.34, (a) calculate and plot the current through the transistors as a function of the input voltage for $0 \le v_I \le 5\,V$. Assume $K_n = K_p = 0.1\,mA/V^2$, $V_{TN} = 0.8\,V$, $V_{TP} = -0.8\,V$, and $V_{DD} = 5\,V$. (b) Repeat part (a) for $V_{DD} = 15\,V$.

16.33 The transistor parameters in the CMOS inverter are: $k_n' = 50\,\mu A/V^2$, $k_p' = 25\,\mu A/V^2$, $V_{TN} = 0.8\,V$, and $V_{TP} = -0.8\,V$. (a) For $(W/L)_n = 2$ and $(W/L)_p = 4$, determine the peak current in the inverter during a switching cycle for $V_{DD} = 5\,V$. (b) Repeat part (a) for $(W/L)_n = (W/L)_p = 2$.

16.34 A load capacitor of 0.2 pF is connected to the output of a CMOS inverter. Determine the power dissipated in the CMOS inverter for a switching frequency of 10 MHz, for inverter parameters described in (a) Problem 16.32 and (b) Problem 16.33.

16.35 A CMOS digital logic circuit contains the equivalent of 2 million CMOS inverters and is biased at $V_{DD} = 5\,V$. (a) The equivalent load capacitance of each inverter is 0.4 pF and each inverter is switching at 150 MHz. Determine the total average power dissipated in the circuit. (b) If the switching frequency is doubled, but the total power dissipated is to remain the same and the load capacitance remains constant, determine the required bias voltage.

16.36 Consider a CMOS inverter. (a) Show that when $v_I \cong V_{DD}$, the resistance of the NMOS device is approximately $1/[k_n'(W/L)_n(V_{DD} - V_{TN})]$, and when $v_I \cong 0$, the resistance of the PMOS device is approximately $1/[k_p'(W/L)_p(V_{DD} + V_{TP})]$. (b) Using the results of part (a), determine the maximum current that the NMOS device can sink such that the output voltage stays below 0.5 V, and determine the maximum current that the PMOS device can source such that the output voltage does not drop more than 0.5 V below V_{DD}.

16.37 Consider the CMOS inverter in Figure 16.34. Let $K_p = K_n$, $V_{TN} = +1.5\,V$, $V_{TP} = -1.5\,V$, and $V_{DD} = 10\,V$. Determine the two values of v_I and the corresponding values of v_O for which $(dv_O/dv_I) = -1$ on the voltage transfer characteristics. What are the noise margins?

16.38 Repeat Problem 16.37 if the CMOS inverter transistor parameters are: $V_{TN} = +1.5\,V$, $V_{TP} = -1.5\,V$, $K_n = 100\,\mu A/V^2$, and $K_p = 50\,\mu A/V^2$. Let $V_{DD} = 10\,V$.

Section 16.4 CMOS Logic Circuits

16.39 Consider the three-input CMOS NAND circuit in Figure P16.39. Assume $k_n' = 2k_p'$ and $V_{TN} = |V_{TP}| = 0.8\,V$. (a) If $v_A = v_B = 5\,V$, determine v_C such that both N_3 and

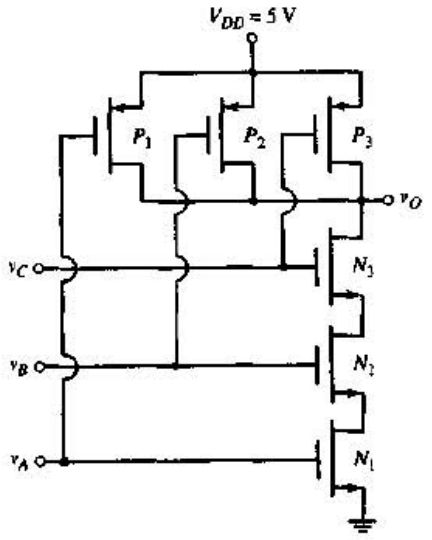


Figure P16.39

P_3 are biased in the saturation region when $(W/L)_p = 2(W/L)_n$. (State any assumptions you make.) (b) If $v_A = v_B = v_C = v_t$, determine the relationship between $(W/L)_p$ and $(W/L)_n$ such that $v_t = 2.5\,\text{V}$ when all transistors are biased in the saturation region. (c) Using the results of part (b) and assuming $v_A = v_B = 5\,\text{V}$, determine v_C such that both N_3 and P_3 are biased in the saturation region. (State any assumptions you make.)

16.40 Consider the circuit in Figure P16.40. (a) The inputs v_X, v_Y, and v_Z listed in the following table are either a logic 0 or a logic 1. These inputs are the outputs from similar-type CMOS logic circuits. The input logic conditions listed are sequential in time. State whether the transistors listed are "on" or "off," and determine the output voltage. (b) What logic function does this circuit implement?

v_X	v_Y	v_Z	N_1	N_2	N_3	N_4	N_5	v_O
1	0	1						
0	0	1						
1	1	0						
1	1	1						

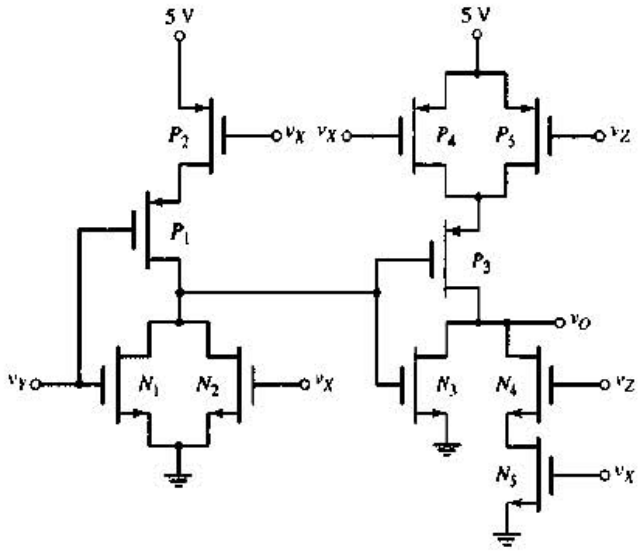


Figure P16.40

D16.41 (a) Given inputs A, B, and C, design a CMOS circuit to implement the logic function $Y = ABC + \overline{ABC}$. (b) For $k_n' = 2k_p'$ and assuming a minimum width-to-length ratio of unity, size the transistors in the design to provide equal composite conduction parameters.

D16.42 (a) Given inputs A, B, C, and D, design a CMOS circuit to implement the logic function $Y = \overline{(A+B)C + D}$. (b) Repeat part (b) of Problem 16.41 for this circuit.

16.43 Determine the logic function implemented by the circuit in Figure P16.43.

D16.44 Consider a five-input CMOS NAND logic gate. Assume that $k_n' = 2k_p'$ and assume that the minimum width-to-length ratio of any single transistor is unity. Design the width-to-length ratio of each transistor such that the composite conduction parameters of the NMOS and PMOS portions of the circuit are equal and such that the composite conduction parameters are equal to those of a CMOS inverter in which $(W/L)_n = 1$ and $(W/L)_p = 2$.

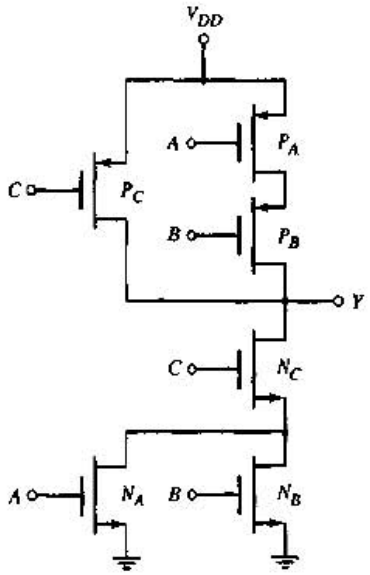


Figure P16.43

***D16.45** (a) Consider a six-input CMOS NOR logic gate whose output is connected to a CMOS inverter, so the output is an OR logic function. Repeat Problem 16.44 for this circuit. (b) Redesign the circuit such that three inputs are connected to one three-input CMOS NOR gate, the other three inputs are connected to another three-input CMOS NOR gate, and the outputs of the NOR gates are connected to a two-input CMOS NAND gate. The output of the NAND gate is still the OR function of the six inputs. Design these logic circuits using the specifications of Problem 16.44. Compare the size of transistors in this design compared to that of part (a). What can be said about the expected propagation delay times of the two circuits?

Section 16.5 Clocked CMOS Logic Circuits

16.46 (a) Figure P16.46 shows a clocked CMOS logic circuit. Make a table showing the state of each transistor ("on" or "off"), and determine the output voltages v_{O1} and v_{O2} for the input logic states listed in the following table. Assume the input conditions are sequential in time from state 1 to state 6. (b) What logic function does the circuit implement?

State	CLK	v_A	v_B	v_C
1	0	0	0	0
2	1	1	0	0
3	0	0	0	0
4	1	0	0	1
5	0	0	0	0
6	1	0	1	1

16.47 (a) For the circuit in Figure P16.47, make a table showing the state of each transistor ("on" or "off"), and determine the output voltages v_{O1}, v_{O2}, and v_{O3} for the input logic states listed in the following table. Assume the input conditions are sequential in time from state 1 to state 6. (b) What logic function does the circuit implement?

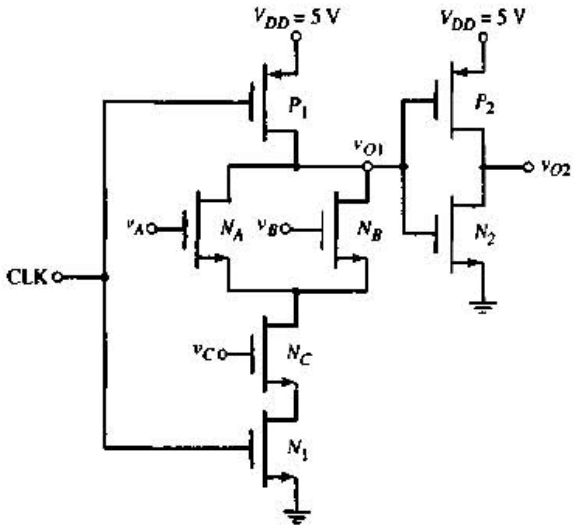


Figure P16.46

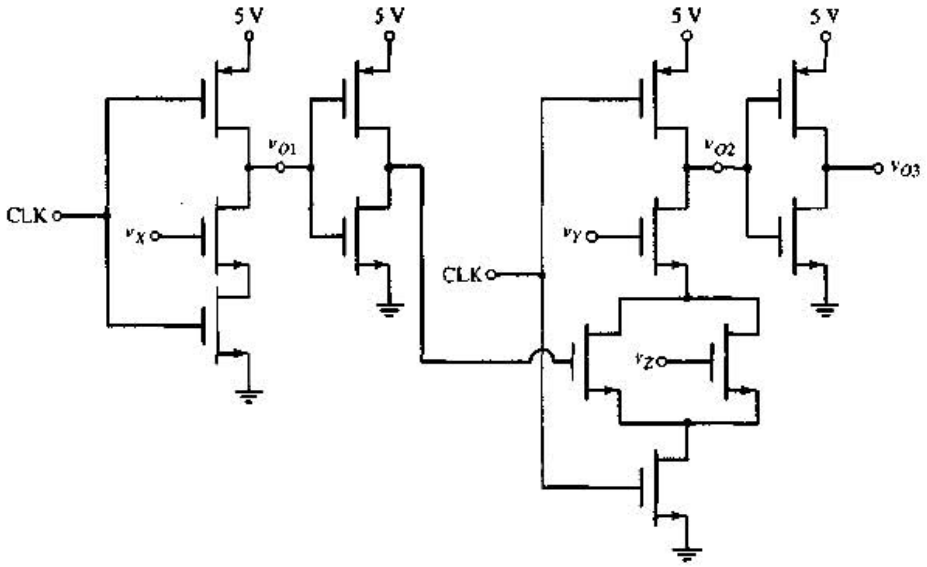


Figure P16.47

State	CLK	v_X	v_Y	v_Z
1	0	0	0	0
2	1	1	1	1
3	0	0	0	0
4	1	0	1	1
5	0	0	0	0
6	1	1	0	1

D16.48 Sketch a clocked CMOS domino logic circuit that realizes the function $Y = ABC + \overline{A}\,\overline{B}\,\overline{C}$.

D16.49 Sketch a clocked CMOS domino logic circuit that realizes the function $Y = (A + B)C + D$.

16.50 Consider the CMOS clocked circuit in Figure 16.52(b). Assume the effective capacitance at the v_{O1} terminal is 25 fF. If the leakage current through the M_{NA} and M_{NB} transistors is $I_{Leakage} = 2\,pA$ when these transistors and M_{P1} are cutoff, determine the time for which v_{O1} will decay by 0.5 V.

Section 16.6 Transmission Gates

16.51 The parameters of an NMOS transmission gate are $V_{TN} = 0.8\,V$, $K_n = 0.5\,mA/V^2$, and $C_L = 1\,pF$. (a) For a gate voltage of $\phi = 5\,V$, determine the quasi-steady-state output voltage for (i) $v_I = 0$, (ii) $v_I = 5\,V$, and (iii) $v_I = 2.5\,V$. (b) Repeat part (a) for a gate voltage of $\phi = 4\,V$.

D16.52 For the circuit in Figure P16.52, the input voltage v_I is either 0.1 V or 5 V. Let $\phi = 5\,V$. The threshold voltages are $V_{TN} = -1.5\,V$ for M_4 and $V_{TN} = 0.8\,V$ for all other transistors. The width-to-length ratios are 1 for M_2 and M_4 and 10 for M_A and M_B. (a) What are the logic 1 values of v_{O1} and v_{O2}? (b) Design the width-to-length ratios of M_1 and M_3 such that the logic 0 values of v_{O1} and v_{O2} are 0.1 V.

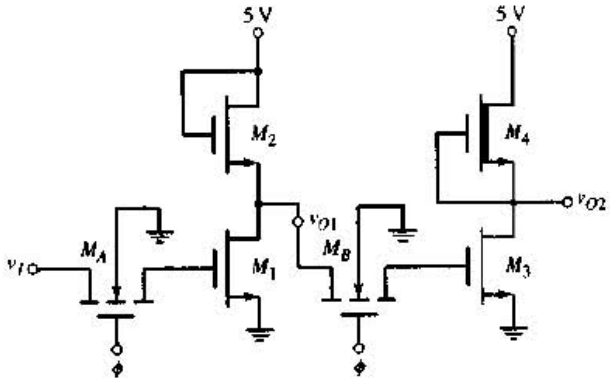


Figure P16.52

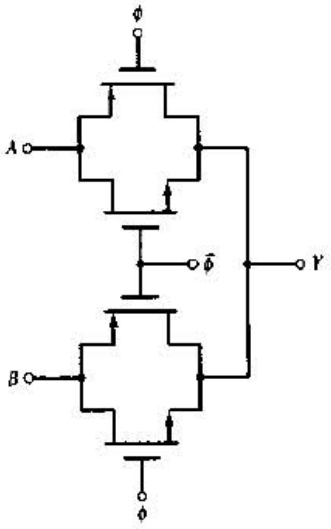


Figure P16.53

16.53 What is the logic function implemented by the circuit shown in Figure P16.53? Assume that all inputs are either 0 or 5 V.

16.54 Consider the circuit in Figure P16.54. What logic function is implemented by this circuit? Are there any potential problems with this circuit?

16.55 What is the logic function implemented by the circuit in Figure P16.55?

16.56 Consider the circuit in Figure P16.56. Signals ϕ_1 and ϕ_2 are nonoverlapping clock signals. Describe the operation of the circuit and the logic function implemented. Discuss any possible relationship between the width-to-length ratios of the load and driver transistors for "proper" circuit operation.

16.57 The circuit in Figure P16.57 is a form of clocked shift register. Signals ϕ_1 and ϕ_2 are nonoverlapping clock signals. Describe the operation of the circuit. Discuss any possible relationship between the width-to-length ratios of the load and driver transistors for "proper" circuit operation.

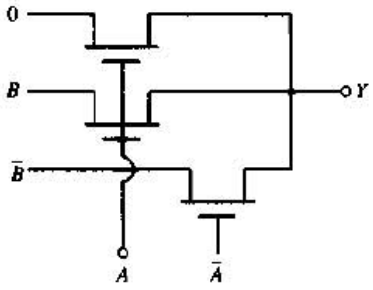


Figure P16.54

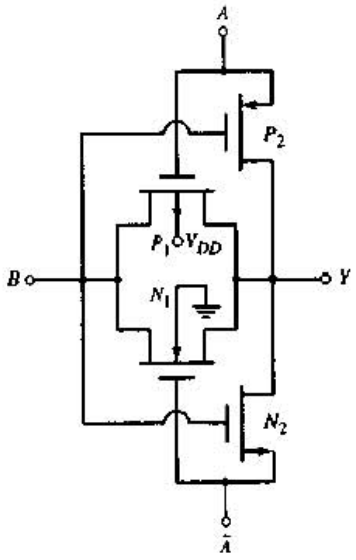


Figure P16.55

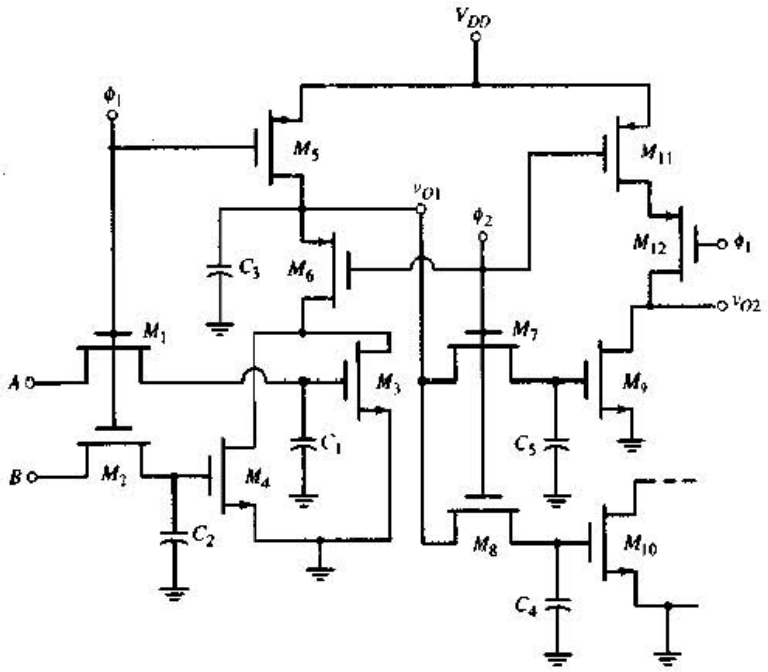


Figure P16.56

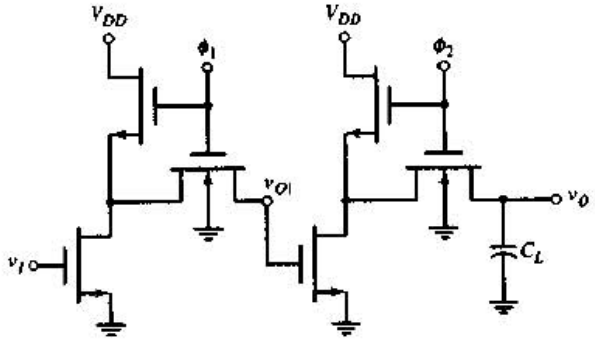


Figure P16.57

Section 16.7 Sequential Logic Circuits

16.58 Consider the NMOS R–S flip-flop in Figure 16.71 biased at $V_{DD} = 5\,V$. The threshold voltages are 1 V (enhancement-mode devices) and $-2\,V$ (depletion-mode devices). The conduction parameters are $K_3 = K_6 = 30\,\mu A/V^2$, $K_2 = K_5 = 100\,\mu A/V^2$, and $K_1 = K_4 = 200\,\mu A/V^2$. If Q = logic 0 and $\overline{Q}$ = logic 1 initially, determine the voltage at S that will cause the flip-flop to change states.

16.59 A CMOS R–S flip-flop is shown in Figure P16.59. Assume $V_{DD} = 5\,V$, $|V_{TN}| = |V_{TP}| = 1\,V$, $K_1 = K_2 = K_3 = K_4 \equiv K$, and $K_5 = K_6$. If Q = logic 1 and $\overline{Q}$ = logic 0 initially, determine the relationship between K_5 and K such that the flip-flop changes state when $R = 2.5\,V$.

D16.60 The CMOS R–S flip-flop in Figure P15.59 is not a fully complementary CMOS design. Design a fully complementary CMOS clocked R–S flip-flop. [Note: the design contains 12 transistors.]

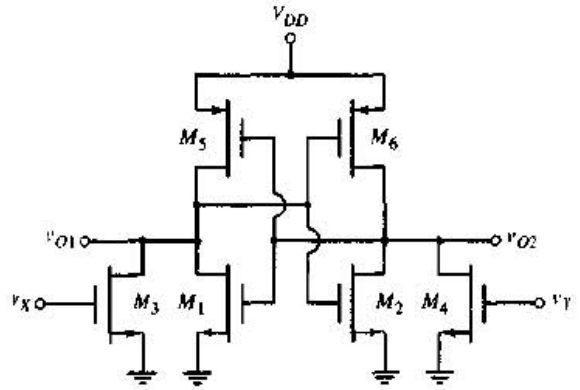


Figure P16.59

D16.61 The circuit in Figure P16.61 is an example of a D flip-flop. (a) Explain the operation of the circuit. Is this a positive- or negative-edge-triggered flip-flop? (b) Redesign the circuit to make this a static flip-flop.

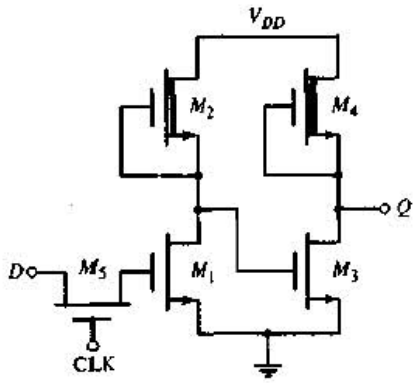


Figure P16.61

16.62 Show that the circuit in Figure P16.62 is a J–K flip-flop.

16.63 Reconsider the circuit shown in Figure P16.40. Show that this circuit is a J–K flip-flop with $J = v_X$, $K = v_Y$, and CLK $= v_Z$.

Section 16.8 Memories: Classifications and Architectures

16.64 A 64-K memory is organized in a square array and uses the NMOS NOR decoder in Figure 16.81(b) for the row- and column decoders. (a) How many inputs does each decoder require? (b) What input to the row decoder is required to address rows (i) 94 and (ii) 239? (c) What input to the column decoder is required to address columns (i) 39 and (ii) 123?

D16.65 A 1024-bit RAM consists of 128 words of 8 bits each. Design the memory array to minimize the number of row and column address decoder transistors required. How many row and column address lines are necessary?

16.66 Assume that an NMOS address decoder can source 250 μA when the output goes high. If the effective capacitance of each memory cell is $C_L = 0.8\,\text{pF}$ and the effective capacitance of the address line is $C_{LA} = 5\,\text{pF}$, determine the rise time of the address line voltage if $V_{IH} = 2.7\,\text{V}$.

Section 16.9 RAM Memory Cells

D16.67 Consider the NMOS RAM cell with resistor load in Figure 16.82(b). Assume parameter values of $k_n' = 35\,\mu\text{A/V}^2$, $V_{TN} = 0.7\,\text{V}$, $V_{DD} = 5\,\text{V}$, and $R = 1\,\text{M}\Omega$. (a) Design the width-to-length ratios such that $v_{DS} = 0.1\,\text{V}$ for the on transistor. (b) Consider a 16-K memory with the cell described in part (a). Determine the standby current and power of the memory for a standby voltage of $V_{DD} = 2\,\text{V}$.

D16.68 A 16-K NMOS RAM, with the cell design shown in Figure 16.82(b), is to dissipate no more than 200 mW in standby when biased at $V_{DD} = 2.5\,\text{V}$. Design the width-to-length ratios of the transistors and the resistance value. Assume $V_{TN} = 0.7\,\text{V}$ and $k_n' = 35\,\mu\text{A/V}^2$.

***16.69** Consider the CMOS RAM cell and data lines in Figure 16.84 biased at $V_{DD} = 5\,\text{V}$. Assume transistor parameters $k_n' = 40\,\mu\text{A/V}^2$, $k_p' = 20\,\mu\text{A/V}^2$, $V_{TN} = 0.8\,\text{V}$, $V_{TP} = -0.8\,\text{V}$, $W/L = 2$ (M_{N1} and M_{N2}), $W/L = 4$ (M_{P1} and M_{P2}), and $W/L =$

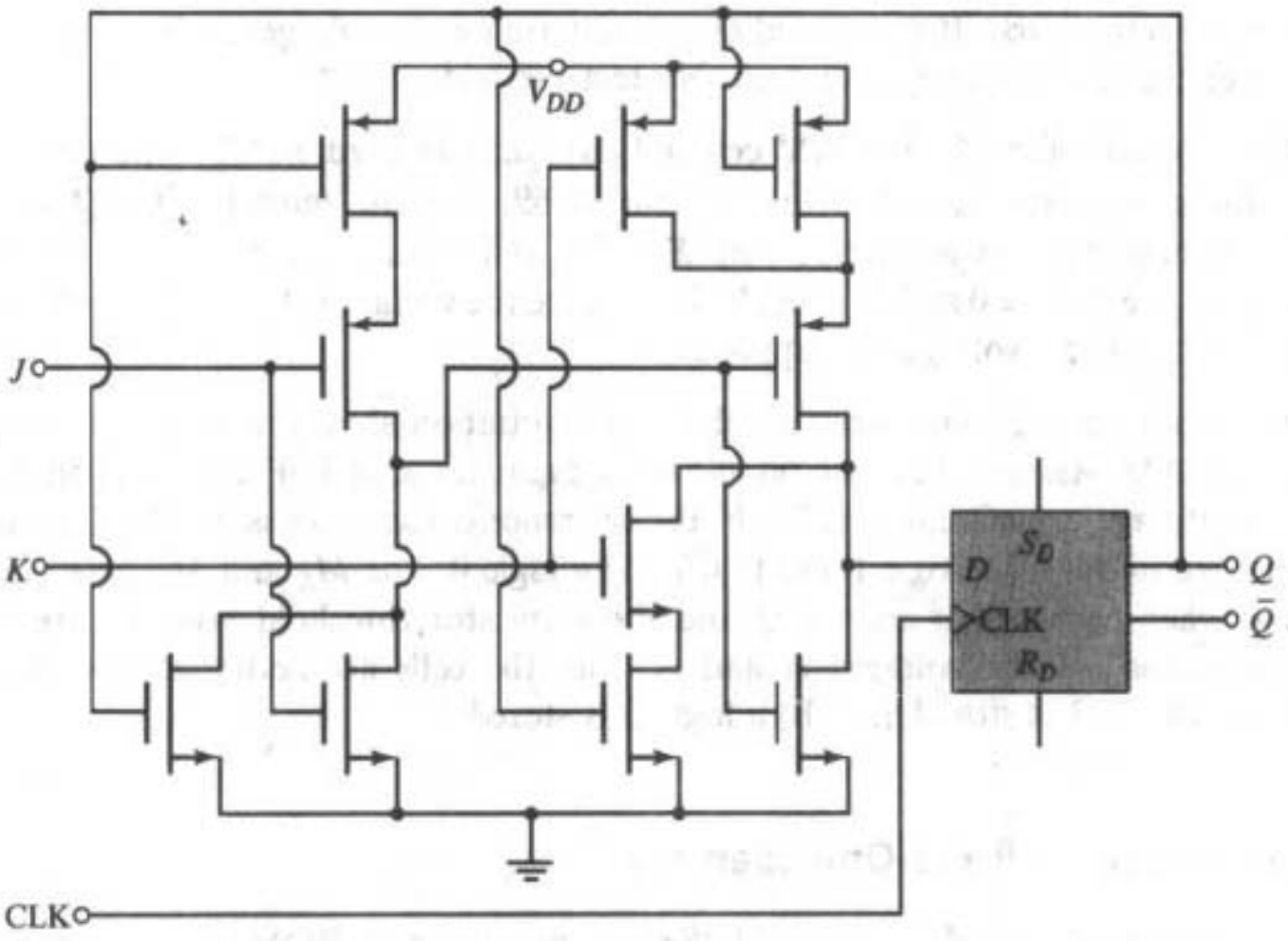


Figure P16.62

1 (all other transistors). If $Q = 0$ and $\overline{Q} = 1$, determine the voltages at D and $\overline{D}$ a short time after the row has been addressed. Neglect the body effect.

***16.70** Consider the CMOS RAM cell and data lines in Figure 16.84 with circuit and transistor parameters described in Problem 16.69. Assume initially that $Q = 0$ and $\overline{Q} = 1$. Assume the row is selected with $X = 5\,\text{V}$ and assume the data lines, through a write cycle, are at $\overline{D} = 0$ and $D = 4.2\,\text{V}$. Determine the voltages at Q and $\overline{Q}$ a short time after the write cycle voltages are applied.

***16.71** Consider a general sense amplifier configuration shown in Figure 16.90 for a dynamic RAM. Assume that each bit line has a capacitance of 1 pF and is precharged to 4 V. The storage capacitance is 0.05 pF, the reference capacitance is 0.025 pF, and each are charged to 5 V for a logic 1 and to 0 V for a logic 0. The M_S and M_R gate voltages are 5 V when each cell is addressed and the transistor threshold voltages are 0.5 V. Determine the bit line voltages v_1 and v_2 after the cells are addressed for the case when (a) a logic 1 is stored and (b) a logic 0 is stored.

Section 16.10 Read-Only Memory

D16.72 Design a 4-word × 4-bit NMOS mask-programmed ROM to produce outputs of 1011, 1111, 0110, and 1001 when rows 1, 2, 3, and 4, respectively, are addressed.

D16.73 Design an NMOS 16 × 4 mask-programmed ROM that provides the 4-bit product of two 2-bit variables.

D16.74 Design an NMOS mask-programmed ROM that decodes a binary input and produces the output for a seven-segment array. (See Figure 2.40, Chapter 2.) The output is to be high when a particular LED is to be turned on.

COMPUTER SIMULATION PROBLEMS

16.75 The three types of NMOS inverters are shown in Figures 16.5(a), 16.8(a), and 16.10(a). Using PSpice, investigate the voltage transfer characteristics and the current versus input voltage characteristics for the three types of inverters as a function of various width-to-length ratios and as a function of the body effect.

16.76 Again consider the three-types of NMOS inverters. Investigate the propagation delay times and switching characteristics of the three types of inverters using PSpice. Consider a series of inverters as shown in Figure 16.19. Include appropriate transistor capacitance values and assume effective C_T load capacitor values of 0.2 pF. Determine the propagation delay times with and without the body effect. Consider various transistor width-to-length ratios.

16.77 Consider a three-input CMOS NAND logic circuit similar to the two-input circuit shown in Figure 16.45(a). Using PSpice, investigate the voltage transfer characteristics and the current versus input voltage characteristics for various transistor width-to-length ratios and various input conditions similar to the results in Figure 16.46 for the CMOS NOR circuit.

16.78 Investigate the propagation delay times and switching characteristics of the CMOS inverter using PSpice. Set up a series of CMOS inverters similar to the series of inverters shown in Figure 16.19. Include appropriate transistor capacitance values and assume effective C_T load capacitor values of 0.2 pF. Determine the propagation delay times as a function of various transistor width-to-length ratios.

16.79 Consider the dynamic shift register shown in Figure 16.68. Assume appropriate transistor and load capacitance values. Using PSpice, investigate the transient effects in voltages v_{O1}, v_{O2}, v_{O3}, and v_{O4} after the clock signals go to zero.

DESIGN PROBLEMS

***D16.80** Design an NMOS logic circuit that will implement the logic function $Y = (A + (B \cdot C)) \cdot D$.

***D16.81** Design clocked CMOS logic circuits that will implement the logic functions: (a) $Y = [\overline{A + (B \cdot C)}]$, and (b) $Y = [\overline{(A + B) \cdot (C + D)}]$. If the smallest width-to-length ratio is 2, determine the appropriate width-to-length ratios of each transistor in your design.

***D16.82** Design an NMOS pass logic network that implements the logic functions described in Problem 16.81.

***D16.83** Design a clocked CMOS R–S flip-flop such that the output becomes valid on the negative-going edge of a clock signal.

***D16.84** Design a clocked CMOS dynamic shift register in which the output becomes valid on the positive-going edge of a clock signal.

CHAPTER

17

Bipolar Digital Circuits

17.0 PREVIEW

In the previous chapter, we presented the basic concepts of MOSFET logic circuits. In this chapter, we discuss the basic principles of bipolar logic circuits. Prior to the emergence of the MOS digital technology, the bipolar digital family of transistor–transistor logic circuits was used extensively. Bipolar digital circuits are now used less frequently because of their relatively large power requirements.

Our study of bipolar digital circuits begins with emitter-coupled logic (ECL). This is the fastest bipolar technology and is used in specialized applications where high speed is required. One price to pay for high speed is a relatively low noise margin. The basis of ECL is a differential amplifier that is operated in the nonlinear region.

A bipolar technology that has a higher noise margin is transistor–transistor logic (TTL). Transistors in this technology are driven between cutoff and saturation. The storage time related to transistors driven into saturation slows the switching speed of TTL compared to that of ECL. Higher speed in TTL is achieved in Schottky TTL circuits. The basic principle of the Schottky transistor is discussed and the transistor is then applied to digital circuits. Low-power Schottky TTL makes a trade-off between speed and power.

The BiCMOS inverter and BiCMOS digital logic circuit are considered. These circuits take advantage of the low-power properties of CMOS and the high-current drive capability of bipolar transistors.

17.1 EMITTER-COUPLED LOGIC (ECL)

The emitter-coupled logic (ECL) circuit is based on the differential amplifier circuit, which we studied in Chapter 11 in the context of linear amplifiers. In digital applications, the diff-amp is driven into its nonlinear region. The transistors are either cut off or in the active region. Saturation is avoided in order to minimize switching times and propagation delay times. ECL circuits have the shortest propagation delay times of any bipolar digital technology.

17.1.1 Differential Amplifier Circuit Revisited

Consider the basic diff-amp circuit in Figure 17.1. For a linear diff-amp, the input voltages are small and both transistors remain biased in the active region at all times. The relationship between collector currents and base–emitter voltages for Q_1 and Q_2 can be written[1]

$$i_{C1} = I_S e^{v_{BE1}/V_T} \tag{17.1(a)}$$

and

$$i_{C2} = I_S e^{v_{BE2}/V_T} \tag{17.1(b)}$$

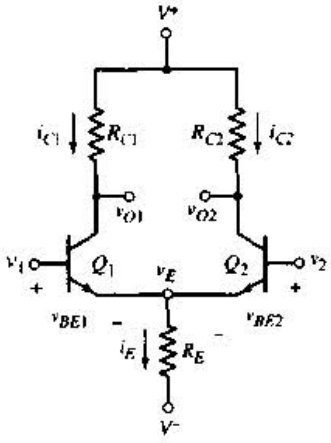


Figure 17.1 Basic differential amplifier circuit

where Q_1 and Q_2 are assumed to be matched and parameter I_S is the same for both devices. The current–voltage transfer curves are shown in Figure 17.2.

In digital applications, the input voltages are large, which means that one transistor remains biased in its active region while the opposite transistor is cut off. For example, if $v_{BE1} = v_{BE2} + 0.12$, then the ratio of i_{C1} and i_{C2} is

$$\frac{i_{C1}}{i_{C2}} = \frac{e^{v_{BE1}/V_T}}{e^{v_{BE2}/V_T}} = e^{(v_{BE1}-v_{BE2})/V_T} = e^{0.12/0.026} = 101 \tag{17.2}$$

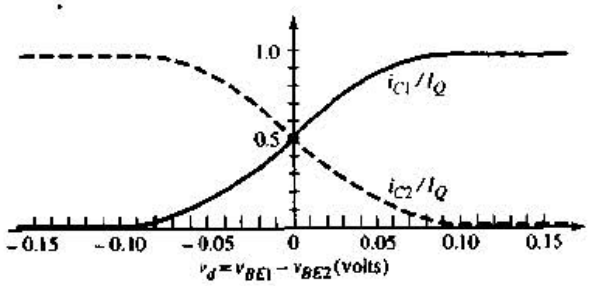


Figure 17.2 Normalized dc transfer characteristics, BJT differential amplifier

[1] In most cases in this chapter, total instantaneous current and voltage parameters are used, even though most analyses of logic circuits involve dc calculations.

When the base–emitter voltage of Q_1 is 120 mV greater than the base–emitter voltage of Q_2, the collector current of Q_1 is 100 times that of Q_2; for all practical purposes, Q_1 is on and Q_2 is cut off.

Conversely, if v_1 is less than v_2 by at least 120 mV, then Q_1 is effectively cut off and Q_2 is on. The difference amplifier, when operating as a digital circuit, operates as a current switch. When $v_1 > v_2$ by at least 120 mV, it switches an approximately constant current through R_E to Q_1; when $v_2 > v_1$ by at least 120 mV, the current goes to Q_2.

Example 17.1 **Objective:** Calculate the currents and voltages in the basic differential amplifier circuit used as a digital circuit.

Consider the circuit in Figure 17.1. Assume that $V^+ = -V^- = 5\,\text{V}$, $R_{C1} = R_{C2} \equiv R_C = 1\,\text{k}\Omega$, $R_E = 2.15\,\text{k}\Omega$, and $v_2 = 0$. In the dc analysis, assume that dc base currents are negligible.

Solution: For $v_1 = 0$, both transistors are on. Assuming a base–emitter turn-on voltage of 0.7 V, then $v_E = -0.7\,\text{V}$ and

$$i_E = \frac{v_E - V^-}{R_E} = \frac{-0.7 - (-5)}{2.15} = 2.0\,\text{mA}$$

Assuming Q_1 and Q_2 are matched, we have $i_{C1} = i_{C2} = i_E/2$ since $v_{BE1} = v_{BE2}$ and $i_{C1} = i_{C2} \equiv i_C = 1\,\text{mA}$. In this case,

$$v_{O1} = v_{O2} = V_{CC} - i_C R_C = 5 - (1)(1) = 4\,\text{V}$$

Both Q_1 and Q_2 are now biased in the active region.

Now let $v_1 = -1\,\text{V}$. Since the base voltage of Q_1 is less than the base voltage of Q_2 by more than 120 mV, Q_1 is cut off and Q_2 is on. In this case, $v_E = v_2 - V_{BE}(\text{on}) = -0.7\,\text{V}$ and $i_E = 2\,\text{mA}$, as before. However, $i_{C1} = 0$ and $i_{C2} = i_E = 2\,\text{mA}$, so that

$$v_{O1} = V_{CC} = 5\,\text{V}$$

and

$$v_{O2} = V_{CC} - i_{C2} R_C = 5 - (2)(1) = 3\,\text{V}$$

For $v_1 = +1\,\text{V}$, Q_1 is on and Q_2 is cut off. For this case, $v_E = v_1 - V_{BE}(\text{on}) = 1 - 0.7 = +0.3\,\text{V}$, the current i_E is

$$i_E = i_{C1} = \frac{v_E - V^-}{R_E} = \frac{0.3 - (-5)}{2.15} = 2.47\,\text{mA}$$

and

$$v_{O1} = V_{CC} - i_{C1} R_C = 5 - (2.47)(1) = 2.53\,\text{V}$$

and

$$v_{O2} = V_{CC} = 5\,\text{V}$$

Comment: For the three conditions given, transistors Q_1 and Q_2 are biased either in cutoff or in the active region. In terms of digital applications, output v_{O2} is in phase with input v_1 and output v_{O1} is 180 degrees out of phase.

When biased on, transistor Q_1 conducts slightly more heavily than Q_2 when it is conducting. To obtain symmetrical complementary outputs, R_{C1} should therefore be slightly smaller than R_{C2}.

Test Your Understanding

D17.1 Consider the differential amplifier circuit in Figure 17.1 biased at $V^+ = 5\,\text{V}$, $V^- = -5\,\text{V}$, and $v_2 = 0$. Assume $V_{BE}(\text{on}) = 0.7\,\text{V}$ and neglect base currents. (a) Design the circuit such that $i_E = 1\,\text{mA}$ and $v_{O1} = v_{O2} = 3.5\,\text{V}$ when $v_1 = 0$. (b) Using the results of part (a), calculate i_E, v_{O1}, and v_{O2} for: (i) $v_1 = +1\,\text{V}$, and (ii) $v_1 = -1\,\text{V}$. (Ans. (a) $R_E = 4.3\,\text{k}\Omega$, $R_{C1} = R_{C2} = 3\,\text{k}\Omega$ (b) (i) $i_E = 1.23\,\text{mA}$, $v_{O1} = 1.31\,\text{V}$, $v_{O2} = 5\,\text{V}$ (ii) $v_{O2} = 2\,\text{V}$, $v_{O1} = 5\,\text{V}$)

17.1.2 Basic ECL Logic Gate

A basic two-input ECL OR/NOR logic circuit is shown in Figure 17.3. The two input transistors, Q_1 and Q_2, are connected in parallel. On the basis of the differential amplifier, if both v_X and v_Y are less than the reference voltage V_R (by at least 120 mV), then both Q_1 and Q_2 are cut off, while the reference transistor Q_R is biased on its active region. In this situation, the output voltage v_{O1} is greater than v_{O2}. If either v_X or v_Y becomes greater than V_R, then Q_R turns off and v_{O2} becomes larger than v_{O1}. The OR logic is at the v_{O2} output and the NOR logic is at the v_{O1} output. An advantage of ECL gates is the availability of complementary outputs, precluding the need for separate inverters to provide the complementary outputs.

One problem with the OR/NOR circuit in Figure 17.3 is that the output voltage levels differ from the required input voltage levels; the output voltages are not compatible with the input voltages. The mismatch arises because ECL

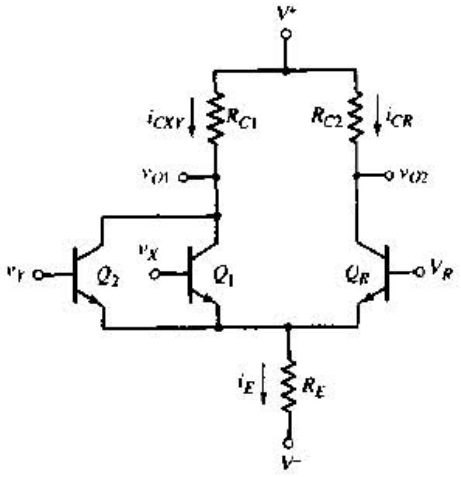


Figure 17.3 Basic two-input ECL OR/NOR logic circuit

circuit transistors operate between their cutoff and active regions, requiring that the base–collector junctions be reverse biased at all times. We see that a logic 1 voltage of the output is $V_{OH} = V^+$. If this voltage were to be applied to either the v_X or v_Y input, then either Q_1 or Q_2 would turn on and the collector voltage v_{O1} would decrease below V^+; the base–collector voltage would then become forward biased and the transistor would go into saturation. Emitter-follower circuits are added to provide outputs that are compatible with the inputs of similar gates.

Test Your Understanding

D17.2 For the ECL logic gate in Figure 17.3, the bias voltages are: $V^+ = 3.5\,\text{V}$, $V^- = -3.5\,\text{V}$, and $V_R = 1.5\,\text{V}$. Assume $V_{BE}(\text{on}) = 0.7\,\text{V}$ and neglect base currents. (a) Determine R_E and R_{C2} such that $i_E = 2\,\text{mA}$ and $v_{O2} = 2\,\text{V}$ when $v_x = v_y = \text{logic 0}$. (b) Find R_{C1} such that $v_{O1} = 2\,\text{V}$ when $v_x = v_y = 2\,\text{V}$. What is i_E? (Ans. (a) $R_E = 2.15\,\text{k}\Omega$, $R_{C2} = 0.75\,\text{k}\Omega$ (b) $i_E = 2.23\,\text{mA}$, $R_{C1} = 0.673\,\text{k}\Omega$)

ECL Logic Gate with Emitter Followers

In the ECL circuit in Figure 17.4, emitter followers are added to the OR/NOR outputs, and supply voltage V^+ is set equal to zero. The ground and power supply voltages are reversed because analyses show that using the collector–emitter voltage as the output results in less noise sensitivity. If the forward current gain of the transistors is on the order of 100, then the dc base currents may be neglected with little error in the calculations.

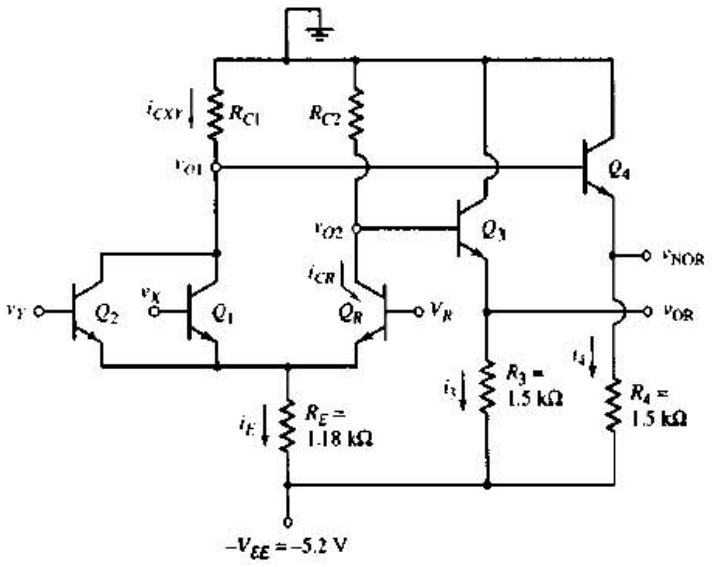


Figure 17.4 Two-input ECL OR/NOR logic gate with emitter-follower output stages

If either v_X or v_Y is a logic 1 (defined as greater than V_R by at least 120 mV), then the reference transistor Q_R is cut off, $i_{CR} = 0$, and $v_{O2} = 0$. Output transistor Q_3 is biased in the active region, and $v_{OR} = v_{O2} - V_{BE}(\text{on}) = -0.7\,\text{V}$. If both v_X and v_Y are a logic 0 (defined as less than V_R by at least 120 mV), then both Q_1 and Q_2 are cut off, $v_{O1} = 0$, and $v_{\text{NOR}} = 0 - V_{BE}(\text{on}) = -0.7\,\text{V}$. The largest possible voltage that can be achieved at either output is -0.7 V; therefore, -0.7 V is defined as the logic 1 level.

In the following example, we will determine the currents and the logic 0 values in the basic ECL gate.

Example 17.2 **Objective:** Calculate current, resistor, and logic 0 values in the basic ECL logic gate.

Consider the circuit in Figure 17.4. Determine R_{C1} and R_{C2} such that when Q_1, Q_2, and then Q_R are conducting, the B–C voltages are zero.

Solution: Let $v_X = v_Y = -0.7\,\text{V}$ = logic 1 > V_R such that Q_1 and Q_2 are on. We find that

$$v_E = v_X - V_{BE}(\text{on}) = -0.7 - 0.7 = -1.4\,\text{V}$$

and the current is

$$i_E = i_{Cxy} = \frac{v_E - V^-}{R_E} = \frac{-1.4 - (-5.2)}{1.18} = 3.22\,\text{mA}$$

In order for the B–C voltages of Q_1 and Q_2 to be zero, voltage v_{O1} must be -0.7 V. Therefore

$$R_{C1} = \frac{-v_{O1}}{I_{Cxy}} = \frac{0.7}{3.22} = 0.217\,\text{k}\Omega$$

The NOR output logic 0 value is then

$$v_{\text{NOR}} = v_{O1} - V_{BE}(\text{on}) = -0.70 - 0.7 = -1.40\,\text{V}$$

Input voltages v_X and v_Y are greater than V_R in a logic 1 state and less than V_R in a logic 0 state. If V_R is set at the midpoint between the logic 0 and logic 1 levels, then

$$V_R = \frac{-0.7 - 1.40}{2} = -1.05\,\text{V}$$

When Q_R is on, we have

$$v_E = V_R - V_{BE}(\text{on}) = -1.05 - 0.7 = -1.75\,\text{V}$$

and

$$i_E = i_{CR} = \frac{v_E - V^-}{R_E} = \frac{-1.75 - (-5.2)}{1.18} = 2.92\,\text{mA}$$

For $v_{O2} = -0.7$ V, we find that

$$R_{C2} = \frac{-v_{O2}}{i_{C2}} = \frac{0.7}{2.92} = 0.240\,\text{k}\Omega$$

The OR logic 0 value is therefore

$$v_{\text{OR}} = v_{O2} - V_{BE}(\text{on}) = -0.7 - 0.7 = -1.40\,\text{V}$$

Comment: For symmetrical complementary outputs, R_{C1} and R_{C2} are not equal. If R_{C1} and R_{C2} become larger than the designed values, transistors Q_1, Q_2, and Q_R will be driven into saturation when they are conducting.

Test Your Understanding

D17.3 Redesign the ECL circuit in Figure 17.4 such that the logic 0 values at the v_{OR} and v_{NOR} terminals are -1.5 V. The maximum value of i_E is to be 2.5 mA, and the maximum values of i_3 and i_4 are to be 2.5 mA. The bias voltages are as shown. Determine all resistor values and the value of V_R. (Ans. $R_E = 1.52\,\text{k}\Omega$, $R_{C1} = 320\,\Omega$, $V_R = -1.1$ V, $R_{C2} = 357\,\Omega$, $R_3 = R_4 = 1.8\,\text{k}\Omega$)

17.4 Using the results of Example 17.2, calculate the power dissipated in the circuit in Figure 17.4; for: (a) $v_x = v_y$ = logic 1, and (b) $v_x = v_y$ = logic 0. (Ans. (a) $P = 45.5$ mW (b) $P = 43.9$ mW)

The Reference Circuit

Another circuit is required to provide the reference voltage V_R. Consider the complete two-input ECL OR/NOR logic circuit shown in Figure 17.5. The reference circuit consists of resistors R_1, R_2, and R_5, diodes D_1 and D_2, and transistor Q_5. The reference portion of the circuit can be specifically designed to provide the desired reference volta-

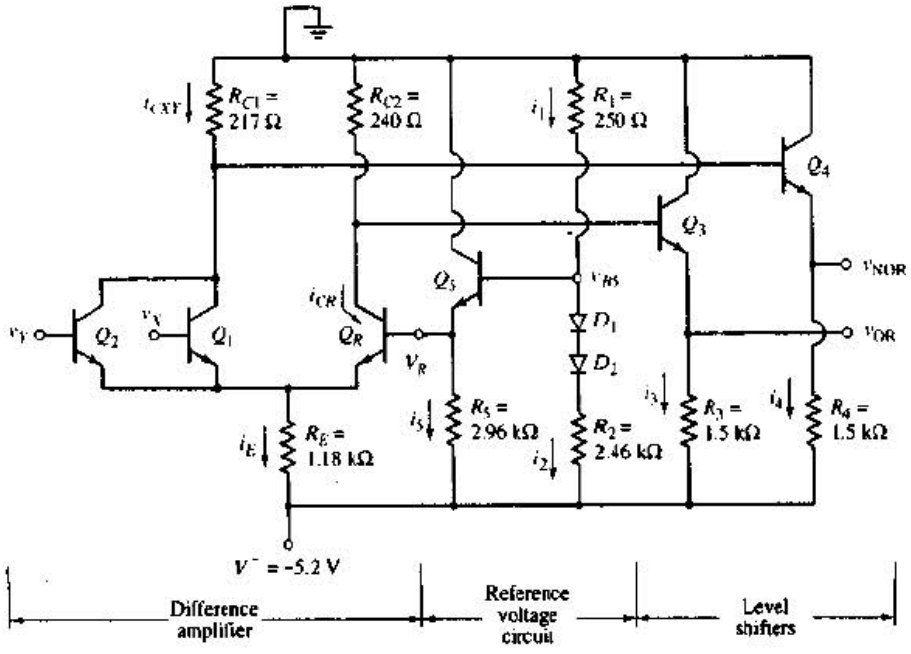


Figure 17.5 Basic ECL logic gate with reference circuit

Design Example 17.3 **Objective:** Design the reference portion of the ECL circuit.

Consider the circuit in Figure 17.5. The reference voltage V_R is to be -1.05 V.

Solution: We know that

$$v_{B5} = V_R + V_{BE}(\text{on}) = -1.05 + 0.7 = -0.35\,\text{V} = -i_1 R_1$$

Since there are two unknowns, we will choose one variable. Let $R_1 = 0.25\,\text{k}\Omega$. Then,

$$i_1 = \frac{0.35}{0.25} = 1.40\,\text{mA}$$

Since this current is on the same order of magnitude as other currents in the circuit, the chosen value of R_1 is reasonable. Neglecting base currents, we can now write

$$i_1 = i_2 = \frac{0 - 2V_\gamma - V^-}{R_1 + R_2}$$

where V_γ is the diode turn-on voltage and is assumed to be $V_\gamma = 0.7$ V. We then have

$$1.40 = \frac{-1.4 - (-5.2)}{R_1 + R_2}$$

which yields

$$R_1 + R_2 = 2.71\,\text{k}\Omega$$

Since $R_1 = 0.25\,\text{k}\Omega$, resistance R_2 is $R_2 = 2.46\,\text{k}\Omega$.

Also, we know that

$$i_5 = \frac{V_R - V^-}{R_5}$$

If we let $i_5 = i_1 = i_2 = 1.40$ mA, then

$$R_5 = \frac{V_R - V^-}{i_5} = \frac{-1.05 - (-5.2)}{1.40} = 2.96\,\text{k}\Omega$$

Comment: As with any design, there is no unique solution. The design presented will provide the required reference voltage to the base of Q_R.

17.1.3 ECL Logic Circuit Characteristics

In this section, we will determine the power dissipation, fanout, and propagation delay times for the ECL logic gate. We will also examine the advantage of using a negative power supply.

Power Dissipation

Power dissipation is an important characteristic of a logic circuit. The power dissipated in the basic ECL logic gate in Figure 17.5 is given by

$$P_D = (i_{Cx} + i_{CR} + i_5 + i_1 + i_3 + i_4)(0 - V^-) \tag{17.3}$$

Example 17.4 **Objective:** Calculate the power dissipated in the ECL logic circuit. Consider the circuit in Figure 17.5. Let $v_X = v_Y = -0.7\,\text{V}$ = logic 1.

Solution: From our previous analysis, we have $i_{C_{XY}} = 3.22\,\text{mA}$, $i_{CR} = 0$, $i_5 = 1.40\,\text{mA}$, and $i_1 = 1.40\,\text{mA}$, and the output voltages are $v_{\text{OR}} = -0.7\,\text{V}$ and $v_{\text{NOR}} = -1.40\,\text{V}$. The currents i_3 and i_4 are

$$i_3 = \frac{v_{\text{OR}} - V^-}{R_3} = \frac{-0.7 - (-5.2)}{1.5} = 3.0\,\text{mA}$$

and

$$i_4 = \frac{v_{\text{NOR}} - V^-}{R_4} = \frac{-1.40 - (-5.2)}{1.5} = 2.53\,\text{mA}$$

The power dissipation is then

$$P_D = (3.22 + 0 + 1.40 + 1.40 + 3.0 + 2.53)(5.2) = 60.0\,\text{mW}$$

Comment: This power dissipation is significantly larger than that in NMOS and CMOS logic circuits. The advantage of ECL, however, is the short propagation delay times, which can be less than 1 ns.

Propagation Delay Time

The major advantage of ECL circuits is their small propagation delay time, on the order of 1 ns or less. The two reasons for the short propagation delay times are: (1) the transistors are not driven into saturation, which eliminates any charge storage effects; and (2) the logic swing in the ECL logic gate is small (about 0.7 V), which means that the voltages across the output capacitances do not have to change as much as in other logic circuits. Also, the currents in the ECL circuit are relatively large, which means that these capacitances can charge and discharge quickly. However, the trade-offs for the small propagation delay time are higher power dissipation and smaller noise margins.

ECL circuits are very fast, and they require that special attention be paid to transmission line effects. Improperly designed ECL circuit boards can experience ringing or oscillations. These problems have less to do with the ECL circuits than with the interconnections between the circuits. Care must therefore be taken to terminate the signal lines properly.

Fanout

Figure 17.6 shows the emitter-follower output stage of the OR output of an ECL circuit used to drive the diff-amp input stage of an ECL load circuit. When v_{OR} is a logic 0, input load transistor Q_1' is cut off, effectively eliminating any load current from the driver output stage. With v_{OR} at a logic 1 level, the input load transistor is on and an input base current i_L' exists. (Up to this point, we have neglected dc base currents; however, they are not zero.) The load current must be supplied through Q_3, whose base current is supplied through R_{C2}. As the load current i_L increases with the addition of more load circuits, a voltage drop occurs across R_{C2} and the output voltage decreases. The maximum fanout is determined partially by the maximum amplitude that the output voltage is allowed to drop from its ideal logic 1 value.

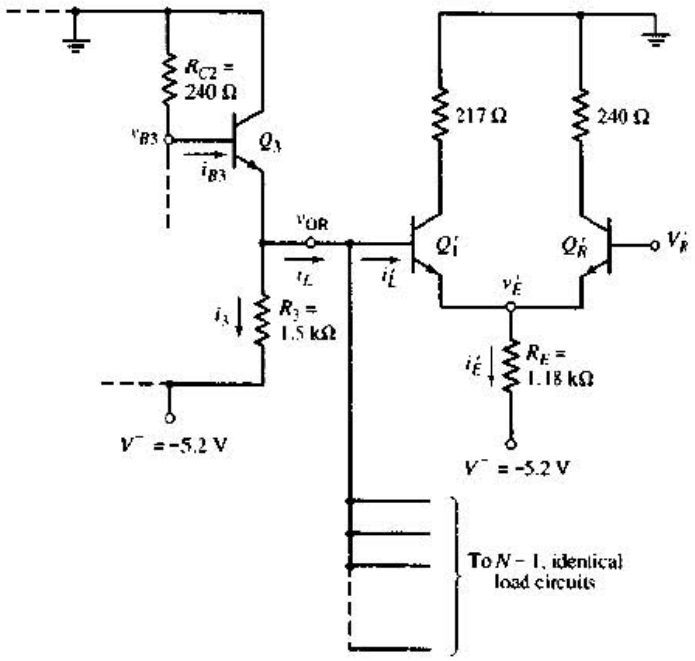


Figure 17.6 Output stage of ECL logic gate driving N identical ECL input stages

---

Example 17.5 **Objective:** Calculate the maximum fanout of an ECL logic gate, based on dc loading effects.

Consider the circuit in Figure 17.6. Assume the current gain of the transistors is $\beta = 50$, which represents a worst-case scenario. Assume that the logic 1 level at the OR output is allowed to decrease by 50 mV at most from a value of −0.70 V to −0.75 V.

Solution: From the figure, we see that

$$i_E' = \frac{v_{OR} - V_{BE}(\text{on}) - V^-}{R_E} = \frac{-0.75 - 0.7 - (-5.2)}{1.18} = 3.18\,\text{mA}$$

The input base current to the load transistor is

$$i_B' = \frac{i_E'}{(1+\beta)} = \frac{3.18}{51} \Rightarrow 62.4\,\mu\text{A} = i_L'$$

The total load current is therefore $i_L = Ni_L'$.

The base current i_{B3} required to produce both the load current i_L and current i_3 is

$$i_{B3} = \frac{i_3 + i_L}{(1+\beta)} = \frac{0 - v_{B3}}{R_{C2}} = \frac{0 - (v_{OR} + V_{BE}(\text{on}))}{R_{C2}} \tag{17.4}$$

Also, from the figure we see that

$$i_3 = \frac{v_{OR} - V^-}{R_3} = \frac{-0.75 - (-5.2)}{1.5} = 2.97\,\text{mA}$$

From Equation (17.4), the maximum fanout for this condition is

$$\frac{2.97 + N(0.0624)}{51} = \frac{0 - (-0.75 + 0.7)}{0.24}$$

which yields $N = 122$.

Comment: This maximum fanout is based on dc conditions and is unrealistic. In practice, the maximum fanout for ECL circuits is determined by the propagation delay time. Each load circuit increases the load capacitance by approximately 3 pF. A maximum fanout of about 15 is usually recommended to keep the propagation delay time within specified limits.

The Negative Supply Voltage

In classic ECL circuits, it is common practice to ground the positive terminal of the supply voltage, reducing the noise signals at the output terminal. Figure 17.7(a) shows an emitter-follower output stage with the supply voltage V_{CC} in series with a noise source V_n. The noise signal may be induced by the effect of switching currents interacting with parasitic inductances and capacitances. The output voltage is measured with respect to ground; therefore, if the positive terminal of V_{CC} is grounded, voltage V_o is taken as the output voltage. If the negative terminal of V_{CC} is at ground, then V_o' is the output voltage.

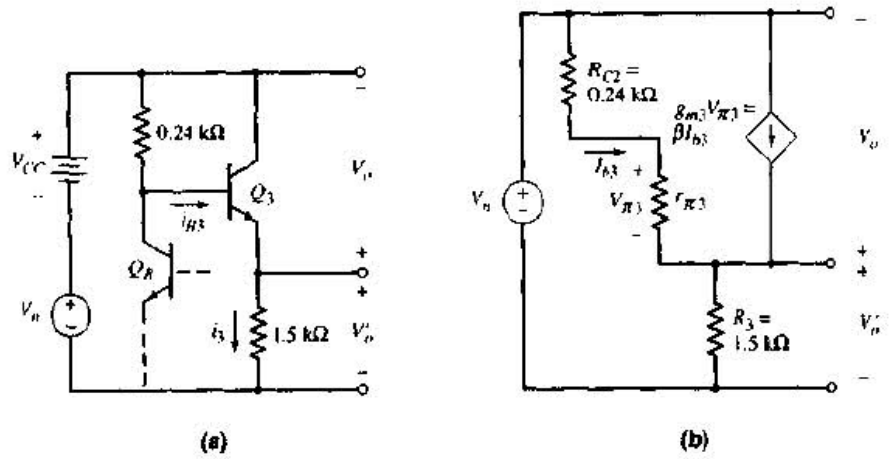


Figure 17.7 (a) Equivalent circuit, ECL emitter-follower output stage and noise generator, and the (b) small-signal hybrid-π equivalent circuit

To determine the effect of the noise voltage at the output, we assume that Q_R is cut off, and we evaluate the small-signal hybrid-π equivalent circuit shown in Figure 17.7(b).

Example 17.6 **Objective:** Determine the effect of a noise signal on the output of an ECL gate.

Consider the small-signal equivalent circuit in Figure 17.7(b). Let $\beta = 100$. Find V_o and V_o' as a function of V_n.

Solution: From a previous analysis, the quiescent collector current in Q_3 for Q_R in cutoff is 3 mA. Then,

$$r_{\pi 3} = \frac{\beta V_T}{I_{CQ}} = \frac{(100)(0.026)}{3} = 0.867\,\text{k}\Omega$$

and

$$g_{m3} = \frac{I_{CQ}}{V_T} = \frac{3}{0.026} = 115\,\text{mA/V}$$

We can also write that

$$V_n = I_{b3}(R_{C2} + r_{\pi 3}) + (1 + \beta)I_{b3}R_3$$

which yields

$$I_{b3} = \frac{V_n}{R_{C2} + r_{\pi 3} + (1 + \beta)R_3} = \frac{V_n}{0.24 + 0.867 + (101)(1.5)} = \frac{V_n}{152.6}$$

The output voltage V_o is

$$V_o = -I_{b3}(R_{C2} + r_{\pi 3}) = -\left(\frac{V_n}{152.6}\right)(0.24 + 0.867) = -0.0073V_n$$

and output voltage V_o' is

$$V_o' = (1 + \beta)I_{b3}R_3 = (101)\left(\frac{V_n}{152.6}\right)(1.5) = 0.99V_n$$

Comment: The effect of noise on the collector–emitter output voltage V_o is much less than on output voltage V_o'. It is advantageous, then, to use V_o, which implies that the positive terminal of V_{CC} is grounded. The noise insensitivity gained with a negative power supply may be critical in a logic circuit with a low noise margin.

17.1.4 Voltage Transfer Characteristics

The voltage transfer curve indicates the circuit characterisics during transition between the two logic states. The voltage transfer characteristics can also be used to determine the noise margins.

DC Analysis

A good approximation of the voltage transfer characteristics can be derived from the piecewise linear model of the two input transistors and the reference transistor. Consider the ECL gate in Figure 17.5. If inputs v_X and v_Y are a logic 0, or $-1.40\,\text{V}$, then Q_1 and Q_2 are cut off and $v_{\text{NOR}} = -0.7\,\text{V}$. The reference transistor Q_R is on and, as previously seen, $i_E = i_{C2} = 2.92\,\text{mA}$, $v_{B3} = -0.70\,\text{V}$, and $v_{\text{OR}} = -1.40\,\text{V}$. As long as $v_X = v_Y$ remains less than $V_R - 0.12 = -1.17\,\text{V}$, the output voltages do not change from these values. During the interval when the inputs are within 120 mV of reference voltage V_R, the output voltage levels vary.

When $v_X = v_Y = V_R + 0.12 = -0.93\,\text{V}$, then Q_1 and Q_2 are on and Q_R is off. At this point, $i_E = i_{C1} = 3.03\,\text{mA}$, $v_{B4} = -0.657\,\text{V}$, and $v_{\text{NOR}} = -1.36\,\text{V}$. As determined previously, when $v_X = v_Y = -0.7\,\text{V}$, $v_{\text{NOR}} = -1.40\,\text{V}$. The voltage transfer curves are shown in Figure 17.8.

Noise Margin

For the ECL gate, we define the threshold logic levels V_{IL} and V_{IH} as the points of discontinuity in the voltage transfer curves. These values are $V_{IL} = -1.17\,\text{V}$

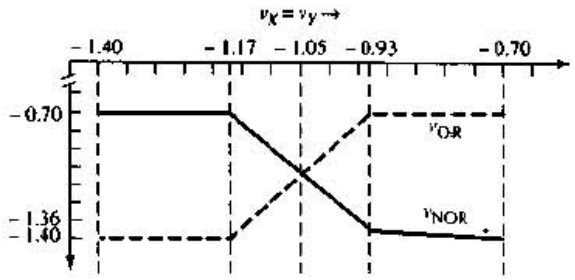


Figure 17.8 ECL OR/NOR logic gate voltage transfer characteristics

and $V_{IH} = -0.93\,\text{V}$. The high logic level is $V_{OH} = -0.7\,\text{V}$ and the low logic value is $V_{OL} = -1.40\,\text{V}$.

The noise margins are defined as

$$\text{NM}_H = V_{OH} - V_{IH} \tag{17.5(a)}$$

and

$$\text{NM}_L = V_{IL} - V_{OL} \tag{17.5(b)}$$

Using the results from Figure 17.8, we find that $\text{NM}_H = 0.23\,\text{V}$ and $\text{NM}_L = 0.23\,\text{V}$. The noise margins for the ECL circuit are considerably lower than those calculated for NMOS and CMOS circuits.

Test Your Understanding

17.5 Consider the ECL circuit in Figure 17.4. Using the results of Example 17.2, plot the voltage transfer characteristics for $-1.40 \leq v_x = v_y \leq -0.7\,\text{V}$. Find the noise margins NM_H and NM_L. (Ans. $\text{NM}_H = 0.23\,\text{V}$, $\text{NM}_L = 0.23\,\text{V}$)

17.2 MODIFIED ECL CIRCUIT CONFIGURATIONS

The large power dissipation in the basic ECL logic gate makes this circuit impractical for large-scale integrated circuits. Certain modifications can simplify the circuit design and decrease the power consumption, making the ECL more compatible with integrated circuits.

17.2.1 Low-Power ECL

Figure 17.9(a) shows a basic ECL OR/NOR logic gate with reference voltage V_R and a positive voltage supply. We can make the output voltage states compatible with the input voltages, eliminating the need for the emitter-follower output stages. In some applications, both complementary outputs may not be required. If, for example, only the OR output is required, then we can eliminate resistor R_{C1}. Removing this resistor does not reduce the circuit power consumption, but it eliminates one element.

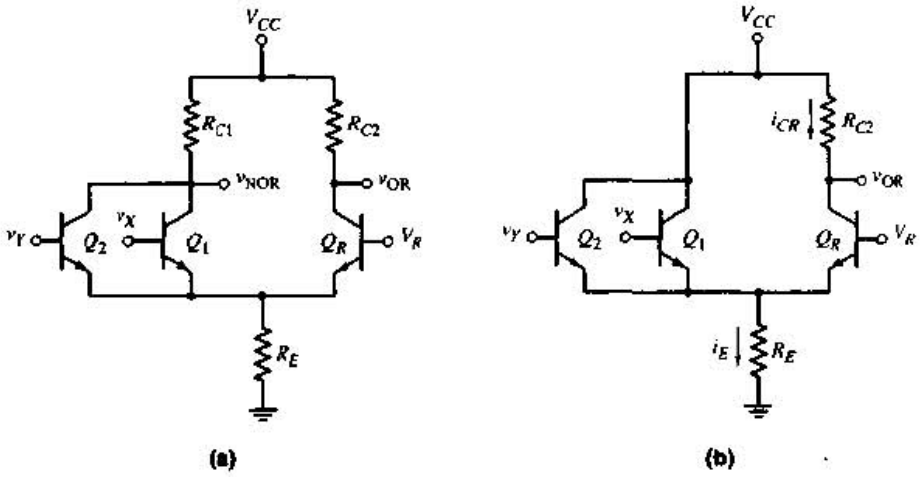


Figure 17.9 (a) Basic ECL OR/NOR logic gate and (b) modified ECL logic gate

Figure 17.9(b) shows the modified ECL gate. For $v_x = v_y$ logic $1 > V_R$, transistors Q_1 and Q_2 are turned on and Q_R is off. The output voltage is $v_{OR} = V_{CC}$. For $v_x = v_y$ = logic $0 < V_R$, then Q_1 and Q_2 are off and Q_R is on. The currents are

$$i_E = \frac{V_R - V_{BE}(\text{on})}{R_E} \cong i_{CR} \tag{17.6}$$

and the output voltage is

$$v_{OR} = V_{CC} - i_{CR}R_{C2} \tag{17.7}$$

If the resistance values of R_E and R_{C2} vary from one circuit to another because of fabrication tolerances, then current i_E and the logic 0 output voltage will vary from one circuit to another.

To establish a well-defined logic 0 output, we can insert a Schottky diode in parallel with resistor R_C, as shown in Figure 17.10. If the two inputs are a logic 0, then Q_1 and Q_2 are off and Q_R is on. For this condition, we want the Schottky diode to turn on. The output will then be $v_{OR} = V_{CC} - V_\gamma$, where

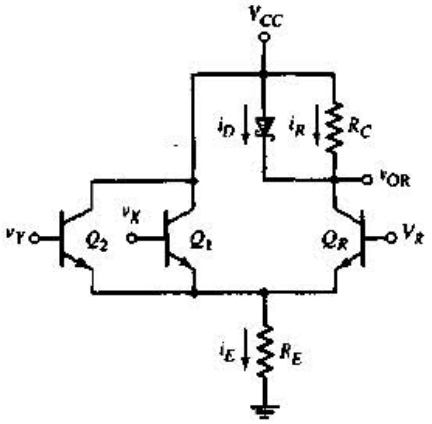


Figure 17.10 Modified ECL logic gate with Schottky diode

V_γ is the turn-on voltage of the Schottky diode. This logic 0 output voltage is a well-defined value. If the diode turns on, then current i_R is limited to $i_R(\text{max}) = V_\gamma / R_C$. Since we must have $i_E > i_R(\text{max})$, the diode current is $i_D = i_E - i_R(\text{max})$.

Example 17.7 **Objective:** Analyze the modified ECL logic gate.

Consider the circuit in Figure 17.10 with parameters $V_{CC} = 1.7\,\text{V}$ and $R_E = R_C = 8\,\text{k}\Omega$. Assume the diode and transistor piecewise linear parameters are $V_\gamma = 0.4\,\text{V}$ and $V_{BE}(\text{on}) = 0.7\,\text{V}$.

Solution: The output voltage values are

$$v_{OR} = \text{logic 1} = V_{CC} = 1.7\,\text{V}$$

and

$$v_{OR} = \text{logic 0} = V_{CC} - V_\gamma = 1.7 - 0.4 = 1.3\,\text{V}$$

For the output voltages to be compatible with the inputs, the reference voltage V_R must be the average of the logic 1 and logic 0 values, or $V_R = 1.5\,\text{V}$. If $v_x = v_y = \text{logic 0} = 1.3\,\text{V}$, then Q_R is on. Therefore,

$$i_E = \frac{V_R - V_{BE}(\text{on})}{R_E} = \frac{1.5 - 0.7}{8} \Rightarrow 100\,\mu\text{A}$$

The maximum current in R_C is

$$i_R(\text{max}) = \frac{V_\gamma}{R_C} = \frac{0.4}{8} \Rightarrow 50\,\mu\text{A}$$

and the current through the diode is

$$i_D = i_E - i_R(\text{max}) = 100 - 50 = 50\,\mu\text{A}$$

For $v_x = v_y = \text{logic 0}$, the power dissipation is $P = i_E V_{CC}$, or

$$P = i_E V_{CC} = (100)(1.7) = 170\,\mu\text{W}$$

For $v_x = v_y = \text{logic 1} = 1.7\,\text{V}$, we have

$$i_E = \frac{v_x - V_{BE}(\text{on})}{R_E} = \frac{1.7 - 0.7}{8} \Rightarrow 125\,\mu\text{A}$$

Therefore, the power dissipation for this condition is

$$P = i_E V_{CC} = (125)(1.7) = 213\,\mu\text{W}$$

Comment: If the resistance values of R_E and R_C were to change by as much as ± 20 percent as a result of manufacturing tolerances, for example, the currents would still be sufficient to turn the Schottky diode on when Q_R is on. This means that the logic 0 output is well defined. Also, the power dissipation in this ECL gate is considerably less than that in the classic ECL OR/NOR logic circuit. The reduced power is a result of fewer components, lower bias voltage, and smaller currents.

When transistor Q_R is off, its collector voltage is 1.7 V and the B–C junction is reverse biased by 0.2 V. When Q_R is conducting, its collector voltage is 1.3 V, the B–C junction is forward biased by 0.2 V, and the transistor is biased slightly in saturation. However, this slight saturation bias does not degrade the switching of Q_R, so the fast-switching characteristic of the ECL circuit is retained.

Test Your Understanding

D17.6 Design the basic ECL logic gate in Figure 17.11 such that the maximum power dissipation is 0.2 mW and the logic swing is 0.4 V. (Ans. $I_Q = 118\,\mu A$, $R_C = 3.39\,k\Omega$, $V_R = 1.5\,V$)

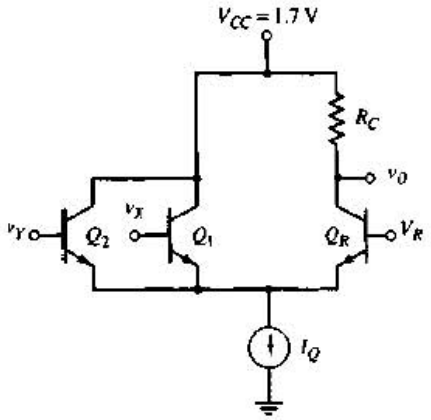


Figure 17.11 Figure for Exercise 17.6

17.2.2 Alternative ECL Gates

In an ECL system, as in all digital systems, a gate is used to drive other logic gates. Connecting load circuits to the basic ECL gate demonstrates changes that can be made to incorporate ECL into integrated circuits more effectively.

Figure 17.12 shows the basic ECL gate with two load circuits. In this configuration, the collectors of Q_2' and Q_2'' are at the same potential, as are the bases of the two transistors. We can therefore replace Q_2' and Q_2'' by a single multiemitter transistor.

In Figure 17.13, the multiemitter transistor Q_O is part of the driver circuit. The operation of the circuit is as follows:

- $v_x = v_y =$ logic 1 $= 1.7\,V$: The two input transistors Q_1 and Q_2 are on, Q_R is off, and $v_O = 1.7\,V$. Since the base voltage of Q_O is higher than the base voltages of Q_R' and Q_R'', then Q_O is conducting, Q_R' and Q_R'' are off, and $v_E' = v_E'' = 1.7 - 0.7 = 1.0\,V$. The currents i_E' and i_E'' flow through the emitters of Q_O.The output voltages are $v_O' = v_O'' = 1.7\,V$.
- $v_x = v_y =$ logic 0 $= 1.3\,V$: For this case, the two input transistors Q_1 and Q_2 are off, Q_R is on, and $v_O = 1.3\,V$. The output transistor Q_O is off and both Q_R' and Q_R'' are on. The output voltages are then $v_O' = v_O'' = 1.3\,V$.

The two load circuits in Figure 17.13 each have only a single input, which limits the circuit functionality. The versatility of the circuit can be further enhanced by making the load transistor Q_R' a multiemitter transistor. This is shown in Figure 17.14. For simplicity, we show only a single input transistor to each of the two driver circuits. The operation of this circuit for various combinations of input voltages is as follows.

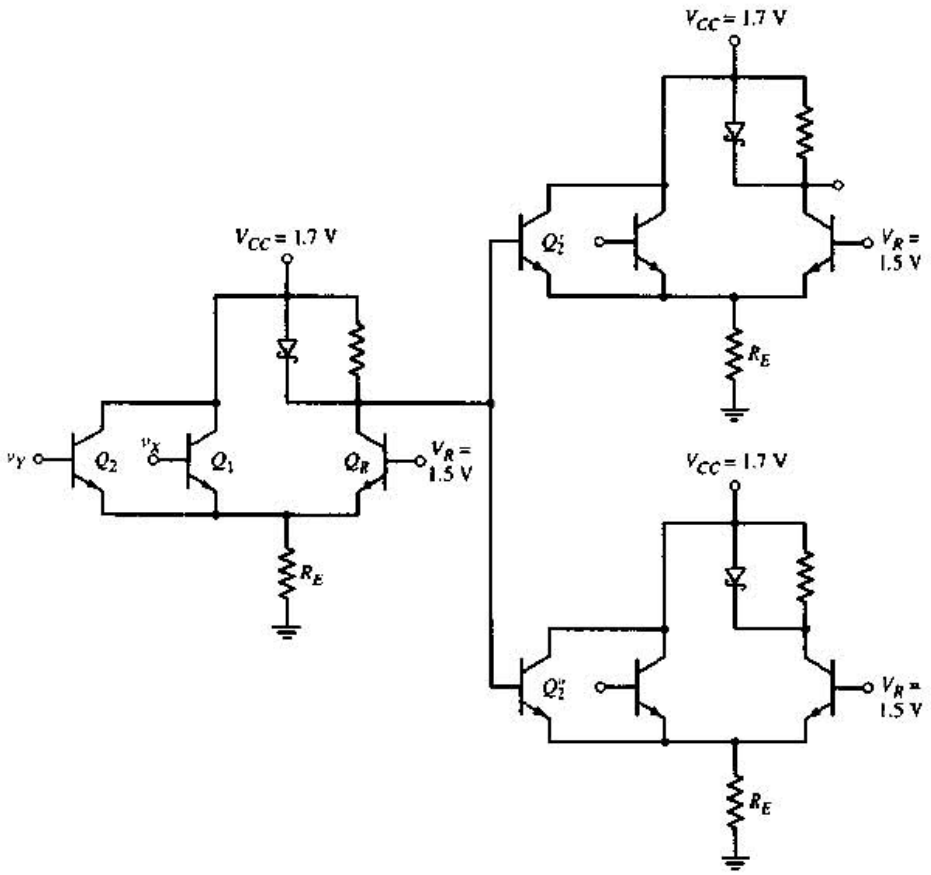


Figure 17.12 Modified ECL logic gate with two load circuits

- $v_1 = v_2 =$ logic 0 = 1.3 V: The two input transistors Q_1 and Q_2 are off and the two reference transistors Q_{R1} and Q_{R2} are on. This means that $v_{O1} = v_{O2} = 1.3$ V and both output transistors Q_{O1} and Q_{O2} are off. Both emitters of Q_R' are forward biased, currents i_{E1} and i_{E2} flow through Q_R', and the output voltage is $v_O' =$ logic 0 = 1.3 V.
- $v_1 = 1.7$ V, $v_2 = 1.3$ V: For this case, Q_1 is on, Q_{R1} is off, Q_2 is off, and Q_{R2} is on. The output voltages are $v_{O1} = 1.7$ V and $v_{O2} = 1.3$ V. This means that Q_{O1} is on and Q_{O2} is off. With Q_{O1} on, current i_{E1} flows through Q_{O1} and no current flows in emitter E_1. With Q_{O2} off, emitter E_2 is forward biased, current i_{E2} flows through Q_R', and the output voltage is $v_O' =$ logic 0 = 1.3 V.
- $v_1 = 1.3$ V, $v_2 = 1.7$ V: This case is the complement of the one just discussed. Here, Q_{O1} is off and Q_{O2} is on. This means that i_{E1} flows through emitter E_1 of Q_R', and i_{E2} flows through Q_{O2}. The output voltage is $v_O' =$ logic 0 = 1.3 V.
- $v_1 = v_2 = 1.7$ V: The two input transistors Q_1 and Q_2 are on, the two reference transistors Q_{R1} and Q_{R2} are off, and $v_{O1} = v_{O2} = 1.7$ V. This means that both Q_{O1} and Q_{O2} are on and Q_R' is off. Currents i_{E1} and i_{E2} flow through Q_{O1} and Q_{O2}, respectively, and the output voltage is $v_O' =$ logic 1 = 1.7 V.

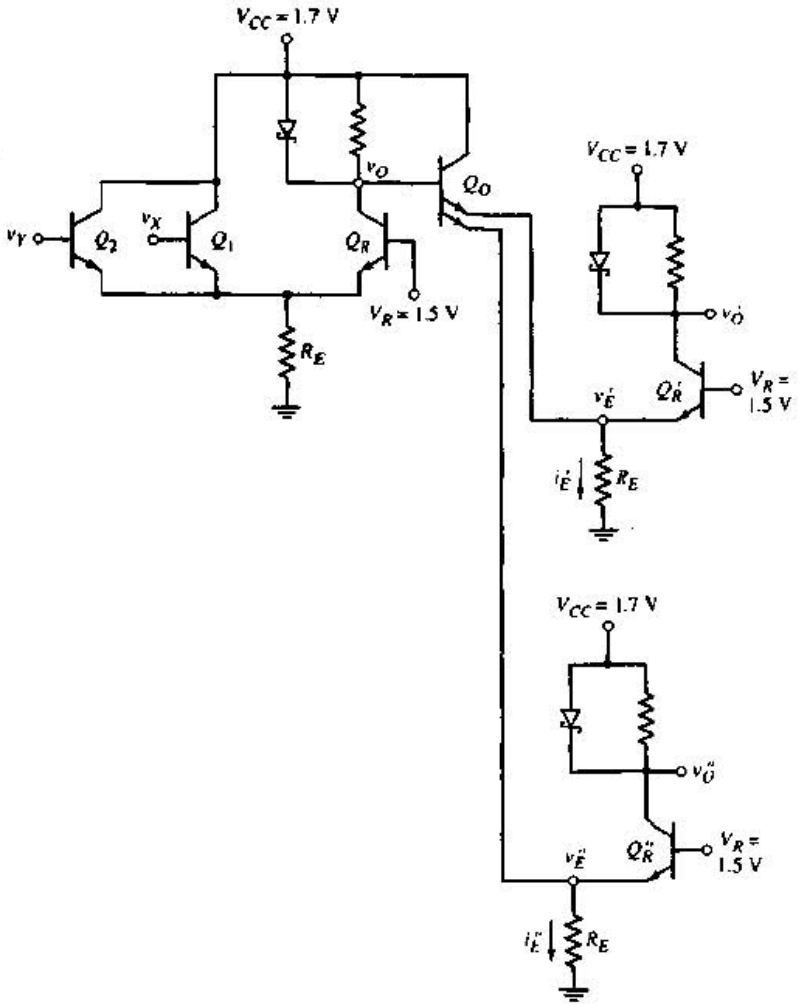


Figure 17.13 Modified ECL logic gate with multiemitter output transistor and two load circuits

These results are summarized in Table 17.1, which shows that this circuit performs the AND logic function. A more complicated or sophisticated logic function can be performed if multiple inputs are used in the driver circuits.

In integrated circuits, resistors R_E are replaced by current sources using transistors. Replacing resistors with transistors in integrated circuits usually results in reduced chip area.

Table 17.1 Summary of results for the ECL circuit in Figure 17.14

v_1(V)	v_2(V)	v_O'(V)
1.3	1.3	1.3
1.7	1.3	1.3
1.3	1.7	1.3
1.7	1.7	1.7

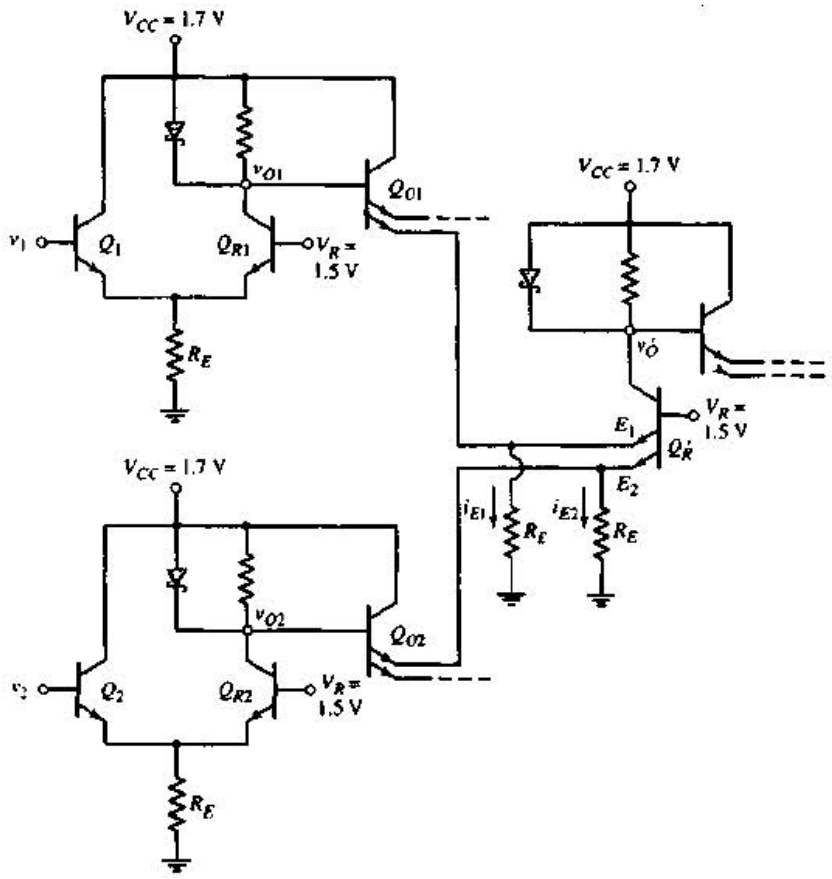


Figure 17.14 Two ECL driver circuits with a multi-input load circuit

17.2.3 Series Gating

Series gating is a bipolar logic circuit technique that allows complex logic functions to be performed with a minimum number of devices and with maximum speed. Series gating is formed by using cascode stages.

Figure 17.15(a) shows the basic emitter-coupled pair, and Figure 17.15(b) shows a cascode stage, also referred to as two-level series gating. Reference voltage V_{R1} is approximately 0.7 V greater than reference voltage V_{R2}. The input voltages v_x and v_y must also be shifted approximately 0.7 V with respect to each other.

As an example, we use the multiemitter load circuit from Figure 17.14 as part of a cascode configuration as shown in Figure 17.16. Transistors Q_{O1}, Q_{O2}, and Q_{O3} represent the output transistors of three ECL driver circuits. We assume a logic 1 level of 2.5 V and a logic 0 level of 2.1 V. The 0.4 V logic swing results from incorporating a Schottky diode in each output stage.

With three input signals, there are eight possible combinations of input states. We will only consider two combinations here:

- $A = B = C$ = logic 0 = 2.1 V: In this case, transistors Q_{O1} and Q_{O2} are off and transistor Q_1 is off. This means that current I_Q flows through Q_2 and Q_R, and v_O = logic 0 = 2.1 V.

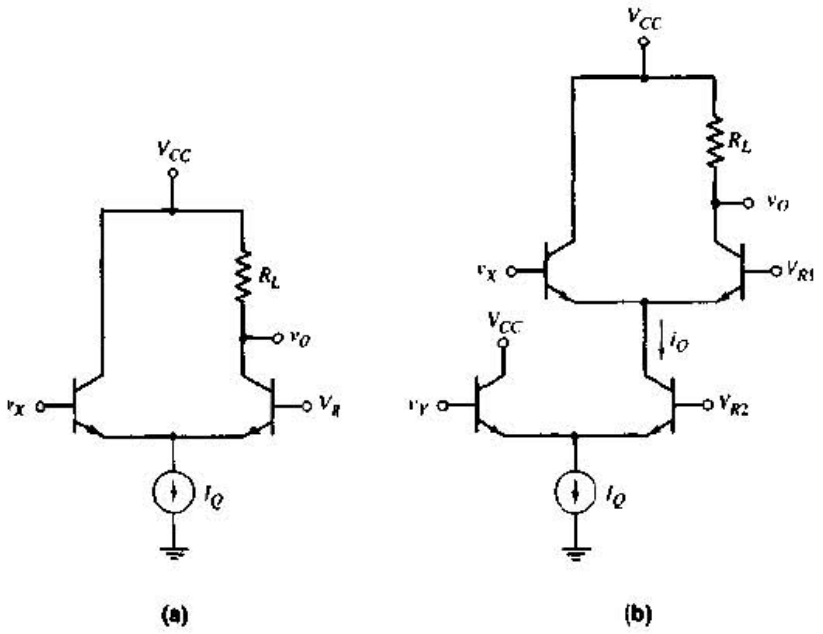


Figure 17.15 (a) Basic emitter-coupled pair and (b) ECL cascode configuration

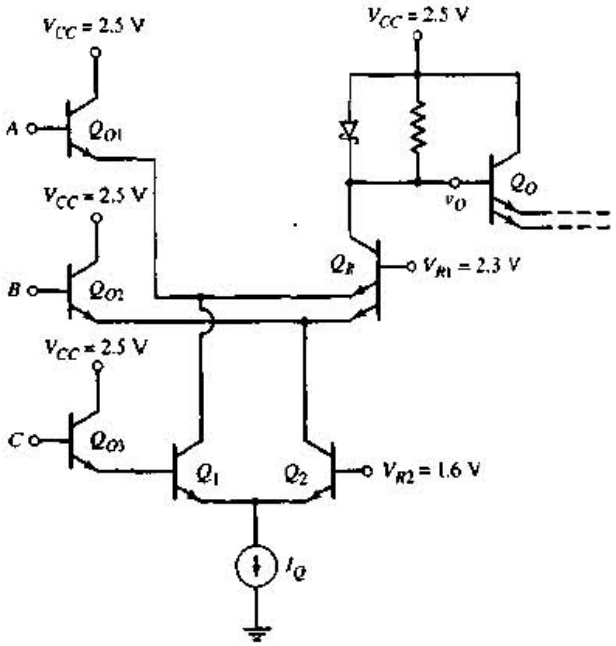


Figure 17.16 ECL series gating example

- $A = C = 2.1\,\text{V}$, $B = 2.5\,\text{V}$: Transistors Q_{O1} and Q_1 are off, Q_{O2} is on, and current I_Q flows through Q_2 and Q_{O2}. Since Q_1 is off, no current is available to flow through Q_R, even though Q_{O1} is off. The output is v_O = logic 1 = 2.5 V.

For the output voltage v_O to be a logic 1, no current must flow through Q_R. This occurs when both Q_{O1} and Q_{O2} are on, or when a B–E junction of Q_R is

turned on but no current is available through Q_1 or Q_2. We can show that this circuit performs the logic function

$$(A \text{ AND } C) \text{ OR } (B \text{ AND } \overline{C}) \tag{17.8}$$

We are now beginning to integrate logic functions into a circuit rather than using separate, distinct logic gates. This reduces the number of devices required, as well as the propagation delay time.

Another example of series gating is shown in Figure 17.17. A negative supply voltage is again used. The operation of the circuit is as follows.

- $v_x = v_y =$ logic $0 = -0.4$ V: Transistors Q_1, Q_4, and Q_7 are on, current I_Q flows through Q_7 and Q_4, the diode turns on, and the output voltage is -0.4 V.
- $v_x = -0.4$ V, $v_y = 0$: Transistors Q_1, Q_4, and Q_6 are on, current I_Q flows through Q_6 and Q_1 to ground, and current I_{Q2} flows through Q_4 and the resistor. The output voltage is $v_O = -R_C I_{Q2} = -(1)(0.05) = -0.05$ V. This voltage is not sufficient to turn the Schottky diode on. Although it is not zero volts, the voltage still represents a logic 1.
- $v_x = 0$, $v_y = -0.4$ V: Transistors Q_2, Q_3, and Q_7 are on, current I_Q flows through Q_7 and Q_3 to ground, and current I_{Q1} flows through Q_2 and the resistor. Again, $v_O = -0.05$ V = logic 1.

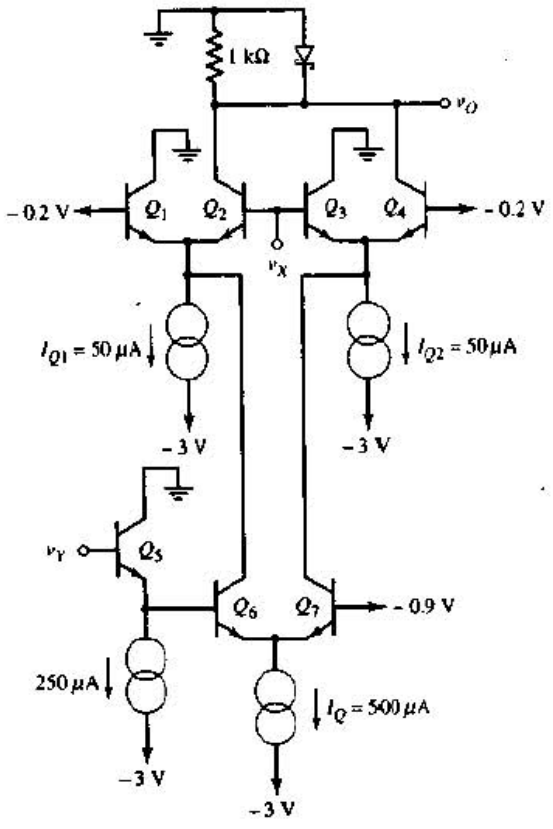


Figure 17.17 ECL series gating example

- $v_x = v_y$ = logic 1 $\cong$ 0 V: Transistors Q_2, Q_3, and Q_6 are on, I_Q flows through Q_6, Q_2, and the Schottky diode, and output voltage is $v_O = -0.4\,\text{V}$ = logic 0.

These results are summarized in Table 17.2, in which the logic levels are given. The results show that the circuit performs the exclusive-OR logic function.

Table 17.2 Summary of logic levels for ECL circuit in Figure 17.17

v_x	v_y	v_O
0	0	0
0	1	1
1	0	1
1	1	0

17.2.4 Propagation Delay Time

ECL is the fastest bipolar logic technology. Bipolar technology can produce small, very fast transistors with cutoff frequencies in the range of 3 to 15 GHz. Logic gates that use these transistors are so fast that interconnect line delays tend to dominate the propagation delay times. Minimizing these interconnect delays involves minimizing the metal lengths and using sufficient current drive capability.

Speed is derived from low-signal logic swings, nonsaturating logic, and the ability to drive a load capacitance. Figure 17.18 is the emitter-follower output stage found in many ECL circuits, showing an effective load capacitance. Usually, the emitter-follower current I_Q is two to four times larger than the cell current.

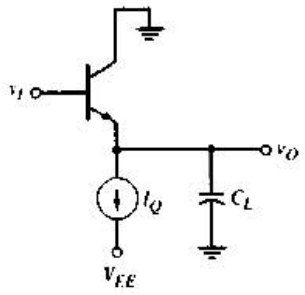


Figure 17.18 Emitter-follower stage with load capacitance

In the pull-down cycle, the current I_Q discharges C_L. The current–voltage relationship of the capacitor is

$$i = C_L \frac{dv_O}{dt} \tag{17.9(a)}$$

or

$$v_O = \frac{1}{C_L} \int i\,dt \tag{17.9(b)}$$

Assuming C_L and $i = I_Q$ are constants, the fall time is

$$\tau_F = (0.8)\frac{C_L V_S}{I_Q} \tag{17.10}$$

where V_S is the logic swing, and the factor (0.8) occurs because τ_F is defined as the time required for the output to swing from 10 percent to 90 percent of its final value.

As an example, if $V_S = 0.4\,\text{V}$ and $I_Q = 250\,\mu\text{A}$, then for a minimum fall time of $\tau_F = 0.8\,\text{ns}$, the maximum load capacitance is $C_L(\text{max}) = 0.625\,\text{pF}$. This calculation shows that the load capacitance must be minimized to realize short propagation delay times.

Test Your Understanding

17.7 Consider the ECL circuit in Figure 17.16. For each of the eight possible combinations of input states, determine the conduction state (on or off) of each transistor. Verify that this circuit performs the logic function given by Equation (17.8).

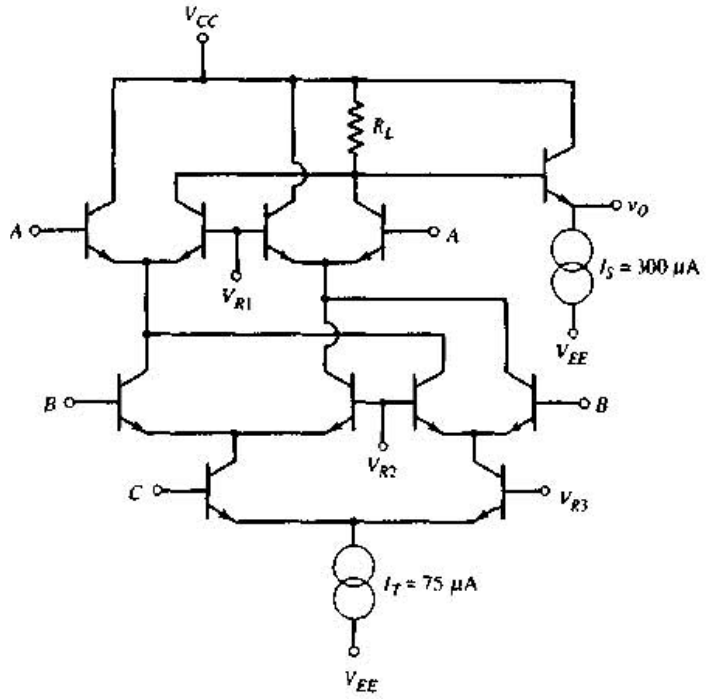


Figure 17.19 Figure for Exercise 17.8

17.8 The ECL circuit in Figure 17.19 is an example of three-level series gating. Determine the logic function that the circuit performs. (Ans. $(A \oplus B) \oplus C$)

17.3 TRANSISTOR–TRANSISTOR LOGIC

The bipolar inverter is the basic circuit from which most bipolar saturated logic circuits are developed, including diode–transistor logic (DTL) and transistor–transistor logic (TTL). However, the basic bipolar inverter suffers from loading effects. Diode–transistor logic combines diode logic (Chapter 2) and the bipolar inverter to minimize loading effects. Transistor–transistor logic, which evolved directly from DTL, provides reduced propagation delay times, as we will show.

In DTL and TTL circuits, bipolar transistors are driven between cutoff and saturation. Since the transistor is being used essentially as a switch, the current gain is not as important as in amplifier circuits. Typically, for transistors used in these circuits, the current gain is assumed to be in the range of 25 to 50. These transistors need not be fabricated to as tight a tolerance as that of high-gain amplifier transistors.

Table 17.3 lists the piecewise linear parameters used in the analysis of bipolar digital circuits, along with their typical values. Also included is the pn junction diode turn-on voltage V_γ. Generally, the B–E voltage increases as the transistor is driven into saturation, since the base current increases. When the transistor is biased in the saturation region, the B–E voltage is $V_{BE}(\text{sat})$, where $V_{BE}(\text{sat}) > V_{BE}(\text{on})$.

Table 17.3 Piecewise linear parameters for a pn junction diode and npn bipolar transistor

Parameter	Value
V_γ	0.7 V
$V_{BE}(\text{on})$	0.7 V
$V_{BE}(\text{sat})$	0.8 V
$V_{CE}(\text{sat})$	0.1 V

17.3.1 Basic Diode–Transistor Logic Gate

The basic diode–transistor logic (DTL) gate is shown in Figure 17.20. The circuit is designed such that the output transistor operates between cutoff and saturation. This provides the maximum output voltage swing, minimizes loading effects, and produces the maximum noise margins. When Q_o is in saturation, the output voltage is $v_O = V_{CE}(\text{sat}) \cong 0.1\,\text{V}$ and is defined as logic 0 for the DTL circuit. As we will see, the basic DTL logic gate shown in Figure 17.20 performs the NAND logic function.

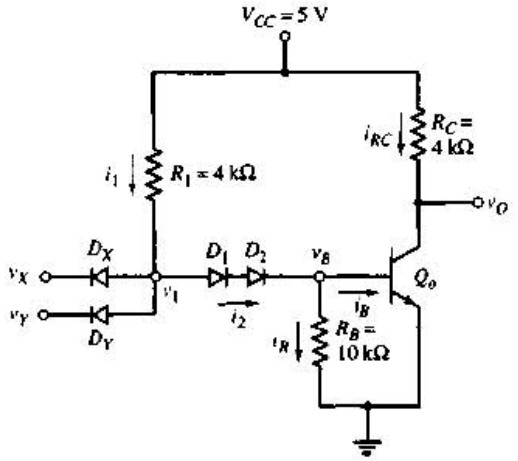


Figure 17.20 Basic diode–transistor logic gate

Basic DTL NAND Circuit Operation

If both input signals v_X and v_Y are at logic 0, then the two input diodes D_X and D_Y are forward biased through resistor R_1 and voltage source V_{CC}. The input diodes conduct, and voltage v_1 is clamped to a value that is one diode drop above the input voltage. If $v_X = v_Y = 0.1\,\text{V}$ and $V_\gamma = 0.7\,\text{V}$, then $v_1 = 0.8\,\text{V}$. Diodes D_1 and D_2 and output transistor Q_o are nonconducting and are off. If D_1 and D_2 were conducting, then voltage v_B would be $-0.6\,\text{V}$ for $V_\gamma = 0.7\,\text{V}$. However, no mechanism exists for v_B to become negative and still have a forward-biased diode current. Thus, the current in D_1 and D_2, the current in Q_o, and the voltage v_B are all zero. Since Q_o is cut off, then the output voltage is $v_O = V_{CC}$. This is the largest possible output voltage and is therefore defined as the logic 1 level. This same condition applies as long as at least one input is at logic 0.

When both v_X and v_Y are at logic 1, which is equal to V_{CC}, both D_X and D_Y are cut off. Diodes D_1 and D_2 become forward biased, output transistor Q_o is driven into saturation, and $v_O = V_{CE}(\text{sat})$, which is the smallest possible output voltage and is defined as the logic 0 level.

This circuit is a two-input DTL NAND logic gate. However, the circuit is not limited to two inputs. Additional input diodes may be included to increase the fan-in.

Example 17.8 **Objective:** Determine the currents and voltages in the DTL logic circuit.

Consider the DTL circuit in Figure 17.20. Assume the transistor parameters are as given in Table 17.3 and let $\beta = 25$.

Solution: Let $v_X = v_Y =$ logic $0 = 0.1\,\text{V}$. For this case,

$$v_1 = v_X + V_\gamma = 0.1 + 0.7 = 0.8\,\text{V}$$

and

$$i_1 = \frac{V_{CC} - v_1}{R_1} = \frac{5 - 0.8}{4} = 1.05\,\text{mA}$$

Since diodes D_1 and D_2 and output transistor Q_o are nonconducting, we assume that current i_1 divides evenly between the matched diodes D_X and D_Y. In this case, the currents $i_2 = i_B = i_C = 0$ and the output voltage is $v_O = 5\,\text{V} =$ logic 1.

If $v_X = 0.1\,\text{V}$ and $v_Y = 5\,\text{V}$, or $v_X = 5\,\text{V}$ and $v_Y = 0.1\,\text{V}$, then the output transistor is still cut off and $v_O = 5\,\text{V} =$ logic 1.

If $v_X = v_Y =$ logic $1 = 5\,\text{V}$, it is impossible for input diodes D_X and D_Y to be forward biased. In this case, diodes D_1 and D_2 and the output transistor are biased on, which means that, starting at ground potential at the emitter of Q_o, v_1 is

$$v_1 = V_{BE}(\text{sat}) + 2V_\gamma = 0.8 + 2(0.7) = 2.2\,\text{V}$$

Voltage v_1 is clamped at this value and cannot increase. We see that D_X and D_Y are indeed reverse biased and turned off, as assumed.

Currents i_1 and i_2 are

$$i_1 = i_2 = \frac{V_{CC} - v_1}{R_1} = \frac{5 - 2.2}{4} = 0.70\,\text{mA}$$

and current i_R is

$$i_R = \frac{V_{BE}(\text{sat})}{R_B} = \frac{0.8}{10} = 0.08\,\text{mA}$$

The base current into the output transistor is then

$$i_B = i_2 - i_R = 0.70 - 0.08 = 0.62\,\text{mA}$$

Since the circuit is to be designed such that Q_o is driven into saturation, the collector current is

$$i_C = \frac{V_{CC} - V_{CE}(\text{sat})}{R_C} = \frac{5 - 0.1}{4} = 1.23\,\text{mA}$$

Finally, the ratio of collector to base current is

$$\frac{i_C}{i_B} = \frac{1.23}{0.62} = 1.98 < \beta$$

Comment: Since the ratio of the collector current to base current is less than β, the output transistor is biased in the saturation region. Since the output transistor is biased between cutoff and saturation, the maximum swing between logic 0 and logic 1 is obtained.

Test Your Understanding

[Note: In the following exercises, assume the piecewise linear transistor parameters are as listed in Table 17.3.]

17.9 The DTL circuit in Figure 17.20 has new circuit parameters of $R_1 = 6\,k\Omega$, $R_C = 5\,k\Omega$, and $R_B = 15\,k\Omega$. Assume $V_{CC} = 5\,V$ and $\beta = 25$. Determine i_1, i_2, i_R, i_B, i_{RC}, and v_O for: (a) $v_X = v_Y = 0.1\,V$, (b) $v_X = 5\,V$, $v_Y = 0.1\,V$, and (c) $v_X = v_Y = 5\,V$. (Ans. (a) $i_1 = 0.7\,mA$, $i_2 = i_R = i_B = i_{RC} = 0$, $v_O = 5\,V$ (b) same as part (a) (c) $i_1 = i_2 = 0.467\,mA$, $i_R = 0.053\,mA$, $i_B = 0.414\,mA$, $i_{RC} = 0.98\,mA$, $v_O = 0.1\,V$)

17.10 Consider the basic DTL circuit in Figure 17.20 with circuit and transistor parameters given in Example 17.8. Assume no load is connected to the output. Calculate the power dissipated in the circuit for (a) $v_X = v_Y = 5\,V$ and (b) $v_X = v_Y = 0$.

Minimum β

To ensure that the output transistor is in saturation, the common-emitter current gain β must be at least as large as the ratio of collector current to base current. For example 17.8, the minimum β, or β_{min}, is 1.98. If the common-emitter current gain were less than 1.98, then Q_o would not be driven into saturation, and the currents and voltages in the circuit would have to be recalculated. A current gain greater than 1.98 ensures that Q_o is driven into saturation for the given circuit parameters and for the no-load condition.

Pull-Down Resistor

In the basic DTL NAND logic circuit in Figure 17.20, a resistor R_B is connected between the base of the output transistor and ground. This resistor is called a pull-down resistor, and its purpose is to decrease the output transistor switching time as it goes from saturation to cutoff. As previously discussed, excess minority carriers must be removed from the base before a transistor can be switched to cutoff. This base charge removal produces a current out of the transistor base terminal until the transistor is turned off. Without the pull-down resistor, this reverse base current would be limited to the reverse-bias leakage current in diodes D_1 and D_2, resulting in a relatively long turn-off time. The pull-down resistor provides a path for the reverse base current.

The base charge can be removed more rapidly if the value of R_B is reduced. The larger the reverse base current, the shorter the transistor turn-off time. However, a trade-off must be made in choosing the value of R_B. A small R_B provides faster switching, but lowers the base current to the transistor in the on state by diverting some drive current to ground. A lower base current reduces the circuit drive capability, or maximum fanout.

17.3.2 The Input Transistor of TTL

Figure 17.21(a) shows a basic DTL circuit with one input diode D_X and one offset diode D_1. The structure of these back-to-back diodes is the same as an npn transistor, as indicated in Figure 17.21(b). The base–emitter junction of Q_1 corresponds to input diode D_X and the base–collector junction corresponds to offset diode D_1.

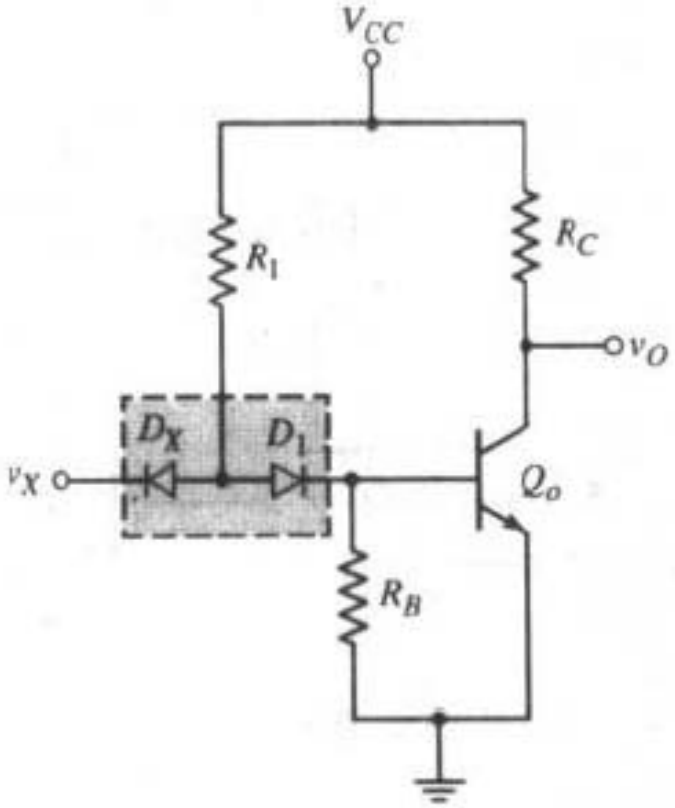
(a) (b)

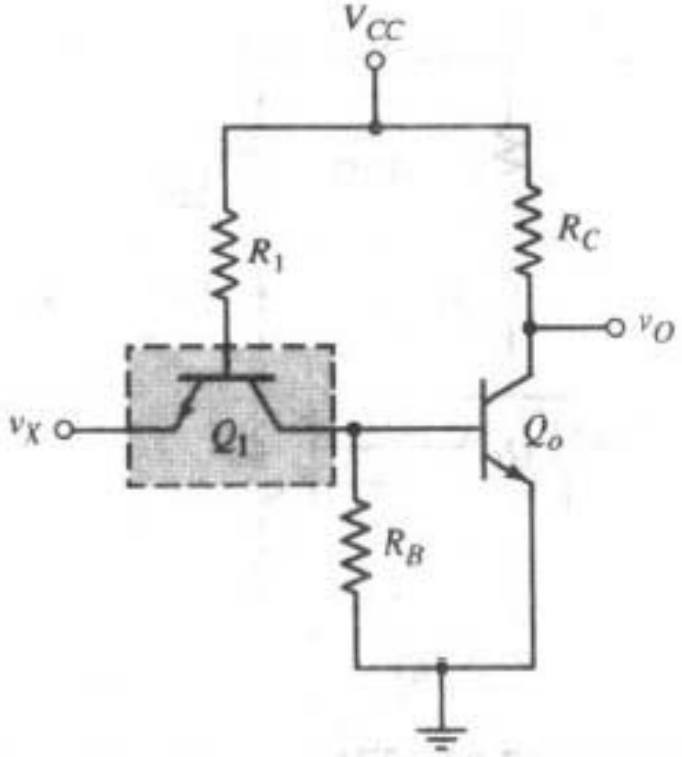
Figure 17.21 (a) Basic DTL gate and (b) basic TTL gate

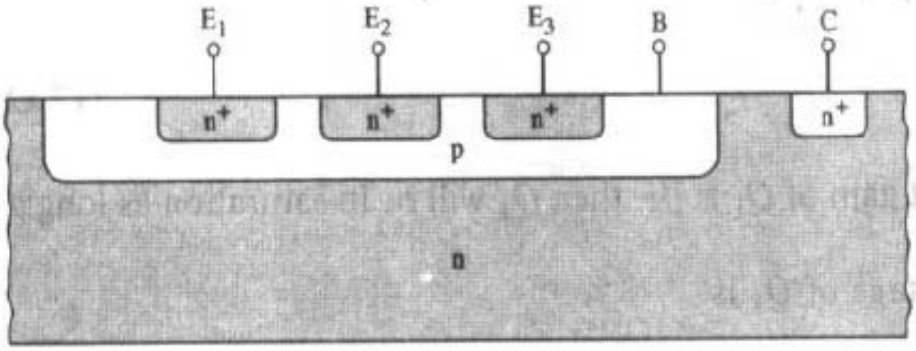
In isoplanar integrated circuit technology, the emitter of a bipolar transistor is fabricated in the base region. More emitters can then be added in the same base region to form a multiemitter, multi-input device. Figure 17.22(a) shows a simplified cross section of a three-emitter transistor, which is used as the input device in a TTL circuit. Figure 17.22(b) shows the basic TTL circuit with the multiemitter input transistor.

Figure 17.22 (a) Simplified cross section of three-emitter transistor and (b) TTL circuit with three-emitter input transistor

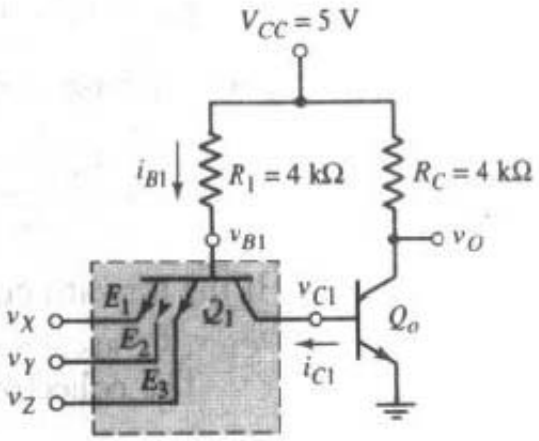
This circuit performs the same NAND operation as its DTL counterpart. The multiemitter transistor reduces the silicon area required, compared to the DTL input diodes, and it increases the switching speed. Transistor Q_1 assists in pulling output transistor Q_o out of saturation and into cutoff during a low-to-high transition of the output voltage. Pull-down resistor R_B in Figure 17.21(b) is no longer necessary, since the excess minority carriers in the base of Q_o use transistor Q_1 as a path to ground.


V_{CC}
R_1
R_C
v_O
D_X
D_1
v_X
Q_o
R_B


V_{CC}
R_1
R_C
v_O
v_X
Q_1
Q_o
R_B


E1
E2
E3
B
C
n+
n+
n+
n+
p
n

(a)


VCC = 5 V
iB1
R1 = 4 kΩ
RC = 4 kΩ
vB1
vO
E1
E2
E3
Q1
vC1
Qo
vX
vY
vZ
iC1

(b)

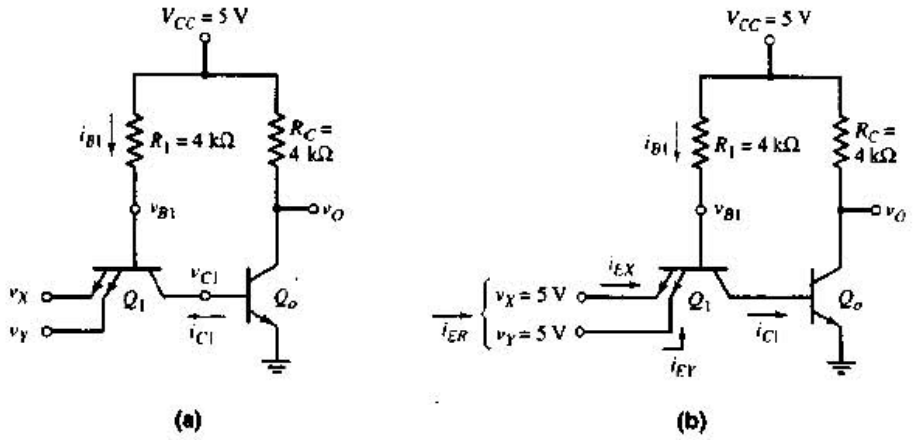


Figure 17.23 TTL circuit (a) with at least one input low and (b) with all inputs high

The operation of input transistor Q_1 is somewhat unconventional. In Figure 17.23(a), if either or both of the two inputs to Q_1 are in a low state, the base–emitter junction is forward biased through R_1 and V_{CC}. The base current enters Q_1, and the emitter current exits the specific emitter connected to the low input. Transistor action forces the collector current into Q_1, but the only steady-state collector current in this direction is a reverse-bias saturation current out of the base of Q_o. The steady-state collector current of Q_1 is usually much smaller than the base current, implying that Q_1 is biased in saturation.

If at least one input is low such that Q_1 is biased in saturation, then from Figure 17.23(a), we see that the base voltage of Q_1 is

$$v_{B1} = v_X + V_{BE}(\text{sat}) \tag{17.11}$$

and the base current into Q_1 is

$$i_{B1} = \frac{V_{CC} - v_{B1}}{R_1} \tag{17.12}$$

If the forward current gain of Q_1 is β_F, then Q_1 will be in saturation as long as $i_{C1} < \beta_F i_{B1}$.

The collector voltage of Q_1 is

$$v_{C1} = v_X + V_{CE}(\text{sat}) \tag{17.13}$$

If both v_X and $V_{CE}(\text{sat})$ are approximately 0.1 V, then v_{C1} is small enough for the output transistor to cut off and $v_O = V_{CC} =$ logic 1.

If all inputs are high, $v_X = v_Y = 5$ V, as shown in Figure 17.23(b), then the base–emitter junctions of the input transistor are reverse biased. Base voltage v_{B1} increases, which forward-biases the B–C junction of Q_1 and drives output transistor Q_o into saturation. Since the B–E junction of Q_1 is reverse biased and the B–C junction is forward biased, Q_1 is biased in the inverse-active mode. In this bias mode, the roles of the emitter and collector are interchanged.

When input transistor Q_1 is biased in the inverse-active mode, base voltage v_{B1} is

$$v_{B1} = V_{BE}(\text{sat})_{Q_o} + V_{BC}(\text{on})_{Q_1} \tag{17.14}$$

where $V_{BC}(\text{on})$ is the B–C junction turn-on voltage. We assume that the B–C junction turn-on voltage is equal to the B–E junction turn-on voltage. The terminal current relationships for Q_1 are therefore

$$i_{EX} = i_{EY} = \beta_R i_{B1} \tag{17.15}$$

and

$$i_{C1} = i_{B1} + i_{EX} + i_{EY} = (1 + 2\beta_R) i_{B1} \tag{17.16}$$

where β_R is the inverse-active mode current gain of each input emitter of the input transistor.

Since a bipolar transistor is not symmetrical, the inverse and forward current gains are not equal. The inverse current gain is generally quite small, usually less than one. In Figure 17.23(b), the input transistor has a fan-in of two. Transistor Q_1 may be considered as two separate transistors with their bases and collectors connected. For simplicity, when all inputs are high, we assume that current i_{ER} splits evenly between the input emitters.

The inverse-active mode current into the emitters of Q_1 is not desirable, since this is a load current that must be supplied by a driver logic circuit when its output voltage is in its high state. Because of the transistor action, these currents tend to be larger than the reverse saturation currents of DTL circuit input diodes. The major advantage of TTL over DTL is faster switching of the output transistor from saturation to cutoff.

If all inputs are initially high and then at least one input switches to the logic 0 state, 0.1 V, the B–E junction of Q_1 becomes forward biased and base voltage v_{B1} becomes approximately $0.1 + 0.7 = 0.8$ V. Collector voltage v_{C1} is held at 0.8 V as long as output transistor Q_o remains in saturation. At this instant in time, Q_1 is biased in the forward-active mode. A large collector current into Q_1 can exist, which pulls the excess minority carrier charge out of the base of Q_o. A large reverse base current from Q_o will very quickly pull the output transistor out of saturation. In the TTL circuit, the action of the input transistor reduces the propagation delay time compared to that of DTL logic circuits. For example, the propagation delay time is reduced from approximately 40 ns in a DTL NAND gate to approximately 10 ns in an equivalent TTL circuit.

17.3.3 Basic TTL NAND Circuit

We can improve the circuit performance of the simple TTL circuit in Figure 17.23 by adding a second current gain stage. The resulting basic TTL NAND circuit is shown in Figure 17.24. In this circuit, both transistors Q_2 and Q_o are driven into saturation when $v_X = v_Y =$ logic 1. When at least one input switches from high to low, input transistor Q_1 very quickly pulls Q_2 out of saturation and pull-down resistor R_B provides a path for the excess charge in Q_o, which means that the output transistor can turn off fairly quickly.

DC Current–Voltage Analysis

The analysis of the TTL circuit is very similar to that of the DTL circuit, as demonstrated in the following example.

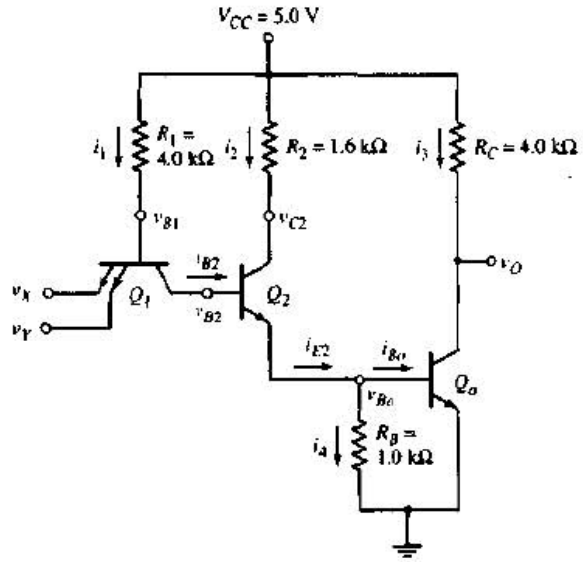


Figure 17.24 TTL circuit with currents and voltages

Example 17.9 **Objective:** Calculate the currents and voltages for the basic TTL NAND circuit.

Consider the TTL circuit in Figure 17.24. Assume the piecewise linear transistor parameters are as listed in Table 17.3. Assume the forward current gain is $\beta_F \equiv \beta = 25$ and the inverse current gain of each input emitter is $\beta_R = 0.1$.

Solution: For $v_X = v_Y = 0.1$ V, Q_1 is biased in saturation and

$$v_{B2} = v_X + v_{CE}(\text{sat}) = 0.1 + 0.1 = 0.2\,\text{V}$$

which means that Q_2 and Q_3 are both cut off. The base voltage v_{B1} is then

$$v_{B1} = v_X + V_{BE}(\text{sat}) = 0.1 + 0.8 = 0.9\,\text{V}$$

and current i_1 is

$$i_1 = \frac{V_{CC} - v_{B1}}{R_1} = \frac{5 - 0.9}{4} = 1.03\,\text{mA}$$

This current flows out of the input transistor emitters. Since Q_2 and Q_3 are cut off, all other currents are zero and the output voltage is $v_O = 5$ V.

If $v_X = v_Y = 5$ V, then the input transistor is biased in the inverse active mode. The base voltage v_{B1} is

$$\begin{aligned} v_{B1} &= V_{BE}(\text{sat})_{Q_3} + V_{BE}(\text{sat})_{Q_2} + V_{BC}(\text{on})_{Q_1} \\ &= 0.8 + 0.8 + 0.7 = 2.3\,\text{V} \end{aligned}$$

and the collector voltage v_{C2} is

$$v_{C2} = V_{BE}(\text{sat})_{Q_3} + V_{CE}(\text{sat})_{Q_2} = 0.8 + 0.1 = 0.9\,\text{V}$$

The currents are

$$i_1 = \frac{V_{CC} - v_{B1}}{R_1} = \frac{5 - 2.3}{4} = 0.675\,\text{mA}$$

and

$$i_{B2} = (1 + 2\beta_R)i_1 = (1 + 0.2)(0.675) = 0.810\,\text{mA}$$

Also,

$$i_2 = \frac{V_{CC} - v_{C2}}{R_2} = \frac{5 - 0.9}{1.6} = 2.56\,\text{mA}$$

which means that

$$i_{E2} = i_2 + i_{B2} = 2.56 + 0.81 = 3.37\,\text{mA}$$

The current in the pull-down resistor is

$$i_4 = \frac{V_{BE}(\text{sat})}{R_B} = \frac{0.8}{1} = 0.8\,\text{mA}$$

and the base drive to the output transistor is

$$i_{Bo} = i_{E2} - i_4 = 3.37 - 0.8 = 2.57\,\text{mA}$$

Current i_3 is

$$i_3 = \frac{V_{CC} - V_{CE}(\text{sat})}{R_C} = \frac{5 - 0.1}{4} = 1.23\,\text{mA}$$

Comment: As mentioned, the analysis of the basic TTL circuit is essentially the same as that of the DTL circuit. The magnitudes of currents and voltages in the basic TTL circuit are also very similar to the DTL results.

Test Your Understanding

[Note: In the following exercise, assume the piecewise linear transistor parameters are as listed in Table 17.3.]

17.11 The parameters of the TTL NAND circuit in Figure 17.24 are: $R_1 = 6\,\text{k}\Omega$, $R_2 = 1.5\,\text{k}\Omega$, $R_B = 1.5\,\text{k}\Omega$, and $R_C = 2.2\,\text{k}\Omega$. Assume that $\beta_F \equiv \beta = 20$ and $\beta_R = 0.1$ (for each input emitter). For a no-load condition, determine the base and collector currents in each transistor for: (a) $v_X = v_Y = 0.1\,\text{V}$, and (b) $v_X = v_Y = 3.6\,\text{V}$. Prove that Q_2 and Q_o are driven into saturation for $v_X = v_Y = 3.6\,\text{V}$. (Ans. (a) $i_1 = i_{B1} = 0.683\,\text{mA}$, $i_{C1} \cong 0$, $i_{B2} = i_{C2} = 0$, $i_{Bo} = i_{Co} = 0$ (b) $i_1 = i_{B1} = 0.45\,\text{mA}$, $i_{B2} = |i_{C1}| = 0.54\,\text{mA}$, $i_2 = i_{C2} = 2.73\,\text{mA}$, $i_{Bo} = 2.74\,\text{mA}$, $i_3 = i_{Co} = 2.23\,\text{mA}$)

17.3.4 TTL Output Stages and Fanout

The propagation delay time can be improved by replacing the output collector resistor with a current source.

When the output changes from low to high, the load capacitance must be charged by a current through the collector pull-up resistor. The total load capacitance is composed of the input capacitances of the load circuits and the capacitances of the interconnect lines. The associated RC time constant for a load capacitance of 15 pF and a collector resistance of 4 kΩ is 60 ns, which is large compared to the propagation delay time of a commercial TTL circuit.

Totem-Pole Output Stage

In Figure 17.25, the combination of Q_3, D_1, and Q_o forms an output stage called a totem pole. Transistor Q_2 forms a phase splitter, because the collector

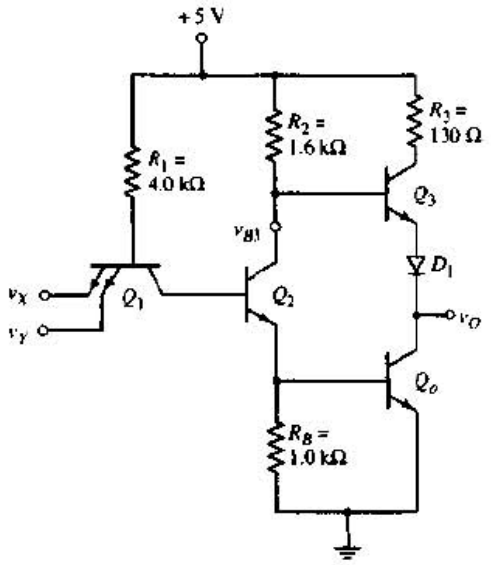


Figure 17.25 TTL circuit with totem-pole output stage

and emitter voltages are 180 degrees out of phase. If $v_X = v_Y$ = logic 1, input transistor Q_1 is biased in the inverse-active mode, and both Q_2 and Q_o are driven into saturation. The voltage at the base of Q_3 is

$$v_{B3} = V_{C2} = V_{BE}(\text{sat})_{Q_o} + V_{CE}(\text{sat})_{Q_2} \tag{17.17}$$

which is on the order of 0.9 V, and the output voltage is approximately 0.1 V. The difference between the base voltage of Q_3 and the output voltage is not sufficient to turn Q_3 and D_1 on. The pn junction offset voltage associated with D_1 must be included so that Q_3 is cut off when the output is low. For this condition, the saturation output transistor discharges the load capacitance and pulls the output low very quickly.

If $v_X = v_Y$ = logic 0, then Q_2 and Q_o are cut off, and the base voltage to Q_3 goes high. The transistor Q_3 and diode D_1 turn on so that the output load capacitance can be charged and the output goes high. Since Q_3 acts like an emitter follower, the output resistance is small so that the effective RC time constant to charge the load capacitance is now very small.

Fanout

Logic gates are not operated in isolation, but are used to drive other similar type logic gates to implement a complex logic function. Figure 17.26 shows the TTL NAND gate with a totem-pole output stage connected to N identical TTL NAND gates. The maximum fanout is defined as the maximum number of similar-type logic circuits that can be connected to the logic gate output without affecting proper circuit operation. For example, the output transistor Q_o must remain in saturation when the output goes low to its logic 0 value. For a given value of β, there is then a maximum allowable load current, and therefore a maximum allowable number of load circuits that can be connected to the output. As another condition, the output transistor is usually rated for a

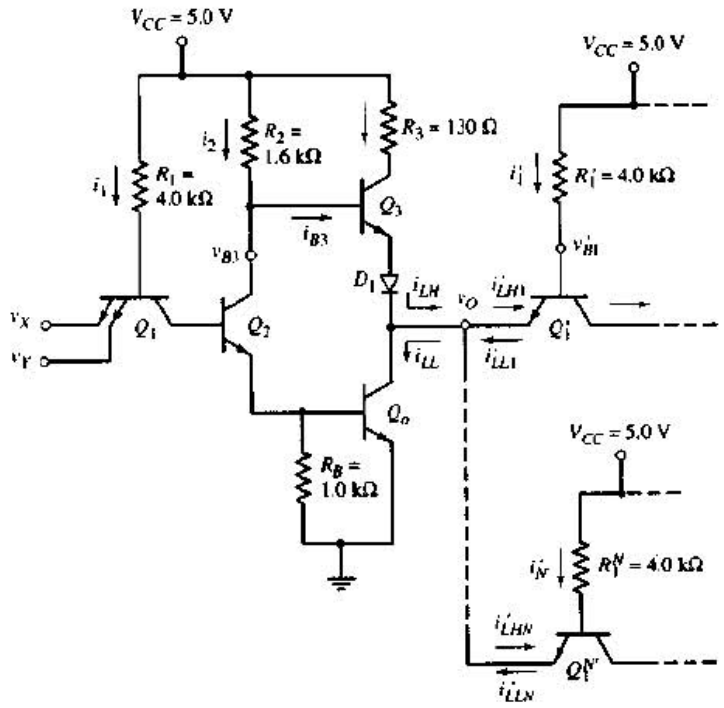


Figure 17.26 TTL circuit with totem-pole output stage driving N identical TTL stages

maximum collector current. For an output low condition, the current i_{LL} is the load current that Q_o must sink from the load circuits.

Example 17.10 **Objective:** Calculate the maximum fanout for the output low condition.

Let $\beta = 25$ for the output transistor.

Solution: Transistor Q_o to remain in saturation. In Example 17.9, we calculated the base current into Q_o as $i_{Bo} = 2.57\,\text{mA}$. The output voltage is $v_O = 0.1\,\text{V}$ so that $v_{B1}' = 0.1 + 0.8 = 0.9\,\text{V}$. Each individual load current is then

$$i_{LL1}' = i_1' \simeq \frac{5 - 0.9}{4} = 1.025\,\text{mA}$$

The maximum collector current in Q_o is

$$i_{Co}(\text{max}) = \beta i_{Bo} = N i_{LL1}'$$

The maximum fanout, N, is then found as

$$N = \frac{\beta i_{Bo}}{i_{LL1}'} = \frac{(25)(2.57)}{1.025} = 62.7$$

The number of load circuits must be an integer, so we round to the next lower integer, or $N = 62$.

With 62 load circuits connected to the output, the collector current would be

$$i_{Co} = N i_{LL1}' = (62)(1.025) = 63.55\,\text{mA}$$

which is a relatively large value. In most cases, the output transistor has a maximum rated collector current that may limit the maximum fanout.

Solution: Maximum rated output current. If the maximum rated collector current of the output transistor is $i_{Co}(\text{rated}) = 20\,\text{mA}$, then the maximum fanout is determined by

$$i_{Co}(\text{rated}) = Ni'_{LL}$$

or

$$N = \frac{i_{Co}(\text{rated})}{i'_{LL}} = \frac{20}{1.025} = 19.5 \rightarrow 19$$

Comment: In the first solution, the resulting fanout of 62 is not realistic since the output transistor current is excessive. In the second solution, a maximum fanout of 19 is more realistic. However, another limitation in terms of proper circuit operation is propagation delay time. For a large number of load circuits connected to the output, the output load capacitance may be quite large which slows down the switching speed to unacceptably large values. The maximum fanout, then, may be limited by the propagation delay time specification.

Again, Figure 17.26 shows the TTL circuit with N identical load circuits and the inputs in their low state. The input transistor is biased in saturation, and both Q_2 and Q_o are cut off, causing base voltage v_{B3} and the output voltage to go high. The input transistors of the load circuits are biased in the inverse-active mode, and the load currents are supplied through Q_3 and D_1. In this circuit, the input transistors of the load gates are one-input NAND (inverter) gates, to illustrate the worst-case or maximum load current under the high input condition. Since the load current is supplied through Q_3, a base current into Q_3 must be supplied from V_{CC} through R_2. As the load current increases, the base current through R_2 increases, which means that voltage v_{B3} decreases because of the voltage drop across R_2. Assuming the B–E voltage of Q_3 and the diode voltage across D_1 remain essentially constant, the output voltage v_O decreases from its maximum value.

A reasonable fanout of 10 or 15 for the high output condition means that the load current will be small, base current i_{B3} will be very small, and the voltage drop across R_2 will be negligible. The output voltage will then be approximately two diode drops below V_{CC}. For typical TTL circuits, the logic 1 = V_{OH} value is on the order of 3.6 V, rather than the 5 V previously determined.

Test Your Understanding

[Note: In the following exercises, assume the piecewise linear transistor parameters are as listed in Table 17.3.]

17.12 (a) For the basic DTL logic circuit, the parameters are as given in Exercise 17.9. Calculate the maximum fanout for the low output condition such that Q_o remains in saturation. (b) Repeat part (a) if the rated collector current of Q_o is $I_{C,\text{rated}} = 15\,\text{mA}$. (Ans. (a) $N = 13$ (b) $N = 13$)

17.13 Consider the TTL circuit shown in Figure 17.24 with parameters as given in Exercise 17.11. Calculate the maximum fanout for the low output. For the low output condition, assume that the output transistor must remain in saturation. (Ans. $N = 76$)

17.14 The TTL circuit shown in Figure 17.25 is redesigned such that $R_1 = 6\,\text{k}\Omega$, $R_2 = 2\,\text{k}\Omega$, $R_3 = 80\,\text{k}\Omega$, and $R_B = 1.5\,\text{k}\Omega$. Assume that $\beta_F = \beta = 20$ and $\beta_R = 0.1$ (for each input emitter). Calculate the fanout for $v_X = v_Y = 3.6\,\text{V}$. For the low output condition, assume that the output transistor must remain in saturation. (Ans. $N = 60$)

Modified Totem-Pole Output Stage

Figure 17.27 shows a modified totem-pole output stage in which transistor Q_4 is used in place of a diode. This has several advantages. First, the transistor pair Q_3 and Q_4 provides greater current gain, which in turn increases the fanout capability of this circuit in its high state. Second, the output impedance in the high state is lower than that of the single transistor, decreasing the switching time. Third, the base–emitter junction of Q_3 fulfills the function of diode D_1; therefore, the diode is no longer needed to provide a voltage offset. In integrated circuits, the fabrication of transistors is no more complex than the fabrication of diodes.

When the output is switched to its low state, resistor R_4 provides a path to ground for the minority carriers that must be pulled out of the base of Q_3 to turn the transistor off. Note that when the output is low, with Q_2 and Q_o in saturation, the voltage at the base of Q_4 is approximately 0.9 V, which is sufficient to bias Q_4 in its active region. However, the voltage at the emitter of Q_4 is only approximately 0.2 V, which means that the current in Q_4 is very small and does not add significantly to the power dissipation.

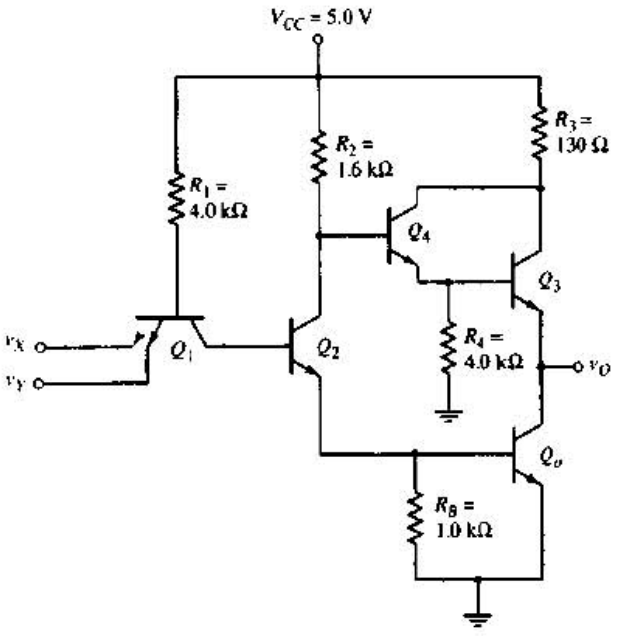


Figure 17.27 TTL circuit with modified totem-pole output stage

17.3.5 Tristate Output

The output impedances of the totem-pole output TTL logic circuits considered thus far are extremely low when the output voltage is in either the high or low state. In memory circuit applications, situations arise in which the outputs of many TTL circuits must be connected together to form a single output. This creates a serious loading situation, demanding that all other TTL outputs be disabled or put into a high impedance state, as shown symbolically in Figure 17.28. Here, G_1 and G_3 are disconnected from the output; the output voltage v_O then measures only the output of logic gate G_2.

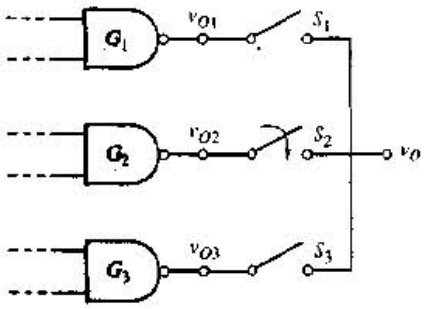


Figure 17.28 Circuit symbolically showing tristate output

The TTL circuit in Figure 17.29 may be used to put the logic output into a high impedance state. When $\overline{D} = 5\,\text{V}$, the state of input transistor Q_1 is controlled by inputs v_X and v_Y. Under these circumstances, diode D_2 is always reverse biased and the circuit function is the NAND function already considered.

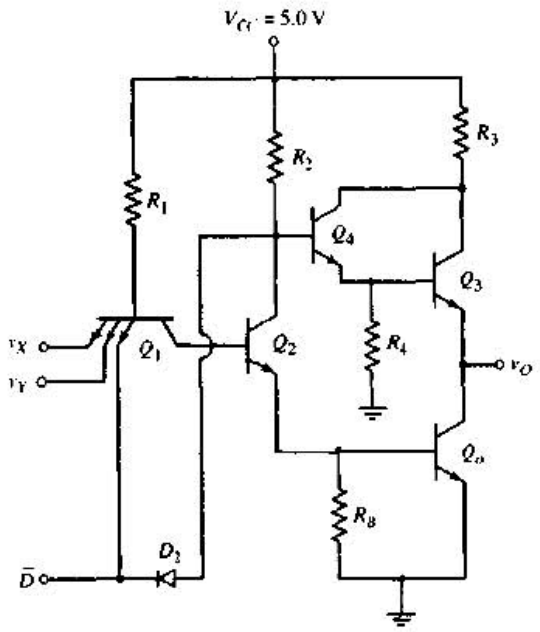


Figure 17.29 TTL circuit with tristate output stage

When $\overline{D}$ is driven to a logic 0 state of 0.1 V, the low voltage at the emitter of Q_1 ensures that both Q_2 and Q_o are cut off, and the low voltage applied to D_2 means that D_2 is forward biased. The voltage at the base of Q_4 is approximately 0.8 V, which means that Q_3 is also cut off. In this condition, then, both output transistors Q_3 and Q_o are cut off. The impedance looking back into transistors that are cut off is normally in the megohm range. Therefore, when TTL circuits are paralleled to increase the capability of a digital system, the tristate output stage is either enabled or disabled via the $\overline{D}$ select line. The output stage on only one TTL circuit may be enabled at any one time.

Test Your Understanding

[Note: In the following exercise, assume the piecewise linear transistor parameters are as listed in Table 17.3.]

17.15 For the tristate TTL circuit in Figure 17.29, the parameters are: $R_1 = 6\,\text{k}\Omega$, $R_2 = 2\,\text{k}\Omega$, $R_3 = 100\,\Omega$, $R_4 = 4\,\text{k}\Omega$, and $R_B = 1\,\text{k}\Omega$. Assume that $\beta_F \equiv \beta = 20$ and $\beta_R = 0.1$ (for each input emitter). For $\overline{D} = 0.1$ V, calculate the base and collector currents in each transistor. (Ans. $i_{B1} = 0.683\,\text{mA}$, $|i_{C1}| = i_{B2} = i_{C2} = i_{Bo} = i_{Co} = 0$, $i_{B4} = 1.19\,\mu\text{A}$, $i_{C4} = 23.8\,\mu\text{A}$, $i_{B3} = i_{C3} = 0$)

17.4 SCHOTTKY TRANSISTOR–TRANSISTOR LOGIC

The TTL circuits considered thus far drive the output and phase-splitter transistors between cutoff in the high output stage and saturation in the low output state. The input transistor is driven between saturation and the inverse-active mode. Since the propagation delay time of a TTL gate is a strong function of the storage time of the saturation transistors, a nonsaturation logic circuit would be an advantage. In the Schottky clamped transistor, the transistor is prevented from being driven into deep saturation and has a storage time of only approximately 50 ps.

17.4.1 Schottky Clamped Transistor

The symbol for the Schottky clamped transistor, or simply the Schottky transistor, is shown in Figure 17.30(a); its equivalent configuration is

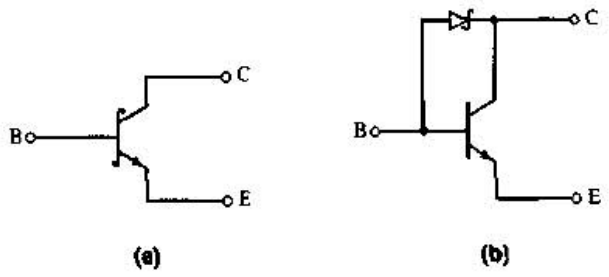


Figure 17.30 (a) Schottky clamped transistor symbol and (b) Schottky clamped transistor equivalent circuit

given in Figure 17.30(b). In this transistor, a Schottky diode is connected between the base and collector of an npn bipolar transistor. Two characteristics of the Schottky diode are: a low turn-on voltage and a fast-switching time. When the transistor is in its active region, the base–collector junction is reverse biased, which means that the Schottky diode is reverse biased and effectively out of the circuit. The Schottky transistor then behaves like a normal npn bipolar transistor. As the Schottky transistor goes into saturation, the base–collector junction becomes forward biased, and the base-collector voltage is effectively clamped at the Schottky diode turn-on voltage, which is normally between 0.3 and 0.4 V. The excess base current is shunted through the diode, and the basic npn transistor is prevented from going deeply into saturation.

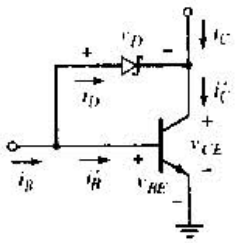


Figure 17.31 Schottky clamped transistor equivalent circuit, with currents and voltages

Figure 17.31 shows the equivalent circuit of the Schottky transistor with designated currents and voltages. Currents i_C and i_B are the collector and base currents, respectively, of the Schottky transistor, while i'_C and i'_B are the collector and base currents, respectively, of the internal npn transistor.

The three defining equations for the Schottky transistor are

$$i'_C = i_D + i_C \tag{17.18}$$

$$i_B = i'_B + i_D \tag{17.19}$$

and

$$i'_C = \beta i'_B \tag{17.20}$$

Equation (17.20) is appropriate since the internal transistor is clamped at the edge of saturation. If $i_C < \beta i_B$, then the Schottky diode is forward biased, $i_D > 0$, and the Schottky transistor is said to be in saturation. However, the internal transistor is only driven to the edge of saturation in this case.

Combining Equations (17.19) and (17.20), we find that

$$i_D = i_B - i'_B = i_B - \frac{i'_C}{\beta} \tag{17.21}$$

Substituting this equation into Equation (17.18) yields

$$i'_C = i_B - \frac{i'_C}{\beta} + i_C \tag{17.22(a)}$$

or

$$i'_C = \frac{i_B + i_C}{1 + (1/\beta)} \tag{17.22(b)}$$

Equation (17.22(b)) relates the internal transistor collector current to the external Schottky transistor collector and base currents.

Example 17.11 **Objective**: Determine the currents in a Schottky transistor.

Consider the Schottky transistor in Figure 17.31 with an input base current of $i_B = 1\,\text{mA}$. Assume that $\beta = 25$. Determine the internal currents in the Schottky transistor for $i_C = 2\,\text{mA}$, and then for $i_C = 20\,\text{mA}$.

Solution: For $i_C = 2\,\text{mA}$, the internal collector current is, from Equation (17.22(b)),

$$i_C' = \frac{1+2}{1+(1/25)} = 2.89\,\text{mA}$$

and the internal base current is

$$i_B' = \frac{i_C'}{\beta} = \frac{2.89}{25} = 0.115\,\text{mA}$$

The Schottky diode current is therefore

$$i_D = i_B - i_B' = 1 - 0.115 = 0.885\,\text{mA}$$

Repeating the calculations for $i_C = 20\,\text{mA}$, we obtain

$$i_C' = 20.2\,\text{mA}$$
$$i_B' = 0.808\,\text{mA}$$
$$i_D = 0.192\,\text{mA}$$

Comment: For a relatively small collector current into the Schottky transistor, the majority of the input base current is shunted through the Schottky diode. As the collector current into the Schottky transistor increases, less current is shunted through the Schottky diode and more current flows into the base of the npn transistor.

Test Your Understanding

[Note: In the following exercise, assume the piecewise linear transistor parameters are as listed in Table 17.3. In addition, assume a Schottky diode turn-on voltage of $V_\gamma(\text{SD}) = 0.3\,\text{V}$.]

17.16 Consider the Schottky clamped transistor in Figure 17.32. Assume $\beta = 10$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, and $V_\gamma(\text{SD}) = 0.3\,\text{V}$. (a) For no load, $i_L = 0$, find the currents i_D, i_B', and i_C'. (b) Determine the maximum load current i_L that the transistor can sink and still remain at the edge of saturation. (Ans. (a) $i_C' = 3.67\,\text{mA}$, $i_B' = 0.367\,\text{mA}$, $i_D = 1.63\,\text{mA}$ (b) $i_L(\text{max}) \cong 18\,\text{mA}$)

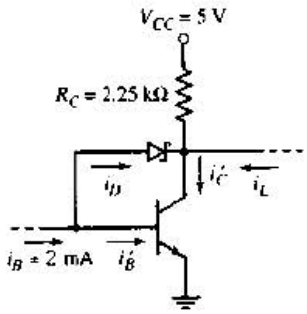


Figure 17.32 Figure for Exercise 17.16

Since the internal npn bipolar transistor is not driven deeply into saturation, we assume that the B–E junction voltage remains equal to the turn-on voltage, or $v_{BE} = V_{BE}(\text{on})$. If the Schottky transistor is biased in saturation, then the C–E voltage is

$$v_{CE} = V_{CE}(\text{sat}) = V_{BE}(\text{on}) - V_\gamma(\text{SD}) \tag{17.23}$$

where $V_\gamma(\text{SD})$ is the turn-on voltage of the Schottky diode. Assuming parameter values of $V_{BE}(\text{on}) = 0.7\,\text{V}$ and $V_\gamma(\text{SD}) = 0.3\,\text{V}$, the collector–emitter saturation voltage of a Schottky transistor is $V_{CE}(\text{sat}) = 0.4\,\text{V}$. When the Schottky transistor is at the edge of saturation, then $i_D = 0$, $i_C = \beta i_B$, and $v_{CE} = V_{CE}(\text{sat})$.

17.4.2 Schottky TTL NAND Circuit

Figure 17.33 shows a Schottky TTL NAND circuit in which all of the transistors except Q_3 are Schottky clamped transistors. The connection of Q_4 across the base–collector of Q_3 prevents this junction from becoming forward biased, ensuring that Q_3 never goes into saturation. Another difference between this circuit and the standard TTL circuit is that the pull-down resistor at the base of output transistor Q_o has been replaced by transistor Q_5 and two resistors. This arrangement is called a **squaring network**, since it squares, or sharpens, the voltage transfer characteristics of the circuit.

Device Q_2 is prevented from conducting until the input voltage is large enough to turn on both Q_2 and Q_o simultaneously. Recall that the passive pull-down resistor on the TTL circuit provided a pathway for removing stored charge in the base of the output transistor, when the output transistor was turned off from the saturated state. Transistor Q_5 now provides an active pull-down network that pulls Q_o out of saturation more quickly.

This is one example of a circuit in which the piecewise linear model of a transistor fails to provide an adequate solution for the circuit analysis. With the piecewise linear model, Q_5 would apparently never turn on. However, because of the exponential relationship between collector current and base-emitter voltage, transistor Q_5 does turn on and does help pull Q_o out of saturation during switching.

The two Schottky diodes between the input terminals and ground act as clamps to suppress any ringing that might occur from voltage transitions. The input diodes clamp any negative undershoots at approximately −0.3 V.

The dc current–voltage analysis of the Schottky TTL circuit in Figure 17.33 is similar to that for the standard TTL circuit. One minor difference is that when the inputs are high and the input transistor is in the inverse-active

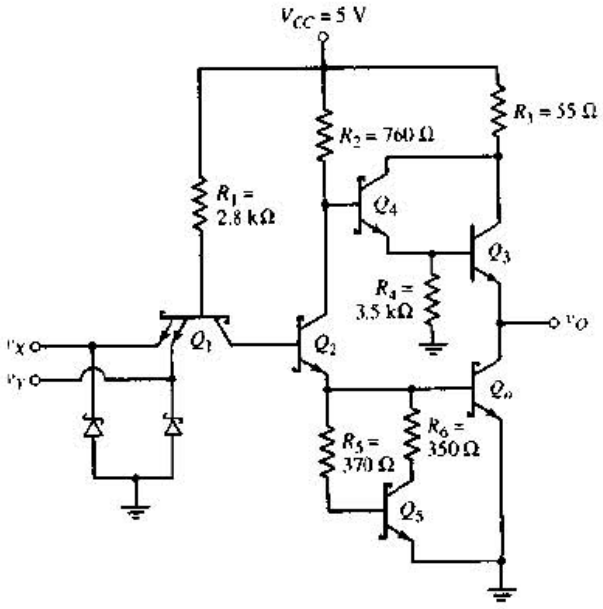


Figure 17.33 Schottky TTL NAND logic circuit

mode, the B-C forward bias voltage is 0.3 V, because of the Schottky diode connected between the base and collector junctions.

The major difference between the Schottky circuit and standard TTL circuits is the quantity of excess minority carrier storage in the transistors when they are driven into or near saturation. The internal npn transistor of the Schottky clamped transistor is held at the edge of saturation, and the resulting propagation delay time is on the order of 2 to 5 ns, compared to a nominal 10 to 15 ns for standard TTL circuits.

A slight difference between the Schottky and standard TTL circuits is the value of the output voltage in the logic 0 state. The low output voltage of a standard TTL circuit is in the range of 0.1 to 0.2 V, while the Schottky transistor low output saturation voltage, V_{OL}, is approximately 0.4 V. The output voltage in the logic 1 state is essentially the same for both types of logic circuits.

Test Your Understanding

(Note: In the following exercise, assume the piecewise linear transistor parameters are as listed in Table 17.3. In addition, assume a Schottky diode turn-on voltage of $V_\gamma(SD) = 0.3$ V.]

17.17 In the Schottky TTL NAND circuit in Figure 17.33, assume $\beta_F \equiv \beta = 25$ and $\beta_R = 0$. For a no-load condition, calculate the power dissipation for: (a) $v_X = v_Y = 0.4$ V, and (b) $v_X = v_Y = 3.6$ V. (Ans. $P = 12.5$ mW (b) $P = 32.1$ mW)

17.4.3 Low-Power Schottky TTL Circuits

The Schottky TTL circuit in Figure 17.33 and the standard TTL circuit dissipate approximately the same power, since voltage and resistance values in the two circuits are similar. The advantage of the Schottky TTL circuit is the reduction in propagation delay time by a factor of 3 to 10.

Propagation delay times depend on the type of transistors (Schottky clamped or regular) used in the circuit, and on the current levels in the circuit. The storage time of a regular transistor is a function of the reverse base current that pulls the transistor out of saturation. Also, the transistor turn-on time depends on the current level charging the base–emitter junction capacitance. A desirable trade-off can therefore be made between current levels (power dissipation) and propagation delay times. Smaller current levels lead to lower power dissipation, but at the expense of increased propagation delay times. This trade-off has been successful in commercial applications, where very short propagation delay times are not always necessary, but reduced power requirements are always an advantage.

A **low-power Schottky** TTL NAND circuit is shown in Figure 17.34. With few exceptions, these circuits do not use the multiemitter input transistor of standard TTL circuits. Most low-power Schottky circuits use a DTL type of input circuit, with Schottky diodes performing the AND function. This circuit is faster than the classic multiemitter input transistor circuit, and the input breakdown voltage is also higher.

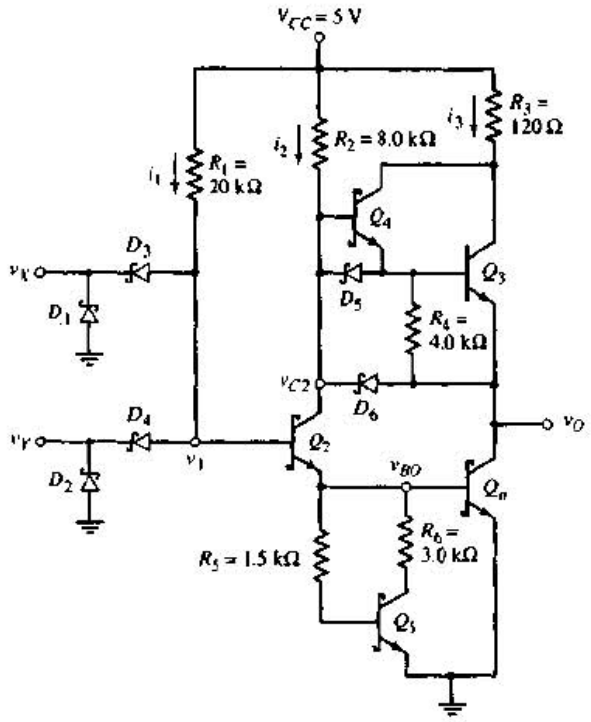


Figure 17.34 Low-power Schottky TTL NAND logic circuit

The dc analysis of the low-power Schottky circuit is identical to that of DTL circuits.

Example 17.12 **Objective:** Calculate the power dissipation in a low-power Schottky TTL circuit.

Consider the circuit shown in Figure 17.34. Assume the Schottky diode turn-on voltage is $V_\gamma(SD) = 0.3$ V and the transistor parameters are: $V_{BE}(on) = 0.7$ V, $V_{CE}(sat) = 0.4$ V, and $\beta = 25$.

Solution: For the low input condition, $v_X = v_Y = 0.4$ V and $v_1 = 0.4 + 0.3 = 0.7$ V. Current i_1 is

$$i_1 = \frac{V_{CC} - v_1}{R_1} = \frac{5 - 0.7}{20} = 0.215\,\text{mA}$$

Since Q_2 and Q_o are cut off with a no-load condition, all other currents in the circuit are zero. The power dissipation for the low input condition is therefore

$$P_L = i_1(V_{CC} - v_X) = (0.215) \cdot (5 - 0.4) = 0.989\,\text{mW}$$

For the high input condition, $v_X = v_Y = 3.6$ V, voltage v_1 is

$$v_1 = V_{BE}(on)_{Q_o} + V_{BE}(on)_{Q_2} = 0.7 + 0.7 = 1.4\,\text{V}$$

and voltage v_{C2} is

$$v_{C2} = V_{BE}(on)_{Q_o} + V_{CE}(sat)_{Q_2} = 0.7 + 0.4 = 1.1\,\text{V}$$

The currents are then

$$i_1 = \frac{V_{CC} - v_1}{R_1} = \frac{5 - 1.4}{20} = 0.18\,\text{mA}$$

and

$$i_2 = \frac{V_{CC} - v_{C2}}{R_2} = \frac{5 - 1.1}{8} = 0.488\,\text{mA}$$

When $v_{C2} = 1.1\,\text{V}$ and $v_O = 0.4\,\text{V}$, transistor Q_4 is at the edge of turn-on, however, since there is no voltage drop across R_4, Q_4 has negligible emitter current. For a no-load condition, all other currents are zero. Therefore, the power dissipation for the high input condition is

$$P_H = (i_1 + i_2)V_{CC} = (0.18 + 0.488) \cdot 5 = 3.34\,\text{mW}$$

Comment: The power dissipation in this low-power Schottky TTL circuit is approximately a factor of five smaller than in the Schottky or standard TTL logic gates. The propagation delay time in the low-power Schottky circuit is approximately 10 ns, which compares closely with the propagation delay time for a standard TTL circuit.

Diodes D_5 and D_6 are called **speedup diodes**. As we showed in the dc analysis, these diodes are reverse biased when the inputs are in either a static logic 0 or a logic 1 mode. When at least one input is in a logic 0 state, the output is high, and Q_3 and Q_4 tend to turn on, supplying any necessary load current. When both inputs are switched to their logic 1 state, Q_2 turns on and v_{C2} decreases, forward biasing D_5 and D_6. Diode D_5 helps to pull charge out of the base of Q_3, turning this transistor off more rapidly. Diode D_6 helps discharge the load capacitance, which means that output voltage v_O switches low more rapidly.

Test Your Understanding

[Note: In the following exercise, assume the piecewise linear transistor parameters are as listed in Table 17.3. In addition, assume a Schottky diode turn-on voltage of $V_\gamma(\text{SD}) = 0.3\,\text{V}$.]

17.18 Assume the low-power Schottky TTL circuit in Figure 17.34 is redesigned such that $R_1 = 40\,\text{k}\Omega$ and $R_2 = 12\,\text{k}\Omega$, and all other circuit parameters remain the same. The transistor and diode parameters are: $V_{BE}(\text{on}) = 0.7\,\text{V}$, $V_{CE}(\text{sat}) = 0.4\,\text{V}$, $\beta = 25$, and $V_\gamma(\text{SD}) = 0.3\,\text{V}$. Assuming no load, determine the base and collector currents in each transistor, and the power dissipation in the gate, for: (a) $v_X = v_Y = 0.4\,\text{V}$, and (b) $v_X = v_Y = 3.6\,\text{V}$. (Ans. (a) $i_{B2} = i_{C2} = i_{B_0} = i_{C_0} = i_{B5} = i_{C5} = 0$, $i_{B3} = i_{C3} = i_{B4} = i_{C4} = 0$, $P = 497\,\mu\text{W}$ (b) $i_{B2} = 90\,\mu\text{A}$, $i_{C2} = 325\,\mu\text{A}$, $i_{B4} = i_{C4} = i_{B3} = i_{C3} = 0$, $i_{B5} \cong i_{C5} \cong 0$, $i_{B_0} = 415\,\mu\text{A}$, $i_{C_0} = 0$, $P = 2.08\,\text{mW}$)

17.4.4 Advanced Schottky TTL Circuits

The advanced low-power Schottky circuit possesses the lowest speed-power product with a propagation delay time short enough to accommodate a large

number of digital applications, while still maintaining the low power dissipation of the low-power Schottky family of logic circuits. The major modification lies in the design of the input circuitry. Consider the circuit shown in Figure 17.35. The input circuit contains a pnp transistor Q_1, a current amplification transistor Q_2, and a Schottky diode D_2 from the base of Q_3 to the input. Diode D_2 provides a low-impedance path to ground when the input makes a high-to-low transition. This enhances the inverter switching time. The current driver transistor Q_1 provides a faster transition when the input goes from low to high than if a Schottky diode input stage were used. Transistor Q_4 provides the switch element that steers current from R_1 either to Q_2 or the input source.

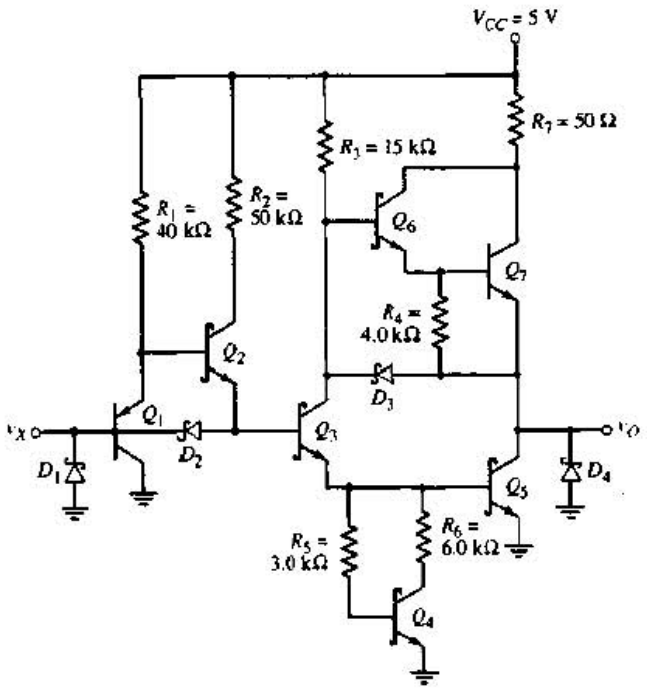


Figure 17.35 Advanced low-power Schottky (ALS) inverter gate

When $v_X = 0.4$ V, the E–B junction of Q_4 is forward biased, and Q_1 is biased in its active region. The base voltage of Q_2 is approximately 1.1 V; Q_2, Q_3, and Q_5 are cut off; and the output voltage goes high. Most of the current through R_1 goes to ground through Q_1, so very little current sinking is required of the driver output transistor. When $v_X = 3.6$ V, transistors Q_2, Q_3, and Q_5 turn on, the voltage at the base of Q_2 is clamped at approximately 2.1 V, the E–B junction of Q_1 is reverse biased, and Q_1 is cut off.

With fast switching circuits, inductances, capacitances, and signal delays may introduce problems requiring the use of transmission line theory. Clamping diodes D_1 and D_4 at the input and output terminals clamp any negative-going switching transients that result from ringing signals on the interconnect lines.

Test Your Understanding

[Note: In the following exercise, assume the piecewise linear transistor parameters are as listed in Table 17.3. In addition, assume a Schottky diode turn-on voltage of $V_\gamma(\text{SD}) = 0.3\,\text{V}$.]

17.19 Consider the advanced low-power Schottky circuit shown in Figure 17.35. Let $V_{CC} = 5\,\text{V}$. Determine the current in R_1 for: (a) $v_X = 0.4\,\text{V}$, and (b) $v_X = 3.6\,\text{V}$. (Ans. (a) $i_1 = 97.5\,\mu\text{A}$ (b) $i_1 = 72.5\,\mu\text{A}$)

17.5 BiCMOS DIGITAL CIRCUITS

As we have discussed previously, BiCMOS technology combines bipolar and CMOS circuits on one IC chip. This technology combines the high-input-impedance, low-power characteristics of CMOS with the high-current drive characteristics of bipolar circuits. If the CMOS circuit has to drive a few other similar CMOS logic circuits, the current drive capability is not a problem. However, if a circuit has to drive a relatively large capacitive load, bipolar circuits are preferable because of the relatively large transconductance of BJTs.

We consider a BiCMOS inverter circuit and then a simple example of a BiCMOS digital circuit. This section is intended only to introduce this technology.

17.5.1 BiCMOS Inverter

Several BiCMOS inverter configurations have been proposed. In each case, npn bipolar transistors are used as output devices and are driven by a quasi-CMOS inverter configuration. The simplest BiCMOS inverter is shown in Figure 17.36(a). The output stage of the npn transistors is similar to the totem-pole output stage of the TTL circuits that were considered in Section 17.3.

When the input voltage v_I of the BiCMOS inverter in Figure 17.36(a) is low, the transistors M_N and Q_2 are cut off. The transistor M_P is turned on and provides base current to Q_1 so that Q_1 turns on and supplies current to the load capacitance. The load capacitance charges and the output voltage goes high. As the output voltage goes high, the output current will normally become very small, so that M_N is driven into its nonsaturation region and the drain-to-source voltage will become essentially zero. The transistor Q_1 will essentially cut off and the output voltage will charge to a maximum value of approximately $v_O(\text{max}) = V_{DD} - V_{BE}(\text{on})$.

When the input voltage v_I goes high, M_P turns off, eliminating any bias current to Q_1, so Q_1 is also off. The two transistors M_N and Q_2 turn on and provide a discharge path for the load capacitance so the output voltage goes low. In steady state, the load current will normally be very small, so M_N will be biased in the nonsaturation region. The drain-to-source voltage will become essentially zero. The transistor Q_2 will be essentially off and the

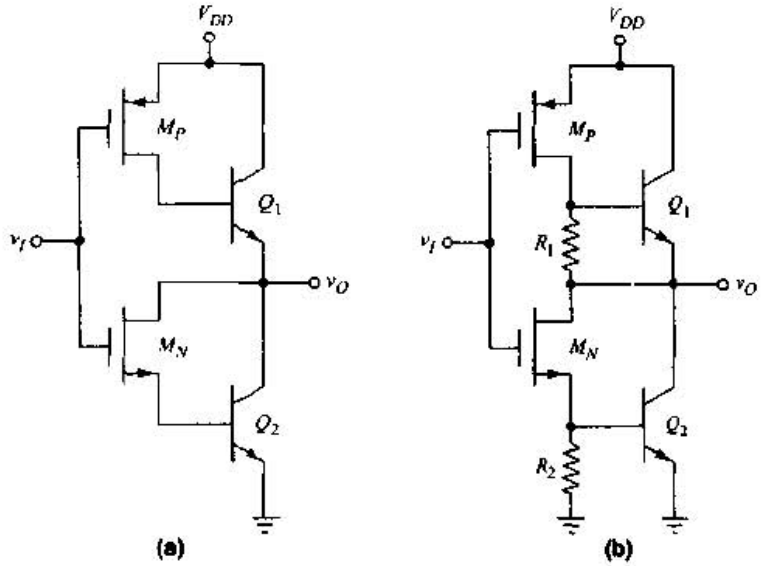


Figure 17.36 (a) Basic BiCMOS inverter. (b) Improved version of BiCMOS inverter

output voltage will discharge to a minimum value of approximately $v_O(\text{min}) \cong V_{BE}(\text{on})$.

One serious disadvantage of the inverter in Figure 17.36(a) is that there is no path through which base charge from the npn transistors can be removed when they are turning off. Thus, the turn-off time of the two npn transistors can be relatively long. A solution to this problem is to include pull-down resistors, as shown in the circuit in Figure 17.36(b). Now, when the npn transistors are being turned off, the stored base charge can be removed to ground through R_1 or R_2. An added advantage of this circuit is, that when v_I goes high and the output goes low, the very small output current through M_N and R_2 means the output voltage is pulled to ground potential. Also, as v_I goes low and the output goes high, the very small load current means that the output is pulled up to essentially V_{DD} through the resistor R_1. We may note that the two npn output transistors are never on at the same time.

Other circuit designs incorporate other transistors that aid in turning transistors off and increasing switching speed. However, these two examples have demonstrated the basic principle used in BiCMOS inverter circuit designs.

17.5.2 BiCMOS Logic Circuit

In BiCMOS logic circuits, the logic function is implemented by the CMOS portion of the circuit and the bipolar transistors again act as a buffered output stage providing the necessary current drive. One example of a BiCMOS logic circuit is shown in Figure 17.37. This is a two-input NOR gate. As seen in the figure, the CMOS configuration is the same as the basic CMOS NOR logic gate considered previously. The two npn output transistors and the R_1 and R_2 resistors have the same configuration and purpose as was seen in the BiCMOS inverter.

Other BiCMOS logic circuits are designed in a manner similar to that shown for the BiCMOS NOR gate.

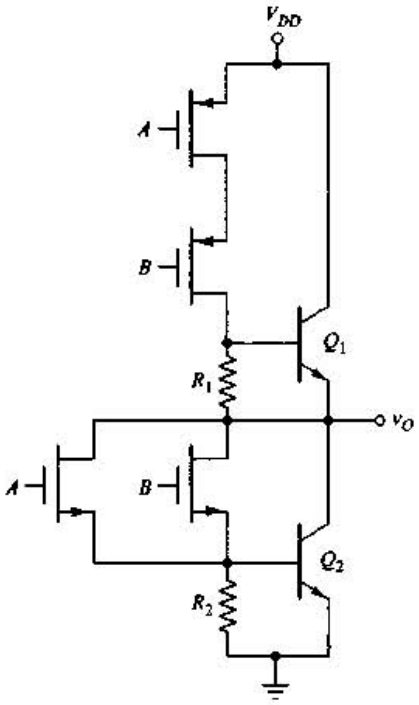


Figure 17.37 Two-input BiCMOS NOR circuit

17.6 SUMMARY

- This chapter presented the analysis and design of bipolar digital logic circuits, which were historically the first logic gate technology used in digital systems.
- Emitter coupled logic (ECL) is used in specialized high-speed applications. The basic ECL gate is the same as the differential amplifier, but transistors are switched between cutoff and the active region. Avoiding driving transistors into saturation keeps the propagation delay time to a minimum. The classical ECL gate uses the diff-amp configuration in conjunction with emitter-follower output stages and a reference voltage circuit. Both NOR and OR output are available. Although the propagation delay of this logic gate is short, on the order of a nanosecond, the power dissipated in the circuit is rather large.
- Transistor–transistor logic (TTL) was introduced by discussing Diode–transistor logic (DTL). The analysis of the DTL circuit introduced saturating bipolar logic circuits and their characteristics.
- The input transistor of the TTL circuit is driven between saturation and the inverse active mode. This transistor reduces the switching time by quickly pulling charge out of the base of a saturated transistor. The totem-pole output stage was introduced in order to increase the switching speed of the output stage. The maximum fanout was determined by specifying that the output transistor was to remain biased in the saturation region and also by specifying a maximum collector current in the output transistor. Maximum fanout is also a function of the specified propagation delay time.
- Schottky TTL was introduced. The Schottky clamped transistor has a Schottky diode between base and collector of an npn transistor. When the transistor starts into

saturation, this diode turns on and clamps the forward-bias base–collector voltage to approximately 0.3 V, thus preventing the transistor from being driven deep into saturation. This effect substantially reduces the turn-off time of the transistor. The propagation delay time of Schottky TTL, then, is shorter than that of regular TTL.

- Low-power Schottky TTL has the same basic configuration as the DTL circuit. Resistor values are increased so as to reduce the currents, which in turn reduce the power dissipated per circuit. However, since current is reduced, the time to charge and discharge circuit and load capacitances is increased and propagation time increases. The trade-off is between power dissipation and propagation delay time.
- BiCMOS circuits incorporate the best characteristics of both the CMOS and bipolar technologies. Two examples of a BiCMOS inverter were discussed. A basic CMOS inverter drives a bipolar output stage. Thus, the high input impedance and low power dissipation of the CMOS design is coupled with the high-current drive capability of a bipolar output stage. An example of a BiCMOS NOR logic circuit was considered.

CHECKPOINT

After studying this chapter, the reader should have the ability to:

✔ Analyze and design a basic ECL OR/NOR logic gate. (Section 17.1)

✔ Analyze and design modified, lower-power ECL logic gates. (Section 17.2)

✔ Describe the operation and characteristics of the input transistor of a TTL logic circuit. (Section 17.3)

✔ Analyze and design a TTL NAND logic gate. (Section 17.3)

✔ Describe the operation and characteristics of a Schottky transistor, and analyze and design a Schottky TTL logic circuit. (Section 17.4)

REVIEW QUESTIONS

1. Sketch a basic bipolar differential amplifier circuit and sketch the dc transfer characteristics. Explain how the circuit is used in a digital application.
2. Why must emitter-follower output stages be added to the diff-amp to make this circuit a practical logic gate? Explain the operation of the circuit in terms of the reference voltage.
3. Sketch the voltage transfer characteristics of the basic ECL circuit. Describe the noise margins.
4. Sketch a modified ECL circuit in which a Schottky diode is incorporated in the collector portion of the circuit. Explain the purpose of the Schottky diode.
5. Explain the concept of series gating for ECL circuits. What are the advantages of this configuration?
6. Sketch a diode–transistor NAND circuit and explain the operation of the circuit. Explain the concept of minimum β and the purpose of the pull-down resistor.
7. Explain the operation and purpose of the input transistor in a TTL circuit.
8. Sketch a basic TTL NAND circuit and explain its operation.
9. Sketch a totem-pole output stage and explain its operation and the advantages of incorporating this circuit in the TTL circuit.
10. Explain how maximum fanout can be based on maintaining the output transistor in saturation when the output is low.
11. Explain how maximum fanout can be based on a maximum rated collector current in the output transistor when the output is low.
12. Explain the operation of a Schottky clamped transistor. What are its advantages?

13. What is the primary advantage of a Schottky TTL NAND gate compared to a regular TTL NAND gate.
14. Sketch a low-power Schottky TTL NAND circuit. What are the primary differences between this circuit and the regular DTL circuit considered earlier in the chapter?
15. Sketch a basic BiCMOS inverter and explain its operation. Explain the advantages of this inverter compared to a simple CMOS inverter.
16. Sketch a BiCMOS NAND logic circuit and explain its operation.

PROBLEMS

[Note: In the following problems, assume the transistor and diode parameters are as listed in Table 17.3 and $T = 300\,°K$, unless otherwise stated.]

Section 17.1 Emitter-Coupled Logic (ECL)

17.1 For the differential amplifier in Figure P17.1, neglect base currents. (a) For $v_I = -1.5\,V$, calculate i_E, v_{O1}, and v_{O2}. (b) For $v_I = 1.0\,V$, calculate i_E and v_{O2}. (c) Determine R_{C1} such that the logic 0 level at v_{O1} is the same as the logic 0 value at v_{O2}.

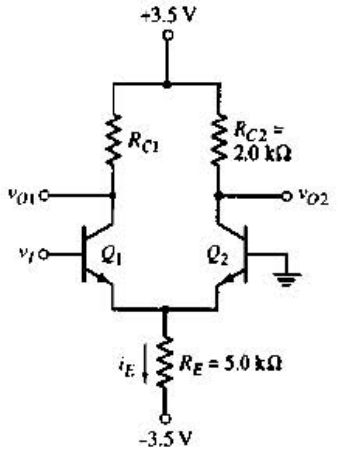


Figure P17.1

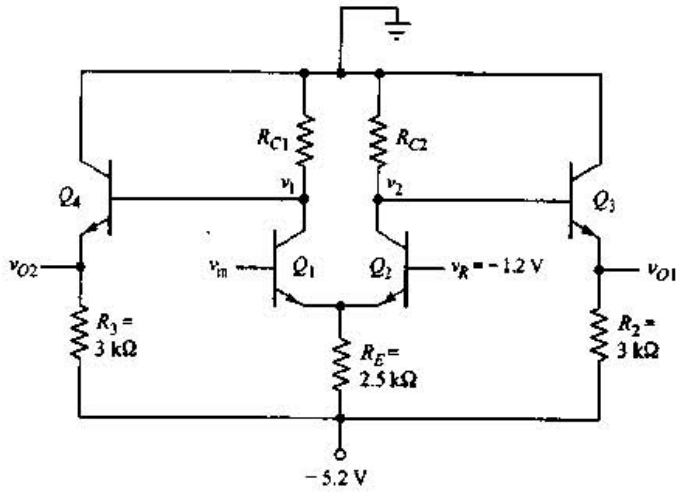


Figure P17.2

17.2 Consider the circuit in Figure P17.2. (a) Determine R_{C2} such that $v_2 = -1\,V$ when Q_2 is on and Q_1 is off. (b) For $v_{in} = -0.7\,V$, determine R_{C1} such that $v_1 = -1\,V$. (c) For $v_{in} = -0.7\,V$, find v_{O1} and v_{O2}, and for $v_{in} = -1.7\,V$, find v_{O1} and v_{O2}. (d) Find the power dissipated in the circuit for (i) $v_{in} = -0.7\,V$ and for (ii) $v_{in} = -1.7\,V$.

17.3 Consider the ECL logic circuit in Figure P17.3. Neglect base currents. (a) Determine the reference voltage V_R. (b) Find the logic 0 and logic 1 voltage values at each output v_{O1} and v_{O2}. Assume that inputs v_X and v_Y have the same values as the logic levels at v_{O1} and v_{O2}.

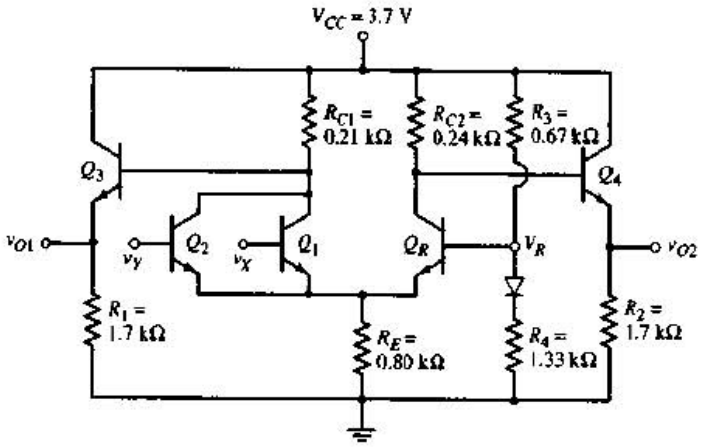


Figure P17.3

17.4 Consider the circuit in Figure P17.4. Neglect base currents. Calculate all resistor values such that the following specifications are satisfied: logic 1 = 1.0 V and logic 0 = 0 V; V_R is the average of logic 1 and logic 0; $i_E = 1.0$ mA when Q_R is on; $i_1 = i_2 = 1.0$ mA; $i_3 = 3.0$ mA when v_{OR} = logic 1; and $i_4 = 3.0$ mA when v_{NOR} = logic 0.

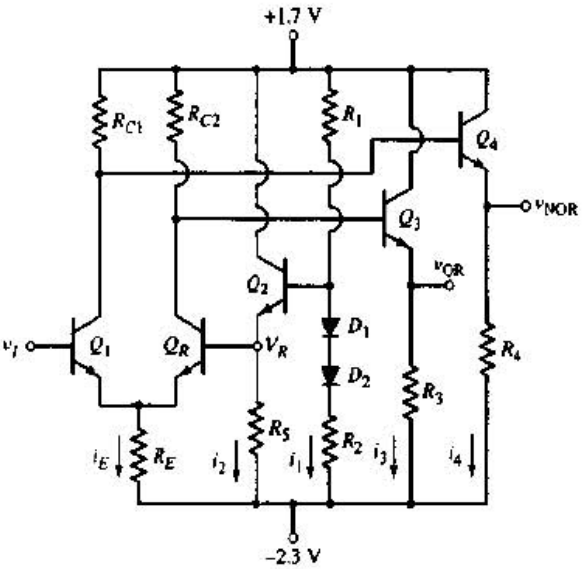


Figure P17.4

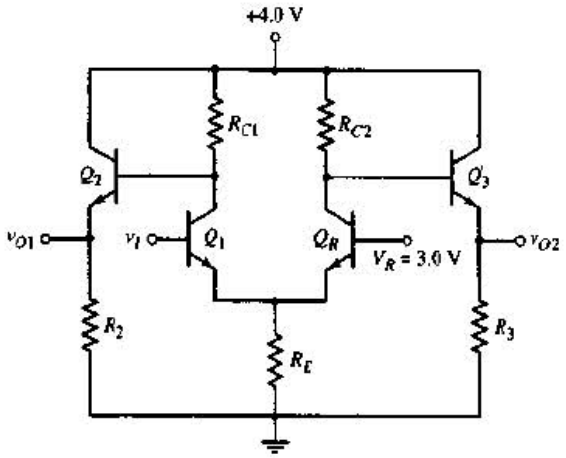


Figure P17.5

17.5 In the ECL circuit in Figure P17.5, the outputs have a logic swing of 0.60 V, which is symmetrical about the reference voltage. Neglect base currents. The maximum emitter current for all transistors is 5.0 mA. Assume the input logic voltages v_I are compatible with the output logic voltages. Calculate the resistances of R_{C1}, R_{C2}, R_E, R_2 and R_3.

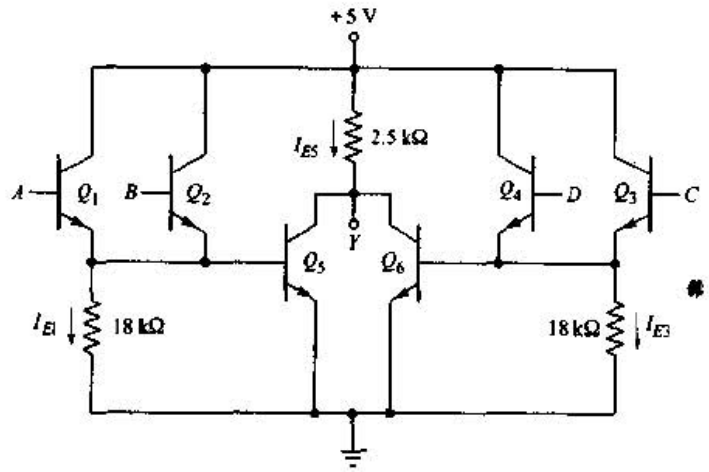


Figure P17.6

17.6 For the circuit in Figure P17.6, complete the following table. What logic function does the circuit perform?

A	B	C	D	I_{E1}	I_{E3}	I_{E5}	Y
0	0	0	0				
5 V	0	0	0				
5 V	0	5 V	0				
5 V	5 V	5 V	5 V				

17.7 Consider the ECL circuit in Figure P17.7. The input voltages A and B are compatible with the output voltages v_{O1} and v_{O2}. (a) Determine the reference voltage V_R. (b) Determine the logic 0 and logic 1 levels at the outputs v_{O1} and v_{O2}. (c) Determine the voltage V_E for $A = B =$ logic 0 and for $A = B =$ logic 1. (d) Determine the total power dissipated in the circuit for $A = B =$ logic 0 and for $A = B =$ logic 1.

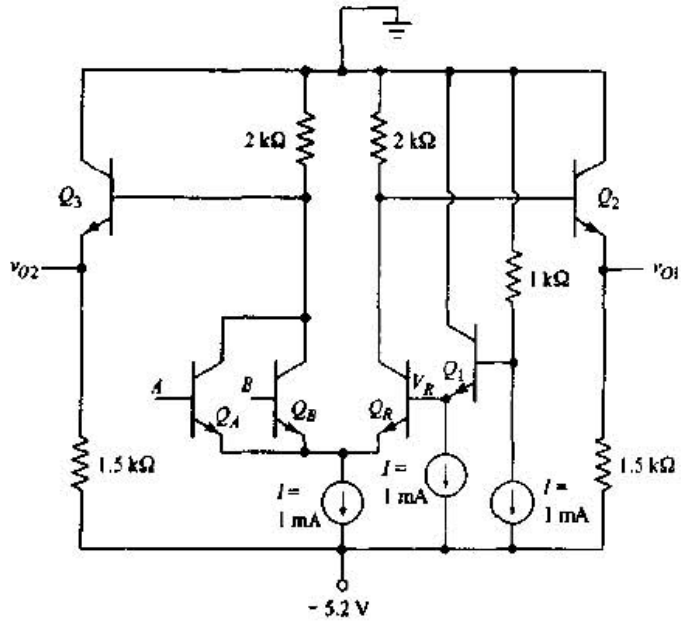


Figure P17.7

17.8 A positive-voltage-supply ECL logic gate is shown in Figure P17.8. Neglect base currents. (a) What logic function is performed by this circuit. (b) What are the logic 1 and logic 0 values of v_2 at the output? (c) When v_1 = logic 0 for one of the three inputs, determine i_{E1}, i_{E2}, i_{C3}, i_{C2}, and v_2. (d) Repeat part (c) when v_1 = logic 1 for all three inputs.

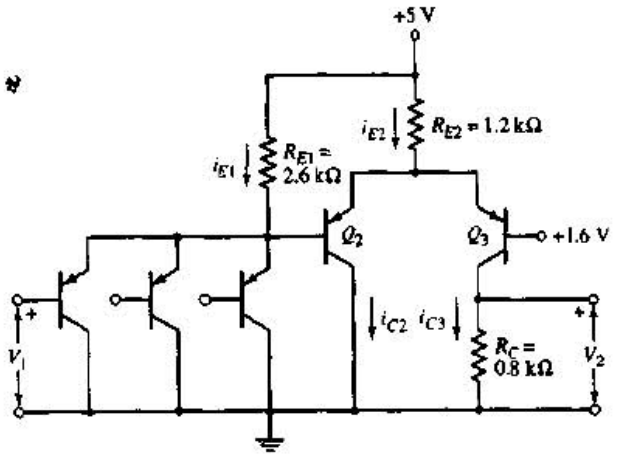


Figure P17.8

Section 17.2 Modified ECL Circuit Configurations

D17.9 In the circuit in Figure P17.9, the output voltages v_{O1} and v_{O2} are compatible with the input voltages v_X and v_Y. Neglect base currents. (a) Design an appropriate value of V_R. State the reason for your selection. (b) Determine R_{C1} such that when Q_1 is on, the current in R_{C1} is the same as the current in D_1. (c) Determine R_{C2} such that when Q_2 is on, the current in R_{C2} is the same as the current in D_2. (d) Calculate the power dissipated in the circuit when v_X = logic 0 and v_Y = logic 1.

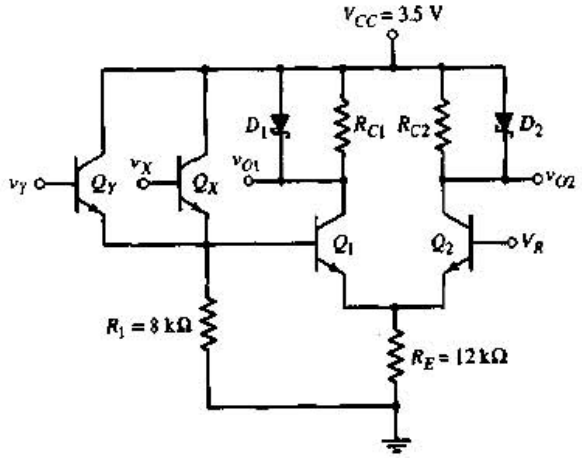


Figure P17.9

17.10 Consider the circuit in Figure P17.10. Neglect base currents. (a) What are the logic 1 and logic 0 voltage levels at the output terminals v_{O1} and v_{O2}? (b) When $v_X = v_Y$ = logic 0, the current i_E is to be 0.8 mA. Determine R_E. (c) Using the results

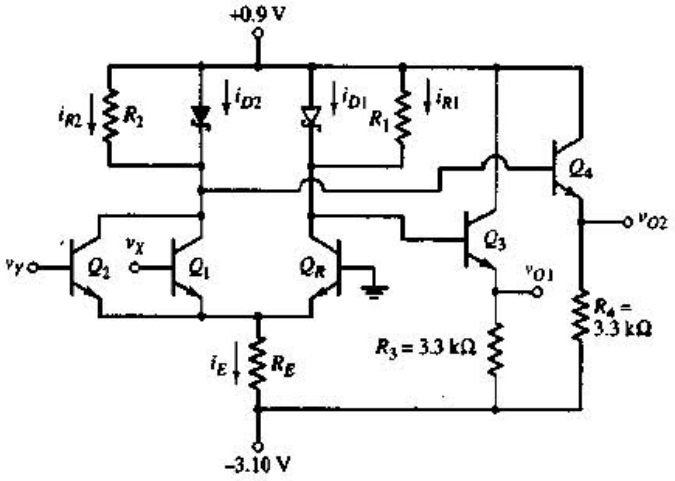


Figure P17.10

of part (b), determine R_1 such that $i_{D1} = R_{R1}$ when Q_R is conducting. (d) If $R_1 = R_2$, determine i_{R2} and i_{D2} for Q_1 and Q_2 conducting. (e) For $v_X = v_Y =$ logic 1, calculate the power dissipated in the circuit.

17.11 For the circuit in Figure P17.11, assume transistor and diode parameters of $V_{BE}(\text{on}) = 0.7\,\text{V}$ and $V_\gamma = 0.4\,\text{V}$. Neglect base currents. Find i_1, i_2, i_3, i_4, i_D, and v_O for: (a) $v_X = v_Y = -0.4\,\text{V}$, (b) $v_X = 0$, $v_Y = -0.4\,\text{V}$, (c) $v_X = -0.4\,\text{V}$, $v_Y = 0$, (d) $v_X = v_Y = 0$.

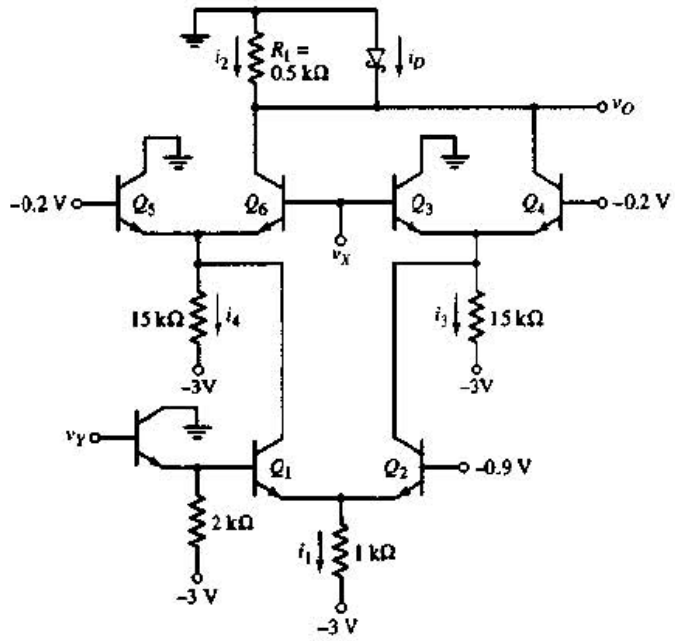


Figure P17.11

17.12 Assume the inputs A, B, C, and D to the circuit in Figure P17.12 are either 0 or 2.5 V. Let the B–E turn-on voltage be 0.7 V for both the npn and pnp transistors. Assume $\beta = 120$ for the npn devices and $\beta = 50$ for the pnp devices. (a) Determine the voltage at Y for: (i) $A = B = C = D = 0$, and (ii) $A = C = 0$, $B = D = 2.5\,\text{V}$. (b) What logic function does this circuit implement?

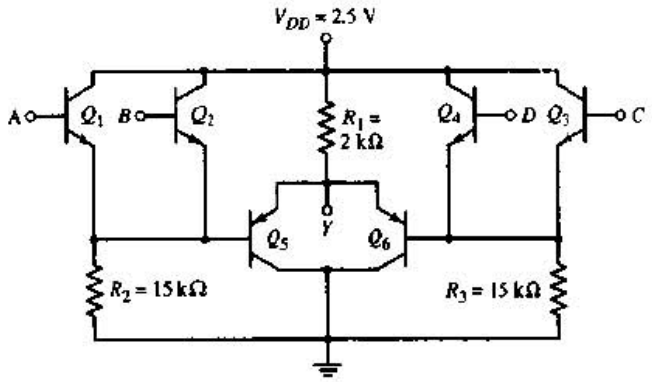


Figure P17.12

17.13 The input and output voltage levels for the circuit in Figure P17.13 are compatible. (a) What are the logic 0 and logic 1 voltage levels? (b) What are the logic functions implemented by this circuit at v_{O1}, v_{O2}, and v_{O3}?

17.14 Consider the circuit in Figure P17.14. (a) Explain the operation of the circuit. Demonstrate that the circuit functions as a clocked D flip-flop. (b) Neglecting base currents, if $i_{DC} = 50\,\mu$A, calculate the maximum power dissipated in the circuit.

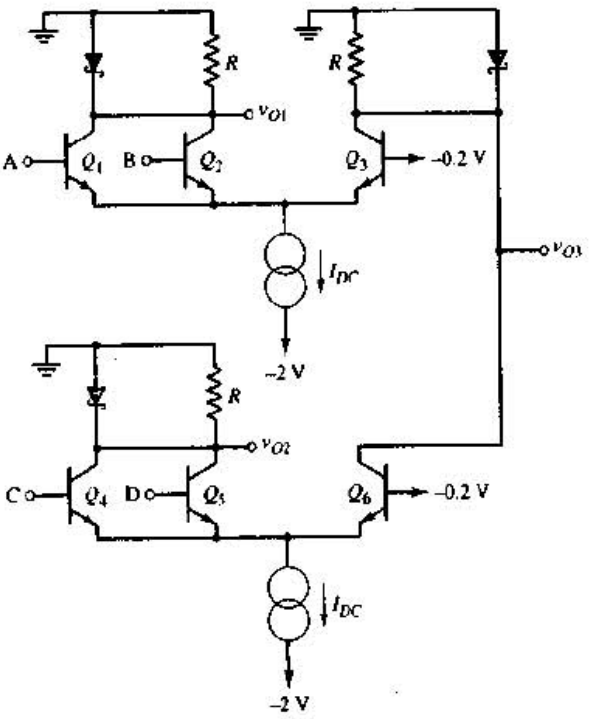


Figure P17.13

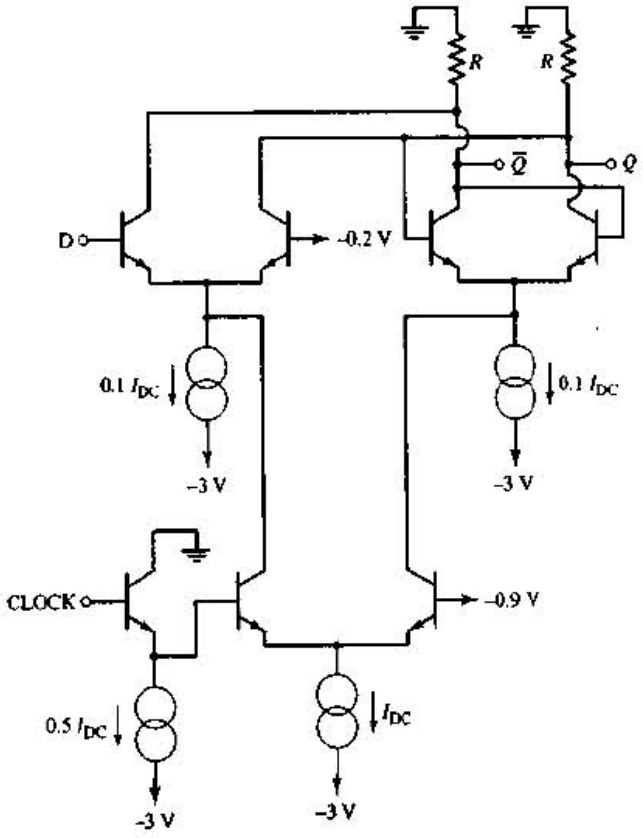


Figure P17.14

Section 17.3 Transistor–Transistor Logic

17.15 In Figure P17.15, the transistor current gain is $\beta = 20$. Find the currents and voltages i_1, i_3, i_4, and v' for the input conditions: (i) $v_X = v_Y = 0.10\,\text{V}$, and (ii) $v_X = v_Y = 5\,\text{V}$.

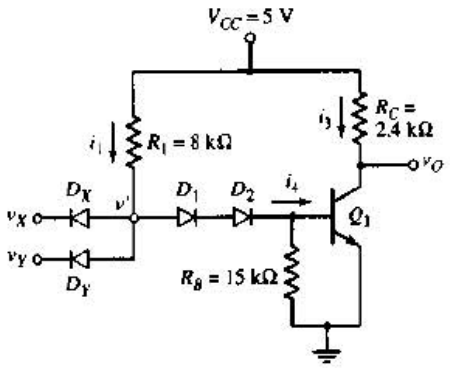


Figure P17.15

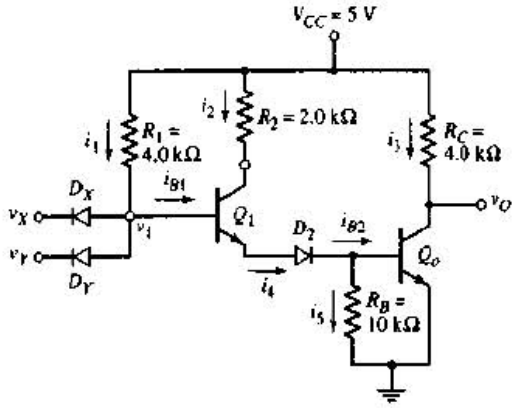


Figure P17.16

17.16 Figure P17.16 shows an improved version of the DTL circuit. One offset diode is replaced by transistor Q_1, providing increased current drive to Q_o. Assume $\beta = 20$ for both transistors. (a) For $v_X = v_Y = 5\,\text{V}$, determine the currents and voltages listed in the figure. (b) Calculate the maximum fanout for the low output condition.

17.17 For the modified DTL circuit in Figure P17.17, calculate the indicated currents in the figure for $v_X = v_Y = 5\,\text{V}$.

17.18 For the transistors in the TTL circuit in Figure P17.18, the parameters are $\beta_F = 20$ and $\beta_R = 0$. (a) Determine the currents i_1, i_2, i_3, i_4, i_{B2}, and i_{B3} for the following input conditions: (i) $v_X = v_Y = 0.1\,\text{V}$, and (ii) $v_X = v_Y = 5\,\text{V}$. (b) Show that for $v_X = v_Y = 5\,\text{V}$, transistors Q_2 and Q_3 are biased in saturation.

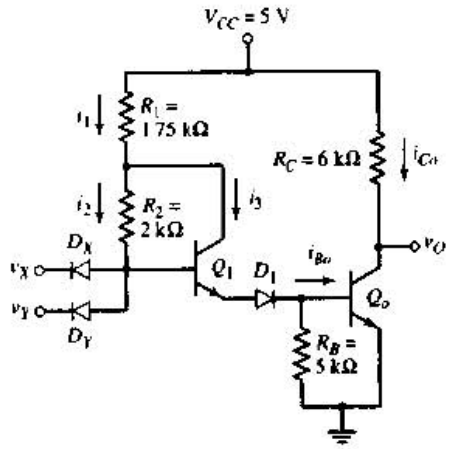


Figure P17.17

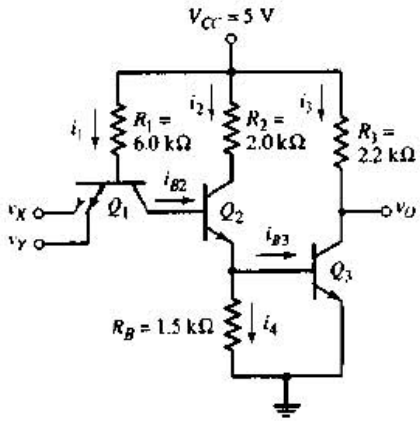


Figure P17.18

17.19 Reconsider the circuit in Figure P17.15. (a) Calculate the maximum fanout for the output low condition for the condition that Q_1 remains in saturation. (b) If the maximum collector current in Q_1 is limited to 5 mA, determine the maximum fanout for the low output condition.

17.20 In the TTL circuit in Figure P17.20, the transistor parameters are $\beta_F = 20$ and $\beta_R = 0.10$ (for each input emitter). (a) Calculate the maximum fanout for $v_X = v_Y = 5\,\text{V}$. (b) Calculate the maximum fanout for $v_X = v_Y = 0.1\,\text{V}$. (Assume v_O is allowed to decrease by 0.10 V from the no-load condition.)

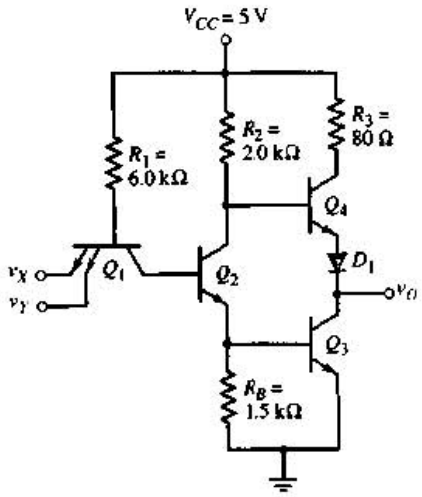


Figure P17.20

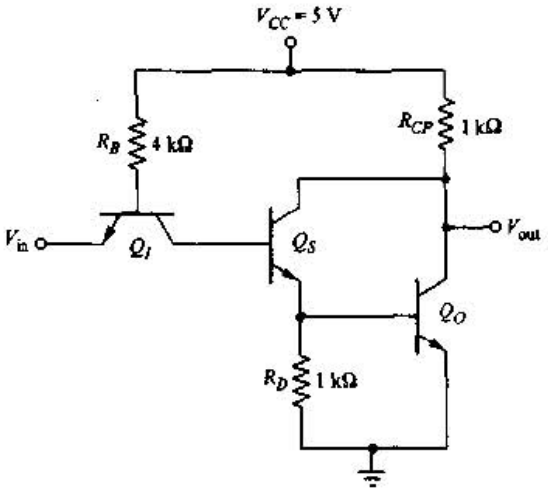


Figure P17.21

17.21 For the TTL circuit in Figure P17.21, assume parameters of $\beta_F = 50$, $\beta_R = 0.1$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, $V_{BE}(\text{sat}) = 0.8\,\text{V}$, and $V_{CE}(\text{sat}) = 0.1\,\text{V}$. Determine the power dissipated in the circuit (no load condition) for (a) $V_{\text{in}} = 0.1\,\text{V}$ and (b) $V_{\text{in}} = 5\,\text{V}$.

17.22 Consider the basic TTL logic gate in Figure P17.22 with a fanout of 5. Assume transistor parameters of $\beta_F = 50$ and $\beta_R = 0.5$ (for each input emitter). Calculate the base and collector currents in each transistor for: (a) $v_X = v_Y = v_Z = 0.1\,\text{V}$, and (b) $v_X = v_Y = v_Z = 5\,\text{V}$.

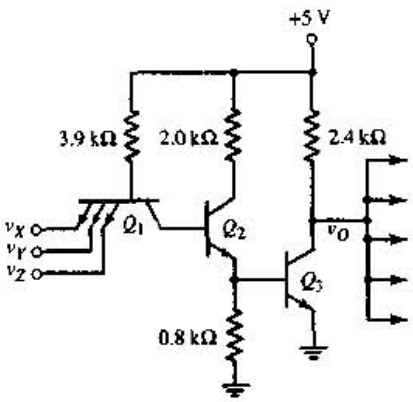


Figure P17.22

17.23 For the transistors in the TTL circuit in Figure P17.23, the parameters are $\beta_F = 100$ and $\beta_R = 0.3$ (for each input emitter). (a) For $v_X = v_Y = v_Z = 2.8\,\text{V}$, determine i_{B1}, i_{B2}, and i_{B3}. (b) For $v_X = v_Y = v_Z = 0.1\,\text{V}$, determine i_{B1} and i_{B4} for a fanout of 5.

17.24 A low-power TTL logic gate with an active pnp pull-up device is shown in Figure P17.24. The transistor parameters are $\beta_F = 100$ and $\beta_R = 0.2$ (for each input emitter). Assume a fanout of 5. (a) For $v_X = v_Y = v_Z = 0.1\,\text{V}$, determine i_{B1}, i_{B2}, i_{B3}, i_{C2}, and i_{C3}. (b) Repeat part (a) for $v_X = v_Y = v_Z = 2\,\text{V}$.

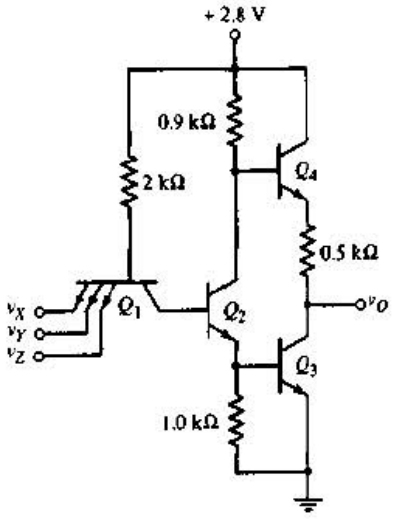


Figure P17.23

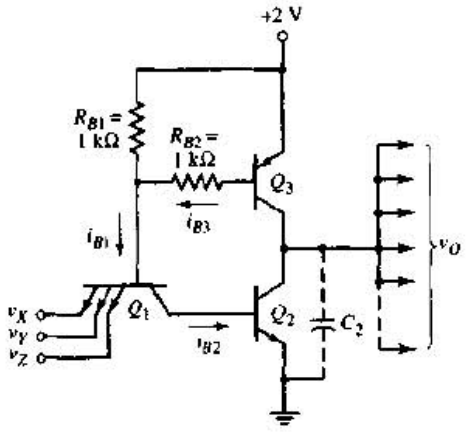


Figure P17.24

Section 17.4 Schottky Transistor–Transistor Logic

17.25 Consider the Schottky transistor circuit in Figure P17.25. Assume parameter values of $\beta = 50$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, and $V_\gamma = 0.3\,\text{V}$ for the Schottky diode. (a) Determine I_B, I_D, I_C, and V_{CE}. (b) Remove the Schottky diode and repeat part (a) assuming additional parameter values of $V_{BE}(\text{sat}) = 0.8\,\text{V}$ and $V_{CE}(\text{sat}) = 0.1\,\text{V}$.

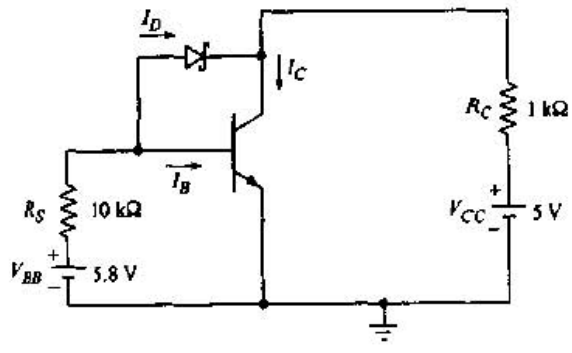


Figure P17.25

17.26 Consider the Schottky TTL circuit in Figure 17.33. The transistor parameters are $\beta_F = 30$ and $\beta_R = 0.1$ (for each emitter). (a) Determine all base currents, collector currents, and node voltages for $v_X = v_Y = 0.4\,\text{V}$. (b) Repeat part (a) for $v_X = v_Y = 3.6\,\text{V}$.

17.27 A modified Schottky TTL NAND gate is shown in Figure P17.27. The current gain of all transistors is $\beta = 50$. (a) With all inputs high and only one load connected, Q_2 is biased in saturation and $i_{B2} = i_{C2} = 0.5\,\text{mA}$. Determine the values of R_{B1} and R_{C1}. (b) With all inputs at logic 0 and with one load circuit, calculate v_{B1}, v_{C2}, and all base and collector currents. (c) With all inputs at logic 1 and with one load circuit, calculate v_{B1}, v_{C1}, and all base and collector currents. (d) Determine the maximum fanout for a low output state.

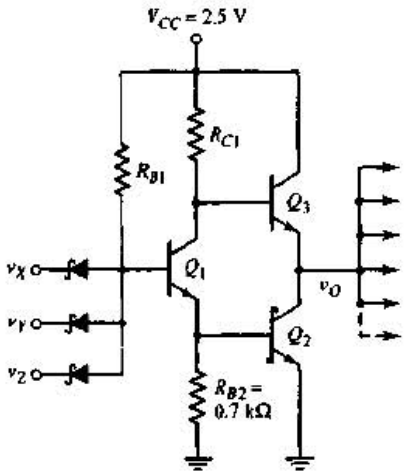


Figure P17.27

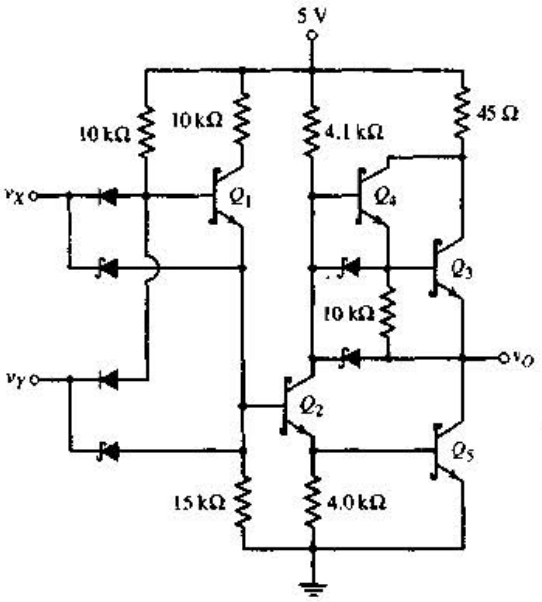


Figure P17.28

17.28 A low-power Schottky TTL logic circuit is shown in Figure P17.28. Assume a transistor current gain of $\beta = 30$ for all transistors. (a) Calculate the maximum fanout for $v_X = v_Y = 3.6$ V. (b) Using the results of part (a), determine the power dissipated in the circuit for $v_X = v_Y = 3.6$ V.

17.29 For all transistors in the circuit in Figure 17.35, the current gain is $\beta = 50$. (a) Calculate the power dissipation in the circuit when the input is at logic 0. (b) Repeat part (a) when the input is at logic 1. (c) Calculate the output short-circuit current. (Assume the input is a logic 0 and the output is inadvertently shorted to ground.)

Section 17.5 BiCMOS Digital Circuits

17.30 Consider the basic BiCMOS inverter in Figure 17.36(a). Assume circuit and transistor parameters of $V_{DD} = 5$ V, $K_n = K_p = 0.1\,\text{mA/V}^2$, $V_{TN} = +0.8$ V, $V_{TP} = -0.8$ V, and $\beta = 50$. (a) For $v_I = v_O = 2.5$ V, determine the current in each transistor. (b) If the current calculated for Q_1 were charging a 15 pF load capacitance, how long would it take to charge the capacitance from 0 to 5 V? (c) Repeat part (b) for the current in the transistor M_p.

17.31 Repeat Problem 17.30 for the BiCMOS inverter shown in Figure 17.36(b).

COMPUTER SIMULATION PROBLEMS

17.32 Consider the modified ECL logic circuit in Figure 17.17. Using PSpice, generate the voltage transfer characteristics and determine the power dissipation. Investigate the transfer characteristics at several temperatures.

17.33 Using PSpice, generate the voltage transfer characteristics of the DTL logic circuit shown in Figure 17.20.

17.34 Repeat Problem 17.32 for the TTL logic circuit in Figure 17.27. In addition, investigate the propagation delay time of this TTL circuit for one load circuit and for five load circuits connected to the output.

17.35 Repeat Problem 17.34 for the low-power Schottky TTL NAND logic circuit shown in Figure 17.34.

DESIGN PROBLEMS

***D17.36** Design an ECL R–S flip-flop.

***D17.37** Design an ECL series gating logic circuit, similar to the one shown in Figure 17.16, that will implement the logic functions: (a) $Y = [\overline{A + (B \cdot C)}]$, and (b) $Y = [\overline{(A + B) \cdot (C + D)}]$.

***D17.38** Design a clocked D flip-flop, using a modified ECL circuit design, such that the output becomes valid on the negative-going edge of the clock signal.

***D17.39** Design a low-power Schottky TTL exclusive-OR logic circuit.

***D17.40** Design a TTL R–S flip-flop.

APPENDIX

A

Physical Constants and Conversion Factors

General Constants and Conversion Factors

Angstrom	Å	$1\ Å = 10^{-4}\ \mu m = 10^{-8}\ cm = 10^{-10}\ m$
Boltzmann's constant	k	$k = 1.38 \times 10^{-23}\ J/K = 8.6 \times 10^{-5}\ eV/K$
Electron-volt	eV	$1\ eV = 1.6 \times 10^{-19}\ J$
Electronic charge	e or q	$q = 1.6 \times 10^{-19}\ C$
Micron	μm	$1\ \mu m = 10^{-4}\ cm = 10^{-6}\ m$
Mil		$1\ mil = 0.001\ in. = 25.4\ \mu m$
Nanometer	nm	$1\ nm = 10^{-9}\ m = 10^{-3}\ \mu m = 10\ Å$
Permittivity of free space	ε_o	$\varepsilon_o = 8.85 \times 10^{-14}\ F/cm$
Permeability of free space	μ_o	$\mu_o = 4\pi \times 10^{-9}\ H/cm$
Planck's constant	h	$h = 6.625 \times 10^{-34}\ J\text{-}s$
Thermal voltage	V_T	$V_T = kT/q \cong 0.026\ V$ at 300 °K
Velocity of light in free space	c	$c = 2.998 \times 10^{10}\ cm/s$

Semiconductor Constants

	Si	Ge	GaAs	SiO_2
Relative dielectric constant	11.7	16.0	13.1	3.9
Bandgap energy, E_g(eV)	1.1	0.66	1.4	
Intrinsic carrier concentration, n_i (cm^{-3} at 300 °K)	1.5×10^{10}	2.4×10^{13}	1.8×10^{6}	

APPENDIX

B

Introduction to PSpice

B.0 PREVIEW

Several computer software packages enhance electronic analysis and design. SPICE, an acronym for **S**imulation **P**rogram with **I**ntegrated **C**ircuit **E**mphasis, is by far the most widely used computer simulation program for elecronic circuits. The program was first developed by the University of California at Berkeley in the mid-1970s. The original version was used on mainframe computers, but many upgrades have been developed, including versions written for the personal computer. These programs are generally referred to as PSpice (the prefix P denoting the personal computer). Relatively simple and inexpensive PSpice versions, generally referred to as student versions, are available.

The 8.0 student version from MicroSim Corporation was used in this text. More sophisticated programs included in SPICE, such as a Monte Carlo analysis, are not usually available in the student versions. However, this version is adequate for conducting basic PSpice analyses of transistor circuits. As mentioned in the Preface, the computer simulation should be used in conjunction with hand analyses and to fine-tune a circuit design.

Electronic circuit design generally begins by systematically combining various subcircuits, using relatively simple mathematical models of transistors. These models enable the designer to determine if the circuit can potentially meet the required specifications. However, a complex IC design generally requires a computer analysis that incorporates sophisticated device models. This prefabrication phase of the design process is important because any changes in the IC design after fabrication are expensive. A computer simulation can minimize design errors.

This appendix is intended to provide a basic description of PSpice. A few examples are included to illustrate various simulation analyses. The references listed in Appendix E will provide much more comprehensive descriptions of PSpice, as well as more detailed model parameters of diodes and transistors.

B.1 INTRODUCTION

There are three major programs to this version of PSpice: *Schematics*, *PSpice*, and *Probe*. Schematics is the program that lets you draw the circuit on the screen. PSpice is the program that analyzes the circuit created in Schematics and generates voltages and currents. The combination of Schematics and PSpice eliminates the need to create a netlist before an analysis can be

performed. Probe is a graphics program that generates plots of specified circuit parameters such as currents and voltages.

The description in this appendix assumes that the software has already been installed.

B.2 DRAWING THE CIRCUIT

To begin, open the Schematics program. A blank page may appear or the page may have a grid that looks like engineering paper. At the top of the page is a menu bar. Drawing the circuit begins by selecting components from a library. Resistors, inductors, capacitors, and power supplies are available. In addition, a large number of standard transistors, op-amps, and digital components are available.

The mouse is an important tool in drawing the circuit. A single click selects an item, either a menu item or a device in the circuit. A double click with the left mouse button performs an action, such as editing a selection or ending an operation. To drag a selected item, click on the item with the left mouse button, and then, holding the button down, drag the item to a new location. Release the button when the item has been placed.

The steps in drawing a circuit are as follows:

1. A component is chosen from the **Get New Part** menu. Drag the component to the drawing board and place it in an appropriate position.
2. The component may be rotated or flipped by using the **Edit** menu to place the item in the proper orientation.
3. Components can be wired together by choosing **Wire** from the menu. The cursor will change to a pencil shape. Click the left mouse button with the pencil on one terminal of a device and drag the pencil to the terminal of another device. Double click to end this mode of operation.
4. Components can be relabeled by clicking on the item label (such as R, L, or Q). An **Edit Preference Designator** box will appear. Type in the new label and click on the OK.
5. The attributes of the items can be changed by clicking on the item value (such as 1K, 10μF, etc.). A **Set Attribute Value** box will appear. Type in the new value and click on the OK button.
6. Be sure to include a ground connection in the circuit.
7. Save the schematic.

B.3 TYPE OF ANALYSIS

The **Setup** command from the **Analysis** menu allows you to choose the type of circuit analysis to be performed. The most common types of simulations are dc bias point, dc sweep analysis, ac sweep analysis, and transient analysis.

The *dc bias point analysis* calculates all the dc nodal voltages and also calculates all electronic device quiescent values. This analysis includes determining transistor quiescent currents and voltages. As part of this analysis, the small signal parameters are determined for the electronic devices.

The *dc sweep analysis* involves allowing the voltage of a particular source to vary over a range of values with a given increment. The current through a

particular component or the voltage at a given node can then be measured as the source voltage changes. This analysis can be used in diode or transistor circuits to determine the "proper" dc voltages that need to be applied.

The *ac sweep analysis* performs a frequency analysis of the circuit by varying the input signal frequency over a range of values with a given increment. A linear, decade, or octave frequency scale can be chosen. This analysis can be used to determine the bandwidth of an amplifier.

The *transient analysis* determines the circuit response as a function of time. The start and end times as well as the time increment can be chosen. This analysis can be used to determine propagation delay times in digital circuits, for example.

B.4 DISPLAYING RESULTS OF SIMULATION

Probe is the program that allows the simulation results to be graphically displayed. A voltage level or current level marker is placed at the point in the circuit where the voltage or current is to be measured. To use Probe, select Run Probe from the **Analysis** menu. From the Probe setup options, Probe can be automatically run after a simulation. Probe will open with an initial graph in which the axes are automatically set.

B.5 EXAMPLE ANALYSES

The following three examples illustrate the various types of analyses.

Example B.1 **Objective:** Determine the dc operating point and the dc transfer characteristics of a diode circuit.

The dc bias voltages will be determined for the circuit in Figure B.1 for an input voltage of 3 V, and then the output voltage will be measured as the input voltage is swept between −2 and +6 V. Standard IN4002 diodes are used in the circuit.

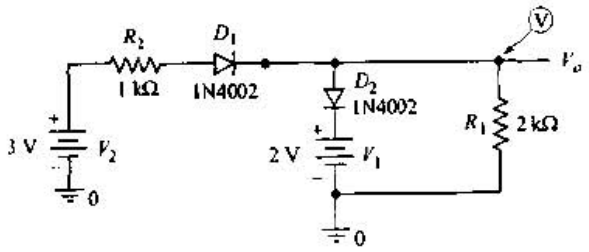


Figure B.1 Diode circuit for Example B.1

DC Analysis: The results of the dc analysis with the input voltage set at 3 V show that the output voltage is 1.625 V, which means that the diode D_2 is reverse biased. Listed in Table B.1 are the quiescent currents and voltages of the two diodes. As indicated, the current and voltage of the diode D_2 are for a reverse-biased diode.

Table B.1 Quiescent diode parameters for Example B.1

NAME	D_D1	D_D2
MODEL	D1N4002	D1N4002
ID	8.13E-04	-1.42E-08
VD	5.62E-01	-3.75E-01
REQ	6.31E+01	4.35E+09

DC Voltage Sweep: The dc sweep analysis was chosen from the **Setup** command in the **Analysis** menu. The input voltage V_2 was set to sweep from −2 to +6 V. A voltage level marker was placed at the output node, as shown in the figure, to measure the output voltage. The Probe pogram was set to run automatically after the simulation.

Figure B.2 shows the analysis results. The output voltage begins to increase when the input voltage is approximately 0.4 V, indicating that the diode D_1 has begun to conduct. When the input voltage reaches approximately 4.5 V, the output voltage tends to reach a maximum value, indicating that diode D_2 has turned on. Since the output voltage is not exactly a constant, this result shows that the voltage across the diode does increase slightly as the current through the diode increases.

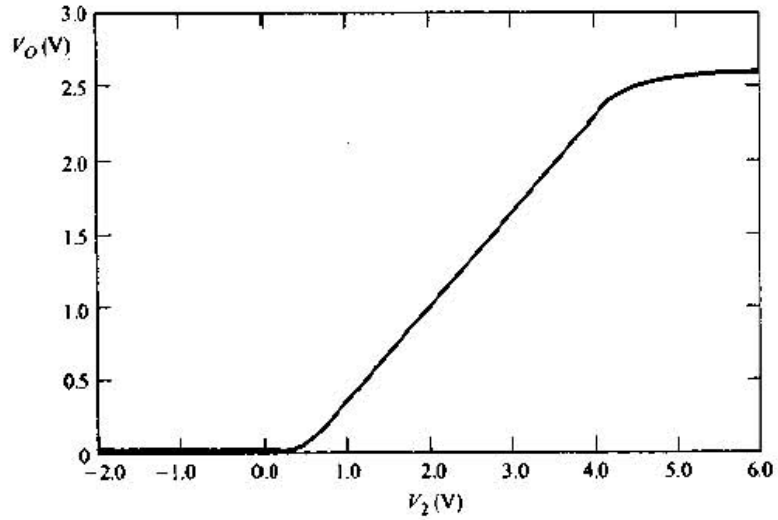


Figure B.2 DC voltage transfer characteristics of the diode circuit in Example B.1

Example B.2 **Objective:** Determine the input resistance and small-signal voltage gain versus frequency of a common-emitter amplifier.

This analysis is an example of a steady-state sinusoidal frequency analysis.

A common-emitter circuit is shown in Figure B.3. A standard 2N3904 npn bipolar transistor is used in the circuit. A 10 mV, 1 kHz ac signal is initially applied at the input. The input coupling capacitor is 1 μF, the output load capacitor is 15 pF, and the emitter-bypass capacitor is 1 kF, which means that it is essentially a short circuit to all signal currents and voltages.

DC Analysis: A dc analysis was initially performed to ensure that the bipolar transistor was biased in the forward active region. The model parameters of the 2N3904

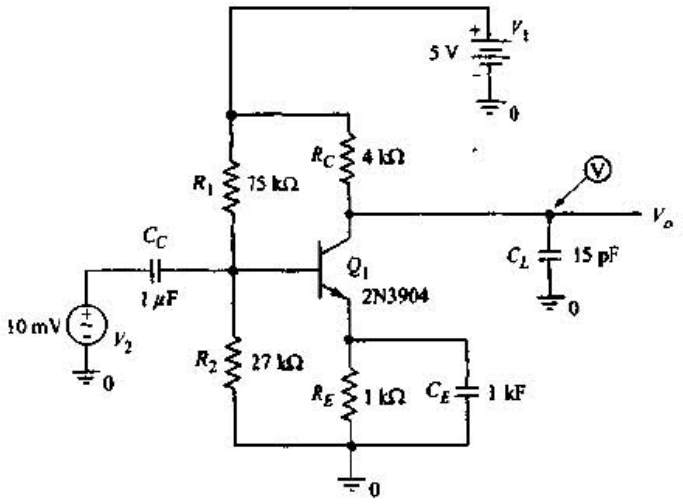


Figure B.3 Figure for Example B.2

transistor and the quiescent characteristics of the transistor are listed in Table B.2. The quiescent collector current is 0.577 mA and the quiescent collector-emitter voltage is 2.11 V, which means that the transistor is indeed biased in the forward active region.

Input Resistance: A current level marker was placed at the node of the input voltage source. With a 1 kHz, 10 mV input signal applied, the input current was measured to be

Table B.2 Model parameters and quiescent characteristics of the transistor in Example B.2

	Model parameters	Quiescent characteristics	
	Q2N3904		
	NPN	NAME	Q_Q1
IS	6.734000E-15	MODEL	Q2N3904
BF	416.4	IB	4.59E-06
NF	1	IC	5.77E-04
VAF	74.03	VBE	6.51E-01
IKF	.06678	VBC	-1.46E+00
ISE	6.734000E-15	VCE	2.11E+00
NE	1.259	BETADC	1.26E+02
BR	.7371	GM	2.21E-02
NR	1	RPI	6.58E+03
RB	10	RX	1.00E+01
RC	1	RO	1.31E+05
CJE	4.493000E-12	CBE	1.31E-11
MJE	.2593	CBC	2.61E-12
CJC	3.638000E-12	CJS	0.00E+00
MJC	.3085	BETAAC	1.46E+02
TF	301.200000E-12	CBX	0.00E+00
XTF	2	FT	2.25E+08
VTF	4		
ITF	.4		
TR	239.500000E-09		
XTB	1.5		

2.03 μA. The input resistance is then found to be 4.93 kΩ. This agrees very well with calculated values of $R_1 \| R_2 \| r_\pi$. The value of r_π is given in Table B.2.

AC Sweep Analysis: The frequency of the input signal source was swept from 1 Hz to 100 MHz with 100 data points calculated per decade of frequency. The magnitude of the output voltage, plotted on a log scale, is shown in Figure B.4(a) for the case when a 15 pF capacitor is included in the output. The lower corner frequency, which is a function of the coupling capacitor, is approximately 30 Hz, and the upper corner frequency, which is a function of the load capacitor, is approximately 30 MHz. The midband voltage gain is (0.85 V)/(0.01 V) = 85.

The frequency response for the case when the load capacitance is set equal to zero is shown in Figure B.4(b). The upper corner frequency is now a result of the transistor capacitances and the effective Miller capacitance. The transistor capacitances were determined for this transistor during the dc analysis and are listed in Table B.2.

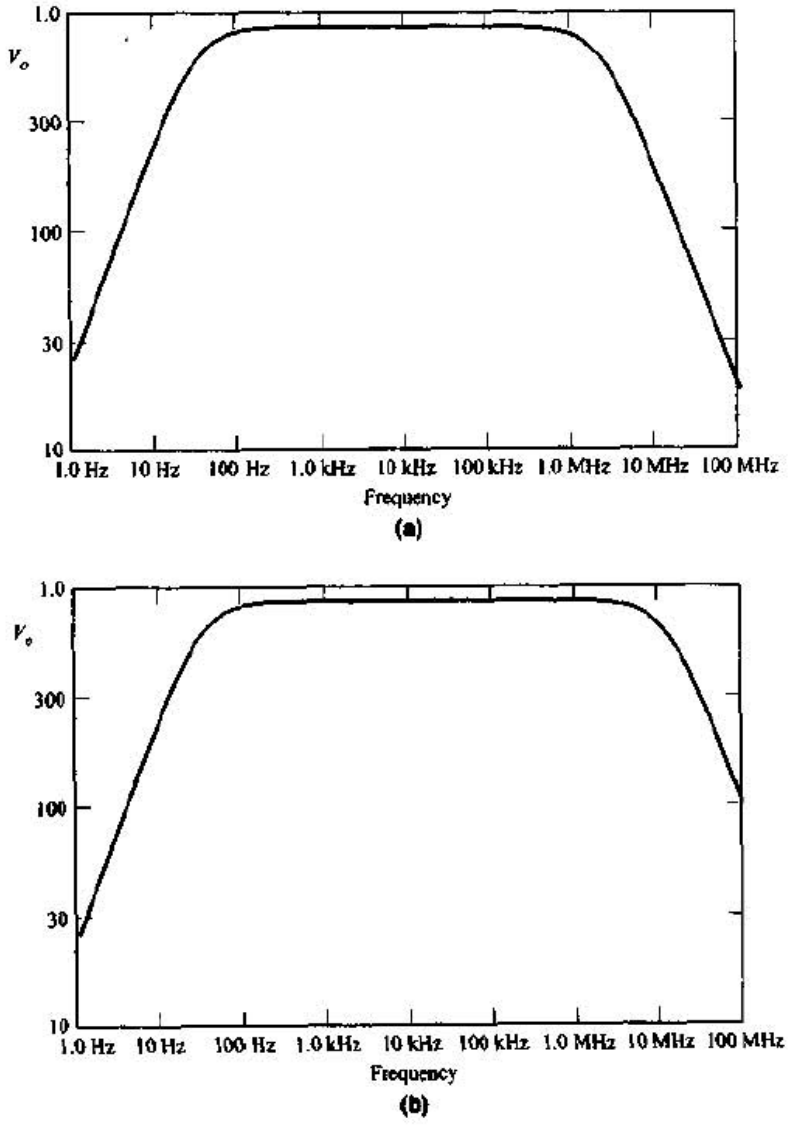


Figure B.4 Output voltage versus frequency for the circuit in Example B.2: (a) load capacitance is 15 pF and (b) load capacitance is zero

Example B.3 **Objective:** Determine the transient response of cascaded CMOS inverters.

A series of three CMOS inverters is shown in Figure B.5. The input voltage is a 5 V pulse lasting 400 ns. Capacitances are shown at the output of each inverter. These capacitors model the transistor capacitances as well as any interconnect capacitance. The capacitance values are larger than typical IC capacitance values, but are used to illustrate this type of analysis.

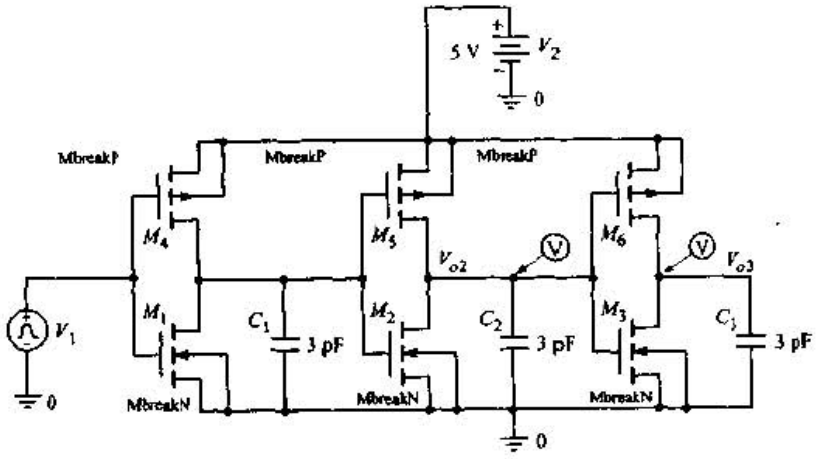


Figure B.5 CMOS inverter circuit in Example B.3

The voltages at the outputs of the second and third inverters, V_{o2} and V_{o3}, were measured as a function of time. These curves are shown in Figure B.6. This type of measurement is useful in determining propagation delay times. At the midpoint voltage of 2.5 V, there is a delay between the voltage of the third inverter compared to that of the second inverter. These time delays are referred to as propagation delay times and are important parameters in digital circuits.

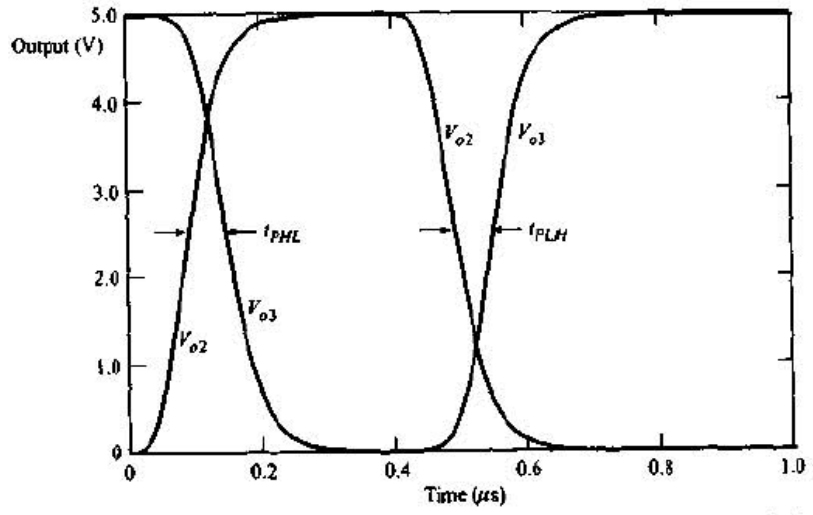


Figure B.6 Voltage versus time at the outputs of the second and third inverters of the circuit for Example B.

APPENDIX

C

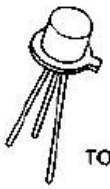
Selected Manufacturers' Data Sheets

This appendix contains data sheets representative of transistors and op-amps. This appendix is not meant as a substitute for the appropriate data books. In some cases, therefore, only selected information is presented. These data sheets are provided courtesy of National Semiconductor.

CONTENTS

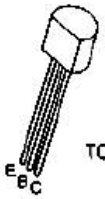
National Semiconductor

2N2222
2N2222A



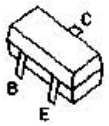
TO-18

PN2222
PN2222A



TO-92

MMBT2222
MMBT2222A



TO-236
(SOT-23)

MPQ2222

TO-116

NPN General Purpose Amplifier

Electrical Characteristics T_A = 25 °C unless otherwise noted

Symbol	Parameter		Min	Max	Units
OFF CHARACTERISTICS					
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage (Note 1) (I_C = 10 mA, I_B = 0)	2222 2222A	30 40		V
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage (I_C = 10 µA, I_E = 0)	2222 2222A	60 75		V
$V_{(BR)EBO}$	Emitter Base Breakdown Voltage (I_E = 10 µA, I_C = 0)	2222 2222A	5.0 6.0		V
I_{CEX}	Collector Cutoff Current (V_{CE} = 60 V, $V_{EB(OFF)}$ = 3.0 V)	2222A		10	nA
I_{CBO}	Collector Cutoff Current (V_{CB} = 50 V, I_E = 0) (V_{CB} = 60 V, I_E = 0) (V_{CB} = 50 V, I_E = 0, T_A = 150 °C) (V_{CB} = 60 V, I_E = 0, T_A = 150 °C)	2222 2222A 222 2222A		0.01 0.01 10 10	µA
I_{EBO}	Emitter Cutoff Current (V_{EB} = 3.0 V, I_C = 0)	2222A		10	nA
I_{BL}	Base Cutoff Current (V_{CE} = 60 V, $V_{EB(OFF)}$ = 3.0)	2222A		20	nA
ON CHARACTERISTICS					
h_{FE}	DC Current Gain (I_C = 0.1 mA, V_{CE} = 10 V) (I_C = 1.0 mA, V_{CE} = 10 V) (I_C = 10 mA, V_{CE} = 10 V) (I_C = 10 mA, V_{CE} = 10 V, T_A = −55 °C) (I_C = 150 mA, V_{CE} = 10 V) (Note 1) (I_C = 150 mA, V_{CE} = 1.0 V) (Note 1) (I_C = 500 mA, V_{CE} = 10 V) (Note 1)	 2222 2222A	35 50 75 35 100 50 30 40	 300 	

Note 1: Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%

NPN General Purpose Amplifier (Continued)

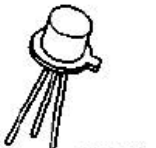
Electrical Characteristics T_A = 25 °C unless otherwise noted (Continued)

Symbol	Parameter		Min	Max	Units
ON CHARACTERISTICS (Continued)					
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage (Note 1) (I_C = 150 mA, I_B = 15 mA)	2222 2222A		0.4 0.3	V
	(I_C = 500 mA, I_B = 50 mA)	2222 2222A		1.6 1.0	
$V_{BE(sat)}$	Base-Emitter Saturation Voltage (Note 1) (I_C = 150 mA, I_B = 15 mA)	2222 2222A	0.6 0.8	1.3 1.2	V
	(I_C = 500 mA, I_B = 50 mA)	2222 2222A		2.6 2.0	
SMALL-SIGNAL CHARACTERISTICS					
f_T	Current Gain—Bandwidth Product (Note 3) (I_C = 20 mA, V_{CE} = 20 V, f = 100 MHz)	2222 2222A	250 300		MHz
C_{obo}	Output Capacitance (Note 3) (V_{CB} = 10 V, I_E = 0, f = 100 kHz)			8.0	pF
C_{ibo}	Input Capacitance (Note 3) (V_{EB} = 0.5 V, I_C = 0, f = 100 kHz)	2222 2222A		30 25	pF
$r_b'C_C$	Collector Base Time Constant (I_E = 20 mA, V_{CB} = 20 V, f = 31.8 MHz)	2222A		150	ps
NF	Noise Figure (I_C = 100 µA, V_{CE} = 10V, R_S = 1.0 kΩ, f = 1.0 kHz)	2222A		4.0	dB
$Re(h_{ie})$	Real Part of Common-Emitter High Frequency Input Impedance (I_C = 20 mA, V_{CE} = 20 V, f = 300 MHz)			60	Ω
SWITCHING CHARACTERISTICS					
t_D	Delay Time	(V_{CC} = 30 V, $V_{BE(OFF)}$ = 0.5 V, I_C = 150 mA, I_{B1} = 15 mA) except MPQ2222		10	ns
t_R	Rise Time			25	ns
t_S	Storage Time	(V_{CC} = 30 V, I_C = 150 mA, I_{B1} = I_{B2} = 15 mA) except MPQ2222		225	ns
t_F	Fall Time			60	ns

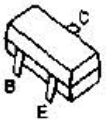
Note 1: Pulse Test: Pulse Width < 300 µs, Duty Cycle ≤ 2.0%.
Note 2: For characteristics curves, see Process 19.
Note 3: f_T is defined as the frequency at which h_{fe} extrapolates to unity.

National Semiconductor

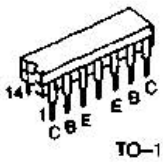
2N2907 2N2907A **PN2907 PN2907A** **MMBT2907 MMBT2907A** **MPQ2907**


TO-18

TO-92



TO-236 (SOT-23)



TO-116

PNP General Purpose Amplifier

Electrical Characteristics T_A = 25 °C unless otherwise noted

Symbol	Parameter		Min	Max	Units
OFF CHARACTERISTICS					
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage (Note 1) (I_C = 10 mAdc, I_B = 0)	2907 2907A	40 60		Vdc
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage (I_C = 10 μAdc, I_E = 0)		60		Vdc
$V_{(BR)EBO}$	Emitter Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)		5.0		Vdc
I_{CEX}	Collector Cutoff Current (V_{CE} = 30 Vdc, V_{BE} = 0.5 Vdc)			50	nAdc
I_{CBO}	Collector Cutoff Current (V_{CB} = 50 Vdc, I_E = 0) (V_{CB} = 50 Vdc, I_E = 0, T_A = 150 °C)	2907 2907A 2907 2907A		0.020 0.010 20 10	μAdc
I_B	Base Cutoff Current (V_{CE} = 30 Vdc, V_{EB} = 0.5 Vdc)			50	nAdc

PNP General Purpose Amplifier (Continued)

Electrical Characteristics T_A = 25 °C unless otherwise noted (Continued)

Symbol	Parameter		Min	Max	Units
ON CHARACTERISTICS					
h_{FE}	DC Current Gain				
	(I_C = 0.1 mAdc, V_{CE} = 10 Vdc)	2907	35		
		2907A	75		
	(I_C = 1.0 mAdc, V_{CE} = 10 Vdc)	2907	50		
		2907A	100		
	(I_C = 10 mAdc, V_{CE} = 10 Vdc)	2907	75		
		2907A	100		
	(I_C = 150 mAdc, V_{CE} = 10 Vdc) (Note 1)		100	300	
	(I_C = 500 mAdc, V_{CE} = 10 Vdc) (Note 1)	2907	30		
		2907A	50		
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage (Note 1)				
	(I_C = 150 mAdc, I_B = 15 mAdc)			0.4	Vdc
	(I_C = 500 mAdc, I_B = 50 mAdc)			1.6	
$V_{BE(sat)}$	Base-Emitter Saturation Voltage				
	(I_C = 150 mAdc, I_B = 15 mAdc), (Note 1)			1.3	Vdc
	(I_C = 500 mAdc, I_B = 50 mAdc)			2.6	
SMALL-SIGNAL CHARACTERISTICS					
f_T	Current Gain—Bandwidth Product (I_C = 50 mAdc, V_{CE} = 20 Vdc, f = 100 MHz)		200		MHz
C_{obo}	Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)			8.0	pF
C_{ibo}	Input Capacitance (V_{EB} = 2.0 Vdc, I_C = 0, f = 100 kHz)			30	pF
SWITCHING CHARACTERISTICS					
t_{on}	Turn-On Time	(V_{CC} = 30 Vdc, I_C = 150 mAdc, I_{B1} = 15 mAdc) Except MPQ2907		45	ns
t_d	Delay Time			10	ns
t_r	Rise Time			40	ns
t_{off}	Turn-Off Time	(V_{CC} = 6.0 Vdc, I_C = 150 mAdc, I_{B1} = I_{B2} = 15 mAdc) Except MPQ2907		100	ns
t_s	Storage Time			80	ns
t_f	Fall Time			30	ns

Note 1: Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

National Semiconductor

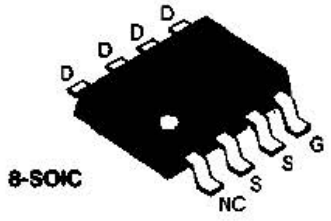
NDS9410
Single N-Channel Enhancement Mode Field Effect Transistor

General Description

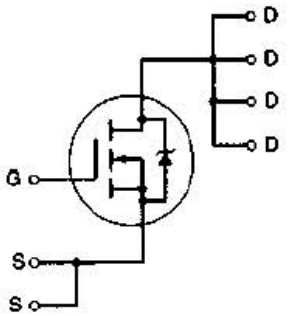
These N-channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited to low voltage applications such as laptop computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- 7.0A, 30V. $R_{DS(ON)} = 0.03\ \Omega$
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor
- High density cell design (3.8 million/in^2) for extremely low $R_{DS(ON)}$
- High power and current handling capability in a widely used surface mount package
- Critical DC electrical parameters specified at elevated temperature



8-SOIC



ABSOLUTE MAXIMUM RATINGS T_C = 25 °C unless otherwise noted

Symbol	Parameter	NDS9410	Units
V_{DSS}	Drain-Source Voltage	30	V
V_{DGR}	Drain-Gate Voltage ($R_{GS} \leq 1$ MΩ)	30	V
V_{GSS}	Gate-Source Voltage	±20	V
I_D	Drain Current – Continuous @ T_A = 25 °C	±7.0	A
	– Continuous @ T_A = 70 °C	±5.8	A
	– Pulsed	±20	A
P_D	Maximum Power Dissipation @ T_A = 25 °C	2.5 (Note 1)	W
$T_J T_{STG}$	Operating and Storage Temperature Range	-55 to 150	°C
THERMAL CHARACTERISTICS			
$R_{\theta JA}(t)$	Thermal Resistance, Junction-to-Ambient (Pulse = 10 seconds)	50 (Note 1)	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Steady-State)	100 (Note 2)	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25 °C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V			2	μA
		T_C = 125 °C			25	μA
I_{GSSF}	Gate–Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate–Body Leakage, Reverse	V_{GS} = −20 V, V_{DS} = 0 V			−100	nA
ON CHARACTERISTICS (Note 3)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	1	1.4	3	V
		T_C = 125 °C	0.7	1	2.2	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 7.0 A		0.022	0.03	Ω
		T_C = 125 °C		0.033	0.045	Ω
		V_{GS} = 4.5 V, I_D = 3.5 A		0.031	0.05	Ω
		T_C = 125 °C		0.045	0.075	Ω
$I_{D(ON)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 5 V	20			A
		V_{GS} = 2.7 V, V_{DS} = 2.7 V		7.7		A
g_{FS}	Forward Transconductance	V_{DS} = 15 V, I_D = 7.0 V		15		S
DYNAMIC CHARTACTERISTICS						
C_{ISS}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1.0 MHz		1250		pF
C_{OSS}	Output Capacitance			610		pF
C_{RSS}	Reverse Transfer Capacitance			260		pF
SWITCHING CHARACTERISTICS (Note 3)						
$t_{D(ON)}$	Turn-On Delay Time	V_{DD} = 25 V, I_D = 1 A, V_{GEN} = 10 V, R_{GEN} = 6 Ω		10	30	ns
t_r	Turn-On Rise Time			15	60	ns
$t_{D(OFF)}$	Turn-Off Delay Time			70	150	ns
t_f	Turn-Off Fall Time			50	140	ns
Q_g	Total Gate Charge	V_{DS} = 15 V, I_D = 2.0 A, V_{GS} = 10 V		41	50	nC
Q_{gs}	Gate-Source Charge			2.8		nC
Q_{gd}	Gate-Drain Charge			12		nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain–Source Diode Forward Current				2.2	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 2.0 A (Note 3)		0.76	1.1	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = 2 A, dI_S/dt = 100 A/μs		100		ns

Notes:
1. Maximum power dissipation and thermal resistance based on an assumption that a 10 second pulse is equivalent to steady-state and using a single-sided maximum-copper mounting board.
2. Junction-to-ambient thermal resistance based on steady-state conditions in still air using mounting board with minimum heat dissipation characteristics.
3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

TYPICAL ELECTRICAL CHARACTERISTICS

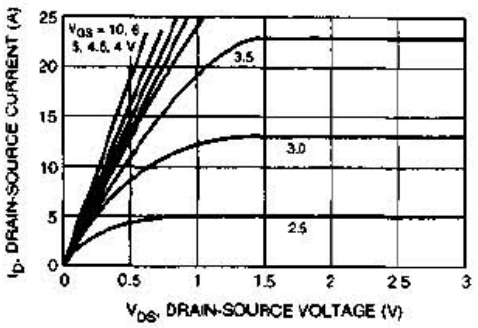


Figure 1. On-Region Characteristics

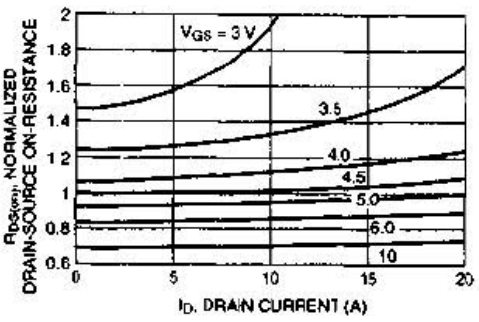


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

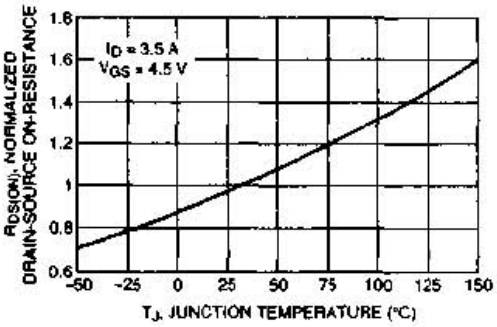


Figure 3. On-Resistance Variation with Temperature

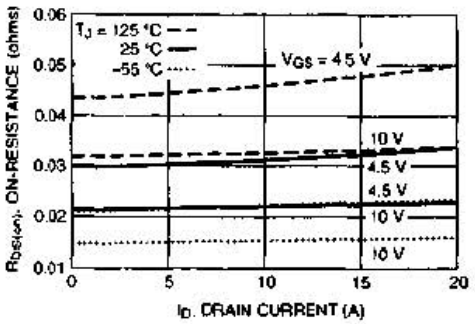


Figure 4. On-Resistance Variation with Drain Current and Temperature

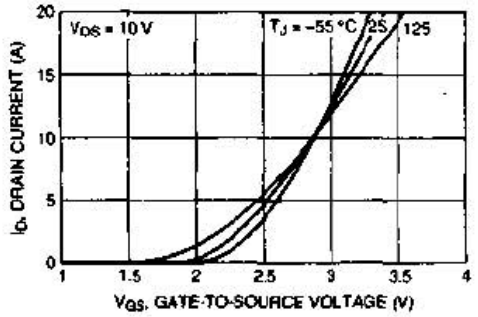


Figure 5. Transfer Characteristics

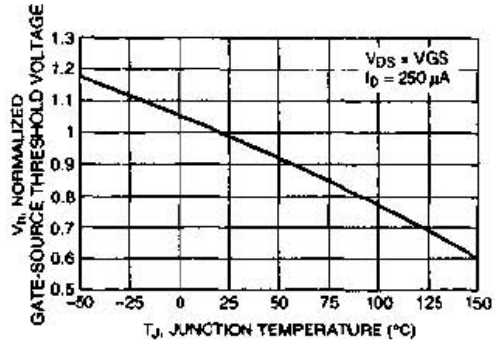


Figure 6. Gate Threshold Variation with Temperature

National Semiconductor

LM741 Operation Amplifier

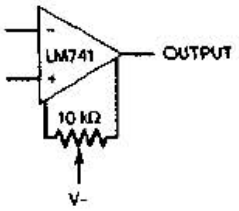
General Description

The LM741 series are general purpose operational amplifiers which feature improved performance over industry standards like the LM709. They are direct, plug-in replacements for the 709C, LM201, MC1439 and 748 in most applications. The amplifiers offer many features which make their application nearly foolproof: overload protection on the input and output, no latch-up when the common mode range is exceeded as well as freedom from oscillations.

The LM741C/LM741E are identical to the LM741/LM741A except that the LM741C/LM741E have their performance guaranteed over a 0 °C to +70 °C temperature range, instead of −55 °C to +125 °C.

Schematic Diagram – (See Figure 13.3 in text)

Offset Nulling Circuit



Absolute Maximum Ratings

	LM741A	LM741E	LM741	LM741C
Supply Voltage	±22 V	±22 V	±22 V	±18 V
Power Dissipation	500 mW	500 mW	500 mW	500 mW
Differential Input Voltage	±30 V	±30 V	±30 V	±30 V
Input Voltage (Note 2)	±15 V	±15 V	±15 V	±15 V
Output Short Circuit Duration	Continuous	Continuous	Continuous	Continuous
Operating Temperature Range	−55 °C to +125 °C	0 °C to +70 °C	−55 °C to +125 °C	0 °C to +70 °C
Storage Temperature Range	−65 °C to +150 °C	−65 °C to +150 °C	−65 °C to +150 °C	−65 °C to +150 °C
Junction Temperature	150 °C	100 °C	150 °C	100 °C

Electrical Characteristics

Parameter	Conditions	LM741A/LM741E			LM741			LM741C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$T_A = 25$ °C $R_S \le 10$ kΩ $R_S \le 50$ Ω		0.8	3.0		1.0	5.0		2.0	6.0	mV mV
	$T_{AMIN} \le T_A \le T_{AMAX}$ $R_S \le 50$ Ω $R_S \le 10$ kΩ			4.0			6.0			7.5	mV mV
Average Input Offset Voltage Drift				15							µV/°C
Input Offset Voltage Adjustment Range	$T_A = 25$ °C, $V_S = \pm 20$ V	±10				±15			±15		mV
Input Offset Current	$T_A = 25$ °C		3.0	30		20	200		20	200	nA
	$T_{AMIN} \le T_A \le T_{AMAX}$			70		85	500			300	nA
Average Input Offset Current Drift				0.5							nA/°C
Input Bias Current	$T_A = 25$ °C		30	80		80	500		80	500	nA
	$T_{AMIN} \le T_A \le T_{AMAX}$			0.210			1.5			0.8	µA
Input Resistance	$T_A = 25$ °C, $V_S = \pm 20$ V	1.0	6.0		0.3	2.0		0.3	2.0		MΩ
	$T_{AMIN} \le T_A \le T_{AMAX}$, $V_S = \pm 20$ V	0.5									MΩ
Input Voltage Range	$T_A = 25$ °C							±12	±13		V
	$T_{AMIN} \le T_A \le T_{AMAX}$				±12	±13					V
Large Signal Voltage Gain	$T_A = 25$ °C, $R_L \ge 2$ kΩ $V_S = \pm 20$ V, $V_O = \pm 15$ V $V_S = \pm 15$ V, $V_O = \pm 10$ V	50			50	200		20	200		V/mV V/mV
	$T_{AMIN} \le T_A \le T_{AMAX}$, $R_L \ge 2$ kΩ $V_S = \pm 20$ V, $V_O = \pm 15$ V $V_S = \pm 15$ V, $V_O = \pm 10$ V $V_S = \pm 5$ V, $V_O = \pm 2$ V	32 10			25			15			V/mV V/mV V/mV

Electrical Characteristics (Continued)

Parameter	Conditions	LM741A/LM741E			LM741			LM741C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Voltage Swing	$V_S = \pm 20$ V $R_L \geq 10$ kΩ $R_L \geq 2$ kΩ	±16 ±15									V V
	$V_S = \pm 15$ V $R_L \geq 10$ kΩ $R_L \geq 2$ kΩ				±12 ±10	±14 ±13		±12 ±10	±14 ±13		V V
Output Short Circuit Current	$T_A = 25$ °C $T_{AMIN} \leq T_A \leq T_{AMAX}$	10 10	25	35 40		25			25		mA mA
Common-Mode Rejection Ratio	$T_{AMIN} \leq T_A \leq T_{AMAX}$ $R_S \leq 10$ kΩ, $V_{CM} = \pm 12$ V $R_S \leq 50$ Ω, $V_{CM} = \pm 12$ V	80	95		70	90		70	90		dB dB
Supply Voltage Rejection Ratio	$T_{AMIN} \leq T_A \leq T_{AMAX}$ $V_S = \pm 20$ V to $V_S = \pm 5$ V $R_S \leq 50$ Ω $R_S \leq 10$ Ω	96	96		77	96		77	96		dB dB
Transient Response Rise Time Overshoot	$T_A = 25$ °C, Unity Gain		0.25 6.0	0.8 20		0.3 5			0.3 5		µs %
Bandwidth	$T_A = 25$ °C	0.437	1.5								MHz
Slew Rate	$T_A = 25$ °C, Unity Gain	0.3	0.7			0.5			0.5		V/µs
Supply Current	$T_A = 25$ °C					1.7	2.8		1.7	2.8	mA
Power Consumption	$T_A = 25$ °C $V_S = \pm 20$ V $V_S = \pm 15$ V		80	150		50	85		50	85	mW mW
LM741A	$V_S = \pm 20$ V $T_A = T_{AMIN}$ $T_A = T_{AMAX}$			165 135							mW mW
LM741E	$V_S = \pm 20$ V $T_A = T_{AMIN}$ $T_A = T_{AMAX}$			150 150							mW mW
LM741	$V_S = \pm 15$ V $T_A = T_{AMIN}$ $T_A = T_{AMAX}$					60 45	100 75				mW mW

Note 2: For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage

APPENDIX

D

Standard Resistor and Capacitor Values

In this appendix, we list standard component values, which are used for selecting resistor and capacitor values in designing discrete electronic circuits and systems. Low-power carbon and film resistors with 2 percent to 20 percent tolerances have a standard set of values and a standard color-band marking scheme. These tabulated values may vary from one manufacturer to another, so the tables should be considered as typical.

D.1 CARBON RESISTORS

Standard resistor values are listed in Table D.1. The lightface type indicates 2 percent and 5 percent tolerance values; the boldface type indicates 10% tolerance resistor values.

Discrete carbon resistors have a standard color-band marking scheme, which makes it easy to recognize resistor values in a circuit or a parts bin, without having to search for a printed legend. The color bands start at one end of the resistor, as shown in Figure D.1. Two digits and a multiplier digit determine the resistor value. The additional color bands indicate the tolerance and reliability. The digit and multiplier color-code is given in Table D.2.

For example, the first three color bands of a 4.7 kΩ resistor are yellow, violet, and red. The first two digits are 47 and the multiplier is 100. The first three color bands on a 150 kΩ resistor are brown, green, and yellow.

Ten percent tolerance carbon resistors are available in the following power ratings: $\frac{1}{4}$, $\frac{1}{2}$, 1, and 2 W.

Table D.1 Standard resistance values ($\times 10^n$)

10	16	27	43	**68**
11	**18**	30	**47**	75
12	20	33	51	**82**
13	**22**	36	**56**	91
15	24	**39**	62	**100**

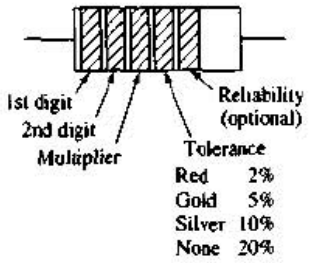


Figure D.1 Color-band notation of low-power carbon-composition resistors

Table D.2 Digit and multiplier color code

Digit	Color	Multiplier	Number of zeros
	Silver	0.01	−2
	Gold	0.1	−1
0	Black	1	0
1	Brown	10	1
2	Red	100	2
3	Orange	1 k	3
4	Yellow	10 k	4
5	Green	100 k	5
6	Blue	1 M	6
7	Violet	10 M	7
8	Gray		
9	White		

D.2 PRECISION RESISTORS (ONE PERCENT TOLERANCE)

Metal-film precision resistors can have tolerance levels in the $\frac{1}{2}$ percent to 1 percent range. These resistors use a four-digit code printed on the resistor body, rather than the color-band scheme. The first three digits denote a value, and the last digit is the multiplier for the number of zeros. For example, 2503 denotes a 250 kΩ resistor, and 2000 denotes a 200 Ω resistor. If the resistor's value is too small to be described in this way, an *R* is used to indicate the decimal point; for example, 37R5 is a 37.5 Ω resistor, and 10R0 is a 10.0 Ω resistor.

The standard values typically range from 10 Ω to 301 kΩ. Standard values in each decade are given in Table D.3.

Table D.3 Standard precision resistance values

100	140	196	274	383	536	750
102	143	200	280	392	549	768
105	147	205	287	402	562	787
107	150	210	294	412	576	806
110	154	215	301	422	590	825
113	158	221	309	432	604	845
115	162	226	316	442	619	866
118	165	232	324	453	634	887
121	169	237	332	464	649	909
124	174	243	340	475	665	931
127	178	249	348	487	681	953
130	182	255	357	499	698	976
133	187	261	365	511	715	
137	191	267	374	523	732	

One percent resistors are often used in applications that require excellent stability and accuracy; a small adjustable trimmer resistor may be connected in series to the 1 percent resistor to set a precise resistance value. It is important to realize that 1 percent resistors are only guaranteed to be within 1 percent of their rated value under a specified set of conditions. Resistance variations due to temperature or humidity changes, and operation at full rated power can exceed the 1 percent tolerance.

D.3 CAPACITORS

Typical capacitor values for 10 percent tolerance capacitors from one manufacturer are listed in Table D.4. The range of capacitance values for the ceramic-disk capacitor is approximately 10 pF to 1 μF.

Table D.4 Ceramic-disk capacitors

3.3	30	200	600	2700
5	39	220	680	3000
6	47	240	750	3300
6.8	50	250	800	3900
7.5	51	270	820	4000
8	56	300	910	4300
10	68	330	1000	4700
12	75	350	1200	5000
15	82	360	1300	5600
18	91	390	1500	6800
20	100	400	1600	7500
22	120	470	1800	8200
24	130	500	2000	
25	150	510	2200	
27	180	560	2500	

Tantalum capacitors ($\times 10^n$) (to 330 μF)

0.0047	0.010	0.022
0.0056	0.012	0.027
0.0068	0.015	0.033
0.0082	0.018	0.039

APPENDIX

E

Reading List

GENERAL ELECTRONICS TEXTS

Burns, S. G.; and P. R. Bond. *Principles of Electronic Circuits*. 2nd ed. Boston: PWS Publishing Co., 1997.

Colclaser, R. A.; D. A. Neamen; and C. F. Hawkins. *Electronic Circuit Analysis: Basic Principles*. New York: John Wiley and Sons, Inc., 1984.

Gaussi, M. S. *Electronic Devices and Circuits: Discrete and Integrated*. New York: Holt, Rinehart, and Winston, 1985.

Hambley, A. R. *Electronics*. New York: Macmillan Publishing Co., 1994.

Hayt, W. H., Jr.; and G. W. Neudeck. *Electronic Circuit Analysis and Design*. 2nd ed. Boston: Houghton Mifflin Co., 1984.

Horenstein, M. N. *Microelectronic Circuits and Devices*. 2nd ed. Englewood Cliffs, NJ: Prentice Hall, Inc., 1995.

Horowitz, P.; and W. Hill. *The Art of Electronics*. 2nd ed. New York: Cambridge University Press, 1989.

Jaeger, R. C. *Microelectronic Circuit Design*. New York: McGraw-Hill Companies, Inc., 1997.

Malik, N. R. *Electronic Circuits: Analysis, Simulation, and Design*. Englewood Cliffs, NJ: Prentice Hall, Inc., 1995.

Mauro, R. *Engineering Electronics*. Englewood Cliffs, NJ: Prentice Hall, Inc., 1989.

Millman, J.; and A. Graybel. *Microelectronics*. 2nd ed. New York: McGraw-Hill Book Co., 1987.

Mitchell, F. H., Jr.; and F. H. Mitchell, Sr. *Introduction to Electronics Design*. 2nd ed. Englewood Cliffs, NJ: Prentice-Hall, Inc., 1992.

Rashid, M. H. *Microelectronic Circuits: Analysis and Design*. Boston: PWS Publishing Co., 1999.

Roden, M. S.; and G. L. Carpenter. *Electronic Design: From Concept to Reality*. 3rd ed. Burbank, CA: Discovery Press, 1997.

Sedra, A. S.; and K. C. Smith. *Microelectronic Circuits*. 4th ed. New York: Oxford University Press, 1998.

LINEAR CIRCUIT THEORY

Alexander, C. K.; and M. N. O. Sadiku. *Fundamentals of Electric Circuits*. Boston: McGraw-Hill Companies, Inc., 2000.

Bode, H. W. *Network Analysis and Feedback Amplifier Design*. Princeton, NJ; D. Van Nostrand Co., 1945.

Hayt, W. H., Jr.; and J. E. Kemmerley. *Engineering Circuit Analysis*. 4th ed. New York: McGraw-Hill Book Co., 1986.

Irwin, J. D.; and C-H. Wu. *Basic Engineering Circuit Analysis*. 6th ed. Upper Saddle River, NJ: Prentice-Hall, Inc., 1999.

Johnson, D. E.; J. L. Hillburn; J. R. Johnson; and P. D. Scott. *Basic Electric Circuit Analysis*. 5th ed. Englewood Cliffs, NJ: Prentice Hall, Inc., 1995.

Nilsson, J. W.; and S. A. Riedel. *Electric Circuits*. 6th ed. Upper Saddle River, NJ: Prentice-Hall, Inc., 2000.

SEMICONDUCTOR DEVICES

Neamen, D. A. *Semiconductor Physics and Devices: Basic Principles*. 2nd ed. Homewood, IL: Richard D. Irwin, Inc., 1997.

Streetman, B. G. *Solid State Electronic Devices*. 4th ed. Englewood Cliffs, NJ: Prentice Hall, Inc., 1995.

ANALOG INTEGRATED CIRCUITS

Allen, P. E.; and D. R. Hoberg. *CMOS Analog Circuit Design*. New York: Holt, Rinehart, and Winston, 1987.

Geiger, R. L.; P. E. Allen; and N. R. Strader. *VLSI Design Techniques for Analog and Digital Circuits*. New York: McGraw-Hill Publishing Co., 1990.

Gray, P. R.; and R. G. Meyer. *Analysis and Design of Analog Integrated Circuits*. 3rd ed. New York: John Wiley and Sons, Inc., 1993.

Johns, D. A.; and K. Martin. *Analog Integrated Circuit Design*. New York: John Wiley and Sons, Inc., 1997.

Laker, K. R.; and W. M. C. Sansen. *Design of Analog Integrated Circuits and Systems*. New York: McGraw-Hill, Inc., 1994.

Northrop, R. B. *Analog Electronic Circuits*. Reading, MA: Addison-Wesley Publishing Co., 1990.

Soclof, S. *Design and Applications of Analog Integrated Circuits*. Englewood Cliffs, NJ: Prentice Hall, Inc., 1991.

Solomon, J. E. "The Monolithic Op-Amp: A Tutorial Study," *IEEE Journal of Solid-State Circuits* SC-9, No. 6 (December 1974), pp. 314–32.

Widlar, R. J. "Design Techniques for Monolithhic Operational Amplifiers," *IEEE Journal of Solid-State Circuits* SC-4 (August 1969), pp. 184–91.

OPERATIONAL AMPLIFIER CIRCUITS

Barna, A.; and D. I. Porat. *Operational Amplifiers*. 2nd ed. New York: John Wiley and Sons, Inc., 1989.

Berlin, H. M. *Op-Amp Circuits and Principles*. Carmel, IN: SAMS, A division of Macmillan Computer Publishing, 1991.

Coughlin, R. F.; and F. F. Driscoll. *Operational Amplifiers and Linear Integrated Circuits*. Englewood Cliffs, NJ: Prentice Hall, Inc., 1977.

Graeme, J. G.; G. E. Tobey; and L. P. Huelsman. *Operational Amplifiers: Design and Applications*. New York: McGraw-Hill Book Co., 1971.