Collector Current Since the doping concentration in the emitter is much larger than that in the base region, the vast majority of emitter current is due to the injection of electrons into the base. The number of these injected electrons reaching the collector is the major component of collector current.

The number of electrons reaching the collector per unit time is proportional to the number of electrons injected into the base, which in turn is a function of the B–E voltage. To a first approximation, the collector current is proportional to e^{v_{BE}/V_T} and is independent of the reverse-biased B–C voltage. The device therefore looks like a **constant-current source**. The collector current is controlled by the B–E voltage; in other words, the current at one terminal (the collector) is controlled by the voltage across the other two terminals. *This control is the basic transistor action.*

The collector current is proportional to the emitter current, so we can write the collector current as[1]

$$i_C = \alpha_F i_E = \alpha_F I_S e^{v_{BE}/V_T} \tag{3.2}$$

where α_F is a constant less than 1 but very close to 1. This parameter is called the **common-base current gain**. The reason for this name will become clearer as we proceed through the chapter.

Base Current Since the B–E junction is forward biased, holes from the base flow across the B–E junction into the emitter. However, because these holes do not contribute to the collector current, they are not part of the transistor action. Instead, the flow of holes forms one component of the base current. This component is also an exponential function of the B–E voltage, because of the forward-biased B–E junction. We can write

$$i_{B1} \propto e^{v_{BE}/V_T} \tag{3.3(a)}$$

A few electrons recombine with majority carrier holes in the base. The holes that are lost must be replaced through the base terminal. The flow of such holes is a second component of the base current. This "recombination current" is directly proportional to the number of electrons being injected from the emitter, which in turn is an exponential function of the B–E voltage. We can write

$$i_{B2} \propto e^{v_{BE}/V_T} \tag{3.3(b)}$$

The total base current is the sum of the two components from Equations (3.3(a)) and (3.3(b)):

$$i_B \propto e^{v_{BE}/V_T} \tag{3.4}$$

Figure 3.5 shows the flow of electrons and holes in an npn bipolar transistor, as well as the terminal currents.[2] (Reminder: the conventional current

[1] In many cases, the multiplying constant in the collector current, i_C, equation is written as I_S, which means that the multiplying constant for the emitter current would be I_S/α_F. The important point of this discussion is that the currents are an exponential function of the B–E voltage. Which multiplying parameter is used in each equation is simply a matter of preference.

[2] A more thorough study of the physics of the bipolar transistor shows that there are other current components, in addition to the ones mentioned. However, these additional currents do not change the basic properties of the transistor and can be neglected for our purposes.

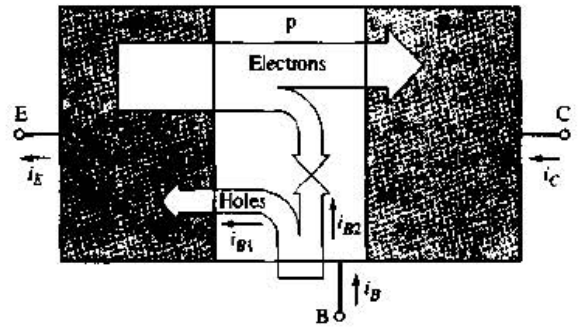


Figure 3.5 Electron and hole currents in an npn transistor biased in the forward-active mode

direction is the same as the flow of positively charged holes and opposite to the flow of negatively charged electrons.)

If the concentration of electrons in the n-type emitter is much larger than the concentration of holes in the p-type base, then the number of electrons injected into the base will be much larger than the number of holes injected into the emitter. This means that the i_{B1} component of the base current will be much smaller than the collector current. In addition, if the base width is small, then the number of electrons that recombine in the base will be small, and the i_{B2} component of the base current will also be much smaller than the collector current.

Common-Emitter Current Gain

In the transistor, the rate of flow of electrons and the resulting collector current are an exponential function of the B–E voltage, as is the resulting base current. This means that the collector current and the base current are linearly related. Therefore, we can write

$$\frac{i_C}{i_B} = \beta_F \tag{3.5}$$

or

$$i_B = \frac{\alpha_F I_S}{\beta_F} e^{v_{BE}/V_T} \tag{3.6}$$

The parameter β is the **common-emitter current gain** and is a key parameter of the bipolar transistor. In this idealized situation, β is considered to be a constant for any given transistor. The value of β is usually in the range of $50 < \beta < 300$, but it can be smaller or larger for special devices.

Figure 3.6 shows an npn bipolar transistor in a circuit. Because the emitter is the common connection, this circuit is referred to as a **common-emitter configuration**. When the transistor is biased in the forward-active mode, the B–E junction is forward biased and the B–C junction is reverse biased. Using the piecewise linear model of a pn junction, we assume that the B–E voltage is equal to V_{BE}(on), the junction turn-on voltage. Since $V_{CC} = v_{CE} + i_C R_C$, the power supply voltage must be sufficiently large to keep the B–C junction reverse biased. The base current is established by V_{BB} and R_B, and the resulting collector current is $i_C = \beta i_B$.

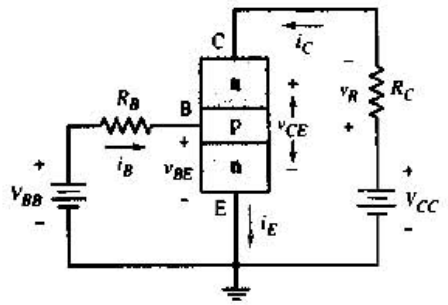


Figure 3.6 An npn transistor circuit in the common-emitter configuration

If we set $V_{BB} = 0$, the B–E junction will have zero applied volts; therefore, $i_B = 0$, which implies that $i_C = 0$. This condition is called **cutoff**.

Current Relationships

If we treat the bipolar transistor as a single node, then, by Kirchhoff's current law, we have

$$i_E = i_C + i_B \tag{3.7}$$

If the transistor is biased in the forward-active mode, then

$$i_C = \beta i_B \tag{3.8}$$

Substituting Equation (3.8) into (3.7), we obtain the following relationship between the emitter and base currents:

$$i_E = (1 + \beta) i_B \tag{3.9}$$

Solving for i_B in Equation (3.8) and substituting into Equation (3.9), we obtain a relationship between the collector and emitter currents, as follows:

$$i_C = \left(\frac{\beta}{1 + \beta}\right) i_E \tag{3.10}$$

From Equation (3.2), we had $i_C = \alpha_F i_E$ so

$$\alpha_F = \frac{\beta_F}{1 + \beta_F} \tag{3.11}$$

The parameter α_F is called the common-base current gain and is always slightly less than 1. We may note that if $\beta_F = 100$, then $\alpha_F = 0.99$, so α_F is indeed close to 1. From Equation (3.11), we can state the common-emitter current gain in terms of the common-base current gain:

$$\beta_F = \frac{\alpha_F}{1 - \alpha_F} \tag{3.12}$$

Summary of Transistor Operation

We have presented a first-order model of the operation of the npn bipolar transistor biased in the forward-active region. The forward-biased B–E voltage, v_{BE}, causes an exponentially related flow of electrons from the emitter into the base where they diffuse across the base region and are collected in the

collector region. The collector current, i_C, is independent of the B–C voltage as long as the B–C junction is reverse biased. The collector, then, behaves as an ideal current source. The collector current is a fraction α_F of the emitter current, and the base current is a fraction $1/\beta_F$ of the collector current. If $\beta_F \gg 1$, then $\alpha_F \cong 1$ and $i_C \cong i_E$.

Example 3.1 **Objective:** Calculate the collector and emitter currents, given the base current and current gain.

Assume a common-emitter current gain of $\beta = 150$ and a base current of $i_B = 15\,\mu A$. Also assume that the transistor is biased in the forward-active mode.

Solution: The relation between collector and base currents gives

$$i_C = \beta i_B = (150)(15\,\mu A) \Rightarrow 2.25\,mA$$

and the relation between emitter and base currents yields

$$i_E = (1 + \beta)i_B = (151)(15\,\mu A) \Rightarrow 2.27\,mA$$

From Equation (3.11), the common-base current gain is

$$\alpha = \frac{\beta}{1 + \beta} = \frac{150}{151} = 0.9934$$

Comment: For reasonable values of β, the collector and emitter currents are nearly equal, and the common-base current gain is nearly 1.

Test Your Understanding

3.1 Transistors of a particular type have common-base current gains in the range of $0.980 \leq \alpha \leq 0.995$. Find the corresponding range of β. (Ans. $49 \leq \beta \leq 199$)

3.2 The common-emitter current gains of two transistors are $\beta = 75$ and $\beta = 125$. Determine the common-base current gains. (Ans. $\alpha = 0.9868$, $\alpha = 0.9921$)

3.1.3 pnp Transistor: Forward-Active Mode Operation

We have discussed the basic operation of the npn bipolar transistor. The complementary device is the pnp transistor. Figure 3.7 shows the flow of holes and electrons in a pnp device biased in the forward-active mode. Since the B–E junction is forward biased, the p-type emitter is positive with respect to the n-type base, holes flow from the emitter into the base, the holes diffuse across the base, and they are swept into the collector. The collector current is a result of this flow of holes.

Again, since the B–E junction is forward biased, the emitter current is an exponential function of the B–E voltage. Noting the direction of emitter current and the polarity of the foward-biased B–E voltage, we can write

$$i_E = I_S e^{v_{EB}/V_T} \tag{3.13}$$

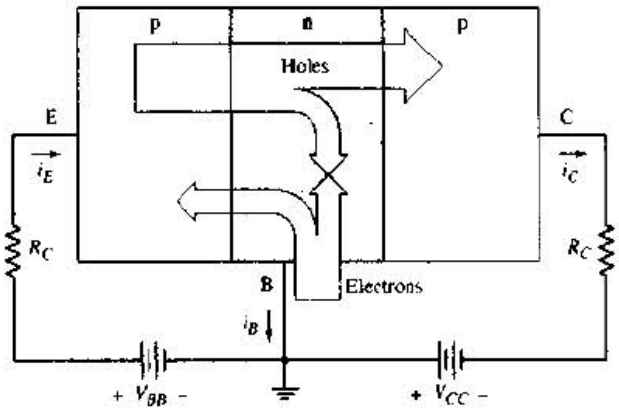


Figure 3.7 Electron and hole currents in a pnp transistor biased in the forward-active mode

where we are again assuming the (−1) term in the ideal diode equation is negligible.

The collector current is an exponential function of the E–B voltage, and the direction is out of the collector terminal, which is opposite to that in the npn device. We can now write

$$i_C = \alpha_F i_E = \alpha_F I_S e^{v_{EB}/V_T} \tag{3.14}$$

where α_F is again the common-base current gain.

The base current in a pnp device is the sum of two components. The first component comes from electrons flowing from the base into the emitter as a result of the forward-biased E–B junction. The second component comes from the flow of electrons supplied through the base terminal to replace those lost by recombination with holes in the base. The direction of the base current is out of the base terminal. The base current in the pnp device is also an exponential function of the E–B voltage, as follows:

$$i_B = \frac{i_C}{\beta_F} = \frac{\alpha_F I_S}{\beta_F} e^{v_{EB}/V_T} \tag{3.15}$$

The parameter β is also the common-emitter current gain of the pnp bipolar transistor.

The relationships between the terminal currents of the pnp transistor are exactly the same as those of the npn transistor and are summarized in Table 3.1 in the next section. Also the relationships between β_F and α_F are the same as given in Equations (3.11) and (3.12).

3.1.4 Circuit Symbols and Conventions

The block diagram and conventional circuit symbol of an npn bipolar transistor are shown in Figures 3.8(a) and 3.8(b). The arrowhead in the circuit symbol is always placed on the emitter terminal, and it indicates the direction of the emitter current. For the npn device, this direction is out of the emitter. The simplified block diagram and conventional circuit symbol of a pnp bipolar transistor are shown in Figures 3.9(a) and 3.9(b). Here, the arrowhead on the

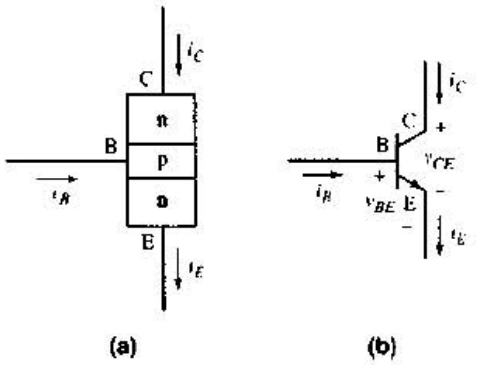


Figure 3.8 npn bipolar transistor: (a) simple block diagram and (b) circuit symbol

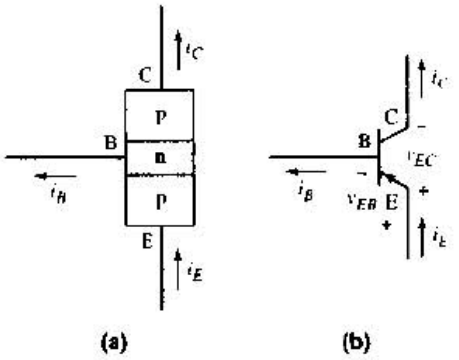


Figure 3.9 pnp bipolar transistor: (a) simple block diagram and (b) circuit symbol

emitter terminal indicates that the direction of the emitter current is into the emitter.

Referring to the circuit symbols given for the npn (Figure 3.8(b)) and pnp (Figure 3.9(b)) transistors showing current directions and voltage polarities, we can summarize the current–voltage relationships as given in Table 3.1.

Figure 3.10(a) shows a common-emitter circuit with an npn transistor. The figure includes the transistor currents, and the base-emitter (B–E) and collector-emitter (C–E) voltages. Figure 3.10(b) shows a common-emitter circuit with a

Table 3.1 Summary of the bipolar current–voltage relationships in the active region

npn	pnp
$i_E = I_S e^{v_{BE}/V_T}$	$i_E = I_S e^{v_{EB}/V_T}$
$i_C = \alpha_F i_E = \alpha_F I_S e^{v_{BE}/V_T}$	$i_C = \alpha_F i_E = \alpha_F I_S e^{v_{EB}/V_T}$
$i_B = \dfrac{i_C}{\beta_F} = \dfrac{\alpha_F I_S}{\beta_F} e^{v_{BE}/V_T}$	$i_B = \dfrac{i_C}{\beta_F} = \dfrac{\alpha_F I_S}{\beta_F} e^{v_{EB}/V_T}$
For both transistors	
$i_C = \beta_F i_B$	$\alpha_F = \dfrac{\beta_F}{1+\beta_F}$
$i_E = (1+\beta_F) i_B$	
$i_C = \left(\dfrac{\beta_F}{1+\beta_F}\right) i_E = \alpha_F i_E$	$\beta_F = \dfrac{\alpha_F}{1-\alpha_F}$

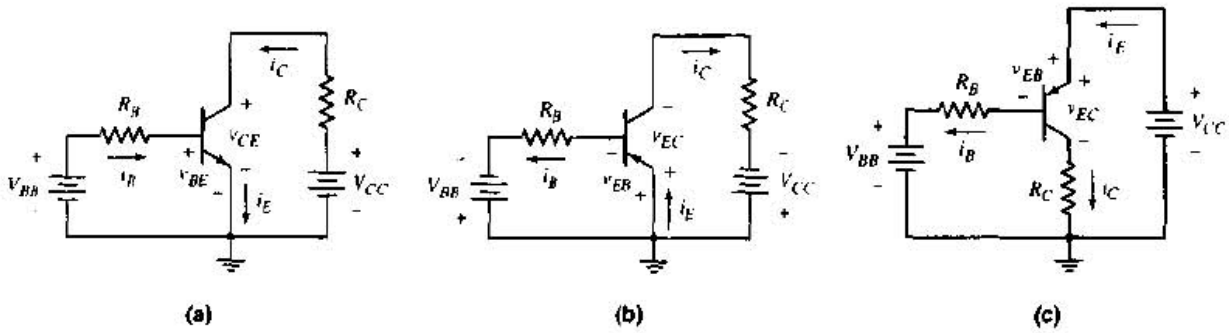


Figure 3.10 Common-emitter circuits: (a) with an npn transistor, (b) with a pnp transistor, and (c) with a pnp transistor biased with a positive voltage source

pnp bipolar transistor. Note the different current directions and voltage polarities in the two circuits. A more usual circuit configuration using the pnp transistor is shown in Figure 3.10(c). This circuit allows positive voltage supplies to be used.

Test Your Understanding

3.3 An npn transistor is biased in the forward-active mode. The base current is $I_B = 9.60\,\mu A$ and the emitter current is $I_E = 0.780\,mA$. Determine β, α, and I_C. (Ans. $\beta = 80.3$, $\alpha = 0.9877$, $I_C = 0.771\,mA$)

3.4 The emitter current in a pnp transistor biased in the forward-active mode is $I_E = 2.15\,mA$. The common-base current gain of the transistor is $\alpha = 0.990$. Determine β, I_B, and I_C. (Ans. $\beta = 99$, $I_B = 21.5\,\mu A$, $I_C = 2.13\,mA$)

3.1.5 Current–Voltage Characteristics

Figures 3.11(a) and 3.11(b) are **common-base circuit configurations** for an npn and a pnp bipolar transistor, respectively. The current sources provide the emitter current. Previously, we stated that the collector current i_C was nearly independent of the C–B voltage as long as the B–C junction was reverse biased. When the B–C junction becomes forward biased, the transistor is no longer in the forward-active mode, and the collector and emitter currents are no longer related by $i_E = \alpha_F i_C$.

Figure 3.12 shows the typical common-base current–voltage characteristics. When the collector–base junction is reverse biased, then for constant values of emitter current, the collector current is nearly equal to i_E. These characteristics show that the common-base device is nearly an ideal constant-current source.

The C–B voltage can be varied by changing the V^+ voltage (Figure 3.11(a)) or the V^- voltage (Figure 3.11(b)). When the collector–base junction becomes forward biased in the range of 0.2 and 0.3 V, the collector current i_C is still essentially equal to the emitter current i_E. In this case, the transistor is still

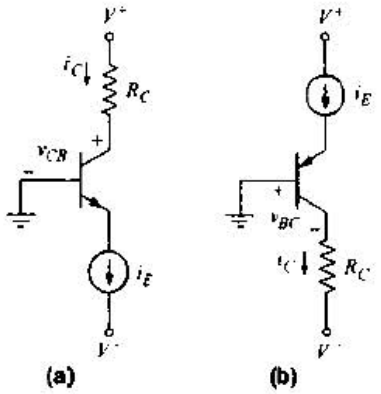


Figure 3.11 Common-base circuit configurations: (a) an npn transistor and (b) a pnp transistor

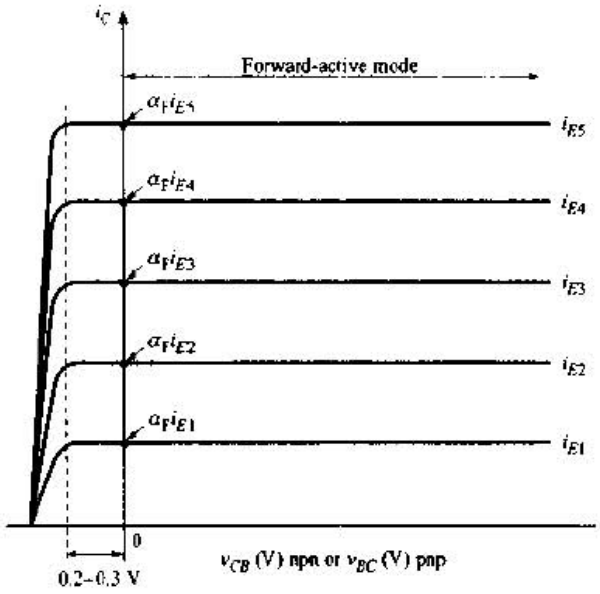


Figure 3.12 Transistor current–voltage characteristics of the common-base circuit

basically biased in the forward-active mode. However, as the forward-bias C–B voltage increases, the linear relationship between the collector and emitter currents is no longer valid, and the collector current very quickly drops to zero.

The common-emitter circuit configuration provides a slightly different set of current-voltage characteristics, as shown in Figure 3.13. For these curves, the collector current is plotted against the collector–emitter voltage, for various constant values of the base current. These curves are generated from the common-emitter circuits shown in Figure 3.10. In this circuit, the V_{BB} source forward biases the B–E junction and controls the base current i_B. The C–E voltage can be varied by changing V_{CC}.

In the npn device, in order for the transistor to be biased in the forward-active mode, the B–C junction must be zero or reverse biased, which means

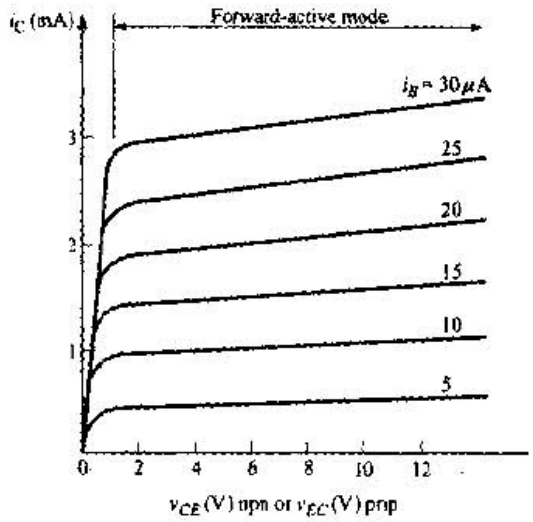


Figure 3.13 Transistor current–voltage characteristics of the common-emitter circuit

that V_{CE} must be greater than approximately $V_{BE}(\text{on})$.[3] For $V_{CE} > V_{BE}(\text{on})$, there is a finite slope to the curves. If, however, $V_{CE} < V_{BE}(\text{on})$, the B-C junction becomes forward biased, the transistor is no longer in the forward-active mode, and the collector current very quickly drops to zero.

Figure 3.14 shows an exaggerated view of the current–voltage characteristics plotted for constant values of the B-E voltage. The curves are theoretically linear with respect to the C–E voltage in the forward-active mode. When the curves are extrapolated to zero current, they meet at a point on the negative voltage axis, at $v_{CE} = -V_A$. The voltage V_A is a positive quantity called the **Early voltage**, after J. M. Early, who first predicted these characteristics. Typical values of V_A are in the range $50 < V_A < 300$ V.

For a given value of v_{BE}, if v_{CE} increases, the reverse-bias voltage on the collector-base junction increases, which means that the width of the B–C

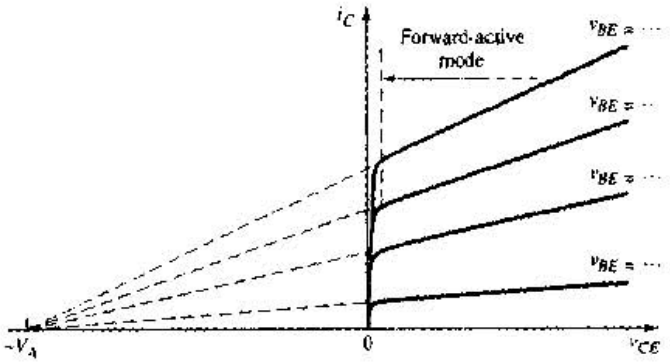


Figure 3.14 Current–voltage characteristics for the common-emitter circuit, showing the Early voltage

[3] Even though the collector current is essentially equal to the emitter current when the B–C junction becomes slightly forward biased, as was shown in Figure 3.12, the transistor is said to be biased in the forward-active mode when the B–C junction is zero or reverse biased.

space-charge region also increases. This in turn reduces the neutral base width W (see Figure 3.4). A decrease in the base width causes the gradient in the minority carrier concentration to increase, which increases the diffusion current through the base. The collector current then increases as the C–E voltage increases.

The linear dependence of i_C versus v_{CE} in the forward-active mode can be described by

$$i_C = \alpha_F I_S\left(e^{v_{BE}/V_t}\right)\cdot\left(1+\frac{v_{CE}}{V_A}\right) \tag{3.16}$$

where I_S and α_F are assumed to be constant.

In Figure 3.14, the nonzero slope of the curves indicates that the **output resistance** r_o looking into the collector is finite. This output resistance is determined from

$$\frac{1}{r_o} = \left.\frac{\partial i_C}{\partial v_{CE}}\right|_{v_{BE}=\text{const.}} \tag{3.17}$$

Using Equation (3.16), we can show that

$$r_o \cong \frac{V_A}{I_C} \tag{3.18}$$

where I_C is the quiescent collector current when v_{BE} is a constant and v_{CE} is small compared to V_A.

In most cases, the dependence of i_C on v_{CE} is not critical in the dc analysis or design of transistor circuits. However, the finite output resistance r_o may significantly affect the amplifier characteristics of such circuits. This effect is examined more closely in Chapter 4 of this text.

Test Your Understanding

3.5 Find the output resistance r_o of a bipolar transistor for which $V_A = 150\,\text{V}$ at collector currents of $I_C = 0.1$, 1.0, and 10 mA. (Ans. $r_o = 1.5\,\text{M}\Omega$, $150\,\text{k}\Omega$, $15\,\text{k}\Omega$)

3.6 Assume that $I_C = 1\,\text{mA}$ at $V_{CE} = 1\,\text{V}$, and that V_{BE} is held constant. Determine I_C at $V_{CE} = 10\,\text{V}$ if: (a) $V_A = 75\,\text{V}$; and (b) $V_A = 150\,\text{V}$. (Ans. $I_C = 1.12\,\text{mA}$, $1.06\,\text{mA}$)

3.1.6 Nonideal Transistor Leakage Currents and Breakdown Voltage

In discussing the current–voltage characteristics of the bipolar transistor in the previous sections, two topics were ignored: leakage currents in the reverse-biased pn junctions and breakdown voltage effects.

Leakage Currents

In the common-base circuits in Figure 3.11, if we set the current source $i_E = 0$, transistors will be cut off, but the B–C junctions will still be reverse biased. A reverse-bias leakage current exists in these junctions, and this current corre-

sponds to the reverse-bias saturation current in a diode, as described in Chapter 1. The direction of these reverse-bias leakage currents is the same as that of the collector currents. The term I_{CBO} is the collector leakage current in the common-base configuration, and is the collector-base leakage current when the emitter is an open circuit.

Another leakage current can exist between the emitter and collector with the base terminal an open circuit. Figure 3.15 is a block diagram of an npn transistor in which the base is an open circuit ($i_B = 0$). The current component I_{CBO} is the normal leakage current in the reverse-biased B–C pn junction. This current component causes the base potential to increase, which forward biases the B–E junction and induces the B-E current I_{CEO}. The current component αI_{CEO} is the normal collector current resulting from the emitter current I_{CEO}. We can write

$$I_{CEO} = \alpha I_{CEO} + I_{CBO} \tag{3.19(a)}$$

or

$$I_{CEO} = \frac{I_{CBO}}{1-\alpha} \cong \beta I_{CBO} \tag{3.19(b)}$$

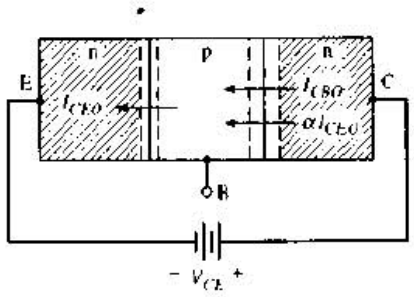


Figure 3.15 Block diagram of an npn transistor in an open-base configuration

This relationship indicates that the open-base configuration produces different characteristics than the open-emitter configuration.

When the transistors are biased in the forward-active mode, the leakage currents still exist. The common-emitter and common-base current gain parameters, β_F and α_F, are dc parameters and can be written as $\beta_F = I_C/I_B$ and $\alpha_F = I_C/I_E$, where I_C includes the leakage current component. In the next chapter, we will discuss ac current gain factors. In most instances in this text, leakage currents will be completely negligible.

Breakdown Voltage: Common-Base Characteristics

The common-base current–voltage characteristics shown in Figure 3.12 are ideal in that breakdown is not shown. Figure 3.16 shows the same i_C versus v_{CB} characteristics with the breakdown voltage.

Consider the curve for $i_E = 0$ (the emitter terminal is effectively an open circuit). The collector–base junction breakdown voltage is indicated as BV_{CBO}. This is a simplified figure in that it shows breakdown occurring abruptly at BV_{CBO}. For the curves in which $i_E > 0$, breakdown actually begins earlier. The carriers flowing across the junction initiate the breakdown avalanche process at somewhat lower voltages.

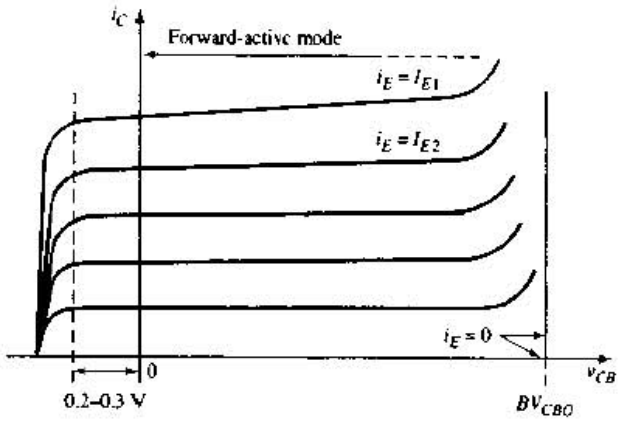


Figure 3.16 The i_C versus v_{CB} common-base characteristics, showing the collector–base junction breakdown

Breakdown Voltage: Common-Emitter Characteristics

Figure 3.17 shows the i_C versus v_{CE} characteristics of an npn transistor, for various constant base currents, and an ideal breakdown voltage of BV_{CEO}. The value of BV_{CEO} is less than the value of BV_{CBO} because BV_{CEO} includes the effects of the transistor action, while BV_{CBO} does not. This same effect was observed in the I_{CEO} leakage current.

The breakdown voltage characteristics for the two configurations are also different. The breakdown voltage for the open-base case is given by

$$BV_{CEO} = \frac{BV_{CBO}}{\sqrt[n]{\beta}} \tag{3.20}$$

where n is an empirical constant usually in the range of 3 to 6.

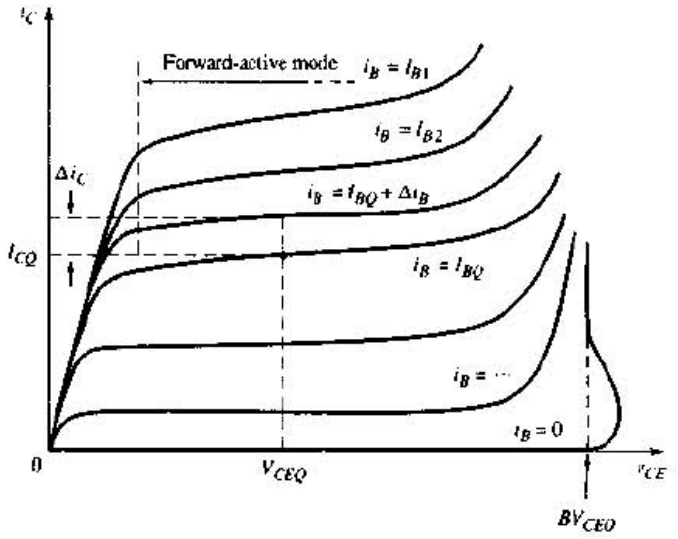


Figure 3.17 Common-emitter characteristics showing breakdown effects

Example 3.2 **Objective:** Calculate the breakdown voltage of a transistor connected in the open-base configuration.

Assume that the transistor current gain is $\beta = 100$ and that the breakdown voltage of the B–C junction is $BV_{CBO} = 120\,\text{V}$.

Solution: If we assume an empirical constant of $n = 3$, we have

$$BV_{CEO} = \frac{BV_{CBO}}{\sqrt[n]{\beta}} = \frac{120}{\sqrt{100}} = 25.9\,\text{V}$$

Comment: The breakdown voltage of the open-base configuration is substantially less than that of the C-B junction. This represents a worst-case condition, which must be considered in any circuit design.

Design Pointer: The designer must be aware of the breakdown voltage of the specific transistors used in a circuit, since this will be a limiting factor in the size of the dc bias voltages that can be used.

Breakdown may also occur in the B–E junction if a reverse-bias voltage is applied to that junction. The junction breakdown voltage decreases as the doping concentrations increase. Since the emitter doping concentration is usually substantially larger than the doping concentration in the collector, the B-E junction breakdown voltage is normally much smaller than that of the B-C junction. Typical B–E junction breakdown voltage values are in the range of 6 to 8 V.

Test Your Understanding

3.7 The open-emitter breakdown voltage is $BV_{CBO} = 200\,\text{V}$, the current gain is $\beta = 120$, and the empirical constant is $n = 3$. Determine BC_{CEO}. (Ans. 40.5 V)

3.8 A particular transistor circuit requires a minimum open-base breakdown voltage of $BV_{CEO} = 30\,\text{V}$. If $\beta = 100$ and $n = 3$, determine the minimum required value of BV_{CBO}. (Ans. 139 V)

3.2 DC ANALYSIS OF TRANSISTOR CIRCUITS

We've considered the basic transistor characteristics and properties. We can now start analyzing and designing the dc biasing of bipolar transistor circuits. A primary purpose of the rest of the chapter is to become familiar and comfortable with the bipolar transistor and transistor circuits. The dc biasing of transistors, the focus of this chapter, is an important part of designing bipolar amplifiers, the focus of the next chapter.

The piecewise linear model of a pn junction can be used for the dc analysis of bipolar transistor circuits. We will first analyze the common-emitter circuit and introduce the load line for that circuit. We will then look at the dc analysis of other bipolar transistor circuit configurations. Since a transistor in a linear

amplifier must be biased in the forward-active mode, we emphasize, in this section, the analysis and design of circuits in which the transistor is biased in this mode.

3.2.1 Common-Emitter Circuit

One of the basic transistor circuit configurations is called the **common-emitter circuit**. Figure 3.18(a) shows one example of a common-emitter circuit. The emitter terminal is obviously at ground potential. This circuit configuration will appear in many amplifiers that will be considered in Chapter 4.

Figure 3.18(a) shows a common-emitter circuit with an npn transistor, and Figure 3.18(b) shows the dc equivalent circuit. We will assume that the B–E junction is forward biased, so the voltage drop across that junction is the cut-in or turn-on voltage $V_{BE}(\text{on})$. When the transistor is biased in the forward-active mode, the collector current is represented as a dependent current source that is a function of the base current. We are neglecting the reverse-biased junction leakage current and the Early effect in this case. In the following circuits, we will be considering dc currents and voltages, so the dc notation for these parameters will be used.

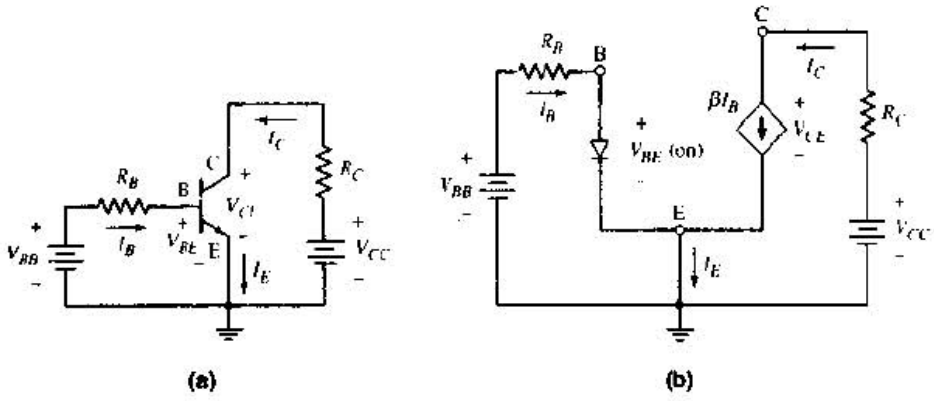


Figure 3.18 (a) Common-emitter circuit with an npn transistor and (b) dc equivalent circuit, with piecewise linear parameters

The base current is

$$I_B = \frac{V_{BB} - V_{BE}(\text{on})}{R_B} \tag{3.21}$$

Implicit in Equation (3.21) is that $V_{BB} > V_{BE}(\text{on})$, which means that $I_B > 0$. When $V_{BB} < V_{BE}(\text{on})$, the transistor is cut off and $I_B = 0$.

In the collector–emitter portion of the circuit, we can write

$$I_C = \beta I_B \tag{3.22}$$

and

$$V_{CC} = I_C R_C + V_{CE} \tag{3.23(a)}$$

or

$$V_{CE} = V_{CC} - I_C R_C \tag{3.23(b)}$$

In Equation (3.23(b)), we are also implicitly assuming that $V_{CE} > V_{BE}(\text{on})$, which means that the B-C junction is reverse biased and the transistor is biased in the forward-active mode.

Example 3.3 **Objective:** Calculate the base, collector, and emitter currents and the C-E voltage for a common-emitter circuit.

For the circuit shown in Figure 3.18(a), the parameters are: $V_{BB} = 4\,\text{V}$, $R_B = 220\,\text{k}\Omega$, $R_C = 2\,\text{k}\Omega$, $V_{CC} = 10\,\text{V}$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, and $\beta = 200$. Figure 3.19(a) shows the circuit without explicitly showing the voltage sources.

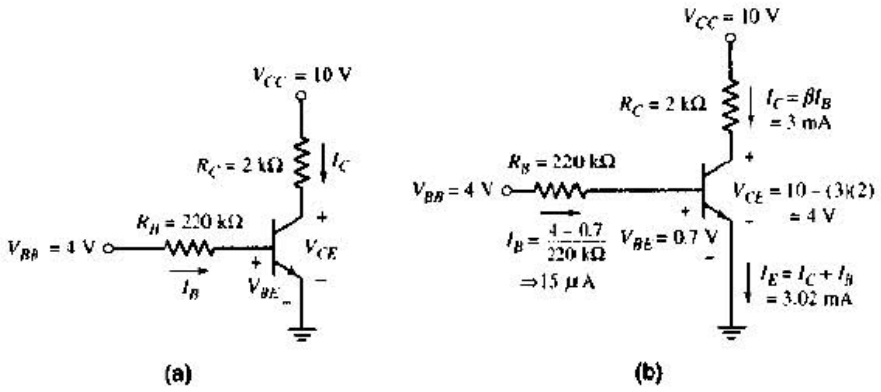


Figure 3.19 Circuit for Example 3.3

Solution: Referring to Figure 3.19(b), the base current is found as

$$I_B = \frac{V_{BB} - V_{BE}(\text{on})}{R_B} = \frac{4 - 0.7}{220} \Rightarrow 15\,\mu\text{A}$$

The collector current is

$$I_C = \beta I_B = (200)(15\,\mu\text{A}) \Rightarrow 3\,\text{mA}$$

and the emitter current is

$$I_E = (1 + \beta)\, I_B = (201)(15\,\mu\text{A}) \Rightarrow 3.02\,\text{mA}$$

From Equation (3.23(b)), the collector-emitter voltage is

$$V_{CE} = V_{CC} - I_C R_C = 10 - (3)(2) = 4\,\text{V}$$

Comment: Since $V_{BB} > V_{BE}(\text{on})$ and $V_{CE} > V_{BE}(\text{on})$, the transistor is indeed biased in the forward-active mode. As a note, in an actual circuit, the voltage across a B–E junction may not be exactly 0.7 V, as we have assumed using the piecewise linear approximation. This may lead to slight inaccuracies between the calculated currents and voltages and the measured values. Also note that, if we take the difference between I_E and I_C, which is the base current, we obtain $I_B = 20\,\mu\text{A}$ rather than $15\,\mu\text{A}$. The difference is the result of roundoff error in the emitter current.

Figure 3.20(a) shows a common-emitter circuit with a pnp bipolar transistor, and Figure 3.20(b) shows the dc equivalent circuit. In this circuit, the emitter is at ground potential, which means that the polarities of the V_{BB}

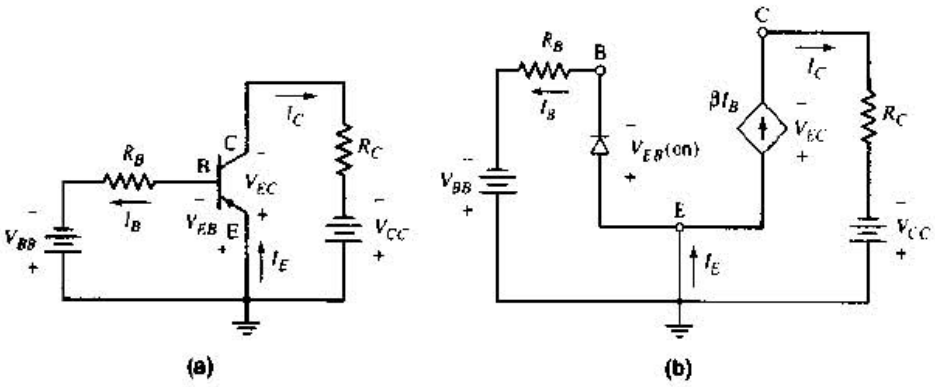


Figure 3.20 (a) Common-emitter circuit with a pnp transistor and (b) dc equivalent circuit using piecewise linear parameters

and V_{CC} power supplies must be reversed compared to those in the npn circuit. The analysis proceeds exactly as before, and we can write

$$I_B = \frac{V_{BB} - V_{EB}(\text{on})}{R_B} \tag{3.24}$$

$$I_C = \beta I_B \tag{3.25}$$

and

$$V_{EC} = V_{CC} - I_C R_C \tag{3.26}$$

We can see that Equations (3.24), (3.25), and (3.26) for the pnp bipolar transistor in the common-emitter configuration are exactly the same as Equations (3.21), (3.22), and (3.23(b)) for the npn bipolar transistor in a similar circuit, if we properly define the current directions and voltage polarities.

In many cases, the pnp bipolar transistor will be reconfigured in a circuit so that positive voltage sources, rather than negative ones, can be used. We see this in the following example.

Example 3.4 **Objective:** Analyze the common-emitter circuit with a pnp transistor.

For the circuit shown in Figure 3.21(a), the parameters are: $V_{BB} = 1.5\,\text{V}$, $R_B = 580\,\text{k}\Omega$, $V_{CC} = 5\,\text{V}$, $V_{EB}(\text{on}) = 0.6\,\text{V}$, and $\beta = 100$. Find I_B, I_C, I_E, and R_C such that $V_{EC} = (\frac{1}{2})V_{CC}$.

Solution: Writing a Kirchhoff voltage law equation around the E-B loop, we find the base current to be

$$I_B = \frac{V_{CC} - V_{EB}(\text{on}) - V_{BB}}{R_B} = \frac{5 - 0.6 - 1.5}{580} \Rightarrow 5\,\mu\text{A}$$

The collector current is

$$I_C = \beta I_B = (100)(5\,\mu\text{A}) \Rightarrow 0.5\,\text{mA}$$

and the emitter current is

$$I_E = (1 + \beta)I_B = (101)(5\,\mu\text{A}) \Rightarrow 0.505\,\text{mA}$$

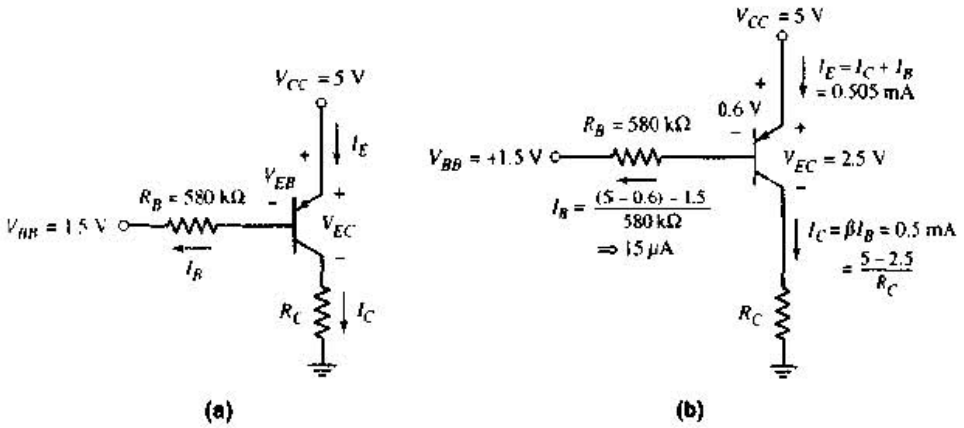


Figure 3.21 *Circuit for Example 3.4*

For a C–E voltage of $V_{EC} = \frac{1}{2}V_{CC} = 2.5$ V, R_C is

$$R_C = \frac{V_{CC} - V_{EC}}{I_C} = \frac{5 - 2.5}{0.5} = 5\,\text{k}\Omega$$

Comment: In this case, the difference between V_{CC} and V_{BB} is greater than the transistor turn-on voltage, or $(V_{CC} - V_{BB}) > V_{EB}(\text{on})$. Also, because $V_{EC} > V_{EB}(\text{on})$, the pnp bipolar transistor is biased in the forward-active mode.

Discussion: In this example, we used an emitter-base turn-on voltage of $V_{EB}(\text{on}) = 0.6$ V, whereas previously we used a value of 0.7 V. We must keep in mind that the turn-on voltage is an approximation and the actual base–emitter voltage will depend on the type of transistor used and the current level. In most situations, choosing a value of 0.6 V or 0.7 V will make only minor differences. However, most people tend to use the value of 0.7 V.

The dc equivalent circuits, such as those given in Figures 3.18(b) and 3.20(b), are useful initially in analyzing transistor circuits. From this point on, however, we will not explicitly draw the equivalent circuit. We will simply analyze the circuit using the transistor circuit symbols, as in Figures 3.19 and 3.21.

3.2.2 Load Line and Modes of Operation

The load line can help us visualize the characteristics of a transistor circuit. For the common-emitter circuit in Figure 3.19(a), we can use a graphical technique for both the B–E and C–E portions of the circuit. Figure 3.22(a) shows the piecewise linear characteristics for the B–E junction and the input load line. The input load line is obtained from Kirchhoff's voltage law equation around the B–E loop, written as follows:

$$I_B = \frac{V_{BB}}{R_B} - \frac{V_{BE}}{R_B} \tag{3.27}$$

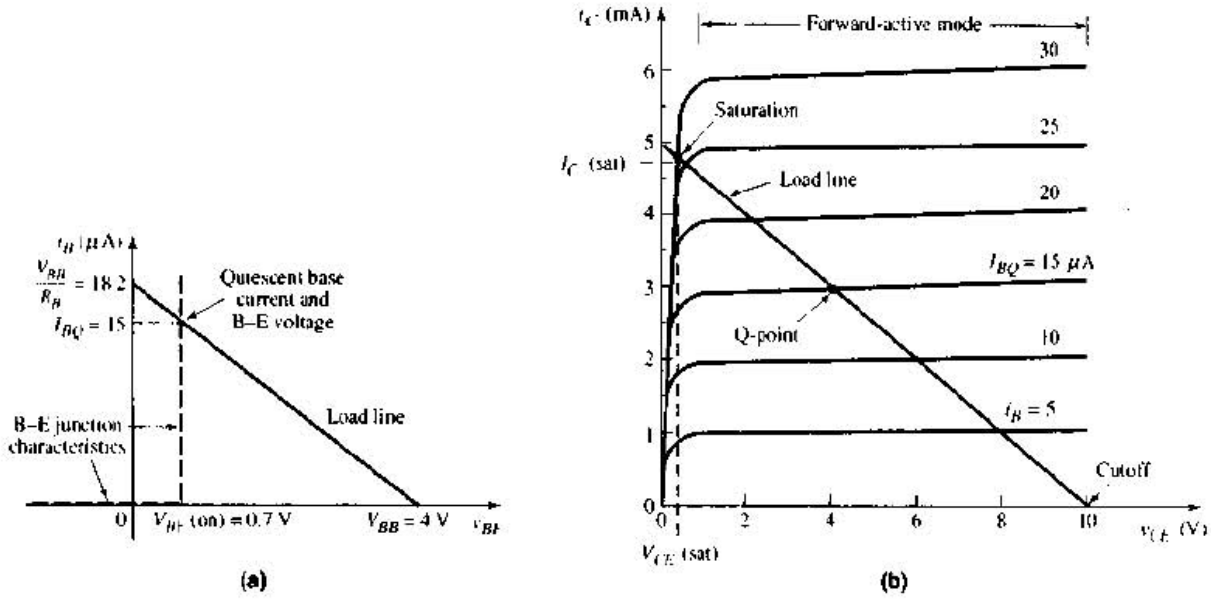


Figure 3.22 (a) Base–emitter junction characteristics and the input load line and (b) common-emitter transistor characteristics and the collector–emitter load line

Both the load line and the quiescent base current change as either or both V_{BB} and R_B change. The load line in Figure 3.22(a) is essentially the same as the load line characteristics for diode circuits, as shown in Chapter 1.

For the C–E portion of the circuit in Figure 3.19(a), the load line is found by writing Kirchhoff's voltage law equation around the C–E loop. We obtain

$$V_{CE} = V_{CC} - I_C R_C \tag{3.28(a)}$$

which can be written in the form

$$I_C = \frac{V_{CC}}{R_C} - \frac{V_{CE}}{R_C} = 5 - \frac{V_{CE}}{2}\ (\text{mA}) \tag{3.28(b)}$$

Equation (3.28(b)) is the load line equation, showing a linear relationship between the collector current and collector–emitter voltage. Since we are considering the dc analysis of the transistor circuit, this relationship represents the dc load line. The ac load line is presented in the next chapter.

Figure 3.22(b) shows the transistor characteristics for the transistor in Example 3.3, with the load line superimposed on the transistor characteristics. The two end points of the load line are found by setting $I_C = 0$, yielding $V_{CE} = V_{CC} = 10$ V, and by setting $V_{CE} = 0$, yielding $I_C = V_{CC}/R_C = 5$ mA.

The quiescent point, or Q-point, of the transistor is given by the dc collector current and the collector–emitter voltage. The Q-point is the intersection of the load line and the I_C versus V_{CE} curve corresponding to the appropriate base current. The Q-point also represents the simultaneous solution to two expressions. The load line is useful in visualizing the bias point of the transistor. In the figure, the Q-point shown is for the transistor in Example 3.3.

As previously stated, if the power supply voltage in the base circuit is smaller than the turn-on voltage, then $V_{BB} < V_{BE}$(on) and $I_B = I_C = 0$, and the transistor is in the cutoff mode. In this mode, all transistor currents are

zero, neglecting leakage currents, and for the circuit shown in Figure 3.19(a), $V_{CE} = V_{CC} = 10\,\text{V}$.

As V_{BB} increases ($V_{BB} > V_{BE}(\text{on})$), the base current I_B increases and the Q-point moves up the load line. As I_B continues to increase, a point is reached where the collector current I_C can no longer increase. At this point, the transistor is biased in **the saturation mode**; that is, the transistor is said to be in saturation. The B–C junction becomes forward biased, and the relationship between the collector and base currents is no longer linear. The transistor C–E voltage in saturation, $V_{CE}(\text{sat})$, is less than the B–E cut-in voltage. The forward-biased B–C voltage is always less than the forward-biased B–E voltage, so the C–E voltage in saturation is a small positive value. Typically, $V_{CE}(\text{sat})$ is in the range of 0.1 to 0.3 V.

Example 3.5 **Objective:** Calculate the currents and voltages in a circuit when the transistor is driven into saturation.

For the circuit shown in Figure 3.23, the transistor parameters are: $\beta = 100$, and $V_{BE}(\text{on}) = 0.7\,\text{V}$. If the transistor is biased in saturation, assume $V_{CE}(\text{sat}) = 0.2\,\text{V}$.

Solution: Since +8 V is applied to the input side of R_B, the base–emitter junction is certainly forward biased, so the transistor is turned on. The base current is

$$I_B = \frac{V_{BB} - V_{BE}(\text{on})}{R_B} = \frac{9 - 0.7}{220} \Rightarrow 33.2\,\mu\text{A}$$

If we first assume that the transistor is biased in the active region, then the collector current is

$$I_C = \beta I_B = (100)(33.2\,\mu\text{A}) \Rightarrow 3.32\,\text{mA}$$

The collector–emitter voltage is then

$$V_{CE} = V_{CC} - I_C R_C = 10 - (3.32)(4) = -3.28\,\text{V}$$

However, the collector–emitter voltage of the npn transistor in the common-emitter configuration shown in Figure 3.23(a) cannot be negative. Therefore, our initial assumption of the transistor being biased in the forward-active mode is incorrect. Instead, the transistor must be biased in saturation.

As given in the "objective" statement, set $V_{CE}(\text{sat}) = 0.2\,\text{V}$. The collector current is

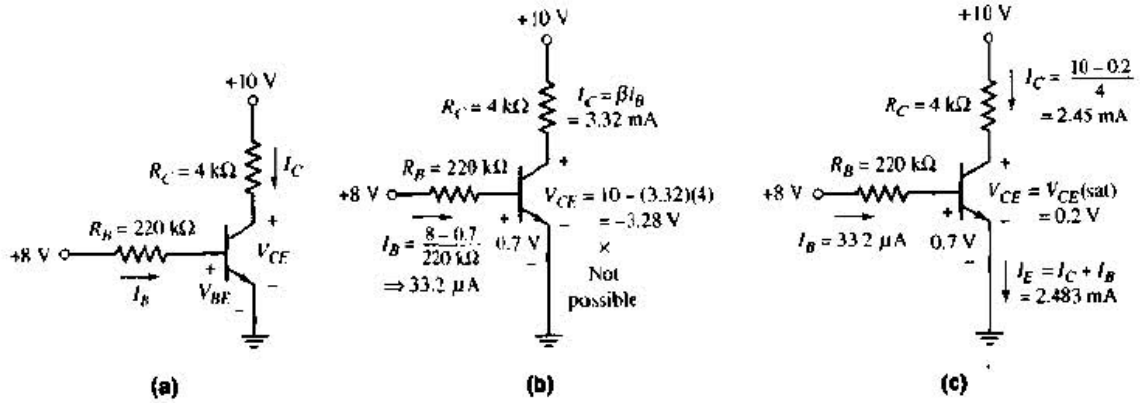


Figure 3.23 Circuit for Example 3.5

$$I_C \simeq I_C(\text{sat}) = \frac{V_{CC} - V_{CE}(\text{sat})}{R_C} \simeq \frac{10 - 0.2}{4} = 2.45\,\text{mA}$$

Assuming that the B–E voltage is still equal to $V_{BE}(\text{on}) = 0.7\,\text{V}$, the base current is $I_B = 33.2\,\mu\text{A}$, as previously determined. If we take the ratio of collector current to base current, then

$$\frac{I_C}{I_B} = \frac{2.45}{0.0332} = 74 < \beta$$

The emitter current is

$$I_E = I_C + I_B \simeq 2.45 + 0.033 = 2.48\,\text{mA}$$

Comment: When a transistor is driven into saturation, we use $V_{CE}(\text{sat})$ as another piecewise linear parameter. In addition, when a transistor is biased in the saturation mode, we have $I_C < \beta I_B$. This condition is very often used to prove that a transistor is indeed biased in the saturation mode.

Problem-Solving Technique: Bipolar DC Analysis

Analyzing the dc response of a bipolar transistor circuit requires knowing the mode of operation of the transistor. In some cases, the mode of operation may not be obvious, which means that we have to guess the state of the transistor, then analyze the circuit to determine if we have a solution consistent with our initial guess. To do this, we can:

1. Assume that the transistor is biased in the forward-active mode in which case $V_{BE} \simeq V_{BE}(\text{on})$, $I_B > 0$, and $I_C = \beta I_B$.
2. Analyze the "linear" circuit with this assumption.
3. Evaluate the resulting state of the transistor. If the initial assumed parameter values and $V_{CE} > V_{CE}(\text{sat})$ are true, then the initial assumption is correct. However, if $I_B < 0$, then the transistor is probably cut off, and if $V_{CE} < 0$, the transistor is likely biased in saturation.
4. If the initial assumption is proven incorrect, then a new assumption must be made and the new "linear" circuit must be analyzed. Step 3 must then be repeated.

Because it is not always clear whether a transistor is biased in the forward-active or saturation mode, we may initially have to make an educated guess as to the state of the transistor and then verify our initial assumption. This is similar to the process we used for the analysis of multidiode circuits. For instance, in Example 3.5, we assumed a forward-active mode, performed the analysis, and showed that $V_{CE} < 0$. However, a negative V_{CE} for an npn transistor in the common-emitter configuration is not possible. Therefore, our initial assumption was disproved, and the transistor was biased in the saturation mode. Using the results of Example 3.5, we also see that when a transistor is in saturation, the ratio of I_C to I_B is always less than β, or

$$I_C/I_B < \beta$$

This condition is true for both the npn and the pnp transistor biased in the saturation mode.

Another mode of operation for a bipolar transistor is the **inverse-active mode**. In this mode, the B–E junction is reverse biased and the B–C junction is forward biased. In effect, the transistor is operating "upside down"; that is, the emitter is acting as the collector and the collector is operating as the emitter. We will postpone discussions on this operating mode until we discuss digital electronic circuits later in this text.

To summarize, the four modes of operation for an npn transistor are shown in Figure 3.24. The four possible combinations of B–E and B–C voltages determine the modes of operation. If $v_{BE} > 0$ (forward-biased junction) and $v_{BC} < 0$ (reverse-biased junction), the transistor is biased in the forward-active mode. If both junctions are zero or reverse biased, the transistor is in cutoff. If both junctions are forward biased, the transistor is in saturation. If the B–E junction is reverse biased and the B–C junction is forward biased, the transistor is in the inverse-active mode.

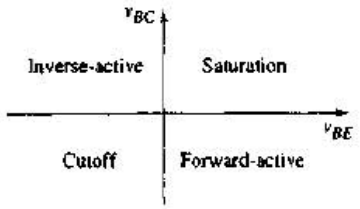


Figure 3.24 Bias conditions for the four modes of operation of an npn transistor

Test Your Understanding

3.9 For the circuit shown in Figure 3.25, assume $\beta = 50$. Determine V_O, I_B, and I_C for: (a) $V_I = 0.2\,\text{V}$, and (b) $V_I = 3.6\,\text{V}$. Then, calculate the power dissipated in the transistor for the two conditions. (Ans. (a) $I_B = I_C = 0$, $V_O = 5\,\text{V}$, $P = 0$; (b) $I_B = 4.53\,\text{mA}$, $I_C = 10.9\,\text{mA}$, $P = 5.35\,\text{mW}$)

3.10 For the circuit shown in Figure 3.25, let $\beta = 50$, and determine V_I such that $V_{BC} = 0$. Calculate the power dissipated in the transistor. (Ans. $V_I = 0.825\,\text{V}$, $P = 6.98\,\text{mW}$)

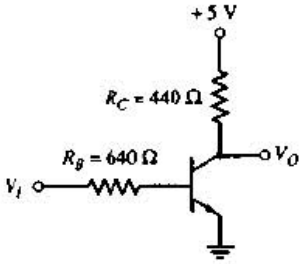


Figure 3.25 Figure for Exercises 3.9 and 3.10

3.2.3 Common Bipolar Circuits: DC Analysis

There are a number of other bipolar transistor circuit configurations in addition to the common-emitter circuits shown in Figures 3.19 and 3.21. Several examples of such circuits are presented in this section. BJT circuits tend to be very similar in terms of dc analysis procedures, so that the same basic analysis approach will work regardless of the appearance of the circuit. We continue our dc analysis and design of bipolar circuits to increase our proficiency and to become more comfortable with these types of circuits.

Example 3.6 **Objective:** Calculate the characteristics of a circuit containing an emitter resistor.

For the circuit shown in Figure 3.26(a), let $V_{BE}(\text{on}) = 0.7\,\text{V}$ and $\beta = 75$.

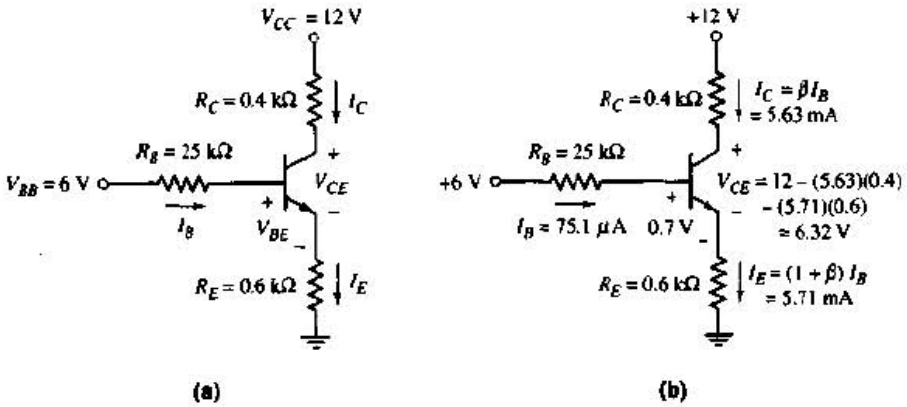


Figure 3.26 Circuit for Example 3.6

Solution:

***Q*-Point Values:**

Writing the Kirchhoff's voltage law equation around the B–E loop, we have

$$V_{BB} = I_B R_B + V_{BE}(\text{on}) + I_E R_E \tag{3.29}$$

Assuming the transistor is biased in the forward-active mode, we can write $I_E = (1 + \beta) I_B$. We can then solve Equation (3.29) for the base current:

$$I_B = \frac{V_{BB} - V_{BE}(\text{on})}{R_B + (1 + \beta) R_E} = \frac{6 - 0.7}{25 + (76)(0.6)} \Rightarrow 75.1\,\mu\text{A}$$

The collector and emitter currents are

$$I_C = \beta I_B = (75)(75.1\,\mu\text{A}) \Rightarrow 5.63\,\text{mA}$$

and

$$I_E = (1 + \beta) I_B = (76)(75.1\,\mu\text{A}) \Rightarrow 5.71\,\text{mA}$$

Referring to Figure 3.26(b), the collector–emitter voltage is

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E = 12 - (5.63)(0.4) - (5.71)(0.6)$$

or

$$V_{CE} = 6.32\,\text{V}$$

Solution:

Load Line:

We again use Kirchhoff's voltage law around the C–E loop. From the relationship between the collector and emitter currents, we find

$$V_{CE} = V_{CC} - I_C \left[R_C + \left(\frac{1 + \beta}{\beta} \right) R_E \right] = 12 - I_C \left[0.4 + \left(\frac{76}{75} \right) (0.6) \right]$$

or

$$V_{CE} = 12 - I_C (1.01)$$

The load line and the calculated Q-point are shown in Figure 3.27. A few transistor characteristics of I_C versus V_{CE} are superimposed on the figure.

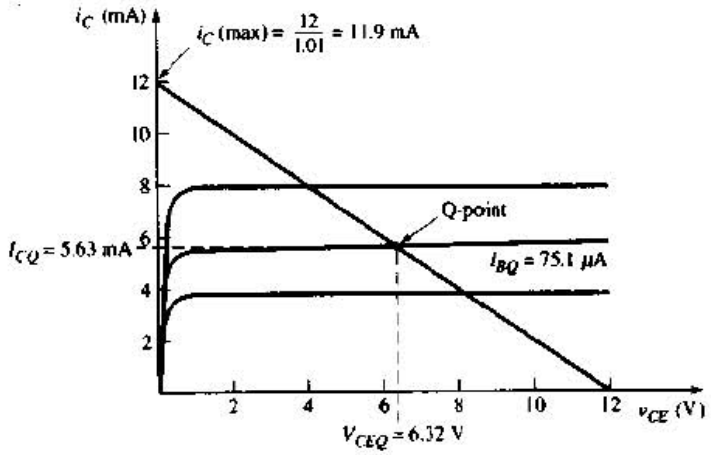


Figure 3.27 Load line for the circuit in Figure 3.26

Comment: Since the C–E voltage is 6.32 V, $V_{CE} > V_{BE}(\text{on})$ and the transistor is biased in the forward-active mode, as initially assumed. We will see, later in the chapter, the value of including an emitter resistor in a circuit.

Example 3.7 **Objective:** Calculate the characteristics of a circuit containing both a positive and a negative power supply voltage.

For the circuit shown in Figure 3.28, let $V_{BE}(\text{on}) = 0.65$ V and $\beta = 100$. Even though the base is at ground potential, the B–E junction is forward biased through R_E and V^-.

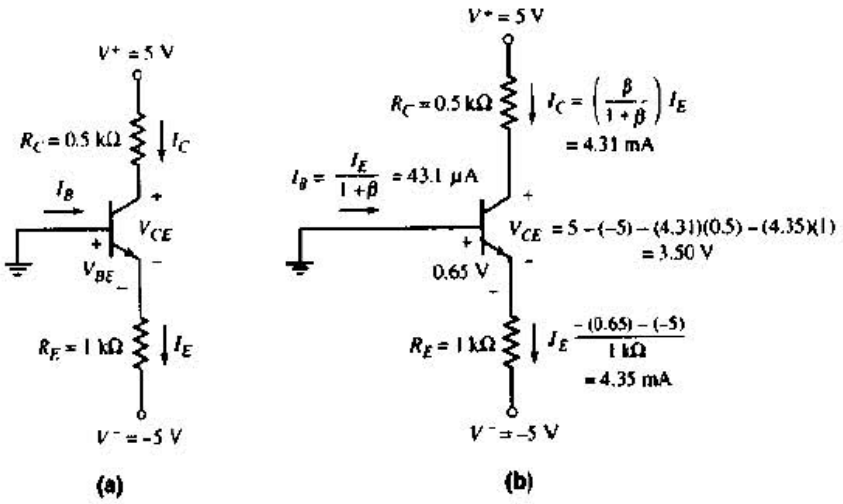


Figure 3.28 Circuit for Example 3.7

Solution:
***Q*-Point Values:**
Writing the Kirchhoff's voltage law equation around the B–E loop, we have

$$0 = V_{BE}(\text{on}) + I_E R_E + V^-$$

which yields

$$I_E = \frac{-V^- - V_{BE}(\text{on})}{R_E} = \frac{-(-5) - 0.65}{1} = 4.35\,\text{mA}$$

The base current is

$$I_B = \frac{I_E}{1+\beta} = \frac{4.35}{101} \Rightarrow 43.1\,\mu\text{A}$$

and the collector current is

$$I_C = \left(\frac{\beta}{1+\beta}\right) I_E = \left(\frac{100}{101}\right) \cdot (4.35) = 4.31\,\text{mA}$$

Referring to Figure 3.28(b), the C–E voltage is

$$V_{CE} = V^+ - I_C R_C - I_E R_E - V^-$$

or

$$V_{CE} = 5 - (4.31)(0.5) - (4.35)(1) - (-5) = 3.50\,\text{V}$$

Solution:
Load Line:
The load line equation is

$$V_{CE} = (V^+ - V^-) - I_C\left[R_C + \left(\frac{1+\beta}{\beta}\right)R_E\right] = (5 - (-5)) - I_C\left[0.5 + \left(\frac{101}{100}\right)(1)\right]$$

or

$$V_{CE} = 10 - I_C(1.51)$$

The load line and the calculated *Q*-point are shown in Figure 3.29.

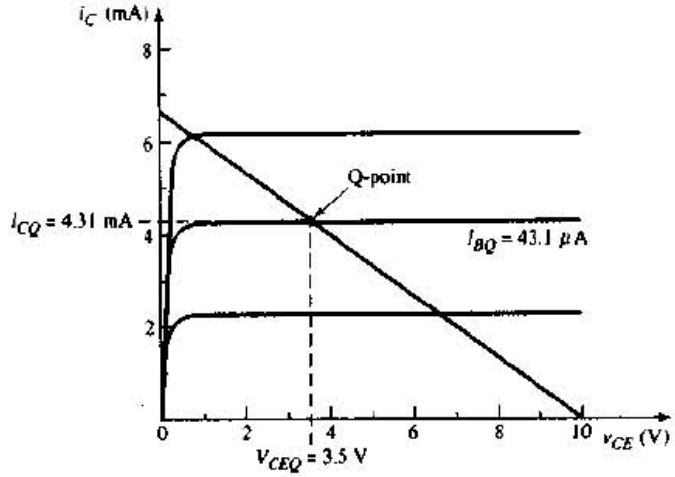


Figure 3.29 Load line for the circuit in Figure 3.28

Comment: The B–E junction is forward biased, even though V_{BB} is at ground potential. The forward-bias voltage is a result of the negative potential V^- applied at the "bottom" of the emitter resistor R_E. The transistor is biased in the forward-active mode.

Test Your Understanding

(Note: In the following exercises, assume the B–E cut-in voltage is 0.7 V for both the npn and pnp transistors. Also assume that the C–E saturation voltage is 0.2 V for each type of transistor.)

RD3.11 Redesign the circuit shown in Figure 3.30 such that $I_{CQ} = 1.5\,\text{mA}$ and $V_C = +4\,\text{V}$. Assume $\beta = 100$. (Ans. $R_C = 4\,\text{k}\Omega$, $R_E = 6.14\,\text{k}\Omega$)

3.12 For the circuit shown in Figure 3.31, the measured value of V_C is $V_C = +6.34\,\text{V}$. Determine I_B, I_E, I_C, V_{CE}, β, and α (Ans. $I_C = 0.915\,\text{mA}$, $I_E = 0.930\,\text{mA}$, $\alpha = 0.9839$, $I_B = 15.0\,\mu\text{A}$, $\beta = 61$, $V_{CE} = 7.04\,\text{V}$)

3.13 Determine I_B, I_C, I_E, and V_{EC}, assuming $\beta = 50$ for the circuit shown in Figure 3.32. (Ans. $I_E = 1.16\,\text{mA}$, $I_B = 22.7\,\mu\text{A}$, $I_C = 1.14\,\text{mA}$, $V_{EC} = 6.14\,\text{V}$)

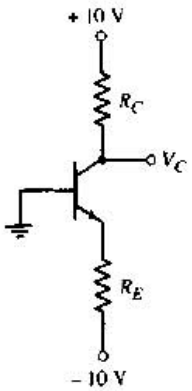


Figure 3.30 Figure for Exercise 3.11

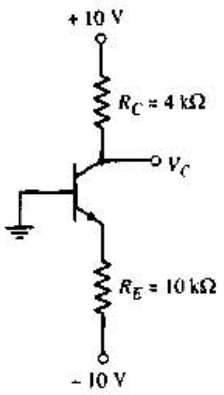


Figure 3.31 Figure for Exercise 3.12

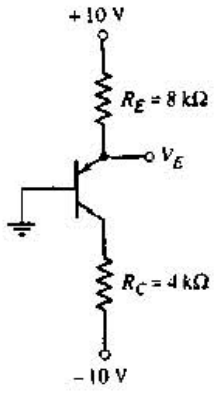


Figure 3.32 Figure for Exercise 3.13

Design Example 3.8 **Objective:** Design a pnp bipolar transistor circuit.

For the circuit shown in Figure 3.33(a), let $V_{EB}(\text{on}) = 0.6\,\text{V}$ and $\beta = 60$. Design the circuit such that $V_{ECQ} = 2.5\,\text{V}$.

Solution:

***Q*-Point Values:**

Writing the Kirchhoff's voltage law equation around the E–C loop, we obtain

$$V^+ = I_E R_E + V_{EC}$$

or

$$5 = I_E(2) + 2.5$$

which yields $I_E = 1.25\,\text{mA}$. The collector current is

$$I_C = [\beta/(1+\beta)]I_E = [(60)/61](1.25) = 1.23\,\text{mA}$$

The base current is

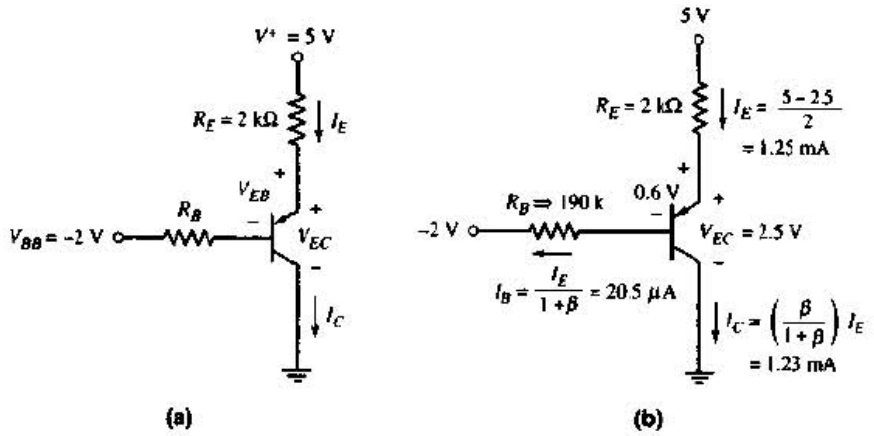


Figure 3.33 Circuit for Example 3.8

$$I_B = I_E/(1+\beta) = 1.25/61 = 0.0205\,\text{mA}$$

Writing the Kirchhoff's voltage law equation around the E–B loop, we find

$$V^+ = I_E R_E + V_{EB}(\text{on}) + I_B R_B + V_{BB}$$

or

$$5 = (1.25)(2) + 0.6 + (0.0205)R_B + (-2)$$

which yields $R_B = 190\,\text{k}\Omega$.

Solution:

Load Line:

The load line equation is

$$V_{EC} = V^+ - I_E R_E = V^+ - I_C\left(\frac{1+\beta}{\beta}\right)R_E$$

or

$$V_{EC} = 5 - I_C\left(\frac{61}{60}\right)(2) = 5 - I_C(2.03)$$

The load line and calculated Q-point are shown in Figure 3.34.

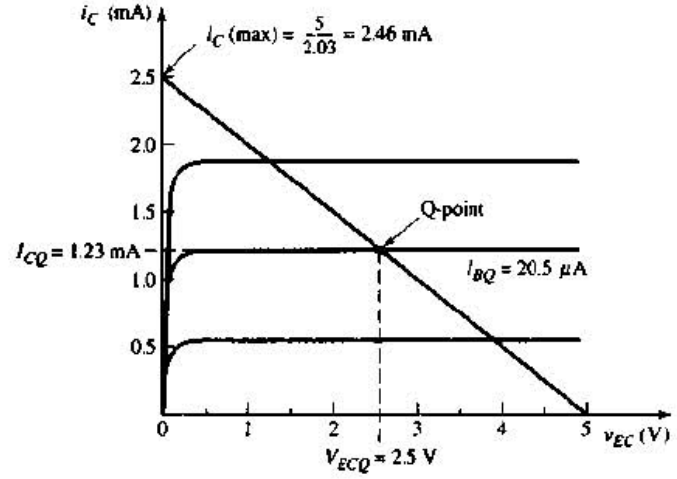


Figure 3.34 Load line for the circuit in Figure 3.33

Comment: Even though there is no collector resistor, there is still a collector current. Also, the transistor is biased in the forward-active mode.

Computer Simulation: It is often desirable to verify a transistor circuit design with a computer simulation. This verification becomes more important as the complexity of the circuit increases and as the complexity of the transistor model increases.

As an introduction to computer simulation, a PSpice analysis of the circuit design shown in Figure 3.33(b) was performed. Figure 3.35 shows the PSpice circuit schematic. A standard 2N3906 transistor from the circuit library was used. Shown below are the schematic's netlist that was created; a partial listing of the transistor parameters, and the resulting Q-point values.

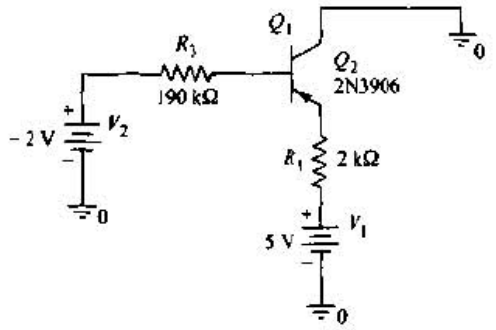


Figure 3.35 PSpice circuit schematic for Example 3.8

```
          *Schematics Netlist*
 Q_Q1   0 $N_0001 $N_0002 Q2N3906
 V_V2   $N_0003 0 -2V
 V_V1   $N_0004 0 5V
 R_R3   $N_0003 $N_0001 190K
 R_R1   $N_0004 $N_0002 2K

     Q2N3906          **** BIPOLAR JUNCTION TRANSISTORS
     PNP
  IS   1.410000E-15
  BF 180.7              NAME          Q_Q1
  NF   1                MODEL         Q2N3906
 VAF  18.7              IB           -1.15E-05
 IKF    .08             IC           -2.04E-03
  BR   4.977            VBE          -7.25E-01
  NR   1                VBC           1.77E-01
  RB  10                VCE          -9.01E-01
 RBM  10                BETADC        1.78E+02
  RC   2.5
```

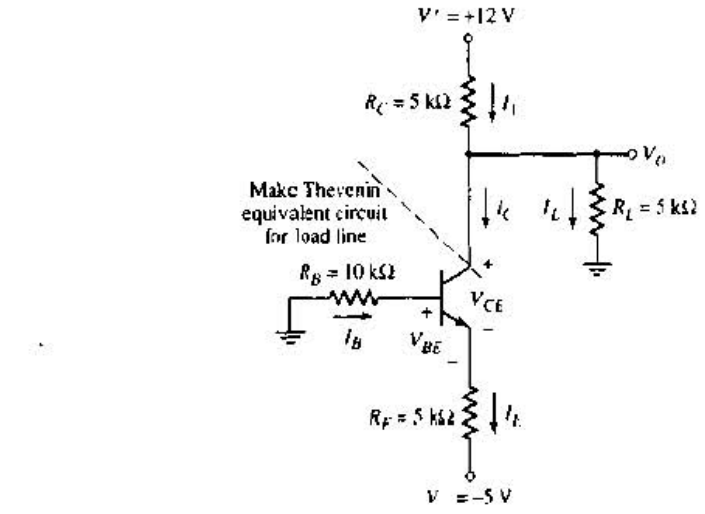
We see that the current gain β_F of the 2N3906 is approximately 180 compared to the assumed value of 60 used in the design calculations. This important difference produces an emitter–collector voltage of $V_{EC} = 0.901$ V compared to the desired value of 2.5 V. Using the value of $\beta_F = 180$, a new value of R_3 would need to be determined to produce the desired V_{EC} value.

Discussion: This example illustrates one extremely important point. In order for the computer simulation to accurately predict the circuit response, the transistor parameters must be known. In the above design, if the circuit is to actually function properly with

$\beta_F = 60$, then the transistor in the PSpice analysis would need to be changed and a different transistor with the proper parameters would need to be used. However, for a given device model, PSpice can determine the value of β_F depending on operating point and temperature.

Example 3.9 **Objective:** Calculate the characteristics of an npn bipolar circuit with a load resistance. The load resistance can represent a second transistor stage connected to the output of a transistor circuit.

For the circuit shown in Figure 3.36(a), the transistor parameters are: $V_{BE}(\text{on}) = 0.7\,\text{V}$, and $\beta = 100$.



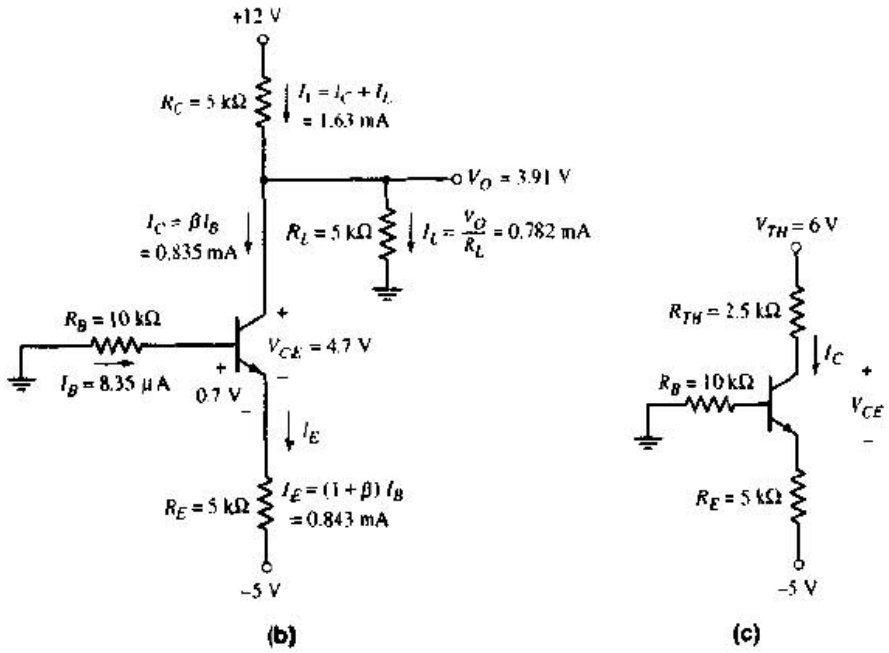


Figure 3.36 Circuit for Example 3.9

Solution:

***Q*-Point Values:**

Kirchhoff's voltage law equation around the B–E loop yields

$$I_B R_B + V_{BE}(\text{on}) + I_E R_E + V^- = 0$$

Again assuming $I_E = (1+\beta)I_B$, we find

$$I_B = \frac{-(V^- + V_{BE}(\text{on}))}{R_B + (1+\beta)R_E} = \frac{-(-5+0.7)}{10+(101)(5)} \Rightarrow 8.35\,\mu\text{A}$$

The collector and emitter currents are

$$I_C = \beta I_B = (100)(8.35\,\mu\text{A}) \Rightarrow 0.835\,\text{mA}$$

and

$$I_E = (1+\beta)I_B = (101)(8.35\,\mu\text{A}) \Rightarrow 0.843\,\text{mA}$$

At the collector node, we can write

$$I_C = I_1 - I_L = \frac{V^+ - V_O}{R_C} - \frac{V_O}{R_L}$$

or

$$0.835 = \frac{12 - V_O}{5} - \frac{V_O}{5}$$

Solving for V_O, we get $V_O = 3.91\,\text{V}$. The currents are then $I_1 = 1.62\,\text{mA}$ and $I_L = 0.782\,\text{mA}$. Referring to Figure 3.36(b), the collector–emitter voltage is

$$V_{CE} = V_O - I_E R_E - (-5) = 3.91 - (0.843)(5) - (-5) = 4.70\,\text{V}$$

Solution:

Load Line:

The load line equation for this circuit is not as straightforward as for previous circuits. The easiest approach to finding the load line is to make a "Thevenin equivalent circuit" of R_L, R_C, and V^+, as indicated in Figure 3.36(a). (Thevenin equivalent circuits are also covered later in this chapter, in Section 3.4.) The Thevenin equivalent resistance is

$$R_{TH} = R_L \| R_C = 5 \| 5 = 2.5\,\text{k}\Omega$$

and the Thevenin equivalent voltage is

$$V_{TH} = \left(\frac{R_L}{R_L + R_C}\right) \cdot V^+ = \left(\frac{5}{5+5}\right) \cdot (12) = 6\,\text{V}$$

The equivalent circuit is shown in Figure 3.36(c). The Kirchhoff voltage law equation around the C–E loop is

$$V_{CE} = (6 - (-5)) - I_C R_{TH} - I_E R_E = 11 - I_C(2.5) - I_C\left(\frac{101}{100}\right) \cdot (5)$$

or

$$V_{CE} = 11 - I_C(7.55)$$

The load line and the calculated *Q*-point values are shown in Figure 3.37.

Comment: Remember that the collector current, determined from $I_C = \beta I_B$, is the current into the collector terminal of the transistor; it is not necessarily the current in the collector resistor R_C.

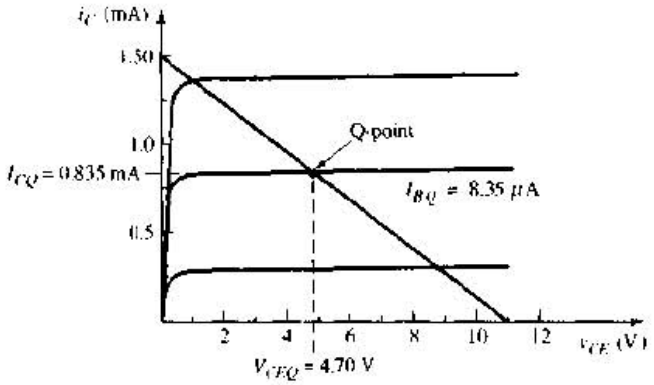


Figure 3.37 Load line for the circuit in Figure 3.36(a)

Test Your Understanding

RD3.14 For the transistor shown in the circuit of Figure 3.38, the common-base current gain is $\alpha = 0.9920$. Determine R_E such that the emitter current is limited to $I_E = 1.0\,\text{mA}$. Also determine I_B, I_C, and V_{BC}. (Ans. $R_E = 3.3\,\text{k}\Omega$, $I_C = 0.992\,\text{mA}$, $I_B = 8.0\,\mu\text{A}$, $V_{BC} = 4.01$ V)

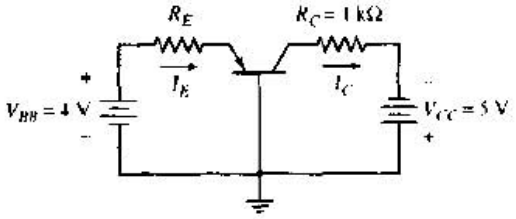


Figure 3.38 Figure for Exercise 3.14

3.15 For the circuit shown in Figure 3.39, determine I_E, I_B, I_C, and V_{CE}, if $\beta = 75$. (Ans. $I_B = 15.1\,\mu\text{A}$, $I_C = 1.13\,\text{mA}$, $I_E = 1.15\,\text{mA}$, $V_{CE} = 6.03$ V)

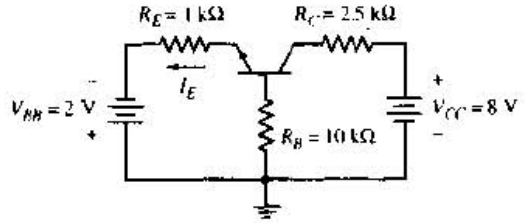


Figure 3.39 Figure for Exercise 3.15

RD3.16 Let $\beta = 100$ for the circuit shown in Figure 3.40. Determine R_E such that $V_{CE} = 2.5$ V. (Ans. $R_E = 138\,\Omega$)

3.17 For the circuit shown in Figure 3.41, assume $\beta = 50$ and determine V_{BB} such that $I_E = 2.2\,\text{mA}$. Then, find I_C and V_{EC}. (Ans. $I_C = 2.16\,\text{mA}$, $V_{BB} = 5.06$ V, $V_{EC} = 2.8$ V)

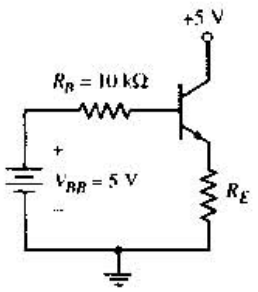


Figure 3.40 Figure for Exercise 3.16

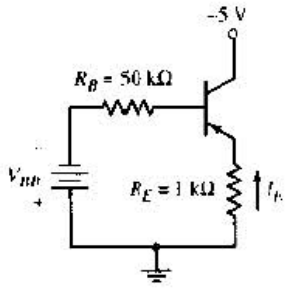


Figure 3.41 Figure for Exercise 3.17

3.3 BASIC TRANSISTOR APPLICATIONS

Transistors can be used to: switch currents, voltages, and power; perform digital logic functions; and amplify time-varying signals. In this section, we consider the switching properties of the bipolar transistor, analyze a simple transistor digital logic circuit, and then show how the bipolar transistor is used to amplify time-varying signals.

3.3.1 Switch

Figure 3.42 shows a bipolar circuit called an inverter, in which the transistor in the circuit is switched between cutoff and saturation. The load, for example, could be a motor, a light-emitting diode (see Exercise 3.21), or some other electrical device. If $v_I < V_{BE}(\text{on})$, then $i_B = i_C = 0$ and the transistor is cut off. Since $i_C = 0$, the voltage drop across R_C is zero, so the output voltage is $v_O = V_{CC}$. Also, since the currents in the transistor are zero, the power dissipation in the transistor is zero. If the load were a motor, the motor would be off with zero current. Likewise, if the load were a light-emitting diode, the light output would be zero with zero current.

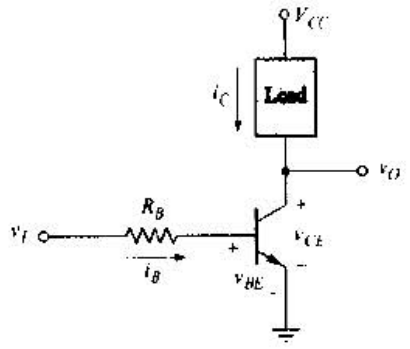


Figure 3.42 An npn bipolar inverter circuit used as a switch

If we let $v_I = V_{CC}$ and if the ratio of R_B to R_C, where R_C is the effective resistance of the load, is less than β, then the transistor is usually driven into saturation, which means that

$$i_B \cong \frac{v_I - V_{BE}(\text{on})}{R_B} \tag{3.30}$$

$$i_C = I_C(\text{sat}) = \frac{V_{CC} - V_{CE}(\text{sat})}{R_C} \tag{3.31}$$

and

$$v_O = V_{CE}(\text{sat}) \tag{3.32}$$

In this case, a collector current is induced that would turn on the motor or the LED, depending on the type of load.

Equation (3.30) assumes that the B- E voltage can be approximated by the turn-on voltage. This approximation will be modified slightly when we discuss bipolar digital logic circuits.

Example 3.10 **Objective:** Calculate the currents, output voltage, and power dissipation in the transistor for the bipolar inverter shown in Figure 3.42.

Assume the circuit and transistor parameters are: $R_B = 240\,\Omega$, $V_{CC} = 12\,\text{V}$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, $V_{CE}(\text{sat}) = 0.1\,\text{V}$, and $\beta = 75$. Assume the load is a motor with an effective resistance of $R_C = 5\,\Omega$.

Solution: For $v_I = 0$, the transistor is cut off, $i_B = i_C = 0$, $v_O = V_{CC} = 12\,\text{V}$, and the power dissipated in the transistor is zero. For $v_I = 12\,\text{V}$,

$$i_B = \frac{v_I - V_{BE}(\text{on})}{R_B} = \frac{12 - 0.7}{240} \Rightarrow 47.1\,\text{mA}$$

Assuming the transistor is in saturation, we find that

$$i_C = \frac{V_{CC} - V_{CE}(\text{sat})}{R_C} = \frac{12 - 0.1}{5} = 2.38\,\text{A}$$

If we take the ratio of collector current to base current, we have

$$\frac{i_C}{i_B} = \frac{2.38}{0.0471} = 50.6 < \beta$$

Since $i_C/i_B < \beta$, the transistor is indeed in saturation, as we initially assumed. Also, since the transistor is in saturation, the output voltage is

$$v_O = V_{CE}(\text{sat}) = 0.1\,\text{V}$$

The power dissipated in the transistor is

$$P = i_C v_{CE} + i_B v_{BE} = (2.38)(0.1) + (0.0471)(0.7)$$

or

$$P = 0.271\,\text{W}$$

Comment: With a collector current of 2.38 A, the transistor would have to be a power transistor. However, from the results we see that we can "switch" a relatively large collector current ($i_C = 2.38\,\text{A}$) using only a relatively small base current ($i_B = 47\,\text{mA}$).

Design Pointer: Motors tend to be inductive, so that during start-up and shutdown a relatively large di/dt voltage could be induced in the circuit. This voltage, especially during shutdown, could cause the transistor to go into breakdown and be damaged.

When a transistor is biased in saturation, the relationship between the collector and base currents is no longer linear. Consequently, this mode of operation cannot be used for linear amplifiers. On the other hand, switching a transistor between cutoff and saturation produces the greatest change in output voltage, which is especially useful in digital logic circuits, as we will see in the next section.

3.3.2 Digital Logic

In the simple transistor inverter circuit shown in Figure 3.43(a), if the input is approximately zero volts, the transistor is in cutoff and the *output* is high and equal to V_{CC}. If, on the other hand, the *input* is high and equal to V_{CC}, the transistor is driven into saturation, and the output is low and equal to $V_{CE}(\text{sat})$.

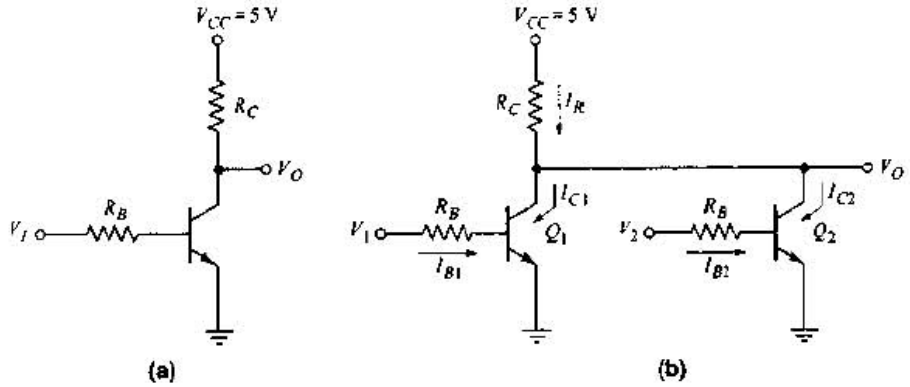


Figure 3.43 A bipolar (a) inverter circuit and (b) NOR logic gate

Now consider the case when a second transistor is connected in parallel, as shown in Figure 3.43(b). When the two inputs are zero, both transistors Q_1 and Q_2 are in cutoff, and $V_O = 5\,\text{V}$. When $V_1 = 5\,\text{V}$ and $V_2 = 0$, transistor Q_1 can be driven into saturation, and Q_2 remains in cutoff. With Q_1 in saturation, the output voltage is $V_O = V_{CE}(\text{sat}) \cong 0.2\,\text{V}$. If we reverse the input voltages so that $V_1 = 0$ and $V_2 = 5\,\text{V}$, then Q_1 is in cutoff, Q_2 can be driven into saturation, and $V_O = V_{CE}(\text{sat}) \cong 0.2\,\text{V}$. If both inputs are high, meaning $V_1 = V_2 = 5\,\text{V}$, then both transistors can be driven into saturation, and $V_O = V_{CE}(\text{sat}) \cong 0.2\,\text{V}$.

Table 3.2 shows these various conditions for the circuit in Figure 3.43(b). In a **positive logic system**, meaning that the larger voltage is a logic 1 and the lower voltage is a logic 0, this circuit performs the **NOR logic function**. The circuit of Figure 3.43(b) is then a two-input bipolar NOR logic circuit.

Table 3.2 The bipolar NOR logic circuit response

V_1 (V)	V_2 (V)	V_O (V)
0	0	5
5	0	0.2
0	5	0.2
5	5	0.2

Example 3.11 **Objective:** Determine the currents and voltages in the circuit shown in Figure 3.43(b).

Assume the transistor parameters are: $\beta = 50$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, and $V_{CE}(\text{sat}) = 0.2\,\text{V}$. Let $R_C = 1\,\text{k}\Omega$ and $R_B = 20\,\text{k}\Omega$. Determine the currents and output voltage for various input conditions.

Solution: The following table indicates the equations and results for this example.

Condition	V_O	I_R	Q_1	Q_2
$V_1 = 0$, $V_2 = 0$	5 V	0	$I_{B1} = I_{C1} = 0$	$I_{B2} = I_{C2} = 0$
$V_1 = 5$ V, $V_2 = 0$	0.2 V	$\frac{5 - 0.2}{1} = 4.48$ mA	$I_{B1} = \frac{5 - 0.7}{20} = 0.215$ mA $I_{C1} = I_R = 4.8$ mA	$I_{B2} = I_{C2} = 0$
$V_1 = 0$, $V_2 = 5$ V	0.2 V	4.8 mA	$I_{B1} = I_{C1} = 0$	$I_{B2} = 0.215$ mA $I_{C2} = I_R = 4.8$ mA
$V_1 = 5$ V, $V_2 = 5$ V	0.2 V	4.8 mA	$I_{B1} = 0.215$ mA $I_{C1} = \frac{I_R}{2} = 2.4$ mA	$I_{B2} = 0.215$ mA $I_{C2} = \frac{I_R}{2} = 2.4$ mA

Comment: In this example, we see that whenever a transistor is conducting, the ratio of collector current to base current is always less than β. This shows that the transistor is in saturation, which occurs when either V_1 or V_2 is 5 V.

This example and the accompanying discussion illustrate that bipolar transistor circuits can be configured to perform logic functions. In Chapter 17, we will see that this circuit can experience loading effects when load circuits or other digital logic circuits are connected to the output. Therefore, logic circuits must be designed to minimize or eliminate such loading effects.

3.3.3 Amplifier

The bipolar inverter circuit shown in Figure 3.43(a) can also be used as an amplifier. We will initially develop the voltage transfer characteristics of a specific inverter circuit and then superimpose a time-varying signal on a dc input voltage.

Example 3.12 **Objective:** Determine the dc voltage transfer characteristics and then the amplification factor of the circuit shown in Figure 3.44(a).

Assume the transistor parameters are: $\beta_F = 100$, $V_A = \infty$, $V_{BE}(\text{on}) = 0.7$ V, and $V_{CE}(\text{sat}) = 0.2$ V.

DC Solution: For $v_I \leq 0.7$ V, Q is cut off and $v_O = 5$ V. For $v_I > 0.7$ V, Q turns on and is biased in the active region, so that

$$i_B = \frac{v_I - V_{BE}(\text{on})}{R_B} = \frac{v_I - 0.7}{100\,\text{k}\Omega}$$

The output voltage is

$$v_O = V^+ - i_C R_C = V^+ - \beta_F i_B R_C$$

or

$$v_O = 5 - (100)\left[\frac{v_I - 0.7}{100\,\text{k}\Omega}\right](4\,\text{k}\Omega) = 7.8 - 4v_I$$

This equation is valid for $v_I \geq 0.7$ V and $v_O \geq V_{CE}(\text{sat}) = 0.2$ V. The input voltage for $v_O = 0.2$ V is found to be $v_I = 1.9$ V. Now, for $v_I > 1.9$ V, the transistor is biased in

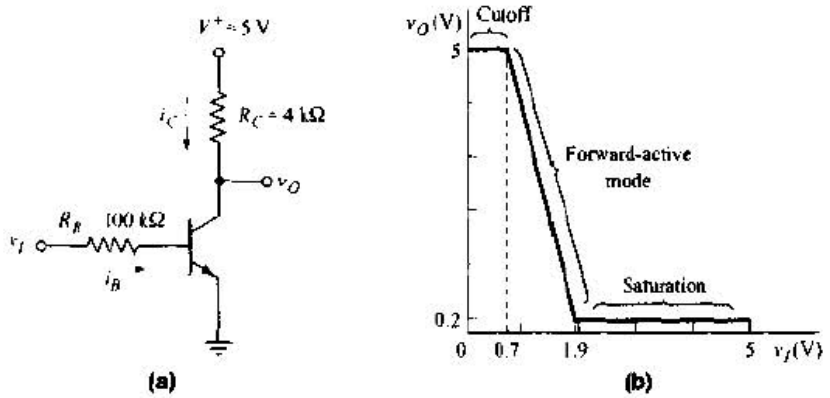


Figure 3.44 (a) A bipolar inverter used as an amplifier; (b) the inverter voltage transfer characteristics

saturation and the output voltage is constant at 0.2 V. The voltage transfer characteristics are shown in Figure 3.44(b).

AC Solution: Now bias the transistor in the center of the active region with an input voltage of $v_I = V_{BB} = 1.3$ V. Also include a second input voltage source, denoted as Δv_I in Figure 3.45(a). The dc output voltage is 2.6 V, which is the Q-point of the transistor.

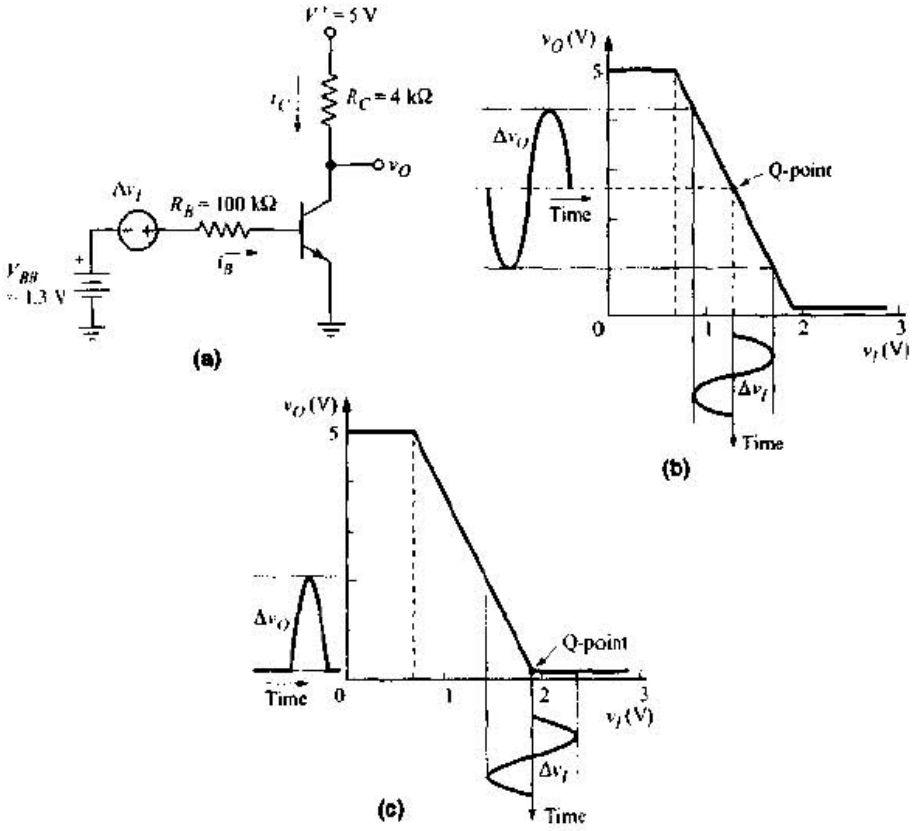


Figure 3.45 (a) The inverter circuit with both a dc and an ac input signal; (b) the dc voltage transfer characteristics, Q-point, and sinusoidal input and output signals; (c) the transfer characteristics showing improper dc biasing

From Figure 3.45(a), we see that the base current is

$$i_B = \frac{V_{BB} + \Delta v_I - V_{BB}(\text{on})}{R_B} = \frac{(1.3 - 0.7) + \Delta v_I}{100\,\text{k}\Omega}$$

where the B–E voltage is assumed to be constant at 0.7 V. The output voltage is

$$v_O = V^+ - i_C R_C = V^+ - \beta_F i_B R_C$$

which can be written as

$$v_O = 5 - (100)\left[\frac{0.6 + \Delta v_I}{100\,\text{k}\Omega}\right](4\,\text{k}\Omega) = 2.6 - 4(\Delta v_I)$$

The change in the output voltage due to the change in the input voltage can be written as

$$\Delta v_O = -4(\Delta v_I)$$

The change in output voltage per change in input voltage is the amplification, or

$$A_v = \frac{\Delta v_O}{\Delta v_I} = -4$$

Comment: As the input voltage changes, we move along the voltage transfer characteristics as shown in Figure 3.35(b). The negative sign occurs because of the inverting property of the circuit.

Discussion: In this example, we have biased the transistor in the center of the active region. If the input signal Δv_I is a sinusoidal function as shown in Figure 3.45(b), then the output signal Δv_O is also a sinusoidal signal, which is the desired response for an analog circuit. (This assumes the magnitude of the sinusoidal input signal is not too large.) If the Q-point, or dc biasing, of the transistor were at $v_I = 1.9$ V and $v_O = 0.2$ V, as in Figure 3.45(c), the output response changes. Shown in the figure is a symmetrical sinusoidal input signal. When the input sinusoidal signal is on its positive cycle, the transistor remains biased in saturation and the output voltage does not change. During the negative half of the input signal, the transistor becomes biased in the active region, so a half sinusoidal output response is produced. The output signal is obviously not a replication of the input signal.

This discussion emphasizes the importance of properly biasing the transistor for analog or amplifier applications. The primary objective of this chapter, as stated previously, is to help readers become familiar with transistor circuits, but it is also to enable them to design the dc biasing of transistor circuits that are to be used in analog applications.

Test Your Understanding

[Note: In the following exercises, assume the B–E cut-in voltage is 0.7 V for both the npn and pnp transistors. Also assume the C–E saturation voltage is 0.2 V for both types of transistor.]

***3.18** Consider the circuit in Figure 3.46. Determine I_B, I_C, I_E, and V_{CE} for $\beta = 80$. (Ans. $I_B = 0.402\,\text{mA}$, $I_C = 0.880\,\text{mA}$, $I_E = 1.28\,\text{mA}$, $V_{CE} = 0.2\,\text{V}$)

3.19 For the circuit in Figure 3.47, assume $\beta = 50$ and determine V_I such that $I_C/I_B = 2$. Determine the values of I_B, I_C, and V_{EC}. (Ans. $V_{EC} = 0.2\,\text{V}$, $I_C = 0.48\,\text{mA}$, $I_B = 0.24\,\text{mA}$, $V_I = -5.5\,\text{V}$)

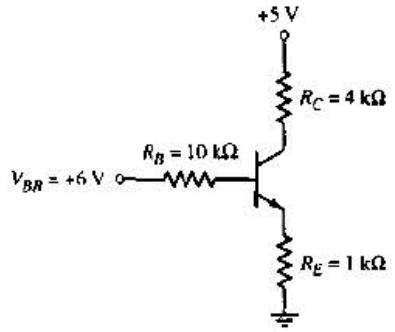


Figure 3.46 Figure for Exercise 3.18

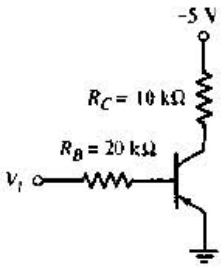


Figure 3.47 Figure for Exercise 3.19

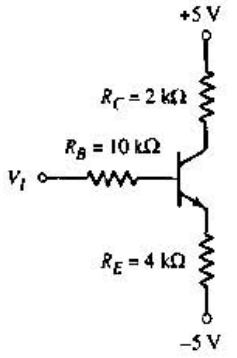


Figure 3.48 Figure for Exercise 3.20

***3.20** For the circuit in Figure 3.48, let $\beta = 75$, and determine I_C, I_E, and V_{CE} for: (a) $V_I = -4.5$ V; (b) $V_I = -3.5$ V; and (c) $V_I = +3.5$ V. (Ans. (a) $I_B = I_C = I_E = 0$, $V_{CE} = 10$ V; (b) $I_B = 2.55\,\mu$A, $I_C = 0.191$ mA, $I_E = 0.194$ mA, $V_{CE} = 8.84$ V; (c) $I_B = 0.112$ mA, $I_C = 1.56$ mA, $I_E = 1.67$ mA, $V_{CE} = 0.2$ V)

D3.21 The transistor in the circuit in Figure 3.49 is used to turn the LED on and off. Assume $\beta_F = 50$ for the transistor and $V_\gamma = 1.5$ V for the LED. Determine the value of R to limit the diode current to 15 mA when the transistor is driven into saturation. Determine R_B such that $I_C/I_B = 20$ when the transistor is driven into saturation for $v_I = 5$ V.

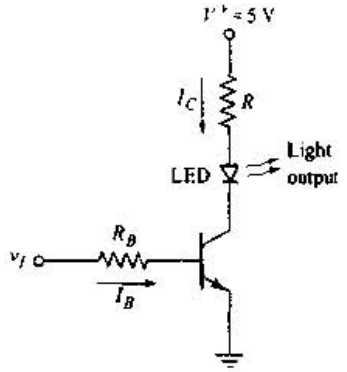


Figure 3.49 Figure for Exercise 3.21

3.22 The transistor parameters in the circuit in Figure 3.43(b) are: $\beta = 40$, $V_{BE}(\text{on}) = 0.7$ V, and $V_{CE}(\text{sat}) = 0.2$ V. Let $R_C = 600\,\Omega$ and $R_B = 950\,\Omega$. Determine the currents and output voltage for: (a) $V_1 = V_2 = 0$; (b) $V_1 = 5$ V, $V_2 = 0$; and (c) $V_1 = V_2 = 5$ V. (Ans. (a) The currents are zero, $V_O = 5$ V; (b) $I_{B2} = I_{C2} = 0$, $I_{B1} = 4.53$ mA, $I_{C1} = I_R = 8$ mA, $V_O = 0.2$ V; (c) $I_{B1} = I_{B2} = 4.53$ mA, $I_{C1} = I_{C2} = 4$ mA $= I_R/2$, $V_O = 0.2$ V)

D3.23 Consider the inverter amplifier shown in Figure 3.45(a). Redesign the circuit such that the voltage amplification is $\Delta v_O/\Delta v_I = -5$. Determine the Q-point values so that the transistor is biased in the center of the active region.

3.4 BIPOLAR TRANSISTOR BIASING

As mentioned in the previous section, in order to create a linear amplifier, we must keep the transistor in the forward-active mode, establish a Q-point near the center of the load line, and couple the time-varying input signal to the base. The circuit in Figure 3.45(a) is impractical for two reasons: (1) the signal source is not connected to ground, and (2) the dc base current flows through the signal source. In this section, we will examine several alternative biasing schemes. These basic biasing circuits illustrate some desirable and some undesirable biasing characteristics. More sophisticated biasing circuits that use additional transistors and that are used in integrated circuits are discussed in Chapter 10.

3.4.1 Single Base Resistor Biasing

The circuit shown in Figure 3.50(a) is one of the simplest transistor circuits. There is a single dc power supply, and the quiescent base current is established through the resistor R_B. The **coupling capacitor** C_C acts as an open circuit to dc, isolating the signal source from the dc base current. If the frequency of the input signal is large enough and C_C is large enough, the signal can be coupled through C_C to the base with little attenuation. Figure 3.50(b) is the dc equivalent circuit; the Q-point values are indicated by the additional subscript Q.

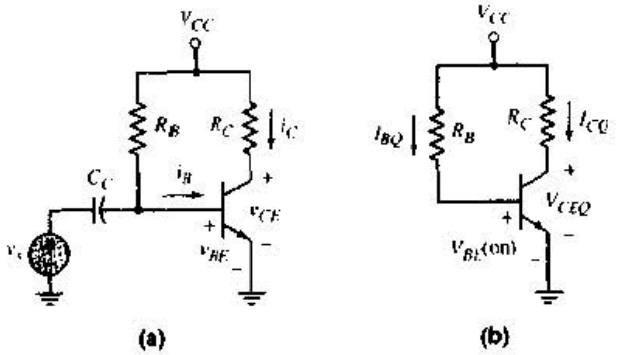


Figure 3.50 (a) Common-emitter circuit with a single bias resistor in the base and (b) dc equivalent circuit

Design Example 3.13 **Objective:** Design the circuit shown in Figure 3.50(b) to yield a given I_{CQ} and V_{CEQ}.

Assume that $V_{CC} = 12\,\text{V}$, $\beta = 100$, and $V_{BE}(\text{on}) = 0.7\,\text{V}$. The Q-point values are to be $I_{CQ} = 1\,\text{mA}$ and $V_{CEQ} = 6\,\text{V}$.

Solution: The collector resistance can be found from

$$R_C = \frac{V_{CC} - V_{CEQ}}{I_{CQ}} = \frac{12 - 6}{1} = 6\,\text{k}\Omega$$

The base current must then be

$$I_{BQ} = \frac{I_{CQ}}{\beta} = \frac{1\,\text{mA}}{100} \Rightarrow 10\,\mu\text{A}$$

and the base resistance is determined to be

$$R_B = \frac{V_{CC} - V_{BE}(\text{on})}{I_{BQ}} = \frac{12 - 0.7}{10\,\mu\text{A}} = 1.13\,\text{M}\Omega$$

Comment: Although a value of 1.13 MΩ for R_B will establish the required base current, this resistance is too large to be used in an integrated circuit.

Figure 3.51(a) shows the transistor characteristics and load line for the circuit in Example 3.13. Although we assumed a current gain of $\beta = 100$, a given transistor type may exhibit a range of values for β as a result of slight variations in the fabrication process. For example, a second circuit with the same configuration as Figure 3.50(a) could be fabricated using a transistor with

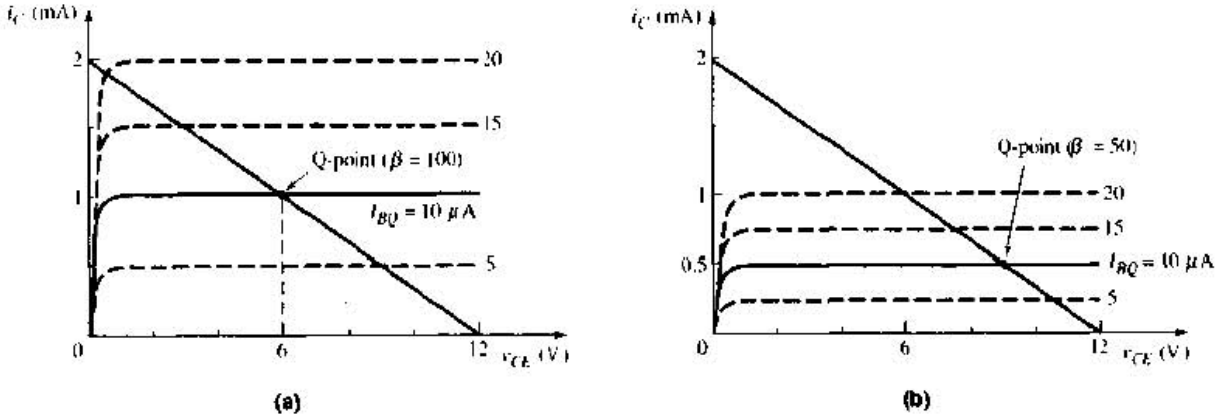


Figure 3.51 Transistor characteristics and load line for the circuit in Example 3.13 when (a) $\beta = 100$ and (b) $\beta = 50$

a current gain of $\beta = 50$. Using the R_C and R_B values previously determined, we would find new quiescent values, as follows:

$$I_{BQ} = \frac{V_{CC} - V_{BE}(\text{on})}{R_B} = 10\,\mu\text{A (unchanged)} \tag{3.33}$$

$$I_{CQ} = \beta I_{BQ} = (50)(10\,\mu\text{A}) \Rightarrow 0.5\,\text{mA} \tag{3.34}$$

and

$$V_{CEQ} = V_{CC} - I_{CQ}R_C = 12 - (0.5)(6) = 9\,\text{V} \tag{3.35}$$

Figure 3.51(b) shows the new transistor characteristics, load line, and Q-point. We can see that the Q-point has shifted substantially. In this circuit, then, the Q-point is not stabilized against variations in β; as β changes, the Q-point varies significantly. We noted in Example 3.12 that the position of the Q-point is significant in a circuit design.

The Q-point is also influenced by variations in resistance values. Tolerances in discrete resistance and integrated circuit resistance values result from process variations and material property variations. For example, if a

discrete resistor has a ±5 percent tolerance, a 6 kΩ resistor may actually have a value between 5.7 and 6.3 kΩ; similarly, a 1.13 MΩ resistor may actually be between 1.07 and 1.19 MΩ.

Assuming $\beta = 100$, as in the last example, a ±5 percent variation in R_B means that the base current may be in the range of 9.5 to 10.6 μA. The collector current would then be in the range of 0.95 to 1.06 mA. The variation in collector current, in conjunction with a ±5 percent tolerance in R_C, means that the C–E voltage may range from 5.32 to 6.59 V. Our design, then, may specify a value of $V_{CE} = 6$ V, but the actual value of V_{CE} may vary considerably.

Test Your Understanding

[Note: In the following exercises, assume the B–E cut-in voltage is 0.7 V for both the npn and pnp transistors. Also assume the C–E saturation voltage is 0.2 V for both types of transistor.]

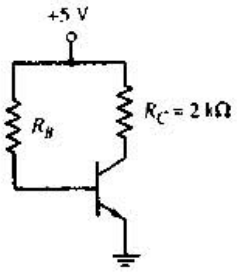


Figure 3.52 Figure for Exercises 3.24 and 3.25

3.24 Consider the circuit shown in Figure 3.52. (a) If $\beta = 100$, determine R_B such that $V_{CEQ} = 2.5$ V. (b) Determine the minimum and maximum allowed values of β if the quiescent collector–emitter voltage is to be in the range $1 \le V_{CEQ} \le 4$ V. (Ans. (a) $R_B = 344$ kΩ; (b) $40 \le \beta \le 160$)

***D3.25** For the circuit shown in Figure 3.52, let $R_B = 800$ kΩ. If the range of β is between 75 and 150, determine a new value of R_C such that the Q-point will always be in the range $1 \le V_{CEQ} \le 4$ V. What will be the actual range of V_{CEQ} for the new value of R_C? (Ans. For $V_{CEQ} = 2.5$ V, $R_C = 4.14$ kΩ; (b) $1.66 \le V_{CEQ} \le 3.33$ V)

3.4.2 Voltage Divider Biasing and Bias Stability

The circuit in Figure 3.53(a) is a classic example of discrete transistor biasing. The single bias resistor R_B in the previous circuit is replaced by a pair of

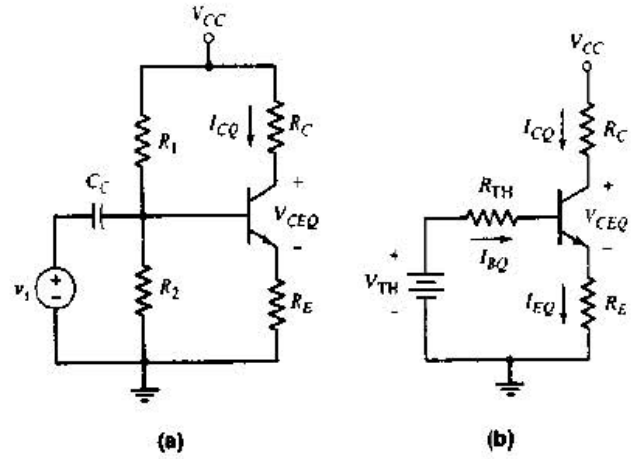


Figure 3.53 (a) A common-emitter circuit with an emitter resistor and voltage divider bias circuit in the base; (b) the dc circuit with a Thevenin equivalent base circuit

resistors R_1 and R_2, and an emitter resistor R_E is added. The ac signal is still coupled to the base of the transistor through the coupling capacitor C_C.

The circuit is most easily analyzed by forming a **Thevenin equivalent circuit** for the base circuit. The coupling capacitor acts as an open circuit to dc. The equivalent Thevenin voltage is

$$V_{TH} = [R_2/(R_1 + R_2)]V_{CC}$$

and the equivalent Thevenin resistance is

$$R_{TH} = R_1 \| R_2$$

where the symbol $\|$ indicates the parallel combination of resistors. Figure 3.53(b) shows the equivalent dc circuit. As we can see, this circuit is similar to those we have previously considered.

Applying Kirchhoff's law around the B–E loop, we obtain

$$V_{TH} = I_{BQ}R_{TH} + V_{BE}(\text{on}) + I_{EQ}R_E \tag{3.36}$$

If the transistor is biased in the forward-active mode, then

$$I_{EQ} = (1 + \beta)I_{BQ}$$

and the base current, from Equation (3.36), is

$$I_{BQ} = \frac{V_{TH} - V_{BE}(\text{on})}{R_{TH} + (1 + \beta)R_E} \tag{3.37}$$

The collector current is then

$$I_{CQ} = \beta I_{BQ} = \frac{\beta(V_{TH} - V_{BE}(\text{on})}{R_{TH} + (1 + \beta)R_E} \tag{3.38}$$

Example 3.14 **Objective:** Analyze a circuit using a voltage divider bias circuit, and determine the change in the Q-point with a variation in β when the circuit contains an emitter resistor.

For the circuit given in Figure 3.53(a), let $R_1 = 56\,\text{k}\Omega$, $R_2 = 12.2\,\text{k}\Omega$, $R_C = 2\,\text{k}\Omega$, $R_E = 0.4\,\text{k}\Omega$, $V_{CC} = 10\,\text{V}$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, and $\beta = 100$.

Solution: Using the Thevenin equivalent circuit in Figure 3.53(b), we have

$$R_{TH} = R_1 \| R_2 = 56 \| 12.2 = 10.0\,\text{k}\Omega$$

and

$$V_{TH} = \left(\frac{R_1}{R_1 + R_2}\right) \cdot V_{CC} = \left(\frac{12.2}{56 + 12.2}\right)(10) = 1.79\,\text{V}$$

Writing the Kirchhoff voltage law equation around the B–E loop, we obtain

$$I_{BQ} = \frac{V_{TH} - V_{BE}(\text{on})}{R_{TH} + (1 + \beta)R_E} = \frac{1.79 - 0.7}{10 + (101)(0.4)} \Rightarrow 21.6\,\mu\text{A}$$

The collector current is

$$I_{CQ} = \beta I_{BQ} = (100)(21.6\,\mu\text{A}) \Rightarrow 2.16\,\text{mA}$$

and the emitter current is

$$I_{EQ} = (1 + \beta)I_{BQ} = (101)(21.6\,\mu\text{A}) \Rightarrow 2.18\,\text{mA}$$

The quiescent C-E voltage is then

$$V_{CEQ} = V_{CC} - I_{CQ}R_C - I_{EQ}R_E = 10 - (2.16)(2) - (2.18)(0.4) = 4.81\,\text{V}$$

These results show that the transistor is biased in the active region.

If the current gain of the transistor were to decrease to $\beta_F = 50$ or increase to $\beta_F = 150$, we obtain the following results:

β_F	$I_{BQ}(\mu\text{A})$	$I_{CQ}(\text{mA})$	$I_{EQ}(\text{mA})$	$V_{CEQ}(\text{V})$
50	35.9	1.80	1.83	5.67
100	21.6	2.16	2.18	4.81
150	15.5	2.32	2.34	4.40

For a 3 : 1 ratio in β_F, the collector current and collector-emitter voltage change by only a 1.29 : 1 ratio.

Comment: The voltage divider circuit of R_1 and R_2 can bias the transistor in its active region using resistor values in the low kilohm range. In contrast, single resistor biasing requires a resistor in the megohm range. In addition, the change in I_{CQ} and V_{CEQ} with a change in β_F has been substantially reduced compared to the change shown in Figure 3.51. Including an emitter resistor R_E has tended to **stabilize** the Q-point. This means that including the emitter resistor helps to stabilize the Q-point with respect to variations in β.

The design requirement for bias stability is $R_{TH} \ll (1 + \beta)R_E$. Consequently, the collector current, from Equation (3.38), becomes approximately

$$I_{CQ} \cong \frac{\beta(V_{TH} - V_{BE}(\text{on}))}{(1 + \beta)R_E} \tag{3.39}$$

Normally, $\beta \gg 1$; therefore, $\beta/(1 + \beta) \cong 1$, and

$$I_{CQ} \cong \frac{(V_{TH} - V_{BE}(\text{on}))}{R_E} \tag{3.40}$$

Now the quiescent collector current is essentially a function of only the dc voltages and the emitter resistance, and the Q-point is stabilized against β variations. However, if R_{TH} is too small, then R_1 and R_2 are small, and excessive power is dissipated in these resistors. The general rule is that a circuit is considered **bias stable** when

$$R_{TH} \cong 0.1(1 + \beta)R_E \tag{3.41}$$

Design Example 3.15 **Objective:** Design a bias-stable circuit.

Consider the circuit shown in Figure 3.53(a). Let $V_{CC} = 5\,\text{V}$, $R_C = 1\,\text{k}\Omega$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, and $\beta = 120$. Choose R_E and determine R_1 and R_2 such that the circuit is bias stable and that $V_{CEQ} = 3\,\text{V}$.

Design Pointer: Typically, the voltage across R_E should be on the same order of magnitude as $V_{BE}(\text{on})$. Larger voltage drops may mean the supply voltage V_{CC} has to be increased in order to get the required voltage across the collector-emitter and across R_C.

Solution: With $\beta = 120$, $I_{CQ} \approx I_{EQ}$. Then, choosing a standard value of 0.51 kΩ for R_E, we find

$$I_{CQ} \cong \frac{V_{CC} - V_{CEQ}}{R_C + R_E} = \frac{5-3}{1+0.51} = 1.32\,\text{mA}$$

The voltage drop across R_E is now (1.32)(0.51) = 0.673 V, which is approximately the desired value. The base current is found to be

$$I_{BQ} = \frac{I_{CQ}}{\beta} = \frac{1.32}{120} \Rightarrow 11.0\,\mu\text{A}$$

Using the Thevenin equivalent circuit in Figure 3.53(b), we find

$$I_{BQ} = \frac{V_{TH} - V_{BE}(\text{on})}{R_{TH} + (1+\beta)R_E}$$

For a bias-stable circuit, $R_{TH} = 0.1(1+\beta)R_E$, or

$$R_{TH} = (0.1)(121)(0.51) = 6.17\,\text{k}\Omega$$

Then,

$$I_{BQ} = 11.0\,\mu\text{A} \Rightarrow \frac{V_{TH} - 0.7}{6.17 + (121)(0.51)}$$

which yields

$$V_{TH} = 0.747 + 0.70 = 1.45\,\text{V}$$

Now

$$V_{TH} = \left(\frac{R_2}{R_1 + R_2}\right)V_{CC} = \left(\frac{R_2}{R_1 + R_2}\right)5 = 1.45\,\text{V}$$

or

$$\left(\frac{R_2}{R_1 + R_2}\right) = \frac{1.45}{5} = 0.288$$

Also,

$$R_{TH} = \frac{R_1 R_2}{R_1 + R_2} = 6.05\,\text{k}\Omega = R_1\left(\frac{R_2}{R_1 + R_2}\right) = R_1(0.288)$$

which yields

$$R_1 = 21\,\text{k}\Omega$$

and

$$R_2 = 8.5\,\text{k}\Omega$$

From Appendix D, we can choose standard resistor values of $R_1 = 20\,\text{k}\Omega$ and $R_2 = 8.2\,\text{k}\Omega$.

Comment: The Q-point in this example is now considered stabilized against variations in β, and the voltage divider resistors R_1 and R_2 have reasonable values in the kilohm range.

Computer Simulation: Figure 3.54 shows the PSpice circuit schematic with the standard resistor values and with a standard 2N2222 transistor from the PSpice library for the circuit designed in this example. A dc analysis was performed and the resulting transister Q-point values are shown. The collector–emitter voltage is $V_{CE} = 2.80\,\text{V}$, which is close to the design value of 3 V. One reason for the difference is that the standard-valued resistors are not exactly equal to the design values. Another reason

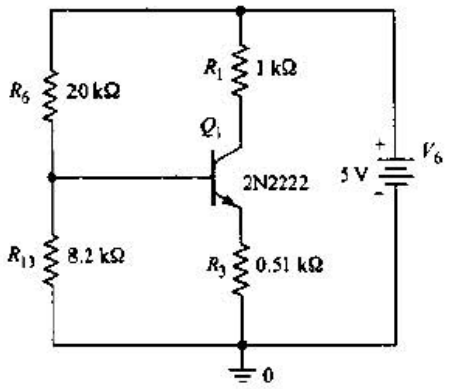


Figure 3.54 PSpice circuit schematic for Example 3.15

for the slight difference is that the effective β_F of the 2N2222 is 157 compared to the assumed value of 120.

```
**** BIPOLAR JUNCTION TRANSISTORS

NAME         Q_Q1
MODEL        Q2N2222
IB           9.25E-06
IC           1.45E-03
VBE          6.55E-01
VBC         -2.15E+00
VCE          2.80E+00
BETADC       1.57E+02
```

Another advantage of including an emitter resistor is that it stabilizes the Q-point with respect to temperature. To explain, we noted in Figure 1.18 that the current in a pn junction increases with increasing temperature, for a constant junction voltage. We then expect the transistor current to increase as the temperature increases. If the current in a junction increases, the junction temperature increases (because of I^2R heating), which in turn causes the current to increase, thereby further increasing the junction temperature. This phenomenon can lead to thermal runaway and to device destruction. However, from Figure 3.53(b), we see that as the current increases, the voltage drop across R_E increases. The Thevenin equivalent voltage and resistance are assumed to be essentially independent of temperature, and the temperature-induced change in the voltage drop across R_{TH} will be small. The net result is that the increased voltage drop across R_E reduces the B–E junction voltage, which then tends to stabilize the transistor current against increases in temperature.

Test Your Understanding

3.26 For the circuit shown in Figure 3.53(a), let $V_{CC} = 5$, $R_1 = 9\,\text{k}\Omega$, $R_2 = 2.25\,\text{k}\Omega$, $R_E = 200\,\Omega$, $R_C = 1\,\text{k}\Omega$, and $\beta = 150$. (a) Determine R_{TH} and V_{TH}. (b) Find I_{BQ}, I_{CQ}, and V_{CEQ}. (c) Repeat part (b) if β changes to $\beta = 75$. (Ans. (a) $R_{TH} = 1.8\,\text{k}\Omega$,

$V_{TH} = 1.0\,V$; (b) $I_{BQ} = 9.38\,\mu A$, $I_{CQ} = 1.41\,mA$, $V_{CEQ} = 3.31\,V$; (c) $I_{BQ} = 17.6\,\mu A$, $I_{CQ} = 1.32\,mA$, $V_{CEQ} = 3.41\,V$)

***3.27** In the circuit shown in Figure 3.53(a), let $V_{CC} = 5\,V$, $R_E = 0.2\,k\Omega$, $R_C = 1\,k\Omega$, and $\beta = 150$. If $R_1 + R_2 = 11.25\,k\Omega$, determine R_1 and R_2 such that the Q-point is in the center of the load line. (Ans. $R_1 = 8.67\,k\Omega$, $R_2 = 2.58\,k\Omega$)

D3.28 Consider the circuit shown in Figure 3.55. Let $\beta = 150$, $R_E = 0.2\,k\Omega$, and $R_C = 1\,k\Omega$. Design a dc bias-stable circuit such that the quiescent output voltage is zero. (Ans. $R_1 = 16.7\,k\Omega$, $R_2 = 3.68\,k\Omega$)

D3.29 In the circuit shown in Figure 3.55, assume $\beta = 120$, $R_C = 1.2\,k\Omega$, and $R_E = 0.3\,k\Omega$. Design a bias-stable circuit such that $V_{CEQ} = 5\,V$. (Ans. $R_1 = 20.1\,k\Omega$, $R_2 = 4.44\,k\Omega$)

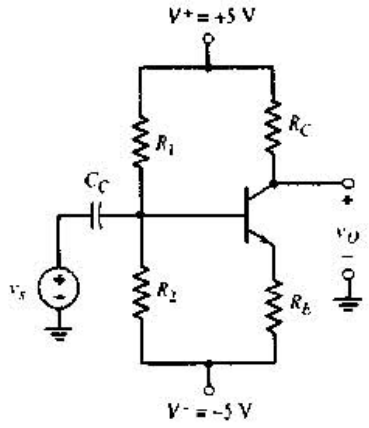


Figure 3.55 Figure for Exercises 3.28 and 3.29

3.4.3 Integrated Circuit Biasing

The resistor biasing of transistor circuits considered up to this point is primarily applied to discrete circuits. For integrated circuits, we would like to eliminate as many resistors as possible since, in general, they require a larger surface area than transistors.

A bipolar transistor can be biased by using a constant-current source I_Q, as shown in Figure 3.56. The advantages of this circuit are that the emitter current is independent of β and R_B, and the collector current and C–E voltage are essentially independent of transistor current gain, for reasonable values of β. The value of R_B can be increased, thus increasing the input resistance at the base, without jeopardizing the bias stability.

The constant-current source can be implemented by using transistors, as shown in Figure 3.57. Transistors Q_1 and Q_2 and resistor R_1 form the constant-current source. Even though transistor Q_1 is connected as a diode, it operates as a transistor in the active region.

Current I_1 is called the **reference current** and is found by writing Kirchhoff's voltage law equation around the R_1–Q_1 loop, as follows:

$$0 = I_1 R_1 + V_{BE}(\text{on}) + V^- \qquad (3.42(a))$$

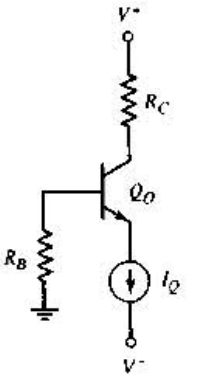


Figure 3.56 Bipolar transistor biased with a constant-current source

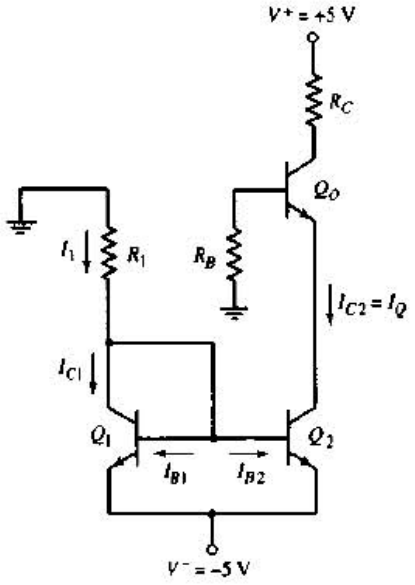


Figure 3.57 Constant-current source biasing

which yields

$$I_1 = \frac{-(V^- + V_{BE}(\text{on}))}{R_1} \tag{3.42(b)}$$

Summing the currents at the collector of Q_1 gives

$$I_1 = I_{C1} + I_{B1} + I_{B2} \tag{3.43}$$

Since the B–E voltages of Q_1 and Q_2 are equal, if Q_1 and Q_2 are identical transistors and are held at the same temperature, then $I_{B1} = I_{B2}$ and $I_{C1} = I_{C2}$. Equation (3.43) can then be written as

$$I_1 = I_{C1} + 2I_{B2} = I_{C2} + \frac{2I_{C2}}{\beta} = I_{C2}\left(1 + \frac{2}{\beta}\right) \tag{3.44}$$

Solving for I_{C2}, we find

$$I_{C2} = I_Q = \frac{I_1}{\left(1 + \frac{2}{\beta}\right)} \tag{3.45}$$

This current biases the transistor Q_O in the active region.

Example 3.16 **Objective:** Determine the currents in a two-transistor current source.

For the circuit in Figure 3.57, the circuit and transistor parameters are: $R_1 = 10\,\text{k}\Omega$, $\beta = 50$, and $V_{BE}(\text{on}) = 0.7\,\text{V}$.

Solution: The reference current is

$$I_1 = \frac{-(V^- + V_{BE}(\text{on}))}{R_1} = \frac{-((-5) + 0.7)}{10} = 0.43\,\text{mA}$$

From Equation (3.45), the bias current I_Q is

$$I_{C2} = I_Q = \frac{I_1}{\left(1+\frac{2}{\beta}\right)} = \frac{0.43}{\left(1+\frac{2}{50}\right)} = 0.413\,\text{mA}$$

The base currents are then

$$I_{B1} = I_{B2} = \frac{I_{C2}}{\beta} = \frac{0.413}{50} \Rightarrow 8.26\,\mu\text{A}$$

Comment: For relatively large values of current gain β, the bias current I_Q is essentially the same as the reference current I_1.

As mentioned, constant-current biasing is used almost exclusively in integrated circuits. As we will see in Part II of the text, circuits in integrated circuits use a minimum number of resistors, and transistors are often used to replace these resistors. Transistors take up much less area than resistors on an IC chip, so it's advantageous to minimize the number of resistors.

Test Your Understanding

***3.30** (a) For the circuit in Figure 3.56, the parameters are: $I_Q = 1\,\text{mA}$, $V^+ = 10\,\text{V}$, $V^- = -10\,\text{V}$, $R_B = 50\,\text{k}\Omega$, and $R_C = 5\,\text{k}\Omega$. For the transistor, $\beta = 100$, and $I_S = 3 \times 10^{-14}\,\text{A}$. Determine the dc voltage at the base and V_{CEQ}. (b) Repeat part (a) if $\beta = 50$. (Ans. (a) $V_B = -0.495\,\text{V}$, $V_{CEQ} = 6.18\,\text{V}$; (b) $V_B = -0.98\,\text{V}$, $V_{CEQ} = 6.71\,\text{V}$)

3.31 The circuit shown in Figure 3.58 is biased with a constant-current source I_Q. For the transistor, $\beta = 120$, and the E–B turn-on voltage is $V_{EB}(\text{on}) = 0.7\,\text{V}$. Determine I_Q such that $V_{ECQ} = 3\,\text{V}$. (Ans. $I_Q = 0.710\,\text{mA}$)

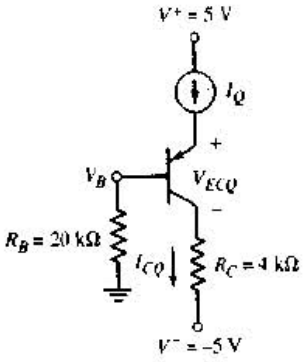


Figure 3.58 Figure for Exercise 3.31

3.5 MULTISTAGE CIRCUITS

Most transistor circuits contain more than one transistor. We can analyze and design these **multistage circuits** in much the same way as we studied single-transistor circuits. As an example, Figure 3.59 shows an npn transistor, Q_1, and a pnp bipolar transistor, Q_2, in the same circuit.

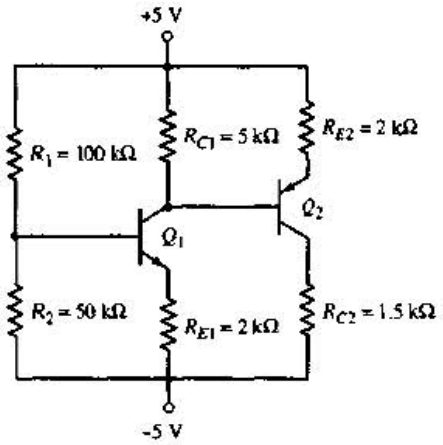


Figure 3.59 A multistage transistor circuit

Example 3.17 **Objective:** Calculate the dc voltages at each node and the dc currents through the elements in a multistage circuit.

For the circuit in Figure 3.59, assume the B–E turn-on voltage is 0.7 V and $\beta = 100$ for each transistor.

Solution: The Thevenin equivalent circuit of the base circuit of Q_1 is shown in Figure 3.60. The various currents and nodal voltages are defined as shown. The Thevenin resistance and voltage are

$$R_{TH} = R_1 \| R_2 = 100 \| 50 = 33.3\,\text{k}\Omega$$

and

$$V_{TH} = \left(\frac{R_2}{R_1 + R_2}\right)(10) - 5 = \left(\frac{50}{150}\right)(10) - 5 = -1.67\,\text{V}$$

Kirchhoff's voltage law equation around the B–E loop of Q_1 is

$$V_{TH} = I_{B1}R_{TH} + V_{BE}(\text{on}) + I_{E1}R_{E1} - 5$$

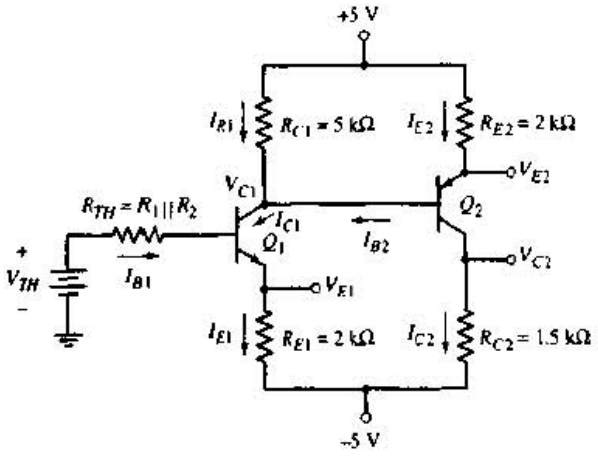


Figure 3.60 Multistage transistor circuit with a Thevenin equivalent circuit in the base of Q_1

Noting that $I_{E1} = (1 + \beta)I_{B1}$, we have

$$I_{B1} = \frac{-1.67 + 5 - 0.7}{33.3 + (101)(2)} \Rightarrow 11.2\,\mu A$$

Therefore,

$$I_{C1} = 1.12\,mA$$

and

$$I_{E1} = 1.13\,mA$$

Summing the currents at the collector of Q_1, we obtain

$$I_{R1} + I_{B2} = I_{C1}$$

which can be written as

$$\frac{5 - V_{C1}}{R_{C1}} + I_{B2} = I_{C1} \tag{3.46}$$

Then, the base current I_{B2} can be written in terms of the emitter current I_{E2}, as follows:

$$I_{B2} = \frac{I_{E2}}{1 + \beta} = \frac{5 - V_{E2}}{(1 + \beta)R_{E2}} = \frac{5 - (V_{C1} + 0.7)}{(1 + \beta)R_{E2}} \tag{3.47}$$

Substituting Equation (3.47) into (3.46), we obtain

$$\frac{5 - V_{C1}}{R_{C1}} + \frac{5 - (V_{C1} + 0.7)}{(1 + \beta)R_{E2}} = I_{C1} = 1.12\,mA$$

which can be solved for V_{C1} to yield

$$V_{C1} = -0.482\,V$$

Then,

$$I_{R1} = \frac{5 - (-0.482)}{5} = 1.10\,mA$$

To find V_{E2}, we have

$$V_{E2} = V_{C1} + V_{EB}(on) = -0.482 + 0.7 = 0.218\,V$$

The emitter current I_{E2} is

$$I_{E2} = \frac{5 - 0.218}{2} = 2.39\,mA$$

Then,

$$I_{C2} = \left(\frac{\beta}{1 + \beta}\right)I_{E2} = \left(\frac{100}{101}\right)(2.39) = 2.37\,mA$$

and

$$I_{B2} = \frac{I_{E2}}{1 + \beta} = \frac{2.39}{101} \Rightarrow 23.7\,\mu A$$

The remaining nodal voltages are

$$V_{E1} = I_{E1}R_{E1} - 5 = (1.13)(2) - 5 \Rightarrow V_{E1} = -2.74\,V$$

and

$$V_{C2} = I_{C1}R_{C2} - 5 = (2.37)(1.5) - 5 \Rightarrow V_{C2} = -1.45\,V$$

We then find that

$$V_{CE1} = -0.482 - (-2.74) = 2.26\,V$$

and that

$$V_{EC2} = 0.218 - (-1.45) = 1.67\,\text{V}$$

Comment: These results show that both Q_1 and Q_2 are biased in the forward-active mode, as originally assumed. However, when we consider the ac operation of this circuit as an amplifier in the next chapter, we will see that a better design would increase the value of V_{EC2}.

Test Your Understanding

[Note: In the following exercises, assume the B–E cut-in voltage is 0.7 V and that $\beta = 100$ for both the npn and pnp transistors.]

***RD3.32** In the circuit shown in Figure 3.59, determine new values of R_{C1} and R_{C2} such that $V_{CEQ1} = 3.25\,\text{V}$ and $V_{ECQ2} = 2.5\,\text{V}$. (Ans. $R_{C1} = 4.08\,\text{k}\Omega$, $R_{C2} = 1.97\,\text{k}\Omega$)

***3.33** For the circuit shown in Figure 3.59, change the +5 V bias to +12 V and the −5 V bias to ground potential. Determine all new currents and node voltages. (Ans. $I_{B1} = 14.0\,\mu\text{A}$, $I_{C1} = 1.40\,\text{mA}$, $I_{E1} = 1.42\,\text{mA}$, $V_{B1} = 3.53\,\text{V}$, $V_{E1} = 2.83\,\text{V}$, $V_{C1} = V_{B2} = 5.15\,\text{V}$, $V_{E2} = 5.85\,\text{V}$, $I_{E2} = 3.08\,\text{mA}$, $I_{C2} = 3.04\,\text{mA}$, $I_{B2} = 30.4\,\mu\text{A}$, $V_{C2} = 4.56\,\text{V}$)

3.6 SUMMARY

- In this chapter, we considered the basic characteristics and properties of the bipolar transistor, which is a three-terminal device that has three separately doped semiconductor regions and two pn junctions. The three terminals are called the base (B), emitter (E), and collector (C). Both npn and pnp complementary bipolar transistors can be formed. The defining transistor action is that the voltage across two terminals (base and emitter) controls the current in the third terminal (collector).
- The modes of operation of a bipolar transistor are determined by the biases applied to the two junctions. The four modes are: forward active, cutoff, saturation, and inverse active. In the forward-active mode, the B–E junction is forward biased and the B–C junction is reverse biased, and the collector and base currents are related by the common-emitter current gain β. The relationship is the same for both npn and pnp transistors, as long as the conventional current directions are maintained. When a transistor is cut off, all currents are zero. In the saturation mode, the collector current is no longer a function of base current.
- The dc analysis and the design of dc biasing of bipolar transistor circuits were emphasized in this chapter. We continued to use the piecewise linear model of the pn junction in these analyses and designs. Techniques to design a transistor circuit with a stable Q-point were developed.
- Basic applications of the transistor were discussed. These include switching currents and voltages, performing digital logic functions, and amplifying time-varying signals. The amplifying characteristics will be considered in detail in the next chapter.

CHECKPOINT

After studying this chapter, the reader should have the ability to:

- ✔ Understand and describe the general current–voltage characteristics for both the npn and pnp bipolar transistors. (Section 3.1)
- ✔ Define the four modes of operation of a bipolar transistor. (Section 3.1)
- ✔ Apply the piecewise linear model to the dc analysis and design of various bipolar transistor circuits, including the understanding of the load line. (Section 3.2)
- ✔ Qualitatively understand how a transistor circuit can be used to switch currents and voltages, to perform digital logic functions, and to amplify time-varying signals. (Section 3.3)
- ✔ Design the dc biasing of a transistor circuit to achieve specified dc currents and voltages, and to stabilize the Q-point against transistor parameter variations. (Section 3.4)
- ✔ Apply the dc analysis and design techniques to multistage transistor circuits. (Section 3.5)

REVIEW QUESTIONS

1. What are the bias voltages that need to be applied to an npn bipolar transistor such that the transistor is biased in the forward-active mode?
2. Define the conditions for cutoff, forward-active mode, and saturation mode for a pnp bipolar transistor.
3. Define common-base current gain and common-emitter current gain.
4. Describe the current components that contribute to the collector current and to the base current.
5. Define Early voltage and collector output resistance.
6. Describe a simple common-emitter circuit with an npn bipolar transistor and discuss the relation between collector–emitter voltage and input base current.
7. Define Q-point.
8. Describe the parameters that define a load line.
9. What are the steps used to analyze the dc response of a bipolar transistor circuit?
10. Describe how an npn transistor can be used to switch an LED diode on and off.
11. Describe a bipolar transistor NOR logic circuit.
12. Describe how a transistor can be used to amplify a time-varying voltage.
13. Discuss the advantages of using resistor voltage divider biasing compared to a single base resistor.
14. How can the Q-point be stabilized against variations in transistor parameters?
15. What is the principal difference between biasing techniques used in discrete transistor circuits and integrated circuits?

PROBLEMS

[Note: In the following problems, let $V_{BE}(\text{on}) = 0.7\,\text{V}$ and $V_{CE}(\text{sat}) = 0.2\,\text{V}$ for npn transistors, and let $V_{EB}(\text{on}) = 0.7\,\text{V}$ and $V_{EC}(\text{sat}) = 0.2\,\text{V}$ for pnp transistors.]

Section 3.1 Basic Bipolar Junction Transistor

3.1 (a) In a bipolar transistor biased in the forward-active mode, the base current is $i_B = 6.0\,\mu A$ and the collector current is $i_C = 510\,\mu A$. Determine β_F, α_F, and i_E. (b) Repeat part (a) if $i_B = 50\,\mu A$ and $i_C = 2.65\,mA$.

3.2 (a) The range of β for a particular type of transistor is $110 \leq \beta \leq 180$. Determine the corresponding range of α. (b) If the base current is $50\,\mu A$, determine the range of collector current.

3.3 An npn transistor with $\alpha = 0.982$ is connected in a common-base configuration. The collector is connected to ground through a 5 V source and a $2\,k\Omega$ resistor. The emitter is driven with a constant-current source. Determine the maximum emitter current such that $V_{CE} \geq 1.0\,V$.

3.4 An npn bipolar transistor with $\beta_F = 120$ is connected in the same circuit configuration described in Problem 3.3. The collector-emitter voltage is $v_{CE} = 2\,V$. Determine i_C, i_B, and i_E.

3.5 A pnp transistor with $\beta = 60$ is connected in a common-base configuration and is biased in the forward-active mode. The collector current is $I_C = 0.85\,mA$. Determine α, I_E, and I_B.

3.6 An npn transistor has a reverse-saturation current of $I_S = 10^{-13}\,A$ and a current gain of $\beta_F = 90$. The transistor is biased at $v_{BE} = 0.685\,V$. Determine I_E, I_C, and I_B.

3.7 Two pnp transistors, fabricated with the same technology, have different junction areas. Both transistors are biased with an emitter-base voltage of $v_{EB} = 0.650\,V$ and have emitter currents of 0.50 and 12.2 mA. Find I_S for each device. What are the relative junction areas?

3.8 A BJT has an Early voltage of 250 V. What is the output resistance for (a) $I_C = 1\,mA$ and (b) $I_C = 0.10\,mA$.

3.9 The open-emitter breakdown voltage of a B–C junction is $BV_{CBO} = 60\,V$. If $\beta = 100$ and the empirical constant is $n = 3$, determine the C–E breakdown voltage in the open-base configuration.

3.10 In a particular circuit application, the minimum required breakdown voltages are $BV_{CBO} = 220\,V$ and $BV_{CEO} = 56\,V$. If $n = 3$, determine the maximum allowed value of β.

3.11 A particular transistor circuit design requires a minimum open-base breakdown voltage of $BV_{CEO} = 50\,V$. If $\beta = 50$ and $n = 3$, determine the minimum required value of BV_{CBO}.

Section 3.2 DC Analysis of Transistor Circuits

3.12 For all the transistors in Figure P3.12, $\beta = 75$. The results of some measurements are indicated on the figures. Find the values of the other labeled currents and voltages.

3.13 The collector resistor values in the circuits shown in Figures P3.12(c) and (d) may vary by ±5 percent from the given value. Determine the range of calculated parameters.

RD3.14 For the circuit shown in Figure 3.20(a), $V_{BB} = 2.5\,V$, $V_{CC} = 5\,V$, and $\beta_F = 70$. Redesign the circuit such that $I_{BQ} = 15\,\mu A$ and $V_{ECQ} = 2.5\,V$.

3.15 In the circuits shown in Figure P3.15, the values of measured parameters are shown. Determine β, α, and the other labeled currents and voltages. Sketch the dc load line and plot the Q-point.

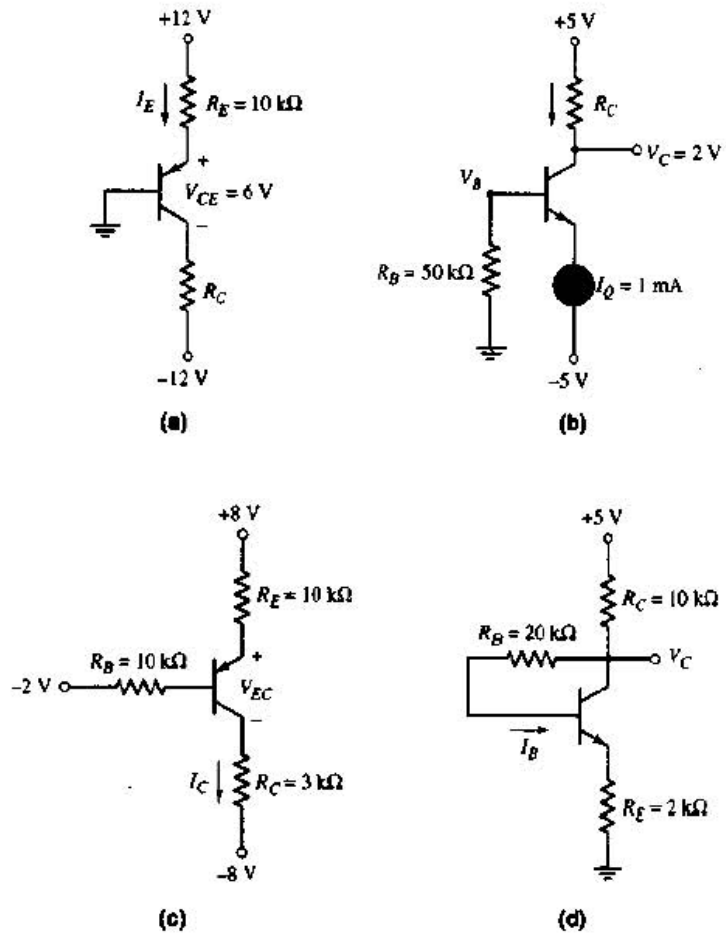


Figure P3.12

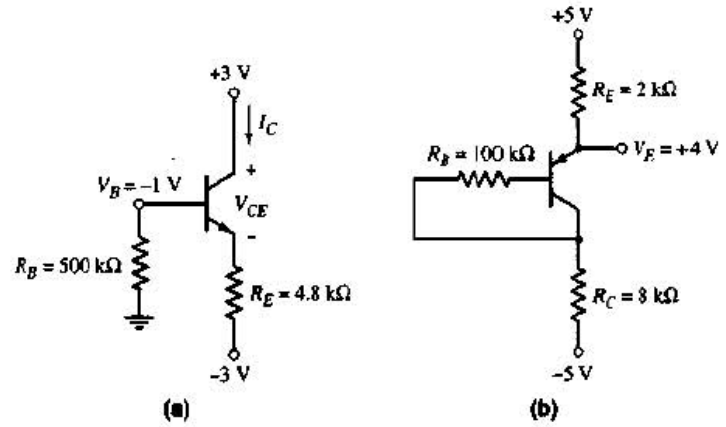


Figure P3.15

3.16 For the transistor in the circuit shown in Figure P3.16, $\beta = 200$. Determine I_E and V_C for: (a) $V_B = 0$, (b) $V_B = 1$ V, and (c) $V_B = 2$ V.

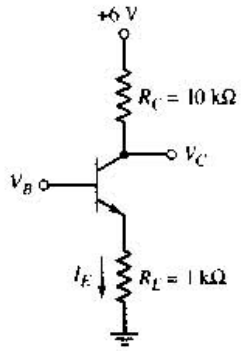


Figure P3.16

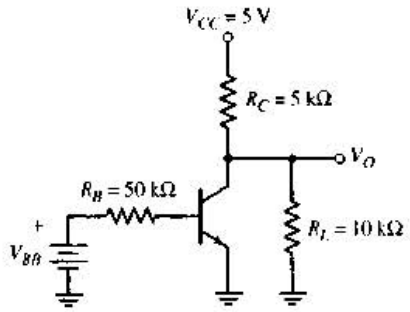


Figure P3.17

3.17 (a) The current gain of the transistor in Figure P3.17 is $\beta = 75$. Determine V_O for: (i) $V_{BB} = 0$, (ii) $V_{BB} = 1$ V, and (iii) $V_{BB} = 2$ V. (b) Verify the results of part (a) with a computer simulation.

3.18 (a) The transistor shown in Figure P3.18 has $\beta_F = 100$. Determine V_O for (i) $I_Q = 0.1$ mA, (ii) $I_Q = 0.5$ mA, and (iii) $I_Q = 2$ mA. (b) Determine the percent change in V_O for the conditions in part (a) if the current gain increases to $\beta_F = 150$.

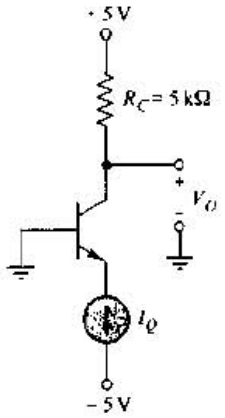


Figure P3.18

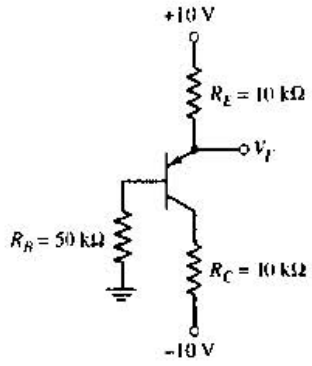


Figure P3.21

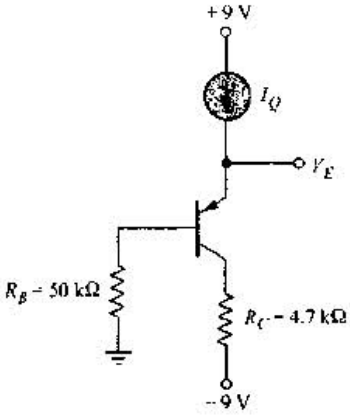


Figure P3.22

3.19 For the circuit in Figure P3.16, determine V_B and I_E such that $V_B = V_C$. Assume $\beta = 50$.

3.20 For the circuit shown in Figure P3.18, determine the value of I_Q such that $V_{CB} = 0.5$ V. Assume $\beta_F = 100$.

3.21 Consider the circuit shown in Figure P3.21. The measured value of the emitter voltage is $V_E = 2$ V. Determine I_E, I_C, β, α, and V_{EC}. Sketch the dc load line and plot the Q-point.

3.22 The transistor in the circuit shown in Figure P3.22 is biased with a constant current in the emitter. If $I_Q = 1$ mA, determine V_C and V_E. Assume $\beta = 50$.

3.23 In the circuit in Figure P3.22, the constant current is $I = 0.5\,\text{mA}$. If $\beta = 50$, determine the power dissipated in the transistor and the power supplied by the constant-current source.

3.24 (a) For the circuit shown in Figure P3.22, calculate and plot the power dissipated in the transistor for $I_Q = 0$, 0.5, 1.0, 1.5, 2.0, 2.5, and 3.0 mA. Assume $\beta_F = 50$. (b) Verify the results of part (a) with a computer simulation.

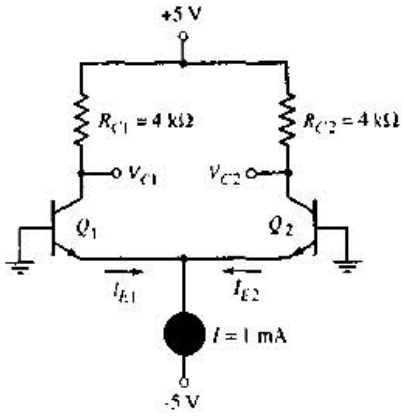


Figure P3.25

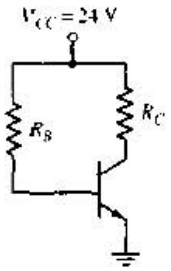


Figure P3.26

3.25 For the circuit shown in Figure P3.25, if $\beta = 200$ for each transistor, determine: (a) I_{E1}, (b) I_{E2}, (c) V_{C1}, and (d) V_{C2}.

D3.26 (a) For the circuit shown in Figure P3.26, the Q-point is $I_{CQ} = 2\,\text{mA}$ and $V_{CEQ} = 12\,\text{V}$ when $\beta = 60$. Determine the values of R_C and R_B. (b) If the transistor is replaced by a new one with $\beta = 100$, find the new values of I_{CQ} and V_{CEQ}. (c) Sketch the load line and Q-point for both parts (a) and (b).

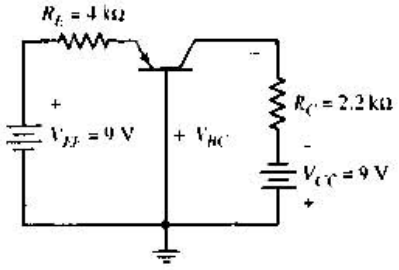


Figure P3.27

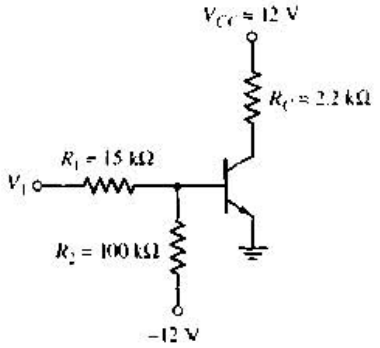


Figure P3.28

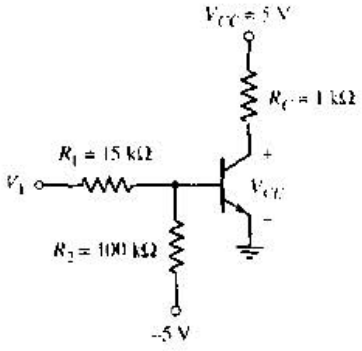


Figure P3.29

3.27 Consider the common-base circuit shown in Figure P3.27. Assume the transistor alpha is $\alpha = 0.9920$. Determine I_E, I_C, and V_{BC}.

3.28 For the transistor in Figure P3.28, $\beta = 30$. Determine V_1 such that $V_{CEQ} = 6\,\text{V}$.

3.29 Let $\beta = 25$ for the transistor in the circuit shown in Figure P3.29. Determine the range of V_1 such that $1.0 \le V_{CE} \le 4.5\,\text{V}$. Sketch the load line and show the range of the Q-point values.

Section 3.4 Bipolar Transistor Biasing

3.30 For the transistor in the circuit shown in Figure P3.30, $\beta = 50$. Determine I_{CQ} and V_{CEQ}.

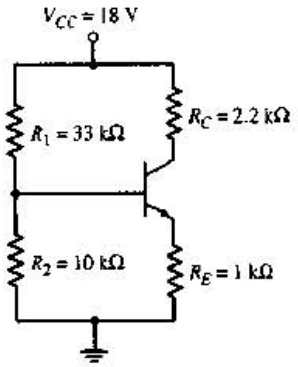


Figure P3.30

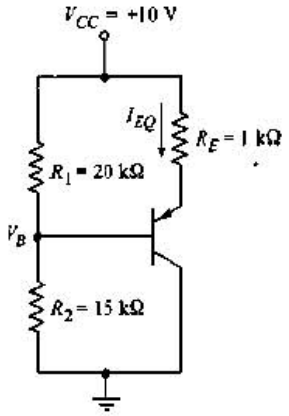


Figure P3.32

***RD3.31** For the circuit shown in Figure P3.30, let $V_{CC} = 18\,\text{V}$, $R_E = 1\,\text{k}\Omega$, and $\beta_F = 80$. Redesign the circuit such that $I_{CQ} = 1.2\,\text{mA}$ and $V_{CEQ} = 9\,\text{V}$. Let $R_{TH} = 50\,\text{k}\Omega$. Correlate the design with a computer simulation.

3.32 The current gain of the transistor shown in the circuit of Figure P3.32 is $\beta = 100$. Determine V_B and I_{EQ}.

3.33 For the circuit shown in Figure P3.33, let $\beta = 125$. (a) Find I_{CQ} and V_{CEQ}. (b) If each resistor can vary by ±5 percent, determine the range in I_{CQ} and V_{CEQ}.

3.34 Consider the circuit shown in Figure P3.34. Determine I_{BQ}, I_{CQ}, and V_{CEQ} for: (a) $\beta = 75$, and (b) $\beta = 150$.

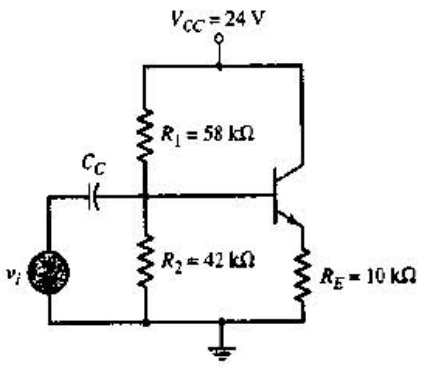


Figure P3.33

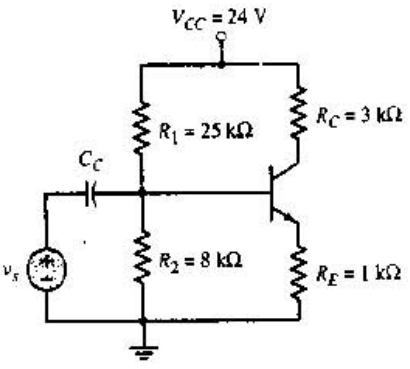


Figure P3.34

RD3.35 (a) Redesign the circuit shown in Figure P3.30 using $V_{CC} = 9\,\text{V}$ such that the voltage drop across R_C is $(\frac{1}{3})V_{CC}$ and the voltage drop across R_E is $(\frac{1}{3})V_{CC}$. Assume $\beta_F = 100$. The quiescent collector current is to be $I_{CQ} = 0.4\,\text{mA}$, and the current through R_1 and R_2 should be approximately $0.2I_{CQ}$. (b) Replace each resistor in part (a) with the closest standard value (Appendix D). What is the value of I_{CQ} and what are the voltage drops across R_C and R_E? (c) Verify the design with a computer simulation.

3.36 For the circuit shown in Figure P3.36, let $\beta = 100$. (a) Find R_{TH} and V_{TH} for the base circuit. (b) Determine I_{CQ} and V_{CEQ}. (c) Draw the load line for the circuit. (d) If each resistor can vary by ±5 percent, determine the range in I_{CQ} and V_{CEQ}.

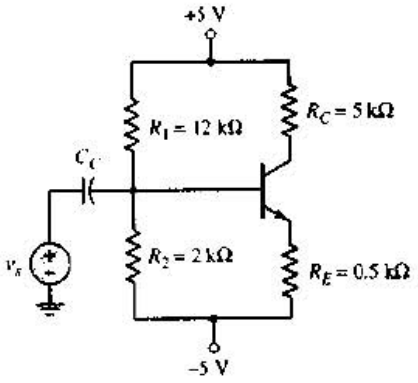


Figure P3.36

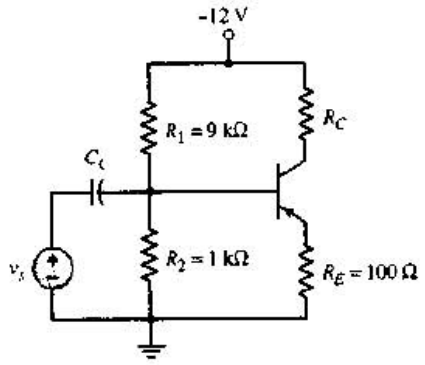


Figure P3.37

D3.37 In the circuit shown in Figure P3.37, find R_C such that the Q-point is in the center of the load line. Let $\beta = 75$. What are the values of I_{CQ} and V_{ECQ}?

D3.38 (a) For the circuit shown in Figure P3.38, design a bias-stable circuit such that $I_{CQ} = 0.8$ mA and $V_{CEQ} = 5$ V. Let $\beta_F = 100$. (b) Using the results of part (a), determine the percentage change in I_{CQ} if β_F is in the range $75 \le \beta_F \le 150$. (c) Repeat parts (a) and (b) if $R_E = 1$ kΩ.

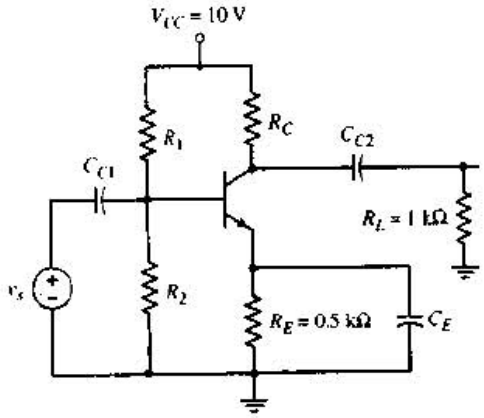


Figure P3.38

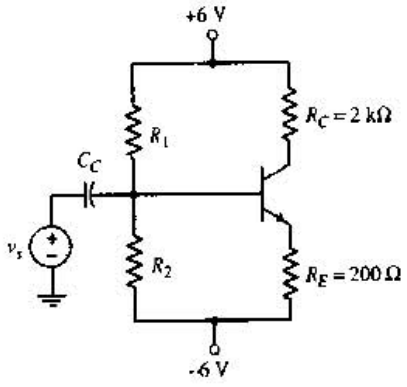


Figure P3.40

***D3.39** Design a bias-stable circuit in the form of Figure P3.38 with $\beta = 120$ such that $I_{CQ} = 0.8$ mA, $V_{CEQ} = 5$ V, and the voltage across R_E is approximately 0.7 V. The current through the bias resistors R_1 and R_2 should be no larger than 0.1 mA.

D3.40 Using the circuit in Figure P3.40, design a bias-stable amplifier such that the Q-point is in the center of the load line. Let $\beta = 125$. Determine I_{CQ}, V_{CEQ}, R_1, and R_2.

D3.41 For the circuit shown in Figure P3.40, the quiescent collector current is to be $I_{CQ} = 1$ mA. (a) Design a bias-stable circuit for $\beta = 80$. Determine V_{CEQ}, R_1, and R_2. (b) If each resistor can vary by ±5 percent, determine the range in I_{CQ} and V_{CEQ}.

***D3.42** A bias-stable circuit with the configuration shown in Figure P3.40 is to be designed such that $I_{CQ} = (3 \pm 0.1)$mA and $V_{CEQ} \cong 5$ V using a transistor with $75 \leq \beta \leq 150$. Verify the design with a computer simulation.

3.43 (a) For the circuit shown in Figure P3.43, assume $\beta = 75$. Determine I_{BQ}, I_{CQ}, and V_{ECQ}. (b) Determine the values of I_{BQ}, I_{CQ}, and V_{ECQ} if $\beta = 100$.

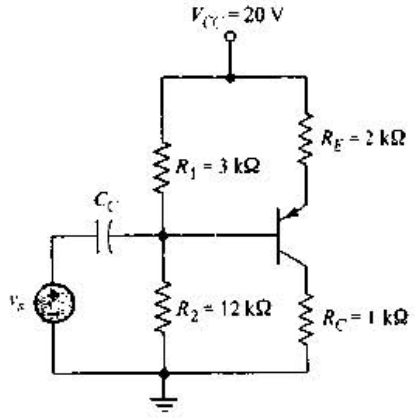


Figure P3.43

D3.44 The dc load line and Q-point of the circuit in Figure P3.44(a) are shown in Figure P3.44(b). For the transistor, $\beta = 120$. Find R_E, R_1, and R_2 such that the circuit is bias stable.

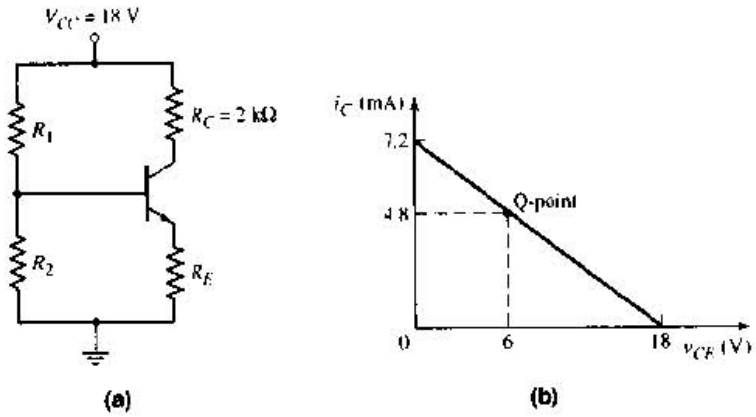


Figure P3.44

***D3.45** The range of β for the transistor in the circuit in Figure P3.45 is $50 \leq \beta \leq 90$. Design a bias-stable circuit such that the nominal Q-point is $I_{CQ} = 2$mA and $V_{CEQ} = 10$ V. The value of I_C must fall in the range $1.75 \leq I_C \leq 2.25$ mA.

***D3.46** The nominal Q-point of the circuit in Figure P3.46 is $I_{CQ} = 1$mA and $V_{CEQ} = 5$V, for $\beta = 60$. The current gain of the transistor is in the range $45 \leq \beta \leq 75$. Design a bias-stable circuit such that I_{CQ} does not vary by more than 10 percent from its nominal value.

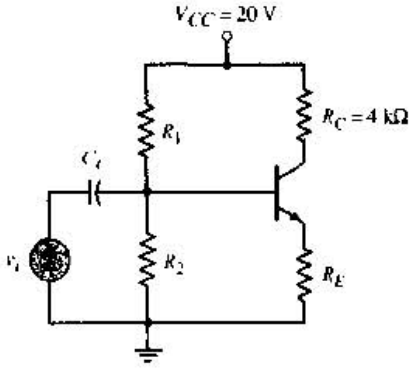


Figure P3.45

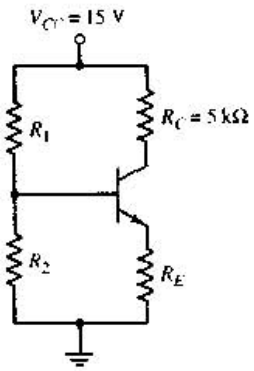


Figure P3.46

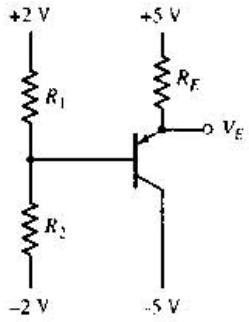


Figure P3.48

RD3.47 (a) For the circuit in Figure P3.46, the value of V_{CC} is changed to 3 V. Let $R_C = 5R_E$ and $\beta_F = 120$. Redesign a bias-stable circuit such that $I_{CQ} = 100\,\mu$A and $V_{CEQ} = 1.4$ V. (b) Using the results of part (a), determine the dc power dissipation in the circuit. (c) Verify the design with a computer simulation.

D3.48 For the circuit in Figure P3.48, let $\beta = 100$ and $R_E = 3\,\text{k}\Omega$. Design a bias-stable circuit such that $V_E = 0$.

3.49 For the circuit in Figure P3.49, let $R_C = 2.2\,\text{k}\Omega$, $R_E = 2\,\text{k}\Omega$, $R_1 = 10\,\text{k}\Omega$, $R_2 = 20\,\text{k}\Omega$, and $\beta = 60$. (a) Find R_{TH} and V_{TH} for the base circuit. (b) Determine I_{BQ}, I_{CQ}, V_E, and V_C.

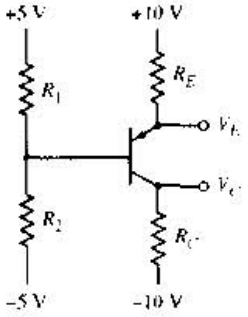


Figure P3.49

***D3.50** Design the circuit in Figure P3.49 to be bias stable and to provide nominal Q-point values of $I_{CQ} = 0.5\,\text{mA}$ and $V_{ECQ} = 8$ V. The maximum current in R_1 and R_2 is to be limited to $40\,\mu$A.

3.51 In the circuit in Figure P3.51, $\beta = 75$. (a) Find V_{TH} and R_{TH} for the base circuit. (b) Determine I_{CQ} and V_{CEQ}. (c) If each resistor can vary by ±5 percent, determine the range in I_{CQ} and V_{CEQ}.

3.52 For the circuit in Figure P3.52, let $\beta = 100$. (a) Find V_{TH} and R_{TH} for the base circuit. (b) Determine I_{CQ} and V_{CEQ}.

3.53 Find I_{CQ} and V_{CEQ} for the circuit in Figure P3.53, if $\beta = 100$.

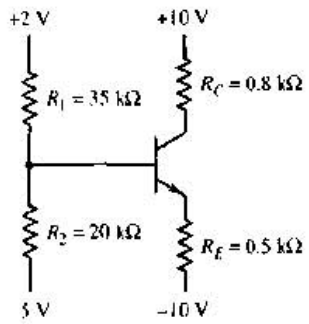


Figure P3.51

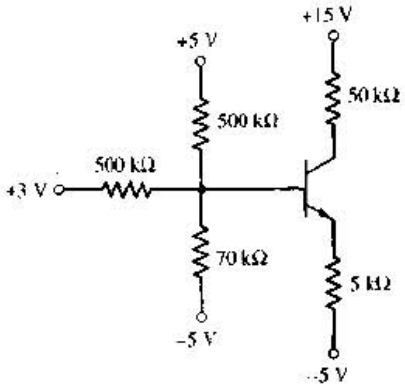


Figure P3.52

Section 3.5 Multistage Circuits

***3.54** For each transistor in the circuit in Figure P3.54, $\beta = 120$ and the B–E turn-on voltage is 0.7 V. Determine the quiescent base, collector, and emitter currents in Q_1 and Q_2. Also determine V_{CEQ1} and V_{CEQ2}.

***3.55** The parameters for each transistor in the circuit in Figure P3.55 are $\beta = 80$ and $V_{BE}(\text{on}) = 0.7\,\text{V}$. Determine the quiescent values of base, collector, and emitter currents in Q_1 and Q_2.

3.56 Consider the circuit used in Example 3.16. Determine the power supplied by the +5 V source and by the −5 V source.

***3.57** (a) For the transistors in the circuit shown in Figure P3.57, the parameters are: $\beta = 100$ and $V_{BE}(\text{on}) = 0.7\,\text{V}$. Determine R_{C1}, R_{E1}, R_{C2}, and R_{E2} such that $I_{C1} = I_{C2} = 0.8\,\text{mA}$, $V_{ECQ1} = 3.5\,\text{V}$, and $V_{CEQ2} = 4.0\,\text{V}$. (b) Correlate the results of part (a) with a computer simulation.

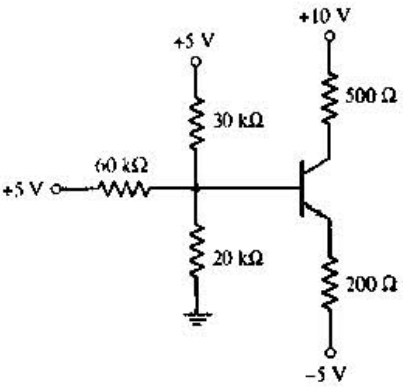


Figure P3.53

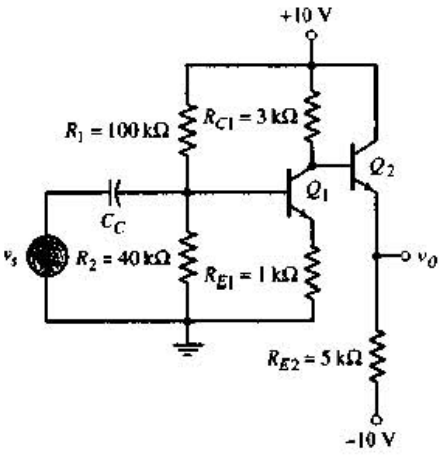


Figure P3.54

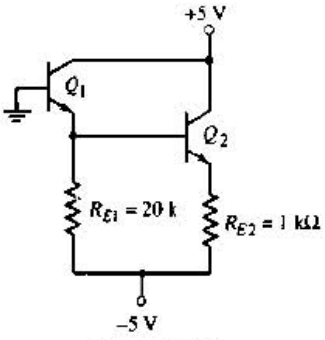


Figure P3.55

COMPUTER ANALYSIS PROBLEMS

3.58 Generate the i_C versus v_{CE} characteristics for an npn silicon bipolar transistor at $T = 300\,^\circ\text{K}$, using a saturation current of $I_S = 10^{-14}\,\text{A}$. Limit the characteristics to $v_{CE}(\text{max}) = 10\,\text{V}$ and $i_C(\text{max}) = 10\,\text{mA}$. Plot curves for: (a) $\beta_F = 100$, $V_A = \infty$ (default value); (b) $\beta_F = 50$, $V_A = \infty$; and (c) $\beta_F = 100$, $V_A = 50\,\text{V}$.

3.59 Correlate the results of Example 3.4 with a computer simulation.

3.60 The circuit shown in Figure P3.18 is driven by a constant-current source. Using a computer simulation, investigate the B–E and C–E voltages as the transistor is driven into saturation.

3.61 For Exercise 3.28, use a computer simulation to obtain a plot of the Q-point values versus temperature over the range $0\,^\circ\text{C} \le T \le 125\,^\circ\text{C}$.

3.62 For Exercise 3.28, use a computer simulation to obtain a plot of the Q-point values versus β over the range $50 \le \beta \le 200$.

DESIGN PROBLEMS

[Note: Each design should be correlated with a computer simulation.]

***D3.63** Consider a common-emitter circuit with the configuration shown in Figure 3.53(a). The circuit parameters are: $V_{CC} = 10\,\text{V}$, $R_E = 0.5\,\text{k}\Omega$, and $R_C = 4\,\text{k}\Omega$. The transistor B–E turn-on voltage is 0.7 V and the current gain is in the range $80 \le \beta \le 120$. Design the circuit such that the nominal Q-point is in the center of the load line and the Q-point parameters do not deviate from the nominal value by more than ±10 percent. In addition, the dc currents in R_1 and R_2 should be at least a factor of ten larger than the quiescent base current.

***D3.64** (a) For the transistors in the circuit shown in Figure 3.57, the parameters are: $V_{BE}(\text{on}) = 0.7\,\text{V}$, and $\beta = 80$. If $R_B = 10\,\text{k}\Omega$ and $R_C = 2\,\text{k}\Omega$, design the circuit such that the quiescent collector–emitter voltage of Q_O is $V_{CEQ}(Q_O) = 3\,\text{V}$. (b) If the three transistors have the same value of β, but the value is in the range $60 \le \beta \le 100$, determine the maximum tolerance in R_1 such that the C–E voltage of Q_O remains in the range $2.7 \le V_{CEQ} \le 3.3\,\text{V}$.

***D3.65** Design a discrete circuit using the configuration shown in Figure P3.65, given that $V^+ = 15\,\text{V}$, $V^- = -15\,\text{V}$, $V_{CEQ} \cong 8\,\text{V}$, and $I_{CQ} \cong 5\,\text{mA}$. The transistor parameters are: $V_{BE}(\text{on}) = 0.7\,\text{V}$, and $100 \le \beta \le 400$. Select standard 5 percent tolerance resistance values.

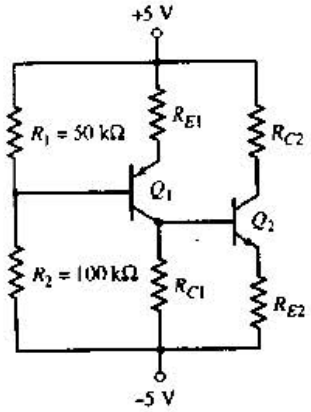


Figure P3.57

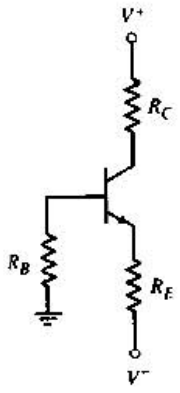


Figure P3.65

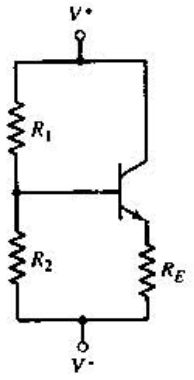


Figure P3.66

***D3.66** Design a discrete emitter-follower with the configuration shown in Figure P3.66, given that $V^+ = 10\,\text{V}$, $V^- = -10\,\text{V}$, $V_{CEQ} \cong (\frac{1}{2})(V^+ - V^-)$, and $I_{CQ} \cong 100\,\text{mA}$. The transistor parameters are: $V_{BE}(\text{on}) = 0.7\,\text{V}$, and $80 \le \beta \le 160$. Select standard 5 percent tolerance resistance values.

***D3.67** Redesign the multistage circuit shown in Figure 3.59 such that $V_{CE1} > 3\,\text{V}$ and $V_{EC2} \cong 5\,\text{V}$. Assume transistor turn-on voltages of 0.7V and nominal transistor gains of $\beta = 100$.

CHAPTER

4

Basic BJT Amplifiers

4.0 PREVIEW

In the last chapter, we described the operation of the bipolar junction transistor, and analyzed and designed the dc response of circuits containing these devices. In this chapter, we emphasize the use of the bipolar transistor in linear amplifier applications.

Linear amplifiers imply that we are dealing with analog signals. The magnitude of an analog signal may have any value and may vary continuously with respect to time. A linear amplifier then means that the output signal is equal to the input signal multiplied by a constant, where the magnitude of the constant of proportionality is, in general, greater than unity. A linear amplifier is capable of producing signal power gain; that is, the power in the output signal is greater than the power in the input signal. We will investigate the source of this "extra" power.

We examine the properties of three basic single-stage, or single-transistor, amplifier circuits. These circuits are the common-emitter, emitter-follower, and common-base configurations. These configurations form the building blocks for more complex amplifiers, so gaining a good understanding of these three amplifier circuits is an important goal of this chapter.

We introduce a few of the many possible multistage configurations in which multiple amplifiers are connected in series, or cascade, to increase the overall small-signal voltage gain or to provide a particular combination of voltage gain and output resistance. Our discussion includes the method of analysis required for these types of circuits and a synopsis of their properties.

4.1 ANALOG SIGNALS AND LINEAR AMPLIFIERS

In this chapter, we will be considering **signals**, **analog** circuits, and **amplifiers**. A signal contains some type of information. For example, sound waves produced by a speaking human contain the information the person is conveying to another person. Our physical senses, such as hearing, vision, and touch, are naturally analog. Analog signals can represent parameters such as temperature, pressure, and wind velocity. Here, we are interested in electrical signals, such as the output signal from a compact disc, a signal from a microphone, or a signal

from a heart rate monitor. The electrical signals are in the form of time-varying currents and voltages.

The magnitude of an **analog signal** can take on any value and may vary continuously with time. Electronic circuits that process analog signals are called **analog circuits**. One example of an analog circuit is a linear amplifier. A **linear amplifier** magnifies an input signal and produces an output signal that is larger and directly proportional to the input signal.

Time-varying signals from a particular source very often need to be amplified before the signal is capable of being "useful." For example, Figure 4.1 shows a signal source that is the output of a compact disc system. That signal consists of a small time-varying voltage and current, which means the signal power is relatively small. The power required to drive the speakers is larger than the output signal from the compact disc, so the compact disc signal must be amplified before it is capable of driving the speakers in order that sound can be heard. Other examples of signals that must be amplified before they are capable of driving loads include the output of a microphone, voice signals received on earth from an orbiting manned shuttle, and video signals from an orbiting weather satellite.

Also shown in Figure 4.1 is a dc voltage source connected to the amplifier. The amplifier contains transistors that must be biased in the forward-active region so that the transistors can act as amplifying devices. We want the output signal to be linearly proportional to the input signal so that the output of the speakers is an exact (as much as possible) reproduction of the signal generated from the compact disc. Therefore, we want the amplifier to be a **linear** amplifier.

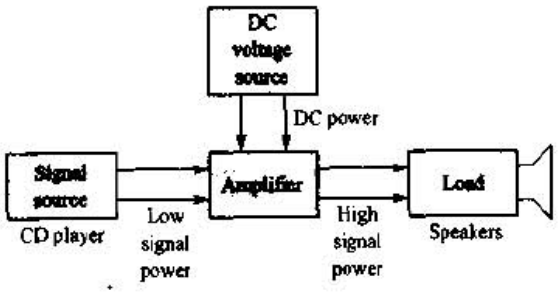


Figure 4.1 Block diagram of a compact disc player system

Figure 4.1 suggests that there are two types of analyses of the amplifier that we must consider. The first is a dc analysis because of the applied dc voltage source, and the second is a time-varying or ac analysis because of the time-varying signal source. A linear amplifier means that the superposition principle applies. The principle of superposition states: *The response of a linear circuit excited by multiple independent input signals is the sum of the responses of the circuit to each of the input signals alone.* For the linear amplifier, then, the dc analysis can be performed with the ac source set to zero, the ac analysis can be performed with the dc source set to zero, and the total response is the sum of the two individual responses.

4.2 THE BIPOLAR LINEAR AMPLIFIER

The transistor is the heart of an amplifier. In this chapter, we will consider bipolar transistor amplifiers. Bipolar transistors have traditionally been used in linear amplifier circuits because of their relatively high gain. In Chapter 6, we will consider the field-effect transistor amplifier, and will compare those results with the bipolar amplifier characteristics developed in this chapter.

We begin our discussion by considering the same bipolar circuit that was discussed in the last chapter. Figure 4.2(a) shows the circuit and Figure 4.2(b) shows the voltage transfer characteristics that were developed in Chapter 3. To use the circuit as an amplifier, the transistor needs to be biased with a dc voltage at a quiescent point (Q-point), as shown in the figure, such that the transistor is biased in the forward-active region. This dc analysis or design of the circuit was the focus of our attention in Chapter 3. If a time-varying (e.g., sinusoidal) signal is superimposed on the dc input voltage, V_{BB}, the output voltage will change along the transfer curve producing a time-varying output voltage. If the time-varying output voltage is directly proportional to and larger than the time-varying input voltage, then the circuit is a linear amplifier. From this figure, we see that if the transistor is not biased in the active region (biased either in cutoff or saturation), the output voltage does not change with a change in the input voltage. Thus, we no longer have an amplifier.

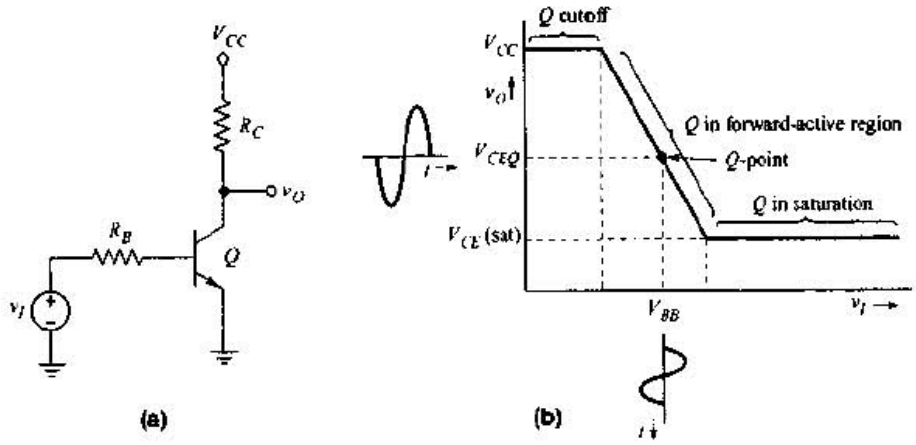


Figure 4.2 (a) Bipolar transistor inverter circuit; (b) inverter transfer characteristics

In this chapter, we are interested in the ac analysis and design of bipolar transistor amplifiers, which means that we must determine the relationships between the time-varying output and input signals. We will initially consider a graphical technique that can provide an intuitive insight into the basic operation of the circuit. We will then develop a small-signal equivalent circuit that will be used in the mathematical analysis of the ac signals. In general, we will be considering a steady-state, sinusoidal analysis of circuits. We will assume that any time-varying signal can be written as a sum of sinusoidal signals of different frequencies and amplitudes (Fourier series), so that a sinusoidal analysis is appropriate.

We will be dealing with time-varying as well as dc currents and voltages in this chapter. Table 4.1 gives a summary of notation that will be used. This

Table 4.1 Summary of notation

Variable	Meaning
i_B, v_{BE}	Total instantaneous values
I_B, V_{BE}	DC values
i_b, v_{be}	Instantaneous ac values
I_b, V_{be}	Phasor values

notation was discussed in the Prologue, but is repeated here for convenience. A lowercase letter with an uppercase subscript, such as i_B or v_{BE}, indicates *total instantaneous values*. An uppercase letter with an uppercase subscript, such as I_B or V_{BE}, indicates *dc quantities*. A lowercase letter with a lowercase subscript, such as i_b or v_{be}, indicates instantaneous values of *ac signals*. Finally, an uppercase letter with a lowercase subscript, such as I_b or V_{be}, indicates *phasor quantities*. The phasor notation, which was reviewed in the Prologue becomes especially important in Chapter 7 during the discussion of frequency response. However, the phasor notation will be generally used in this chapter in order to be consistent with the overall ac analysis.

4.2.1 Graphical Analysis and AC Equivalent Circuit

Figure 4.3 shows the same basic bipolar inverter circuit that has been discussed, but now includes a sinusoidal signal source in series with the dc source. (This circuit is not practical and should not be built in the lab since a dc current flows through the sinusoidal signal source. However, the circuit can be used to conveniently illustrate the basic circuit operation and the mechanism of amplification.)

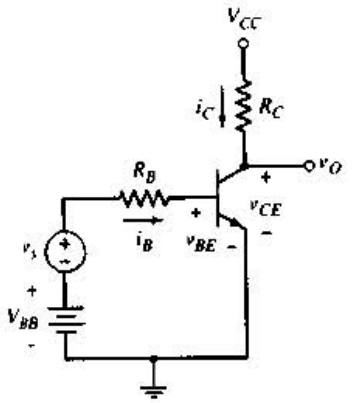


Figure 4.3 A common-emitter circuit with a time-varying signal source in series with the base dc source

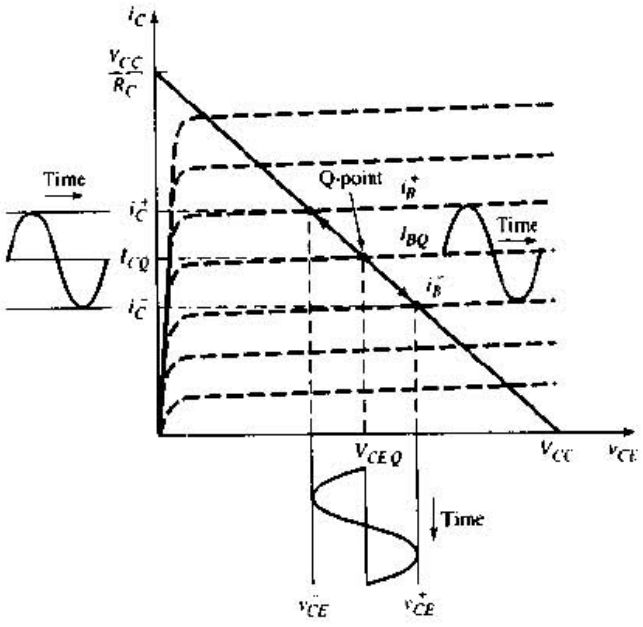


Figure 4.4 Common-emitter transistor characteristics, dc load line, and sinusoidal variation in base current, collector current, and collector–emitter voltage

Figure 4.4 shows the transistor characteristics, the dc load line, and the Q-point. The sinusoidal signal source, v_s, will produce a time-varying or ac base current superimposed on the quiescent base current as shown in the figure. The time-varying base current will induce an ac collector current superimposed on the quiescent collector current. The ac collector current then produces a time-varying voltage across R_C, which induces an ac collector–emitter voltage as shown in the figure. The ac collector–emitter voltage, or output voltage, in general, will be larger than the sinusoidal input signal, so that the circuit has produced signal amplification—that is, the circuit is an amplifier.

We need to develop a mathematical method or model for determining the relationships between the sinusoidal variations in currents and voltages in the circuit. As already mentioned, a linear amplifier implies that superposition applies so that the dc and ac analyses can be performed separately. To obtain a linear amplifier, the time-varying or ac currents and voltages must be small enough to ensure a linear relation between the ac signals. To meet this objective, the time-varying signals are assumed to be *small signals*, which means that the amplitudes of the ac signals are small enough to yield linear relations. The concept of "small enough," or small signal, will be discussed further as we develop the small-signal equivalent circuits.

A time-varying signal source, v_s, in the base of the circuit in Figure 4.3 generates a time-varying component of base current, which implies there is also a time-varying component of base–emitter voltage. Figure 4.5 shows the exponential relationship between base-current and base–emitter voltage. If the magnitudes of the time-varying signals that are superimposed on the dc quiescent point are small, then we can develop a linear relationship between the ac base–emitter voltage and ac base current. This relationship corresponds to the slope of the curve at the Q-point.

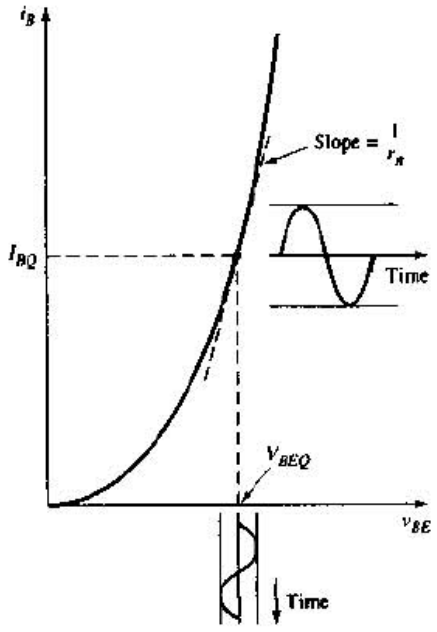


Figure 4.5 Base current versus base–emitter voltage characteristic with superimposed sinusoidal signals

Using Figure 4.5, we can now determine one quantitative definition of small signal. From the discussion in Chapter 3, the relation between base–emitter voltage and base current can be written as

$$i_B = \frac{I_S}{1+\beta_F} \cdot \exp\left(\frac{v_{BE}}{V_T}\right) \tag{4.1}$$

If v_{BE} is composed of a dc term with a sinusoidal component superimposed, i.e., $v_{BE} = V_{BEQ} + v_{be}$, then

$$i_B = \frac{I_S}{1+\beta_F} \cdot \exp\left(\frac{V_{BEQ}+v_{be}}{V_T}\right) = \frac{I_S}{1+\beta_F} \cdot \exp\left(\frac{V_{BEQ}}{V_T}\right) \cdot \exp\left(\frac{v_{be}}{V_T}\right) \tag{4.2}$$

where V_{BEQ} is normally referred to as the base–emitter turn-on voltage, $V_{BE}(\text{on})$. The term $[I_S/(1+\beta_F)] \cdot \exp(V_{BEQ}/V_T)$ is the quiescent base current, so we can write

$$i_B = I_{BQ} \cdot \exp\left(\frac{v_{be}}{V_T}\right) \tag{4.3}$$

The base current, given in this form, cannot be written as an ac current superimposed on a dc quiescent value. However, if $v_{be} \ll V_T$, then we can expand the exponential term in a Taylor series, keeping only the **linear term**. This approximation is what is meant by **small signal**. We then have

$$i_B \cong I_{BQ}\left(1+\frac{v_{be}}{V_T}\right) = I_{BQ} + \frac{I_{BQ}}{V_T} \cdot v_{be} = I_{BQ} + i_b \tag{4.4(a)}$$

where i_b is the time-varying (sinusoidal) base current given by

$$i_b = \left(\frac{I_{BQ}}{V_T}\right) v_{be} \tag{4.4(b)}$$

The sinusoidal base current, i_b, is linearly related to the sinusoidal base–emitter voltage, v_{be}. In this case, the term small-signal refers to the condition in which v_{be} is sufficiently small for the linear relationships between i_b and v_{be} given by Equation (4.4(b)) to be valid. As a general rule, if v_{be} is less than 10 mV, then the exponential relation given by Equation (4.3) and its linear expansion in Equation (4.4(a)) agree within approximately 5 percent.

From the concept of small signal, all the time-varying signals shown in Figure 4.4 will be linearly related and are superimposed on dc values. We can write (refer to notation given in Table 4.1)

$$i_B = I_{BQ} + i_b \tag{4.5(a)}$$

$$i_C = I_{CQ} + i_c \tag{4.5(b)}$$

$$v_{CE} = V_{CEQ} + v_{ce} \tag{4.5(c)}$$

and

$$v_{BE} = V_{BEQ} + v_{be} \tag{4.5(d)}$$

If the signal source, v_s, is zero, then the base–emitter and collector–emitter loop equations are,

$$V_{BB} = I_{BQ}R_B + V_{BEQ} \tag{4.6(a)}$$

and

$$V_{CC} = I_{CQ}R_C + V_{CEQ} \tag{4.6(b)}$$

Taking into account the time-varying signals, we find the base–emitter loop equation is

$$V_{BB} + v_s = i_B R_B + v_{BE} \tag{4.7(a)}$$

or

$$V_{BB} + v_s = (I_{BQ} + i_b)R_B + (V_{BEQ} + v_{be}) \tag{4.7(b)}$$

Rearranging terms, we find

$$V_{BB} - I_{BQ}R_B - V_{BEQ} = i_b R_B + v_{be} - v_s \tag{4.7(c)}$$

From Equation (4.6(a)), the left side of Equation (4.7(c)) is zero. Equation (4.7(c)) can then be written as

$$v_s = i_b R_B + v_{be} \tag{4.8}$$

which is the base–emitter loop equation with all dc terms set equal to zero.

Taking into account the time-varying signals, the collector–emitter loop equation is

$$V_{CC} = i_C R_C + v_{CE} = (I_{CQ} + i_c)R_C + (V_{CEQ} + v_{ce}) \tag{4.9(a)}$$

Rearranging terms, we find

$$V_{CC} - I_{CQ}R_C - V_{CEQ} = i_c R_C + v_{ce} \tag{4.9(b)}$$

From Equation (4.6(b)), the left side of Equation (4.9(b)) is zero. Equation (4.9(b)) can be written as

$$i_c R_C + v_{ce} = 0 \tag{4.10}$$

which is the collector–emitter loop equation with all dc terms set equal to zero.

Equations (4.8) and (4.10) relate the ac parameters in the circuit. These equations can be obtained directly by setting all dc currents and voltages equal to zero, so the dc voltage sources become short circuits and any dc current sources would become open circuits. *These results are a direct consequence of applying superposition to a linear circuit.* The resulting BJT circuit, shown in Figure 4.6, is called the *ac equivalent circuit*, and all currents and voltages shown are time-varying signals. We should stress that this circuit is an

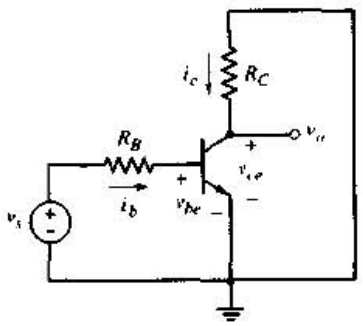


Figure 4.6 The ac equivalent circuit of the common-emitter circuit with an npn transistor

equivalent circuit. We are implicitly assuming that the transistor is still biased in the forward-active region with the appropriate dc voltages and currents.

Another way of looking at the ac equivalent circuit is as follows. In the circuit in Figure 4.3, the base and collector currents are composed of ac signals superimposed on dc values. These currents flow through the V_{BB} and V_{CC} voltage sources, respectively. Since the voltages across these sources are assumed to remain constant, the sinusoidal currents do not produce any sinusoidal voltages across these elements. Then, since the sinusoidal voltages are zero, the equivalent ac impedances are zero, or short circuits. In other words, the dc voltage sources are ac short circuits in an equivalent ac circuit. We say that the node connecting R_C and V_{CC} is at signal ground.

4.2.2 Small-Signal Hybrid-π Equivalent Circuit of the Bipolar Transistor

We developed the ac equivalent circuit shown in Figure 4.6. We now need to develop a **small-signal equivalent circuit** for the transistor. One such circuit is the **hybrid-π** model, which is closely related to the physics of the transistor. This effect will become more apparent in Chapter 7 when a more detailed hybrid-π model is developed to take into account the frequency response of the transistor.

We can treat the bipolar transistor as a two-port network as shown in Figure 4.7. One element of the hybrid-π model has already been described. Figure 4.5 showed the base current versus base–emitter voltage characteristic, with small time-varying signals superimposed at the Q-point. Since the sinusoidal signals are small, we can treat the slope at the Q-point as a constant, which has units of conductance. The inverse of this conductance is the small-signal resistance defined as r_π. We can then relate the small-signal input base current to the small-signal input voltage by

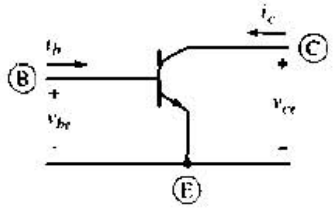


Figure 4.7 The BJT as a small-signal, two-port network

$$v_{be} = i_b r_\pi \tag{4.11}$$

where $1/r_\pi$ is equal to the slope of the i_B–v_{BE} curve, as shown in Figure 4.5. We then find r_π from

$$\frac{1}{r_\pi} = \left.\frac{\partial i_B}{\partial v_{BE}}\right|_{Q\text{-pt}} = \left.\frac{\partial}{\partial v_{BE}}\left[\frac{I_S}{1+\beta_F}\cdot\exp\left(\frac{v_{BE}}{V_T}\right)\right]\right|_{Q\text{-pt}} \tag{4.12(a)}$$

or

$$\frac{1}{r_\pi} = \frac{1}{V_T}\cdot\left[\frac{I_S}{1+\beta_F}\cdot\exp\left(\frac{v_{BE}}{V_T}\right)\right]\Bigg|_{Q\text{-pt}} = \frac{I_{BQ}}{V_T} \tag{4.12(b)}$$

Then

$$\frac{v_{be}}{i_b} = r_\pi = \frac{V_T}{I_{BQ}} = \frac{\beta_F V_T}{I_{CQ}} \tag{4.13}$$

The resistance r_π is called the **diffusion resistance** or base–emitter input resistance. We note that r_π is a function of the Q-point parameters.

We can consider the output terminal characteristics of the bipolar transistor. If we initially consider the case in which the output collector current is

independent of the collector–emitter voltage, then the collector current is a function only of the base–emitter voltage, as discussed in Chapter 3. We can then write

$$\Delta i_C = \left.\frac{\partial i_C}{\partial v_{BE}}\right|_{Q\text{-}pt} \cdot \Delta v_{BE} \tag{4.14(a)}$$

or

$$i_c = \left.\frac{\partial i_C}{\partial v_{BE}}\right|_{Q\text{-}pt} \cdot v_{be} \tag{4.14(b)}$$

From Chapter 3, we had written

$$i_C = \alpha I_S \exp\left(\frac{v_{BE}}{V_T}\right) \tag{4.15}$$

Then

$$\left.\frac{\partial i_C}{\partial v_{BE}}\right|_{Q\text{-}pt} = \frac{1}{V_T} \cdot \alpha I_S \exp\left(\frac{v_{BE}}{V_T}\right)\Bigg|_{Q\text{-}pt} = \frac{I_{CQ}}{V_T} \tag{4.16}$$

The term $\alpha I_S \exp(v_{BE}/V_T)$ evaluated at the Q-point is just the quiescent collector current. The term I_{CQ}/V_T is a conductance. Since this conductance relates a current in the collector to a voltage in the B–E circuit, the parameter is called a **transconductance** and is written

$$g_m = \frac{I_{CQ}}{V_T} \tag{4.17}$$

The small-signal transconductance is also a function of the Q-point parameters and is directly proportional to the dc bias current.

Using these new parameters, we can develop a simplified small-signal hybrid-π equivalent circuit for the npn bipolar transistor, as shown in Figure 4.8. The phasor components are given in parentheses. This circuit can be inserted into the ac equivalent circuit previously shown in Figure 4.6.

We can develop a slightly different form for the output of the equivalent circuit. We can relate the small-signal collector current to the small-signal base current. We can write

$$\Delta i_C = \left.\frac{\partial i_C}{\partial i_B}\right|_{Q\text{-}pt} \cdot \Delta i_B \tag{4.18(a)}$$

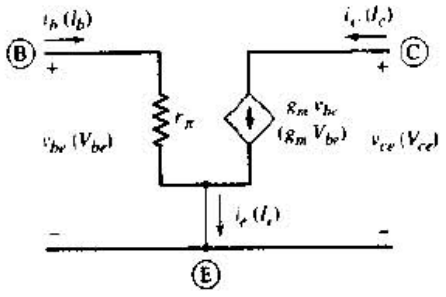


Figure 4.8 A simplified small-signal hybrid-π equivalent circuit for the npn transistor

or

$$i_c = \left.\frac{\partial i_C}{\partial i_B}\right|_{Q\text{-}pt} \cdot i_b \tag{4.18(b)}$$

where

$$\left.\frac{\partial i_C}{\partial i_B}\right|_{Q\text{-}pt} \equiv \beta \tag{4.18(c)}$$

and is called an incremental or ac common-emitter current gain. We can then write

$$i_c = \beta i_b \tag{4.19}$$

The small-signal equivalent circuit of the bipolar transistor in Figure 4.9 uses this parameter. The parameters in this figure are also given as phasors. This circuit can also be inserted in the ac equivalent circuit given in Figure 4.6. Either equivalent circuit, Figure 4.8 or 4.9, may be used. We will use both circuits in the examples that follow in this chapter.

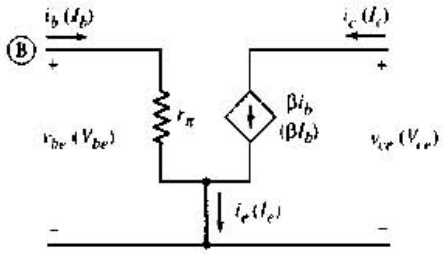


Figure 4.9 BJT small-signal equivalent circuit using common-emitter current gain

Relation between β_F and β

At this point, we need to pause and discuss the relationship between β_F and β. The difference between the two terms is illustrated in Figure 4.10. The term β_F is the ratio of dc collector current to dc base current. These currents include any leakage currents that might exist. As just mentioned, the term β is the ratio of the incremental change in collector current to the incremental change in base current. In an ideal BJT, these terms are identical.

In the derivation of r_π and g_m, the ideal exponential relation between current and base–emitter voltage was assumed. This implies that leakage currents are negligible. If we multiply r_π and g_m, we find

$$r_\pi g_m = \left(\frac{\beta_F V_T}{I_{CQ}}\right) \cdot \left(\frac{I_{CQ}}{V_T}\right) = \beta_F \tag{4.20}$$

Since leakage currents were neglected, and assuming β_F is independent of collector current, the β_F term is actually equivalent to the ac β. In general, we will assume that β and β_F are equivalent throughout the remainder of the text. However, we must keep in mind that β may vary from one device to another and that β does vary with collector current. This variation with I_C will be specified on data sheets for specific transistors.

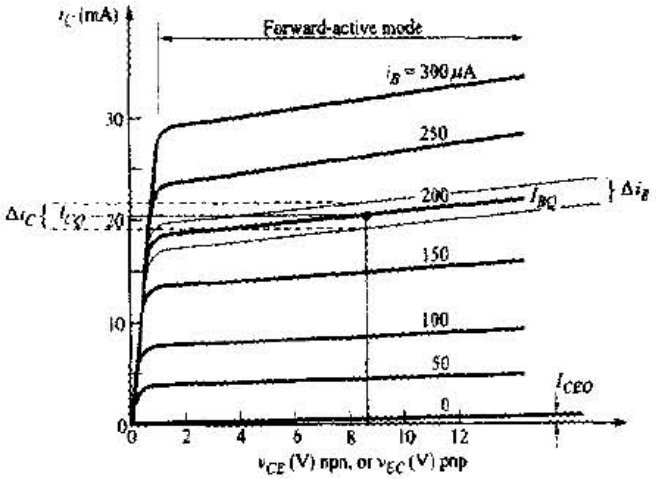


Figure 4.10 Transistor characteristics showing definitions of β_F and β

Continuing our discussion of equivalent circuits, we may now insert the bipolar equivalent circuit in Figure 4.8, for example, into the ac equivalent circuit in Figure 4.6. The result is shown in Figure 4.11. Note that we are using the phasor notation.

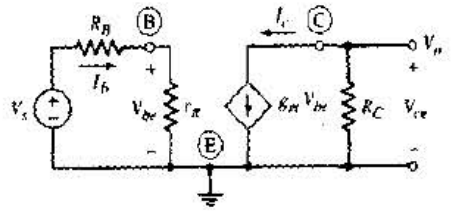


Figure 4.11 The small-signal equivalent circuit of the common-emitter circuit using the npn transistor hybrid-π model

The **small-signal voltage gain**, $A_v = V_o/V_s$, of the circuit is defined as the ratio of output signal voltage to input signal voltage. The dependent current $g_m V_{be}$ flows through R_C, producing a negative collector–emitter voltage, or

$$V_o = V_{ce} = -(g_m V_{be})R_C \tag{4.21}$$

and, from the input portion of the circuit, we find

$$V_{be} = \left(\frac{r_\pi}{r_\pi + R_B}\right) \cdot V_s \tag{4.22}$$

The small-signal voltage gain is then

$$A_v = \frac{V_o}{V_s} = -(g_m R_C) \cdot \left(\frac{r_\pi}{r_\pi + R_B}\right) \tag{4.23}$$

Example 4.1 **Objective:** Calculate the small-signal voltage gain of the bipolar transistor circuit shown in Figure 4.3.

Assume the transistor and circuit parameters are: $\beta = 100$, $V_{CC} = 12\,\text{V}$, $V_{BE} = 0.7\,\text{V}$, $R_C = 6\,\text{k}\Omega$, $R_B = 50\,\text{k}\Omega$, and $V_{BB} = 1.2\,\text{V}$.

DC Solution: We first do the dc analysis to find the Q-point values. We obtain

$$I_{BQ} = \frac{V_{BB} - V_{BE}(\text{on})}{R_B} = \frac{1.2 - 0.7}{50} \Rightarrow 10\,\mu\text{A}$$

so that

$$I_{CQ} = \beta I_{BQ} = (100)(10\,\mu\text{A}) \Rightarrow 1\,\text{mA}$$

Then,

$$V_{CEQ} = V_{CC} - I_{CQ}R_C = 12 - (1)(6) = 6\,\text{V}$$

Therefore, the transistor is biased in the forward-active mode.

AC Solution: The small-signal hybrid-π parameters are

$$r_\pi = \frac{\beta V_T}{I_{CQ}} = \frac{(100)(0.026)}{1} = 2.6\,\text{k}\Omega$$

and

$$g_m = \frac{I_{CQ}}{V_T} = \frac{1}{0.026} = 38.5\,\text{mA/V}$$

The small-signal voltage gain is determined using the small-signal equivalent circuit shown in Figure 4.11. From Equation (4.23), we find

$$A_v = \frac{V_o}{V_s} \simeq -(g_m R_C) \cdot \left(\frac{r_\pi}{r_\pi + R_B}\right)$$

or

$$= -(38.5)(6)\left(\frac{2.6}{2.6 + 50}\right) = -11.4$$

Comment: We see that the magnitude of the sinusoidal output voltage is 11.4 times the magnitude of the sinusoidal input voltage. We will see that other circuit configurations result in even larger small-signal voltage gains.

Discussion: We may consider a specific sinusoidal input voltage. Let

$$v_s = 0.25 \sin \omega t\,\text{V}$$

The sinusoidal base current is given by

$$i_b = \frac{v_s}{R_B + r_\pi} = \frac{0.25 \sin \omega t}{50 + 2.6} \rightarrow 4.75 \sin \omega t\,\mu\text{A}$$

The sinusoidal collector current is

$$i_c = \beta i_b = (100)(4.75 \sin \omega t) \rightarrow 0.475 \sin \omega t\,\text{mA}$$

and the sinusoidal collector-emitter voltage is

$$v_{ce} = -i_c R_C = -(0.475)(6) \sin \omega t = -2.85 \sin \omega t\,\text{V}$$

Figure 4.12 shows the various currents and voltages in the circuit. These include the sinusoidal signals superimposed on the dc values. Figure 4.12(a) shows the sinusoidal input voltage, and Figure 4.12(b) shows the sinusoidal base current superimposed on the quiescent value. The sinusoidal collector current superimposed on the dc quiescent value is shown in Figure 4.12(c). Note that, as the base current increases, the collector current increases.

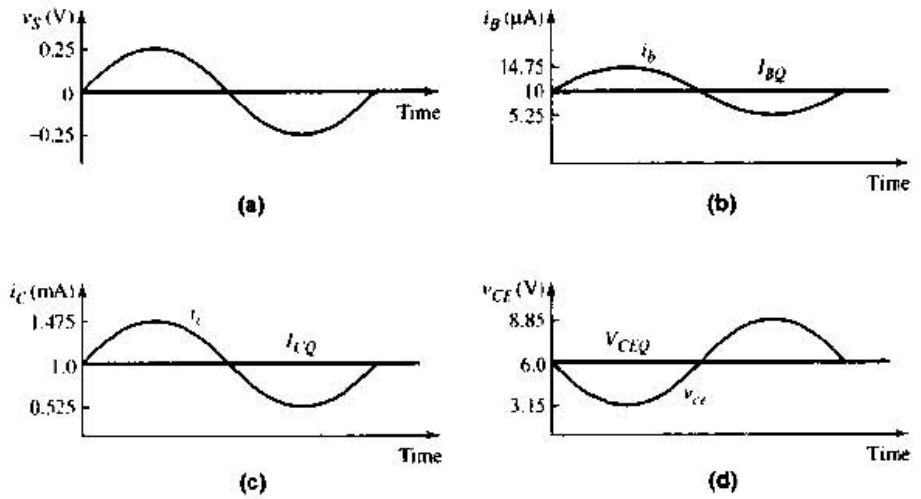


Figure 4.12 The common-emitter circuit: (a) input voltage, (b) input base current, (c) output collector current, and (d) output collector–emitter voltage

Figure 4.12(d) shows the sinusoidal component of the C–E voltage superimposed on the quiescent value. As the collector current increases, the voltage drop across R_C increases so that the C–E voltage decreases. Consequently, the sinusoidal component of the output voltage is 180 degrees out of phase with respect to the input signal voltage. The minus sign in the voltage gain expression represents this 180-degree **phase shift**.

Analysis Method: To summarize, the analysis of a BJT amplifier proceeds as shown in the box "Problem Solving Method: Bipolar AC Analysis."

Problem-Solving Technique: Bipolar AC Analysis

Since we are dealing with linear amplifier circuits, superposition applies, which means that we can perform the dc and ac analyses separately. The analysis of the BJT amplifier proceeds as follows:

1. Analyze the circuit with only the dc sources present. This solution is the dc or quiescent solution, which uses the dc signal models for the elements, as listed in Table 4.2. The transistor must be biased in the forward-active region in order to produce a linear amplifier.
2. Replace each element in the circuit with its small-signal model, as shown in Table 4.2. The small-signal hybrid-π model applies to the transistor although it is not specifically listed in the table.
3. Analyze the small-signal equivalent circuit, setting the dc source components equal to zero, to produce the response of the circuit to the time-varying input signals only.

In Table 4.2, the dc model of the resistor is a resistor, the capacitor model is an open circuit, and the inductor model is a short circuit. The forward-biased diode model includes the cut-in voltage V_γ and the forward resistance r_f.

Table 4.2 Transformation of elements in dc and small-signal analysis

Element	I-V relationship	DC model	AC model
Resistor	$I_R = \frac{V}{R}$	R	R
Capacitor	$I_C = sCV$	Open	C
Inductor	$I_L = \frac{V}{sL}$	Short	L
Diode	$I_D = I_S(e^{v_D/V_T} - 1)$	$+V_\gamma - r_f$	$r_d = V_T/I_D$
Independent voltage source	V_S = constant	$+ V_S -$	Short
Independent current source	I_S = constant	I_S	Open

Table suggested by Richard Hester of Iowa State University.

The small-signal models of R, L, and C remain the same. However, if the signal frequency is sufficiently high, the impedance of a capacitor can be approximated by a short circuit. The small-signal, low-frequency model of the diode becomes the diode diffusion resistance r_d. Also, the independent dc voltage source becomes a short circuit, and the independent dc current source becomes an open circuit.

4.2.3 Hybrid-π Equivalent Circuit, Including the Early Effect

So far in the small-signal equivalent circuit, we have assumed that the collector current is independent of the collector–emitter voltage. We discussed the Early effect in the last chapter in which the collector current does vary with collector-emitter voltage. Equation (3.16) in the previous chapter gives the relation

$$i_C = \alpha I_S\left[\exp\left(\frac{v_{BE}}{V_T}\right)\right] \cdot \left(1 + \frac{v_{CE}}{V_A}\right) \tag{3.16}$$

where V_A is the Early voltage. The equivalent circuits in Figures 4.8 and 4.9 can be expanded to take into account the Early voltage.

The output resistance r_o is defined as

$$r_o = \left.\frac{\partial v_{CE}}{\partial i_C}\right|_{Q\text{-}pt} \tag{4.24}$$

Using Equations (3.16) and (4.24), we can write

$$\frac{1}{r_o} = \left.\frac{\partial i_C}{\partial v_{CE}}\right|_{Q\text{-}pt} = \left.\frac{\partial}{\partial v_{CE}}\left\{\alpha I_S\left[\exp\left(\frac{v_{BE}}{V_T}\right)\left(1 + \frac{v_{CE}}{V_A}\right)\right]\right\}\right|_{Q\text{-}pt} \tag{4.25(a)}$$

or

$$\frac{1}{r_o} = \alpha I_S\left[\exp\left(\frac{v_{BE}}{V_T}\right)\right] \cdot \left.\frac{1}{V_A}\right|_{Q\text{-}pt} \cong \frac{I_{CQ}}{V_A} \tag{4.25(b)}$$

Then

$$r_o = \frac{V_A}{I_{CQ}} \tag{4.26}$$

and is called **the small-signal transistor output resistance.**

This resistance can be thought of as an equivalent Norton resistance, which means that r_o is in parallel with the dependent current sources. Figure 4.13(a) and (b) show the modified bipolar equivalent circuits including the output resistance r_o.

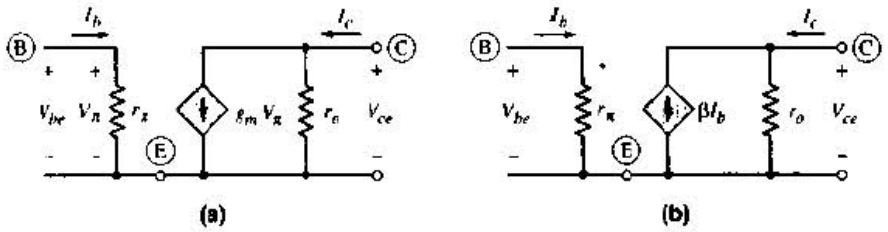


Figure 4.13 Expanded small-signal model of the BJT, including the Early effect, for the case when the circuit contains the (a) transconductance and (b) the current gain parameters

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Example 4.2 **Objective:** Determine the small-signal voltage gain, including the effect of the transistor output resistance r_o.

Reconsider the circuit shown in Figure 4.1, with the parameters given in Example 4.1. In addition, assume the Early voltage is $V_A = 50\,\text{V}$.

Solution: The small-signal output resistance r_o is determined to be

$$r_o = \frac{V_A}{I_{CQ}} = \frac{50}{1\,\text{mA}} = 50\,\text{k}\Omega$$

Using the small-signal equvialent circuit in Figure 4.11, we see that the output resistance r_o is in parallel with R_C. The small-signal voltage gain is therefore

$$A_v = \frac{V_o}{V_i} = -g_m(R_C \| r_o)\left(\frac{r_\pi}{r_\pi + R_B}\right)$$
$$= -(38.5)(6\|50)\left(\frac{2.6}{2.6+50}\right) = -10.2$$

Comment: Comparing this result to that of Example 4.1, we see that r_o reduces the magnitude of the small-signal voltage gain. In many cases, the magnitude of r_o is much larger than that of R_C, which means that the effect of r_o is negligible.

Test Your Understanding

4.1 A BJT with $\beta = 120$ and $V_A = 150\,\text{V}$ is biased such that $I_{CQ} = 0.25\,\text{mA}$. Determine g_m, r_π, and r_o. (Ans. $g_m = 9.62\,\text{mA/V}$, $r_\pi = 12.5\,\text{k}\Omega$, $r_o = 600\,\text{k}\Omega$)

4.2 The Early voltage of a BJT is $V_A = 75\,V$. Determine the minimum required collector current such that the output resistance is at least $r_o = 200\,k\Omega$. (Ans. $I_{CQ} = 0.375\,mA$)

The hybrid-π model derives its name, in part, from the hybrid nature of the parameter units. The four parameters of the equivalent circuits shown in Figures 4.13(a) and 4.13(b) are: input resistance r_π (ohms), current gain β (dimensionless), output resistance r_o (ohms), and transconductance g_m (mhos).

Up to this point, we have considered only circuits with npn bipolar transistors. However, the same basic analysis and equivalent circuit also applies to the pnp transistor. Figure 4.14(a) shows a circuit containing a pnp transistor. Here again, we see the change of current directions and voltage polarities compared to the circuit containing the npn transistor. Figure 4.14(b) is the ac equivalent circuit, with the dc voltage sources replaced by an ac short circuit, and all current and voltages shown are only the sinusoidal components.

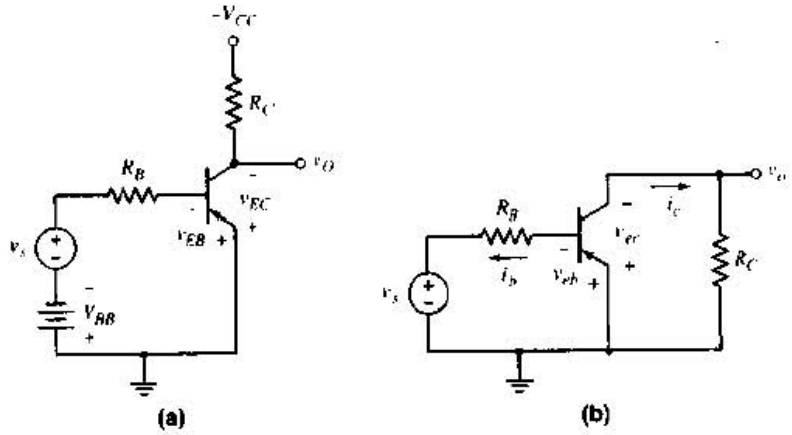


Figure 4.14 (a) A common-emitter circuit with a pnp transistor and (b) the corresponding ac equivalent circuit

The transistor in Figure 4.14(b) can now be replaced by either of the hybrid-π equivalent circuits shown in Figure 4.15. The hybrid-π equivalent circuit of the pnp transistor is the same as that of the npn device, except that again all current directions and voltage polarities are reversed. The hybrid-π parameters are determined by using exactly the same equations as

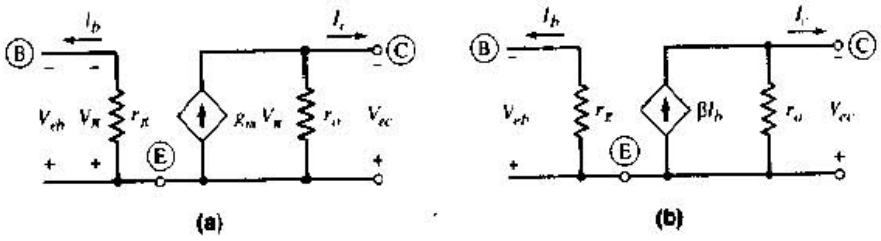


Figure 4.15 The hybrid-π model of the pnp transistor with (a) the transconductance parameter and (b) the current gain parameter

for the npn device; that is, Equation (4.13) for r_π, Equation (4.17) for g_m, and Equation (4.26) for r_o.

We can note that, in the small-signal equivalent circuits in Figure 4.15, if we define currents of opposite direction and voltages of opposite polarity, the equivalent circuit model is exactly the same as that of the npn bipolar transistor. However, the author prefers to use the models shown in Figure 4.15 because the current directions and voltage polarities are consistent with the pnp device.

Combining the hybrid-π model of the pnp transistor (Figure 4.15(a)) with the ac equivalent circuit (Figure 4.14(b)), we obtain the small-signal equivalent circuit shown in Figure 4.16. The output voltage is given by

$$V_o = (g_m V_\pi)(r_o \| R_C) \tag{4.27}$$

The control voltage V_π can be expressed in terms of the input signal voltage V_s using a voltage divider equation. Taking into account the polarity, we find

$$V_\pi = -\frac{V_s r_\pi}{R_B + r_\pi} \tag{4.28}$$

Combining Equations (4.27) and (4.28), we obtain the small-signal voltage gain:

$$A_v = \frac{V_o}{V_s} = \frac{-g_m r_\pi}{R_B + r_\pi}(r_o \| R_C) = \frac{-\beta}{R_B + r_\pi}(r_o \| R_C) \tag{4.29}$$

The expression for the small-signal voltage gain of the circuit containing a pnp transistor is exactly the same as that for the npn transistor circuit. Taking into account the reversed current directions and voltage polarities, the voltage gain still contains a negative sign indicating a 180-degree phase shift between the input and output signals.

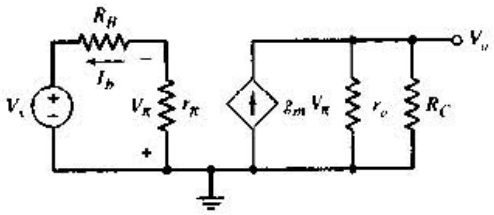


Figure 4.16 The small-signal equivalent circuit of the common-emitter circuit with a pnp transistor

Test Your Understanding

4.3 For the circuit in Figure 4.3 let $\beta = 150$, $V_A = 200\,\text{V}$, $V_{CC} = 7.5\,\text{V}$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, $R_C = 15\,\text{k}\Omega$, $R_B = 100\,\text{k}\Omega$, and $V_{BB} = 0.92\,\text{V}$. (a) Determine the small-signal hybrid-π parameters r_π, g_m, and r_o. (b) Find the small-signal voltage gain $A_v = V_o/V_s$. (Ans. (a) $g_m = 12.7\,\text{mA/V}$, $r_\pi = 11.8\,\text{k}\Omega$, $r_o = 606\,\text{k}\Omega$ (b) $A_v = -19.6$)

4.4 For the circuit in Figure 4.14(a), let $\beta = 90$, $V_A = 120\,\text{V}$, $V_{CC} = 5\,\text{V}$, $V_{EB}(\text{on}) = 0.7\,\text{V}$, $R_C = 2.5\,\text{k}\Omega$, $R_B = 50\,\text{k}\Omega$, and $V_{BB} = 1.145\,\text{V}$. (a) Determine the small-signal hybrid-π parameters r_π, g_m, and r_o. (b) Find the small-signal voltage gain $A_v = V_o/V_s$. (Ans. (a) $g_m = 30.8\,\text{mA/V}$, $r_\pi = 2.92\,\text{k}\Omega$, $r_o = 150\,\text{k}\Omega$ (b) $A_v = -4.17$)

4.2.4 Expanded Hybrid-π Equivalent Circuit

Figure 4.17 shows an expanded hybrid-π equivalent circuit, which includes two additional resistances, r_b and r_μ.

The parameter r_b is the **series resistance** of the semiconductor material between the external base terminal B and an idealized internal base region B′. Typically, r_b is a few tens of ohms and is usually much smaller than r_π; therefore, r_b is normally negligible at low frequencies. However, at high frequencies, r_b may not be negligible, since the input impedance becomes capacitive, as we will see in Chapter 7.

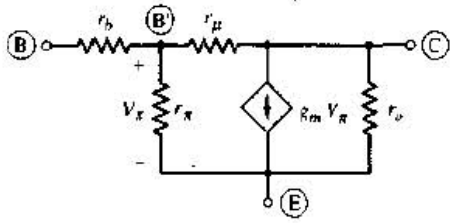


Figure 4.17 Expanded hybrid-π equivalent circuit

The parameter r_μ is the **reverse-biased diffusion resistance** of the base–collector junction. This resistance is typically on the order of megohms and can normally be neglected (an open circuit). However, the resistance does provide some feedback between the output and input, meaning that the base current is a slight function of the collector–emitter voltage.

In this text, when we use the hybrid-π equivalent circuit model, we will neglect both r_b and r_μ, unless they are specifically included.

4.2.5 Other Small-Signal Parameters and Equivalent Circuits

Other small-signal parameters can be developed to model the bipolar transistor or other transistors described in the following chapters.

One common equivalent circuit model for bipolar transistor uses the ***h*-parameters**, which relate the small-signal terminal currents and voltages of a two-port network. These parameters are normally given in bipolar transistor data sheets, and are convenient to determine experimentally at low frequency.

Figure 4.18(a) shows the small-signal terminal current and voltage phasors for a common-emitter transistor. If we assume the transistor is biased at a *Q*-

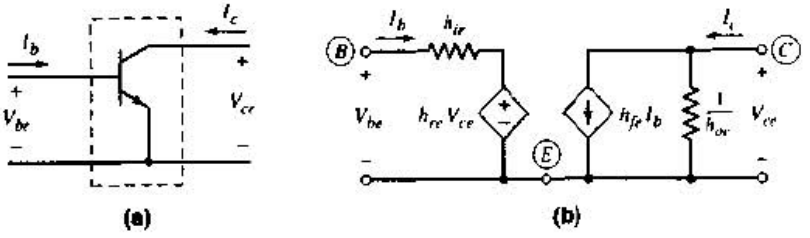


Figure 4.18 (a) Common-emitter npn transistor and (b) the *h*-parameter model of the common-emitter bipolar transistor

point in the forward-active region, the linear relationships between the small-signal terminal currents and voltages can be written as

$$V_{be} = h_{ie} I_b + h_{re} V_{ce} \tag{4.30(a)}$$

$$I_c = h_{fe} I_b + h_{oe} V_{ce} \tag{4.30(b)}$$

These are the defining equations of the common–emitter h-parameters, where the subscripts are: i for input, r for reverse, f for forward, o for output, and e for common emitter.

These equations can be used to generate the small-signal h-parameter equivalent circuit, as shown in Figure 4.18(b). Equation (4.30(a)) represents a Kirchhoff voltage law equation at the input, and the resistance h_{ie} is in series with a dependent voltage source equal to $h_{re} V_{ce}$. Equation (4.30(b)) represents a Kirchhoff current law equation at the output, and the conductance h_{oe} is in parallel with a dependent current source equal to $h_{fe} I_b$.

Since both the hybrid-π and h-parameters can be used to model the characteristics of the same transistor, these parameters are not independent. We can relate the hybrid-π and h-parameters using the equivalent circuit shown in Figure 4.17. The **small-signal input resistance** h_{ie}, from Equation (4.30(a)), can be written as

$$h_{ie} = \left. \frac{V_{be}}{I_b} \right|_{V_{ce} = 0} \tag{4.31}$$

where the small-signal C–E voltage is held zero. With the C–E voltage equal to zero, the circuit in Figure 4.17 is transformed to the one shown in Figure 4.19. From this figure, we see that

$$h_{ie} = r_b + r_\pi \| r_\mu \tag{4.32}$$

In the limit of a very small r_b and a very large r_μ, $h_{ie} \cong r_\pi$.

The parameter h_{fe} is the **small-signal current gain**. From Equation (4.30(b)), this parameter can be written as

$$h_{fe} = \left. \frac{I_c}{I_b} \right|_{V_{ce} = 0} \tag{4.33}$$

Since the collector–emitter voltage is again zero, we can use Figure 4.19, for which the short-circuit collector current is

$$I_c = g_m V_\pi \tag{4.34}$$

If we again consider the limit of a very small r_b and a very large r_μ, then

$$V_\pi = I_b r_\pi$$

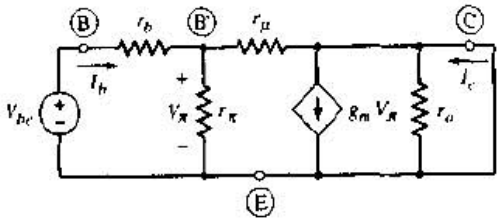


Figure 4.19 Expanded hybrid-π equivalent circuit with the output short-circuited

and

$$h_{fe} = \left.\frac{I_c}{I_b}\right|_{V_{ce}=0} = g_m r_\pi = \beta \tag{4.35}$$

Consequently, at low frequency, the small-signal current gain h_{fe} is essentially equal to β in most situations.

The parameter h_{re} is called the **voltage feedback ratio**, which, from Equation (4.30(a)), can be written as

$$h_{re} = \left.\frac{V_{be}}{V_{ce}}\right|_{I_b=0} \tag{4.36}$$

Since the input signal base current is zero, the circuit in Figure 4.17 is transformed to that shown in Figure 4.20, from which we can see that

$$V_{be} = V_\pi = \left(\frac{r_\pi}{r_\pi + r_\mu}\right) \cdot V_{ce} \tag{4.37(a)}$$

and

$$h_{re} = \left.\frac{V_{be}}{V_{ce}}\right|_{I_b=0} = \frac{r_\pi}{r_\pi + r_\mu} \tag{4.37(b)}$$

Since $r_\pi \ll r_\mu$, this can be approximated as

$$h_{re} \cong \frac{r_\pi}{r_\mu} \tag{4.38}$$

Since r_π is normally in the kilohm range and r_μ is in the megohm range, the value of h_{re} is very small and can usually be neglected.

The fourth h-parameter is the **small-signal output admittance** h_{oe}. From Equation (4.30(b)), we can write

$$h_{oe} = \left.\frac{I_c}{V_{ce}}\right|_{I_b=0} \tag{4.39}$$

Since the input signal base current is again set equal to zero, the circuit in Figure 4.20 is applicable, and a Kirchhoff current law equation at the output node produces

$$I_c = g_m V_\pi + \frac{V_{ce}}{r_o} + \frac{V_{ce}}{r_\pi + r_\mu} \tag{4.40}$$

where V_π is given by Equation (4.37(a)). For $r_\pi \ll r_\mu$, Equation (4.40) becomes

$$h_{oe} = \left.\frac{I_c}{V_{ce}}\right|_{I_b=0} = \frac{1+\beta}{r_\mu} + \frac{1}{r_o} \tag{4.41}$$

In the ideal case, r_μ is infinite, which means that $h_{oe} = 1/r_o$.

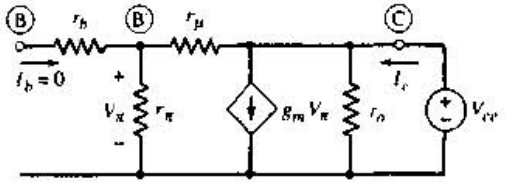


Figure 4.20 Expanded hybrid-π equivalent circuit with the input open-circuited

The h-parameters for a pnp transistor are defined in the same way as those for an npn device. Also, the small-signal equivalent circuit for a pnp transistor using h-parameters is identical to that of an npn device, except that the current directions and voltage polarities are reversed.

Example 4.3 **Objective:** *Determine the h-parameters of a specific transistor.*

The 2N2222A transistor is a commonly used npn transistor. Data for this transistor are shown in Figure 4.21. Assume the transistor is biased at $I_C = 1$ mA and let $T = 300^\circ$K.

Solution: In Figure 4.21, we see that the small-signal current gain h_{fe} is generally in the range $100 < h_{fe} < 170$ for $I_C = 1$ mA, and the corresponding value of h_{ie} is generally

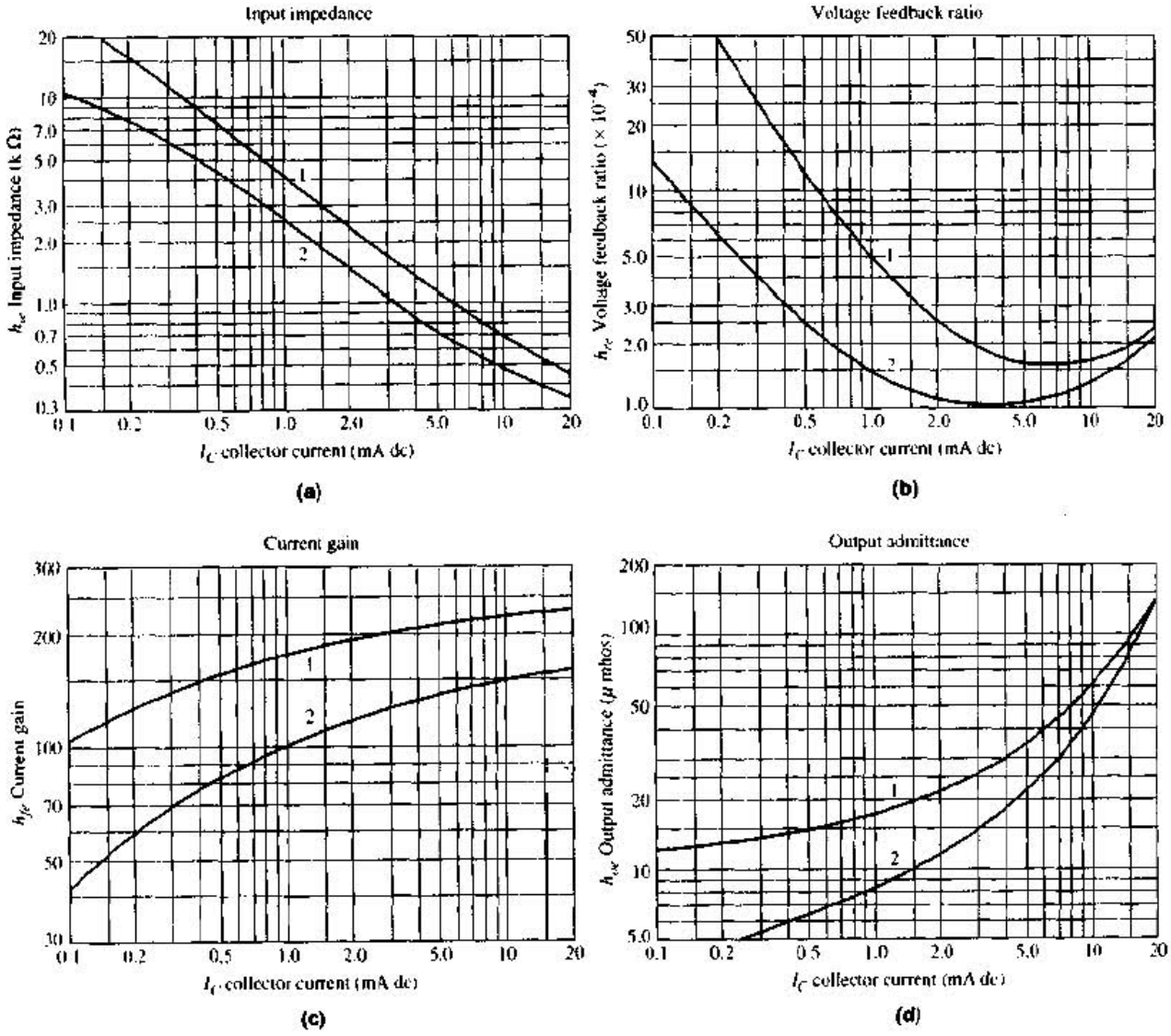


Figure 4.21 h-parameter data for the 2N2222A transistor. Curves 1 and 2 represent data from high-gain and low-gain transistors, respectively

between 2.5 and 5 kΩ. The voltage feedback ratio h_{re} varies between 1.5×10^{-4} and 5×10^{-4}, and the output admittance h_{oe} is in the range $8 < h_{oe} < 18$ μmhos.

Comment: The purpose of this example is to show that the parameters of a given transistor type can vary widely. In particular, the current gain parameter can easily vary by a factor of two. These variations are due to tolerances in the initial semiconductor properties and in the production process variables.

Design Pointer: This example clearly shows that there can be a wide variation in transistor parameters. Normally, a circuit is designed using nominal parameter values, but the allowable variations must be taken into account. In Chapter 3, we noted how a variation in β affects the Q-point. In this Chapter, we will see how the variations in small-signal parameters affect the small-signal voltage gain and other characteristics of a linear amplifier.

In the previous discussion, we indicated that the h-parameters h_{ie} and $1/h_{oe}$ are essentially equivalent to the hybrid-π parameters r_π and r_o, respectively, and that h_{fe} is essentially equal to β. The transistor circuit response is independent of the transistor model used. This reinforces the concept of a relationship between hybrid-π parameters and h-parameters. In fact, this is true for any set of small-signal parameters; that is, any given set of small-signal parameters is related to any other set of parameters.

Data Sheet

In the previous example, we showed some data for the 2N2222 discrete transistor. Figure 4.22 shows additional data from the data sheet for this transistor. Data sheets contain a lot of information, but we can begin to discuss some of the data at this time.

The first set of parameters pertains to the transistor in cutoff. The first two parameters listed are $V_{(BR)CEO}$ and $V_{(BR)CBO}$, which are the collector–emitter breakdown voltage with the base terminal open and the collector–base breakdown voltage with the emitter open. These parameters were discussed in Section 3.1.6 in the last chapter. In that section, we argued that $V_{(BR)CBO}$ was larger than $V_{(BR)CEO}$, which is supported by the data shown. These two voltages are measured at a specific current in the breakdown region. The third parameter, $V_{(BR)EBO}$, is the emitter–base breakdown voltage, which is substantially less than the collector–base or collector–emitter breakdown voltages.

The current I_{CBO} is the reverse-biased collector–base junction current with the emitter open ($I_E = 0$). This parameter was also discussed in Section 3.1.6. In the data sheet, this current is measured at two values of collector–base voltage and at two temperatures. The reverse-biased current increases with increasing temperature, as we would expect. The current I_{EBO} is the reverse-biased emitter–base junction current with the collector open ($I_C = 0$). This current is also measured at a specific reverse-bias voltage. The other two current parameters, I_{CEX} and I_{BL}, are the collector current and base current measured at given specific cutoff voltages.

The next set of parameters applies to the transistor when it is turned on. As was shown in Example 4.3, the data sheets give the h-parameters of the transistor. The first parameter, h_{FE}, is the dc common-emitter current gain and is

measured over a wide range of collector current. We discussed, in Section 3.4.2, stabilizing the Q-point against variations in current gain. The data presented in the data sheet show that the current gain for a given transistor can vary significantly, so that stabilizing the Q-point is indeed an important issue.

We have used V_{CE}(sat) as one of the piecewise linear parameters when a transistor is driven into saturation and have always assumed a particular value in our analysis or design. This parameter, listed in the data sheet, is not a constant but varies with collector current. If the collector becomes relatively large, then the collector–emitter saturation voltage also becomes relatively large. The larger V_{CE}(sat) value would need to be taken into account in large-current situations. The base–emitter voltage for a transistor driven into saturation, V_{BE}(sat), is also given. Up to this point in the text, we have not been concerned with this parameter; however, the data sheet shows that the base–emitter voltage can increase significantly when a transistor is driven into saturation at high current levels.

The other parameters listed in the data sheet become more applicable later in the text when the frequency response of transistors is discussed. The intent of this short discussion is to show that we can begin to read through data sheets even though there are a lot of data presented.

4.3 BASIC TRANSISTOR AMPLIFIER CONFIGURATIONS

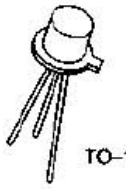
As we have seen, the bipolar transistor is a three-terminal device. Three basic single-transistor amplifier configurations can be formed, depending on which of the three transistor terminals is used as signal ground. These three basic configurations are appropriately called **common emitter**, **common collector (emitter follower)**, and **common base**. Which configuration or amplifier is used in a particular application depends to some extent on whether the input signal is a voltage or current and whether the desired output signal is a voltage or current. The characteristics of the three types of amplifiers will be determined to show the conditions under which each amplifier is most useful.

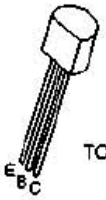
The input signal source can be modeled as either a Thevenin or Norton equivalent circuit. Figure 4.23(a) shows the Thevenin equivalent source that would represent a voltage signal, such as the output of a microphone. The voltage source v_s represents the voltage generated by the microphone. The resistance R_S is called the output resistance of the source and takes into account the change in output voltage as the source supplies current. Figure 4.23(b) shows the Norton equivalent source that would represent a current signal, such as the output of a photodiode. The current source i_s represents the current generated by the photodiode and the resistance R_S is the output resistance of this signal source.

Each of the three basic transistor amplifiers can be modeled as a two-port network in one of four configurations as shown in Table 4.3. We will determine the gain parameters, such as A_{vo}, A_{io}, G_{mo}, and R_{mo}, for each of the three transistor amplifiers. These parameters are important since they determine the amplification of the amplifier. However, we will see that the input and output resistances, R_i and R_o, are also important in the design of these amplifiers. Although one configuration shown in Table 4.3 may be preferable for a given application, any one of the four can be used to model a given amplifier. Since each configuration must produce the same terminal characteristics for a

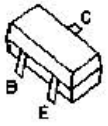
National Semiconductor

2N2222 2N2222A **PN2222 PN2222A** **MMBT2222 MMBT2222A** **MPQ2222**


TO–18



TO–92



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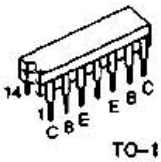


TO–116

NPN General Purpose Amplifier

Electrical Characteristics T_A = 25 °C unless otherwise noted

Symbol	Parameter		Min	Max	Units
OFF CHARACTERISTICS					
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage (Note 1) (I_C = 10 mA, I_B = 0)	2222 2222A	30 40		V
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage (I_C = 10 μA, I_E = 0)	2222 2222A	60 75		V
$V_{(BR)EBO}$	Emitter Base Breakdown Voltage (I_E = 10 μA, I_C = 0)	2222 2222A	5.0 6.0		V
I_{CEX}	Collector Cutoff Current (V_{CE} = 60 V, $V_{EB(off)}$ = 3.0 V)	2222A		10	nA
I_{CBO}	Collector Cutoff Current (V_{CB} = 50 V, I_E = 0) (V_{CB} = 60 V, I_E = 0) (V_{CB} = 50 V, I_E = 0, T_A = 150 °C) (V_{CB} = 60 V, I_E = 0, T_A = 150 °C)	2222 2222A 2222 2222A		0.01 0.01 10 10	μA
I_{EBO}	Emitter Cutoff Current (V_{EB} = 3.0 V, I_C = 0)	2222A		10	nA
I_{BL}	Base Cutoff Current (V_{CE} = 60 V, $V_{EB(off)}$ = 3.0)	2222A		20	nA
ON CHARACTERISTICS					
h_{FE}	DC Current Gain (I_C = 0.1 mA, V_{CE} = 10 V) (I_C = 1.0 mA, V_{CE} = 10 V) (I_C = 10 mA, V_{CE} = 10 V) (I_C = 10 mA, V_{CE} = 10 V, T_A = −55 °C) (I_C = 150 mA, V_{CE} = 10 V) (Note 1) (I_C = 150 mA, V_{CE} = 1.0 V) (Note 1) (I_C = 500 mA, V_{CE} = 10 V) (Note 1)	 2222 2222A	35 50 75 35 100 50 30 40	300	

Note 1: Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

Figure 4.22 Basic data sheet for the 2N2222 bipolar transistor

2222/PN2222/MMBT2222/MPQ2222/2N2222A/PN2222A/MMBT2222A NPN General Purpose Amplifier

NPN General Purpose Amplifier (Continued)

Electrical Characteristics T_A = 25 °C unless otherwise noted (Continued)

Symbol	Parameter		Min	Max	Units
ON CHARACTERISTICS (Continued)					
V_{CE} (sat)	Collector-Emitter Saturation Voltage (Note 1)				
	(I_C = 150 mA, I_B = 15 mA)	2222		0.4	V
		2222A		0.3	
	(I_C = 500 mA, I_B = 50 mA)	2222		1.6	
		2222A		1.0	
V_{BE} (sat)	Base-Emitter Saturation Voltage (Note 1)				
	(I_C = 150 mA, I_B = 15 mA)	2222	0.6	1.3	V
		2222A	0.6	1.2	
	(I_C = 500 mA, I_B = 50 mA)	2222		2.6	
		2222A		2.0	
SMALL-SIGNAL CHARACTERISTICS					
f_T	Current Gain—Bandwidth Product (Note 3)				
	(I_C = 20 mA, V_{CE} = 20 V, f = 100 MHz)	2222	250		MHz
		2222A	300		
C_{obo}	Output Capacitance (Note 3)				
	(V_{CB} = 10 V, I_E = 0, f = 100kHz)			8.0	pF
C_{ibo}	Input Capacitance (Note 3)				
	(V_{EB} = 0.5 V, I_C = 0, f = 100 kHz)	2222		30	pF
		2222A		25	
$r_b'C_C$	Collector Base Time Constant				
	(I_E = 20 mA, V_{CB} = 20 V, f = 31.8 MHz)	2222A		150	ps
NF	Noise Figure				
	(I_C = 100 μA, V_{CE} = 10V, R_S = 1.0 kΩ, f = 1.0 kHz)	2222A		4.0	dB
$Re(h_{ie})$	Real Part of Common-Emitter				
	High Frequency Input Impedance				
	(I_C = 20 mA, V_{CE} = 20 V, f = 300 MHz)			60	Ω
SWITCHING CHARACTERISTICS					
t_D	Delay Time	(V_{CC} = 30 V, V_{BE}(off) = 0.5 V, I_C = 150 mA, I_{B1} = 15 mA) except MPQ2222		10	ns
t_R	Rise Time			25	ns
t_S	Storage Time	(V_{CC} = 30 V, I_C = 150 mA, I_{B1} = I_{B2} = 15 mA) except MPQ2222		225	ns
t_F	Fall Time			60	ns

Note 1: Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

Note 2: For characteristics curves, see Process 19

Note 3: f_T is defined as the frequency at which h_{fe} extrapolates to unity.

Figure 4.22 Continued

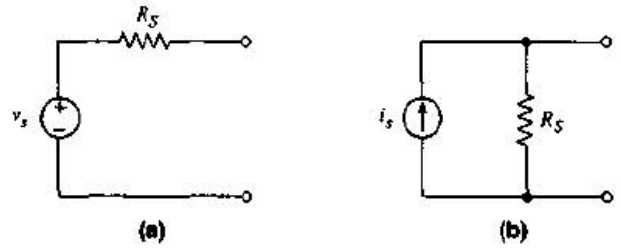
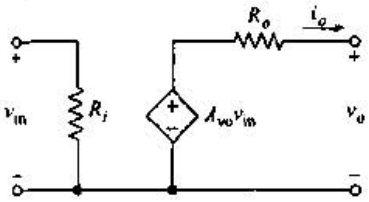
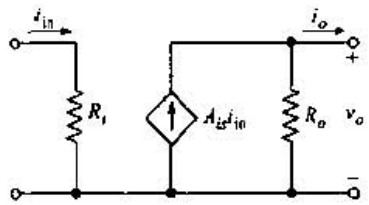
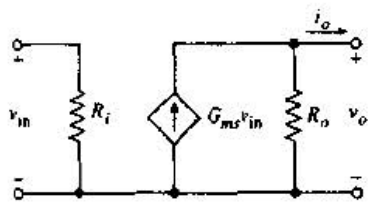
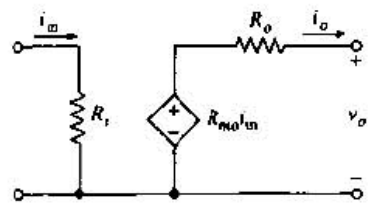


Figure 4.23 Input signal source modeled as (a) Thevenin equivalent circuit and (b) Norton equivalent circuit

Table 4.3 Four equivalent two-port networks

Type	Equivalent circuit	Gain property
Voltage amplifier		Output voltage proportional to input voltage
Current amplifier		Output current proportional to input current
Transconductance amplifier		Output current proportional to input voltage
Transresistance amplifier		Output voltage proportional to input current

given amplifier, the various gain parameters are not independent, but are related to each other.

If we wish to design a voltage amplifier (preamp) so that the output voltage of a microphone, for example, is amplified, the total equivalent circuit may be that shown in Figure 4.24. The input voltage to the amplifier is given by

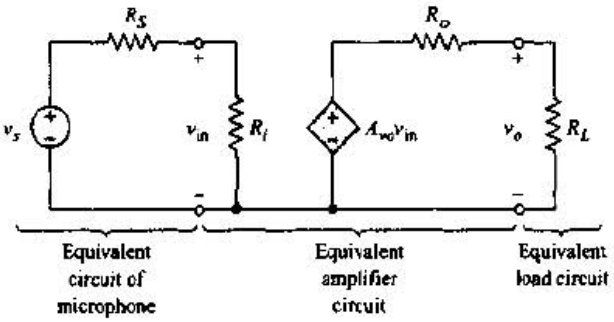


Figure 4.24 Equivalent preamplifier circuit

$$v_{in} = \frac{R_i}{R_i + R_S} \cdot v_s \tag{4.42}$$

In general, we would like the input voltage v_{in} to the amplifier to be as nearly equal to the source voltage v_s as possible. This means, from Equation (4.42), that we need to design the amplifier such that the input resistance R_i is much larger than the signal source output resistance R_S. (The output resistance of an ideal voltage source is zero, but is not zero for most practical voltage sources.) To provide a particular voltage gain, the amplifier must have a gain parameter A_{vo} of a certain value. The output voltage supplied to the load (where the load may be a second power amplifier stage) is given by

$$v_o = \frac{R_L}{R_L + R_o} \cdot A_{vo} v_{in} \tag{4.43}$$

Normally, we would like the output voltage to the load to be equal to the Thevenin equivalent voltage generated by the amplifier. This means that we need $R_o \ll R_L$ for the voltage amplifier. So again, for a voltage amplifier, the output resistance should be very small. The input and output resistances are significant in the design of an amplifier.

For a current amplifier, we would like to have $R_i \ll R_S$ and $R_o \gg R_L$. We will see as we proceed through the chapter that each of the three basic transistor amplifier configurations exhibits characteristics that are desirable for particular applications.

We should note that, in this chapter, we will be primarily using the two-port equivalent circuits shown in Table 4.3 to model single-transistor amplifiers. However, these equivalent circuits are also used to model multitransistor circuits. This will become apparent as we get into Part II of the text.

4.4 COMMON-EMITTER AMPLIFIERS

In this section, we consider the first of the three basic amplifiers—the **common-emitter** circuit. We will apply the equivalent circuit of the bipolar transistor that was previously developed. In general, we will use the hybrid-π model throughout the text.

4.4.1 Basic Common-Emitter Amplifier Circuit

Figure 4.25 shows the basic common-emitter circuit with voltage-divider biasing. We see that the emitter is at ground potential—hence the name common emitter. The signal from the signal source is coupled into the base of the transistor through the coupling capacitor C_C, which provides dc isolation between the amplifier and the signal source. The dc transistor biasing is established by R_1 and R_2, and is not disturbed when the signal source is capacitively coupled to the amplifier.

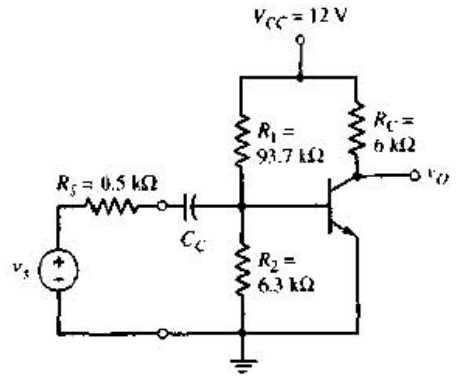


Figure 4.25 A common-emitter circuit with a voltage-divider biasing circuit and a coupling capacitor

If the signal source is a sinusoidal voltage at frequency f, then the magnitude of the capacitor impedance is $|Z_c| = [1/(2\pi f C_C)]$. For example, assume that $C_C = 10\,\mu\text{F}$ and $f = 2\,\text{kHz}$. The magnitude of the capacitor impedance is then

$$|Z_c| = \frac{1}{2\pi f C_C} = \frac{1}{2\pi(2 \times 10^3)(10 \times 10^{-6})} \cong 8\,\Omega \tag{4.44}$$

The magnitude of this impedance is much less than the Thevenin resistance at the capacitor terminals, which in this case is $R_1 \| R_2 \| r_\pi$. We can therefore assume that the capacitor is essentially a short circuit to signals with frequencies greater than 2 kHz. We are also neglecting any capacitance effects within the transistor. Using these results, our analyses in this chapter assume that the signal frequency is sufficiently high that any coupling capacitance acts as a perfect short circuit, and is also sufficiently low that the transistor capacitances can be neglected. Such frequencies are in the midfrequency range, or simply at the midband of the amplifier.

The small-signal equivalent circuit in which the coupling capacitor is assumed to be a short circuit is shown in Figure 4.26. The small-signal variables, such as the input signal voltage and input base current, are given in phasor form. The control voltage V_π is also given as a phasor.

Example 4.4 **Objective:** Determine the small-signal voltage gain of the circuit shown in Figure 4.25.

Assume the transistor parameters are: $\beta = 100$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, and $V_A = 100\,\text{V}$.

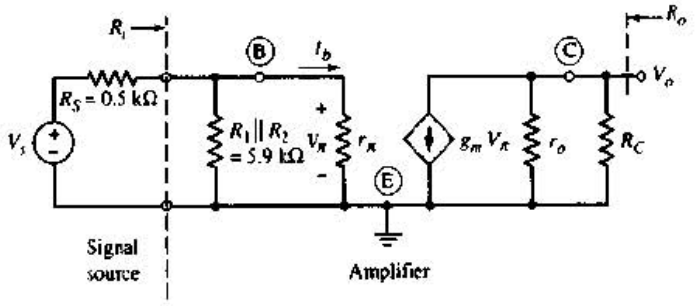


Figure 4.26 The small-signal equivalent circuit, assuming the coupling capacitor is a short circuit

DC Solution: We first do a dc analysis to find the Q-point values. We find that $I_{CQ} = 0.95\,\text{mA}$ and $V_{CEQ} = 6.31\,\text{V}$, which shows that the transistor is biased in the forward-active mode.

AC Solution: The small-signal hybrid-π parameters for the equivalent circuit are

$$r_\pi = \frac{V_T \beta}{I_{CQ}} = \frac{(0.026)(100)}{(0.95)} = 2.74\,\text{k}\Omega$$

$$g_m = \frac{I_{CQ}}{V_T} = \frac{0.95}{0.026} = 36.5\,\text{mA/V}$$

and

$$r_o = \frac{V_A}{I_{CQ}} = \frac{100}{0.95} = 105\,\text{k}\Omega$$

Assuming that C_C acts as a short circuit, Figure 4.26 shows the small-signal equivalent circuit. The small-signal output voltage is

$$V_o = -(g_m V_\pi)(r_o \| R_C)$$

The dependent current $g_m V_\pi$ flows through the parallel combination of r_o and R_C, but in a direction that produces a negative output voltage. We can relate the control voltage V_π to the input voltage V_s by a voltage divider. We have

$$V_\pi = \left(\frac{R_1 \| R_2 \| r_\pi}{R_1 \| R_2 \| r_\pi + R_S}\right) \cdot V_s$$

We can then write the small-signal voltage gain as

$$A_v = \frac{V_o}{V_s} = -g_m \left(\frac{R_1 \| R_2 \| r_\pi}{R_1 \| R_2 \| r_\pi + R_S}\right)(r_o \| R_C)$$

or

$$A_v = -(36.5)\left(\frac{5.9 \| 2.74}{5.9 \| 2.74 + 0.5}\right)(105 \| 6) = -163$$

We can also calculate R_i, which is the input resistance to the amplifier. From Figure 4.26, we see that

$$R_i = R_1 \| R_2 \| r_\pi = 5.9 \| 2.74 = 1.87\,\text{k}\Omega$$

The output resistance R_o is found by setting the independent source V_s equal to zero. In this case, there is no excitation to the input portion of the circuit so $V_\pi = 0$, which implies that $g_m V_\pi = 0$ (an open circuit). The output resistance looking back into the output terminals is then

$$R_o = r_o \| R_C = 105 \| 6 = 5.68\,\text{k}\Omega$$

Comment: In this circuit, the effective series resistance between the voltage source V_s and the base of the transistor is much less than that given in Example 4.1. For this reason, the magnitude of the voltage gain for the circuit given in Figure 4.25 is much larger than that found in Example 4.1.

Discussion: The two-port equivalent circuit along with the input signal source for the common-emitter amplifier analyzed in this example is shown in Figure 4.27. We can determine the effect of the source resistance R_S in conjunction with the amplifier input resistance R_i. Using a voltage-divider equation, we find the input voltage to the amplifier is

$$V_{in} = \left(\frac{R_i}{R_i + R_S}\right)V_s = \left(\frac{1.87}{1.87 + 0.5}\right)V_s = 0.789V_s$$

Because the input resistance to the amplifier is not very much greater than the signal source resistance, the actual input voltage to the amplifier is reduced to approximately 80 percent of the signal voltage. This is called a **loading effect**. The voltage V_{in} is a function of the amplifier connected to the source. In other amplifier designs, we will try to minimize the loading effect, or make $R_i \gg R_S$, which means that $V_{in} \cong V_s$.

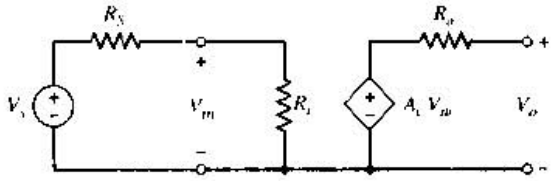


Figure 4.27 Two-port equivalent circuit for the amplifier in Example 4.4

4.4.2 Circuit with Emitter Resistor

For the circuit in Figure 4.25, the bias resistors R_1 and R_2 in conjunction with V_{CC} produce a base current of 9.5 μA and a collector current of 0.95 mA, when the B–E turn-on voltage is assumed to be 0.7 V. If the transistor in the circuit is replaced by a new one with slightly different parameters so that the B–E turn-on voltage is 0.6 V instead of 0.7 V, then the resulting base current is 26 μA, which is sufficient to drive the transistor into saturation. Therefore, the circuit shown in Figure 4.25 is not practical. An improved dc biasing design includes an emitter resistor.

In the last chapter, we found that the Q-point was stabilized against variations in β if an emitter resistor were included in the circuit, as shown in Figure 4.28. We will find a similar property for the ac signals, in that the voltage gain of a circuit with R_E will be less dependent on the transistor current gain β. Even though the emitter of this circuit is not at ground potential, this circuit is still referred to as a common-emitter circuit.

Assuming that C_C acts as a short circuit, Figure 4.29 shows the small-signal hybrid-π equivalent circuit. In this case, we are using the equivalent circuit with the current gain parameter β, and we are assuming that the Early voltage is infinite so the transistor output resistance r_o can be neglected (an open circuit). The ac output voltage is

$$V_o = -(\beta I_b)R_C \tag{4.45}$$

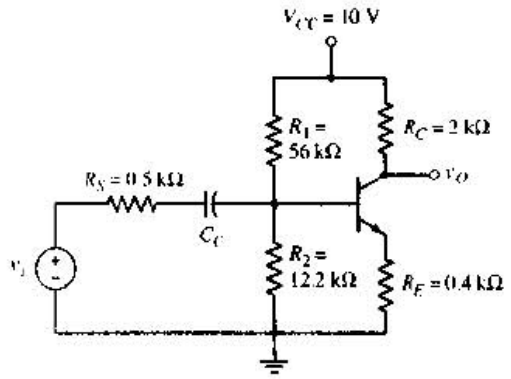


Figure 4.28 A bipolar circuit with an emitter resistor, a voltage-divider biasing circuit, and a coupling capacitor

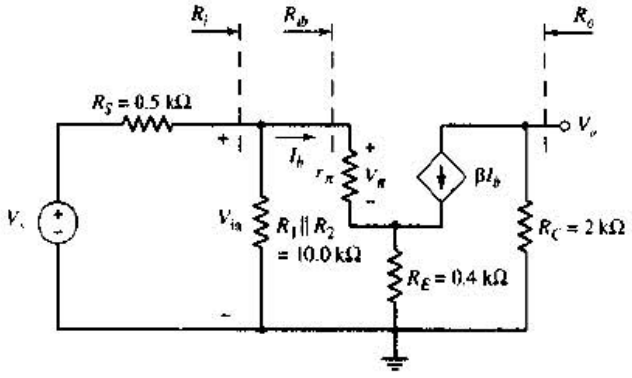


Figure 4.29 The small-signal equivalent circuit with an emitter resistor

To find the small-signal voltage gain, it is worthwhile finding the input resistance first. The resistance R_{ib} is the input resistance looking into the base of the transistor. We can write the following loop equation

$$V_{in} = I_b r_\pi + (I_b + \beta I_b) R_E \tag{4.46}$$

The input resistance R_{ib} is then defined as, and found to be,

$$R_{ib} = \frac{V_{in}}{I_b} = r_\pi + (1 + \beta) R_E \tag{4.47}$$

In the common-emitter configuration that includes an emitter resistance, the small-signal input resistance looking into the base of the transistor is r_π plus the emitter resistance multiplied by the factor $(1 + \beta)$. This effect is called the **resistance reflection rule**. We will use this result throughout the text without further derivation.

The input resistance to the amplifier is now

$$R_i = R_1 \| R_2 \| R_{ib} \tag{4.48}$$

We can again relate V_{in} to V_s through a voltage-divider equation as

$$V_{in} = \left(\frac{R_i}{R_i + R_S} \right) \cdot V_s \tag{4.49}$$

Combining Equations (4.45), (4.47), and (4.49), we find the small-signal voltage gain is

$$A_v = \frac{V_o}{V_s} = \frac{-(\beta I_b) R_C}{V_s} = -\beta R_C \left(\frac{V_{in}}{R_{ib}} \right) \cdot \left(\frac{1}{V_s} \right) \tag{4.50(a)}$$

or

$$A_v = \frac{-\beta R_C}{r_\pi + (1 + \beta) R_E} \left(\frac{R_i}{R_i + R_S} \right) \tag{4.50(b)}$$

From this equation, we see that if $R_i \gg R_S$ and if $(1 + \beta) R_E \gg r_\pi$, then the small-signal voltage gain is approximately

$$A_v \cong \frac{-\beta R_C}{(1 + \beta) R_E} \cong \frac{-R_C}{R_E} \tag{4.51}$$

Equations (4.50(b)) and (4.51) show that the voltage gain is less dependent on the current gain β than in the previous example, which means that there is a smaller change in voltage gain when the transistor current gain changes. The circuit designer now has more control in the design of the voltage gain, but this advantage is at the expense of a smaller gain.

In Chapter 3, we discussed the variation in the Q-point with variations or tolerances in resistor values. Since the voltage gain is a function of resistor values, it is also a function of the tolerances in those values. This must be considered in a circuit design.

Example 4.5 **Objective:** Determine the small-signal voltage gain of a common-emitter circuit with an emitter resistor.

For the circuit in Figure 4.28, the transistor parameters are: $\beta = 100$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, and $V_A = \infty$.

DC Solution: From a dc analysis of the circuit, we can determine that $I_{CQ} = 2.16\,\text{mA}$ and $V_{CEQ} = 4.81\,\text{V}$, which shows that the transistor is biased in the forward-active mode.

AC Solution: The small-signal hybrid-π parameters are determined to be

$$r_\pi = \frac{V_T \beta}{I_{CQ}} = \frac{(0.026)(100)}{(2.16)} = 1.20\,\text{k}\Omega$$

$$g_m = \frac{I_{CQ}}{V_T} = \frac{2.16}{0.026} = 83.1\,\text{mA/V}$$

and

$$r_o = \frac{V_A}{I_{CQ}} = \infty$$

The input resistance to the base can be determined as

$$R_{ib} = r_\pi + (1+\beta)R_E = 1.20 + (101)(0.4) = 41.6\,\text{k}\Omega$$

and the input resistance to the amplifier is now found to be

$$R_i = R_1 \| R_2 \| R_{ib} = 10 \| 41.6 = 8.06\,\text{k}\Omega$$

Using the exact expression for the voltage gain, we find

$$A_v = \frac{-(100)(2)}{1.20 + (101)(0.4)}\left(\frac{8.06}{8.06 + 0.5}\right) = -4.53$$

If we use the approximation given by Equation (4.51), we obtain

$$A_v = \frac{-R_C}{R_E} = \frac{-2}{0.4} = -5.0$$

Comment: The magnitude of the small-signal voltage gain is substantially reduced when an emitter resistor is included. Also, Equation (4.51) gives a good first approximation for the gain, which means that it can be used in the initial design of a common-emitter circuit with an emitter resistor.

Discussion: The amplifier gain is nearly independent of changes in the current gain parameter β. This fact is shown in the following calculations:

β	A_v
50	−4.41
100	−4.53
150	−4.57

In addition to gaining an advantage in stability by including an emitter resistance, we also gain an advantage in the loading effect. We see that, for $\beta = 100$, the input voltage to the amplifier is

$$V_{in} = \left(\frac{R_i}{R_i + R_S}\right) \cdot V_s = (0.942)V_s$$

We see that V_{in} is much closer in value to V_s than in the previous example. There is less loading effect because the input resistance to the base of the transistor is higher when an emitter resistor is included.

The same equivalent circuit as shown in Figure 4.27 applies to this example also. The difference in the two examples is the values of input resistance and gain parameter.

Test Your Understanding

4.5 For the circuit in Figure 4.30, let $R_E = 0.6\,\text{k}\Omega$, $R_C = 5.6\,\text{k}\Omega$, $\beta = 120$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, $R_1 = 250\,\text{k}\Omega$, and $R_2 = 75\,\text{k}\Omega$. (a) For $V_s = \infty$, determine the small-signal voltage gain A_v. (b) Determine the input resistance looking into the base of the transistor. (Ans. (a) $A_v = -8.27$, (b) $R_{ib} = 80.1\,\text{k}\Omega$)

***D4.6** For the circuit shown in Figure 4.30, let $\beta = 100$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, and $V_A = \infty$. Design a bias-stable circuit such that $I_{CQ} = 0.5\,\text{mA}$, $V_{CEQ} = 2.5\,\text{V}$, and $A_v = -8$. (Ans. To a good approximation: $R_C = 4.54\,\text{k}\Omega$, $R_E = 0.454\,\text{k}\Omega$, $R_1 = 24.1\,\text{k}\Omega$, and $R_2 = 5.67\,\text{k}\Omega$)

4.7 Assume a 2N2907A transistor is used in the circuit in Figure 4.31 and that the nominal dc transistor parameters are $\beta = 100$ and $V_{EB}(\text{on}) = 0.7\,\text{V}$. Determine the small-voltage gain, using the h-parameter model of the transistor. Find the minimum and maximum values of gain corresponding to the minimum and maximum h-parameter values. See Appendix C. For simplicity, assume $h_{re} = h_{oe} = 0$. (Ans. $A_v = -2.54$ for both cases)

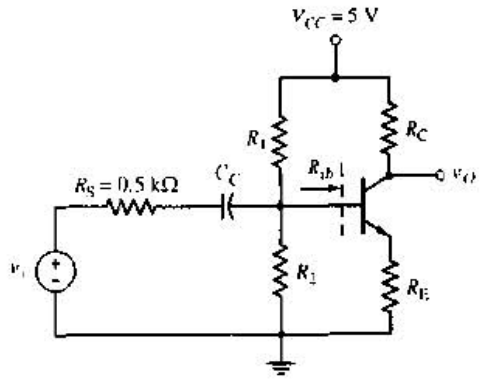


Figure 4.30 Figure for Exercises 4.5 and 4.6

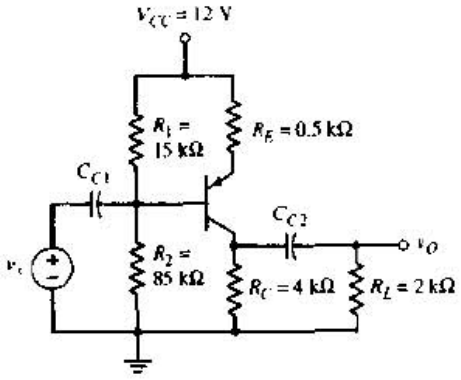


Figure 4.31 Figure for Exercise 4.7

4.4.3 Circuit with Emitter Bypass Capacitor

There may be times when the emitter resistor must be large for the purposes of dc design, but degrades the small-signal voltage gain too severely. We can use an emitter bypass capacitor to effectively short out a portion or all of the emitter resistance as seen by the ac signals. Consider the circuit shown in Figure 4.32 biased with both positive and negative voltages. Both emitter resistors R_{E1} and R_{E2} are factors in the dc design of the circuit, but only R_{E1} is part of the ac equivalent circuit, since C_E provides a short circuit to ground for the ac signals.

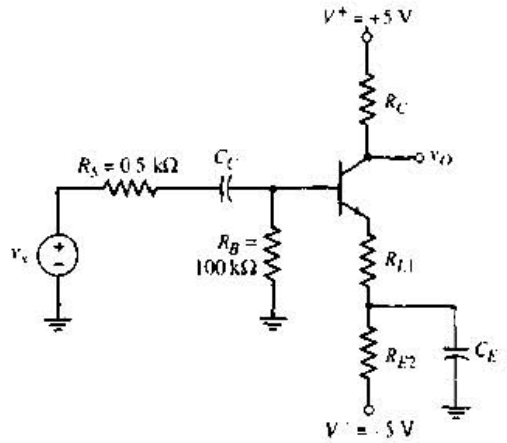


Figure 4.32 A bipolar circuit with an emitter resistor and an emitter bypass capacitor

Design Example 4.6 **Objective:** An amplifier with the configuration in Figure 4.32 is to be designed such that a 12 mV sinusoidal signal from a microphone is amplified to a 0.4 V sinusoidal output signal. Standard resistor values are to be used in the final design.

Initial Design Approach: The magnitude of the voltage gain of the amplifier needs to be

$$|A_v| = \frac{0.4\,\text{V}}{12\,\text{mV}} = 33.3$$

From Equation (4.51), the approximate voltage gain of the amplifier is

$$|A_v| \cong \frac{R_C}{R_{E1}}$$

Noting from the last example that this value of gain produces an optimistically high value, we can set $R_C/R_{E1} = 40$ or $R_C = 40R_{E1}$.

The dc base-emitter loop equation is

$$5 = I_B R_B + V_{BE}(\text{on}) + I_E(R_{E1} + R_{E2})$$

Assuming $\beta = 100$ and $V_{BE}(\text{on}) = 0.7$ V, we can design the circuit to produce a quiescent emitter current of, for example, 0.20 mA. We then have

$$5 = \frac{(0.20)}{(101)}(100) + 0.70 + (0.20)(R_{E1} + R_{E2})$$

which yields

$$R_{E1} + R_{E2} = 20.5\,\text{k}\Omega$$

Assuming $I_E \cong I_C$ and designing the circuit such that $V_{CEQ} = 4$ V, the collector–emitter loop equation produces

$$5 + 5 = I_C R_C + V_{CEQ} + I_E(R_{E1} + R_{E2}) = (0.2)R_C + 4 + (0.2)(20.5)$$

or

$$R_C = 9.5\,\text{k}\Omega$$

Then

$$R_{E1} = \frac{R_C}{40} = \frac{9.5}{40} = 0.238\,\text{k}\Omega$$

and $R_{E2} = 20.3\,\text{k}\Omega$.

From Appendix D, we can pick standard resistor values of $R_{E1} = 240\,\Omega$, $R_{E2} = 20\,\text{k}\Omega$, and $R_C = 10\,\text{k}\Omega$.

Computer Simulation: Since we used approximation techniques in our design, we can use PSpice to give us a more accurate evaluation of the circuit for the standard resistor values that were chosen. Figure 4.33 shows the PSpice circuit schematic.

Using the standard resistor values and the 2N3904 transistor, the output signal voltage produced by a 12 mV input signal is 323 mV. A frequency of 2 kHz and capacitor values of 100 μF were used in the simulation. The magnitude of the output signal is slightly less than the desired value of 400 mV. The principal reason for the difference is that the r_π parameter of the transistor was neglected in the design. For a collector current of approximately $I_C = 0.2$ mA, r_π can be significant.

In order to increase the small-signal voltage gain, a smaller value of R_{E1} is necessary. For $R_{E1} = 160\,\Omega$, the output signal voltage is 410 mV, which is very close to the desired value.

Design Pointer: Approximation techniques are extremely useful in an initial electronic circuit design. A computer simulation, such as PSpice, can then be used to verify the design. Slight changes in the design can then be made to meet the required specifications.

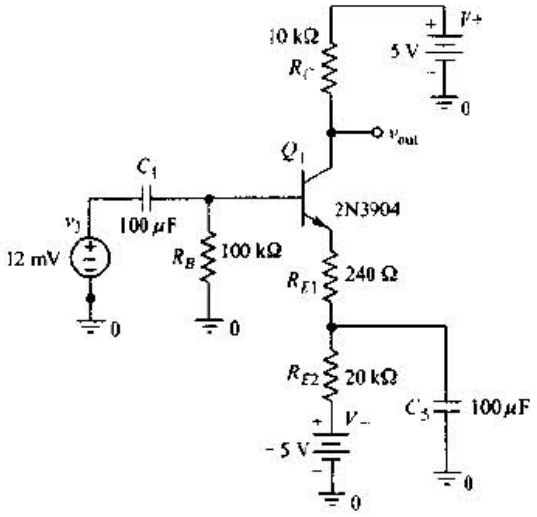


Figure 4.33 PSpice circuit schematic

Test Your Understanding

***D4.8** Design the circuit in Figure 4.34 such that it is bias stable and the small-signal voltage gain is $A_v = -8$. Let $I_{CQ} = 0.6\,\text{mA}$, $V_{ECQ} = 3.75\,\text{V}$, $\beta = 100$, $V_{EB}(\text{on}) = 0.7\,\text{V}$, and $V_A = \infty$. (Ans. To a good approximation: $R_C = 5.62\,\text{k}\Omega$, $R_E = 0.624\,\text{k}\Omega$, $R_1 = 7.40\,\text{k}\Omega$, and $R_2 = 42.4\,\text{k}\Omega$)

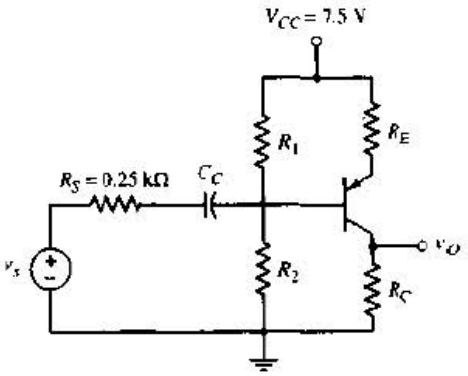


Figure 4.34 Figure for Exercise 4.8

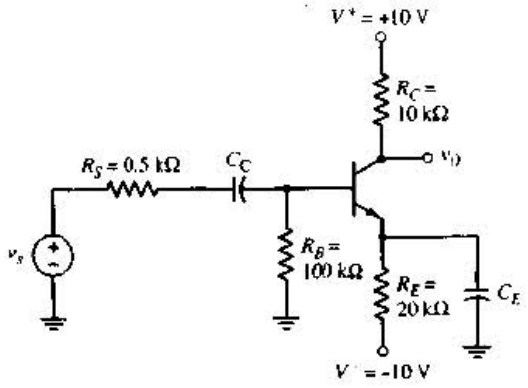


Figure 4.35 Figure for Exercise 4.9

4.9 For the circuit in Figure 4.35, let $\beta = 100$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, and $V_A = 100\,\text{V}$. (a) Determine the small-signal voltage gain. (b) Determine the input resistance seen by the signal source and the output resistance looking back into the output terminal. (Ans. (a) $A_v = -148$ (b) $R_{in} = 6.09\,\text{k}\Omega$, $R_o = 9.58\,\text{k}\Omega$)

4.10 For the circuit in Figure 4.28, the small-signal voltage gain is given approximately by $-R_C/R_E$. For the case of $R_C = 2\,\text{k}\Omega$, $R_E = 0.4\,\text{k}\Omega$, and $R_S = 0$, what must be the value of β such that the approximate value is within 5 percent of the actual value? (Ans. $\beta = 76$)

4.11 For the circuit in Figure 4.36, let $\beta = 125$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, and $V_A = 200\,\text{V}$. (a) Determine the small-signal voltage gain A_v. (b) Determine the output resistance R_o. (Ans. (a) $A_v = -50.5$ (b) $R_o = 2.28\,\text{k}\Omega$)

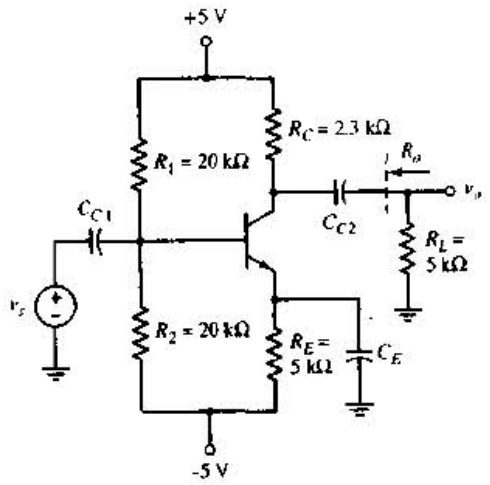


Figure 4.36 Figure for Exercise 4.11

4.4.4 Advanced Common-Emitter Amplifier Concepts

Our previous analysis of common-emitter circuits assumed constant load or collector resistances. The common-emitter circuit shown in Figure 4.37(a) is biased with a constant-current source and contains a nonlinear, rather than a constant, collector resistor. Assume the current–voltage characteristics of the nonlinear resistor are described by the curve in Figure 4.37(b). Neglecting base currents, assume that the collector resistor is biased at I_Q and V_{RQ}. At the Q-point of the resistor, assume the incremental resistance $\Delta v_R/\Delta i_C$ is r_c.

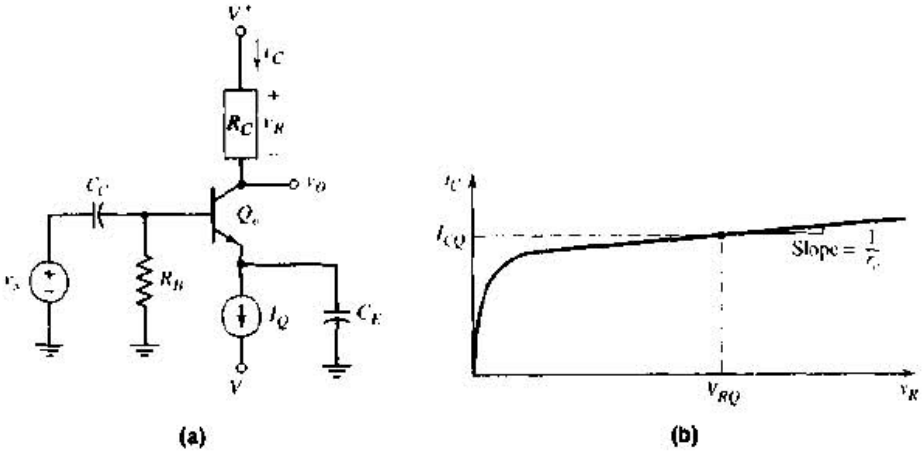


Figure 4.37 (a) A common-emitter circuit with current source biasing and a nonlinear load resistor and (b) current–voltage characteristics of the nonlinear load resistor

The small-signal equivalent circuit of the common-emitter amplifier circuit in Figure 4.37(a) is shown in Figure 4.38. The collector resistor R_C is replaced by the small-signal equivalent resistance r_c that exists at the Q-point. The small-signal voltage gain is then, assuming an ideal voltage signal source,

$$A_v = \frac{V_o}{V_s} = -g_m(r_o \| r_c) \tag{4.52}$$

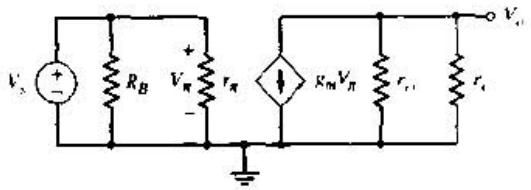


Figure 4.38 Small-signal equivalent circuit of the circuit in Figure 4.37(a)

Example 4.7 **Objective:** Determine the small-signal voltage gain of a common-emitter circuit with a nonlinear load resistance.

Assume the circuit shown in Figure 4.37(a) is biased at $I_Q = 0.5\text{mA}$, and the transistor parameters are $\beta = 120$ and $V_A = 80\text{V}$. Also assume that nonlinear small-signal collector resistance is $r_c = 120\text{k}\Omega$.

Solution: For a transistor current gain of $\beta = 120$, $I_{CQ} \cong I_{EQ} = I_Q$, and the small-signal hybrid-π parameters are

$$g_m = \frac{I_{CQ}}{V_T} = \frac{0.5}{0.026} = 19.2 \text{ mA/V}$$

and

$$r_o = \frac{V_A}{I_{CQ}} = \frac{80}{0.5} = 160 \text{ k}\Omega$$

The small-signal voltage gain is therefore

$$A_v = -g_m(r_o \| r_c) = -(19.2)(160 \| 120) = -1317$$

Comment: As we will see in Part II of this text, the nonlinear resistor R_C is produced by the I–V characteristics of another bipolar transistor. Because the resulting effective load resistance is large, a very large small-signal voltage gain is produced. A large effective load resistance r_c means that the output resistance r_o of the amplifying transistor cannot be neglected; therefore, the loading effects must be taken into account.

4.5 AC LOAD LINE ANALYSIS

A dc load line gives us a way of visualizing the relationship between the Q-point and the transistor characteristics. When capacitors are included in a transistor circuit, a new effective load line, called an **ac load line**, may exist. The ac load line helps in visualizing the relationship between the small-signal response and the transistor characteristics. The ac operating region is on the ac load line.

4.5.1 AC Load Line

The circuit in Figure 4.33 has emitter resistors and an emitter bypass capacitor. The dc load line is found by writing a Kirchhoff voltage law (KVL) equation around the collector–emitter loop, as follows:

$$V^+ = I_C R_C + V_{CE} + I_E(R_{E1} + R_{E2}) + V^- \tag{4.53}$$

Noting that $I_E = [(1 + \beta)/\beta]I_C$, Equation (4.53) can be written as

$$V_{CE} = (V^+ - V^-) - I_C\left[R_C + \left(\frac{1+\beta}{\beta}\right)(R_{E1} + R_{E2})\right] \tag{4.54}$$

which is the equation of the dc load line. For the parameters and standard resistor values found in Example 4.6, the dc load line and the Q-point are plotted in Figure 4.39. If $\beta \gg 1$, then we can approximate $(1 + \beta)/\beta \cong 1$.

From the small-signal analysis in Example 4.6, the KVL equation around the collector–emitter loop is

$$i_c R_C + v_{ce} + i_e R_{E1} = 0 \tag{4.55(a)}$$

or, assuming $i_c \cong i_e$, then

$$v_{ce} = -i_c(R_C + R_{E1}) \tag{4.55(b)}$$