Figure 4.39 The dc and ac load lines for the circuit in Figure 4.33, and the signal responses to input signal

This equation is the ac load line. The slope is given by

$$\text{Slope} = \frac{-1}{R_C + R_{E1}}$$

The ac load line is shown in Figure 4.39. When $v_{ce} = i_c = 0$, we are at the Q-point. When ac signals are present, we deviate about the Q-point on the ac load line.

The slope of the ac load line differs from that of the dc load line because the emitter resistor is not included in the small-signal equivalent circuit. The small-signal C–E voltage and collector current response are functions of the resistor R_C and R_{E1} only.

Example 4.8 **Objective:** Determine the dc and ac load lines for the circuit shown in Figure 4.40.

Assume the transistor parameters are: $V_{EB}(\text{on}) = 0.7\,\text{V}$, $\beta = 150$, and $V_A = \infty$.

DC Solution: The dc load line is found by writing a KVL equation around the C–E loop, as follows:

$$V^+ = I_L R_E + V_{EC} + I_C R_C + V^-$$

The dc load line equation is then

$$V_{EC} = (V^+ - V^-) - I_C \left[R_C + \left(\frac{1+\beta}{\beta} \right) R_E \right]$$

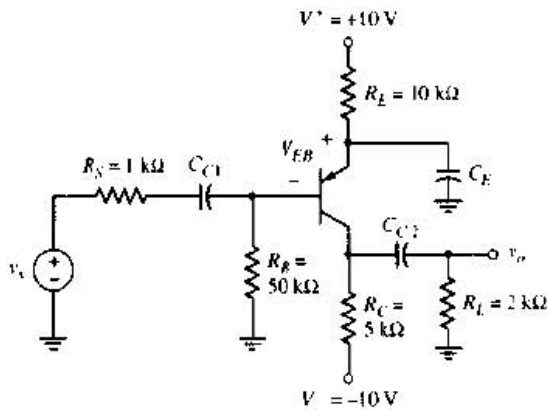Assuming that $(1 + \beta)/\beta \cong 1$, the dc load line is plotted in Figure 4.41.
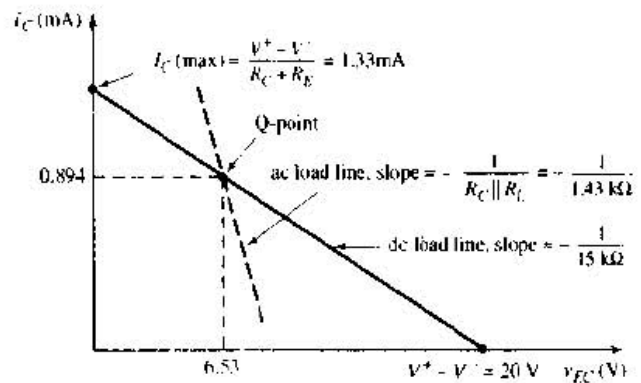
Figure 4.40 Circuit for Example 4.8

Figure 4.41 Plots of dc and ac load lines for Example 4.8

To determine the Q-point parameters, write a KVL equation around the B-E loop, as follows:

$$V^- = (1 + \beta)I_{BQ}R_E + V_{EB}(\text{on}) + I_{BQ}R_B$$

or

$$I_{BQ} = \frac{V^+ - V_{EB}(\text{on})}{R_B + (1 + \beta)R_E} = \frac{10 - 0.7}{50 + (151)(10)} \Rightarrow 5.96\,\mu\text{A}$$

Then,

$$I_{CQ} = \beta I_{BQ} = (150)(5.96\,\mu\text{A}) \Rightarrow 0.894\,\text{mA}$$
$$I_{EQ} = (1 + \beta)I_{BQ} = (151)(5.96\,\mu\text{A}) \Rightarrow 0.90\,\text{mA}$$

and

$$V_{ECQ} = (V^+ - V^-) - I_{CQ}R_C - I_{EQ}R_E$$
$$= [10 - (-10)] - (0.894)(5) - (0.90)(10) = 6.53\,\text{V}$$

The Q-point is also plotted in Figure 4.41.

AC Solution: Assuming that all capacitors act as short circuits, the small-signal equivalent circuit is shown in Figure 4.42. Note that the current directions and voltage polarities in the hybrid-π equivalent circuit of the pnp transistor are reversed compared to those of the npn device. The small-signal hybrid-π parameters are

$$r_\pi = \frac{V_T\beta}{I_{CQ}} = \frac{(0.026)(150)}{0.894} = 4.36\,\text{k}\Omega$$

$$g_m = \frac{I_{CQ}}{V_T} = \frac{0.894}{0.026} = 34.4\,\text{mA/V}$$
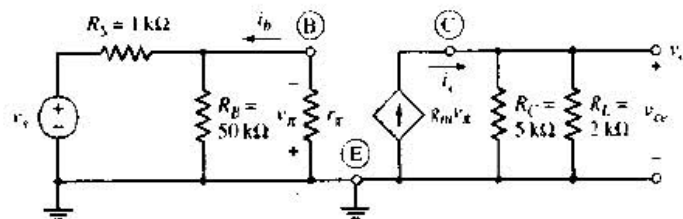

Figure 4.42 The small-signal equivalent circuit for Example 4.8

and

$$r_o = \frac{V_A}{I_{CQ}} = \frac{\infty}{I_{CQ}} = \infty$$

The small-signal output voltage, or C-E voltage, is

$$v_o = v_{ce} = +(g_m v_\pi)(R_C \| R_L)$$

where

$$g_m v_\pi = i_c$$

The ac load line, written in terms of the E-C voltage, is defined by

$$v_{ec} = -i_c(R_C \| R_L)$$

The ac load line is also plotted in Figure 4.41.

Comment: In the small-signal equivalent circuit, the large $10\,k\Omega$ emitter resistor is effectively shorted by the bypass capacitor C_E, the load resistor R_L is in parallel with R_C as a result of the coupling capacitor C_{C2}, so that the slope of the ac load line is substantially different than that of the dc load line.

4.5.2 Maximum Symmetrical Swing

When symmetrical sinusoidal signals are applied to the input of an amplifier, symmetrical sinusoidal signals are generated at the output, as long as the amplifier operation remains linear. We can use the ac load line to determine the **maximum output symmetrical swing**. If the output exceeds this limit, a portion of the output signal will be clipped and signal distortion will occur.

Example 4.9 Objective: Determine the maximum symmetrical swing in the output voltage of the circuit given in Figure 4.40.

Solution: The ac load line is given in Figure 4.41. The maximum negative swing in the collector current is from 0.894 mA to zero; therefore, the maximum possible symmetrical peak-to-peak ac collector current is

$$\Delta i_c = 2(0.894) = 1.79\,mA$$

The maximum symmetrical peak-to-peak output voltage is given by

$$|\Delta v_{ce}| = |\Delta i_c|(R_C \| R_L) = (1.79)(5\|2) = 2.56\,V$$

Therefore, the maximum instantaneous collector current is

$$i_C = I_{CQ} + \tfrac{1}{2}|\Delta i_c| = 0.894 + 0.894 = 1.79\,mA$$

Comment: Considering the Q-point and the maximum swing in the C-E voltage, the transistor remains biased in the forward-active region. Note that the maximum instantaneous collector current, 1.79 mA, is larger than the maximum dc collector current, 1.33 mA, as determined from the dc load line. This apparent anomaly is due to the different resistance in the C-E circuit for the ac signal and the dc signal.

Problem-Solving Technique: Maximum Symmetrical Swing

Again, since we are dealing with linear amplifier circuits, superposition applies so that we can add the dc and ac analysis results. To design a BJT amplifier for maximum symmetrical swing, we perform the following steps.

1. Write the dc load line equation that relates the quiescent values I_{CQ} and V_{CEQ}.

2. Write the ac load line equation that relates the ac values i_c and v_{ce}: $v_{ce} = -i_c R_{eq}$ where R_{eq} is the effective ac resistance in the collector-emitter circuit.

3. In general, we can write $i_c = I_{CQ} - I_C(\text{min})$, where $I_C(\text{min})$ is zero or some other specified minimum collector current.

4. In general, we can write $v_{ce} = V_{CEQ} - V_{CE}(\text{min})$, where $V_{CE}(\text{min})$ is some specified minimum collector-emitter voltage.

5. The above four equations can be combined to yield the optimum I_{CQ} and V_{CEQ} values to obtain the maximum symmetrical swing in the output signal.

Test Your Understanding

4.12 For the circuit in Figure 4.30, use the parameters given in Exercise 4.5. If the total instantaneous current must always be greater than 0.1 mA and the total instantaneous C-E voltage must be in the range $0.5 \leq v_{CE} \leq 5$V, determine the maximum symmetrical swing in the output voltage. (Ans. 3.82 V peak-to-peak)

4.13 Reconsider the circuit in Figure 4.31. Let $r_o = \infty$, $\beta = 120$, and $V_{EB}(\text{on}) = 0.7$V. (a) Plot the dc and ac load lines on the same graph. (b) Determine the maximum symmetrical swing in the output voltage, for $i_c > 0$ and $0.5 \leq v_{EC} \leq 12$V. (Ans. (b) 6.58V peak-to-peak)

*D4.14 For the circuit in Figure 4.35, assume the transistor parameters are: $\beta = 100$, $V_{BE}(\text{on}) = 0.7$V, and $V_A = \infty$. Determine a new value of R_E that will achieve a maximum symmetrical swing in the output voltage, for $i_c > 0$ and $0.7 \leq v_{CE} \leq 19.5$V. What is the maximum symmetrical swing that can be achieved? (Ans. $R_E = 16.4$kΩ, 10.6 V peak-to-peak)

4.15 For the circuit in Figure 4.36, let $\beta = 125$, $V_{BE}(\text{on}) = 0.7$V, and $V_A = 200$ V. (a) Plot the dc and ac load lines on the same graph. (b) Determine the maximum symmetrical swing in the output voltage for $i_c > 0$ and $0.5 \leq v_{CE} \leq 9.5$V. (Ans. (b) 2.66V)

*D4.16 For the circuit shown in Figure 4.43, let $\beta = 120$, $V_{EB}(\text{on}) = 0.7$V, and $r_o = \infty$. (a) Design a bias-stable circuit such that $I_{CQ} = 1.6$mA. Determine V_{ECQ}. (b) Determine the value of R_L that will produce the maximum symmetrical swing in the output voltage and collector current for $i_C \geq 0.1$ mA and $0.5 \leq v_{EC} \leq 11.5$V. (Ans. (a) $R_1 = 15.24$kΩ, $R_2 = 58.7$kΩ, $V_{ECQ} = 3.99$ V (b) $R_L = 5.56$kΩ)
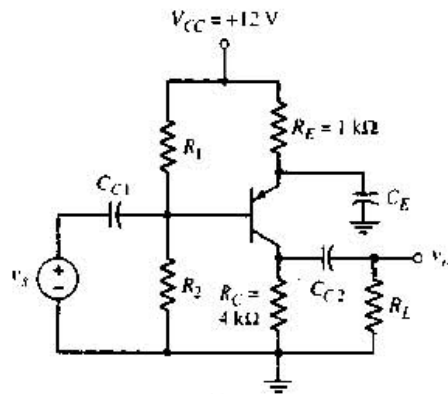
Figure 4.43 Figure for Exercise 4.16

4.6 COMMON-COLLECTOR (EMITTER-FOLLOWER) AMPLIFIER

The second type of transistor amplifier to be considered is the **common-collector circuit**. An example of this circuit configuration is shown in Figure 4.44. As seen in the figure, the output signal is taken off of the emitter with respect to ground and the collector is connected directly to V_{CC}. Since V_{CC} is at signal ground in the ac equivalent circuit, we have the name common-collector. The more common name for this circuit is **emitter follower**. The reason for this name will become apparent as we proceed through the analysis.

4.6.1 Small-Signal Voltage Gain

The dc analysis of the circuit is exactly the same as we have already seen, so we will concentrate on the small-signal analysis. The hybrid-π model of the bipolar transistor can also be used in the small-signal analysis of this circuit. Assuming the coupling capacitor C_C acts as a short circuit, Figure 4.45 shows the small-signal equivalent circuit of the circuit shown in Figure 4.44. The collector terminal is at signal ground and the transistor output resistance r_o is in parallel with the dependent current source.

Figure 4.46 shows the equivalent circuit rearranged so that all signal grounds are at the same point.
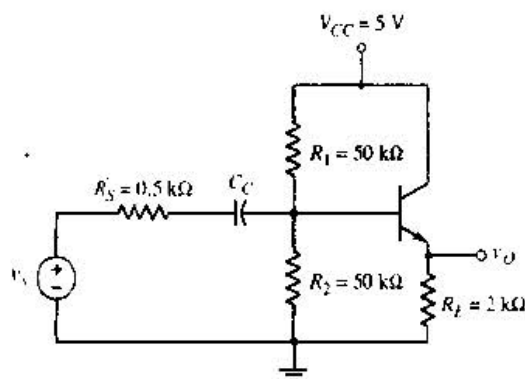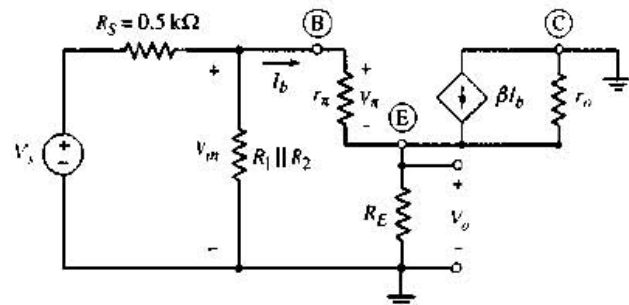

Figure 4.44 Emitter-follower circuit

Figure 4.45 Small-signal equivalent circuit of the emitter-follower
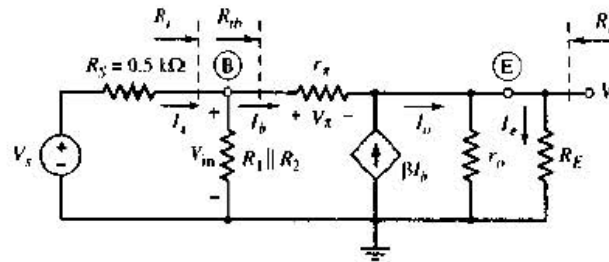
Figure 4.46 Another small-signal equivalent circuit for the emitter-follower

We see that

$$I_o = (1 + \beta)I_b \tag{4.56}$$

so the output voltage can be written as

$$V_o = I_b(1 + \beta)(r_o \| R_E) \tag{4.57}$$

Writing a KVL equation around the base-emitter loop, we obtain

$$V_{in} = I_b[r_\pi + (1 + \beta)(r_o \| R_E)] \tag{4.58(a)}$$

or

$$R_{ib} = \frac{V_{in}}{I_b} = r_\pi + (1 + \beta)(r_o \| R_E) \tag{4.58(b)}$$

We can also write

$$V_{in} = \left(\frac{R_i}{R_i + R_S} \right) \cdot V_s \tag{4.59}$$

where $R_i = R_1 \| R_2 \| R_{ib}$.

Combining Equations (4.57), (4.58(b)), and (4.59), the small-signal voltage gain is

$$A_v = \frac{V_o}{V_s} = \frac{(1 + \beta)(r_o \| R_E)}{r_\pi + (1 + \beta)(r_o \| R_E)} \cdot \left(\frac{R_i}{R_i + R_S} \right) \tag{4.60}$$

Example 4.10 **Objective:** Calculate the small-signal voltage gain of an emitter-follower circuit.

For the circuit shown in Figure 4.44, assume the transistor parameters are: $\beta = 100$, $V_{BE}(on) = 0.7\,V$, and $V_A = 80\,V$.

Solution: The dc analysis shows that $I_{CQ} = 0.793\,mA$ and $V_{CEQ} = 3.4\,V$. The small-signal hybrid-π parameters are determined to be

$$r_\pi = \frac{V_T \beta}{I_{CQ}} = \frac{(0.026)(100)}{0.793} = 3.28\,k\Omega$$

$$g_m = \frac{I_{CQ}}{V_T} = \frac{0.793}{0.026} = 30.5\,mA/V$$

and

$$r_o = \frac{V_A}{I_{CQ}} = \frac{80}{0.793} \cong 100\,k\Omega$$

We may note that

$$R_{ib} = 3.28 + (101)(100\|2) = 201\,k\Omega$$

and

$$R_i = 50\|50\|201 = 22.2\,k\Omega$$

The small-signal voltage gain is then

$$A_v = \frac{(101)(100\|2)}{3.28 + (101)(100\|2)} \cdot \left(\frac{22.2}{22.2 + 0.5}\right)$$

or

$$A_v = +0.962$$

Comment: The magnitude of the voltage gain is slightly less than 1. An examination of Equation (4.60) shows that this is always true. Also, the voltage gain is positive, which means that the output signal voltage at the emitter is in phase with the input signal voltage. The reason for the terminology emitter-follower is now clear. The output voltage at the emitter is essentially equal to the input voltage.

At first glance, a transistor amplifier with a voltage gain essentially of 1 may not seem to be of much value. However, the input and output resistance characteristics make this circuit extremely useful in many applications, as we will show in the next section.

4.6.2 Input and Output Impedance

The input impedance, or small-signal input resistance, of the emitter-follower is determined in the same manner as for the common-emitter circuit. For the circuit in Figure 4.44, the input resistance looking into the base is denoted R_{ib} and is indicated in the small-signal equivalent circuit shown in Figure 4.46.

The input resistance R_{ib} was given by Equation (4.58(b)) as

$$R_{ib} = r_\pi + (1 + \beta)(r_o \| R_E) \tag{4.58(b)}$$

Since the emitter current is $(1 + \beta)$ times the base current, the effective impedance in the emitter is multiplied by $(1 + \beta)$. We saw this same effect when an emitter resistor was included in a common-emitter circuit. This multiplication by $(1 + \beta)$ is again called the resistance reflection rule. The input resistance at the base is r_π plus the effective resistance in the emitter multiplied by the $(1 + \beta)$ factor. This resistance reflection rule will be used extensively throughout the remainder of the text.

The circuit in Figure 4.47 can be used to determine the output resistance of the emitter-follower circuit looking back into the output terminals. The independent voltage source is set equal to zero ($v_s = 0$), which means v_s acts as a short circuit. A test voltage V_x is applied to the output terminals, and the resulting test current is I_x. The output resistance, R_o, is given by
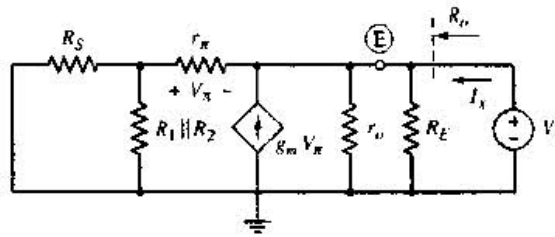
Figure 4.47 Small-signal equivalent circuit for emitter-follower output resistance calculations

$$R_o = \frac{V_x}{I_x} \qquad (4.61)$$

In this case, the control voltage V_π is not zero, but is a function of the test voltage V_x. The dependent current source must be included in this analysis. Summing currents at the output node, we have

$$I_x + g_m V_\pi = \frac{V_x}{R_E} + \frac{V_x}{r_o} + \frac{V_x}{r_\pi + R_1 \| R_2 \| R_S} \qquad (4.62)$$

The control voltage can be written in terms of the test voltage by a voltage divider equation as

$$V_\pi = -\left(\frac{r_\pi}{r_\pi + R_1 \| R_2 \| R_S}\right) \cdot V_x \qquad (4.63)$$

Equation (4.62) can then be written as

$$I_x = \left(\frac{g_m r_\pi}{r_\pi + R_1 \| R_2 \| R_S}\right) \cdot V_x + \frac{V_x}{R_E} + \frac{V_x}{r_o} + \frac{V_x}{r_\pi + R_1 \| R_2 \| R_S} \qquad (4.64)$$

Noting that $g_m r_\pi = \beta$, we find

$$\frac{I_x}{V_x} = \frac{1}{R_o} = \frac{1+\beta}{r_\pi + R_1 \| R_2 \| R_S} + \frac{1}{R_E} + \frac{1}{r_o} \qquad (4.65)$$

or

$$R_o = \left(\frac{r_\pi + R_1 \| R_2 \| R_S}{1+\beta}\right) \| R_E \| r_o \qquad (4.66)$$

Equation (4.66) says that the output resistance looking back into the output terminals is the effective resistance in the emitter, $R_E \| r_o$, in parallel with the resistance looking back into the emitter. In turn, the resistance looking into the emitter is the total resistance in the base circuit divided by $(1 + \beta)$. This is an important result and is the inverse of the resistance reflection rule looking to the base.

Example 4.11 Objective: Calculate the input and output resistance of the emitter-follower circuit shown in Figure 4.44.

The small-signal parameters, as determined in Example 4.10, are $r_\pi = 3.28\,\text{k}\Omega$. $\beta = 100$, and $r_o = 100\,\text{k}\Omega$.

Solution: Input Resistance. The input resistance looking into the base was determined in Example 4.10 as

$$R_{ib} = r_\pi + (1 + \beta)(r_o \| R_E) = 3.28 + (101)(100\|2) = 201 \, k\Omega$$

and the input resistance seen by the signal source R_i is

$$R_i = R_1 \| R_2 \| R_{ib} = 50\|50\|201 = 22.2 \, k\Omega$$

Comment: The input resistance of the emitter-follower looking into the base is substantially larger than that of the simple common-emitter circuit because of the $(1 + \beta)$ factor. This is one advantage of the emitter-follower circuit. However, in this case, the input resistance seen by the signal source is dominated by the bias resistors R_1 and R_2. To take advantage of the large input resistance of the emitter-follower circuit, the bias resistors must be designed to be much larger.

Solution: Output Resistance. The output resistance is found from Equation (4.66) as

$$R_o = \left(\frac{r_\pi + R_1 \| R_2 \| R_S}{1 + \beta} \right) \| R_E \| r_o = \left(\frac{3.28 + 50\|50\|0.5}{101} \right) \|2\|100$$

or

$$R_o = 0.0373\|2\|100 = 0.0366 \, k\Omega \Rightarrow 36.6 \, \Omega$$

The output resistance is dominated by the first term that has $(1 + \beta)$ in the denominator.

Comment: The emitter-follower circuit is sometimes referred to as an **impedance transformer**, since the input impedance is large and the output impedance is small. The very low output resistance makes the *emitter-follower act almost like an ideal voltage source*, so the output is not loaded down when used to drive another load. Because of this, the emitter-follower is often used as the output stage of a multistage amplifier.

Test Your Understanding

4.17 For the circuit shown in Figure 4.44, let $V_{CC} = 5 \, V$, $\beta = 120$, $V_A = 100 \, V$, $R_E = 1 \, k\Omega$, $V_{BE}(on) = 0.7 \, V$, $R_1 = 25 \, k\Omega$, and $R_2 = 50 \, k\Omega$. (a) Determine the small-signal voltage gain $A_v = V_o/V_s$. (b) Find the input resistance looking into the base of the transistor. (c) Find the output resistance looking into the output terminals. (Ans. (a) $A_v = 0.956$ (b) $R_{ib} = 120 \, k\Omega$ (c) $R_o = 15 \, \Omega$)

D4.18 Assume the transistor parameters for the circuit in Figure 4.44 are: $\beta = 100$, $V_{BE}(on) = 0.7 \, V$, and $V_A = \infty$. Assume the circuit parameters are: $R_E = 2 \, k\Omega$, and $V_{CC} = 10 \, V$. Design the circuit such that $V_{CEQ} = 5 \, V$ and the resistance seen by the signal source is at least $65 \, k\Omega$. What is the resulting small-signal voltage gain and output resistance? (Ans. $I_E = 2.5 \, mA$, $R_1 = 118 \, k\Omega$, $R_2 = 504 \, k\Omega$, $A_v = 0.995$, $R_o = 10.3 \, \Omega$, neglecting R_S)

4.6.3 Small-Signal Current Gain

We can determine the small-signal current gain of an emitter-follower by using the input resistance and the concept of current dividers. For the small-signal emitter-follower equivalent circuit shown in Figure 4.46, the small signal current gain is defined as

$$A_i = \frac{I_e}{I_i} \tag{4.67}$$

where I_e and I_i are the output and input current phasors.

Using a current divider equation, we can write the base current in terms of the input current, as follows:

$$I_b = \left(\frac{R_1 \| R_2}{R_1 \| R_2 + R_{ib}}\right) I_i \tag{4.68}$$

Since $g_m V_\pi = \beta I_b$, then,

$$I_o = (1 + \beta) I_b = (1 + \beta)\left(\frac{R_1 \| R_2}{R_1 \| R_2 + R_{ib}}\right) I_i \tag{4.69}$$

Writing the load current in terms of I_o produces

$$I_e = \left(\frac{r_o}{r_o + R_E}\right) I_o \tag{4.70}$$

Combining Equations (4.69) and (4.70), we obtain the small-signal current gain, as follows:

$$A_i = \frac{I_e}{I_i} = (1 + \beta)\left(\frac{R_1 \| R_2}{R_1 \| R_2 + R_{ib}}\right)\left(\frac{r_o}{r_o + R_E}\right) \tag{4.71}$$

If we assume that $R_1 \| R_2 \gg R_{ib}$ and $r_o \gg R_E$, then

$$A_i \cong (1 + \beta) \tag{4.72}$$

which is the current gain of the transistor.

Although the small-signal voltage gain of the emitter follower is slightly less than 1, the small-signal current is normally greater than 1. Therefore, the emitter-follower circuit produces a small-signal power gain.

Although we did not explicitly calculate a current gain in the common-emitter circuit previously, the analysis is the same as that for the emitter-follower and in general the current gain is also greater than unity.

Design Example 4.12 **Objective:** Consider the output signal of the amplifier designed in Example 4.6. We now want to design an emitter-follower circuit such that the output signal from this circuit does not vary by more than 5 percent when a load in the range $R_L = 4\,k\Omega$ to $R_L = 20\,k\Omega$ is connected to the output.

Discussion: The output resistance of the common-emitter circuit designed in Example 4.6 is $R_o = R_C = 10\,k\Omega$. Connecting a load resistance between $4\,k\Omega$ and $20\,k\Omega$ will load down this circuit, so that the output voltage will change substantially. For this reason, an emitter-follower circuit with a low output resistance must be designed to minimize the loading effect. The Thevenin equivalent circuit is shown in Figure 4.48. The output voltage can be written as
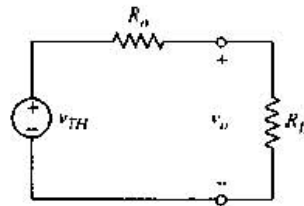
Figure 4.48 Thevenin equivalent of the output of an amplifier.

$$v_o = \left(\frac{R_L}{R_L + R_o}\right) \cdot v_{TH}$$

where v_{TH} is the ideal voltage generated by the amplifier. In order to have v_o change by less than 5 percent as a load resistance R_L is added, we must have R_o less than or equal to approximately 5 percent of the minimum value of R_L. In this case, then, we need R_o to be approximately 200 Ω.

Initial Design Approach: Consider the emitter-follower circuit shown in Figure 4.49. Note that the source resistance is $R_S = 10\,k\Omega$, corresponding to the output resistance of the circuit designed in Example 4.6. Assume that $\beta = 100$, $V_{BE}(on) = 0.7$ V, and $V_A = 80$ V.
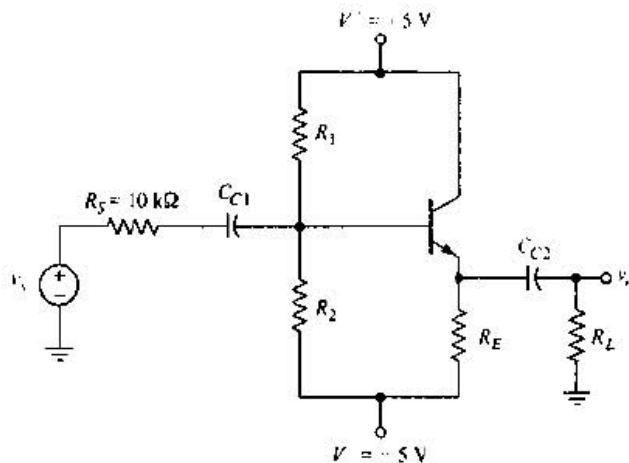

Figure 4.49 Figure for Example 4.12 and Exercises 4.19 and 4.20

The output resistance, given by Equation (4.66), is

$$R_o = \left(\frac{r_\pi + R_1 \| R_2 \| R_S}{1 + \beta}\right) \| R_E \| r_o$$

The first term, with $(1 + \beta)$ in the denominator, dominates, and if $R_1 \| R_2 \| R_S \cong R_S$, then we have

$$R_o \cong \frac{r_\pi + R_S}{1 + \beta}$$

For $R_o = 200\,\Omega$, we find

$$0.2 = \frac{r_\pi + 10}{101}$$

or $r_\pi = 10.2 \,\text{k}\Omega$. Since $r_\pi = (\beta V_T)/I_{CQ}$, the quiescent collector current must be

$$I_{CQ} = \frac{\beta V_T}{r_\pi} = \frac{(100)(0.026)}{10.2} = 0.255 \,\text{mA}$$

Assuming $I_{CQ} \cong I_{EQ}$ and letting $V_{CEQ} = 5 \,\text{V}$, we find

$$R_E = \frac{V^+ - V_{CEQ} - V^-}{I_{EQ}} = \frac{5 - 5 - (-5)}{0.255} = 19.6 \,\text{k}\Omega$$

The term $(1 + \beta)R_E$ is

$$(1 + \beta)R_E = (101)(19.6) \Rightarrow 1.98 \,\text{M}\Omega$$

With this large resistance, we can design a bias-stable circuit as defined in Chapter 3 and still have large values for bias resistances. Let

$$R_{TH} = (0.1)(1 + \beta)R_E = (0.1)(101)(19.6) = 198 \,\text{k}\Omega$$

The base current is

$$I_B = \frac{V_{TH} - V_{BE}(\text{on}) - V^-}{R_{TH} + (1 + \beta)R_E}$$

where

$$V_{TH} = \left(\frac{R_2}{R_1 + R_2}\right)(10) - 5 = \frac{1}{R_1}(R_{TH})(10) - 5$$

We can then write

$$\frac{0.255}{100} = \frac{\frac{1}{R_1}(198)(10) - 5 - 0.7 - (-5)}{198 + (101)(19.6)}$$

We find $R_1 = 344 \,\text{k}\Omega$ and $R_2 = 467 \,\text{k}\Omega$.

Comment: The quiescent collector current $I_{CQ} = 0.255 \,\text{mA}$ establishes the required r_π value which in turn establishes the required output resistance R_o.

Computer Simulation: We again used approximation techniques in our design. For this reason, it is useful to verify our design with a PSpice analysis, since the computer simulation will take into account more details than our hand design.

Figure 4.50 shows the PSpice circuit schematic. A 1 mV sinusoidal signal source is capacitively coupled to the output of the emitter follower. The input signal source has been set equal to zero. The current from the output signal source was found to be
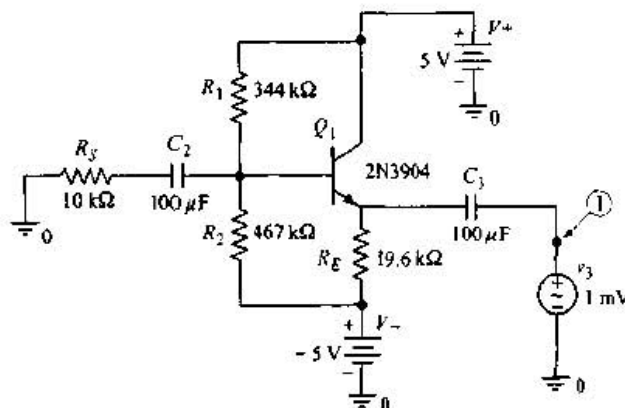

Figure 4.50 PSpice circuit schematic for Example 4.12

5.667 μA. The output resistance of the emitter follower is then $R_o = 176\,\Omega$, which means that we have met our desired specification that the output resistance should be less than $200\,\Omega$.

BJT MODEL PARAMETERS		**** BIPOLAR JUNCTION TRANSISTORS	
	Q2N3904	NAME	Q_Q1
	NPN	MODEL	Q2N3904
IS	6.734000E-15	IB	2.08E-06
BF	416.4	IC	2.39E-04
NF	1	VBE	6.27E-01
VAF	74.03	VBC	-4.65E+00
IKF	.06678	VCE	5.28E+00
ISE	6.734000E-15	BETADC	1.15E+02
NE	1.259	GM	9.19E-03
BR	.7371	RPI	1.47E+04
NR	1	RX	1.00E+01
RB	10	RO	3.30E+05
RBM	10	CBE	9.08E-12
RC	1	CBC	1.98E-12
CJE	4.493000E-12	CJS	0.00E+00
MJE	.2593	BETAAC	1.35E+02
CJC	3.638000E-12	CBX	0.00E+00
MJC	.3085	FT	1.32E+08
TF	301.200000E-12		
XTF	2		
VTF	4		
ITF	.4		
TR	239.500000E-09		
XTB	1.5		

Discussion: The transistor Q-point values from the PSpice analysis are also listed. From the computer simulation, the quiescent collector current is $I_{CQ} = 0.239\,\text{mA}$ compared to the designed value of 0.255 mA. The principal reason for the difference in value is the difference in base-emitter voltage and current gain between the hand analysis and computer simulation.

Test Your Understanding

*D4.19 Design a bias-stable emitter-follower circuit, using the circuit shown in Figure 4.49, such that $I_{CQ} = 0.75\,\text{mA}$ and the small-signal gain is $A_i = i_o/i_i = 15$. Assume $R_s = 0$. The transistor parameters are: $\beta = 100$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, and $V_A = 125\,\text{V}$. (Ans. $R_L = 2.0\,\text{k}\Omega$, $R_1 = 85.2\,\text{k}\Omega$, and $R_2 = 26.5\,\text{k}\Omega$)

*D4.20 For the circuit in Figure 4.49, the transistor parameters are: $\beta = 100$, $V_{BE}(\text{on}) = 0.7\,\text{V}$ and $V_A = 125\,\text{V}$. Assume $R_s = 0$. (a) Design a bias-stable circuit such that $I_{CQ} = 1.25\,\text{mA}$ and $V_{CEQ} = 4\,\text{V}$. (b) What is the small-signal current gain $A_i = i_o/i_i$? (c) What is the output resistance looking back into the output terminals? (d) What is the maximum symmetrical swing in the output voltage if the total collector-emitter voltage is to remain in the range $0.5 \leq v_{CE} \leq 9.5\,\text{V}$? (Ans. (a) $R_E = 4.76\,\text{k}\Omega$, $R_1 = 65.8\,\text{k}\Omega$, $R_2 = 178.8\,\text{k}\Omega$ (b) $A_i = 30.0$ (c) $R_o = 20.4\,\Omega$ (d) 2.07 V peak-to-peak)

4.21 Assume the circuit in Figure 4.51 uses a 2N2222A transistor. Assume a nominal dc current gain $\beta = 130$. Using the average h-parameter values (assume $h_{re} = 0$) given in the data sheets, determine $A_v = v_o/v_s$, $A_i = i_o/i_i$, R_{ib}, and R_o for:

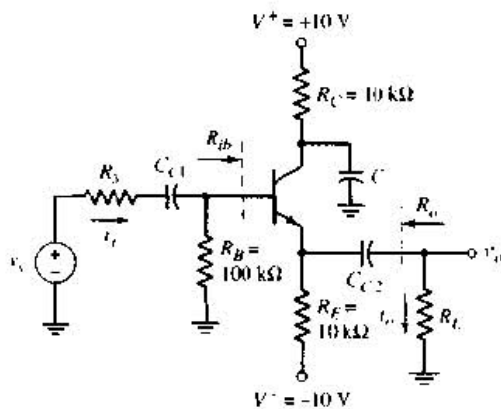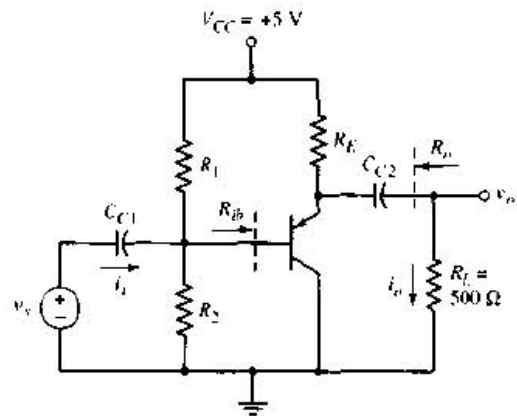**Figure 4.51**   Figure for Exercise 4.21

Figure 4.52   Figure for Exercises 4.22 and 4.23

(a) $R_S = R_L = 10\,k\Omega$, and (b) $R_S = 1\,k\Omega$, $R_L = 10\,k\Omega$. (Ans. (a) $A_v = 0.891$, $A_i = 8.59$, $R_{ib} = 641\,k\Omega$, $R_o = 96.0\,\Omega$ (b) $A_v = 0.982$, $R_o = 36.8\,\Omega$)

4.22   For the circuit in Figure 4.52, $R_E = 2\,k\Omega$, $R_1 = 50\,k\Omega$, $R_2 = 50\,k\Omega$ and the transistor parameters are: $\beta = 100$, $V_{EB}(on) = 0.7\,V$, and $V_A = 125\,V$. (a) Determine the small-signal voltage gain $A_v = v_o/v_s$. (b) Find the resistances R_{ib} and R_o. (c) Determine the range of R_o if each resistor varies by ± 5 percent. (Ans. (a) $A_v = 0.925$ (b) $R_{ib} = 4.37\,k\Omega$, $R_o = 32.0\,\Omega$ (c) $28.6 \le R_o \le 35.7\,\Omega$)

D4.23   For the circuit in Figure 4.52, the transistor parameters are: $\beta = 75$, $V_{EB}(on) = 0.7\,V$, and $V_A = 75\,V$. The small-signal current gain is to be $A_i = i_o/i_i = 10$. Assume $V_{ECQ} = 2.5\,V$. Determine the values of the elements required if: (a) $R_E = R_L$, and (b) $R_E = 4R_L$. (Ans. (a) $R_1 = 26.1\,k\Omega$, $R_2 = 9.55\,k\Omega$ (b) $R_1 = 18.6\,k\Omega$, $R_2 = 9.6\,k\Omega$)

4.7   COMMON-BASE AMPLIFIER

A third amplifier circuit configuration is the **common-base circuit**. To determine the small-signal voltage and current gains, and the input and output impedances, we will use the same hybrid-π equivalent circuit for the transistor that was used previously. The dc analysis of the common-base circuit is essentially the same as for the common-emitter circuit.

4.7.1   Small-Signal Voltage and Current Gains

Figure 4.53 shows the basic common-base circuit, in which the base is at signal ground and the input signal is applied to the emitter. Assume a load is connected to the output through a coupling capacitor C_{C2}.

Figure 4.54(a) again shows the hybrid-π model of the npn transistor, which the output resistance r_o assumed to be infinite. Figure 4.54(b) shows the small-signal equivalent circuit of the common-base circuit, including the hybrid-π model of the transistor. As a result of the common-base configuration, the hybrid-π model in the small-signal equivalent circuit may look a little strange.
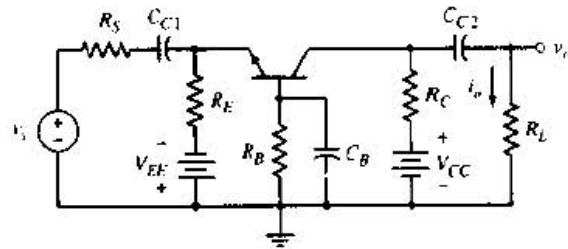
The small signal output voltage is given by

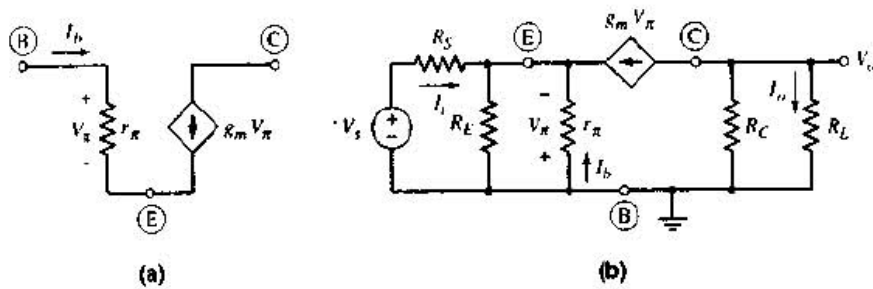**Figure 4.53**   Basic common-base circuit

Figure 4.54   (a) Simplified hybrid-π model of the npn transistor and (b) small-signal equivalent circuit of the common-base circuit

$$V_o = -(g_m V_\pi)(R_C \| R_L) \tag{4.73}$$

Writing a KCL equation at the emitter node, we obtain

$$g_m V_\pi + \frac{V_\pi}{r_\pi} + \frac{V_\pi}{R_E} + \frac{V_s - (-V_\pi)}{R_S} = 0 \tag{4.74}$$

Since $\beta = g_m r_\pi$. Equation (4.74) can be written

$$V_\pi \left(\frac{1+\beta}{r_\pi} + \frac{1}{R_E} + \frac{1}{R_S} \right) = -\frac{V_s}{R_S} \tag{4.75}$$

Then,

$$V_\pi = -\frac{V_s}{R_S} \left[\left(\frac{r_\pi}{1+\beta} \right) \Big\| R_E \| R_S \right] \tag{4.76}$$

Substituting Equation (4.76) into (4.73), we find the small-signal voltage gain, as follows:

$$A_v = \frac{V_o}{V_s} = +g_m \left(\frac{R_C \| R_L}{R_S} \right) \left[\left(\frac{r_\pi}{1+\beta} \right) \Big\| R_E \| R_S \right] \tag{4.77}$$

We can show that as R_S approaches zero, the small-signal voltage gain becomes

$$A_v = g_m (R_C \| R_L) \tag{4.78}$$

Figure 4.54(b) can also be used to determine the small-signal current gain. The current gain is defined as $A_i = I_o/I_i$. Writing a KCL equation at the emitter node, we have

$$I_i + \frac{V_\pi}{r_\pi} + g_m V_\pi + \frac{V_\pi}{R_E} = 0 \tag{4.79}$$

Solving for V_π, we obtain

$$V_\pi = -I_i \left[\left(\frac{r_\pi}{1 + \beta} \right) \middle\| R_E \right]$$ (4.80)

The load current is given by

$$I_o = -(g_m V_\pi)\left(\frac{R_C}{R_C + R_L} \right)$$ (4.81)

Combining Equations (4.80) and (4.81), we obtain an expression for the small-signal current gain, as follows:

$$A_i = \frac{I_o}{I_i} = g_m \left(\frac{R_C}{R_C + R_L} \right)\left[\left(\frac{r_\pi}{1 + \beta} \right) \middle\| R_E \right]$$ (4.82)

If we take the limit as R_E approaches infinity and R_L approaches zero, then the current gain becomes the short-circuit current gain given by

$$A_{io} = \frac{g_m r_\pi}{1 + \beta} = \frac{\beta}{1 + \beta} = \alpha$$ (4.83)

where α is the common-base current gain of the transistor.

Equations (4.77) and (4.83) indicate that, for the common-base circuit, the small-signal voltage gain is usually greater than 1 and the small-signal current gain is slightly less than 1. However, we still have a small-signal power gain. The applications of a common-base circuit take advantage of the input and output resistance characteristics.

4.7.2   Input and Output Impedance

Figure 4.55 shows the small-signal equivalent circuit of the common-base configuration looking into the emitter. In this circuit, for convenience only, we have reversed the polarity of the control voltage, which reverses the direction of the dependent current source.
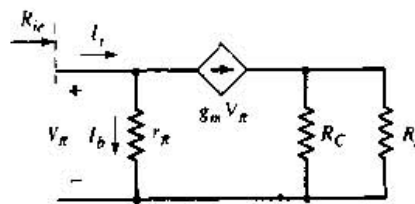

Figure 4.55   Common-base equivalent circuit for input resistance calculations

The input resistance looking into the emitter is defined as

$$R_{ie} = \frac{V_\pi}{I_i}$$ (4.84)

If we write a KCL equation at the input, we obtain

$$I_i = I_b + g_m V_\pi = \frac{V_\pi}{r_\pi} + g_m V_\pi = V_\pi \left(\frac{1 + \beta}{r_\pi} \right)$$ (4.85)

Therefore,

$$R_{ic} = \frac{V_\pi}{I_i} = \frac{r_\pi}{1+\beta} \equiv r_e \qquad (4.86)$$

The resistance looking into the emitter, with the base grounded, is usually defined as r_e and is quite small, as already shown in the analysis of the emitter-follower circuit. When the input signal is a current source, a small input resistance is desirable

Figure 4.56 shows the circuit used to calculate the output resistance. The independent source v_s has been set equal to zero. Writing a KCL equation at the emitter, we find

$$g_m V_\pi + \frac{V_\pi}{r_\pi} + \frac{V_\pi}{R_E} + \frac{V_\pi}{R_S} = 0 \qquad (4.87)$$

This implies that $V_\pi = 0$, which means that the independent source $g_m V_\pi$ is also zero. Consequently, the output resistance looking back into the output terminals is then

$$R_o = R_C \qquad (4.88)$$

Because we have assumed r_o is infinite, the output resistance looking back into the collector terminal is essentially infinite, which means that the common-base circuit looks almost like an ideal current source.
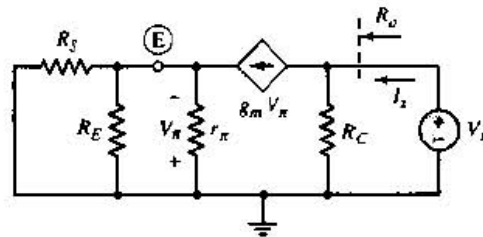

Figure 4.56 Common-base equivalent circuit for output resistance calculations

Discussion

The common-base circuit is very useful when the input signal is a current. We will see this type of application when we discuss the cascode circuit in Section 4.9.

Test Your Understanding

4.24 For the circuit shown in Figure 4.57, the transistor parameters are: $\beta = 100$, $V_{EB}(on) = 0.7$ V, and $r_o = \infty$. (a) Calculate the quiescent values of I_{CQ} and V_{ECQ}. (b) Determine the small-signal current gain $A_i = i_o/i_i$. (c) Determine the small-signal voltage gain $A_v = v_o/v_s$. (d) Determine the maximum symmetrical swing in the output voltage if the emitter–collector voltage is in the range $0.5 \le v_{EC} \le 19.5$ V. (Ans. (a) $I_{CQ} = 0.921$ mA, $V_{ECQ} = 6.1$ V (b) $A_i = 0.987$ (c) $A_v = 177$ (d) 9.21 V peak-to-peak)
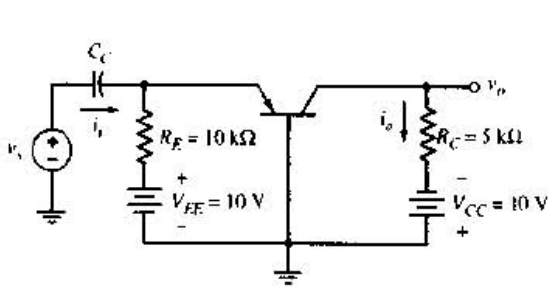
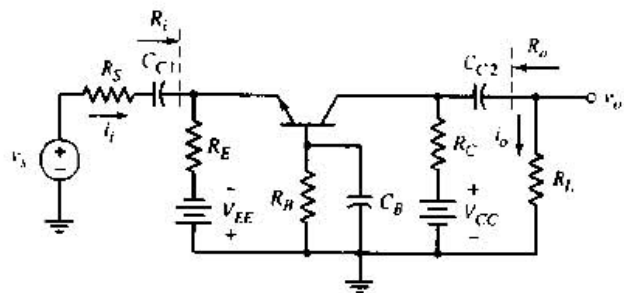**Figure 4.57** Figure for Exercise 4.24

Figure 4.58 Figure for Exercises 4.25 and 4.26

4.25 For the circuit shown in Figure 4.58, the parameters are: $R_B = 100\,\text{k}\Omega$, $R_E = 10\,\text{k}\Omega$, $R_C = 10\,\text{k}\Omega$, $V_{CC} = V_{EE} = 10\,\text{V}$, $R_L = 1\,\text{k}\Omega$, $R_S = 1\,\text{k}\Omega$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, $\beta = 100$, and $V_A = \infty$. (a) Determine the small-signal transistor parameters g_m, r_π, and r_o. (b) Find the small-signal current gain $A_i = i_o/i_i$ and the small-signal voltage gain $A_r = v_o/v_s$. (c) Determine the input resistance R_i and the output resistance R_o. (Ans. (a) $r_\pi = 3.1\,\text{k}\Omega$, $g_m = 32.23\,\text{mA/V}$, $r_o = \infty$ (b) $A_r = 0.870$, $A_i = 0.90$ (c) $R_i = 0.0307\,\text{k}\Omega$, $R_o = 10\,\text{k}\Omega$)

D4.26 For the circuit shown in Figure 4.58, let $R_S = 0$, $C_B = 0$, $R_C = R_L = 2\,\text{k}\Omega$, $V_{CC} = V_{EE} = 5\,\text{V}$, $\beta = 100$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, and $V_A = \infty$. Design R_E and R_B for a dc quiescent collector current of 1 mA and a small-signal voltage gain of 20. (Ans. $R_B = 2.4\,\text{k}\Omega$, $R_E = 4.23\,\text{k}\Omega$)

4.8 THE THREE BASIC AMPLIFIERS: SUMMARY AND COMPARISON

The basic small-signal characteristics of the three single-stage amplifier configurations are summarized in Table 4.4.

Table 4.4 Characteristics of the three BJT amplifier configurations

Configuration	Voltage gain	Current gain	Input resistance	Output resistance
Common emitter	$A_r > 1$	$A_i > 1$	Moderate	Moderate to high
Emitter follower	$A_r \cong 1$	$A_i > 1$	High	Low
Common base	$A_r > 1$	$A_i \cong 1$	Low	Moderate to high

For the common-emitter circuit, the voltage and current gains are generally greater than 1. For the emitter-follower, the voltage gain is slightly less than 1, while the current gain is greater than 1. For the common-base circuit, the voltage gain is greater than 1, while the current gain is less than 1.

The input resistance looking into the base terminal of a common-emitter circuit may be in the low kilohm range; in an emitter follower, it is generally in the 50 to 100 kΩ range. The input resistance looking into the emitter of a common-base circuit is generally on the order of tens of ohms.

The overall input resistance of both the common-emitter and emitter-follower circuits can be greatly affected by the bias circuitry.

The output resistance of the emitter follower is generally in the range of a few ohms to tens of ohms. In contrast, the output resistance looking into the collector terminal of the common-emitter and common-base circuits is very high. In addition, the output resistance looking back into the output terminal of the common-emitter and common-base circuits is a strong function of the collector resistance. For these circuits, the output resistance can easily drop to a few kilohms.

The characteristics of these single-stage amplifiers will be used in the design of multistage amplifiers.

4.9   MULTISTAGE AMPLIFIERS

In most applications, a single transistor amplifier will not be able to meet the combined specifications of a given amplification factor, input resistance, and output resistance. For example, the required voltage gain may exceed that which can be obtained in a single transistor circuit. We also saw an illustration of this effect in Example 4.12, in which a low output resistance was required in a particular design.

Transistor amplifier circuits can be connected in series, or **cascaded**, as shown in Figure 4.59. This may be done either to increase the overall small-signal voltage gain or to provide an overall voltage gain greater than 1, with a very low output resistance. The overall voltage or current gain, in general, is not simply the product of the individual amplification factors. For example, the gain of stage 1 is a function of the input resistance of stage 2. In other words, loading effects may have to be taken into account.

There are may possible multistage configurations; we will examine a few here, in order to understand the type of analysis required.
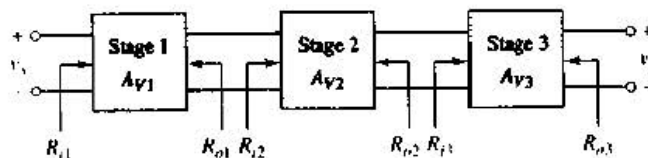

Figure 4.59   A generalized three-stage amplifier

4.9.1   Multistage Analysis: Cascade Configuration

In Figure 4.60, the circuit is a cascade configuration of two common-emitter circuits. The dc analysis of this circuit, done in Example 3.17 of Chapter 3, showed that both transistors are biased in the forward-active mode. Figure 4.61 shows the small-signal equivalent circuit, assuming all capacitors act as short circuits and each transistor output resistance r_o is infinite.

We may start the analysis at the output and work back to the input, or start at the input and work toward the output.

The small-signal voltage gain is

$$A_v = \frac{V_o}{V_s} = g_{m1} g_{m2} (R_{C1} \| r_{\pi2})(R_{C2} \| R_L)\left(\frac{R_i}{R_i + R_S}\right) \qquad (4.89)$$
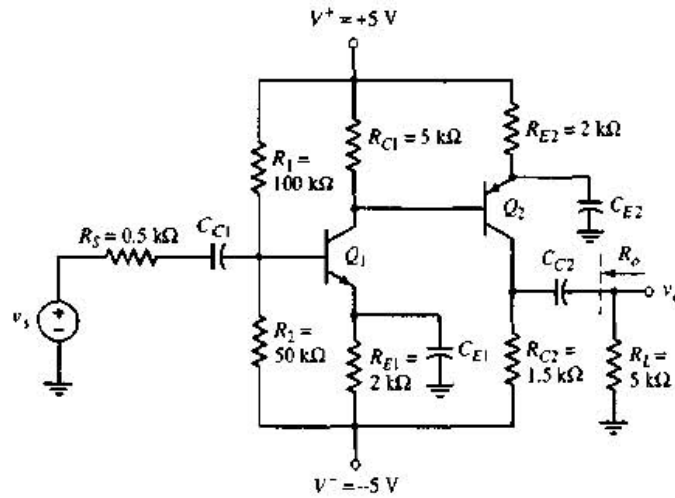
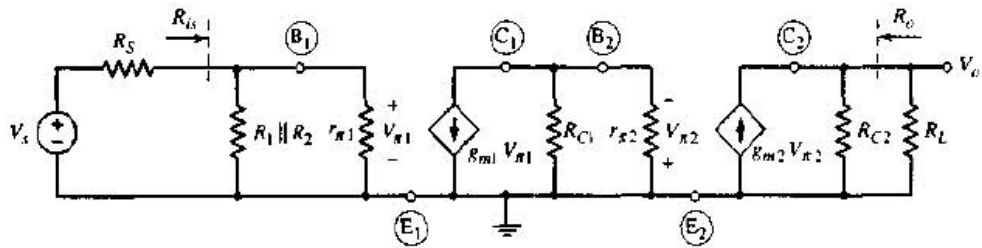**Figure 4.60** A two-stage amplifier in a cascade configuration

Figure 4.61 Small-signal equivalent circuit of the cascade configuration

The input resistance of the amplifier is

$$R_{is} = R_1 \| R_2 \| r_{\pi 1}$$

which is identical to that of a single-stage common-emitter amplifier. Similarly, the output resistance looking back into the output terminals is $R_o = R_{C2}$. To determine the output resistance, the independent source V_s is set equal to zero, which means that $V_{\pi 1} = 0$. Then $g_{m1} V_{\pi 1} = 0$, which gives $V_{\pi 2} = 0$ and $g_{m2} V_{\pi 2} = 0$. The output resistance is therefore R_{C2}. Again, this is the same as the output resistance of a single-stage common-emitter amplifier.

Computer Example 4.13 **Objective:** Determine the small-signal voltage gain of the multitransistor circuit shown in Figure 4.60 using a PSpice analysis.

The dc and ac analyses of a multitransistor circuit become more complex compared to those for a single-transistor circuit. In this situation, a computer simulation of the circuit, without a hand analysis, is extremely useful.

The PSpice circuit schematic is shown in Figure 4.62. Also given are the Q-point values of the transistors. The ac voltage at the collector of the npn transistor is 51 μV and that at the collector of the pnp transistor is 4.79 mV. Since the input voltage was assumed to be 1 μV, this result shows that a significant voltage gain can be achieved in a two-stage amplifier.
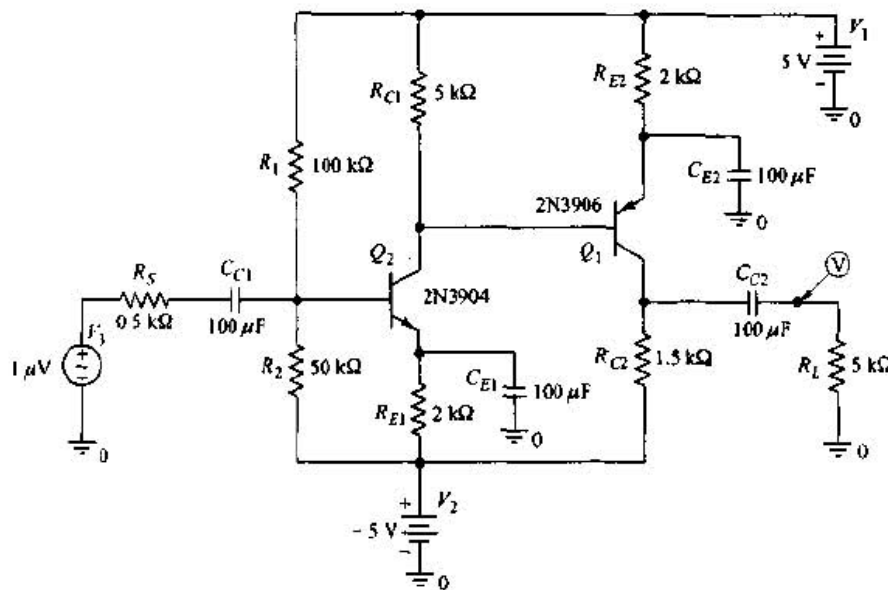
**Figure 4.62**   PSpice circuit schematic for Example 4.13

```
****  BIPOLAR JUNCTION TRANSISTORS
```

NAME	Q_Q1	Q_Q2
MODEL	Q2N3906	Q2N3904
IB	-1.42E-05	8.59E-06
IC	-2.54E-03	1.18E-03
VBE	-7.30E-01	6.70E-01
VBC	3.68E-01	-1.12E+00
VCE	-1.10E+00	1.79E+00
BETADC	1.79E+02	1.37E+02
GM	9.50E-02	4.48E-02
RPI	1.82E+03	3.49E+03
RX	1.00E+01	1.00E+01
RO	7.52E+03	6.37E+04
CBE	3.11E-11	2.00E-11
CBC	7.75E-12	2.74E-12
CJS	0.00E+00	0.00E+00
BETAAC	1.73E+02	1.57E+02
CBX	0.00E+00	0.00E+00
FT	3.89E+08	3.14E+08

Comment: We can see from the Q-point values that the collector–emitter voltage of each transistor is quite small. This implies that the maximum symmetrical swing in the output voltage is limited to a fairly small value. These Q-point values can be increased by a slight redesign of the circuit.

Discussion: The transistors used in this PSpice analysis of the circuit were standard bipolar transistors from the PSpice library. We must keep in mind that, for the computer simulation to be valid, the models of the devices used in the simulation must match those of the actual devices used in the circuit. If the actual transistor characteristics were substantially different from those used in the computer simulation, then the results of the computer analysis would not be accurate.

In some applications, it would be desirable to have a bipolar transistor with a much larger current gain than can normally be obtained. Figure 4.63(a) shows a multitransistor configuration, called a Darlington pair or a Darlington configuration, that provides increased current gain.
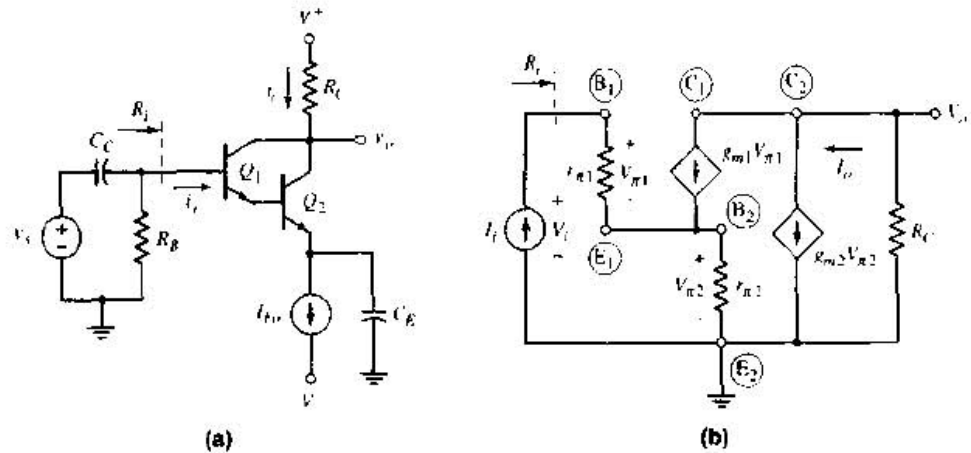
Figure 4.63   (a) A Darlington pair configuration; (b) small-signal equivalent circuit

The small-signal equivalent in which the input signal is assumed to be a current source, is shown in Figure 4.63(b). We will use the input current source to determine the current gain of the circuit. To determine the small-signal current gain $A_i = I_o/I_i$, we see that

$$V_{\pi 1} = I_i r_{\pi 1} \tag{4.90}$$

Therefore,

$$g_{m1} V_{\pi 1} = g_{m1} r_{\pi 1} I_i = \beta_1 I_i \tag{4.91}$$

Then,

$$V_{\pi 2} = (I_i + \beta_1 I_i) r_{\pi 2} \tag{4.92}$$

The output current is

$$I_o = g_{m1} V_{\pi 1} + g_{m2} V_{\pi 2} = \beta_1 I_i + \beta_2 (1 + \beta_1) I_i \tag{4.93}$$

where $g_{m2} r_{\pi 2} = \beta_2$. The overall current gain is then

$$A_i = \frac{I_o}{I_i} = \beta_1 + \beta_2 (1 + \beta_1) \cong \beta_1 \beta_2 \tag{4.94}$$

From Equation (4.94), we see that the overall small-signal current gain of the Darlington pair is essentially the product of the individual current gains.

The input resistance is $R_i = V_i/I_i$. We can write that

$$V_i = V_{\pi 1} + V_{\pi 2} = I_i r_{\pi 1} + I_i (1 + \beta_1) r_{\pi 2} \tag{4.95}$$

so that

$$R_i = r_{\pi 1} + (1 + \beta_1) r_{\pi 2} \tag{4.96}$$

The base of transistor Q_2 is connected to the emitter of Q_1, which means that the input resistance to Q_2 is multiplied by the factor $(1 + \beta_1)$, as we saw in circuits with emitter resistors. We can write

$$r_{\pi 1} = \frac{\beta_1 V_T}{I_{CQ1}} \tag{4.97}$$

and

$$I_{CQ1} \simeq \frac{I_{CQ2}}{\beta_2} \tag{4.98}$$

Therefore,

$$r_{\pi 1} = \beta_1 \left(\frac{\beta_2 V_T}{I_{CQ2}} \right) = \beta_1 r_{\pi 2} \tag{4.99}$$

From Equation (4.96), the input resistance is then approximately

$$R_i \simeq 2\beta_1 r_{\pi 2} \tag{4.100}$$

We see from these equations that the overall gain of the Darlington pair is large. At the same time, the input resistance tends to be large, because of the β multiplication.

4.9.2   Cascode Configuration

A slightly different multistage configuration, called a **cascode configuration**, is shown in Figure 4.64(a). The input is into a common-emitter amplifier (Q_1), which drives a common-base amplifier (Q_2). The ac equivalent circuit is shown in Figure 4.64(b). We see that the output signal current of Q_1 is the input signal of Q_2. We mentioned previously that, normally, the input signal of a common-base configuration is to be a current. One advantage of this circuit is that the output resistance looking into the collector of Q_2 is much larger than the output
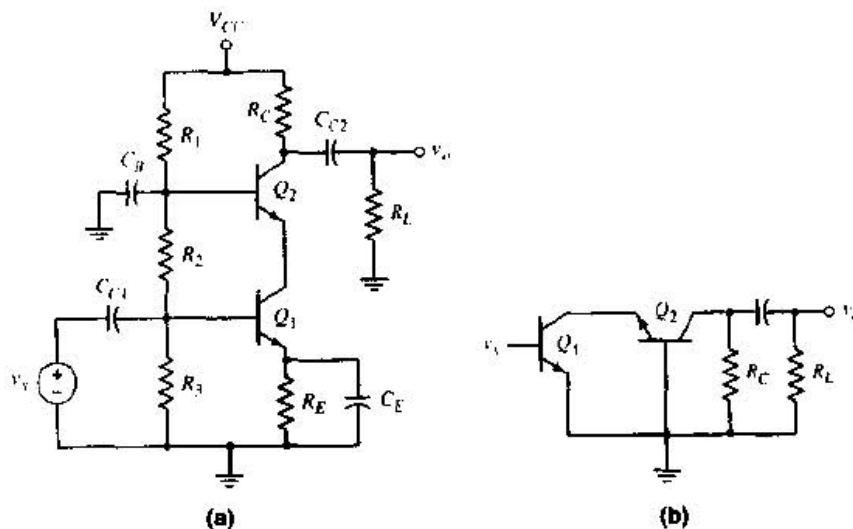

Figure 4.64   (a) Cascode amplifier and (b) the ac equivalent circuit

of a common-emitter circuit. Another important advantage of this circuit is in the frequency response, as we will see in Chapter 7.

The small-signal equivalent circuit is shown in Figure 4.65 for the case when the capacitors act as short circuits. We see that $V_{\pi 1} = V_s$ since we are assuming an ideal signal voltage source. Writing a KCL equation at E_2, we have

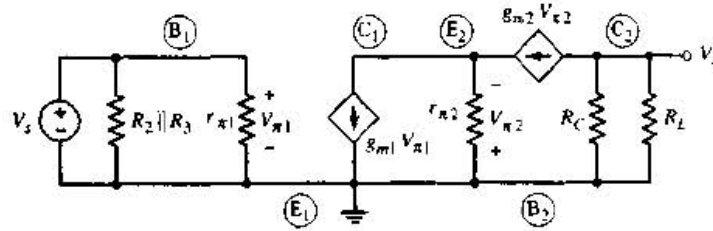$$g_{m1}V_{\pi 1} = \frac{V_{\pi 2}}{r_{\pi 2}} + g_{m2}V_{\pi 2} \qquad (4.101)$$

Figure 4.65 Small-signal equivalent circuit of the cascode configuration

Solving for the control voltage $V_{\pi 2}$, we find

$$V_{\pi 2} = \left(\frac{r_{\pi 2}}{1+\beta_2}\right)(g_{m1}V_s) \qquad (4.102)$$

where $\beta_2 = g_{m2}r_{\pi 2}$. The output voltage is

$$V_o = -(g_{m2}V_{\pi 2})(R_C\|R_L) \qquad (4.103(a))$$

or

$$V_o = -g_{m1}g_{m2}\left(\frac{r_{\pi 2}}{1+\beta_2}\right)(R_C\|R_L)V_s \qquad (4.103(b))$$

Therefore, the small-signal voltage gain is

$$A_v = \frac{V_o}{V_s} = -g_{m1}g_{m2}\left(\frac{r_{\pi 2}}{1+\beta_2}\right)(R_C\|R_L) \qquad (4.104)$$

An examination of Equation (4.104) shows

$$g_{m2}\left(\frac{r_{\pi 2}}{1+\beta_2}\right) = \frac{\beta_2}{1+\beta_2} \cong 1 \qquad (4.105)$$

The gain of the cascode amplifier is then approximately

$$A_v \cong -g_{m1}(R_C\|R_L) \qquad (4.106)$$

which is the same as for a single-stage common-emitter amplifier. This result is to be expected since the current gain of the common-base circuit is essentially unity.

Test Your Understanding

*4.27 For each transistor in the circuit in Figure 4.66, the parameters are: $\beta = 125$, $V_{BE}(\text{on}) = 0.7\,V$, and $r_o = \infty$. (a) Determine the Q-points of each transistor. (b) Find the overall small-signal voltage gain $A_v = V_o/V_s$. (c) Determine the input resistance R_i and the output resistance R_o. (Ans. (a) $I_{CQ1} = 0.366\,mA$, $V_{CEQ1} = 7.90\,V$, $I_{CQ2} = 4.81\,mA$, $V_{CEQ2} = 2.72\,V$ (b) $A_v = -17.7$ (c) $R_i = 4.76\,k\Omega$, $R_o = 43.7\,\Omega$)

*4.28 Consider the circuit in Figure 4.63(a). Let $\beta = 100$, $V_{BE}(\text{on}) = 0.7\,V$, and $V_A = \infty$ for each transistor. Assume $R_B = 10\,k\Omega$, $R_C = 4\,k\Omega$, $I_{EQ} = 1\,mA$, $V^+ = 5\,V$, and $V^- = -5\,V$. (a) Determine the Q-point values for each transistor. (b) Calculate the small-signal hybrid-π parameters for each transistor. (c) Find the overall small-signal voltage gain $A_v = V_o/V_s$. (d) Find the input resistance R_i. (Ans. (a) $I_{CQ1} = 0.0098\,mA$, $V_{CEQ1} = 1.7\,V$, $I_{CQ2} = 0.990\,mA$, $V_{CEQ2} = 2.4\,V$ (b) $r_{\pi1} = 265\,k\Omega$, $g_{m1} = 0.377\,mA/V$, $r_{\pi2} = 2.63\,k\Omega$, $g_{m2} = 38.1\,mA/V$ (c) $A_v = -76.9$ (d) $R_i = 531\,k\Omega$)

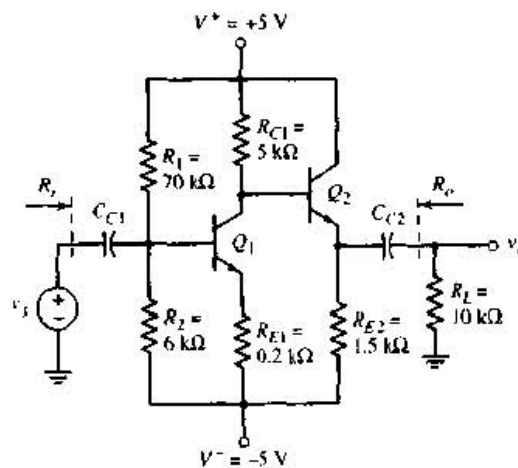**Figure 4.66** Figure for Exercise 4.27

4.29 For the circuit shown in Figure 4.67, let $\beta = 100$, $V_{BE}(\text{on}) = 0.7\,V$, and $V_A = \infty$ for each transistor. Repeat parts (a)-(d) of Exercise 4.28. (Ans. (a) $I_{CQ1} = 0.464\,mA$, $V_{CEQ1} = 8.18\,V$, $I_{CQ2} = 0.842\,mA$, $V_{CEQ2} = 8.88\,V$ (b) $r_{\pi1} = 5.60\,k\Omega$, $g_{m1} = 17.8\,mA/V$, $r_{\pi2} = 3.09\,k\Omega$, $g_{m2} = 32.4\,mA/V$, $r_{o1} = r_{o2} = \infty$ (c) $A_v = -0.298$ (d) $R_i = 1.99\,M\Omega$)
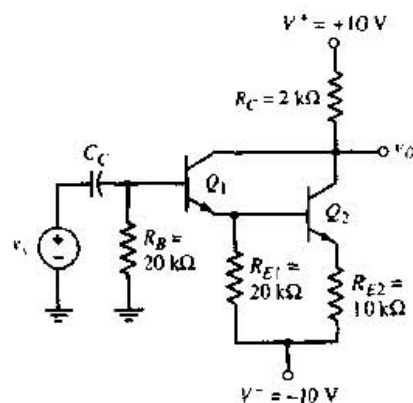

Figure 4.67 Figure for Exercise 4.29

D4.30   Consider the cascode circuit in Figure 4.64(a). Let $\beta = 100$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, and $V_A = \infty$ for each transistor. Assume $V_{CC} = 12\,\text{V}$, $R_L = 2\,\text{k}\Omega$, and $R_E = 0.5\,\text{k}\Omega$. (a) Find R_C, R_1, R_2, and R_3 such that $I_{CQ2} = 0.5\,\text{mA}$ and $V_{CE1} = V_{CE2} = 4\,\text{V}$. Let $R_1 + R_2 + R_3 = 100\,\text{k}\Omega$. (Hint: Neglect the dc base currents and assume $I_C \approx I_E$ in both Q_1 and Q_2.) (b) Determine the small-signal hybrid-π parameters for each transistor. (c) Determine the small-signal voltage gain $A_v = V_o/V_s$. (Ans. (a) $R_C = 7.5\,\text{k}\Omega$, $R_3 = 7.92\,\text{k}\Omega$, $R_2 = 33.3\,\text{k}\Omega$, $R_1 = 58.8\,\text{k}\Omega$ (b) $r_{\pi 1} = r_{\pi 2} = 5.2\,\text{k}\Omega$, $g_{m1} = g_{m2} = 19.23$ mA/V, $r_{o1} = r_{o2} = \infty$ (c) $A_v = -30.1$)

4.10   POWER CONSIDERATIONS

As mentioned previously, an amplifier produces a **small-signal power gain**. Since energy must be conserved, the question naturally arises as to the source of this "extra" signal power. We will see that the "extra" signal power delivered to a load is a result of a redistribution of power between the load and the transistor.

Consider the simple common-emitter circuit shown in Figure 4.68 in which an ideal signal voltage source is connected at the input. The dc power supplied by the V_{CC} voltage source P_{CC}, the dc power dissipated or supplied to the collector resistor P_{RC}, and the dc power dissipated in the transistor P_Q are given, respectively, as
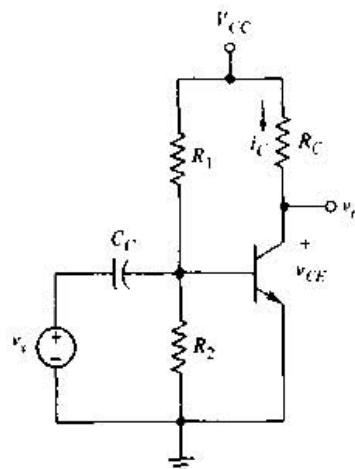
$$P_{CC} = I_{CQ}V_{CC} + P_{\text{Bias}} \tag{4.107(a)}$$

$$P_{RC} = I_{CQ}^2 R_c \tag{4.107(b)}$$

and

$$P_Q = I_{CQ}V_{CEQ} + I_{BQ}V_{BEQ} \cong I_{CQ}V_{CEQ} \tag{4.107(c)}$$

The term P_{Bias} is the power dissipated in the bias resistors R_1 and R_2. Normally in a transistor $I_{CQ} \gg I_{BQ}$, so the power dissipated is primarily a function of the collector current and collector-emitter voltage.

Figure 4.68   Simple common-emitter amplifier for power calculations

If the signal voltage is given by

$$v_s = V_p \cos \omega t \tag{4.108}$$

then the total base current is given by

$$i_B = I_{BQ} + \frac{V_p}{r_\pi} \cos \omega t = I_{BQ} + I_b \cos \omega t \tag{4.109}$$

and the total collector current is

$$i_C = I_{CQ} + \beta I_b \cos \omega t = I_{CQ} + I_c \cos \omega t \tag{4.110}$$

The total instantaneous collector-emitter voltage is

$$v_{CE} = V_{CC} - i_C R_C = V_{CC} - (I_{CQ} + I_c \cos \omega t) R_C = V_{CEQ} - I_c R_C \cos \omega t \tag{4.111}$$

The average power, including ac signals, supplied by the voltage source V_{CC} is given by

$$\begin{aligned}
\bar{p}_s &= \frac{1}{T} \int_0^T V_{CC} \cdot i_C \, dt + P_{Bias} \\
&= \frac{1}{T} \int_0^T V_{CC} \cdot [I_{CQ} + I_c \cos \omega t] \, dt + P_{Bias} \\
&= V_{CC} I_{CQ} + \frac{V_{CC} I_c}{T} \int_0^T \cos \omega t \, dt + P_{Bias}
\end{aligned} \tag{4.112}$$

Since the integral of the cosine function over one period is zero, the average power supplied by the voltage source is the same as the dc power supplied. The dc voltage source does not supply additional power.

The average power delivered to the load R_C is found from

$$\begin{aligned}
\bar{p}_{RC} &= \frac{1}{T} \int_0^T i_C^2 R_C \, dt = \frac{R_C}{T} \int_0^T [I_{CQ} + I_c \cos \omega t]^2 \, dt \\
&= \frac{I_{CQ}^2 R_C}{T} \int_0^T dt + \frac{2 I_{CQ} I_c}{T} \int_0^T \cos \omega t \, dt + \frac{I_c^2 R_C}{T} \int_0^T \cos^2 \omega t \, dt
\end{aligned} \tag{4.113}$$

The middle term of this last expression is again zero, so

$$\bar{p}_{RC} = I_{CQ}^2 R_C + \tfrac{1}{2} I_c^2 R_C \tag{4.114}$$

The average power delivered to the load has increased because of the signal source. This is expected in an amplifier.

Now, the average power dissipated in the transistor is

$$\bar{p}_Q = \frac{1}{T}\int_0^T i_C \cdot v_{CE}\, dt$$

$$= \frac{1}{T}\int_0^T [I_{CQ} + I_c \cos \omega t] \cdot [V_{CEQ} - I_c R_C \cos \omega t]\, dt$$
(4.115)

which produces

$$\bar{p}_Q = I_{CQ}V_{CEQ} - \frac{I_c^2 R_C}{T}\int_0^T \cos^2 \omega t\, dt$$
(4.116(a))

or

$$\bar{p}_Q = I_{CQ}V_{CEQ} - \tfrac{1}{2}I_c^2 R_C$$
(4.116(b))

From Equation (4.116(b)), we can deduce that the average power dissipated in the transistor decreases when an ac signal is applied. The V_{CC} source still supplies all of the power, but the input signal changes the relative distribution of power between the transistor and the load.

Test Your Understanding

4.31   In the circuit in Figure 4.69 the transistor parameters are: $\beta = 80$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, and $V_A = \infty$. Determine the average power dissipated in R_C, R_L, and Q for: (a) $v_s = 0$, and (b) $v_s = 18\cos\omega t\,\text{mV}$. (Ans. (a) $\bar{p}_{RC} = 8\,\text{mW}$, $\bar{p}_{RL} = 0$, $\bar{p}_Q = 14\,\text{mW}$ (b) $\bar{p}_Q = 13.0\,\text{mW}$, $\bar{p}_{RL} = 0.479\,\text{mW}$, $\bar{p}_{RC} = 8.48\,\text{mW}$)

4.32   For the circuit in Figure 4.70, the transistor parameters are: $\beta = 100$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, and $V_A = \infty$. (a) Determine R_C such that the Q-point is in the center of the load line. (b) Determine the average power dissipated in R_C and Q for $v_s = 0$. (c) Considering the maximum symmetrical swing in the output voltage, determine the ratio of maximum signal power delivered to R_C to the total power dissipated in R_C and the transistor. (Ans. (a) $R_C = 2.52\,\text{k}\Omega$ (b) $\bar{p}_{RC} = \bar{p}_Q = 2.48\,\text{mW}$ (c) 0.25)
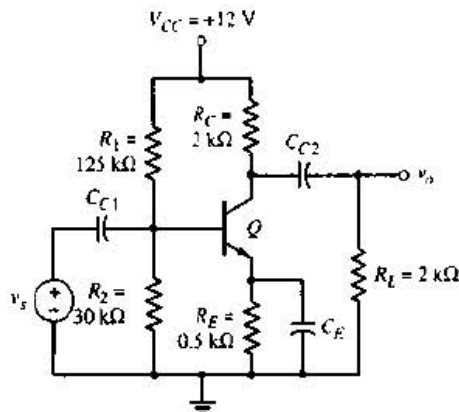

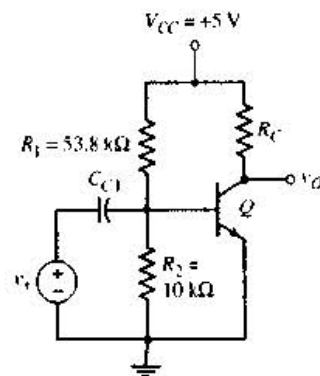**Figure 4.69**   Figure for Exercise 4.31   **Figure 4.70**   Figure for Exercise 4.32

4.11   SUMMARY

- This chapter emphasized the application of bipolar transistors in linear amplifier circuits. A small-signal equivalent circuit for the transistor was developed that is used in the analysis and design of linear amplifiers.

- Three basic circuit configurations were considered: the common–emitter, emitter-follower, and common-base. These three configurations form the basic building blocks for more complex integrated circuits. The small-signal voltage gains, current gains, and input and output resistances for these circuits were analyzed. Table 4.4 compares the circuit characteristics of the three circuits.

- The cascode configuration of two common-emitter circuits was analyzed as one example of a multistage transistor circuit. The overall small-signal voltage gain is increased compared to that of a single stage amplifier. A Darlington pair configuration was also analyzed. In this multistage circuit, the overall current gain increases and the input resistance increases compared to a single transistor circuit.

CHECKPOINT

After studying this chapter, the reader should have the ability to:

✔ Explain graphically the amplification process in a simple bipolar amplifier circuit. (Section 4.2)

✔ Describe the small-signal hybrid-π equivalent circuit of the bipolar transistor and to determine the values of the small-signal hybrid-π parameters. (Section 4.2)

✔ Apply the small-signal hybrid-π equivalent circuit to various bipolar amplifier circuits to obtain the time-varying circuit characteristics.

✔ Characterize the small-signal voltage and current gains and the input and output resistances of a common-emitter amplifier. (Section 4.4)

✔ Characterize the small-signal voltage and current gains and the input and output resistances of an emitter-follower amplifier. (Section 4.6)

✔ Characterize the small-signal voltage and current gains and the input and output resistances of a common-base amplifier. (Section 4.7)

✔ Apply the bipolar small-signal equivalent circuit in the analysis of multistage amplifier circuits

REVIEW QUESTIONS

1. Discuss, using the concept of a load line superimposed on the transistor characteristics, how a simple common-emitter circuit can amplify a time-varying signal.

2. Why can the analysis of a transistor circuit be split into a dc analysis, with all ac sources set equal to zero, and then an ac analysis, with all dc sources set equal to zero?

3. What are the physical meanings of the hybrid-π parameters r_π and r_o?

4. What does the term small-signal imply?

5. Discuss the difference between the ac and dc common-emitter current gains.

6. Discuss similarities and differences between the hybrid-π and h-parameter models of the bipolar transistor.

7. Discuss the four equivalent two-port networks and discuss the conditions under which each equivalent circuit would be used.

8. Sketch a simple common-emitter amplifier circuit and discuss the general ac circuit characteristics (voltage gain, current gain, input and output resistances).

9. Discuss the general conditions under which a common-emitter amplifier would be used.

10. What are the changes in the ac characteristics of a common-emitter amplifier when an emitter resistor and an emitter bypass capacitor are incorporated in the design?

11. Discuss the concepts of a dc load line and an ac load line.

12. Sketch a simple emitter-follower amplifier circuit and discuss the general ac circuit characteristics (voltage gain, current gain, input and output resistances).

13. Discuss the general conditions under which an emitter-follower amplifier would be used.

14. Sketch a simple common-base amplifier circuit and discuss the general ac circuit characteristics (voltage gain, current gain, input and output resistances).

15. Discuss the general conditions under which a common-base amplifier would be used.

16. Compare the ac circuit characteristics of the common-emitter, emitter-follower, and common-base circuits.

17. State at least two reasons why a multistage amplifier circuit would be required in a design rather than a single-stage circuit.

18. If a transistor circuit provides signal power gain, discuss the source of this additional signal power.

PROBLEMS

[Note: In the following problems, assume that the B–E turn-on voltage is 0.7 V for both npn and pnp transistors and that $V_A = \infty$ unless otherwise stated. Also assume that all capacitors act as short circuits to the signal.]

Section 4.2   The Bipolar Linear Amplifier

4.1 (a) If the transistor parameters are $\beta = 180$ and $V_A = 150$ V, and it is biased at $I_{CQ} = 2$ mA, determine the values of g_m, r_π, and r_o. (b) Repeat part (a) if $I_{CQ} = 0.5$ mA.

4.2 The transistor parameters are $\beta = 125$ and $V_A = 200$ V. A value of $g_m = 200$ mA/V is desired. Determine the collector current required, and then find r_π and r_o.

4.3 For the circuit in Figure 4.3, the transistor parameters are $\beta = 120$ and $V_A = \infty$, and the circuit parameters are $V_{CC} = 5$ V, $R_C = 4$ kΩ, $R_B = 250$ kΩ, and $V_{BB} = 2.0$ V. (a) Determine the hybrid-π parameter values of g_m, r_π, and r_o. (b) Find the small-signal voltage gain $A_v = v_o/v_s$. (c) If the time-varying output signal is given by $v_o = 0.8 \sin(100t)$ V, what is v_s?

4.4 The nominal quiescent collector current of a transistor is 1.2 mA. If the range of β for this transistor is $80 \leq \beta \leq 120$ and if the quiescent collector current changes by ± 10 percent, determine the range in values for g_m and r_π.

D4.5 For the circuit in Figure 4.3, $\beta = 120$, $V_{CC} = 5$ V, $V_A = 100$ V, and $R_B = 25$ kΩ. (a) Determine V_{BB} and R_C such that $r_\pi = 5.4$ kΩ and the Q-point is in the center of the load line. (b) Find the resulting small-signal voltage gain $A_v = v_o/v_s$.

D4.6 For the circuit in Figure 4.14, $\beta = 100$, $V_A = \infty$, $V_{CC} = 10$ V, and $R_B = 50$ kΩ. (a) Determine V_{BB} and R_C such that $I_{CQ} = 0.5$ mA and the Q-point is in the center of the load line. (b) Find the small-signal parameters g_m, r_π, and r_o. (c) Determine the small-signal voltage gain $A_v = v_o/v_s$.

Section 4.4   Common-Emitter Amplifier

4.7 The parameters of the transistor in the circuit in Figure P4.7 are $\beta = 100$ and $V_A = 100$ V. (a) Find the dc voltages at the base and emitter terminals. (b) Find R_C such that $V_{CEQ} = 3.5$ V. (c) Assuming C_C and C_E act as short circuits, determine the small-signal voltage gain $A_v = v_o/v_s$. (d) Repeat part (c) if a 500 Ω source resistor is in series with the v_s signal source.
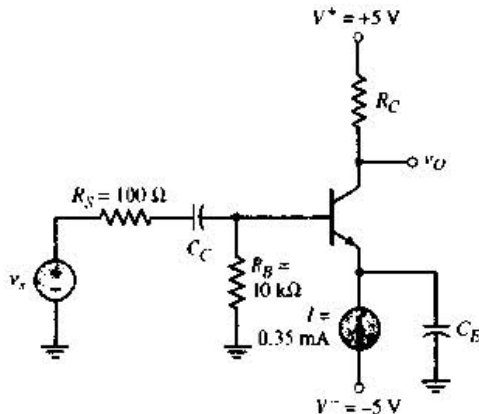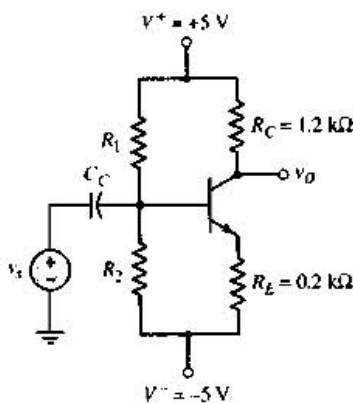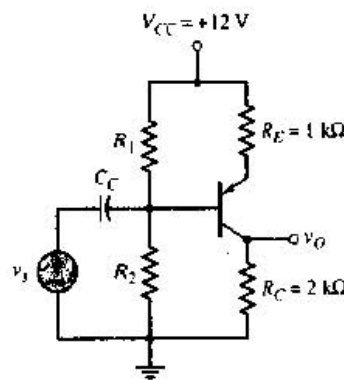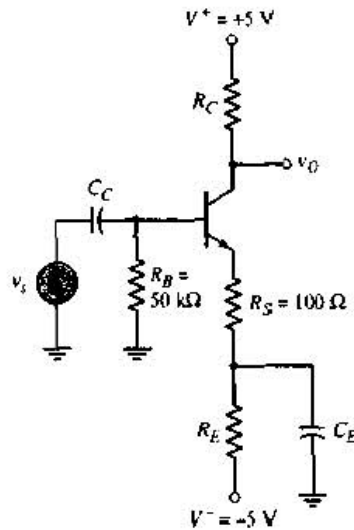

Figure P4.7
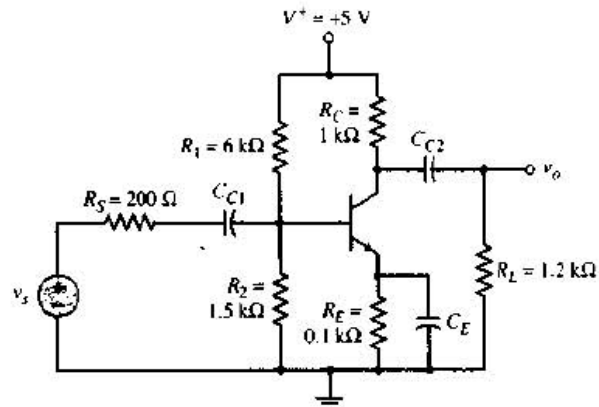
Figure P4.8

4.8 For the circuit in Figure P4.8, the transistor parameters are $\beta = 180$ and $r_o = \infty$. (a) Determine the Q-point values. (b) Find the small-signal hybrid-π parameters. (c) Find the small-signal voltage gain $A_v = v_o/v_s$.

*D4.9 The parameters of the transistor in the circuit in Figure P4.9 are $\beta = 150$ and $V_A = \infty$. (a) Determine R_1 and R_2 to obtain a bias-stable circuit with the Q-point in the center of the load line. (b) Determine the small-signal voltage gain $A_v = v_o/v_s$.

Figure P4.9

Figure P4.10

4.10 Assume that $\beta = 100$, $V_A = \infty$, $R_1 = 10$ kΩ, and $R_2 = 50$ kΩ for the circuit in Figure P4.10. (a) Plot the Q-point on the dc load line. (b) Determine the small-signal voltage gain. (c) Determine the range of voltage gain if each resistor value varies by ± 5 percent.

D4.11 The transistor parameters for the circuit in Figure P4.10 are $\beta = 100$ and $V_A = \infty$. (a) Design the circuit such that it is bias stable and that the Q-point is in the center of the load line. (b) Determine the small-signal voltage gain of the designed circuit.
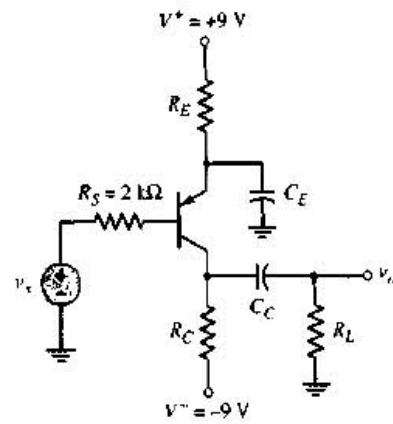
D4.12 For the circuit in Figure P4.12, the transistor parameters are $\beta = 100$ and $V_A = \infty$. Design the circuit such that $I_{CQ} = 0.25\,\text{mA}$ and $V_{CEQ} = 3\,\text{V}$. Find the small-signal voltage gain $A_v = v_o/v_s$. Find the input resistance seen by the signal source v_s.

Figure P4.12   **Figure P4.13**

D4.13 For the circuit in Figure P4.13, the transistor parameters are $\beta = 80$ and $V_A = 80\,\text{V}$. (a) Determine R_E such that $I_{EQ} = 0.75\,\text{mA}$. (b) Determine R_C such that $V_{ECQ} = 7\,\text{V}$. (c) For $R_L = 10\,\text{k}\Omega$, determine the small-signal voltage gain $A_v = v_o/v_s$. (d) Determine the impedance seen by the signal souce v_s.

D4.14 Assume the transistor in the circuit in Figure P4.14 has parameters $\beta = 120$ and $V_A = 100\,\text{V}$. (a) Design the circuit such that $V_{CEQ} = 3.75\,\text{V}$. (b) Determine the small-signal transresistance $R_m = v_o/i_s$.
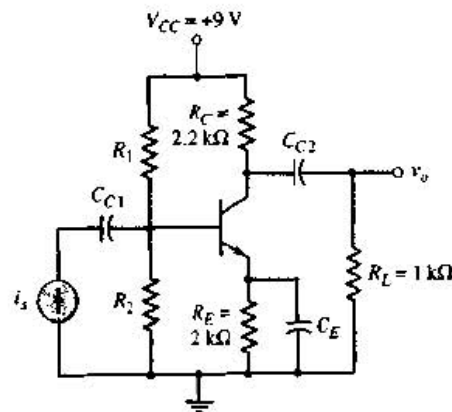

Figure P4.14

D4.15 For transistor parameters $\beta = 65$ and $V_A = 75\,\mathrm{V}$, (a) design the circuit in Figure P4.15 such that the dc voltages at the base and collector terminals are $0.30\,\mathrm{V}$ and $-3\,\mathrm{V}$, respectively. (b) Determine the small-signal transconductance $G_j = i_o/v_s$.
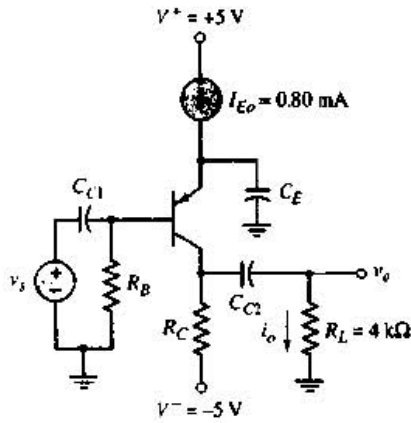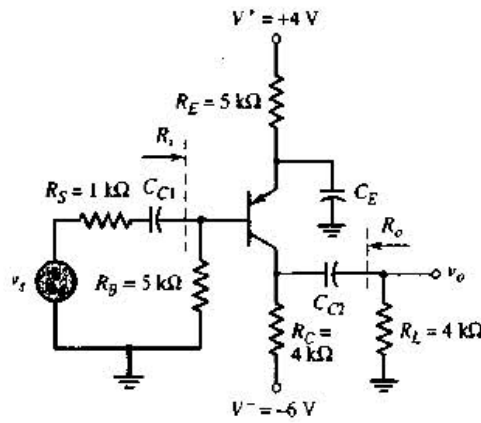

Figure P4.15   **Figure P4.16**

4.16 The transistor in the circuit in Figure P4.16 is a 2N2907A with a nominal dc current gain of $\beta = 100$. Assume the range of h_{fe} is $80 \leq h_{fe} \leq 120$ and the range of h_{oe} is $10 \leq h_{oe} \leq 20\,\mu\mathrm{S}$. For $h_{re} = 0$ determine: (a) the range of small-signal voltage gain $A_v = v_o/v_s$, and (b) the range in the input and output resistances R_i and R_o.

*D4.17 Design a one-transistor common-emitter preamplifier that can amplify a $10\,\mathrm{mV}$ (rms) microphone signal and produce a $0.5\,\mathrm{V}$ (rms) output signal. The source resistance of the microphone is $1\,\mathrm{k}\Omega$.

*4.18 For the transistor in the circuit in Figure P4.18, the parameters are $\beta = 100$ and $V_A = \infty$. (a) Determine the Q-point. (b) Find the small-signal parameters g_m, r_π, and r_o. (c) Find the small-signal voltage gain $A_v = v_o/v_s$ and the small-signal current gain $A_i = i_o/i_s$. (d) Find the input resistances R_{ib} and R_{is}. (e) Repeat part (c) if a $1\,\mathrm{k}\Omega$ source resistor is in series with the v_s signal source.
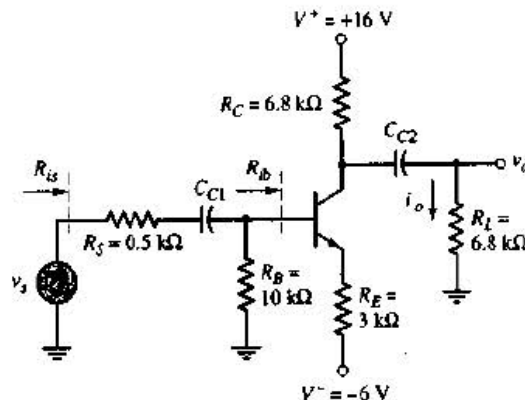

Figure P4.18

4.19 If the collector of a transistor is connected to the base terminal, the transistor continues to operate in the forward-active mode, since the B–C junction is not reverse

biased. Determine the small-signal resistance, $r_z = v_{ze}/i_c$, of this two-terminal device in terms of g_m, r_π, and r_o.

D4.20   Design an amplifier with the configuration similar to that shown in Figure 4.28. The source resistance is $R_S = 100\,\Omega$ and the voltage gain should be approximately −10. The total power dissipated in the circuit should be no more than approximately 0.12 mW.

D4.21   An ideal signal voltage source is given by $v_s = 5\sin(5000t)$ (mV). The peak current that can be supplied by this source is 0.2 μA. The desired output voltage across a 10 kΩ load resistor is $v_o = 100\sin(5000t)$ (mV). Design a one-transistor common-emitter amplifier to meet this specification.

*D4.22   Design a bias-stable common-emitter circuit that has a minimum open-circuit small-signal voltage gain of $|A_v| = 10$. The circuit is to be biased from a single power supply $V_{CC} = 10$ V that can supply a maximum current of 1 mA. The available transistors are pnp's with $\beta = 80$ and $V_A = \infty$. Minimize the number of capacitors required in the circuit.

*D4.23   Design a common-emitter circuit whose output is capacitively coupled to a load resistor $R_L = 10\,k\Omega$. The minimum small-signal voltage gain is to be $|A_v| = 20$. The circuit is to be biased at ±5 V and each voltage source can supply a maximum of 0.5 mA. The parameters of the available transistors are $\beta = 120$ and $V_A = \infty$.

Section 4.5   AC Load Line Analysis

4.24   For the circuit in Figure P4.10 with circuit and transistor parameters as described in Problem 4.10, determine the maximum undistorted swing in the output voltage if the total instantaneous E–C voltage is to remain in the range $1 \le v_{EC} \le 11$ V.

4.25   For the circuit in Figure P4.12, let $\beta = 100$, $V_A = \infty$, $R_E = 12.9\,k\Omega$, and $R_C = 6\,k\Omega$. Determine the maximum undistorted swing in the output voltage if the total instantaneous C–E voltage is to remain in the range $1 \le v_{CE} \le 9$ V and if the total instantaneous collector current is to remain greater or equal to 50 μA.

4.26   Consider the circuit in Figure P4.7 with transistor parameters given in Problem 4.7. Assume $R_C = 6\,k\Omega$. (a) Determine the maximum undistorted swing in the output voltage if the total instantaneous C–E voltage is to remain in the range $0.5 \le v_{CE} \le 4.5$ V. (b) Using the results of part (a), determine the range of collector current.

4.27   Consider the circuit in Figure P4.15. Let $\beta = 100$, $V_A = \infty$, $R_B = 10\,k\Omega$, and $R_C = 4\,k\Omega$. Determine the maximum undistorted swing in the output current i_o if the total instantaneous collector current is $i_C \ge 0.08$ mA and the total instantaneous E–C voltage is in the range $1 \le v_{EC} \le 9$ V.

4.28   Consider the circuit in Figure P4.18 with transistor parameters described in Problem 4.18. Determine the maximum undistorted swing in the output current i_C if the total instantaneous collector current is $i_C \ge 0.1$ mA and the total instantaneous C–E voltage is in the range $1 \le v_{CE} \le 21$ V.

*D4.29   For the circuit in Figure P4.14, the transistor parameters are $\beta = 150$ and $V_A = \infty$. Design a bias-stable circuit to achieve the maximum undistorted swing in the output voltage if the total instantaneous C–E voltage is to remain in the range $1 \le v_{CE} \le 8$ V.

*RD4.30   In the circuit in Figure P4.8 with transistor parameters $\beta = 180$ and $V_A = \infty$, redesign the bias resistors R_1 and R_2 to achieve maximum symmetrical swing in the output voltage and to maintain a bias-stable circuit. The total instantaneous C–E volt-

age is to remain in the range $0.5 \leq v_{CE} \leq 4.5\,V$ and the total instantaneous collector current is to be $i_C \geq 0.25\,mA$.

4.31 For the circuit in Figure P4.16, the transistor parameters are $\beta = 100$ and $V_A = \infty$. (a) Determine the maximum undistorted swing in the output voltage if the total instantaneous E–C voltage is to remain in the range $1 \leq v_{EC} \leq 9\,V$. (b) Using the results of part (a), determine the range of collector current.

Section 4.6   Common-Collector (Emitter-Follower) Amplifier

4.32 The transistor parameters for the circuit in Figure P4.32 are $\beta = 180$ and $V_A = \infty$. (a) Find I_{CQ} and V_{CEQ}. (b) Plot the dc and ac load lines. (c) Calculate the small-signal voltage gain. (d) Determine the input and output resistances R_{ib} and R_o.
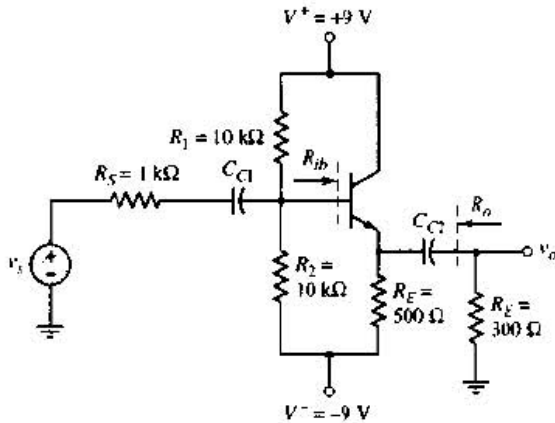

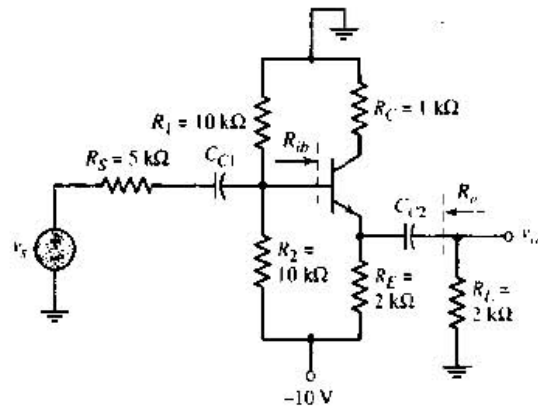**Figure P4.32**   **Figure P4.33**

4.33 Consider the circuit in Figure P4.33. The transistor parameters are $\beta = 120$ and $V_A = \infty$. Repeat parts (a)–(d) of Problem 4.32.

***D4.34** For the circuit in Figure P4.34, the transistor current gain is $\beta = 80$ and $R_L = 500\,\Omega$. Design the circuit to obtain a small-signal current gain of $A_i = i_o/i_i = 8$. Let $V_{CC} = 10\,V$. Find R_1, R_2, and the output resistance R_o if $R_E = 500\,\Omega$. What is the current gain if $R_L = 2000\,\Omega$?
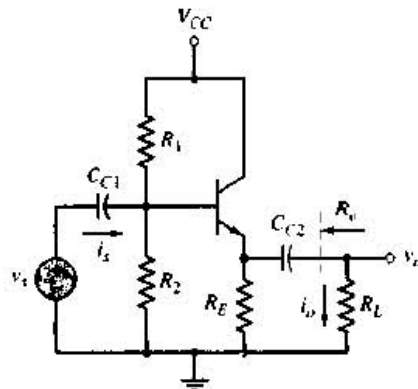

Figure P4.34

D4.35 Design an emitter-follower circuit with the configuration shown in Figure 4.44 such that the input resistance R_i, as defined in Figure 4.46, is 120 kΩ. Assume transistor parameters of $\beta = 120$ and $V_A = \infty$. Let $V_{CC} = 5$ V and $R_E = 2$ kΩ. Find new values of R_1 and R_2. The Q-point should be approximately in the center of the load line.

D4.36 (a) For the emitter-follower circuit in Figure P4.34, assume $V_{CC} = 24$ V, $\beta = 75$, and $A_i = i_o/i_s = 8$. Design the circuit to drive an 8 Ω load. (b) Determine the maximum undistorted swing in the output voltage. (c) Determine the output resistance R_o.

4.37 For the circuit shown in Figure P4.37, let $V_{CC} = 5$ V, $R_L = 4$ kΩ, $R_E = 3$ kΩ, $R_1 = 60$ kΩ, and $R_2 = 40$ kΩ. The transistor parameters are $\beta = 50$ and $V_A = 80$ V. (a) Determine I_{CQ} and V_{ECQ}. (b) Plot the dc and ac load lines. (c) Determine $A_v = v_o/v_s$ and $A_i = i_o/i_s$. (d) Determine R_{ib} and R_o. (e) Determine the range in current gain if each resistor value varies by ± 5 percent.
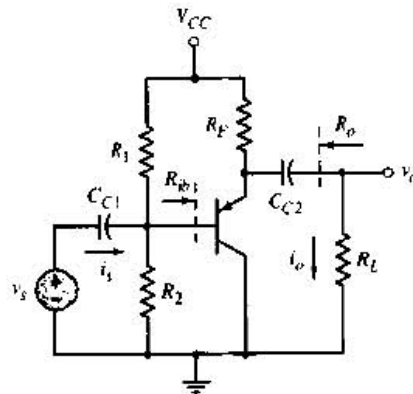

Figure P4.37

*D4.38 The output of an amplifier can be represented by $v_s = 4\sin \omega t$(V) and $R_S = 4$ kΩ. An emitter-follower circuit, with the configuration shown in Figure 4.49, is to be designed such that the output signal does not vary by more than 5 percent when a load in the range $R_L = 4$ to 10 kΩ is connected to the output. The transistor current gain is in the range $90 \le \beta \le 130$ and the Early voltage is $V_A = \infty$. For your design, find the minimum and maximum possible value of the output voltage.

4.39 (a) In the circuit shown in Figure P4.39, determine the range in small-signal voltage gain $A_v = v_o/v_s$ and current gain $A_i = i_o/i_s$ if β is in the range $75 \le \beta \le 150$.
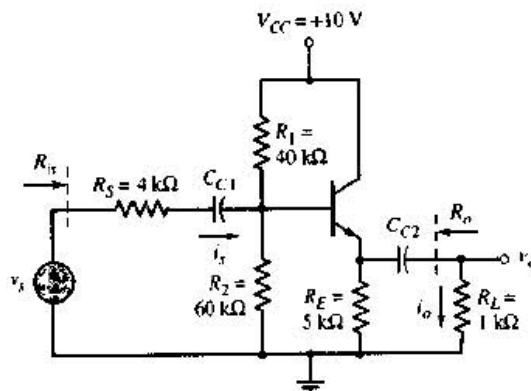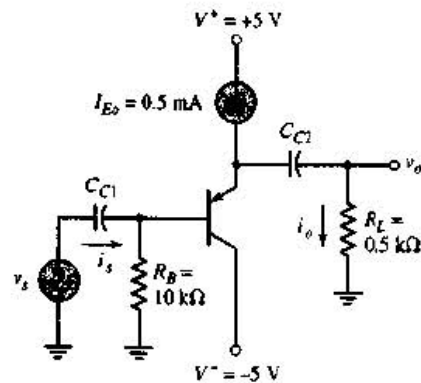

Figure P4.39

Figure P4.40

(b) Repeat part (a) if a $5\,k\Omega$ source resistor is in series with the v_s signal source.

4.40 For the transistor in Figure P4.40, $\beta = 80$ and $V_A = 150\,V$. (a) Determine the dc voltages at the base and emitter terminals. (b) Calculate the small-signal parameters g_m, r_π, and r_o. (c) Determine the small-signal voltage gain and current gain. (d) Repeat part (c) if a $2\,k\Omega$ source resistor is in series with the v_s signal source.

4.41 Consider the circuit shown in Figure P4.40. The transistor current gain is in the range $100 \le \beta \le 180$ and the Early voltage is $V_A = 150\,V$. Determine the range in small-signal voltage gain if the load resistance varies from $R_L = 0.5\,k\Omega$ to $R_L = 500\,k\Omega$.

*D4.42 For the transistor in Figure P4.42, the parameters are $\beta = 100$ and $V_A = \infty$. (a) Design the circuit such that $I_{EQ} = 1\,mA$ and the Q-point is in the center of the dc load line. (b) If the peak-to-peak sinusoidal output voltage is $4\,V$, determine the peak-to-peak sinusoidal signals at the base of the transistor and the peak-to-peak value of v_s. (c) If a load resistor $R_L = 1\,k\Omega$ is connected to the output through a coupling capacitor, determine the peak-to-peak value in the output voltage, assuming v_s is equal to the value determined in part (b).
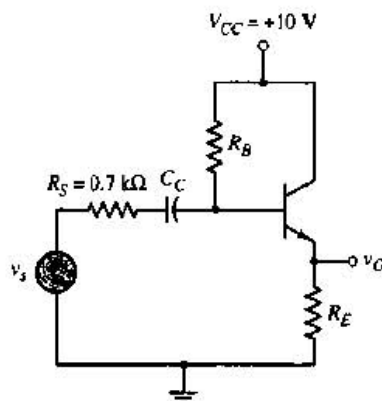

Figure P4.42

*D4.43 An emitter-follower amplifier, with the configuration shown in Figure 4.49, is to be designed such that an audio signal given by $v_s = 5\sin(3000t)$ V but with a source resistance of $R_S = 10\,k\Omega$ can drive a small speaker. Assume the supply voltages are $V^+ = +12\,V$ and $V^- = -12\,V$. The load, representing the speaker, is $R_L = 12\,\Omega$. The amplifier should be capable of delivering approximately $1\,W$ of average power to the load. What is the signal power gain of your amplifier?

Section 4.7   Common-Base Amplifier

4.44 For the circuit shown in Figure P4.44, $\beta = 125$, $V_A = \infty$, $V_{CC} = 18\,V$, $R_L = 4\,k\Omega$, $R_E = 3\,k\Omega$, $R_C = 4\,k\Omega$, $R_1 = 25.6\,k\Omega$, and $R_2 = 10.4\,k\Omega$. The input signal is a current. (a) Determine the Q-point values. (b) Determine the transresistance $R_m = v_o/i_s$. (c) Find the small-signal voltage gain $A_v = v_o/v_s$.
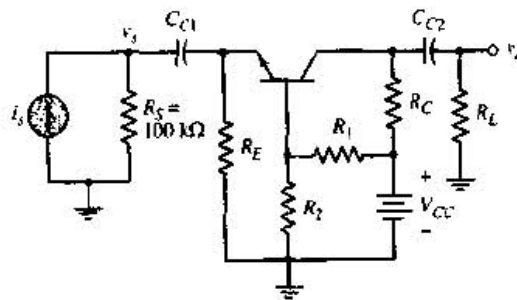

Figure P4.44

*RD4.45 For the common-base circuit shown in Figure P4.44, let $\beta = 100$, $V_A = \infty$, $V_{CC} = 12\,V$, $R_L = 12\,k\Omega$, and $R_E = 500\,\Omega$. (a) Redesign the circuit such that the small-signal voltage gain is $A_v = v_o/v_i = 10$. (b) What are the Q-point values? (c) What is the small-signal voltage gain if R_2 is bypassed by a large capacitor?

*D4.46 A photodiode in an optical transmission system, such as shown in Figure 1.35, can be modeled as a Norton equivalent circuit with i_s in parallel with R_S as shown in Figure P4.44. Assume that the current source is given by $i_s = 2.5 \sin \omega t\,\mu A$ and $R_S = 50\,k\Omega$. Design the common-base circuit of Figure P4.44 such that the output voltage is $v_o = 5 \sin \omega t\,mV$. Assume transistor parameters of $\beta = 120$ and $V_A = \infty$. Let $V_{CC} = 5\,V$.

4.47 For the circuit shown in Figure P4.47, the transistor parameters are $\beta = 100$ and $V_A = \infty$. (a) Determine the dc voltages at the collector, base, and emitter terminals. (b) Determine the small-signal voltage gain $A_v = v_o/v_s$. (c) Find the input resistance R_i.

4.48 In the common-base circuit shown in Figure P4.48, the transistor is a 2N2907A, with a nominal dc current gain of $\beta = 80$. (a) Determine I_{CQ} and V_{ECQ}. (b) Using the h-parameters (assuming $h_{re} = 0$), determine the range in small-signal voltage gain $A_v = v_o/v_s$. (c) Determine the range in input and output resistances R_i and R_o.
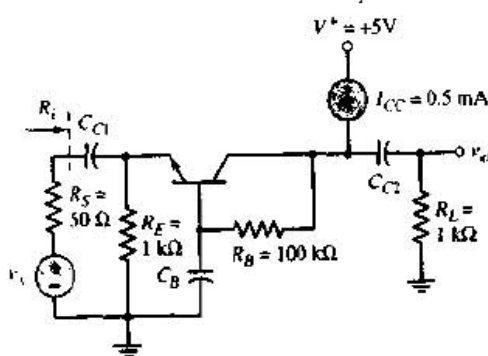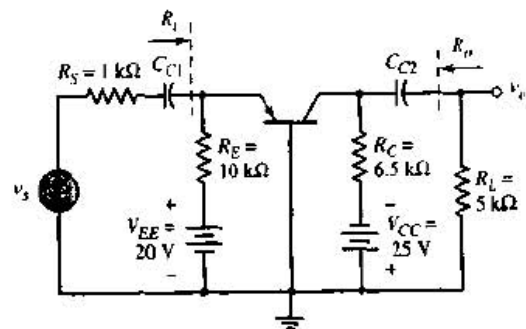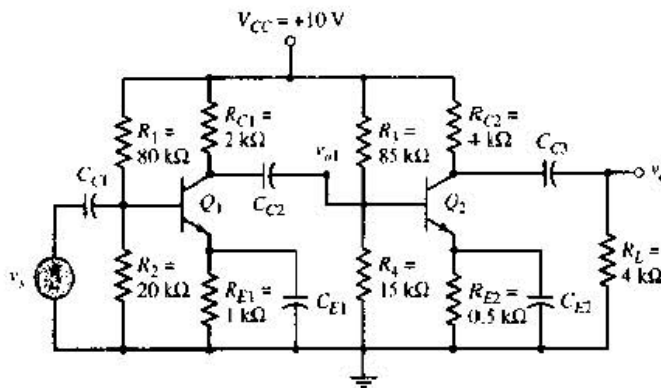

Figure P4.47

Figure P4.48

*D4.49 In the circuit of Figure P4.48, let $V_{EE} = V_{CC} = 5\,V$, $\beta = 100$, $V_A = \infty$, $R_L = 1\,k\Omega$, and $R_S = 0$. (a) Design the circuit such that the small-signal voltage gain is $A_v = v_o/v_s = 25$ and $V_{ECQ} = 3\,V$. (b) What are the values of the small-signal parameters g_m, r_π, and r_o?

Section 4.9 Multistage Amplifiers

*4.50 The parameters for each transistor in the circuit shown in Figure P4.50 are $\beta = 100$ and $V_A = \infty$. (a) Determine the small-signal parameters g_m, r_π, and r_o for both transistors. (b) Determine the small-signal voltage gain $A_{v1} = v_{o1}/v_s$, assuming v_{o1} is connected to an open circuit, and determine the gain $A_{v2} = v_o/v_{o1}$. (c) Determine the overall small-signal voltage gain $A_v = v_o/v_s$. Compare the overall gain with the product $A_{v1} \cdot A_{v2}$, using the values calculated in part (b).

Figure P4.50

*4.51 Consider the circuit shown in Figure P4.51 with transistor parameters $\beta = 120$ and $V_A = \infty$. (a) Determine the small-signal parameters g_m, r_π, and r_o for both transistors. (b) Plot the dc and ac load lines for both transistors. (c) Determine the overall small-signal voltage gain $A_v = v_o/v_s$. (d) Determine the input resistance R_{is} and the output resistance R_o. (e) Determine the maximum undistorted swing in the output voltage.
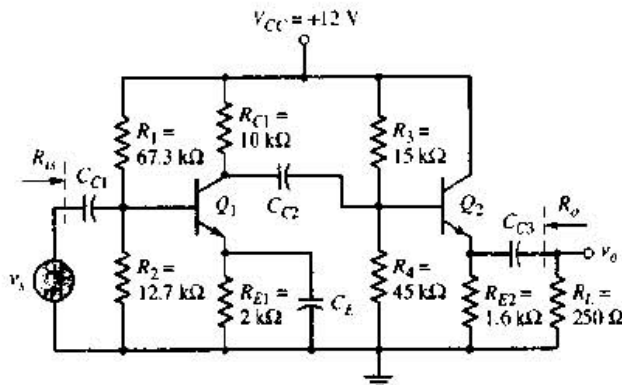
Figure P4.51

4.52 For the circuit shown in Figure P4.52, assume transistor parameters of $\beta = 100$ and $V_A = \infty$. (a) Determine the dc collector current in each transistor. (b) Find the small-signal voltage gain $A_v = v_o/v_s$. (c) Determine the input and output resistances R_{ib} and R_o.
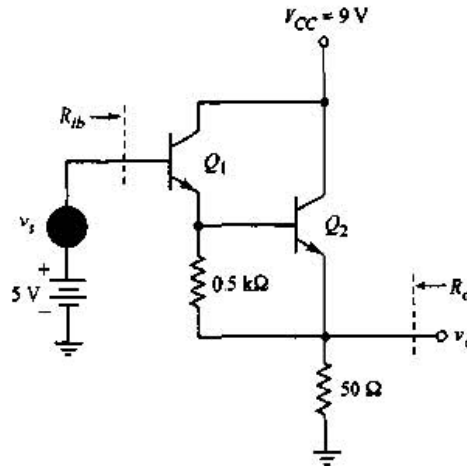

Figure P4.52

*4.53 For each transistor in Figure P4.53, the parameters are $\beta = 100$ and $V_A = \infty$. (a) Determine the Q-point values for both Q_1 and Q_2. (b) Determine the overall small-signal voltage gain $A_v = v_o/v_s$. (c) Determine the input and output resistances R_{is} and R_o.
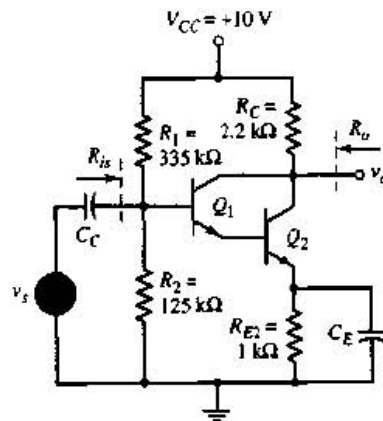
Figure P4.53
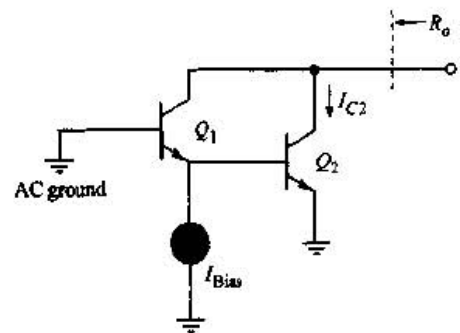
Figure P4.54

4.54 An equivalent ac circuit of a Darlington pair configuration is shown in Figure P4.54. (a) Derive the expression for the output resistance R_o as a function of I_{Bias} and I_{C2}. Take into account the transistor output resistances r_{o1} and r_{o2}. (b) Assuming transistor parameters of $\beta = 100$ and $V_A = 100 \text{V}$, determine R_o for (i) $I_{C2} = I_{Bias} = 1 \text{mA}$ and (ii) $I_{C2} = 1 \text{mA}$, $I_{Bias} = 0$.

Section 4.10   Power Considerations

4.55 The transistor in the circuit shown in Figure 4.25 has parameters $\beta = 100$ and $V_A = 100$ V. (a) Determine the average power dissipated in the transistor and R_C, for $v_s = 0$. (b) Determine the maximum undistorted signal power that can be delivered to R_C.

4.56 Consider the circuit shown in Figure 4.35. The transistor parameters are $\beta = 120$ and $r_o = \infty$. (a) Calculate the average power dissipated in the transistor, R_E, and R_C, for $v_s = 0$. (b) Determine the maximum undistorted signal power that can be delivered to R_L.

4.57 For the circuit shown in Figure 4.40, use the circuit and transistor parameters described in Example 4.8. (a) Calculate the average power dissipated in the transistor, R_E, and R_C, for $v_s = 0$. (b) Determine the maximum signal power that can be delivered to R_L. What are the signal powers dissipated in R_E and R_C, and what is the average power dissipated in the transistor in this case?

4.58 For the circuit shown in Figure 4.51, the transistor parameters are $\beta = 100$ and $V_A = 100$ V, and the source resistor is $R_S = 0$. Determine the maximum undistorted signal power that can be delivered to R_L if: (a) $R_L = 1$ kΩ, and (b) $R_L = 10$ kΩ.

4.59 Consider the circuit shown in Figure 4.58 with parameters given in Exercise 4.25. (a) Calculate the average power dissipated in the transistor and R_C, for $v_s = 0$. (b) Determine the maximum undistorted signal power that can be delivered to R_L, and the resulting average power dissipated in the transistor and R_C.

COMPUTER SIMULATION PROBLEMS

4.60 Consider Example 4.2. Using a computer simulation analysis, investigate the effect of the Early voltage on the small-signal characteristics of the circuit.

4.61 The circuit in Figure P4.61 can be used to simulate the circuit shown in Figure 4.37(a). Assume Early voltages of $V_A = 60$ V. (a) Plot the voltage transfer characteristics, v_O versus V_{BB}, over the range $0 \leq V_{BB} \leq 1$ V. (b) Set V_{BB} such that the dc value of the output voltage is $v_O \cong 2.5$ V. Determine the small-signal voltage gain at this Q-point. Compare the results to those found in Example 4.7.

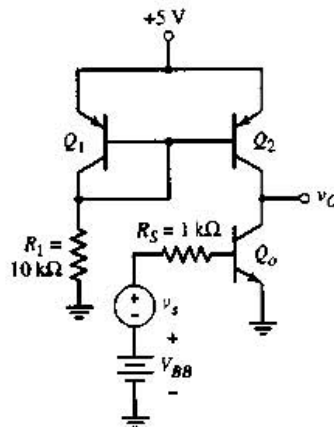**4.62** Verify the results of Example 4.8 with a computer simulation analysis.

Figure P4.61

4.63   Verify the input and output resistances of the emitter-follower circuit described in Example 4.11.

4.64   Perform a computer simulation analysis of the common-base circuit described in Exercise 4.25. In addition, assume $V_A = 80$ V and determine the output resistance looking into the collector of the transistor. How does this value compare to $r_o = V_A/I_{CQ}$?

DESIGN PROBLEMS

[Note: Each design should be correlated with a computer simulation.]

*D4.65   Design a common-emitter circuit with a small-signal voltage gain of $|A_v| = 50$ while driving a load $R_L = 5$ kΩ. The source signal is $v_s = 0.02 \cos \omega t$ V and the source resistance is $R_S = 1$ kΩ. Bias the circuit at ±5 V, and use transistors with a maximum collector current rating of 10 mA and current gains in the range $80 \leq \beta \leq 150$.

*D4.66   For the circuit in Figure P4.37, let $V_{CC} = 10$ V and $R_L = 1$ kΩ. The transistor parameters are $\beta = 120$ and $V_A = \infty$. (a) Design the circuit such that the current gain is $A_i = 18$. (b) Determine R_{ib} and R_o. (c) Find the maximum undistorted swing in the output voltage.

*D4.67   Design a common-base amplifier with the general configuration shown in Figure 4.58. The available power supplies are ±10 V. The output resistance of the signal source is 50 Ω, and the input resistance of the amplifier should match this value. The output resistance is $R_L = 2$ kΩ, and the output voltage is to have the largest possible symmetrical swing. In order to maintain linearity, the peak value of the B–E signal voltage should be limited to 15 mV. Assume that transistors with $\beta = 150$ are available. Specify the current and power ratings of the transistors.

*D4.68   A microphone puts out a peak voltage of 1 mV and has an output resistance of 10 kΩ. Design an amplifier system to drive an 8 Ω speaker, producing 2 W of signal power. Use a 24 V power supply to bias the circuit. Assume a current gain of $\beta = 50$ for the available transistors. Specify the current and power ratings of the transistors.

*D4.69   Redesign the two-stage amplifier in Figure 4.60 such that a symmetrical sine wave with a peak value of ±3 V can be obtained at the output. The load resistor is still $R_L = 5$ kΩ. To avoid distortion, the minimum C–E voltage should be at least 1 V and the maximum C–E voltage should be no more than 9 V. Assume the transistor current gains are $\beta = 100$. If the Early voltage for each transistor is $V_A = \infty$, calculate the resulting overall small-signal voltage gain. State the value of each resistor and the quiescent values of each transistor.

5

The Field-Effect Transistor

5.0 PREVIEW

In the last two chapters, we looked at the bipolar junction transistor and BJT circuits. In this chapter, we introduce the second major type of transistor, the field-effect transistor (FET). There are two general classes of FETs: the metal-oxide-semiconductor FET (MOSFET) and the junction FET (JFET). The MOSFET has led to the second electronics revolution in the 1970s and 1980s, in which the microprocessor has made possible powerful desktop computers and sophisticated hand-held calculators. The MOSFET can be made very small, so high-density VLSI circuits and high-density memories are possible.

We begin the chapter with a look at the physical structure and operation of the MOSFET. The current–voltage characteristics of the device are developed, and then the dc analysis and design of MOSFET circuits are considered. We will see how the MOSFET can be used in place of resistors in a circuit, so that circuits containing only MOSFETs can be designed.

In the junction FET, the junction may be a pn junction, which forms a pn JFET, or a Schottky barrier junction, which forms a metal-semiconductor FET, or MESFET. MESFETs are used in very high speed or high-frequency applications, such as microwave amplifiers. Since JFETs are specialized devices, the discussion of JFET circuits is brief.

Although the emphasis of this chapter is on dc circuits, we discuss how the FET can be used in switch, digital, and linear amplifier applications. A major goal of this chapter is to enable the reader to become very familiar and comfortable with the MOSFET properties and to be able to quickly analyze and design the dc response of FET circuits.

5.1 MOS FIELD-EFFECT TRANSISTOR

The metal-oxide-semiconductor field-effect transistor (MOSFET) became a practical reality in the 1970s. The MOSFET, compared to BJTs, can be made very small (that is, it occupies a very small area on an IC chip). Since digital circuits can be designed using only MOSFETs, with essentially no resistors or diodes required, high-density VLSI circuits, including microprocessors and memories, can be fabricated. The MOSFET has made possible the hand-held calculator and

the powerful personal computer. MOSFETs can also be used in analog circuits, as we will see in the next chapter.

In the MOSFET, the current is controlled by an electric field applied perpendicular to both the semiconductor surface and to the direction of current. The phenomenon used to modulate the conductance of a semiconductor, or control the current in a semiconductor, by applying an electric field perpendicular to the surface is called the **field effect**. Again, the basic transistor principle is that the voltage between two terminals controls the current through the third terminal.

In the following two sections, we will discuss the various types of MOSFETs, develop the $i-v$ characteristics, and then consider the dc biasing of various MOSFET circuit configurations. After studying these sections, you should be familiar and comfortable with the MOSFET and MOSFET circuits.

5.1.1   Two-Terminal MOS Structure

The heart of the MOSFET is the metal-oxide-semiconductor capacitor shown in Figure 5.1. The metal may be aluminum or some other type of metal. In many cases, the metal is replaced by a high-conductivity polycrystalline silicon layer deposited on the oxide. However, the term metal is usually still used in referring to MOSFETs. In the figure, the parameter t_{ox} is the thickness of the oxide and ϵ_{ox} is the oxide permittivity.
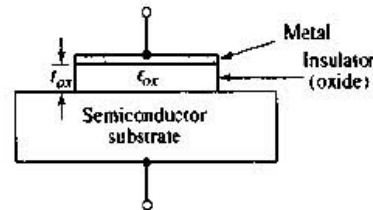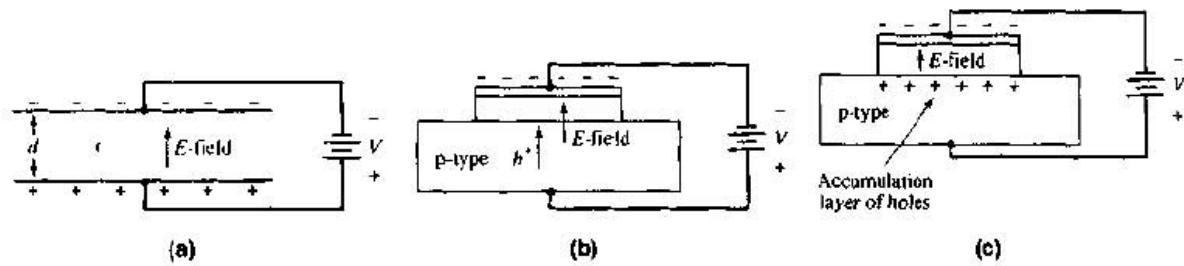

Figure 5.1   The basic MOS capacitor structure

The physics of the MOS structure can be explained with the aid of a simple parallel-plate capacitor.[1] Figure 5.2(a) shows a parallel-plate capacitor with the top plate at a negative voltage with respect to the bottom plate. An insulator material separates the two plates. With this bias, a negative charge exists on the top plate, a positive charge exists on the bottom plate, and an electric field is induced between the two plates, as shown.

A MOS capacitor with a p-type semiconductor substrate is shown in Figure 5.2(b). The top metal terminal, also called the gate, is at a negative voltage with respect to the semiconductor substrate. From the example of the parallel-plate capacitor, we can see that a negative charge will exist on the top metal plate and an electric field will be induced in the direction shown in the figure. If the electric field penetrates the semiconductor, the holes in the p-type semiconductor will experience a force toward the oxide-semiconductor inter-

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[1] The capacitance of a parallel plate capacitor, neglecting fringing fields, is $C = \epsilon A/d$, where A is the area of one plate, d is the distance between plates, and ϵ is the permittivity of the medium between the plates.
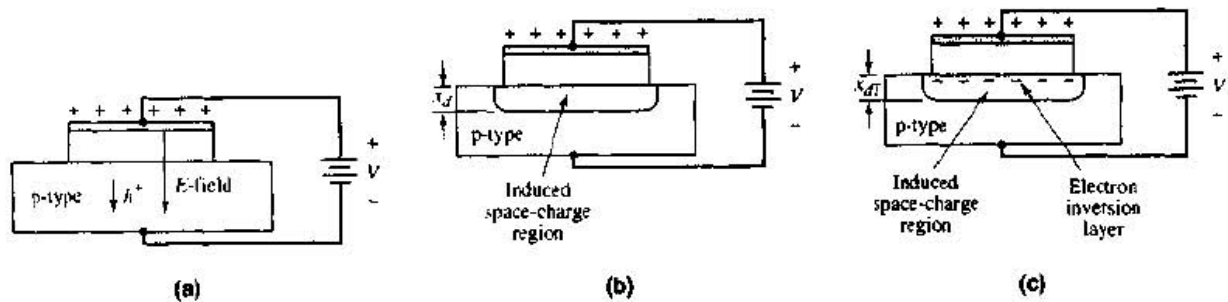
Figure 5.4 The MOS capacitor with n-type substrate for: (a) a positive gate bias, (b) a moderate negative bias, and (c) a larger negative bias

direction shown. In this situation, an accumulation layer of electrons is induced in the n-type semiconductor.

Figure 5.4(b) shows the case when a negative voltage is applied to the gate terminal. A positive space-charge region is induced in the n-type substrate by the induced electric field. When a larger negative voltage is applied, a region of positive charge is created at the oxide-semiconductor interface, as shown in Figure 5.4(c). This region of minority carrier holes is called a **hole inversion layer**. The magnitude of the positive charge in the inversion layer is a function of the applied gate voltage.

The term **enhancement mode** means that a voltage must be applied to the gate to create an inversion layer. For the MOS capacitor with a p-type substrate, a positive gate voltage must be applied to create the electron inversion layer; for the MOS capacitor with an n-type substrate, a negative gate voltage must be applied to create the hole inversion layer.

5.1.2   n-Channel Enhancement-Mode MOSFET

We will now apply the concepts of an inversion layer charge in a MOS capacitor to create a transistor.

Transistor Structure

Figure 5.5(a) shows a simplified cross section of a MOS field-effect transistor. The gate, oxide, and p-type substrate regions are the same as those of a MOS capacitor. In addition, we now have two n-regions, called the **source terminal** and **drain terminal**. The current in a MOSFET is the result of the flow of charge in the inversion layer, also called the **channel region**, adjacent to the oxide-semiconductor interface.

The channel length L and channel width W are defined on the figure. The channel length of a typical integrated circuit MOSFET is less than 1 μm (10^{-6} m), which means that MOSFETs are small devices. The oxide thickness t_{ox} is typically on the order of 400 angstroms, or less.

The diagram in Figure 5.5(a) is a simplified sketch of the basic structure of the transistor. Figure 5.5(b) shows a more detailed cross section of a MOSFET fabricated into an integrated circuit configuration. A thick oxide, called the **field oxide**, is deposited outside the area in which the metal interconnect lines are formed. The gate material is usually heavily doped polysilicon. Even though the actual structure of a MOSFET may be fairly complex, the simplified diagram may be used to develop the basic transistor characteristics.
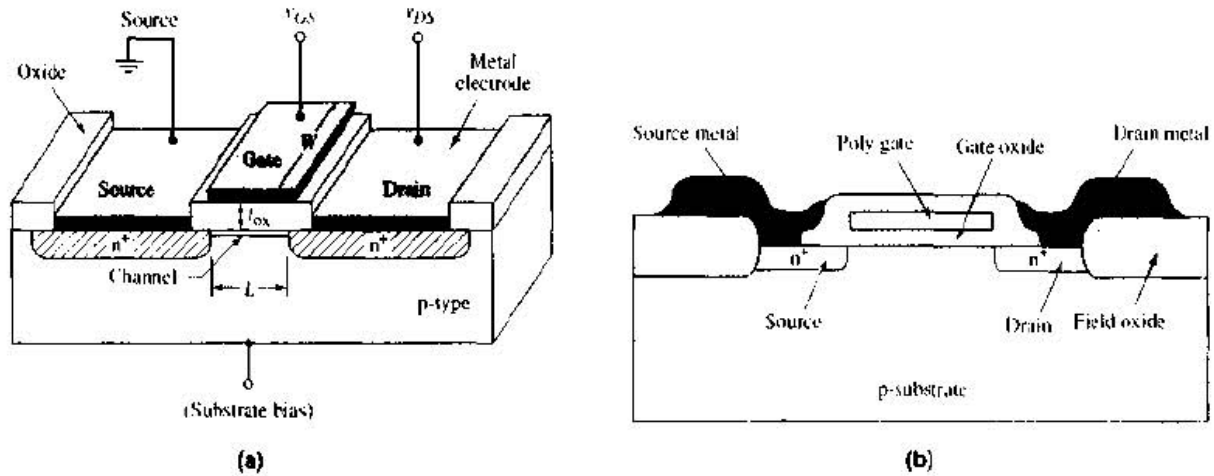
Figure 5.5 (a) Schematic diagram of an n-channel enhancement mode MOSFET and (b) an n-channel MOSFET, showing the field oxide and polysilicon gate

Basic Transistor Operation

With zero bias applied to the gate, the source and drain terminals are separated by the p-region, as shown in Figure 5.6(a). This is equivalent to two back-to-back diodes, as shown in Figure 5.6(b). The current in this case is essentially zero. If a large enough positive gate voltage is applied, an electron inversion layer is created at the oxide–semiconductor interface and this layer "connects" the n-source to the n-drain, as shown in Figure 5.6(c). A current can then be generated between the source and drain terminals. Since a voltage must be applied to the gate to create the inversion charge, this transistor is called an **enhancement-mode MOSFET**. Also, since the carriers in the inversion layer are electrons, this device is also called an **n-channel MOSFET**.

The source terminal supplies carriers that flow through the channel, and the drain terminal allows the carriers to drain from the channel. For the n-channel MOSFET, or **NMOS transistor**, electrons flow from the source to the drain with an applied drain-to-source voltage, which means the conventional
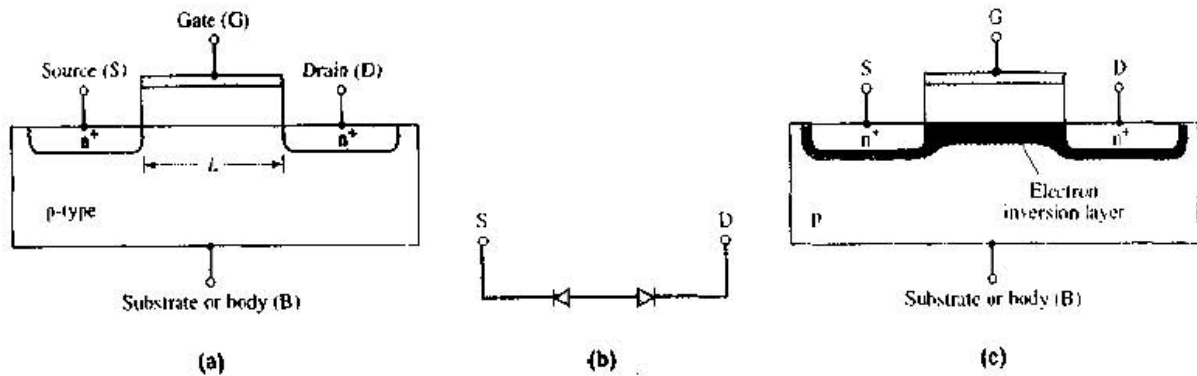
Figure 5.6 (a) Cross section of the n-channel MOSFET prior to the formation of an electron inversion layer, (b) equivalent back-to-back diodes between source and drain when the transistor is in cutoff, and (c) cross section after the formation of an electron inversion layer

current enters the drain and leaves the source. The magnitude of the current is a function of the amount of charge in the inversion layer, which in turn is a function of the applied gate voltage. Since the gate terminal is separated from the channel by an oxide or insulator, there is no gate current. Similarly, since the channel and substrate are separated by a space-charge region, there is essentially no current through the substrate.

5.1.3   Ideal MOSFET Current–Voltage Characteristics

The **threshold voltage** of the n-channel MOSFET is denoted as V_{TN} and is defined[2] as the applied gate voltage needed to create an inversion charge in which the density is equal to the concentration of majority carriers in the semiconductor substrate. In simple terms, we can think of the threshold voltage as the gate voltage required to "turn on" the transistor.

For the n-channel enhancement-mode MOSFET, the threshold voltage is positive because a positive gate voltage is required to create the inversion charge. If the gate voltage is less than the threshold voltage, the current in the device is essentially zero. If the gate voltage is greater than the threshold voltage, a drain-to-source current is generated as the drain-to-source voltage is applied. The gate and drain voltages are measured with respect to the source.

Figure 5.7(a) shows an n-channel enhancement-mode MOSFET with the source and substrate terminals connected to ground. The gate-to-source voltage is less than the threshhold voltage, and there is a small drain-to-source voltage. With this bias configuration, there is no electron inversion layer, the drain-to-substrate pn junction is reverse biased, and the drain current is zero (neglecting pn junction leakage currents).

Figure 5.7(b) shows the same MOSFET with an applied gate voltage greater than the threshold voltage. In this situation, an electron inversion layer is created and, when a small drain voltage is applied, electrons in the inversion layer flow from the source to the positive drain terminal. The conven-
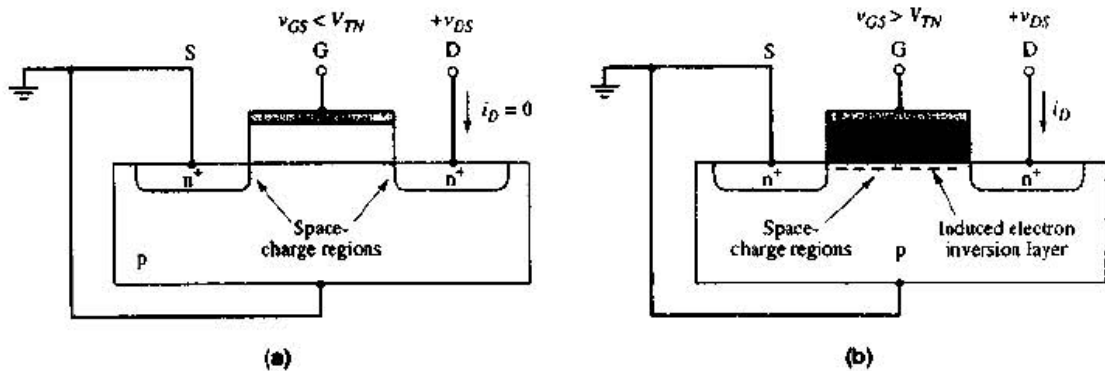
Figure 5.7   The n-channel enhancement-mode MOSFET (a) with an applied gate voltage $v_{GS} < V_{TN}$, and (b) with an applied gate voltage $v_{GS} > V_{TN}$

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[2]The usual notation for threshold voltage is V_T. However, since we have defined the thermal voltage as $V_T = kT/q$, we will use V_{TN} for the threshold voltage of the n-channel device.

tional current enters the drain terminal and leaves the source terminal. Note that a positive drain voltage creates a reverse-biased drain-to-substrate pn junction, so current flows through the channel region and not through a pn junction.

The i_D versus v_{DS} characteristics for small values of v_{DS} are shown in Figure 5.8. When $v_{DS} < V_{TN}$, the drain current is zero. When v_{GS} is greater than V_{TN}, the channel inversion charge is formed and the drain current increases with v_{DS}. Then, with a larger gate voltage, a larger inversion charge density is created, and the drain current is greater for a given value of v_{DS}.

Figure 5.9(a) shows the basic MOS structure for $v_{GS} > V_{TN}$ and a small applied v_{DS}. In the figure, the thickness of the inversion channel layer qualitatively indicates the relative charge density, which for this case is essentially constant along the entire channel length. The corresponding i_D versus v_{DS} curve is also shown in the figure.

Figure 5.9(b) shows the situation when v_{DS} increases. As the drain voltage increases, the voltage drop across the oxide near the drain terminal decreases, which means that the induced inversion charge density near the drain also decreases. The incremental conductance of the channel at the drain then decreases, which causes the slope of the i_D versus v_{DS} curve to decrease. This effect is shown in the i_D versus v_{DS} curve in the figure.

As v_{DS} increases to the point where the potential difference across the oxide at the drain terminal is equal to V_{TN}, the induced inversion charge density at the drain terminal is zero. This effect is shown schematically in Figure 5.9(c). For this condition, the incremental channel conductance at the drain is zero, which means that the slope of the i_D versus v_{DS} curve is zero. We can write

$$v_{GS} - v_{DS}(\text{sat}) = V_{TN} \qquad (5.1(\text{a}))$$

or

$$v_{DS}(\text{sat}) = v_{GS} - V_{TN} \qquad (5.1(\text{b}))$$

where $v_{DS}(\text{sat})$ is the drain-to-source voltage that produces zero inversion charge density at the drain terminal.

When v_{DS} becomes larger than $v_{DS}(\text{sat})$, the point in the channel at which the inversion charge is just zero moves toward the source terminal. In this case, electrons enter the channel at the source, travel through the channel toward the drain, and then, at the point where the charge goes to zero, are injected into the space-charge region, where they are swept by the E-field to the drain contact. This process is similar to electrons being swept across a reverse-biased B–C junction in a bipolar transistor. In the ideal MOSFET, the drain current is constant for $v_{DS} > v_{DS}(\text{sat})$. This region of the i_D versus v_{DS} characteristic is referred to as the **saturation region**,[3] which is shown in Figure 5.9(d).
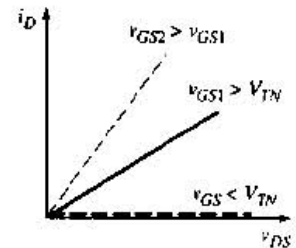
Figure 5.8 Plot of i_D versus v_{DS} characteristic for small values of v_{DS} at three v_{GS} voltages

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[3]The term saturation for MOSFETs is not to be confused with saturation for BJTs. We commonly say that a BJT is driven into *saturation*, which means that the collector current no longer increases with increasing base current and the collector–emitter voltage has reached a minimum value. When a MOSFET is biased in the *saturation region*, the drain current is essentially independent of drain voltage for a constant gate-to-source voltage.
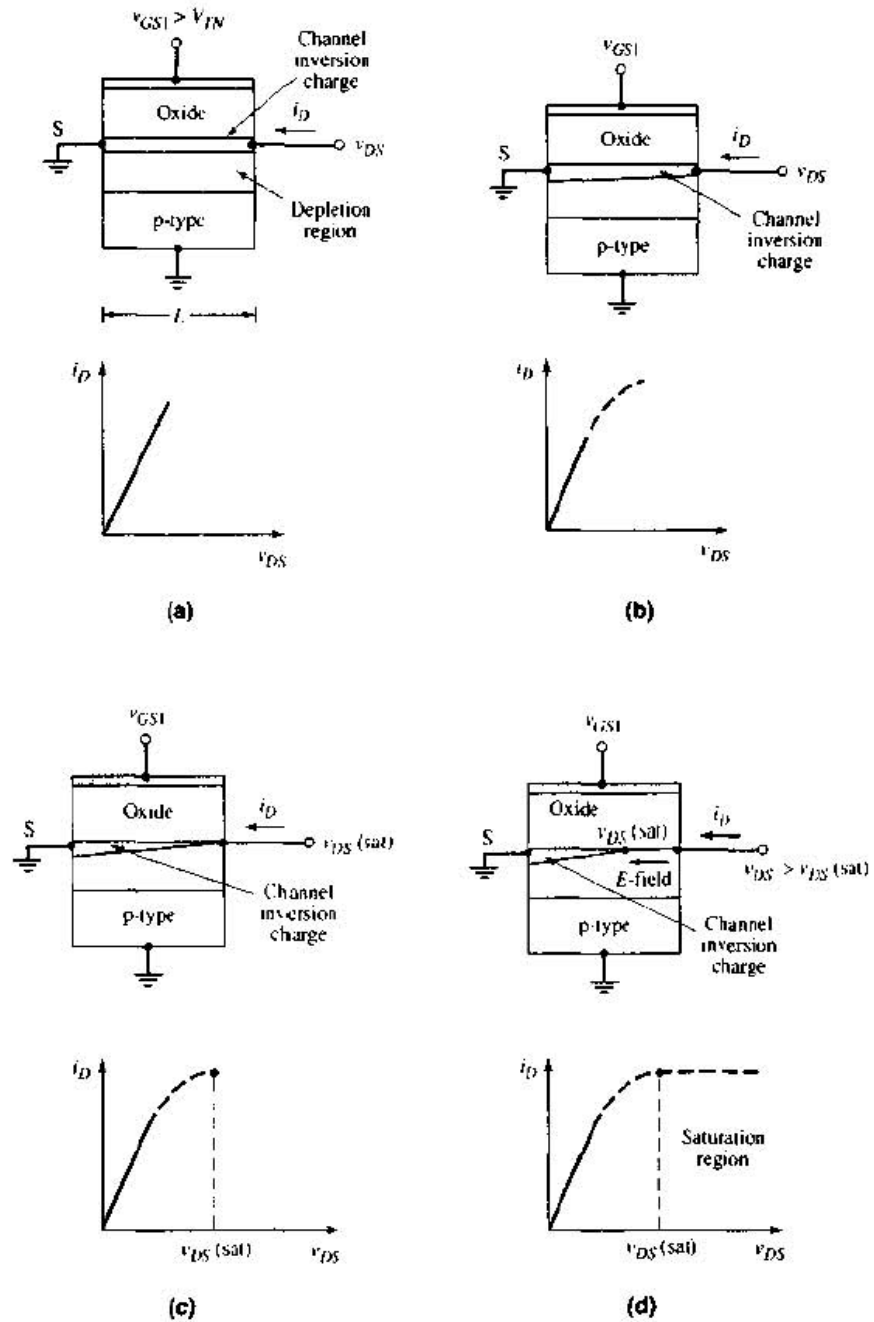
Figure 5.9 Cross section and i_D versus v_{DS} curve for an n-channel enhancement-mode MOSFET when $v_{GS} > V_{TN}$ for: (a) a small v_{DS} value, (b) a larger v_{DS} value, (c) $v_{DS} = v_{DS}(sat)$, and (d) $v_{DS} > v_{DS}(sat)$

As the applied gate-to-source voltage changes, the i_D versus v_{DS} curve changes. In Figure 5.8, we saw that the initial slope of i_D versus v_{DS} increases as v_{GS} increases. Also, Equation (5.1(b)) shows that $v_{DS}(sat)$ is a function of v_{GS}. Therefore, we can generate the family of curves for this n-channel enhancement mode MOSFET as shown in Figure 5.10.

Although the derivation of the current–voltage characteristics of the MOSFET is beyond the scope of this text, we can define the relationships.
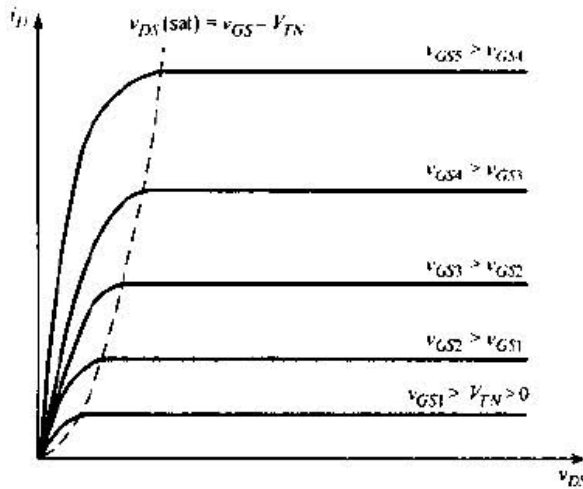
Figure 5.10   Family of i_D versus v_{DS} curves for an n-channel enhancement mode MOSFET

The region for which $v_{DS} < v_{DS}(\text{sat})$ is known as the **nonsaturation** or **triode region**. The ideal current-voltage characteristics in this region are described by the equation

$$i_D = K_n[2(v_{GS} - V_{TN})v_{DS} - v_{DS}^2] \qquad (5.2(a))$$

In the saturation region, the ideal current voltage characteristics for $v_{GS} > V_{TN}$ are described by the equation

$$i_D = K_n(v_{GS} - V_{TN})^2 \qquad (5.2(b))$$

In the saturation region, since the ideal drain current is independent of the drain-to-source voltage, the incremental or small-signal resistance is infinite. We see that

$$r_o = \Delta v_{DS}/\Delta i_D|_{v_{GS}=\text{const.}} = \infty$$

The parameter K_n is called the **conduction parameter** for the n-channel device and is given by

$$K_n = \frac{W\mu_n C_{ox}}{2L} \qquad (5.3(a))$$

where C_{ox} is the oxide capacitance per unit area. The capacitance is given by

$$C_{ox} = \epsilon_{ox}/t_{ox}$$

where t_{ox} is the oxide thickness and ϵ_{ox} is the oxide permittivity. For silicon devices, $\epsilon_{ox} = (3.9)(8.85 \times 10^{-14})$ F/cm. The parameter μ_n is the mobility of the electrons in the inversion layer. The channel width W and channel length L were shown in Figure 5.5(a).

As Equation (5.3(a)) indicates, the conduction parameter is a function of both electrical and geometric parameters. The oxide capacitance and carrier mobility are essentially constants for a given fabrication technology. However, the geometry, or width-to-length ratio W/L, is a variable in the design of MOSFETs that is used to produce specific current-voltage characteristics in MOSFET circuits.

We can rewrite the conduction parameter in the form

$$K_n = \frac{k_n'}{2} \cdot \frac{W}{L}$$ (5.3(b))

where $k_n' = \mu_n C_{ox}$. Normally, k_n' is considered to be a constant, so Equation (5.3(b)) emphasizes that the width-to-length ratio W/L is the transistor design variable.

Example 5.1   **Objective:** Calculate the current in an n-channel MOSFET.

Consider an n-channel enhancement mode MOSFET with the following parameters: $V_{TN} = 0.75$ V, $W = 40\,\mu m$, $L = 4\,\mu m$, $\mu_n = 650\,cm^2/V\text{-s}$, $t_{ox} = 450$ A, and $\epsilon_{ox} = (3.9)(8.85 \times 10^{-14})$ F/cm. Determine the current when $V_{GS} = 2V_{TN}$, for the transistor biased in the saturation region.

Solution: The conduction parameter is determined by Equation (5.3(a)). First, consider the units involved in this equation, as follows:

$$K_n = \frac{W(cm) \cdot \mu_n \left(\dfrac{cm^2}{V\text{-s}}\right) \epsilon_{ox} \left(\dfrac{F}{cm}\right)}{2L(cm) \cdot t_{ox}(cm)} = \frac{F}{V\text{-s}} = \frac{(C/V)}{V\text{-s}} = \frac{A}{V^2}$$

The value of the conduction parameter is therefore

$$K_n = \frac{W \mu_n \epsilon_{ox}}{2L t_{ox}} = \frac{(40 \times 10^{-4})(650)(3.9)(8.85 \times 10^{-14})}{2(4 \times 10^{-4})(450 \times 10^{-8})}$$

or

$$K_n = 0.249 \text{ mA/V}^2$$

From Equation (5.2(b)) for $v_{GS} = 2V_{TN}$, we find

$$i_D = K_n(v_{GS} - V_{TN})^2 = (0.249)(1.5 - 0.75)^2 = 0.140 \text{ mA}$$

Comment: The current capability of a transistor can be increased by increasing the conduction parameter. For a given fabrication technology, K_n is adjusted by varying the transistor width W.

Test Your Understanding

5.1   (a) An n-channel enhancement-mode MOSFET has a threshold voltage of $V_{TN} = 1.2$ V and an applied gate-to-source voltage of $v_{GS} = 2$ V. Determine the region of operation when: (i) $v_{DS} = 0.4$ V; (ii) $v_{DS} = 1$ V; and (iii) $v_{DS} = 5$ V. (b) Repeat part (a) for an n-channel depletion-mode MOSFET with a threshold voltage of $V_{TN} = -1.2$ V. (Ans. (a) (i) nonsaturation, (ii) saturation, (iii) saturation; (b) (i) nonsaturation, (ii) nonsaturation, (iii) saturation)

5.2   The NMOS devices described in Exercise 5.1 have parameters $W = 100\,\mu m$, $L = 7\,\mu m$, $t_{ox} = 450$ A, $\mu_n = 500\,cm^2/V\text{-s}$, and $\lambda = 0$. (a) Calculate the conduction parameter K_n for each device. (b) Calculate the drain current for each bias condition. (Ans. (a) $K_n = 0.274\,mA/V^2$ (b) $i_D = 0.132$, 0.175, and 0.175 mA; $i_D = 0.658$, 1.48, and 2.81 mA)

5.3 An NMOS transistor with $V_{TN} = 1$ V has a drain current $i_D = 0.8$ mA when $v_{GS} = 3$ V and $v_{DS} = 4.5$ V. Calculate the drain current when: (a) $v_{GS} = 2$ V, $v_{DS} = 4.5$ V; and (b) $v_{GS} = 3$ V, $v_{DS} = 1$ V. (Ans. (a) 0.2 mA (b) 0.6 mA)

5.1.4   Circuit Symbols and Conventions

The conventional circuit symbol for the n-channel enhancement-mode MOSFET is shown in Figure 5.11(a). The vertical solid line denotes the gate electrode, the vertical broken line denotes the channel (the broken line indicates the device is enhancement mode), and the separation between the gate line and channel line denotes the oxide that insulates the gate from the channel. The polarity of the pn junction between the substrate and the channel is indicated by the arrowhead on the body or substrate terminal. The direction of the arrowhead indicates the type of transistor, which in this case is an n-channel device.

In most applications in this text, we will implicitly assume that the source and substrate terminals are connected together. Explicitly drawing the substrate terminal for each transistor in a circuit becomes redundant and makes the circuits appear more complex. Instead, we will use the simplified circuit symbol for the n-channel MOSFET shown in Figure 5.11(b). In this symbol, the arrowhead is on the source terminal and it indicates the direction of current, which for the n-channel device is out of the source. By including the arrowhead in the symbol, we do not need to explicitly indicate the source and drain terminals. We will use the simplified circuit symbol throughout the text except in specific applications.

5.1.5   Additional MOSFET Structures and Circuit Symbols

Before we start analyzing MOSFET circuits, there are a number of other MOSFET structures in addition to the n-channel enhancement-mode device that need to be considered.

n-Channel Depletion-Mode MOSFET

Figure 5.12(a) shows the cross section of an n-channel depletion-mode MOSFET. When zero volts are applied to the gate, an n-channel region or inversion layer exists under the oxide as a result, for example, of impurities introduced during device fabrication. Since an n-region connects the n-source and n-drain, a drain-to-source current may be generated in the channel even with zero gate voltage. The term depletion mode means that a channel exists even at zero gate voltage. A negative gate voltage must be applied to the n-channel depletion-mode MOSFET to turn the device off.

Figure 5.12(b) shows the n-channel depletion mode MOSFET with a negative applied gate-to-source voltage. A negative gate voltage induces a space-charge region under the oxide, thereby reducing the thickness of the n-channel region. The reduced thickness decreases the channel conductance, which in turn reduces the drain current. When the gate voltage is equal to the threshold voltage, which is negative for this device, the induced space-charge region

(a)

(b)
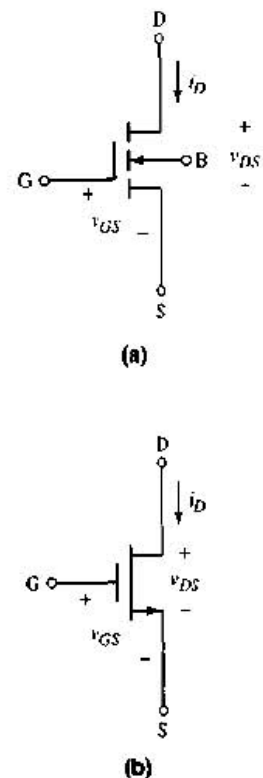
Figure 5.11 The n-channel enhancement-mode MOSFET: (a) conventional circuit symbol and (b) simplified circuit symbol
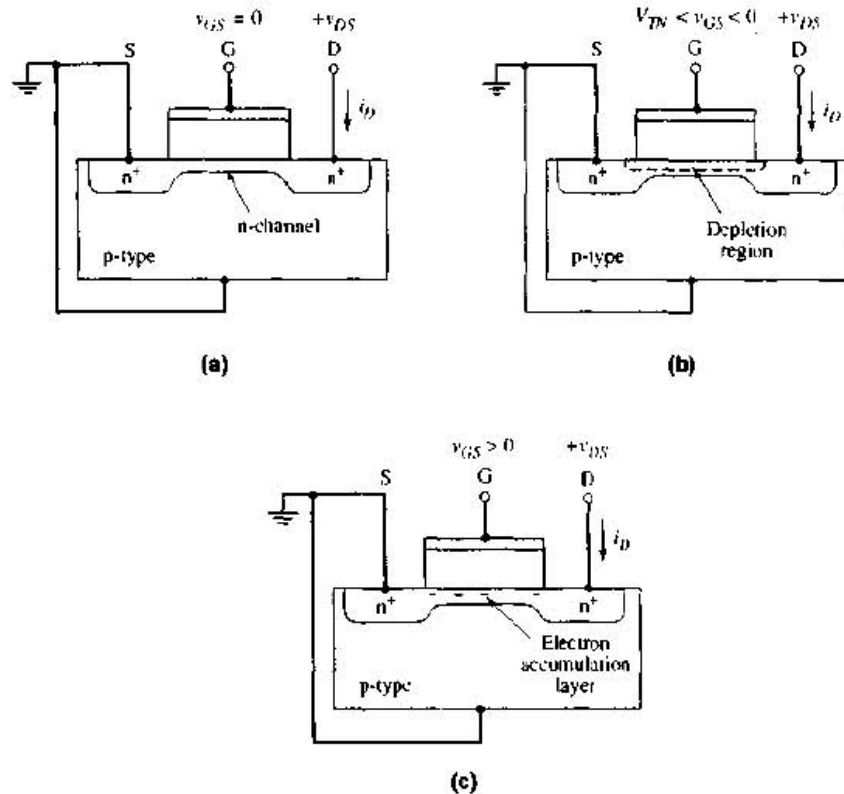
Figure 5.12 Cross section of an n-channel depletion mode MOSFET for: (a) $v_{GS} = 0$, (b) $v_{GS} < 0$, and (c) $v_{GS} > 0$

extends completely through the n-channel region, and the current goes to zero. A positive gate voltage creates an electron accumulation layer, as shown in Figure 5.12(c) which increases the drain current. The general i_D versus v_{DS} family of curves for the n-channel depletion-mode MOSFET is shown in Figure 5.13.

The current–voltage characteristics defined by Equations (5.2(a)) and (5.2(b)) apply to both enhancement- and depletion-mode n-channel devices. The only difference is that the threshold voltage V_{TN} is positive for the enhancement-mode MOSFET and negative for the depletion-mode MOSFET. Even though the current–voltage characteristics of enhancement- and depletion-mode devices are described by the same equations, different circuit symbols are used, simply for purposes of clarity.

The conventional circuit symbol for the n-channel depletion-mode MOSFET is shown in Figure 5.14(a). The vertical solid line denoting the channel indicates the device is depletion mode. A comparison of Figures 5.11(a) and 5.14(a) shows that the only difference between the enhancement- and depletion-mode symbols is the broken versus the solid line representing the channel.

A simplified symbol for the n-channel depletion-mode MOSFET is shown in Figure 5.14(b). The arrowhead is again on the source terminal and indicates the direction of current, which for the n-channel device is out of the source. The heavy solid line represents the depletion-mode channel region. Again,
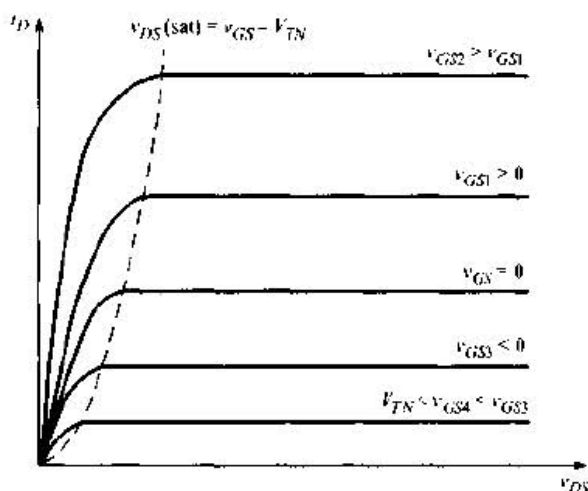
Figure 5.13 Family of i_D vesus v_{DS} curves for an n-channel depletion mode MOSFET

(a)

(b)

Figure 5.14 The n-channel depletion-mode MOSFET: (a) conventional circuit symbol and (b) simplified circuit symbol

using a different circuit symbol for the depletion-mode device compared to the enhancement-mode device is simply for clarity in a circuit diagram.

p-Channel MOSFETs

Figures 5.15(a) and 5.15(b) show cross sections of a p-channel enhancement-mode and a p-channel depletion-mode MOSFET, as well as the biasing configurations and currrent directions. The types of impurity doping in the source, drain, and substrate regions of the **p-channel MOSFET, or PMOS transistor**, are reversed compared to the n-channel device. In the p-channel enhancement-mode device, a negative gate-to-source voltage must be applied to create the inversion layer, or channel region, of holes that "connects" the source and drain regions. The threshold voltage, denoted as V_{TP} for the p-channel device,[4] is negative for an enhancement-mode device. The threshold voltage V_{TP} is positive for a p-channel depletion-mode device. Because holes flow from the source to the drain, the conventional current enters the source and leaves the drain. A p-channel region exists in the depletion-mode device with zero gate voltage.

The operation of the p-channel device is the same as that of the n-channel device, except that the hole is the charge carrier, rather than the electron, and the conventional current direction and voltage polarities are reversed. For the p-channel device biased in the nonsaturation region, the current is given by

$$i_D = K_p[2(v_{SG} + V_{TP})v_{SD} - v_{SD}^2]$$ (5.4(a))

In the saturation region, the current is given by

$$i_D = K_p(v_{SG} + V_{TP})^2$$ (5.4(b))

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[4]Using a different threshold voltage parameter for a PMOS device compared to that for the NMOS device is simply for clarity in particular applications.
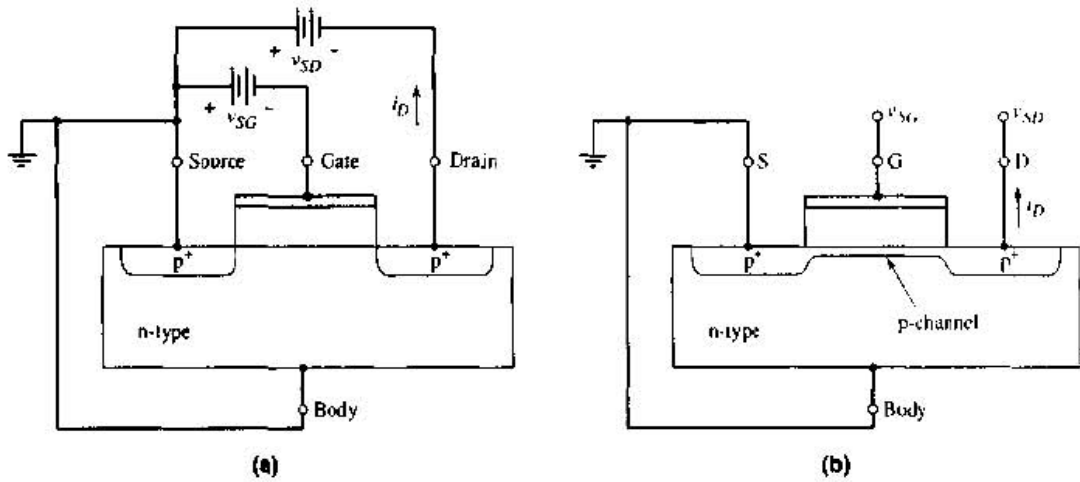
Figure 5.15 Cross section of p-channel MOSFETs: (a) enhancement-mode and (b) depletion-mode

and the drain current exits the drain terminal. The parameter K_p is the conduction parameter for the p-channel device and is given by

$$K_p = \frac{W \mu_p C_{ox}}{2L} \qquad (5.5(a))$$

where W, L, and C_{ox} are the channel width, length, and oxide capacitance per unit area, as previously defined. The parameter μ_p is the mobility of holes in the hole inversion layer. In general, the hole inversion layer mobility is less than the electron inversion layer mobility.

We can also rewrite Equation (5.5(a)) in the form

$$K_p = \frac{k_p'}{2} \cdot \frac{W}{L} \qquad (5.5(b))$$

where $k_p' = \mu_p C_{ox}$.

For a p-channel MOSFET biased in the saturation region, we have

$$v_{SD} > v_{SD}(\text{sat}) = v_{SG} + V_{TP} \qquad (5.6)$$

Example 5.2   Objective: Determine the source-to-drain voltage required to bias a p-channel depletion-mode MOSFET in the saturation region.

Consider a depletion-mode p-channel MOSFET for which $K_p = 0.2\,\text{mA/V}^2$, $V_{TP} = +0.50\,\text{V}$, and $i_D = 0.50\,\text{mA}$.

Solution: In the saturation region, the drain current is given by

$$i_D = K_p(v_{SG} + V_{TP})^2$$

or

$$0.50 = 0.2(v_{SG} + 0.50)^2$$

which yields

$$v_{SG} = 1.08\,\text{V}$$

To bias this p-channel MOSFET in the saturation region, the following must apply:

$$v_{SD} > v_{SD}(\text{sat}) = v_{SG} + V_{TP} = 1.08 + 0.5 = 1.58 \text{ V}$$

Comment: Biasing a transistor in either the saturation or the nonsaturation region depends on both the gate-to-source voltage and the drain-to-source voltage.

Test Your Understanding

5.4 (a) For a PMOS device, the threshold voltage is $V_{TP} = -2$ V and the applied source-to-gate voltage is $v_{SG} = 3$ V. Determine the region of operation when: (i) $v_{SD} = 0.5$ V; (ii) $v_{SD} = 2$ V; and (iii) $v_{SD} = 5$ V. (b) Repeat part (a) for a depletion-mode PMOS device with $V_{TP} = +0.5$ V. (Ans. (a) (i) nonsaturation, (ii) saturation, (iii) saturation; (b) nonsaturation, (ii) nonsaturation, (iii) saturation)

The conventional circuit symbol for the p-channel enhancement-mode MOSFET appears in Figure 5.16(a). Note that the arrowhead direction on the substrate terminal is reversed from that in the n-channel enhancement-mode device. The simplified circuit symbol we will use is shown in Figure 5.16(b). The arrowhead is on the source terminal, indicating the direction of current, which for the p-channel device is into the source.

(a)   (b)
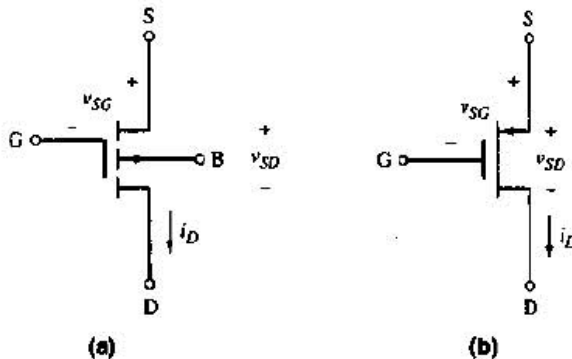
Figure 5.16 The p-channel enhancement-mode MOSFET: (a) conventional circuit symbol and (b) simplified circuit symbol

The conventional and simplified circuit symbols for the p-channel depletion-mode device are shown in Figure 5.17. The heavy solid line in the simplified symbol represents the channel region and denotes the depletion-mode device. The arrowhead is again on the source terminal and it indicates the current direction.

Complementary MOSFETs

Complementary MOS (CMOS) technology uses both n-channel and p-channel devices in the same circuit. Figure 5.18 shows the cross section of n-channel and p-channel devices fabricated on the same chip. CMOS circuits, in general,
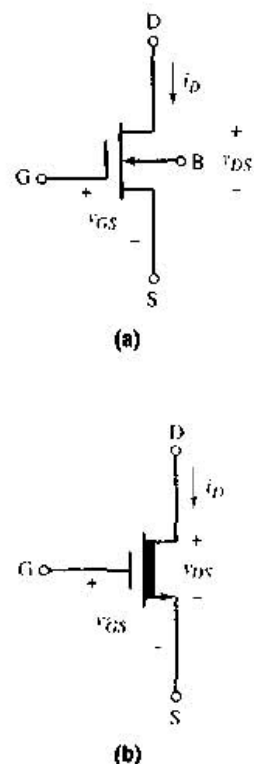

(a)

(b)
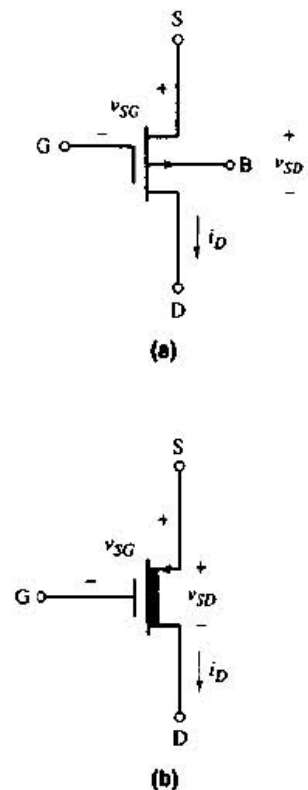
Figure 5.17 The p-channel depletion mode MOSFET: (a) conventional circuit symbol and (b) simplified circuit symbol
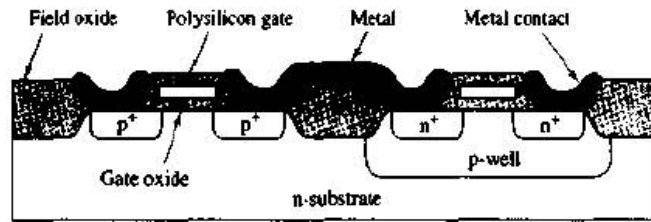
Figure 5.18 Cross sections of n-channel and p-channel transistors fabricated with a p-well CMOS technology

are more complicated to fabricate than circuits using entirely NMOS or PMOS devices. Yet, as we will see in later chapters, CMOS circuits have great advantages over just NMOS or PMOS circuits.

In order to fabricate n-channel and p-channel devices that are electrically equivalent, the magnitude of the threshold voltages must be equal, and the n-channel and p-channel conduction parameters must be equal. Since, in general, μ_n and μ_p are not equal, the design of equivalent transistors involves adjusting the width-to-length ratios of the transistors.

5.1.6   Summary of Transistor Operation

We have presented a first-order model of the operation of the MOS transistor. For an n-channel enhancement-mode MOSFET, a positive gate-to-source voltage, greater than the threshold voltage V_{TN}, must be applied to induce an electron inversion layer. For $v_{GS} > V_{TN}$, the device is turned on. For an n-channel depletion-mode device, a channel between the source and drain exists even for $v_{GS} = 0$. The threshold voltage is negative, so that a negative value of v_{GS} is required to turn the device off.

For a p-channel device, all voltage polarities and current directions are reversed compared to the NMOS device. For the p-channel enhancement-mode transistor, $V_{TP} < 0$ and for the depletion-mode PMOS transistor, $V_{TP} > 0$.

Table 5.1 lists the first-order equations that describe the i–v relationships in MOS devices. We note that K_n and K_p are positive values and that the drain current i_D is positive into the drain for the NMOS device and positive out of the drain for the PMOS device.

Table 5.1 Summary of the MOSFET current–voltage relationships

NMOS	PMOS
Nonsaturation region ($v_{DS} < v_{DS}(\text{sat})$)	Nonsaturation region ($v_{SD} < v_{SD}(\text{sat})$)
$i_D = K_n[2(v_{GS} - V_{TN})v_{DS} - v_{DS}^2]$	$i_D = K_p[2(v_{SG} + V_{TP})v_{SD} - v_{SD}^2]$
Saturation region ($v_{DS} > v_{DS}(\text{sat})$)	Saturation region ($v_{SD} > v_{SD}(\text{sat})$)
$i_D = K_n(v_{GS} - V_{TN})^2$	$i_D = K_p(v_{SG} + V_{TP})^2$
Transition point	Transition point
$v_{DS}(\text{sat}) = v_{GS} - V_{TN}$	$v_{SD}(\text{sat}) = v_{SG} + V_{TP}$
Enhancement mode	Enhancement mode
$V_{TN} > 0$	$V_{TP} < 0$
Depletion mode	Depletion mode
$V_{TN} < 0$	$V_{TP} > 0$

5.1.7 Nonideal Current–Voltage Characteristics

The five nonideal effects in the current–voltage characteristics of MOS transistors are: the finite output resistance in the saturation region, the body effect, subthreshold conduction, breakdown effects, and temperature effects. This section will examine each of these effects.

Finite Output Resistance

In the ideal case, when a MOSFET is biased in the saturation region, the drain current i_D is independent of drain-to-source voltage v_{DS}. However, in actual MOSFET i_D versus v_{DS} characteristics, a nonzero slope does exist beyond the saturation point. For $v_{DS} > v_{DS}(\text{sat})$, the actual point in the channel at which the inversion charge goes to zero moves away from the drain terminal (see Figure 5.9(d)). The effective channel length decreases, producing the phenomenon called **channel length modulation**.

An exaggerated view of the current–voltage characteristics is shown in Figure 5.19. The curves can be extrapolated so that they intercept the voltage axis at a point $v_{DS} = -V_A$. The voltage V_A is usually defined as a positive quantity and is similar to the Early voltage of a bipolar transistor (see Chapter 3). The slope of the curve in the saturation region can be described by expressing the i_D versus v_{DS} characteristic in the form, for an n-channel device,

$$i_D = K_n[(v_{GS} - V_{TN})^2(1 + \lambda v_{DS})] \tag{5.7}$$

where λ is a positive quantity called the channel-length modulation parameter.
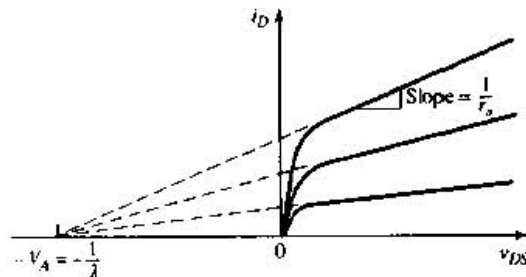
Figure 5.19 Effect of channel length modulation, resulting in a finite output resistance

The parameters λ and V_A are related. From Equation (5.7), we have $(1 + \lambda v_{DS}) = 0$ at the extrapolated point where $i_D = 0$. At this point, $v_{DS} = -V_A$, which means that $V_A = 1/\lambda$.

The output resistance due to the channel length modulation is defined as

$$r_o = \left(\frac{\partial i_D}{\partial v_{DS}}\right)^{-1}\Bigg|_{v_{GS}=\text{const.}} \tag{5.8}$$

From Equation (5.7), the output resistance, evaluated at the Q-point, is

$$r_o = [\lambda K_n(V_{GSQ} - V_{TN})^2]^{-1} \tag{5.9(a)}$$

or

$$r_o \cong [\lambda I_{DQ}]^{-1} = \frac{1}{\lambda I_{DQ}} = \frac{V_A}{I_{DQ}} \qquad (5.9(b))$$

The output resistance r_o is also a factor in the small-signal equivalent circuit of the MOSFET, which is discussed in the next chapter.

Test Your Understanding

5.5 For an NMOS enhancement-mode device, the parameters are: $V_{TN} = 0.8$ V and $K_n = 0.1$ mA/V^2. The device is biased at $v_{GS} = 2.5$ V. Calculate the drain current when $v_{DS} = 2$ V and $v_{DS} = 10$ V for: (a) $\lambda = 0$ and (b) $\lambda = 0.02$ V^{-1}. (c) Calculate the output resistance r_o for parts (a) and (b). (Ans. (a) $i_D = 0.289$ mA for both 2 and 10 V; (b) $i_D = 0.30$ mA (2 V), $i_D = 0.347$ mA (10 V); (c) $r_o = \infty$ (a), $r_o = 173$ kΩ (b))

Body Effect

Up to this point, we have assumed that the substrate, or body, is connected to the source. For this bias condition, the threshold voltage is a constant.

In integrated circuits, however, the substrates of all n-channel MOSFETs are usually common and are tied to the most negative potential in the circuit. An example of two n-channel MOSFETs in series is shown in Figure 5.20. The p-type substrate is common to the two transistors, and the drain of M_1 is common to the source of M_2. When the two transistors are conducting, there is a nonzero drain-to-source voltage on M_1, which means that the source of M_2 is not at the same potential as the substrate. These bias conditions mean that a zero or reverse-bias voltage exists across the source–substrate pn junction, and a change in the source–substrate junction voltage changes the threshold voltage. This is called the **body effect**. The same situation exists in p-channel devices.
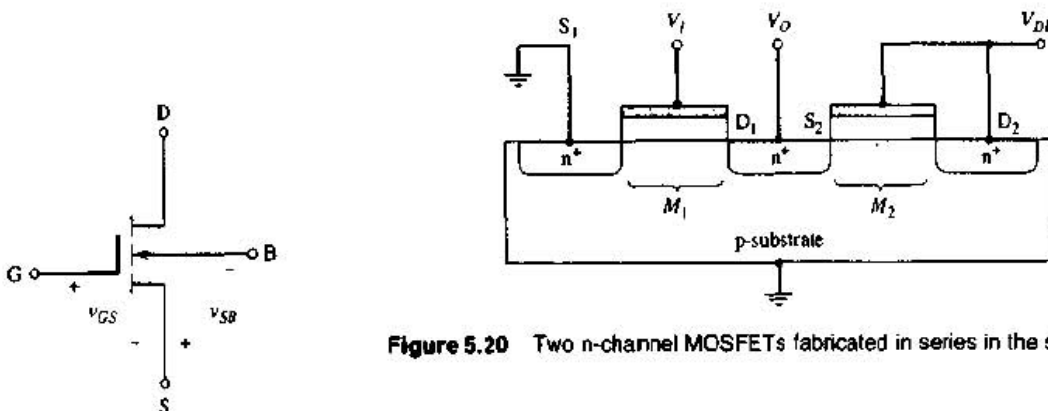

Figure 5.20 Two n-channel MOSFETs fabricated in series in the same substrate
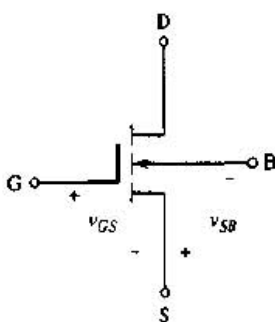

Figure 5.21 An n-channel enhancement-mode MOSFET with a substrate voltage

For example, consider the n-channel device shown in Figure 5.21. To maintain a zero- or reverse-biased source–substrate pn junction, we must have $v_{SB} \geq 0$. The threshold voltage for this condition is given by

$$V_{TN} = V_{TNO} + \gamma\left[\sqrt{2\phi_f + v_{SB}} - \sqrt{2\phi_f}\,\right] \qquad (5.10)$$

where V_{TNO} is the threshold voltage for $v_{SB} = 0$; γ, called the bulk threshold or **body-effect parameter**, is related to device properties, and is typically on the order of $0.5\ \mathrm{V}^{1/2}$; and ϕ_f is a semiconductor parameter, typically on the order of $0.35\ \mathrm{V}$, and is a function of the semiconductor doping. We see from Equation (5.10) that the threshold voltage in n-channel devices increases due to this body effect.

The body effect can cause a degradation in circuit performance because of the changing threshold voltage. However, we will generally neglect the body effect in our circuit analyses, for simplicity.

Test Your Understanding

5.6   An NMOS transistor has parameters $V_{TNO} = 1\ \mathrm{V}$, $\gamma = 0.35\ \mathrm{V}^{1/2}$, and $\phi_f = 0.35\ \mathrm{V}$. Calculate the threshold voltage when: (a) $v_{SB} = 0$, (b) $v_{SB} = 1\ \mathrm{V}$, and (c) $v_{SB} = 4\ \mathrm{V}$. (Ans. (a) 1 V, (b) 1.16 V, (c) 1.47 V)

Subthreshold Conduction

If we consider the ideal current-voltage relationship for the n-channel MOSFET biased in the saturation region, we have, from Equation (5.2(b)),

$$i_D = K_n(v_{GS} - V_{TN})^2$$

Taking the square root of both sides of the equation, we obtain

$$\sqrt{i_D} = \sqrt{K_n}(v_{GS} - V_{TN}) \qquad (5.11)$$

From Equation (5.11), we see that $\sqrt{i_d}$ is a linear function of v_{GS}. Figure 5.22 shows a plot of this ideal relationship.

Also plotted in Figure 5.22 are experimental results, which show that when v_{GS} is slightly less than V_{TN}, the drain current is not zero, as previously assumed. This current is called the **subthreshold current**. The effect may not be significant for a single device, but if hundreds or thousands of devices on an integrated circuit are biased just slightly below the threshold voltage, the power supply current will not be zero but may contribute to significant power dissipation in the integrated circuit. One example of this is a dynamic random access memory (DRAM), as we will see in Chapter 16.

In this text, for simplicity we will not specifically consider the subthreshold current. However, when a MOSFET in a circuit is to be turned off, the "proper" design of the circuit must involve biasing the device at least a few tenths of a volt below the threshold voltage to achieve "true" cutoff.

Figure 5.22 Plot of $\sqrt{i_D}$ versus v_{GS} characteristic showing subthreshold conduction

Breakdown Effects

Several possible breakdown effects may occur in a MOSFET. The drain-to-substrate pn junction may break down if the applied drain voltage is too high

and avalanche multiplication occurs. This breakdown is the same reverse-biased pn junction breakdown discussed in Chapter 1 in Section 1.2.5.

As the size of the device becomes smaller, another breakdown mechanism, called *punch-through*, may become significant. **Punch-through** occurs when the drain voltage is large enough for the depletion region around the drain to extend completely through the channel to the source terminal. This effect also causes the drain current to increase rapidly with only a small increase in drain voltage.

A third breakdown mechanism is called **near-avalanche** or **snapback breakdown**. This breakdown process is due to second-order effects within the MOSFET. The source-substrate-drain structure is equivalent to that of a bipolar transistor. As the device size shrinks, we may begin to see a parasitic bipolar transistor action with increases in the drain voltage. This parasitic action enhances the breakdown effect.

If the electric field in the oxide becomes large enough, breakdown can also occur in the oxide, which can lead to catastrophic failure. In silicon dioxide, the electric field at breakdown is on the order of 6×10^6 V/cm, which, to a first approximation, is given by $E_{ox} = V_G/t_{ox}$. A gate voltage of approximately 30 V would produce breakdown in an oxide with a thickness of $t_{ox} = 500$ Å. However, a safety margin of a factor of 3 is common, which means that the maximum safe gate voltage for $t_{ox} = 500$ Å would be 10 V. A safety margin is necessary since there may be defects in the oxide that lower the breakdown field. We must also keep in mind that the input impedance at the gate is very high, and a small amount of static charge accumulating on the gate can cause the breakdown voltage to be exceeded. To prevent the accumulation of static charge on the gate capacitance of a MOSFET, a gate protection device, such as a reverse-biased diode, is usually included at the input of a MOS integrated circuit.

Temperature Effects

Both the threshold voltage V_{TN} and conduction parameter K_n are functions of temperature. The magnitude of the threshold voltage decreases with temperature, which means that the drain current increases with temperature at a given V_{GS}. However, the conduction parameter is a direct function of the inversion carrier mobility, which decreases as the temperature increases. Since the temperature dependence of mobility is larger than that of the threshold voltage, the net effect of increasing temperature is a decrease in drain current at a given V_{GS}. This particular result provides a negative feedback condition in power MOSFETs. A decreasing value of K_n inherently limits the channel current and provides stability for a power MOSFET.

5.2   MOSFET DC CIRCUIT ANALYSIS

In the last section, we considered the basic MOSFET characteristics and properties. We now start analyzing and designing the dc biasing of MOS transistor circuits. A primary purpose of the rest of the chapter is to continue to become familiar and comfortable with the MOS transistor and MOSFET circuits. As with bipolars, the dc biasing of MOSFETs, the focus of this chapter, is an

important part of the design of amplifiers. MOSFET amplifier design is the focus of the next chapter.

In most of the circuits presented in this chapter, resistors are used in conjunction with the MOS transistors. In a real MOSFET integrated circuit, however, the resistors are generally replaced by other MOSFETs, so the circuit is composed entirely of MOS devices. As we go through the chapter, we will begin to see how this is accomplished and as we finish the text, we will indeed analyze and design circuits containing only MOSFETs.

In the dc analysis of MOSFET circuits, we can use the ideal current–voltage equations listed in Table 5.1 in Section 5.1.

5.2.1   Common-Source Circuit

One of the basic MOSFET circuit configurations is called the common-source circuit. Figure 5.23 shows one example of this type of circuit using an n-channel enhancement-mode MOSFET. The source terminal is at ground potential and is common to both the input and output portions of the circuit. The coupling capacitor C_C acts as an open circuit to dc but it allows the signal voltage to be coupled to the gate of the MOSFET.

The dc equivalent circuit is shown in Figure 5.24(a). In the following dc analyses, we again use the notation for dc currents and voltages. Since the gate current into the transistor is zero, the voltage at the gate is given by a voltage divider, which can be written as

$$V_G = V_{GS} = \left(\frac{R_2}{R_1 + R_2}\right) V_{DD} \tag{5.12}$$
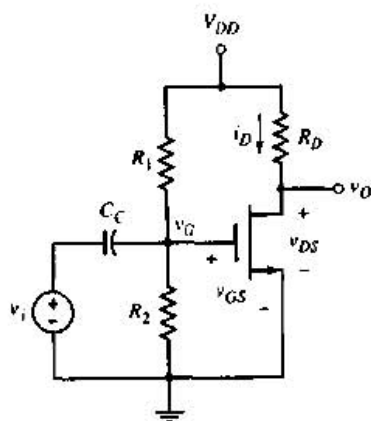

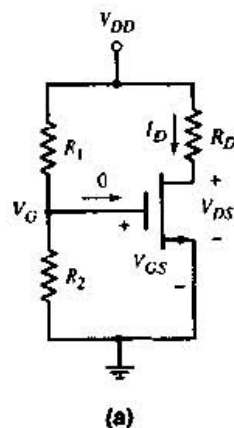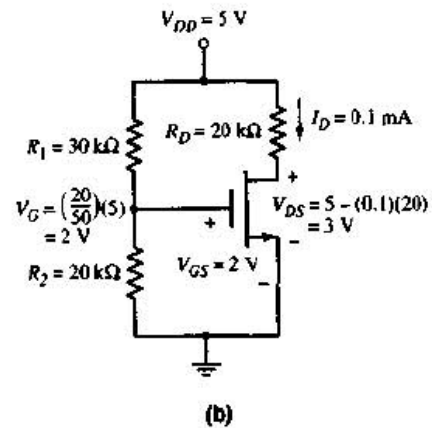**Figure 5.23**   An NMOS common-source circuit

Figure 5.24   (a) An NMOS common-source circuit and (b) the NMOS circuit for Example 5.3

Assuming that the gate-to-source voltage given by Equation (5.12) is greater than V_{TN}, and that the transistor is biased in the saturation region, the drain current is

$$I_D = K_n(V_{GS} - V_{TN})^2 \tag{5.13}$$

The drain-to-source voltage is

$$V_{DS} = V_{DD} - I_D R_D \qquad\qquad (5.14)$$

If $V_{DS} > V_{DS}(\text{sat}) = V_{GS} - V_{TN}$, then the transistor is biased in the saturation region, as we initially assumed, and our analysis is correct. If $V_{DS} < V_{DS}(\text{sat})$, then the transistor is biased in the nonsaturation region, and the drain current is given by Equation (5.2(a)).

Example 5.3 **Objective:** Calculate the drain current and drain-to-source voltage of a common-source circuit with an n-channel enhancement-mode MOSFET.

For the circuit shown in Figure 5.24(a), assume that $R_1 = 30\,\text{k}\Omega$, $R_2 = 20\,\text{k}\Omega$, $R_D = 20\,\text{k}\Omega$, $V_{DD} = 5\,\text{V}$, $V_{TN} = 1\,\text{V}$, and $K_n = 0.1\,\text{mA/V}^2$.

Solution: From the circuit shown in Figure 5.24(b) and Equation (5.12), we have

$$V_G = V_{GS} = \left(\frac{R_2}{R_1 + R_2}\right) V_{DD} = \left(\frac{20}{20+30}\right)(5) = 2\,\text{V}$$

Assuming the transistor is biased in the saturation region, the drain current is

$$I_D = K_n(V_{GS} - V_{TN})^2 = (0.1)(2-1)^2 = 0.1\,\text{mA}$$

and the drain-to-source voltage is

$$V_{DS} = V_{DD} - I_D R_D = 5 - (0.1)(20) = 3\,\text{V}$$

Comment: Because $V_{DS} = 3\,\text{V} > V_{DS}(\text{sat}) = V_{GS} - V_{TN} = 2 - 1 = 1\,\text{V}$, the transistor is indeed biased in the saturation region and our analysis is valid.

Figure 5.25(a) shows a common-source circuit with a p-channel enhancement-mode MOSFET. The source terminal is tied to $+V_{DD}$, which becomes signal ground in the ac equivalent circuit. Thus the terminology common-source applies to this circuit.
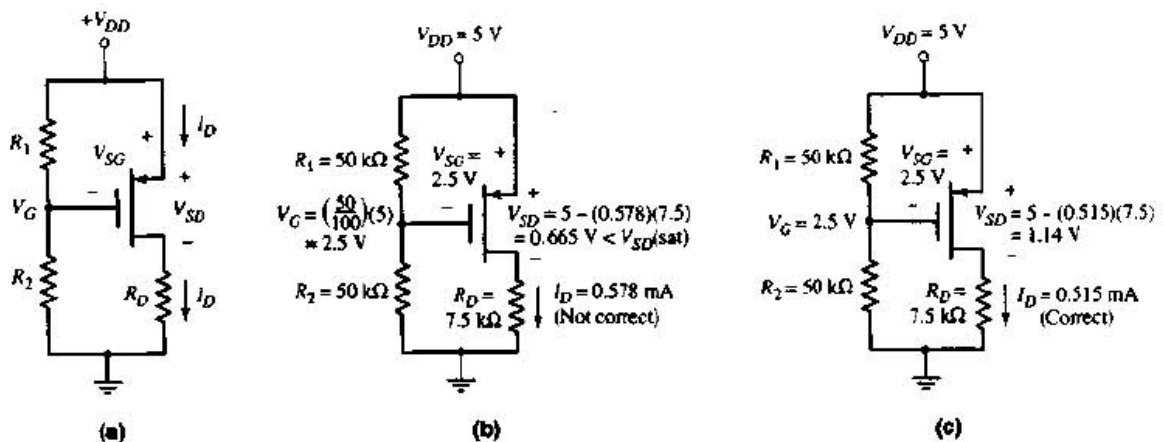
Figure 5.25 (a) A PMOS common-source circuit, (b) results when saturation-region bias assumption is incorrect, and (c) results when nonsaturation-region bias assumption is correct

The dc analysis is essentially the same as for the n-channel MOSFET circuit. The gate voltage is

$$V_G = \left(\frac{R_2}{R_1 + R_2}\right)(V_{DD}) \tag{5.15(a)}$$

and the source-to-gate voltage is

$$V_{SG} = V_{DD} - V_G \tag{5.15(b)}$$

Assuming that $V_{GS} < V_{TP}$, or $V_{SG} > |V_{TP}|$, and that the device is biased in the saturation region, the drain current is given by

$$I_D = K_p(V_{SG} + V_{TP})^2 \tag{5.16}$$

and the source-to-drain voltage is

$$V_{SD} = V_{DD} - I_D R_D \tag{5.17}$$

If $V_{SD} > V_{SD}(\text{sat}) = V_{SG} + V_{TP}$, then the transistor is indeed biased in the saturation region, as we have assumed. However, if $V_{SD} < V_{SD}(\text{sat})$, the transistor is biased in the nonsaturation region.

Example 5.4 Objective: Calculate the drain current and source-to-drain voltage of a common-source circuit with a p-channel enhancement-mode MOSFET.

Consider the circuit shown in Figure 5.25(a). Assume that $R_1 = R_2 = 50\,k\Omega$, $V_{DD} = 5\,V$, $R_D = 7.5\,k\Omega$, $V_{TP} = -0.8\,V$, and $K_p = 0.2\,mA/V^2$.

Solution: From the circuit shown in Figure 5.25(b) and Equation (5.15(a)), we have

$$V_G = \left(\frac{R_2}{R_1 + R_2}\right)(V_{DD}) = \left(\frac{50}{50 + 50}\right)(5) = 2.5\,V$$

The source-to-gate voltage is therefore

$$V_{SG} = V_{DD} - V_G = 5 - 2.5 = 2.5\,V$$

Assuming the transistor is biased in the saturation region, the drain current is

$$I_D = K_p(V_{SG} + V_{TP})^2 = (0.2)(2.5 - 0.8)^2 = 0.578\,mA$$

and the source-to-drain voltage is

$$V_{SD} = V_{DD} - I_D R_D = 5 - (0.578)(7.5) = 0.665\,V$$

Since $V_{SD} = 0.665\,V$ is not greater than $V_{SD}(\text{sat}) = V_{SG} + V_{TP} = 2.5 - 0.8 = 1.7\,V$, the p-channel MOSFET is not biased in the saturation region, as we initially assumed.

In the nonsaturation region, the drain current is given by

$$I_D = K_p[2(V_{SG} + V_{TP})V_{SD} - V_{SD}^2]$$

and the source-to-drain voltage is

$$V_{SD} = V_{DD} - I_D R_D$$

Combining these two equations, we obtain

$$I_D = K_p[2(V_{SG} + V_{TP})(V_{DD} - I_D R_D) - (V_{DD} - I_D R_D)^2]$$

or

$$I_D = (0.2)[2(2.5 - 0.8)(5 - I_D(7.5)) - (5 - I_D(7.5))^2]$$

Solving this quadratic equation for I_D, we find

$\qquad I_D = 0.515 \, \text{mA}$

We also find that

$\qquad V_{SD} = 1.14 \, \text{V}$

Therefore, $V_{SD} < V_{SD}(\text{sat})$, which verifies that the transistor is biased in the nonsaturation region.

Comment: In solving the quadratic equation for I_D, we find a second solution that yields $V_{SD} = 2.93 \, \text{V}$. However, this value of V_{SD} is greater than $V_{SD}(\text{sat})$, so it is not a valid solution since we assumed the transistor to be biased in the nonsaturation region.

As Example 5.4 illustrated, we may not know initially whether a transistor is biased in the saturation or nonsaturation region. The approach involves making an educated guess and then verifying that assumption. If the assumption proves incorrect, we must then change it and reanalyze the circuit.

In linear amplifiers containing MOSFETs, the transistors are biased in the saturation region.

Test Your Understanding

*5.7 For the transistor in the circuit in Figure 5.26, the parameters are $V_{TN} = 1 \, \text{V}$ and $K_n = 0.5 \, \text{mA/V}^2$. Determine V_{GS}, I_D, and V_{DS}. (Ans. $V_{GS} = 2.65 \, \text{V}$, $I_D = 1.36 \, \text{mA}$, $V_{DS} = 5.92 \, \text{V}$)

*5.8 Consider the circuit shown in Figure 5.27. The transistor parameters are $V_{TP} = -1 \, \text{V}$ and $K_p = 0.25 \, \text{mA/V}^2$. Calculate V_{SG}, I_D, and V_{SD} (Ans. $V_{SG} = 3.04 \, \text{V}$, $I_D = 1.04 \, \text{mA}$, $V_{SD} = 4.59 \, \text{V}$)
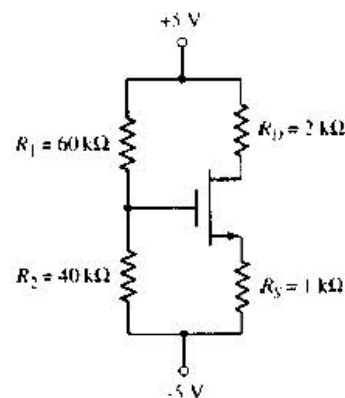
Figure 5.26 Circuit for Exercise 5.7   **Figure 5.27** Circuit for Exercise 5.8
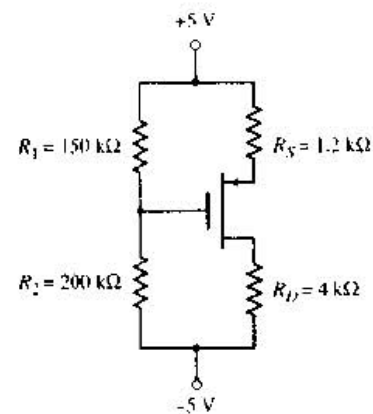
RD5.9 The transistor in the circuit shown in Figure 5.24(a) has parameters $V_{TN} = 0.8 \, \text{V}$ and $K_n = 0.25 \, \text{mA/V}^2$. The circuit is biased with $V_{DD} = 7.5 \, \text{V}$. Let $R_1 + R_2 = 250 \, \text{k}\Omega$. Redesign the circuit such that $I_D = 0.40 \, \text{mA}$ and $V_{DS} = 4 \, \text{V}$ (Ans. $R_2 = 68.7 \, \text{k}\Omega$, $R_1 = 181.3 \, \text{k}\Omega$, $R_D = 8.75 \, \text{k}\Omega$)

5.2.2   Load Line and Modes of Operation

The load line is helpful in visualizing the region in which the MOSFET is biased. Consider again the common-source circuit shown in Figure 5.24(b). Writing a Kirchhoff's voltage law equation around the drain–source loop results in Equation (5.14), which is the load line equation, showing a linear relationship between the drain current and drain-to-source voltage.

Figure 5.28 shows the v_{DS}(sat) characteristic for the transistor described in Example 5.3. The load line is given by

$$V_{DS} = V_{DD} - I_D R_D = 5 - I_D(20) \qquad (5.18(a))$$

or

$$I_D = \frac{5}{20} - \frac{V_{DS}}{20} \text{ (mA)} \qquad (5.18(b))$$

and is also plotted in the figure. The two end points of the load line are determined in the usual manner. If $I_D = 0$, then $V_{DS} = 5$ V; if $V_{DS} = 0$, then $I_D = 5/20 = 0.25$ mA. The Q-point of the transistor is given by the dc drain current and drain-to-source voltage, and it is always on the load line, as shown in the figure. A few transistor characteristics are also shown on the figure.
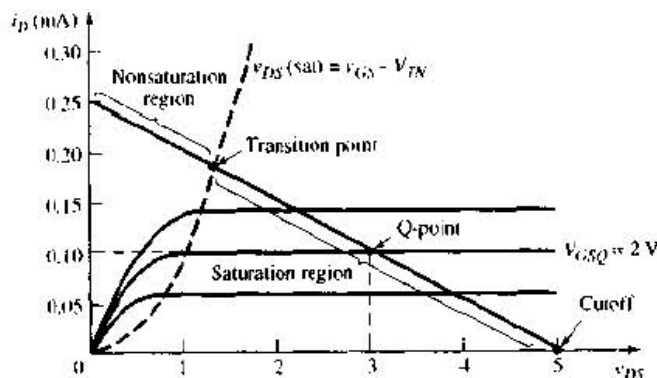
Figure 5.28 Transistor characteristics, v_{DS}(sat) curve, load line, and Q-point for the NMOS common-source circuit in Figure 5.24(b)

If the gate-to-source voltage is less than V_{TN}, the drain current is zero and the transistor is in cutoff. As the gate-to-source voltage becomes just greater than V_{TN}, the transistor turns on and is biased in the saturation region. As V_{GS} increases, the Q-point moves up the load line. The transition point is the boundary between the saturation and nonsaturation regions and is defined as the point where $V_{DS} = V_{DS}$(sat) $= V_{GS} - V_{TN}$. As V_{GS} increase above the transition point value, the transistor becomes biased in the nonsaturation region.

Example 5.5   Objective: Determine the transition point parameters for a common-source circuit.

Consider the circuit shown in Figure 5.24(b). Assume transistor parameters of $V_{TN} = 1$ V and $K_n = 0.1$ mA/V^2.

Solution: At the transition point,

$$V_{DS} = V_{DS}(\text{sat}) = V_{GS} - V_{TN} = V_{DD} - I_D R_D$$

The drain current is still

$$I_D = K_n (V_{GS} - V_{TN})^2$$

Combining the last two equations, we obtain

$$V_{GS} - V_{TN} = V_{DD} - K_n R_D (V_{GS} - V_{TN})^2$$

Rearranging this equation produces

$$K_n R_D (V_{GS} - V_{TN})^2 + (V_{GS} - V_{TN}) - V_{DD} = 0$$

or

$$(0.1)(20)(V_{GS} - V_{TN})^2 + (V_{GS} - V_{TN}) - 5 = 0$$

Solving the quadratic equation, we find that

$$V_{GS} - V_{TN} = 1.35\,\text{V} = V_{DS}$$

Therefore,

$$V_{GS} = 2.35\,\text{V}$$

and

$$I_D = (0.1)(2.35 - 1)^2 = 0.182\,\text{mA}$$

Comment: For $V_{GS} < 2.35\,\text{V}$, the transistor is biased in the saturation region; for $V_{GS} > 2.35\,\text{V}$, the transistor is biased in the nonsaturation region.

Problem-Solving Technique: MOSFET DC Analysis

Analyzing the dc response of a MOSFET circuit requires knowing the bias condition (saturation or nonsaturation) of the transistor. In some cases, the bias condition may not be obvious, which means that we have to guess the bias condition, then analyze the circuit to determine if we have a solution consistent with our initial guess. To do this, we can:

1. Assume that the transistor is biased in the saturation region, in which case $V_{GS} > V_{TN}$, $I_D > 0$, and $V_{DS} \geq V_{DS}(\text{sat})$.
2. Analyze the circuit using the saturation current-voltage relations.
3. Evaluate the resulting bias condition of the transistor. If the assumed parameter values in step 1 are valid, then the initial assumption is correct. If $V_{GS} < V_{TN}$, then the transistor is probably cutoff, and if $V_{DS} < V_{DS}(\text{sat})$, the transistor is likely biased in the nonsaturation region.
4. If the initial assumption is proved incorrect, then a new assumption must be made and the circuit reanalyzed. Step 3 must then be repeated.

5.2.3 Common MOSFET Configurations: DC Analysis

There are various other MOSFET circuit configurations, in addition to the basic common-source circuit. Several examples are discussed in this section. We continue the dc analysis and design of MOSFET circuits to increase our proficiency and to become more adept in the analysis of these types of circuits.

Design Example 5.6 Objective: Design the dc bias of a MOSFET circuit to produce a specified drain current.

For the dc circuit in Figure 5.29, assume the MOSFET parameters are $V_{TN} = 2$ V, $k_n' = 80 \mu A/V^2$, and $W/L = 4$. Choose R_1 and R_2 such that the current in the bias resistors is approximately one-tenth of I_D. Design the circuit such that $I_D = 0.5$ mA. In the final design, standard resistor values are to be used.

Solution: Assuming the transistor is biased in the saturation region, we have

$$I_D = \frac{k_n'}{2} \cdot \frac{W}{L} (V_{GS} - V_{TN})^2$$

or

$$0.5 = \left(\frac{0.080}{2}\right) \cdot (4) \cdot (V_{GS} - 2)^2$$

which yields

$$V_{GS} = 3.77 \text{ V}$$

The current through the bias resistors should be approximately 0.05 mA so that

$$R_1 + R_2 = \frac{10}{0.05} = 200 \text{ k}\Omega$$

We can write

$$V_{GS} = V_G - V_S = \left[\left(\frac{R_2}{R_1 + R_2}\right)(10) - 5\right] - [I_D R_S - 5]$$

so that

$$3.77 = \left(\frac{R_2}{200}\right)(10) - (0.5)(2)$$

We find that

$$R_2 = 95.4 \text{ k}\Omega \quad \text{and} \quad R_1 = 104.6 \text{ k}\Omega$$

The closest standard resistor values are $R_2 = 100 \text{ k}\Omega$ and $R_1 = 110 \text{ k}\Omega$.

Comment: Since $V_{DS} = 4$ V, then $V_{DS} > V_{DS}(\text{sat}) = V_{GS} - V_{TN} = 3.77 - 2 = 1.77$ V. Therefore, the transistor is biased in the saturation region, as initially assumed.

Design Pointer: We must keep in mind that there are certain tolerances in resistor values as well as tolerances in transistor conduction parameter and threshold voltage values. These tolerances lead to variations in the Q-point values. One implication of this variation is that we should not design the Q-point too close to the transition point, or the parameter variations may push the Q-point into the nonsaturation region. This is one situation in which a computer simulation may cut down the number of tedious calculations.
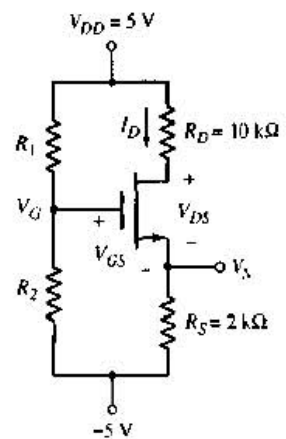
Figure 5.29 NMOS common-source circuit with source resistor

In bipolar circuits, we observed that the Q-point tended to be stabilized when an emitter resistor was included in the circuit. In a similar way, the Q-point of MOSFET circuits will tend to be stabilized against variations in transistor parameters by including a source resistor. The transistor conduction parameter may vary from one device to another because of fabrication tolerances in channel length, channel width, oxide thickness, or carrier mobility. The threshold voltage may also vary from one device to another. Variations in these device parameters will change the Q-point in a given circuit, but the change can be lessened by including a source resistor. Further, in many MOSFET circuits today, the source resistor is replaced by a constant-current source, which biases the transistor with a constant current that is independent of the transistor parameters, thereby stabilizing the Q-point.

Design Example 5.7 **Objective:** Design a MOSFET circuit biased with a constant-current source.

The parameters of the transistor in the circuit shown in Figure 5.30(a) are $V_{TN} = 0.8$ V, $k_n' = 80 \mu A/V^2$, and $W/L = 3$. Design the circuit such that the quiescent values are $I_D = 250 \mu A$ and $V_D = 2.5$ V.

Solution: The dc equivalent circuit is shown in Figure 5.30(b). Since $v_i = 0$, the gate is at ground potential and there is no gate current through R_G.

(a)   (b)
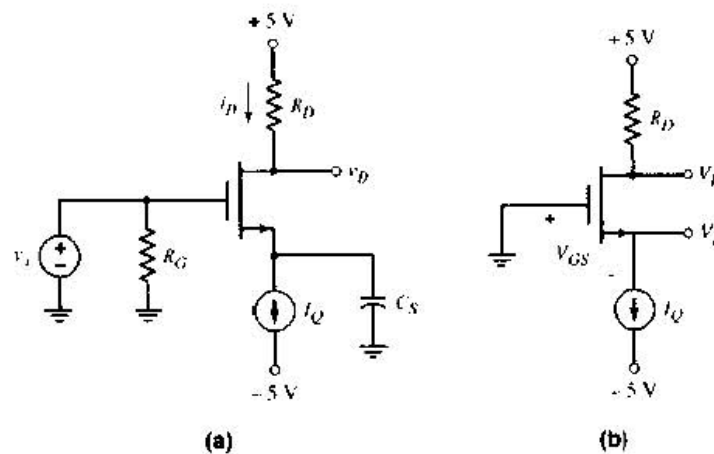
Figure 5.30 (a) NMOS common-source circuit biased with a constant-current source and (b) equivalent dc circuit

Assuming the transistor is biased in the saturation region, we have

$$I_D = \frac{k_n'}{2} \cdot \frac{W}{L}(V_{GS} - V_{TN})^2$$

or

$$250 = \left(\frac{80}{2}\right) \cdot (3)(V_{GS} - 0.8)^2$$

which yields

$$V_{GS} = 2.24 \text{ V}$$

The voltage at the source terminal is $V_S = -V_{GS} = -2.24$ V.

The drain current can also be written as

$$I_D = \frac{5 - V_D}{R_D}$$

For $V_D = 2.5\,V$, we have

$$R_D = \frac{5 - 2.5}{0.25} = 10\,k\Omega$$

The drain-to-source voltage is

$$V_{DS} = V_D - V_S = 2.5 - (-2.24) = 4.74\,V$$

Since $V_{DS} = 4.74\,V > V_{DS}(\text{sat}) = V_{GS} - V_{TN} = 2.24 - 0.8 = 1.44\,V$, the transistor is biased in the saturation region, as initially assumed.

Comment: MOSFET circuits can be biased by using constant-current sources, which in turn are designed by using other MOS transistors.

Test Your Understanding

RD5.10 For the circuit shown in Figure 5.30(b), the transistor parameters are $V_{TN} = 1.2\,V$ and $K_n = 0.080\,mA/V^2$. Redesign the circuit by replacing the current source with a source resistor such that $I_D = 100\,\mu A$ and $V_{DS} = 4.5\,V$. (Ans. $R_S = 26.8\,k\Omega$ and $R_D = 28.2\,k\Omega$)

D5.11 Consider the circuit shown in Figure 5.31. The transistor parameters are $V_{TP} = -0.8\,V$ and $K_p = 0.050\,mA/V^2$. Design the circuit such that $I_D = 120\,\mu A$ and $V_{SD} = 8\,V$. (Ans. $R_S = 63.75\,k\Omega$, $R_D = 36.25\,k\Omega$)
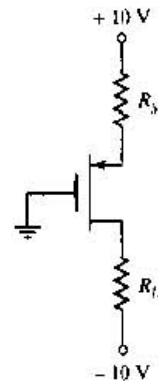
Figure 5.31 Circuit for Exercise 5.11

An enhancement-mode MOSFET connected in a configuration such as that shown in Figure 5.32 can be used as a nonlinear resistor. A transistor with this connection is called an **enhancement load device**. Since the transistor is an enhancement mode device, $V_{TN} > 0$. Also, for this circuit, $v_{DS} = v_{GS} > v_{DS}(\text{sat}) = v_{GS} - V_{TN}$, which means that the transistor is always biased in the saturation region. The general i_D versus v_{DS} characteristics can then be written as

$$i_D = K_n(v_{GS} - V_{TN})^2 = K_n(v_{DS} - V_{TN})^2 \tag{5.19}$$

Figure 5.33 shows a plot of Equation (5.19) for the case when $K_n = 1\,mA/V^2$ and $V_{TN} = 1\,V$.

In the next chapter, we will see how this transistor is used in place of a load resistor in an amplifier circuit. In later chapters, we will show how this transistor is used in digital logic circuits.
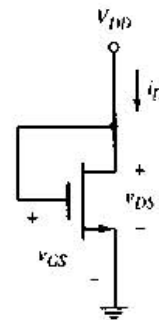
Figure 5.32 Enhancement-mode NMOS device with the gate connected to the drain

Figure 5.33   Current–voltage characteristic of an enhancement load device
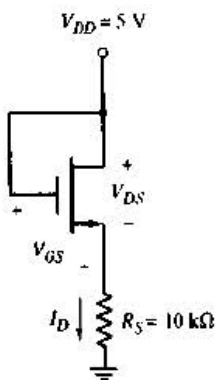
Figure 5.34   Circuit containing an enhancement load device

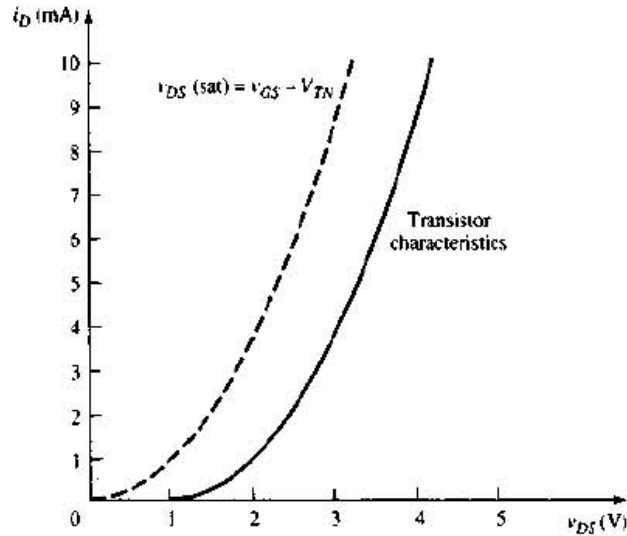**Example   5.8   Objective:** Calculate the characteristics of a circuit containing an enhancement load device.

Consider the circuit shown in Figure 5.34 with transistor parameters $V_{TN} = 0.8$ V and $K_n = 0.05\,\text{mA}/\text{V}^2$.

Solution: Since the transistor is biased in the saturation region, the dc drain current is given by

$$I_D = K_n(V_{GS} - V_{TN})^2$$

and the dc drain-to-source voltage is

$$V_{DS} = V_{GS} = 5 - I_D R_S$$

Combining these two equations, we obtain

$$V_{GS} = 5 - K_n R_S(V_{GS} - V_{TN})^2$$

Substituting parameter values, we obtain

$$V_{GS} = 5 - (0.05)(10)(V_{GS} - 0.8)^2$$

which can be written as

$$0.5V_{GS}^2 + 0.2V_{GS} - 4.68 = 0$$

The two possible solutions are

$$V_{GS} = -3.27\,\text{V} \quad \text{and} \quad V_{GS} = +2.87\,\text{V}$$

Since we are assuming the transistor is conducting, the gate-to-source voltage must be greater than the threshold voltage. We therefore have the following solution:

$$V_{GS} = V_{DS} = 2.87\,\text{V} \quad \text{and} \quad I_D = 0.213\,\text{mA}$$

Comment: This particular circuit is obviously not an amplifier. However, the transistor connected in this configuration is extremely useful as an effective load resistor.

Test Your Understanding

5.12 The parameters for the circuit shown in Figure 5.34 are changed to $V_{DD} = 10$ V and $R_S = 10$ kΩ, and the transistor parameters are $V_{TN} = 2$ V and $K_n = 0.20$ mA/V^2. Calculate I_D, V_{DS}, and the power dissipated in the transistor. (Ans. $V_{GS} = V_{DS} = 3.77$ V, $I_D = 0.623$ mA, $P = 2.35$ mW)

D5.13 The parameters for the circuit shown in Figure 5.34 are $V_{DD} = 5$ V and $R_S = 5$ kΩ. The transistor threshold voltage is $V_{TN} = 1$ V. If $k_n' = 40$ μA/V^2, design the transistor width-to-length ratio such that $V_{DS} = 2.2$ V. (Ans. $W/L = 19.5$)

If an enhancement load device is connected in a circuit with another MOSFET in the configuration in Figure 5.35, the circuit can be used as an amplifier or as an inverter in a digital logic circuit. The load device, M_L, is always biased in the saturation region, and the transistor M_D, called the **driver transistor**, can be biased in either the saturation or nonsaturation region, depending on the value of the input voltage. The next example addresses the dc analysis of this circuit for dc input voltages to the gate of M_D.
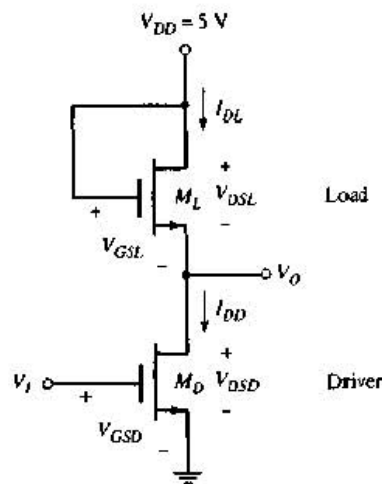
Figure 5.35 Circuit with enhancement load device and NMOS driver

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Example 5.9 **Objective:** Determine the dc transistor currents and voltages in a circuit containing an enhancement load device.

The transistors in the circuit shown in Figure 5.35 have parameters $V_{TND} = V_{TNL} = 1$ V, $K_{nD} = 50$ μA/V^2, and $K_{nL} = 10$ μA/V^2. (The subscript D applies to the driver transistor and the subscript L applies to the load transistor.) Determine V_O for $V_I = 5$ V and $V_I = 1.5$ V.

Solution: ($V_I = 5$ V) Assume that the driver transistor M_D is biased in the nonsaturation region. The drain current in the load device is equal to the drain current in the driver transistor. Writing these currents in generic form, we have

$$I_{DD} = I_{DL}$$

or

$$K_{nD}[2(V_{GSD} - V_{TND})V_{DSD} - V_{DSD}^2] = K_{nL}[V_{GSL} - V_{TNL}]^2$$

Since $V_{GSD} = V_I$, $V_{DSD} = V_O$, and $V_{GSL} = V_{DSL} = V_{DD} - V_O$, then

$$K_{nD}[2(V_I - V_{TND})V_O - V_O^2] = K_{nL}[V_{DD} - V_O - V_{TNL}]^2$$

Substituting numbers, we find

$$(50)[2(5 - 1)V_O - V_O^2] = (10)[5 - V_O - 1]^2$$

Rearranging the terms provides

$$3V_O^2 - 24V_O + 8 = 0$$

Using the quadratic formula, we obtain two possible solutions:

$$V_O = 7.65\,\text{V} \quad \text{or} \quad V_O = 0.349\,\text{V}$$

Since the output voltage cannot be greater than the supply voltage $V_{DD} = 5\,\text{V}$, the valid solution is $V_O = 0.349\,\text{V}$.

Also, since $V_{DSD} = V_O = 0.349\,\text{V} < V_{GSD} - V_{TND} = 5 - 1 = 4\,\text{V}$, the driver M_D is biased in the nonsaturation region, as initially assumed.

The current can be determined from

$$I_D = K_{nL}(V_{GSL} - V_{TNL})^2 = K_{nL}(V_{DD} - V_O - V_{TNL})^2$$

or

$$I_D = (10)(5 - 0.349 - 1)^2 = 133\,\mu\text{A}$$

Solution: ($V_I = 1.5\,\text{V}$) Assume that the driver transistor M_D is biased in the saturation region. Equating the currents in the two transistors and writing the current equations in generic form, we have

$$I_{DD} = I_{DL}$$

or

$$K_{nD}[V_{GSD} - V_{TND}]^2 = K_{nL}[V_{GSL} - V_{TNL}]^2$$

Again, since $V_{GSD} = V_I$ and $V_{GSL} = V_{DSL} = V_{DD} - V_O$, then

$$K_{nD}[V_I - V_{TND}]^2 = K_{nL}[V_{DD} - V_O - V_{TNL}]^2$$

Substituting numbers and taking the square root, we find

$$\sqrt{50}[1.5 - 1] = \sqrt{10}[5 - V_O - 1]$$

which yields $V_O = 2.88\,\text{V}$.

Since $V_{DSD} = V_O = 2.88\,\text{V} > V_{GSD} - V_{TND} = 1.5 - 1 = 0.5\,\text{V}$, the driver transistor M_D is biased in the saturation region, as initially assumed.

The current is

$$I_D = K_{nD}(V_{GSD} - V_{TND})^2 = (50)(1.5 - 1)^2 = 12.5\,\mu\text{A}$$

Comment: For this example, we made an initial guess as to whether the driver transistor was biased in the saturation or nonsaturation region. A more analytical approach is shown following this example.

Computer Simulation: The voltage transfer characteristics of the NMOS inverter circuit with the enhancement load shown in Figure 5.35 were obtained by a PSpice analysis. These results are shown in Figure 5.36. For an input voltage less than 1 V, the driver is cut off and the output voltage is $V_O = V_{DD} - V_{TNL} = 5 - 1 = 4\,\text{V}$. As the
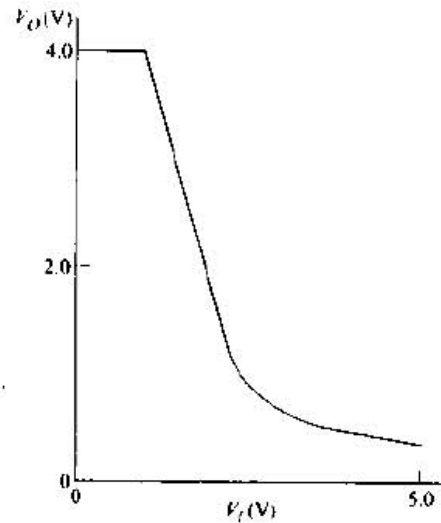
Figure 5.36 Voltage transfer characteristics of NMOS inverter with enhancement load device

input voltage decreases, the output voltage increases, charging and discharging capacitances in the transistors. When the current goes to zero at $V_I = 1$ V and $V_O = 4$ V, the capacitances cease charging and discharging so the output voltage cannot get to the full $V_{DD} = 5$ V value.

When the input voltage is just greater than 1 V, both transistors are biased in the saturation region as the previous analsys for $V_I = 1.5$ V showed. The output voltage is a linear function of input voltage.

For an input voltage greater than approximately 2.25 V, the driver transistor is biased in the nonsaturation region and the output voltage is a nonlinear function of the input voltage.

In the circuit shown in Figure 5.35, we can determine the transition point for the driver transistor that separates the saturation and nonsaturation regions. The transition point is determined by the equation

$$V_{DSD}(\text{sat}) = V_{GSD} - V_{TND} \tag{5.20}$$

Again, the drain currents in the two transistors are equal. Using the saturation drain current relationship for the driver transistor, we have

$$I_{DD} = I_{DL} \tag{5.21(a)}$$

or

$$K_{nD}[V_{GSD} - V_{TND}]^2 = K_{nL}[V_{GSL} - V_{TNL}]^2 \tag{5.21(b)}$$

Again, noting that $V_{GSD} = V_I$ and $V_{GSL} = V_{DSL} = V_{DD} - V_O$, and taking the square root, we have

$$\sqrt{\frac{K_{nD}}{K_{nL}}}(V_I - V_{TND}) = (V_{DD} - V_O - V_{TNL}) \tag{5.22}$$

At the transition point, we can define the input voltage as $V_I = V_{It}$ and the output voltage as $V_{Ot} = V_{DSD}(\text{sat}) = V_{It} - V_{TND}$. Then, from Equation (5.22), the input voltage at the transition point is

$$V_{It} = \frac{V_{DD} - V_{TNL} + V_{TND}(1 + \sqrt{K_{nD}/K_{nL}})}{1 + \sqrt{K_{nD}/K_{nL}}} \tag{5.23}$$

If we apply Equation (5.23) to the previous example, we can show that our initial assumptions were correct.

Test Your Understanding

5.14 For the circuit shown in Figure 5.35, use the transistor parameters given in Example 5.9. (a) Determine V_I and V_O at the transition point for the driver transistor. (b) Calculate the transistor currents at the transition point. (Ans. (a) $V_{It} = 2.24$ V, $V_{Ot} = 1.24$ V; (b) $I_D = 76.9 \,\mu\text{A}$)

D5.15 Consider the circuit shown in Figure 5.35 with transistor parameters $V_{TND} = V_{TNL} = 1$ V. (a) Design the ratio K_{nD}/K_{nL} that will produce a transition point at $V_I = 2.5$ V. (b) Using the results of part (a), find V_O for $V_I = 5$ V. (Ans. (a) $K_{nD}/K_{nL} = 2.78$ (b) $V_O = 0.57$ V)

Up to this point, we have only considered the n-channel enhancement-mode MOSFET as a load device. An n-channel depletion-mode MOSFET can also be used. Consider the depletion-mode MOSFET with the gate and source connected together shown in Figure 5.37(a). The current-voltage characteristics are shown in Figure 5.37(b). The transistor may be biased in either the saturation or nonsaturation regions. The transition point is also shown on the plot. The threshold voltage of the n-channel depletion-mode MOSFET is negative so that $v_{DS}(\text{sat})$ is positive.
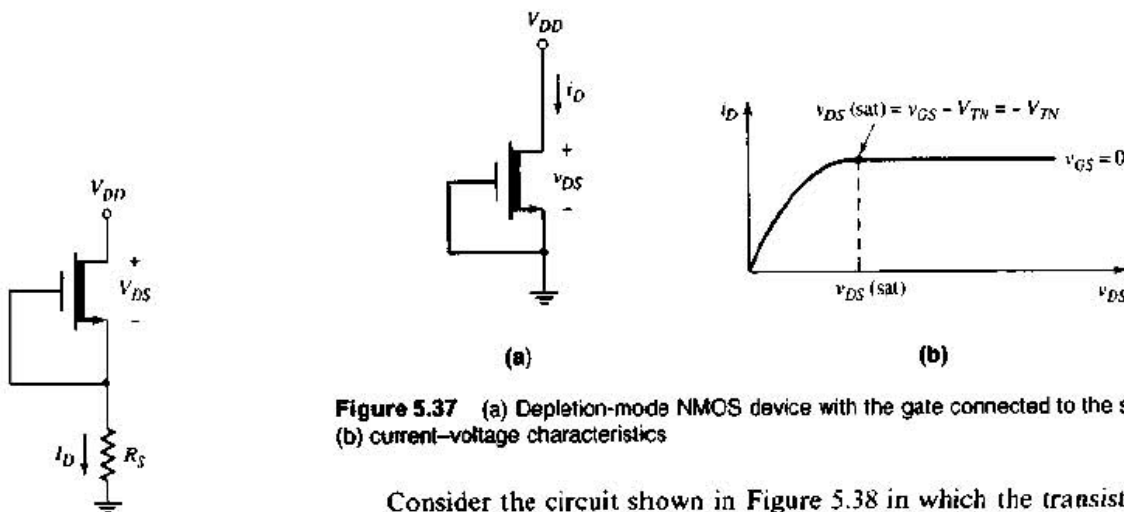
Figure 5.37 (a) Depletion-mode NMOS device with the gate connected to the source and (b) current-voltage characteristics

Consider the circuit shown in Figure 5.38 in which the transistor is *being* used as a **depletion load device**. It may be biased in the saturation or nonsaturation region, depending on the values of the transistor parameters and V_{DD} and R_S.

Figure 5.38 Circuit containing a depletion load device

Example 5.10 Objective: Calculate the characteristics of a circuit containing a depletion load device.

For the circuit shown in Figure 5.38 the transistor parameters are $V_{TN} = -2\,\text{V}$ and $K_n = 0.1\,\text{mA/V}^2$. Assume that $V_{DD} = 5\,\text{V}$ and $R_S = 5\,\text{k}\Omega$.

Solution: If we assume that the transistor is biased in the saturation region, then the dc drain current is

$$I_D = K_n(V_{GS} - V_{TN})^2 = K_n(-V_{TN})^2 = (0.1)(-(-2))^2 = 0.4\,\text{mA}$$

In this case, the transistor is acting as a constant-current source. The dc drain-to-source voltage is

$$V_{DS} = V_{DD} - I_D R_S = 5 - (0.4)(5) = 3\,\text{V}$$

Since

$$V_{DS} = 3\,\text{V} > V_{DS}(\text{sat}) = V_{GS} - V_{TN} = 0 - (-2) = 2\,\text{V}$$

the transistor is biased in the saturation region.

Comment: Although this circuit is also not an amplifier, this transistor configuration is useful as an effective load resistor in both analog and digital circuits.

Test Your Understanding

5.16 For the circuit shown in Figure 5.38, the circuit parameters are $V_{DD} = 10\,\text{V}$ and $R_S = 4\,\text{k}\Omega$, and the transistor parameters are $V_{TN} = -2.5\,\text{V}$ and $K_n = 0.25\,\text{mA/V}^2$. Calculate I_D, V_{DS}, and the power dissipated in the transistor. Is the transistor biased in the saturation or nonsaturation region? (Ans. $I_D = 1.56\,\text{mA}$, $V_{DS} = 3.76\,\text{V}$, $P = 5.87\,\text{mW}$, saturation region)

D5.17 The parameters for the circuit shown in Figure 5.38 are $V_{DD} = 5\,\text{V}$ and $R_S = 8\,\text{k}\Omega$. The transistor threshold voltage is $V_{TN} = -1.8\,\text{V}$. If $k_n' = 35\,\mu\text{A/V}^2$, design the transistor width-to-length ratio such that $V_{DS} = 1.2\,\text{V}$. Is the transistor biased in the saturation or nonsaturation region? (Ans. $W/L = 9.43$, nonsaturation)

A depletion load device can be used in conjunction with another MOSFET, as shown in Figure 5.39, to create a circuit that can be used as an amplifier or as an inverter in a digital logic circuit. Both the load device M_L and driver transistor M_D may be biased in either the saturation or nonsaturation region, depending on the value of the input voltage. We will perform the dc analysis of this circuit for a particular dc input voltage to the gate of the driver transistor.

Example 5.11 Objective: Determine the dc transistor currents and voltages in a circuit containing a depletion load device.

Consider the circuit shown in Figure 5.39 with transistor parameters: $V_{TND} = 1\,\text{V}$, $V_{TNL} = -2\,\text{V}$, $K_{nD} = 50\,\mu\text{A/V}^2$, and $K_{nL} = 10\,\mu\text{A/V}^2$. Determine V_O for $V_I = 5\,\text{V}$.
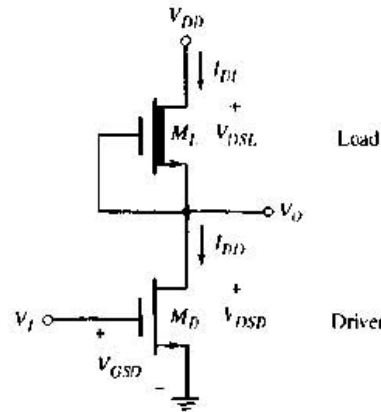
Figure 5.39 Circuit with depletion load device and NMOS driver

Solution: Assume the driver transistor M_D is biased in the nonsaturation region and the load transistor M_L is biased in the saturation region. The drain currents in the two transistors are equal. In generic form, these currents are

$$I_{DD} = I_{DL}$$

or

$$K_{nD}[2(V_{GSD} - V_{TND})V_{DSD} - V_{DSD}^2] = K_{nL}[V_{GSL} - V_{TNL}]^2$$

Since $V_{GSD} = V_I$, $V_{DSD} = V_O$, and $V_{GSL} = 0$, then

$$K_{nD}[2(V_I - V_{TND})V_O - V_O^2] = K_{nL}[-V_{TNL}]^2$$

Substituting numbers, we find

$$(50)[2(5 - 1)V_O - V_O^2] = (10)[-(-2)]^2$$

Rearranging the terms produces

$$5V_O^2 - 40V + 4 = 0$$

Using the quadratic formula, we obtain two possible solutions:

$$V_O = 7.90 \text{ V} \quad \text{or} \quad V_O = 0.10 \text{ V}$$

Since the output voltage cannot be greater than the supply voltage $V_{DD} = 5$ V, the valid solution is $V_O = 0.10$ V.
   The current is

$$I_D = K_{nL}(-V_{TNL})^2 = (10)[-(-2)]^2 = 40 \text{ µA}$$

Comment: Since $V_{DSD} = V_O = 0.10$ V $< V_{GSD} - V_{TND} = 5 - 1 = 4$ V, M_D is biased in the nonsaturation region, as assumed. Similarly, since $V_{DSL} = V_{DD} - V_O = 4.9$ V $> V_{GSL} - V_{TNL} = 0 - (-2) = 2$ V, M_L is biased in the saturation region, as originally assumed.

Computer Simulation: The voltage transfer characteristics of the NMOS inverter circuit with depletion load in Figure 5.39 were obtained using a PSpice analysis. These results are shown in Figure 5.40. For an input voltage less than 1 V, the driver is cut off and the output voltage is $V_O = V_{DD} = 5$ V.
   When the input voltage is just greater than 1 V, the driver transistor is biased in the saturation region and the load device in the nonsaturation region. When the input voltage is approximately 1.9 V, both transistors are biased in the saturation region. If
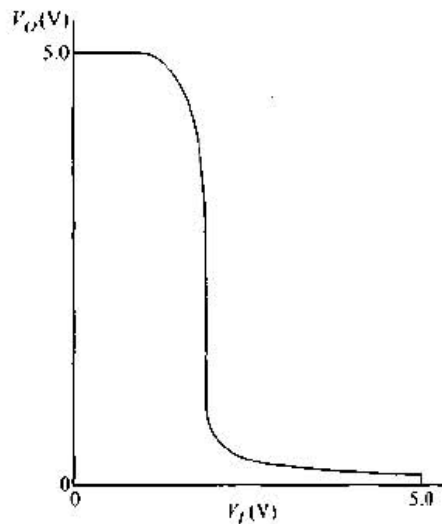
Figure 5.40 Voltage transfer characteristics of NMOS inverter with depletion load device

the channel length modulation parameter λ is assumed to be zero as in this example, there is no change in the input voltage during this transition region. As the input voltage becomes larger than 1.9 V, the driver is biased in the nonsaturation region and the load in the saturation region.

Test Your Understanding

5.18 For the circuit shown in Figure 5.39, use the transistor parameters given in Example 5.11. (a) Determine V_I and V_O at the transition point for the load transistor. (b) Determine V_I and V_O at the transition point for the driver transistor. (Ans. (a) $V_{It} = 1.89$ V, $V_{Ot} = 3$ V; (b) $V_{It} = 1.89$ V, $V_{Ot} = 0.89$ V)

D5.19 Consider the circuit shown in Figure 5.39 with transistor parameters $V_{TND} = 1$ V and $V_{TNL} = -2$ V. (a) Design the ratio K_{nD}/K_{nL} that will produce an output voltage of $V_O = 0.25$ V at $V_I = 5$ V. (b) Find K_{nD} and K_{nL} if the transistor currents are 0.2 mA when $V_I = 5$ V. (Ans. (a) $K_{nD}/K_{nL} = 2.06$ (b) $K_{nL} = 50\,\mu A/V^2$, $K_{nD} = 103\,\mu A/V^2$)

A p-channel enhancement-mode transistor can also be used as a load device to form a **complementary MOS (CMOS)** inverter. The term complementary implies that both n-channel and p-channel transistors are used in the same circuit. The CMOS technology is used extensively in both analog and digital electronic circuits.

Figure 5.41 shows one example of a CMOS inverter. The NMOS transistor is used as the amplifying device, or the driver, and the PMOS device is the load, which is referred to as an active load. This configuration is typically used in analog applications. In another configuration, the two gates are tied together and forms the input. This configuration will be discussed in detail in Chapter 16.
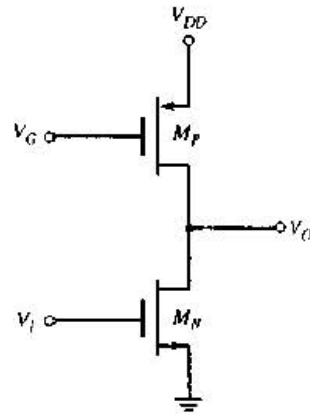
Figure 5.41 Example of CMOS inverter

As with the previous two NMOS inverters, the two transistors shown in Figure 5.41 may be biased in either the saturation or nonsaturation region, depending on the value of the input voltage. The voltage transfer characteristic is most easily determined from a PSpice analysis.

Example 5.12 Objective: Determine the voltage transfer characteristic of the CMOS inverter using a PSpice analysis.

For the circuit shown in Figure 5.41, assume transistor parameters of $V_{TN} = 1$ V, $V_{TP} = -1$ V, and $K_n = K_p$. Also assume $V_{DD} = 5$ V and $V_G = 3.25$ V.

Solution: The voltage transfer characteristics are shown in Figure 5.42. In this case, there is a region, as was the case for an NMOS inverter with depletion load, in which both transistors are biased in the saturation region, and the input voltage is a constant over this transition region for the assumption that the channel length modulation parameter λ is zero.
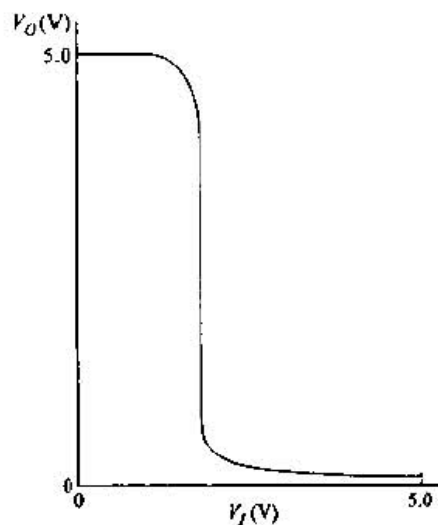

Figure 5.42 Voltage transfer characteristics of CMOS inverter in Figure 5.41

Comment: In this example, the source-to-gate voltage of the PMOS device is only $V_{SG} = 0.75$ V. The effective resistance looking into the drain of the PMOS device is then relatively large. This is a desirable characteristic for an amplifier, as we will see in the next chapter.

5.2.4 Constant-Current Source Biasing

As was shown in Figure 5.30, a MOSFET can be biased by using a constant-current source I_Q. The advantage of this circuit is that the drain current is independent of the transistor parameters.

The constant-current source can be implemented by using MOSFETs as shown in Figure 5.43. The transistors M_2, M_3, and M_4 form the current source. Transistors M_3 and M_4 are each connected in a diode-type configuration, and they establish a reference current. We noted in the last section that this diode-type connection implies the transistor is always biased in the saturation region. Transistors M_3 and M_4 are therefore biased in the saturation region, and M_2 is assumed to be biased in the saturation region. The resulting gate-to-source voltage on M_3 is applied to M_2, and this establishes the bias current I_Q.
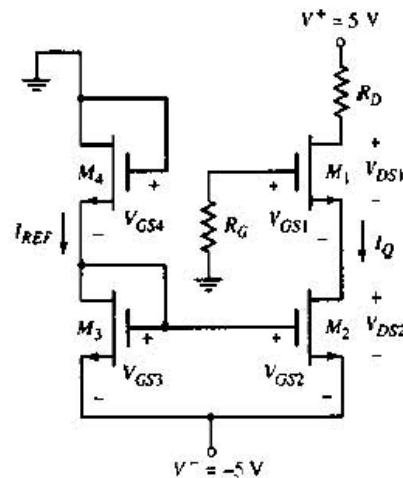

Figure 5.43 Implementation of a MOSFET constant-current source

Since the reference current is the same in transistors M_3 and M_4, we can write

$$K_{n3}(V_{GS3} - V_{TN3})^2 = K_{n4}(V_{GS4} - V_{TN4})^2 \qquad (5.24)$$

We also know that

$$V_{GS4} + V_{GS3} = (-V^-) \qquad (5.25)$$

Solving Equation (5.25) for V_{GS4} and substituting the result into Equation (5.24) yields

$$V_{GS3} = \cfrac{\sqrt{\dfrac{K_{n4}}{K_{n3}}}[(-V^-) - V_{TN4}] + V_{TN3}}{1 + \sqrt{\dfrac{K_{n4}}{K_{n3}}}}$$

(5.26)

Since $V_{GS3} = V_{GS2}$, the bias current is

$$I_Q = K_{n2}(V_{GS3} - V_{TN2})^2$$

(5.27)

Example 5.13 Objective: Determine the currents and voltages in a MOSFET constant-current source.

For the circuit shown in Figure 5.43, the transistor parameters are: $K_{n1} = 0.2\,\text{mA/V}^2$, $K_{n2} = K_{n3} = K_{n4} = 0.1\,\text{mA/V}^2$, and $V_{TN1} = V_{TN2} = V_{TN3} = V_{TN4} = 1\,\text{V}$.

Solution: From Equation (5.26), we can determine V_{GS3}, as follows:

$$V_{GS3} = \cfrac{\sqrt{\dfrac{0.1}{0.1}}[5 - 1] + 1}{1 + \sqrt{\dfrac{0.1}{0.1}}} = 2.5\,\text{V}$$

Since M_3 and M_4 are identical transistors, V_{GS3} should be one-half of the bias voltage. The bias current I_Q is then

$$I_Q = (0.1) \cdot (2.5 - 1)^2 = 0.225\,\text{mA}$$

The gate-to-source voltage on M_1 is found from

$$I_Q = K_{n1}(V_{GS1} - V_{TN1})^2$$

or

$$0.225 = (0.2) \cdot (V_{GS1} - 1)^2$$

which yields

$$V_{GS1} = 2.06\,\text{V}$$

The drain-to-source voltage on M_2 is

$$V_{DS2} = (-V^-) - V_{GS1} = 5 - 2.06 = 2.94\,\text{V}$$

Since $V_{DS2} = 2.94\,\text{V} > V_{DS}(\text{sat}) = V_{GS2} - V_{TN2} = 2.5 - 1 = 1.5\,\text{V}$, M_2 is biased in the saturation region.

Design Consideration: Since in this example M_2 and M_3 are identical transistors, the reference current I_{REF} and bias current I_Q are equal. By redesigning the width-to-length ratios of M_2, M_3, and M_4, we can obtain a specific bias current I_Q. If M_2 and M_3 are not identical, then I_Q and I_{REF} will not be equal. A variety of design options are possible with such a circuit configuration.

Test Your Understanding

D5.20 Consider the constant-current source shown in Figure 5.43. Assume that the threshold voltage of each transistor is $V_{TN} = 1$ V. (a) Design the ratio of K_{n4}/K_{n3} such that $V_{GS3} = 2$ V. (b) Determine K_{n2} such that $I_Q = 100\,\mu$A. (c) Find K_{n3} and K_{n4} such that $I_{REF} = 200\,\mu$A. (Ans. (a) $K_{n4}/K_{n3} = \frac{1}{4}$ (b) $K_{n2} = 0.1$ mA/V^2 (c) $K_{n3} = 0.2$ mA/V^2, $K_{n4} = 0.05$ mA/V^2)

5.3   BASIC MOSFET APPLICATIONS: SWITCH, DIGITAL LOGIC GATE, AND AMPLIFIER

MOSFETs may be used to: switch currents, voltages, and power; perform digital logic functions; and amplify small time-varying signals. In this section, we will examine the switching properties of an NMOS transistor, analyze a simple NMOS transistor digital logic circuit, and discuss how the MOSFET can be used to amplify small signals.

5.3.1   NMOS Inverter

The MOSFET can be used as a switch in a wide variety of electronic applications. The transistor switch provides an advantage over mechanical switches in both speed and reliability. The transistor switch considered in this section is also called an inverter. Two other switch configurations, the NMOS transmission gate and the CMOS transmission gate, are discussed in Chapter 16.

Figure 5.44 shows the n-channel enhancement-mode MOSFET inverter circuit. If $v_I < V_{TN}$, the transistor is in cutoff and $i_D = 0$. There is no voltage drop across R_D, and the output voltage is $v_O = V_{DD}$. Also, since $i_D = 0$, no power is dissipated in the transistor.

If $v_I > V_{TN}$, the transistor is on and initially is biased in the saturation region, since $v_{DS} > v_{GS} - V_{TN}$. As the input voltage increases, the drain-to-source voltage decreases, and the transistor eventually becomes biased in the nonsaturation region. When $v_I = V_{DD}$, the transistor is biased in the nonsaturation region, v_O reaches a minimum value, and the drain current reaches a maximum value. The current and voltage are given by

$$i_D = K_n[2(v_I - V_{TN})v_O - v_O^2] \tag{5.28}$$

and

$$v_O = v_{DD} - i_D R_D \tag{5.29}$$

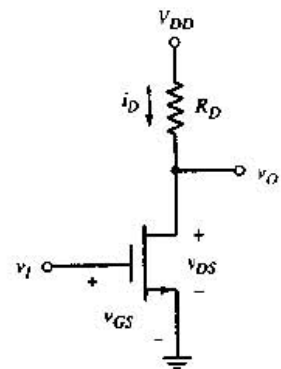where $v_O = v_{DS}$ and $v_I = v_{GS}$.

Figure 5.44   NMOS inverter circuit

Design Example 5.14   Objective: Design the size of a power MOSFET to meet the specification of a particular switch application.

The load in the inverter circuit in Figure 5.44 is a coil of an electromagnet that requires a current of 0.5 A when turned on. The effective load resistance varies between 8 and 10 Ω, depending on temperature and other variables. A 10 V power supply is available. The transistor parameters are $k_n' = 80\,\mu\text{A/V}^2$ and $V_{TN} = 1$ V.

Solution: One solution is to bias the transistor in the saturation region so that the current is constant, independent of the load resistance.

The minimum V_{DS} value is 5 V. We need $V_{DS} > V_{DS}(\text{sat}) = V_{GS} - V_{TN}$. If we bias the transistor at $V_{GS} = 5$ V, then the transistor will always be biased in the saturation region. We can then write

$$I_D = \frac{k_n'}{2} \cdot \frac{W}{L}(V_{GS} - V_{TN})^2$$

or

$$0.5 = \frac{80 \times 10^{-6}}{2}\left(\frac{W}{L}\right)\cdot(5 - 1)^2$$

which yields $W/L = 781$.

The maximum power dissipated in the transistor is

$$P(\text{max}) = V_{DS}(\text{max}) \cdot I_D = (6) \cdot (0.5) = 3\,\text{W}$$

Comment: We see that we can switch a relatively large drain current with essentially no input current to the transistor. The size of the transistor required is fairly large, which implies a power transistor is necessary. If a transistor with a slightly different width-to-length ratio is available, the applied V_{GS} can be changed to meet the specification.
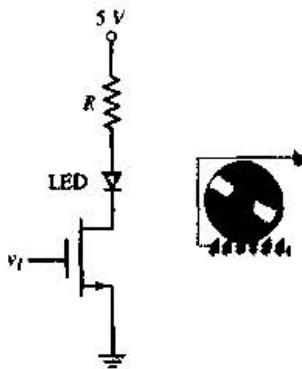

Test Your Understanding

5.21   For the MOS inverter circuit shown in Figure 5.44, assume the circuit values are: $V_{DD} = 5$ V and $R_D = 10\,\text{k}\Omega$. The threshold voltage of the transistor is $V_{TN} = 1$ V. Determine the value of the conduction parameter K_n such that $v_O = 1$ V when $v_I = 5$ V. What is the power dissipated in the transistor? (Ans. $K_n = 0.057\,\text{mA/V}^2$, $P = 0.4\,\text{mW}$)

D5.22   The circuit shown in Figure 5.44 is biased with $V_{DD} = 10$ V and the transistor has parameters $V_{TN} = 0.70$ V and $K_n = 0.050\,\text{mA/V}^2$. Design the value of R_D for which the output voltage will be $v_O = 0.35$ V, when $v_I = 10$ V. (Ans. $R_D = 30.3\,\text{k}\Omega$)

D5.23   The transistor in the circuit shown in Figure 5.45 has parameters $K_n = 4\,\text{mA/V}^2$ and $V_{TN} = 0.8$ V, and is used to switch the LED on and off. The LED cutin voltage is $V_\gamma = 1.5$ V. The LED is turned on by applying an input voltage of $v_I = 5$ V. (a) Determine the value of R such that the diode current is 12 mA. (b) From the results of part (a), what is the value of v_{DS}? (Ans. (a) $R = 261\,\Omega$, (b) $v_{DS} = 0.374$ V)

Figure 5.45

5.3.2 Digital Logic Gate

For the transistor inverter circuit in Figure 5.44, when the input is low and approximately zero volts, the transistor is cut off, and the output is high and equal to V_{DD}. When the input is high and equal to V_{DD}, the transistor is biased in the nonsaturation region and the output reaches a low value. Since the input voltages will be either high or low, we can analyze the circuit in terms of dc parameters.

Now consider the case when a second transistor is connected in parallel, as shown in Figure 5.46. If the two inputs are zero, both M_1 and M_2 are cut off, and $V_O = 5$ V. When $V_1 = 5$ V and $V_2 = 0$, the transistor M_1 turns on and M_2 is still cut off. Transistor M_1 is biased in the nonsaturation region, and V_O reaches a low value. If we reverse the input voltages such that $V_1 = 0$ and $V_2 = 5$ V, then M_1 is cut off and M_2 is biased in the nonsaturation region. Again, V_O is at a low value. If both inputs are high, at $V_1 = V_2 = 5$ V, then both transistors are biased in the nonsaturation region and V_O is low.
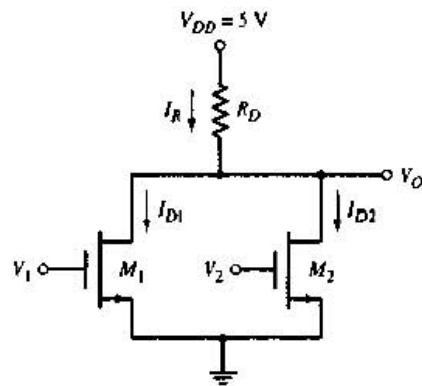

Figure 5.46 A two-input NMOS NOR logic gate

Table 5.2 shows these various conditions for the circuit in Figure 5.46. In a positive logic system, these results indicate that this circuit performs the NOR logic function, and, it is therefore called a two-input NOR logic circuit. In actual NMOS logic circuits, the resistor R_D is replaced by another NMOS transistor.

Table 5.2 NMOS NOR logic circuit response

V_1 (V)	V_2 (V)	V_O (V)
0	0	High
5	0	Low
0	5	Low
5	5	Low

Example 5.15   Objective: Determine the currents and voltages in a digital logic gate, for various input conditions.

Consider the circuit shown in Figure 5.46 with circuit and transistor parameters $R_D = 20\,\text{k}\Omega$, $K_n = 0.1\,\text{mA/V}^2$, and $V_{TN} = 0.8\,\text{V}$.

Solution: For $V_1 = V_2 = 0$, both M_1 and M_2 are cut off and $V_O = V_{DD} = 5\,\text{V}$. For $V_1 = 5\,\text{V}$ and $V_2 = 0$, the transistor M_1 is biased in the nonsaturation region, and we can write

$$I_R = I_{D1} = \frac{5 - V_O}{R_D} = K_n[2(V_1 - V_{TN})V_O - V_O^2]$$

Solving for the output voltage V_O, we obtain $V_O = 0.29\,\text{V}$.

The currents are

$$I_R = I_{D1} = \frac{5 - 0.29}{20} = 0.236\,\text{mA}$$

For $V_1 = 0$ and $V_2 = 5\,\text{V}$, we have $V_O = 0.29\,\text{V}$ and $I_R = I_{D2} = 0.236\,\text{mA}$. When both inputs go high to $V_1 = V_2 = 5\,\text{V}$, we have $I_R = I_{D1} + I_{D2}$, or

$$\frac{5 - V_O}{R_D} = K_n[2(V_1 - V_{TN})V_O - V_O^2] + K_n[2(V_2 - V_{TN})V_O - V_O^2]$$

which can be solved for V_O to yield $V_O = 0.147\,\text{V}$.

The currents are

$$I_R = \frac{5 - 0.147}{20} = 0.243\,\text{mA}$$

and

$$I_{D1} = I_{D2} = \frac{I_R}{2} = 0.121\,\text{mA}$$

Comment: When either transistor is biased on, it is biased in the nonsaturation region, since $V_{DS} < V_{DS}(\text{sat})$, and the output voltage reaches a low state.

This example and discussion illustrates that MOS transistors can be configured in a circuit to perform logic functions. A more detailed analysis and design of MOSFET logic gates and circuits is presented in Chapter 16.

Test Your Understanding

5.24 For the circuit in Figure 5.46, assume the circuit and transistor parameters are: $R_D = 30\,\text{k}\Omega$, $V_{TN} = 1\,\text{V}$, and $K_n = 50\,\mu\text{A/V}^2$. Determine V_O, I_R, I_{D1}, and I_{D2} for: (a) $V_1 = 5\,\text{V}$, $V_2 = 0$; and (b) $V_1 = V_2 = 5\,\text{V}$. (Ans. (a) $V_O = 0.40\,\text{V}$, $I_R = I_{D1} = 0.153\,\text{mA}$, $I_{D2} = 0$ (b) $V_O = 0.205\,\text{V}$, $I_R = 0.16\,\text{mA}$, $I_{D1} = I_{D2} = 0.080\,\text{mA}$)

5.25 In the circuit in Figure 5.46, let $R_D = 25\,\text{k}\Omega$ and $V_{TN} = 1\,\text{V}$. (a) Determine the value of the conduction parameter K_n required such that $V_O = 0.10\,\text{V}$ when $V_1 = 0$ and $V_2 = 5\,\text{V}$. (b) Using the results of part (a), find the value of V_O when $V_1 = V_2 = 5\,\text{V}$. (Ans. (a) $K_n = 0.248\,\text{mA/V}^2$, (b) $V_O = 0.0502\,\text{V}$)

5.3.3   MOSFET Small-Signal Amplifier

The MOSFET, in conjunction with other circuit elements, can amplify small time-varying signals. Figure 5.47(a) shows the MOSFET small-signal amplifier, which is a common-source circuit in which a time-varying signal is coupled to the gate through a coupling capacitor. Figure 5.47(b) shows the transistor characteristics and the load line. The load line is determined for $v_i = 0$.

We can establish a particular Q-point on the load line by designing the ratio of the bias resistors R_1 and R_2. If we assume that $v_i = V_i \sin \omega t$, the gate-to-source voltage will have a sinusoidal signal superimposed on the dc quiescent value. As the gate-to-source voltage changes over time, the Q-point will move up and down the line, as indicated in the figure.
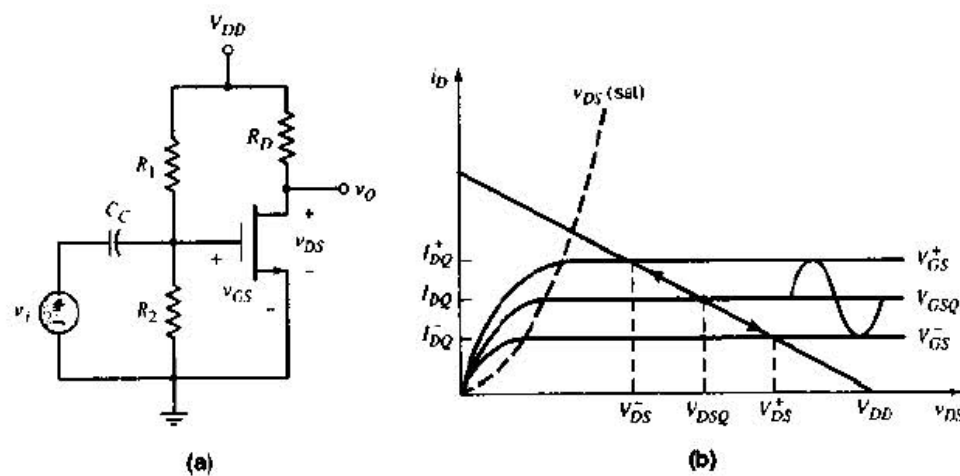
Figure 5.47   (a) An NMOS common-source circuit with a time-varying signal coupled to the gate and (b) transistor characteristics, load line, and superimposed sinusoidal signals

Moving up and down the load line translates into a sinusoidal variation in the drain current and in the drain-to-source voltage. The variation in output voltage can be larger than the input signal voltage, which means the input signal is amplified. The actual signal gain depends on both the transistor parameters and the circuit element values.

In the next chapter, we will develop an equivalent circuit for the transistor used to determine the time-varying small-signal gain and other characteristics of the circuit.

5.4   JUNCTION FIELD-EFFECT TRANSISTOR

The two general categories of **junction field-effect transistor (JFET)** are the pn junction FET, or **pn JFET**, and the **metal-semiconductor field-effect transistor (MESFET)**, which is fabricated with a Schottky barrier junction.

The current in a JFET is through a semiconductor region known as the channel, with ohmic contacts at each end. The basic transistor action is the modulation of the channel conductance by an electric field perpendicular to the

channel. Since the modulating electric field is induced in the space-charge region of a reverse-biased pn junction or Schottky barrier junction, the field is a function of the gate voltage. Modulation of the channel conductance by the gate voltage modulates the channel current.

JFETs were developed before MOSFETs, but the applications and uses of the MOSFET have far surpassed those of the JFET. One reason is that the voltages applied to the gate and drain of a MOSFET are the same polarity (both positive or both negative), whereas the voltages applied to the gate and drain of most JFETs must have opposite polarities. Since the JFET is used only in specialized applications, our discussion will be brief.

5.4.1   pn JFET and MESFET Operation

pn JFET

A simplified cross section of a symmetrical pn JFET is shown in Figure 5.48. In the n-region channel between the two p-regions, majority carrier electrons flow from the source to the drain terminal; thus, the JFET is called a majority-carrier device. The two gate terminals shown in Figure 5.48 are connected to form a single gate.
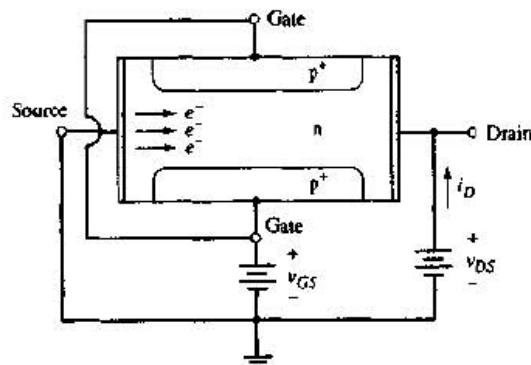

Figure 5.48   Cross section of a symmetrical n-channel pn junction field-effect transistor

In a p-channel JFET, the p- and n-regions are reversed from those of the n-channel device, and holes flow in the channel from the source to the drain. The current direction and voltage polarities in the p-channel JFET are reversed from those in the n-channel device. Also, the p-channel JFET is generally a lower-frequency device than the n-channel JFET, because hole mobility is lower than electron mobility.

Figure 5.49(a) shows an n-channel JFET with zero volts applied to the gate. If the source is at ground potential, and if a small positive drain voltage is applied, a drain current i_D is produced between the source and drain terminals. Since the n-channel acts essentially as a resistance, the i_D versus v_{DS} characteristic for small v_{DS} values is approximately linear, as shown in the figure.

If a voltage is applied to the gate of a pn JFET, the channel conductance changes. If a negative gate voltage is applied to the n-channel pn JFET in Figure 5.49, the gate-to-channel pn junction becomes reverse biased. The space-charge region widens, the channel region narrows, the resistance of the
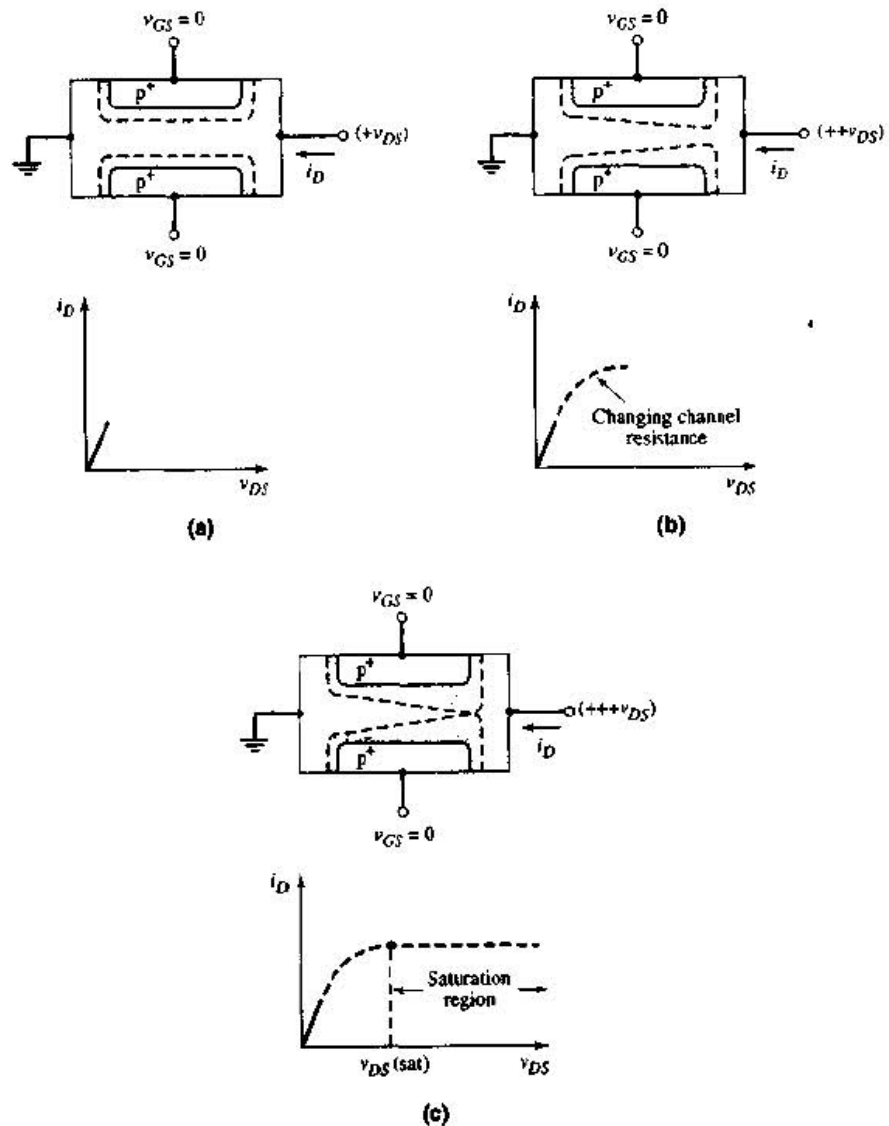
(a)

(b)

(c)
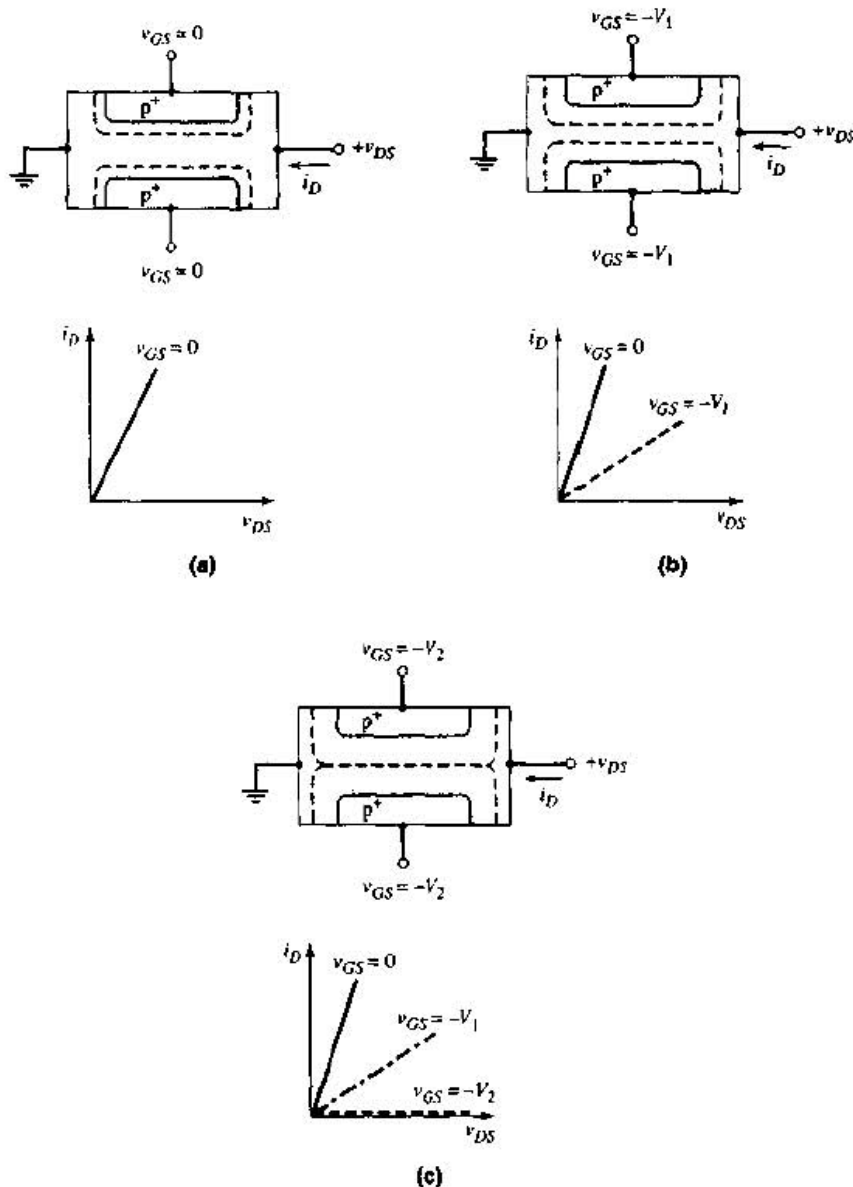
Figure 5.49   Gate-to-channel space-charge regions and current–voltage characteristics for small drain-to-source voltages and for: (a) zero gate voltage, (b) small reverse-biased gate voltage, and (c) a gate voltage that achieves pinchoff

n-channel increases, and the slope of the i_D versus v_{DS} curve, for small v_{DS}, decreases. These effects are shown in Figure 5.49(b). If a larger negative gate voltage is applied, the condition shown in Figure 5.49(c) can be achieved. The reverse-biased gate-to-channel space-charge region completely fills the channel region. This condition is known as **pinchoff**. Since the depletion region isolates the source and drain terminals, the drain current at pinchoff is essentially zero. The i_D versus v_{DS} curves are shown in Figure 5.49(c). The current in the channel is controlled by the gate voltage. The control of the current in one part of the device by a voltage in another part of the device is the basic transistor action. The pn JFET is a "normally on," or depletion mode, device; that is, a voltage must be applied to the gate terminal to turn the device off.

Consider the situation in which the gate voltage is zero, $v_{GS} = 0$, and the drain voltage changes, as shown in Figure 5.50(a). As the drain voltage increases (positive), the gate-to-channel pn junction becomes reverse biased near the drain terminal, and the space-charge region widens, extending farther into the channel. The channel acts essentially as a resistor, and the effective channel resistance increases as the space-charge region widens; therefore, the slope of the i_D versus v_{DS} characteristic decreases, as shown in Figure 5.50(b). The effective channel resistance now varies along the channel length, and, since the channel current must be constant, the voltage drop through the channel becomes dependent on position.

If the drain voltage increases further, the condition shown in Figure 5.50(c) can result. The channel is pinched off at the drain terminal. Any

(a)   (b)

(c)

Figure 5.50 Gate-to-channel space-charge regions and current–voltage characteristics for zero gate voltage and for: (a) a small drain voltage, (b) a larger drain voltage, and (c) a drain voltage that achieves pinchoff at the drain terminal

further increase in drain voltage will not increase the drain current. The i_D–v_{DS} characteristic for this condition is also shown in the figure. The drain voltage at pinchoff is $v_{DS}(\text{sat})$. Therefore, for $v_{DS} > v_{DS}(\text{sat})$, the transistor is biased in the saturation region, and the drain current for this ideal case is independent of v_{DS}.

MESFET

In the MESFET, the gate junction is a Schottky barrier junction, instead of a pn junction. Although MESFETs can be fabricated in silicon, they are usually associated with gallium arsenide or other compound-semiconductor materials.

A simplified cross section of a GaAs MESFET is shown in Figure 5.51. A thin, epitaxial layer of GaAs is used for the active region; the substrate is a very high resistivity GaAs material, referred to as a semi-insulating substrate. The advantages of these devices include: higher electron mobility in GaAs, hence smaller transit time and faster response; and decreased parasitic capacitance and a simplified fabrication process, resulting from the semi-insulating GaAs substrate.
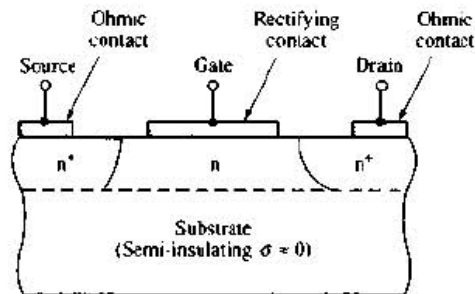

Figure 5.51   Cross section of an n-channel MESFET with a semi-insulating substrate

In the MESFET in Figure 5.51, a reverse-bias gate-to-source voltage induces a space-charge region under the metal gate, which modulates the channel conductance, as in the case of the pn JFET. If a negative applied gate voltage is sufficiently large, the space-charge region will eventually reach the substrate. Again, pinchoff will occur. Also, the device shown in the figure is a depletion mode device, since a gate voltage must be applied to pinch off the channel, that is, to turn the device off.

In another type of MESFET, the channel is pinched off even at $v_{GS} = 0$, as shown in Figure 5.52(a). For this MESFET, the channel thickness is smaller than the zero-biased space-charge width. To open a channel, the depletion region must be reduced; that is, a forward-biased voltage must be applied to the gate-semiconductor junction. When a slightly forward-bias voltage is applied, the depletion region extends just to the width of the channel as shown in Figure 5.52(b). The threshold voltage is the gate-to-source voltage required to create the pinchoff condition. The threshold voltage for this n-channel MESFET is positive, in contrast to the negative threshold voltage of the n-channel depletion-mode device. If a larger forward-bias voltage is applied, the channel region opens, as shown in Figure 5.52(c). The applied
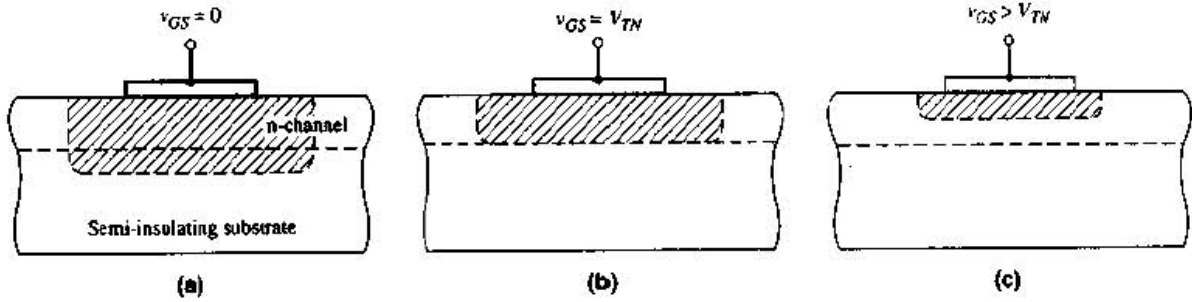
Figure 5.52 Channel space-charge region of an enhancement-mode MESFET for:
(a) $v_{GS} = 0$, (b) $v_{GS} = V_{TN}$, and (c) $v_{GS} > V_{TN}$

forward-bias gate voltage is limited to a few tenths of a volt before a significant gate current occurs.

This device is an **n-channel enhancement-mode MESFET**. Enhancement-mode p-channel MESFETs and enhancement-mode pn JFETs have also been fabricated. The advantage of enhancement-mode MESFETs is that circuits can be designed in which the voltage polarities on the gate and drain are the same. However, the output voltage swing of these devices is quite small.

5.4.2 Current–Voltage Characteristics

The circuit symbols for the n-channel and p-channel JFETs are shown in Figure 5.53, along with the gate-to-source voltages and current directions. The ideal current–voltage characteristics, when the transistor is biased in the saturation region, are described by

$$i_D = I_{DSS}\left(1 - \frac{v_{GS}}{V_P}\right)^2 \tag{5.30}$$

where I_{DSS} is the saturation current when $v_{GS} = 0$, and V_P is the **pinchoff voltage**.

The current–voltage characteristics for n-channel and p-channel JFETs are shown in Figures 5.54(a) and 5.54(b), respectively. Note that the pinchoff voltage V_P for the n-channel JFET is negative and the gate-to-source voltage v_{GS} is usually negative; therefore, the ratio v_{GS}/V_P is positive. Similarly, the pinchoff voltage V_P for the p-channel JFET is positive and the gate-to-source voltage v_{GS} must be positive, and therefore the ratio v_{GS}/V_P is positive.
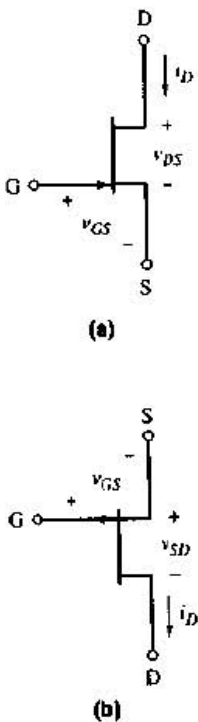
For the n-channel device, the saturation region occurs when $v_{DS} \geq v_{DS}(\text{sat})$ where

$$v_{DS}(\text{sat}) = v_{GS} - V_P \tag{5.31}$$

For the p-channel device, the saturation region occurs when $v_{SD} \geq v_{SD}(\text{sat})$ where

$$v_{SD}(\text{sat}) = V_P - v_{GS} \tag{5.32}$$

The voltage transfer characteristics of i_D versus v_{GS}, when the transistor is biased in the saturation region, are shown in Figure 5.55, for both the n-channel and p-channel JFET.

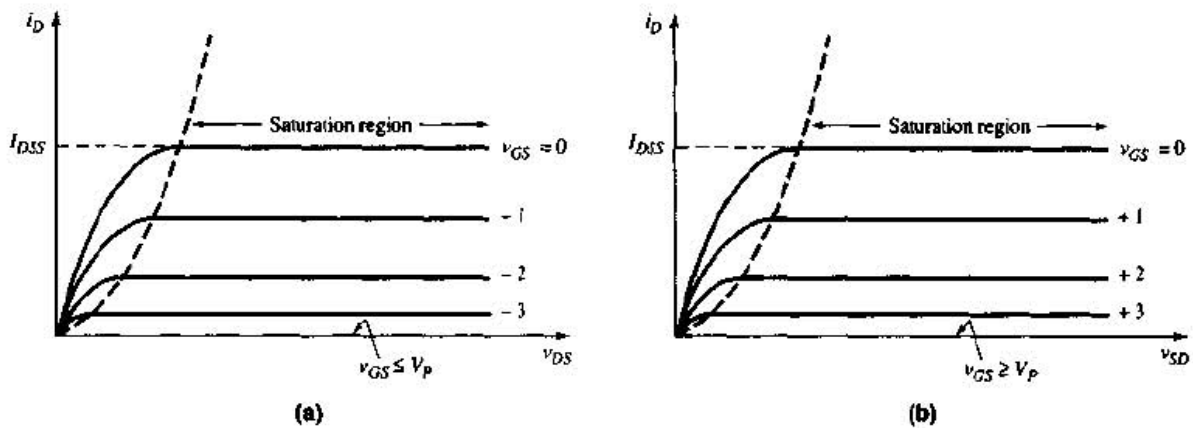**Figure 5.53** Circuit symbols for: (a) n-channel JFET and (b) p-channel JFET

Figure 5.54 Current–voltage characteristics for: (a) n-channel JFET and (b) p-channel JFET
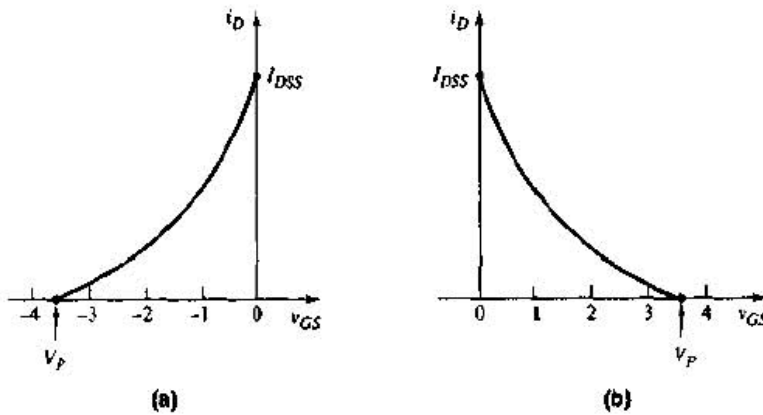

Figure 5.55 Drain current versus gate-to-source voltage characteristics for the transistor biased in the saturation region (a) n-channel JFET and (b) p-channel JFET.

Example 5.16 Objective: Calculate i_D and $v_{DS}(\text{sat})$ in an n-channel pn JFET.

Assume the saturation current is $I_{DSS} = 2\,\text{mA}$ and the pinchoff voltage is $V_P = -3.5\,\text{V}$. Calculate i_D and $v_{DS}(\text{sat})$ for $v_{GS} = 0$, $V_P/4$, and $V_P/2$.

Solution: From Equation (5.30), we have

$$i_D = I_{DSS}\left(1 - \frac{v_{GS}}{V_P}\right)^2 = (2)\left(1 - \frac{v_{GS}}{(-3.5)}\right)^2$$

Therefore, for $v_{GS} = 0$, $V_P/4$, and $V_P/2$, we obtain

$$i_D = 2, 1.13, \text{ and } 0.5\,\text{mA}$$

From Equation (5.31), we have

$$v_{DS}(\text{sat}) = v_{GS} - V_P = v_{GS} - (-3.5)$$

Therefore, for $v_{GS} = 0$, $V_P/4$, and $V_P/2$, we obtain

$$v_{DS}(\text{sat}) = 3.5, 2.63, \text{ and } 1.75\,\text{V}$$

Comment: The current capability of a JFET can be increased by increasing the value of I_{DSS}, which is a function of the transistor width.

As for the MOSFET, the i_D versus v_{DS} characteristic may have a nonzero slope beyond the saturation point. This nonzero slope can be described through the following equation:

$$i_D = I_{DSS}\left(1 - \frac{v_{GS}}{V_P}\right)^2 (1 + \lambda v_{DS}) \tag{5.33}$$

where λ^{-1} is analogous to the Early voltage in bipolar transistors.

The output resistance r_o is defined as

$$r_o = \left(\frac{\partial i_D}{\partial v_{DS}}\right)^{-1}\Bigg|_{v_{GS}=const.} \tag{5.34}$$

Using Equation (5.33), we find that

$$r_o = \left[\lambda I_{DSS}\left(1 - \frac{V_{GSQ}}{V_P}\right)^2\right]^{-1} \tag{5.35(a)}$$

or

$$r_o \cong [\lambda I_{DQ}]^{-1} = \frac{1}{\lambda I_{DQ}} \tag{5.35(b)}$$

The output resistance will be considered again when we discuss the small-signal equivalent circuit of the JFET in the next chapter.

Enhancement-mode GaAs MESFETs can be fabricated with current-voltage characteristics much like those of the enhancement-mode MOSFET. Therefore, for the ideal enhancement-mode MESFET biased in the saturation region, we can write

$$i_D = K_n(v_{GS} - V_{TN})^2 \tag{5.36(a)}$$

For the ideal enhancement-mode MESFET biased in the nonsaturation region,

$$i_D = K_n[2(v_{GS} - V_{TN})v_{DS} - v_{DS}^2] \tag{5.36(b)}$$

where K_n is the conduction parameter and V_{TN} is the threshold voltage, which in this case is equivalent to the pinchoff voltage. For an n-channel enhancement-mode MESFET, the threshold voltage is positive.

Test Your Understanding

5.26 The parameters of an n-channel JFET are $I_{DSS} = 12\,mA$, $V_P = -4.5\,V$, and $\lambda = 0$. Determine $V_{DS}(sat)$ for $V_{GS} = -1.2\,V$, and calculate I_D for $V_{DS} > V_{DS}(sat)$. (Ans. $V_{DS}(sat) = 3.3\,V$, $I_D = 6.45\,mA$)

5.27 For an n-channel JFET, the parameters are: $I_{DSS} = 2\,mA$, $V_P = -2.5\,V$, and $\lambda = 0$. What is the value of V_{GS} when $I_D = 1.2\,mA$ and the transistor is biased in the saturation region? (Ans. $V_{GS} = -0.564\,V$)

5.28 A p-channel JFET has a pinchoff voltage of $V_P = 3.8\,\text{V}$. The drain current in the saturation region is $I_D = 3\,\text{mA}$ when $V_{GS} = 0.8\,\text{V}$. Determine I_{DSS} and $V_{SD}(\text{sat})$. (Ans. $I_{DSS} = 4.81\,\text{mA}$, $V_{SD}(\text{sat}) = 3.0\,\text{V}$)

5.29 An n-channel GaAs MESFET has parameters $K_n = 25\,\mu\text{A}/\text{V}^2$ and $V_{TN} = 0.25\,\text{V}$. Determine I_D in the saturation region for: (a) $V_{GS} = 0.35\,\text{V}$, and (b) $V_{GS} = 0.50\,\text{V}$. (Ans. (a) $I_D = 0.25\,\mu\text{A}$, (b) $I_D = 1.56\,\mu\text{A}$)

5.4.3   Common JFET Configurations: DC Analysis

There are several common JFET circuit configurations. We will look at a few of these, using examples, and will illustrate the dc analysis and design of such circuits.

Design Example 5.17   Objective: Design the dc bias of a JFET circuit with an n-channel depletion-mode JFET.

For the circuit in Figure 5.56(a), the transistor parameters are: $I_{DSS} = 5\,\text{mA}$, $V_P = -4\,\text{V}$, and $\lambda = 0$. Design the circuit such that $I_D = 2\,\text{mA}$ and $V_{DS} = 6\,\text{V}$.
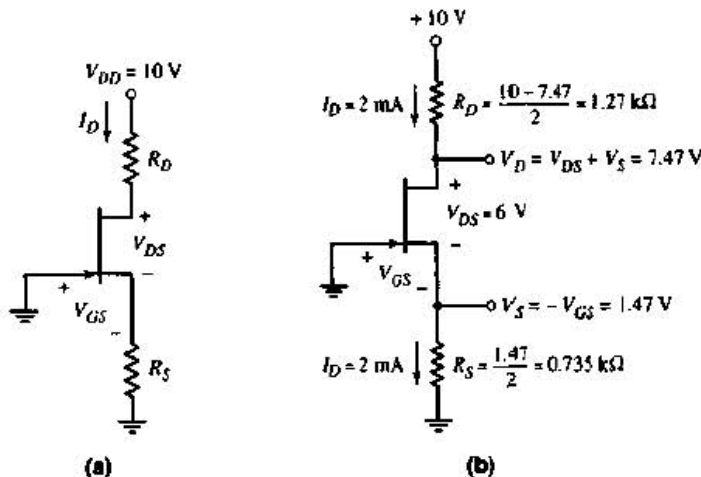
Figure 5.56   (a) An n-channel JFET circuit with a self-biasing source resistor and (b) circuit for Example 5.16

Solution: Assume the transistor is biased in the saturation region. The dc drain current is then given by

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

or

$$2 = 5\left(1 - \frac{V_{GS}}{(-4)}\right)^2$$

Therefore,

$$V_{GS} = -1.47\,\text{V}$$

From Figure 5.56(b) we see that the current through the source resistor can be written as

$$I_D = \frac{-V_{GS}}{R_S}$$

Therefore,

$$R_S = \frac{-V_{GS}}{I_D} = \frac{-(-1.47)}{2} = 0.735\,\text{k}\Omega$$

The drain-to-source voltage is

$$V_{DS} = V_{DD} - I_D R_D - I_D R_S$$

Therefore,

$$R_D = \frac{V_{DD} - V_{DS} - I_D R_S}{I_D} = \frac{10 - 6 - (2)(0.735)}{2} = 1.27\,\text{k}\Omega$$

We also see that

$$V_{DS} = 6\,\text{V} > V_{GS} - V_P = -1.47 - (-4) = 2.53\,\text{V}$$

which shows that the JFET is indeed biased in the saturation region, as initially assumed.

Comment: Since the source terminal must be positive with respect to the gate in order to bias the transistor on, the source resistor self-biases the JFET, even though the gate and the "bottom" of R_S are at ground potential.

Design Example 5.18   Objective: Design a JFET circuit with a voltage divider biasing circuit.
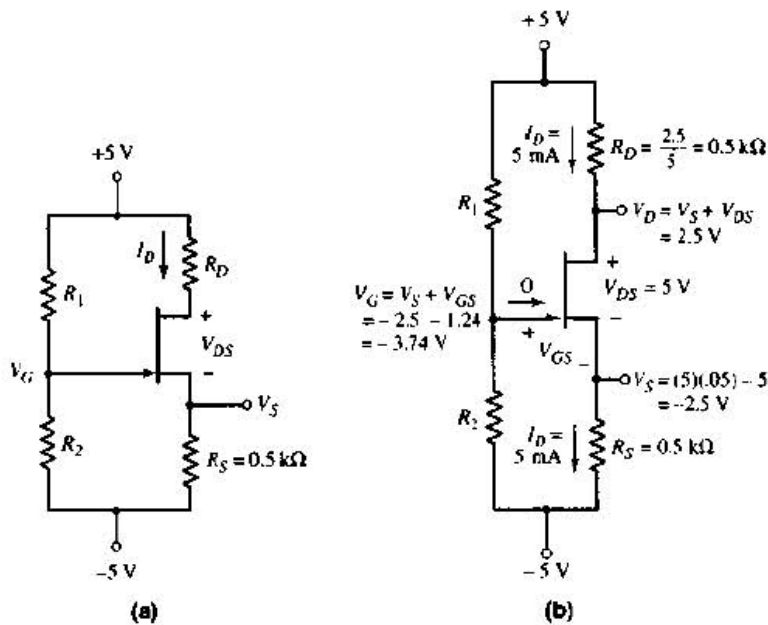
Consider the circuit shown in Figure 5.57(a) with transistor parameters $I_{DSS} = 12\,\text{mA}$, $V_P = -3.5\,\text{V}$, and $\lambda = 0$. Let $R_1 + R_2 = 100\,\text{k}\Omega$. Design the circuit such that the dc drain current is $I_D = 5\,\text{mA}$ and the dc drain-to-source voltage is $V_{DS} = 5\,\text{V}$.

Solution: Assume the transistor is biased in the saturation region. The dc drain current is then given by

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Therefore,

$$5 = 12\left(1 - \frac{V_{GS}}{(-3.5)}\right)^2$$

Figure 5.57   (a) An n-channel JFET circuit with voltage divider biasing and (b) the n-channel JFET circuit for Example 5.18

which yields

$$V_{GS} = -1.24\,\text{V}$$

From Figure 5.57(b), the voltage at the source terminal is

$$V_S = I_D R_S - 5 = (5)(0.5) - 5 = -2.5\,\text{V}$$

which means that the gate voltage is

$$V_G = V_{GS} + V_S = -1.24 - 2.5 = -3.74\,\text{V}$$

We can also write the gate voltage as

$$V_G = \left(\frac{R_2}{R_1 + R_2}\right)(10) - 5$$

or

$$-3.74 = \frac{R_2}{100}(10) - 5 \cdot$$

Therefore,

$$R_2 = 12.6\,\text{k}\Omega$$

and

$$R_1 = 87.4\,\text{k}\Omega$$

The drain-to-source voltage is

$$V_{DS} = 5 - I_D R_D - I_D R_S - (-5)$$

Therefore,

$$R_D = \frac{10 - V_{DS} - I_D R_S}{I_D} = \frac{10 - 5 - (5)(0.5)}{5} = 0.5\,\text{k}\Omega$$

We also see that

$$V_{DS} = 5\,V > V_{GS} - V_P = -1.24 - (-3.5) = 2.26\,V$$

which shows that the JFET is indeed biased in the saturation region, as initially assumed.

☞ **Comment:** The dc analysis of the JFET circuit is essentially the same as that of the MOSFET circuit, since the gate current is assumed to be zero.

Example 5.19 Objective: Calculate the quiescent current and voltage values in a p-channel JFET circuit.

The parameters of the transistor in the circuit shown in Figure 5.58 are: $I_{DSS} = 2.5\,mA$, $V_P = +2.5\,V$, and $\lambda = 0$. The transistor is biased with a constant-current source.

Solution: From Figure 5.58, we can write the dc drain current as

$$I_D = I_Q = 0.8\,mA = \frac{V_D - (-9)}{R_D}$$

which yields

$$V_D = (0.8)(4) - 9 = -5.8\,V$$

Now, assume the transistor is biased in the saturation region. We then have

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

or

$$0.8 = 2.5\left(1 - \frac{V_{GS}}{2.5}\right)^2$$

which yields

$$V_{GS} = 1.086\,V$$
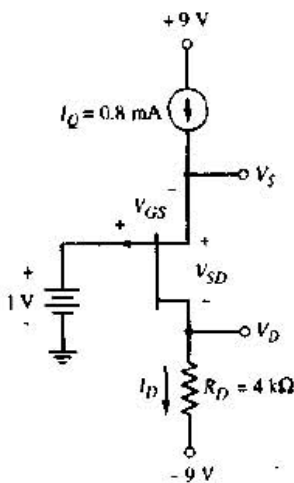
Then

$$V_S = 1 - V_{GS} = 1 - 1.086 = -0.086\,V$$

and

$$V_{SD} = V_S - V_D = -0.086 - (-5.8) = 5.71\,V$$

Again, we see that

$$V_{SD} = 5.71\,V > V_P - V_{GS} = 2.5 - 1.086 = 1.41\,V$$

which verifies that the transistor is biased in the saturation region, as assumed.

**Figure 5.58** A p-channel JFET circuit biased with a constant-current source

Comment: In the same way as bipolar or MOS transistors, junction field-effect transistors can be biased using constant-current sources.

Design Example 5.20 Objective: Design a circuit with an enhancement-mode MESFET.

Consider the circuit shown in Figure 5.59(a). The transistor parameters are: $V_{TN} = 0.24\,V$, $K_n = 1.1\,mA/V^2$, and $\lambda = 0$. Let $R_1 + R_2 = 50\,k\Omega$. Design the circuit such that $V_{GS} = 0.50\,V$ and $V_{DS} = 2.5\,V$.

(a)   (b)
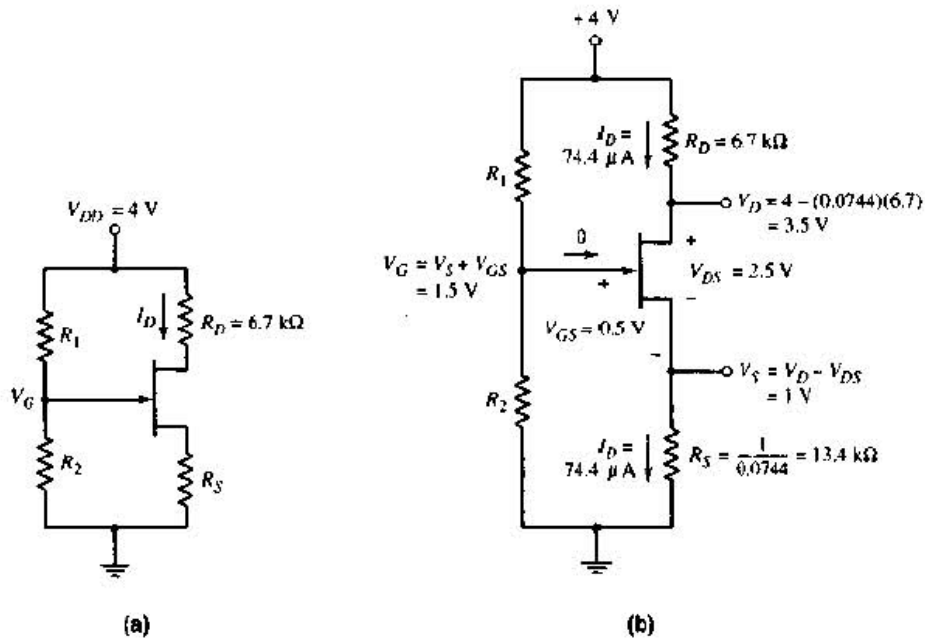
Figure 5.59 (a) An n-channel enhancement-mode MESFET circuit and (b) the n-channel MESFET circuit for Example 5.20

Solution: From Equation (5.36(a)) the drain current is

$$I_D = K_n(V_{GS} - V_{TN})^2 = (1.1)(0.5 - 0.24)^2 = 74.4\,\mu A$$

From Figure 5.59(b), the voltage at the drain is

$$V_D = V_{DD} - I_D R_D = 4 - (0.0744)(6.7) = 3.5\,V$$

Therefore, the voltage at the source is

$$V_S = V_D - V_{DS} = 3.5 - 2.5 = 1\,V$$

The source resistance is then

$$R_S = \frac{V_S}{I_D} = \frac{1}{0.0744} = 13.4\,k\Omega$$

The voltage at the gate is

$$V_G = V_{GS} + V_S = 0.5 + 1 = 1.5\,V$$

Since the gate current is zero, the gate voltage is also given by a voltage divider equation, as follows:

$$V_G = \left(\frac{R_2}{R_1 + R_2}\right)(V_{DD})$$

or

$$1.5 = \left(\frac{R_2}{50}\right)(4)$$

which yields

$$R_2 = 18.75\,\text{k}\Omega$$

and

$$R_1 = 31.25\,\text{k}\Omega$$

Again, we see that

$$V_{DS} = 2.5\,\text{V} > V_{GS} - V_{TN} = 0.5 - 0.24 = 0.26\,\text{V}$$

which confirms that the transistor is biased in the saturation region, as initially assumed.

Comment: The dc analysis and design of an enhancement-mode MESFET circuit is similar to that of MOSFET circuits, except that the gate-to-source voltage of the MESFET must be held to no more than a few tenths of a volt.

Test Your Understanding

5.30 For the circuit in Figure 5.60, the transistor parameters are: $V_P = -3.5\,\text{V}$, $I_{DSS} = 18\,\text{mA}$, and $\lambda = 0$. Calculate V_{GS} and V_{DS}. Is the transistor biased in the saturation or nonsaturation region? (Ans. $V_{GS} = -1.17\,\text{V}$, $V_{DS} = 7.43\,\text{V}$, saturation region)

5.31 The transistor in the circuit in Figure 5.61 has parameters $I_{DSS} = 6\,\text{mA}$, $V_P = -4\,\text{V}$, and $\lambda = 0$. Design the circuit such that $I_{DQ} = 2.5\,\text{mA}$ and $V_{DS} = 6\,\text{V}$, and the total power dissipated in R_1 and R_2 is 2 mW. (Ans. $R_D = 1.35\,\text{k}\Omega$, $R_1 = 158\,\text{k}\Omega$, $R_2 = 42\,\text{k}\Omega$)

*5.32 For the p-channel transistor in the circuit in Figure 5.62, the parameters are: $I_{DSS} = 6\,\text{mA}$, $V_P = 4\,\text{V}$, and $\lambda = 0$. Calculate the quiescent values of I_D, V_{GS}, and V_{SD}. Is the transistor biased in the saturation or nonsaturation region? (Ans. $V_{GS} = 1.81\,\text{V}$, $I_D = 1.81\,\text{mA}$, $V_{SD} = 2.47\,\text{V}$, saturation region)
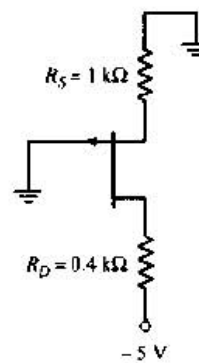
*D5.33 Consider the circuit shown in Figure 5.63 with transistor parameters $I_{DSS} = 8\,\text{mA}$, $V_P = 4\,\text{V}$, and $\lambda = 0$. Design the circuit such that $R_{in} = 100\,\text{k}\Omega$, $I_{DQ} = 5\,\text{mA}$, and $V_{SDQ} = 12\,\text{V}$. (Ans. $R_D = 0.4\,\text{k}\Omega$, $R_1 = 387\,\text{k}\Omega$, $R_2 = 135\,\text{k}\Omega$)
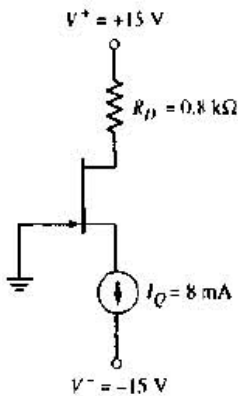
Figure 5.60 Circuit for Exercise 5.30
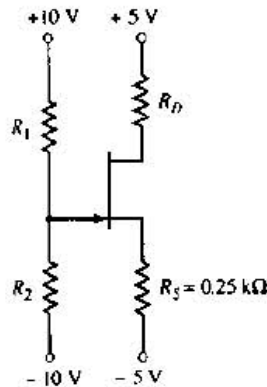
Figure 5.61 Circuit for Exercise 5.31

Figure 5.62 Circuit for Exercise 5.32