5.34 The n-channel enhancement-mode MESFET in the circuit shown in Figure 5.64 has parameters $K_n = 50\,\mu A/V^2$ and $V_{TN} = 0.15\,V$. Find the value of V_{GG} so that $I_{DQ} = 5\,\mu A$. What are the values of V_{GS} and V_{DS}? (Ans. $V_{GG} = 0.516\,V$, $V_{GS} = 0.466\,V$, $V_{DS} = 4.45\,V$)

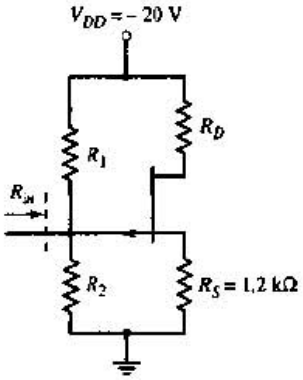

Figure 5.63 Circuit for Exercise 5.33

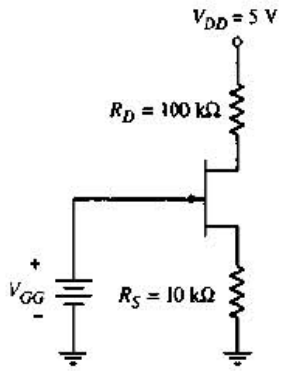

Figure 5.64 Circuit for Exercise 5.34

5.35 For the inverter circuit shown in Figure 5.65, the n-channel enhancement-mode MESFET parameters are $K_n = 100\,\mu A/V^2$ and $V_{TN} = 0.2\,V$. Determine the value of R_D required to produce $V_O = 0.10\,V$ when $V_I = 0.7\,V$. (Ans. $R_D = 267\,k\Omega$)

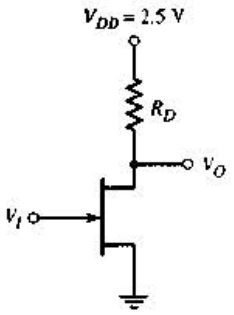

Figure 5.65 Circuit for Exercise 5.35

5.5 SUMMARY

- In this chapter, we have emphasized the structure and dc characteristics of the metal-oxide-semiconductor field-effect transistor (MOSFET). This device, because of its small size, has made possible the microprocessor and other high-density VLSI circuits, so this device is extremely important in integrated circuit technology.
- The current in the MOSFET is controlled by an electric field perpendicular to the surface of the semiconductor. This electric field is a function of the gate voltage. In the nonsaturation bias region of operation, the drain current is a function of the drain voltage, whereas in the saturation bias region of operation, the drain current is

essentially independent of the drain voltage. The drain current is directly proportional to the width-to-length ratio of the transistor, so this parameter becomes the primary design variable in MOSFET circuit design.

- The dc analysis and the design of dc biasing of MOSFET circuits were emphasized in this chapter. Several circuit configurations were analyzed and designed by using the ideal current-voltage relationships. The use of MOSFETs, both enhancement-mode and depletion-mode devices, in place of resistors was developed. This leads to the design of all-MOSFET circuits.
- Basic applications of the MOSFET were discussed. These include switching currents and voltages, performing digital logic functions, and amplifying time-varying signals. The amplifying characteristics will be considered in the next chapter and the important digital applications will be considered in Chapter 16.

CHECKPOINT

After studying this chapter, the reader should have the ability to:

✔ Understand and describe the general operation of n-channel and p-channel enhancement-mode and depletion-mode MOSFETs. (Section 5.1)

✔ Understand the meaning of the various transistor parameters, including threshold voltage, width-to-length ratio, and drain-to-source saturation voltage. (Section 5.1)

✔ Apply the ideal current–voltage relations in the dc analysis and design of various MOSFET circuits using any of the four basic MOSFETs. (Section 5.2)

✔ Understand how MOSFETs can be used in place of resistor load devices to create all-MOSFET circuits. (Section 5.2)

✔ Qualitatively understand how MOSFETs can be used to switch currents and voltages, to perform digital logic functions, and to amplify time-varying signals. (Section 5.3)

✔ Understand the general operation and characteristics of junction FETs. (Section 5.4)

REVIEW QUESTIONS

1. Describe the basic operation of a MOSFET. Define enhancement mode and depletion mode.
2. Describe the general current–voltage characteristics for both enhancement-mode and depletion-mode MOSFETs.
3. Describe what is meant by threshold voltage, width-to-length ratio, and drain-to-source saturation voltage.
4. Define the saturation and nonsaturation bias regions.
5. Describe the channel length modulation effect and define the parameter λ. Describe the body effect and define the parameter γ.
6. Describe a simple common-source MOSFET circuit with an n-channel enhancement-mode device and discuss the relation between the drain-to-source voltage and gate-to-source voltage.
7. What are the steps in the dc analysis of a MOSFET circuit?
8. How do you prove that a MOSFET is biased in the saturation region?
9. In the dc analysis of some MOSFET circuits, quadratic equations in gate-to-source voltage are developed. How do you determine which of the two possible solutions is the correct one?
10. How can the Q-point be stabilized against variations in transistor parameters?

11. Describe the current–voltage relation of an n-channel enhancement-mode MOSFET with the gate connected to the drain.
12. Describe the current–voltage relation of an n-channel depletion-mode MOSFET with the gate connected to the source.
13. What is the principal difference between biasing techniques used in discrete transistor circuits and integrated circuits?
14. Describe how an n-channel enhancement-mode MOSFET can be used to switch a motor on and off.
15. Describe a MOSFET NOR logic circuit.
16. Describe how a MOSFET can be used to amplify a time-varying voltage.
17. Describe the basic operation of a junction FET.
18. What is the difference between a MESFET and a pn junction FET?

PROBLEMS

[Note: In all problems, assume the transistor parameter $\lambda = 0$, unless otherwise stated.]

Section 5.1 MOS Field-Effect Transistor

5.1 Consider an n-channel enhancement-mode MOSFET with parameters $V_{TN} = 1.5\,V$ and $K_n = 0.25\,mA/V^2$. Determine I_D for: (a) $V_{GS} = 5\,V$, $V_{DS} = 6\,V$; and (b) $V_{GS} = 5\,V$, $V_{DS} = 2.5\,V$.

5.2 The parameters of an n-channel enhancement-mode MOSFET are $V_{TN} = 0.8\,V$, $k_n' = 80\,\mu A/V^2$, and $W/L = 5$. (a) Assume the transistor is biased in the saturation region and $I_D = 0.5\,mA$. Determine $V_{DS}(sat)$ and the required V_{GS}. (b) Repeat part (a) for $I_D = 1.5\,mA$.

5.3 For an n-channel depletion-mode MOSFET, the parameters are $V_{TN} = -2.5\,V$ and $K_n = 1.1\,mA/V^2$. (a) Determine I_D for $V_{GS} = 0$; and: (i) $V_{DS} = 0.5\,V$, (ii) $V_{DS} = 2.5\,V$, and (iii) $V_{DS} = 5\,V$. (b) Repeat part (a) for $V_{GS} = 2\,V$.

5.4 Consider an n-channel depletion-mode MOSFET with parameters $V_{TN} = -2\,V$ and $k_n' = 80\,\mu A/V^2$. The drain current is $I_D = 1.5\,mA$ at $V_{GS} = 0$ and $V_{DS} = 3\,V$. Determine the W/L ratio.

5.5 An n-channel enhancement-mode MOSFET has parameters $V_{TN} = 0.8\,V$, $W = 64\,\mu m$, $L = 4\,\mu m$, $t_{ox} = 450\,Å$, and $\mu_n = 650\,cm^2/V\text{–}s$. (a) Calculate the conduction parameter K_n. (b) Determine the drain current when $V_{GS} = V_{DS} = 3\,V$.

5.6 For a depletion NMOS device, the parameters are: $V_{TN} = -2\,V$, $W = 100\,\mu m$, $L = 5\,\mu m$, $t_{ox} = 600\,Å$, and $\mu_n = 500\,cm^2/V\text{–}s$. (a) Calculate the conduction parameter K_n. (b) Determine the drain current when: (i) $V_{GS} = 0$, $V_{DS} = 5\,V$, and (ii) $V_{GS} = 2\,V$, $V_{DS} = 1\,V$.

5.7 A particular NMOS device has parameters $V_{TN} = 1\,V$, $L = 2.5\,\mu m$, $t_{ox} = 400\,Å$, and $\mu_n = 600\,cm^2/V\text{–}s$. A drain current of $I_D = 1.2\,mA$ is requried when the device is biased in the saturation region at $V_{GS} = 5\,V$. Determine the necessary channel width of the device.

5.8 For a p-channel enhancement-mode MOSFET, $k_p' = 40\,\mu A/V^2$. The device has drain currents of $I_D = 0.225\,mA$ at $V_{SG} = V_{SD} = 3\,V$ and $I_D = 1.40\,mA$ at $V_{SG} = V_{SD} = 4\,V$. Determine the W/L ratio and the value of V_{TP}.

5.9 For a p-channel enhancement-mode MOSFET, the parameters are $K_P = 2\,mA/V^2$ and $V_{TP} = -0.5\,V$. The gate is at ground potential, and the source and substrate

terminals are at +5 V. Determine I_D when the drain terminal voltage is: (a) $V_D = 0$ V, (b) $V_D = 2$ V, (c) $V_D = 4$ V, and (d) $V_D = 5$ V.

5.10 A p-channel depletion-mode MOSFET has parameters $V_{TP} = +2$ V, $k_p' = 40\,\mu A/V^2$, and $W/L = 6$. Determine V_{SD}(sat) for: (a) $V_{SG} = -1$ V, (b) $V_{SG} = 0$, and (c) $V_{SG} = +1$ V. If the transistor is biased in the saturation region, calculate the drain current for each value of V_{SG}.

5.11 Consider a p-channel depletion-mode MOSFET with parameters $K_p = 0.5\,mA/V^2$ and $V_{TP} = +2$ V. If $V_{SG} = 0$, determine I_D for: (a) $V_{SD} = 1$ V, (b) $V_{SD} = 2$ V, and (c) $V_{SD} = 3$ V.

D5.12 Enhancement-mode NMOS and PMOS devices both have parameters $L = 4\,\mu m$ and $t_{ox} = 500$ Å. For the NMOS transistor, $V_{TN} = +0.6$ V, $\mu_n = 675\,cm^2/V\text{-}s$, and the channel width is W_n; for the PMOS transistor, $V_{TP} = -0.6$ V, $\mu_p = 375\,cm^2/V\text{-}s$, and the channel width is W_p. Design the widths of the two transistors such that they are electrically equivalent and the drain current in the PMOS transistor is $I_D = 0.8$ mA when it is biased in the saturation region at $V_{SG} = 5$ V. What are the values of K_n, K_p, W_n, and W_p?

5.13 For an NMOS enhancement-mode transistor, the parameters are: $V_{TN} = 1.2$ V, $K_n = 0.20\,mA/V^2$, and $\lambda = 0.01\ V^{-1}$. Calculate the output resistance r_o for $V_{GS} = 2.0$ V and for $V_{GS} = 4.0$ V. What is the value of V_A?

5.14 The parameters of an n-channel enhancement-mode MOSFET are $V_{TN} = 0.8$ V, $k_n' = 80\,\mu A/V^2$, and $W/L = 4$. What is the maximum value of λ and the minimum value of V_A such that for $V_{GS} = 3$ V, $r_o \geq 200\,k\Omega$?

5.15 An enhancement-mode NMOS transistor has parameters $V_{TNO} = 0.8$ V, $\gamma = 0.8\,V^{1/2}$, and $\phi_f = 0.35$ V. At what value of V_{SB} will the threshold voltage change by 2 V due to the body effect?

5.16 Consider an NMOS device with parameters $V_{TNO} = 1$ V and $\phi_f = 0.37$ V. Determine the maximum value of γ such that the shift in threshold voltage between $V_{SB} = 0$ and $V_{SB} = 10$ V is no more than 1.2 V.

5.17 The silicon dioxide gate insulator of an MOS transistor has a thickness of $t_{ox} = 275$ Å. (a) Calculate the ideal oxide breakdown voltage. (b) If a safety factor of three is required, determine the maximum safe gate voltage that may be applied.

5.18 In a power MOS transistor, the maximum applied gate voltage is 24 V. If a safety factor of three is specified, determine the minimum thickness necessary for the silicon dioxide gate insulator.

Section 5.2 Transistor DC Analysis

5.19 In the circuit in Figure P5.19, the transistor parameters are $V_{TN} = 0.8$ V and $K_n = 0.5\,mA/V^2$. Calculate V_{GS}, I_D, and V_{DS}.

5.20 For the transistor in the circuit in Figure P5.20, the parameters are $V_{TN} = 2$ V, $k_n' = 60\,\mu A/V^2$, and $W/L = 60$. Determine V_{GS}, I_D, and V_{DS}.

5.21 Consider the circuit in Figure P5.21. The transistor parameters are $V_{TP} = -2$ V and $K_p = 1\,mA/V^2$. Determine I_D, V_{SG}, and V_{SD}.

5.22 For the circuit in Figure P5.22, the transistor parameters are $V_{TP} = -0.8$ V and $K_p = 200\,\mu A/V^2$. Determine V_S and V_{SD}.

***D5.23** Design a MOSFET circuit in the configuration shown in Figure P5.19. The transistor parameters are $V_{TN} = 1.2$ V, $k_n' = 60\,\mu A/V^2$, and $\lambda = 0$. The circuit parameters are $V_{DD} = 10$ V and $R_D = 5\,k\Omega$. Design the circuit so that $V_{DSQ} \cong 5$ V, the voltage across

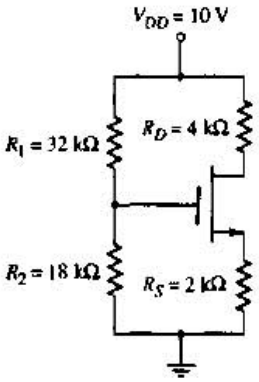

Figure P5.19

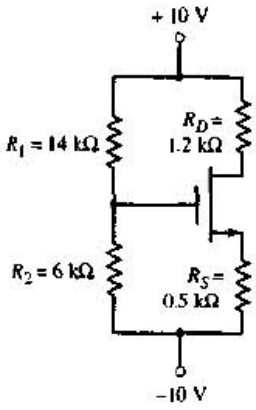

Figure P5.20

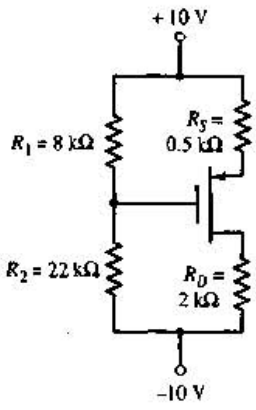

Figure P5.21

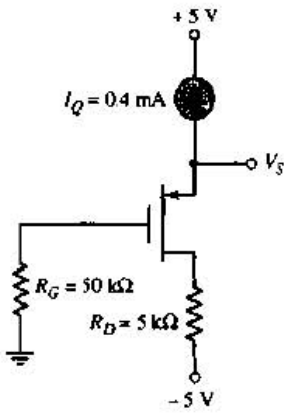

Figure P5.22

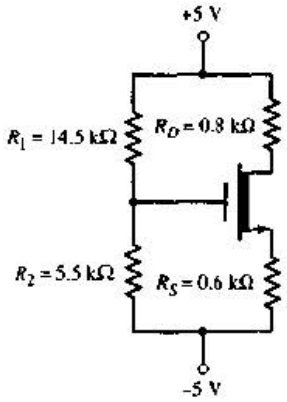

Figure P5.24

R_S is approximately equal to V_{GS}, and the current through the bias resistors is approximately 5 percent of the drain current.

5.24 The parameters of the transistor in the circuit in Figure P5.24 are $V_{TN} = -1$ V and $K_n = 0.5\,\text{mA/V}^2$. Determine V_{GS}, I_D, and V_{DS}.

***D5.25** Design a MOSFET circuit with the configuration shown in Figure P5.21. The transistor parameters are $V_{TP} = -2$ V, $k_p' = 40\,\mu\text{A/V}^2$, and $\lambda = 0$. The circuit bias is ± 10 V, the drain current is to be 0.8 mA, the drain-to-source voltage is to be approximately 10 V, and the voltage across R_S is to be approximately equal to V_{GS}. In addition, the current through the bias resistors is to be no more than 10 percent of the drain current.

5.26 The parameters of the transistors in Figures P5.26(a) and (b) are $K_n = 0.5\,\text{mA/V}^2$, $V_{TN} = 1.2$ V, and $\lambda = 0$. Determine v_{GS} and v_{DS} for each transistor when (i) $I_Q = 50\,\mu$A and (ii) $I_Q = 1$ mA.

5.27 For the circuit in Figure P5.27, the transistor parameters are $V_{TN} = 0.6$ V and $K_n = 200\,\mu\text{A/V}^2$. Determine V_S and V_D.

D5.28 Design the circuit in Figure P5.28, such that $I_D = 0.8$ mA and $V_D = 1$ V. The transistor parameters are $K_n = 400\,\mu\text{A/V}^2$ and $V_{TN} = 1.7$ V.

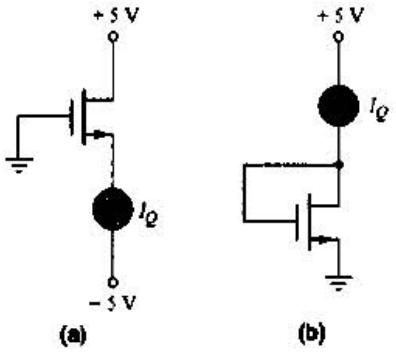

Figure P5.26

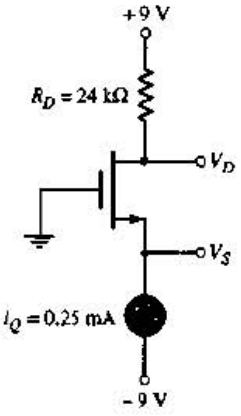

Figure P5.27

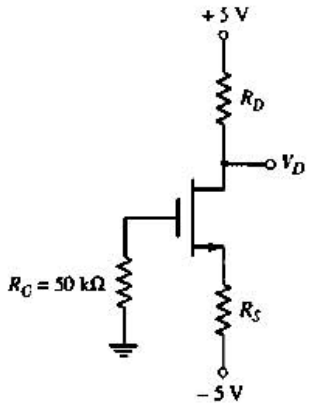

Figure P5.28

D5.29 The PMOS transistor in Figure P5.29 has parameters $V_{TP} = -1.5\,\text{V}$, $k_p' = 25\,\mu\text{A/V}^2$, $L = 4\,\mu\text{m}$, and $\lambda = 0$. Determine the values of W and R such that $I_D = 0.1\,\text{mA}$ and $V_{SD} = 2.5\,\text{V}$.

D5.30 Design the circuit in Figure P5.30 so that $V_{SD} = 2.5\,\text{V}$. The current in the bias resistors should be no more than 10 percent of the drain current. The transistor parameters are $V_{TP} = +1.5\,\text{V}$ and $K_p = 0.5\,\text{mA/V}^2$.

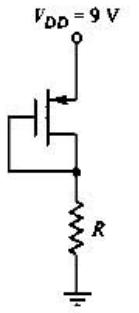

Figure P5.29

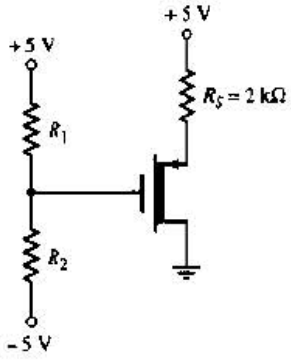

Figure P5.30

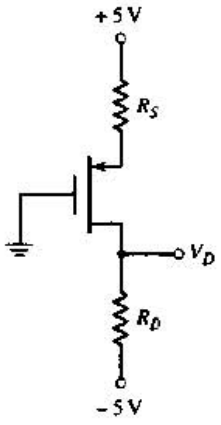

Figure P5.31

D5.31 Design the circuit in Figure P5.31 such that $I_D = 0.5\,\text{mA}$ and $V_D = -3\,\text{V}$. The transistor parameters are $k_p' = 30\,\mu\text{A/V}^2$, $W/L = 20$, and $V_{TP} = -1.2\,\text{V}$.

D5.32 The parameters of the transistor in the circuit in Figure P5.32 are $V_{TP} = -1.75\,\text{V}$ and $K_p = 3\,\text{mA/V}^2$. Design the circuit such that $I_D = 5\,\text{mA}$, $V_{SD} = 6\,\text{V}$, and $R_{\text{in}} = 80\,\text{k}\Omega$.

***5.33** For each transistor in the circuit in Figure P5.33, $k_n' = 60\,\mu\text{A/V}^2$. Also for M_1, $W/L = 4$ and $V_{TN} = +0.8\,\text{V}$, and for M_2, $W/L = 1$ and $V_{TN} = -1.8\,\text{V}$. Determine the region of operation of each transistor and the output voltage v_O for: (a) $v_I = 1\,\text{V}$, (b) $v_I = 3\,\text{V}$, and (c) $v_I = 5\,\text{V}$.

***D5.34** Consider the circuit in Figure P5.33. The transistor parameters are for M_1, $V_{TN} = +0.8\,\text{V}$ and $k_n' = 40\,\mu\text{A/V}^2$, and for M_2, $V_{TN} = -2\,\text{V}$, $k_n' = 40\,\mu\text{A/V}^2$, and $W/L = 1$. Determine the W/L ratio for M_1 such that $v_O = 0.15\,\text{V}$ when $v_I = 5\,\text{V}$.

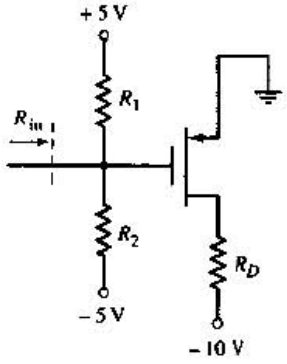

Figure P5.32

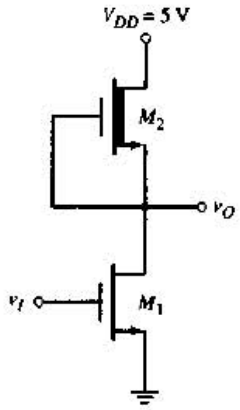

Figure P5.33

***5.35** The transistors in the circuit in Figure P5.35 both have parameters $V_{TN} = 0.8\,\text{V}$ and $k_n' = 30\,\mu\text{A/V}^2$. (a) If the width-to-length ratios of M_1 and M_2 are $(W/L)_1 = (W/L)_2 = 40$, determine V_{GS1}, V_{GS2}, V_O, and I_D. (b) Repeat part (a) if the width-to-length ratios are changed to $(W/L)_1 = 40$ and $(W/L)_2 = 15$.

D5.36 Consider the circuit in Figure P5.36. The transistor parameters are $V_{TN} = 1\,\text{V}$ and $k_n' = 36\,\mu\text{A/V}^2$. Design the width-to-length ratio required in each transistor such that $I_D = 0.5\,\text{mA}$, $V_1 = 2\,\text{V}$, and $V_2 = 5\,\text{V}$.

D5.37 The transistors in the circuit in Figure 5.35 in the text have parameters $V_{TN} = 0.8\,\text{V}$, $k_n' = 40\,\mu\text{A/V}^2$, and $\lambda = 0$. The width-to-length ratio of M_L is $(W/L)_L = 1$. Design the width-to-length ratio of the driver transistor such that $V_O = 0.10\,\text{V}$ when $V_I = 5\,\text{V}$.

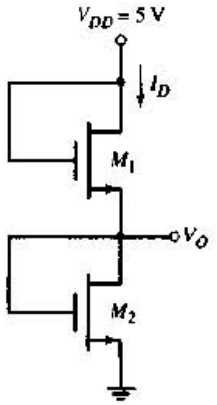

Figure P5.35

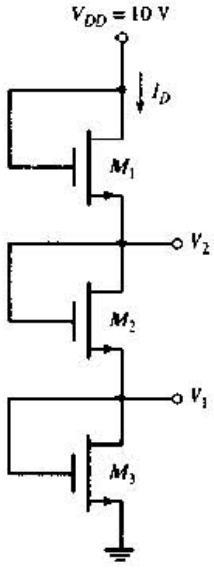

Figure P5.36

D5.38 For the circuit in Figure 5.39 in the text, the transistor parameters are: $V_{TND} = 0.8\,\text{V}$, $V_{TNL} = -1.8\,\text{V}$, $k_n' = 40\,\mu\text{A/V}^2$, and $\lambda = 0$. Let $V_{DD} = 5\,\text{V}$. The width-to-length ratio of M_L is $(W/L)_L = 1$. Design the width-to-length ratio of the driver transistor such that $V_O = 0.05\,\text{V}$ when $V_I = 5\,\text{V}$.

5.39 All transistors in the circuit in Figure 5.43 in the text have parameters $V_{TN} = 1\,\text{V}$ and $\lambda = 0$. Assume the conduction parameters are $K_{n1} = 80\,\mu\text{A/V}^2$, $K_{n2} = 100\,\mu\text{A/V}^2$, $K_{n3} = 200\,\mu\text{A/V}^2$, and $K_{n4} = 400\,\mu\text{A/V}^2$. Determine I_{REF}, I_Q, and each gate-to-source voltage.

Section 5.3 MOSFET Switch and Amplifier

5.40 Consider the circuit in Figure P5.40. The transistor parameters are $V_{TN} = 0.8\,\text{V}$ and $k_n' = 30\,\mu\text{A/V}^2$. The resistor is $R_D = 10\,\text{k}\Omega$. Determine the transistor width-to-length ratio (W/L) such that $V_O = 0.1\,\text{V}$ when $V_I = 4.2\,\text{V}$.

D5.41 The transistor in the circuit in Figure P5.41 is used to turn the LED on and off. The transistor parameters are $V_{TN} = 0.8\,\text{V}$, $k_n' = 40\,\mu\text{A/V}^2$, and $\lambda = 0$. The diode cut-in voltage is $V_\gamma = 1.6\,\text{V}$. Design R_D and the transistor W/L ratio such that $I_D = 12\,\text{mA}$ for $V_I = 5\,\text{V}$ and $V_{DS} = 0.2\,\text{V}$.

D5.42 The circuit in Figure P5.42 is another configuration used to switch an LED on and off. The transistor parameters are $V_{TP} = -0.8\,\text{V}$, $k_p' = 20\,\mu\text{A/V}^2$, and $\lambda = 0$. The diode cut-in voltage is $V_\gamma = 1.6\,\text{V}$. Design R_D and the transistor W/L ratio such that $I_D = 15\,\text{mA}$ for $V_I = 0\,\text{V}$ and $V_{SD} = 0.15\,\text{V}$.

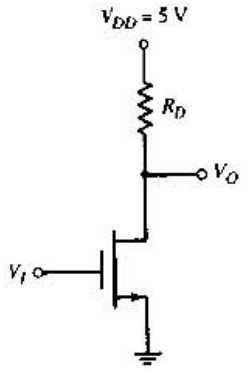

Figure P5.40

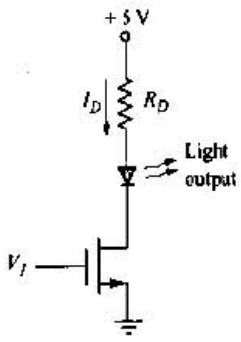

Figure P5.41

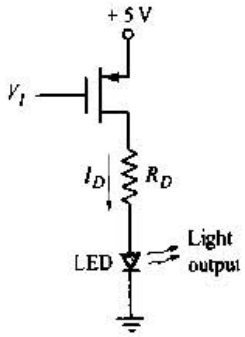

Figure P5.42

Section 5.4 Junction Field-Effect Transistor

5.43 The gate and source of an n-channel depletion-mode JFET are connected together. What value of V_{DS} will ensure that this two-terminal device is biased in the saturation region. What is the drain current for this bias condition?

5.44 For an n-channel JFET, the parameters are $I_{DSS} = 6\,\text{mA}$ and $V_P = -3\,\text{V}$. Calculate $V_{DS}(\text{sat})$. If $V_{DS} > V_{DS}(\text{sat})$, determine I_D for: (a) $V_{GS} = 0$, (b) $V_{GS} = -1\,\text{V}$, (c) $V_{GS} = -2\,\text{V}$, and (d) $V_{GS} = -3\,\text{V}$.

5.45 A p-channel JFET biased in the saturation region with $V_{SD} = 5\,\text{V}$ has a drain current of $I_D = 2.8\,\text{mA}$ at $V_{GS} = 1\,\text{V}$ and $I_D = 0.30\,\text{mA}$ at $V_{GS} = 3\,\text{V}$. Determine I_{DSS} and V_P.

5.46 Consider the p-channel JFET in Figure P5.46. Determine the range of V_{DD} that will bias the transistor in the saturation region. If $I_{DSS} = 6\,\text{mA}$ and $V_P = 2.5\,\text{V}$, find V_S.

5.47 Consider a GaAs MESFET. When the device is biased in the saturation region, we find that $I_D = 18.5\,\mu\text{A}$ at $V_{GS} = 0.35\,\text{V}$ and $I_D = 86.2\,\mu\text{A}$ at $V_{GS} = 0.50\,\text{V}$. Determine the conduction parameter k and the threshold voltage V_{TN}.

5.48 The threshold voltage of a GaAs MESFET is $V_{TN} = 0.24\,\text{V}$. The maximum allowable gate-to-source voltage is $V_{GS} = 0.75\,\text{V}$. When the transistor is biased in the saturation region, the maximum drain current is $I_D = 250\,\mu\text{A}$. What is the value of the conduction parameter k?

***5.49** For the transistor in the circuit in Figure P5.49, the parameters are: $I_{DSS} = 10\,\text{mA}$ and $V_P = -5\,\text{V}$. Determine I_{DQ}, V_{GSQ}, and V_{DSQ}.

D5.50 Consider the source follower with the n-channel JFET in Figure P5.50. The input resistance is to be $R_{in} = 500\,\text{k}\Omega$. We wish to have $I_{DQ} = 5\,\text{mA}$, $V_{DSQ} = 8\,\text{V}$, and $V_{GSQ} = -1\,\text{V}$. Determine R_S, R_1, and R_2, and the required transistor values of I_{DSS} and V_P.

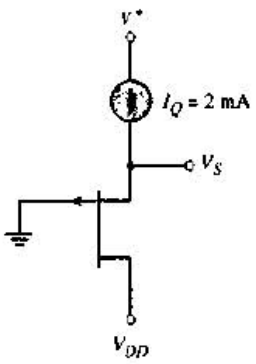

Figure P5.46

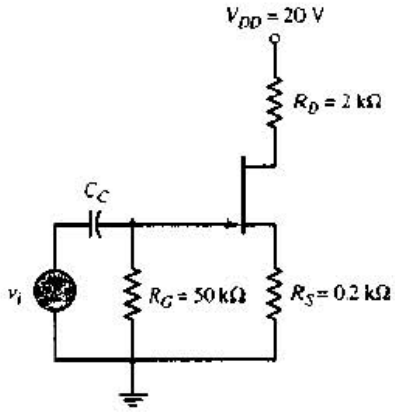

Figure P5.49

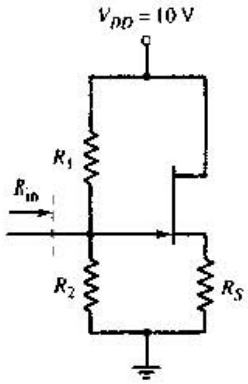

Figure P5.50

D5.51 The transistor in the circuit in Figure P5.51 has parameters $I_{DSS} = 8\,\text{mA}$ and $V_P = 4\,\text{V}$. Design the circuit such that $I_D = 5\,\text{mA}$. Assume $R_{in} = 100\,\text{k}\Omega$. Determine V_{GS} and V_{SD}.

D5.52 For the circuit in Figure P5.52, the transistor parameters are $I_{DSS} = 7\,\text{mA}$ and $V_P = 3\,\text{V}$. Let $R_1 + R_2 = 100\,\text{k}\Omega$. Design the circuit such that $I_{DQ} = 5.0\,\text{mA}$ and $V_{SDQ} = 6\,\text{V}$.

5.53 The transistor in the circuit in Figure P5.53 has parameters $I_{DSS} = 8\,\text{mA}$ and $V_P = -4\,\text{V}$. Determine V_G, I_{DQ}, V_{GSQ}, and V_{DSQ}.

5.54 Consider the circuit in Figure P5.54. The quiescent value of V_{DS} is found to be $V_{DSQ} = 5\,\text{V}$. If $I_{DSS} = 10\,\text{mA}$, determine I_{DQ}, V_{GSQ}, and V_P.

D5.55 For the circuit in Figure P5.55, the transistor parameters are $I_{DSS} = 4\,\text{mA}$ and $V_P = -3\,\text{V}$. Design R_D such that $V_{DS} = |V_P|$. What is the value of I_D?

D5.56 Consider the source-follower circuit in Figure P5.56. The transistor parameters are $I_{DSS} = 2\,\text{mA}$ and $V_P = 2\,\text{V}$. Design the circuit such that $I_{DQ} = 1\,\text{mA}$, $V_{SDQ} = 10\,\text{V}$, and the current through R_1 and R_2 is $0.1\,\text{mA}$.

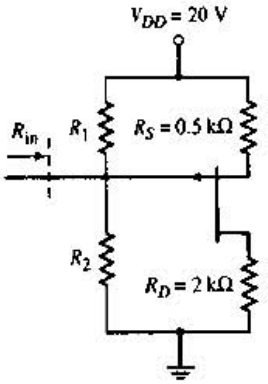

Figure P5.51

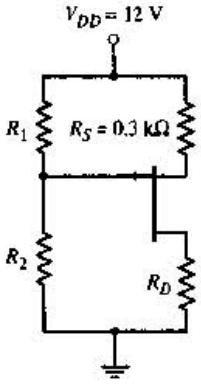

Figure P5.52

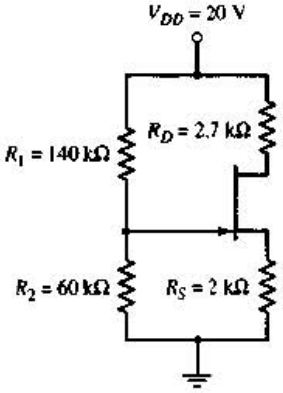

Figure P5.53

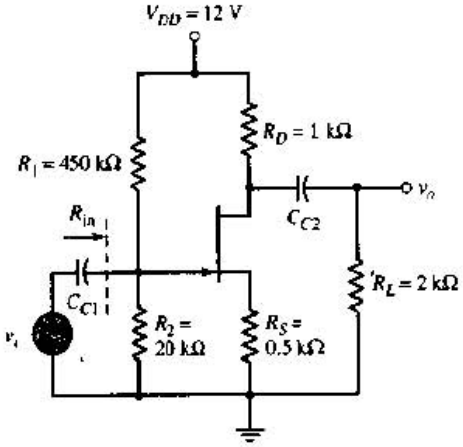

Figure P5.54

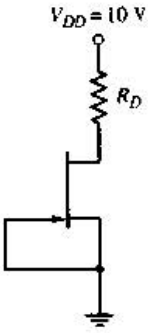

Figure P5.55

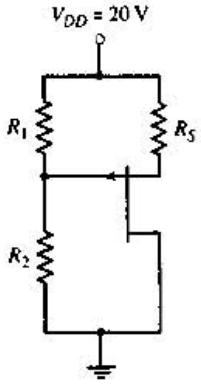

Figure P5.56

D5.57 The GaAs MESFET in the circuit in Figure P5.57 has parameters $k = 250\,\mu A/V^2$ and $V_{TN} = 0.20$ V. Let $R_1 + R_2 = 150$ kΩ. Design the circuit such that $I_D = 40\,\mu A$ and $V_{DS} = 2$ V.

5.58 For the circuit in Figure P5.58, the GaAs MESFET threshold voltage is $V_{TN} = 0.15$ V. Let $R_D = 50$ kΩ. Determine the value of the conduction parameter required so that $V_O = 0.70$ V when $V_I = 0.75$ V.

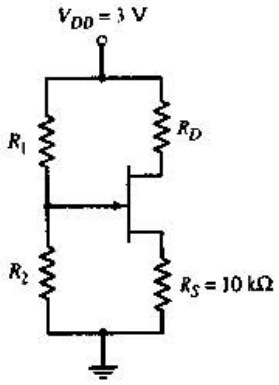

Figure P5.57

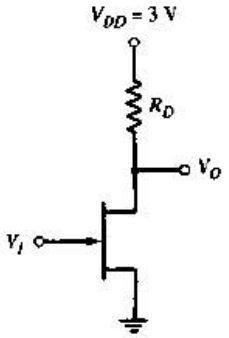

Figure P5.58

COMPUTER SIMULATION PROBLEMS

5.59 Generate the i_D versus v_{DS} characteristics for an n-channel enhancement-mode silicon MOSFET at $T = 300^\circ$K. Limit the characteristics to $v_{DS}(\text{max}) = 10\,\text{V}$ and $v_{GS}(\text{max}) = 10\,\text{V}$. Plot curves for: (a) $W/L = 4$, $\lambda = 0$; (b) $W/L = 40$, $\lambda = 0$; and (c) $W/L = 4$, $\lambda = 0.02\,\text{V}^{-1}$.

5.60 Consider the NMOS circuit with enhancement load shown in Figure 5.35. Assume a width-to-length ratio of $W/L = 1$ for M_L. From a computer analysis, plot the dc voltage transfer characteristics V_O versus V_I for M_D width-to-length ratios of: (a) $W/L = 2$, (b) $W/L = 9$, (c) $W/L = 16$, and (d) $W/L = 100$. Consider the case when the body effect is neglected, and then when the body effect is included.

5.61 Consider the NMOS circuit with depletion load shown in Figure 5.39. Use a computer analysis to plot the dc voltage transfer characteristics V_O versus V_I for the same parameters listed in Problem 5.60. Consider the case when the body effect is neglected, and then when the body effect is included.

5.62 (a) Correlate the results of Example 5.13 with a computer analysis. (b) Repeat the analysis if the width-to-length ratio of M_3 is doubled.

5.63 Correlate the JFET design in Example 5.18 with a computer analysis.

DESIGN PROBLEMS

[Note: All design should be correlated with a computer simulation.]

***D5.64** Consider a discrete common-source circuit with the configuration shown in Figure 5.29. The circuit and transistor parameters are: $V_{DD} = 10\,\text{V}$, $R_S = 0.5\,\text{k}\Omega$, $R_D = 4\,\text{k}\Omega$, and $V_{TN} = 2\,\text{V}$. Design the circuit such that the nominal Q-point is midway between the transition point and cutoff, and determine the conduction parameter. The dc currents in R_1 and R_2 should be approximately a factor of ten smaller than the quiescent drain current.

***D5.65** For the circuit shown in Figure 5.43, the threshold voltage of each transistor is $V_{TN} = 1\,\text{V}$, and the parameter value $k_n' = 40\,\mu\text{A/V}^2$ is the same for all devices. If $R_D = 4\,\text{k}\Omega$, design the circuit such that the quiescent drain-to-source voltage of M_1 is 4 V and $I_Q = (\frac{1}{2})I_{REF}$.

***D5.66** The NMOS circuit with depletion load shown in Figure 5.39 is biased at $V_{DD} = 5\,\text{V}$. The threshold voltage of M_D is $V_{TND} = 0.8\,\text{V}$ and that of M_L is $V_{TNL} = -2\,\text{V}$. For each transistor, $k_n' = 40\,\mu\text{A/V}^2$. Design the transistors such that $V_O = 0.1\,\text{V}$ when $V_I = 5\,\text{V}$ and the maximum power dissipated in the circuit is 1.0 mW.

***D5.67** The threshold voltage of the load transistor M_L in Figure 5.35 is $V_{TNL} = 0.8\,\text{V}$. All other parameters are the same as given in Problem 5.66. Design the transistors to meet the same specifications given in Problem 5.66.

***D5.68** Consider the JFET common-source circuit shown in Figure 5.57(a). The transistor pinchoff voltage is $V_P = -4\,\text{V}$ and the saturation current is in the range $1 \le I_{DSS} \le 2\,\text{mA}$. Design the circuit such that the nominal Q-point is in the center of the load line and the Q-point parameters do not deviate from the nominal value by more than 10 percent. The value of R_S may be changed, the current in R_1 and R_2 should be approximately a factor of ten less than the quiescent drain current, and the standard tolerance resistance value of 5 percent should be used.

CHAPTER

6

Basic FET Amplifiers

6.0 PREVIEW

In the last chapter, we described the operation of the FET, in particular the MOSFET, and analyzed and designed the dc response of circuits containing these devices. In this chapter, we emphasize the use of FETs in linear amplifier applications. Although a major use of MOSFETs is in digital applications, they are also used in linear amplifier circuits.

There are three basic configurations of single-stage or single-transistor FET amplifiers. These are the common-source, source-follower, and common-gate configurations. We investigate the characteristics of each configuration and show how these properties are used in various applications. Since MOSFET integrated circuit amplifiers normally use MOSFETs as load devices instead of resistors because of their small size, we introduce the technique of using MOSFET enhancement or depletion devices as loads. These three configurations form the building blocks for more complex amplifiers, so gaining a good understanding of these three amplifier circuits is an important goal of this chapter.

In integrated circuit systems, amplifiers are usually connected in series or cascade, forming a multistage configuration, to increase the overall voltage gain, or to provide a particular combination of voltage gain and output resistance. We consider a few of the many possible multistage configurations, to introduce the analysis methods required for such circuits, as well as their properties.

JFET amplifiers are also considered. These circuits, again, tend to be specialized, so the JFET discussion is brief.

6.1 THE MOSFET AMPLIFIER

In Chapter 4, we discussed the reasons linear amplifiers are necessary in analog electronic systems. In this chapter, we continue the analysis and design of linear amplifiers that use field-effect transistors as the amplifying device. The term **small signal** means that we can linearize the ac equivalent circuit. We will define what is meant by small signal in the case of MOSFET circuits. The term linear amplifiers means that we can use superposition so that the dc analysis and ac

analysis of the circuits can be performed separately and the total response is the sum of the two individual responses.

The mechanism with which MOSFET circuits amplify small time-varying signals was introduced in the last chapter. In this section, we will expand that discussion using the graphical technique, dc load line, and ac load line. In the process, we will develop the various small-signal parameters of linear circuits and the corresponding equivalent circuits.

There are four possible equivalent circuits that can be used. These are listed in Table 4.3 of Chapter 4. The most common equivalent circuit that is used for the FET amplifiers is the transconductance amplifier, in which the input signal is a voltage and the output signal is a current. The small-signal parameters associated with this equivalent circuit are developed in the following section.

6.1.1 Graphical Analysis, Load Lines, and Small-Signal Parameters

Figure 6.1 shows an NMOS common-source circuit with a time-varying voltage source in series with the dc source. We assume the time-varying input signal is sinusoidal. Figure 6.2 shows the transistor characteristics, dc load line, and Q-point, where the dc load line and Q-point are functions of v_{GS}, V_{DD}, R_D, and the transistor parameters. For the output voltage to be a linear function of the input voltage, the transistor must be biased in the saturation region. (Note that, although we primarily use n-channel, enhancement-mode MOSFETs in our discussions, the same results apply to the other MOSFETs.)

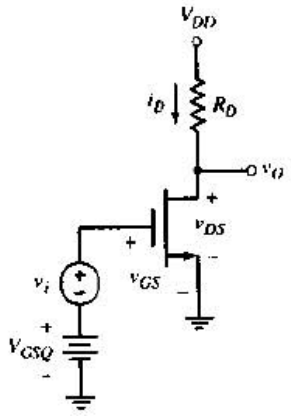

Figure 6.1 NMOS common-source circuit with time-varying signal source in series with gate dc source

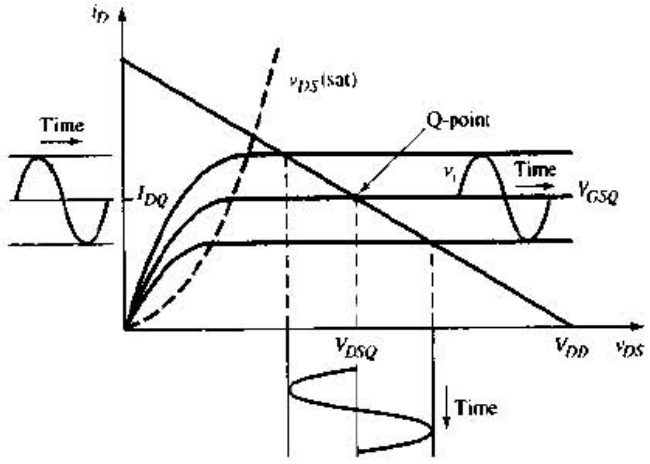

Figure 6.2 Common-source transistor characteristics, dc load line, and sinusoidal variation in gate-to-source voltage, drain current, and drain-to-source voltage

Also shown in Figure 6.2 are the sinusoidal variations in the gate-to-source voltage, drain current, and drain-to-source voltage, as a result of the sinusoidal source v_i. The total gate-to-source voltage is the sum of V_{GSQ} and v_i. As v_i increases, the instantaneous value of v_{GS} increases, and the bias point moves up

the load line. A larger value of v_{GS} means a larger drain current and a smaller value of v_{DS}. For a negative v_i (the negative portion of the sine wave), the instantaneous value of v_{GS} decreases below the quiescent value, and the bias point moves down the load line. A smaller v_{GS} value means a smaller drain current and increased value of v_{DS}. Once the Q-point is established, we can develop a mathematical model for the sinusoidal, or small-signal, variations in gate-to-source voltage, drain-to-source voltage, and drain current.

The time-varying signal source v_i in Figure 6.1 generates a time-varying component of the gate-to-source voltage. In this case, $v_{gs} = v_i$, where v_{gs} is the time-varying component of the gate-to-source voltage. For the FET to operate as a linear amplifier, the transistor must be biased in the saturation region, and the instantaneous drain current and drain-to-source voltage must also be confined to the saturation region.

Transistor Parameters

The instantaneous gate-to-source voltage is

$$v_{GS} = V_{GSQ} + v_i = V_{GSQ} + v_{gs} \tag{6.1}$$

where V_{GSQ} is the dc component and v_{gs} is the ac component. The instantaneous drain current is

$$i_D = K_n(v_{GS} - V_{TN})^2 \tag{6.2}$$

Substituting Equation (6.1) into (6.2) produces

$$i_D = K_n[V_{GSQ} + v_{gs} - V_{TN}]^2 = K_n[(V_{GSQ} - V_{TN}) + v_{gs}]^2 \tag{6.3(a)}$$

or

$$i_D = K_n(V_{GSQ} - V_{TN})^2 + 2K_n(V_{GSQ} - V_{TN})v_{gs} + K_n v_{gs}^2 \tag{6.3(b)}$$

The first term in Equation (6.3(b)) is the dc or quiescent drain current I_{DQ}, the second term is the time-varying drain current component that is linearly related to the signal v_{gs}, and the third term is proportional to the square of the signal voltage. For a sinusoidal input signal, the squared term produces undesirable harmonics, or nonlinear distortion, in the output voltage. To minimize these harmonics, we require

$$v_{gs} \ll 2(V_{GSQ} - V_{TN}) \tag{6.4}$$

which means that the third term in Equation (6.3(b)) will be much smaller than the second term. *Equation (6.4) represents the small-signal condition that must be satisfied for linear amplifiers.*

Neglecting the v_{gs}^2 term, we can write Equation (6.3(b))

$$i_D = I_{DQ} + i_d \tag{6.5}$$

Again, small-signal implies linearity so that the total current can be separated into a dc component and an ac component. The ac component of the drain current is given by

$$i_d = 2K_n(V_{GSQ} - V_{TN})v_{gs} \tag{6.6}$$

The small-signal drain current is related to the small-signal gate-to-source voltage by the transconductance g_m. The relationship is

$$g_m = \frac{i_d}{v_{gs}} = 2K_n(V_{GSQ} - V_{TN}) \tag{6.7}$$

The transconductance is a transfer coefficient relating output current to input voltage and can be thought of as representing the gain of the transistor.

The transconductance can also be obtained from the derivative

$$g_m = \left.\frac{\partial i_D}{\partial v_{GS}}\right|_{v_{GS}=V_{GSQ}=\text{const.}} = 2K_n(V_{GSQ} - V_{TN}) \tag{6.8(a)}$$

which can be written

$$g_m = 2\sqrt{K_n I_{DQ}} \tag{6.8(b)}$$

The drain current versus gate-to-source voltage for the transistor biased in the saturation region is given in Equation (6.2) and is shown in Figure 6.3. The transconductance g_m is the slope of the curve. If the time-varying signal v_{gs} is sufficiently small, the transconductance g_m is a constant. With the Q-point in the saturation region, the transistor operates as a current source that is linearly controlled by v_{gs}. If the Q-point moves into the nonsaturation region, the transistor no longer operates as a linearly controlled current source.

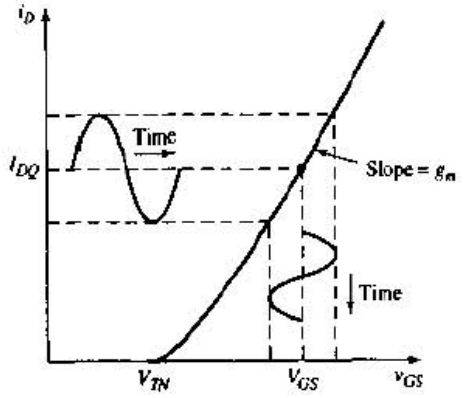

Figure 6.3 Drain current versus gate-to-source voltage characteristics, with superimposed sinusoidal signals

As shown in Equation (6.8(a)), the transconductance is directly proportional to the conduction parameter K_n, which in turn is a function of the width-to-length ratio. Therefore, increasing the width of the transistor increases the transconductance, or gain, of the transistor.

Example 6.1 **Objective:** Calculate the transconductance of an n-channel MOSFET.

Consider an n-channel MOSFET with parameters $V_{TN} = 1\,\text{V}$, $\left(\frac{1}{2}\right)\mu_n C_{ox} = 20\,\mu\text{A/V}^2$, and $W/L = 40$. Assume the drain current is $I_D = 1\,\text{mA}$.

Solution: The conduction parameter is

$$K_n = \left(\frac{1}{2}\mu_n C_{ox}\right)\left(\frac{W}{L}\right) = (20)(40)\,\mu\text{A/V}^2 \Rightarrow 0.80\,\text{mA/V}^2$$

Assuming the transistor is biased in the saturation region, the transconductance is determined from Equation (6.8(b)),

$$g_m = 2\sqrt{K_n I_{DQ}} = 2\sqrt{(0.8)(1)} = 1.79\,\text{mA/V}$$

Comment The transconductance of a bipolar transistor is $g_m = (I_{CQ}/V_T)$, which is 38.5 mA/V for a collector current of 1 mA. The transconductance values of MOSFETs tend to be small compared to those of BJTs. However, the advantages of MOSFETs include high input impedance, small size, and low power dissipation.

AC Equivalent Circuit

From Figure 6.1, we see that the output voltage is

$$v_{DS} = v_O = V_{DD} - i_D R_D \tag{6.9}$$

Using Equation (6.5), we obtain

$$v_O = V_{DD} - (I_{DQ} + i_d)R_D = (V_{DD} - I_{DQ}R_D) - i_d R_D \tag{6.10}$$

The output voltage is also a combination of dc and ac values. The time-varying output signal is the time-varying drain-to-source voltage, or

$$v_o = v_{ds} = -i_d R_D \tag{6.11}$$

Also, from Equations (6.6) and (6.7), we have

$$i_d = g_m v_{gs} \tag{6.12}$$

In summary, the following relationships exist between the time-varying signals for the circuit in Figure 6.1. The equations are given in terms of the instantaneous ac values, as well as the phasors. We have

$$v_{gs} = v_i \tag{6.13(a)}$$

or

$$V_{gs} = V_i \tag{6.13(b)}$$

and

$$i_d = g_m v_{gs} \tag{6.14(a)}$$

or

$$I_d = g_m V_{gs} \tag{6.14(b)}$$

Also,

$$v_{ds} = -i_d R_D \tag{6.15(a)}$$

or

$$V_{ds} = -I_d R_D \tag{6.15(b)}$$

The ac equivalent circuit in Figure 6.4 is developed by setting the dc sources in Figure 6.1 equal to zero. The small-signal relationships are given in Equations (6.13), (6.14), and (6.15). As shown in Figure 6.1, the drain current, which is composed of ac signals superimposed on the quiescent value, flows through the voltage source V_{DD}. Since the voltage across this

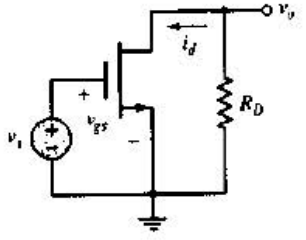

Figure 6.4 AC equivalent circuit of common-source amplifier with NMOS transistor

source is assumed to be constant, the sinusoidal current produces no sinusoidal voltage component across this element. The equivalent ac impedance is therefore zero, or a short circuit. Consequently, in the ac equivalent circuit, the dc voltage sources are equal to zero. We say that the node connecting R_D and V_{DD} is at signal ground.

6.1.2 Small-Signal Equivalent Circuit

Now that we have the ac equivalent circuit for the NMOS amplifier circuit, (Figure 6.4), we must develop a small-signal equivalent circuit for the transistor.

Initially, we assume that the signal frequency is sufficiently low so that any capacitance at the gate terminal can be neglected. The input to the gate thus appears as an open circuit, or an infinite resistance. Equation (6.14) relates the small-signal drain current to the small-signal input voltage, and Equation (6.7) shows that the transconductance g_m is a function of the Q-point. The resulting simplified small-signal equivalent circuit for the NMOS device is shown in Figure 6.5. (The phasor components are in parentheses.)

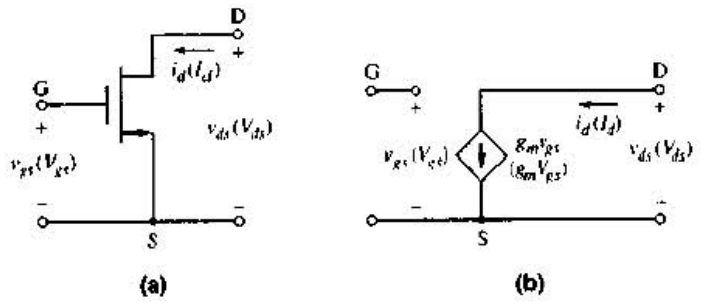

Figure 6.5 (a) Common-source NMOS transistor with small-signal parameters and (b) simplified small-signal equivalent circuit for NMOS transistor

This small-signal equivalent circuit can also be expanded to take into account the finite output resistance of a MOSFET biased in the saturation region. This effect, discussed in the last chapter, is a result of the nonzero slope in the i_D versus v_{DS} curve.

We know that

$$i_D = K_n[(v_{GS} - V_{TN})^2(1 + \lambda v_{DS})] \tag{6.16}$$

where λ is the channel-length modulation parameter and is a positive quantity. The small-signal output resistance, as previously defined, is

$$r_o = \left(\frac{\partial i_D}{\partial v_{DS}}\right)^{-1}\Bigg|_{v_{GS}=V_{GSQ}=\text{const.}} \tag{6.17}$$

or

$$r_o = [\lambda K_n(V_{GSQ} - V_{TN})^2]^{-1} \cong [\lambda I_{DQ}]^{-1} \tag{6.18}$$

This small-signal output resistance is also a function of the Q-point parameters.

The expanded small-signal equivalent circuit of the n-channel MOSFET is shown in Figure 6.6 in phasor notation. Note that this equivalent circuit is a transconductance amplifier (see Table 4.3) in that the input signal is a voltage and the output signal is a current. This equivalent circuit can now be inserted into the amplifier ac equivalent circuit in Figure 6.4 to produce the circuit in Figure 6.7. We may note that the small-signal equivalent circuit for the MOSFET circuit is very similar to that of the BJT circuits considered in Chapter 4.

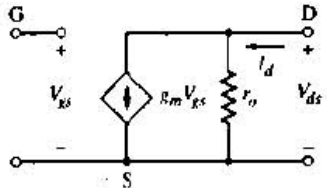

Figure 6.6 Expanded small-signal equivalent circuit, including output resistance, for NMOS transistor

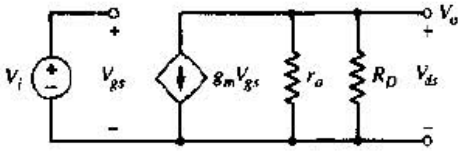

Figure 6.7 Small-signal equivalent circuit of common-source circuit with NMOS transistor model

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Example 6.2 **Objective:** Determine the small-signal voltage gain of a MOSFET circuit.

For the circuit in Figure 6.1, assume parameters are: $V_{GSQ} = 2.12\,\text{V}$, $V_{DD} = 5\,\text{V}$, and $R_D = 2.5\,\text{k}\Omega$. Assume transistor parameters are: $V_{TN} = 1\,\text{V}$, $K_n = 0.80\,\text{mA/V}^2$, and $\lambda = 0.02\,\text{V}^{-1}$. Assume the transistor is biased in the saturation region.

Solution: The quiescent values are

$$I_{DQ} \cong K_n(V_{GSQ} - V_{TN})^2 = (0.8)(2.12 - 1)^2 = 1.0\,\text{mA}$$

and

$$V_{DSQ} = V_{DD} - I_{DQ}R_D = 5 - (1)(2.5) = 2.5\,\text{V}$$

Therefore,

$$V_{DSQ} = 2.5\,\text{V} > V_{DS}(\text{sat}) = V_{GS} - V_{TN} = 1.82 - 1 = 0.82\,\text{V}$$

which means that the transistor is biased in the saturation region, as initially assumed, and as required for a linear amplifier. The transconductance is

$$g_m = 2K_n(V_{GSQ} - V_{TN}) = 2(0.8)(2.12 - 1) = 1.79\,\text{mA/V}$$

and the output resistance is

$$r_o = [\lambda I_{DQ}]^{-1} = [(0.02)(1)]^{-1} = 50\,\text{k}\Omega$$

From Figure 6.7, the output voltage is

$$V_o = -g_m V_{gs}(r_o \| R_D)$$

Since $V_{gs} = V_i$, the small-signal voltage gain is

$$A_v = \frac{V_o}{V_i} = -g_m(r_o \| R_d) = -(1.79)(50 \| 2.5) = -4.26$$

Comment: Because of the relatively low value of transconductance, MOSFET circuits tend to have a lower small-signal voltage gain than comparable bipolar circuits. Also, the small-signal voltage gain contains a minus sign, which means that the sinusoidal output voltage is 180 degrees out of phase with respect to the input sinusoidal signal.

Problem-Solving Technique: MOSFET AC Analysis

Since we are dealing with linear amplifiers, superposition applies, which means that we can perform the dc and ac analyses separately. The analysis of the MOSFET amplifier proceeds as follows:

1. Analyze the circuit with only the dc sources present. This solution is the dc or quiescent solution. The transistor must be biased in the saturation region in order to produce a linear amplifier.
2. Replace each element in the circuit with its small-signal model, which means replacing the transistor by its small-signal equivalent circuit.
3. Analyze the small-signal equivalent circuit, setting the dc source components equal to zero, to produce the response of the circuit to the time-varying input signals only.

Test Your Understanding

6.1 For an n-channel MOSFET biased in the saturation region, the parameters are $K_n = 0.5\,\text{mA/V}^2$, $V_{TN} = 0.8\,\text{V}$, and $\lambda = 0.01\,\text{V}^{-1}$, and $I_{DQ} = 0.75\,\text{mA}$. Determine g_m and r_o. (Ans. $g_m = 1.22\,\text{mA/V}$, $r_o = 1.33\,\text{k}\Omega$)

6.2 The parameters of an n-channel MOSFET are: $V_{TN} = 1\,\text{V}$, $\frac{1}{2}\mu_n C_{ox} = 18\,\mu\text{A/V}^2$, and $\lambda = 0.015\,\text{V}^{-1}$. The transistor is to be biased in the saturation region with $I_{DQ} = 2\,\text{mA}$. Design the width-to-length ratio such that the transconductance is $g_m = 3.4\,\text{mA/V}$. Calculate r_o for this condition. (Ans. $W/L = 80.6$, $r_o = 33.3\,\text{k}\Omega$)

6.3 For the circuit shown in Figure 6.1, $V_{DD} = 10\,\text{V}$ and $R_D = 10\,\text{k}\Omega$. The transistor parameters are: $V_{TN} = 2\,\text{V}$, $K_n = 0.5\,\text{mA/V}^2$, and $\lambda = 0$. (a) Determine V_{GSQ} such that $I_{DQ} = 0.4\,\text{mA}$. Calculate V_{DSQ}. (b) Calculate g_m and r_o, and determine the small-signal voltage gain. (c) If $v_i = 0.4\sin\omega t$, find v_{ds}. Does the transistor remain in the saturation region? (Ans. (a) $V_{GSQ} = 2.89\,\text{V}$, $V_{DSQ} = 6\,\text{V}$; (b) $g_m = 0.89\,\text{mA/V}$, $r_o = \infty$, $A_v = -8.9$; (c) $v_{ds} = -3.56\sin\omega t$, yes)

The previous discussion was for an n-channel MOSFET amplifier. The same basic analysis and equivalent circuit also applies to the p-channel transistor. Figure 6.8(a) shows a circuit containing a p-channel MOSFET. Note that the power supply voltage V_{DD} is connected to the source. (The subscript DD can be used to indicate that the supply is connected to the drain terminal. Here, however, V_{DD} is simply the usual notation for the power supply voltage in MOSFET circuits.) Also note the change in current directions and voltage polarities compared to the circuit containing the NMOS transistor. Figure 6.8(b) shows the ac equivalent circuit, with the dc voltage sources replaced

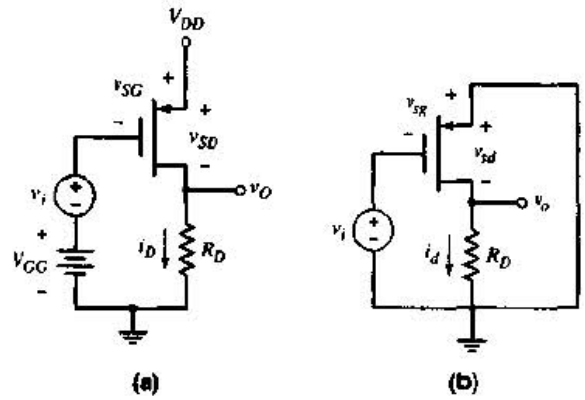

Figure 6.8 (a) Common-source circuit with PMOS transistor and (b) corresponding ac equivalent circuit

by ac short circuits, and all currents and voltages shown are the time-varying components.

In the circuit of Figure 6.8(b), the transistor can be replaced by the equivalent circuit in Figure 6.9. The equivalent circuit of the p-channel MOSFET is the same as that of the n-channel device, except that all current directions and voltage polarities are reversed.

The final small-signal equivalent circuit of the p-channel MOSFET amplifier is shown in Figure 6.10. The output voltage is

$$V_o = g_m V_{sg}(r_o \| R_D) \tag{6.19}$$

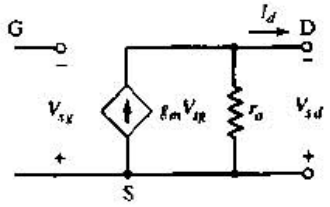

Figure 6.9 Small-signal equivalent circuit of PMOS transistor

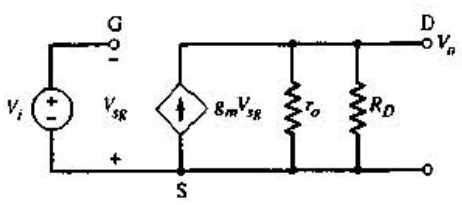

Figure 6.10 Small-signal equivalent circuit of common-source amplifier with PMOS transistor model

The control voltage V_{sg}, given in terms of the input signal voltage, is

$$V_{sg} = -V_i \tag{6.20}$$

and the small-signal voltage gain is

$$A_v = \frac{V_o}{V_i} = -g_m(r_o \| R_D) \tag{6.21}$$

This expression for the small-signal voltage gain of the p-channel MOSFET amplifier is exactly the same as that for the n-channel MOSFET amplifier. The negative sign indicates that a 180-degree phase reversal exists between the ouput and input signals, for both the PMOS and the NMOS circuit.

We may again note that if the polarity of the small-signal gate-to-source voltage is reversed, then the small-signal drain current direction is reversed and the small-signal equivalent circuit of the PMOS device is exactly identical to that of the NMOS device. However, the author prefers to use the small-signal equivalent circuit in Figure 6.9 to be consistent with the voltage polarities and current directions of the PMOS transistor.

6.1.3 Modeling the Body Effect

As mentioned in Section 5.1.7, Chapter 5, the body effect occurs in a MOSFET in which the substrate, or body, is not connected to the source. For an NMOS device, the body is connected to the most negative potential in the circuit and will be at signal ground. Figure 6.11(a) shows the four-terminal MOSFET with dc voltages and Figure 6.11(b) shows the device with ac voltages. Keep in mind that v_{SB} must be greater than or equal to zero. The simplified current-voltage relation is

$$i_D = K_n(v_{GS} - V_{TN})^2 \tag{6.22}$$

and the threshold voltage is given by

$$V_{TN} = V_{TNO} + \gamma\left[\sqrt{2\phi_f + v_{SB}} - \sqrt{2\phi_f}\right] \tag{6.23}$$

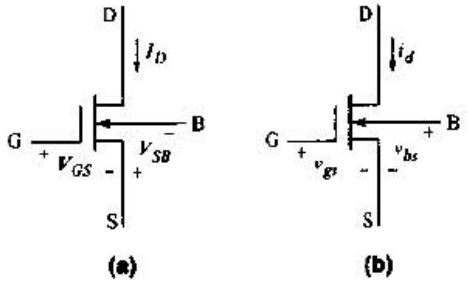

Figure 6.11 The four-terminal NMOS device with (a) dc voltages and (b) ac voltages

If an ac component exists in the source-to-body voltage, v_{SB}, there will be an ac component induced in the threshold voltage, which causes an ac component in the drain current. Thus, a back-gate transconductance can be defined as

$$g_{mb} = \left.\frac{\partial i_D}{\partial v_{BS}}\right|_{Q\text{-}pt} = \left.\frac{-\partial i_D}{\partial v_{SB}}\right|_{Q\text{-}pt} = -\left(\frac{\partial i_D}{\partial V_{TN}}\right)\cdot\left.\left(\frac{\partial V_{TN}}{\partial v_{SB}}\right)\right|_{Q\text{-}pt} \tag{6.24}$$

Using Equation (6.22), we find

$$\frac{\partial i_D}{\partial V_{TN}} = -2K_n(v_{GS} - V_{TN}) = -g_m \tag{6.25(a)}$$

and using Equation (6.23), we find

$$\frac{\partial V_{TN}}{\partial v_{SB}} = \frac{\gamma}{2\sqrt{2\phi_f + v_{SB}}} \equiv \eta \tag{6.25(b)}$$

The back-gate transconductance is then

$$g_{mb} = -(-g_m) \cdot (\eta) = g_m \eta \tag{6.26}$$

Including the body effect, the small-signal equivalent circuit of the MOSFET is shown in Figure 6.12. We note the direction of the current and the polarity of the small-signal source-to-body voltage. If $v_{bs} > 0$, then v_{SB} decreases, V_{TN} decreases, and i_D increases. The current direction and voltage polarity are thus consistent.

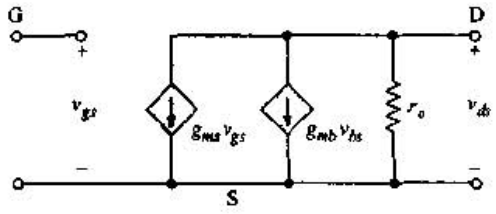

Figure 6.12 Small-signal equivalent circuit of NMOS device including body effect

For $\phi_f = 0.35\,\text{V}$ and $\gamma = 0.35\,\text{V}^{1/2}$, the value of η from Equation (6.25(b)) is $\eta \cong 0.23$. Therefore, η will be in the range $0 \leq \eta \leq 0.23$. The value of v_{bs} will depend on the particular circuit.

In general, we will neglect g_{mb} in our hand analyses and designs, but will investigate the body effect in PSpice analyses.

Test Your Understanding

6.4 The parameters for the circuit in Figure 6.8 are $V_{DD} = 12\,\text{V}$ and $R_D = 6\,\text{k}\Omega$. The transistor parameters are: $V_{TP} = -1\,\text{V}$, $K_p = 2\,\text{mA/V}^2$, and $\lambda = 0$. (a) Determine V_{SG} such that $V_{SDQ} = 7\,\text{V}$. (b) Determine g_m and r_o, and calculate the small-signal voltage gain. (Ans. (a) $V_{SG} = 1.65\,\text{V}$; (b) $g_m = 2.6\,\text{mA/V}$, $r_o = \infty$, $A_v = -15.6$)

6.5 Show that, for an NMOS transistor biased in the saturation region, with a drain current of I_{DQ}, the transconductance can be expressed as given in Equation (6.8(b)), that is

$$g_m = 2\sqrt{K_n I_{DQ}}$$

6.6 A transistor has the same parameters as those given in Exercise 6.1. In addition, the body effect coefficient is $\gamma = 0.40\,\text{V}^{1/2}$ and $\phi_f = 0.35\,\text{V}$. Determine the value of η and the back-gate transconductance g_{mb} for (a) $v_{SB} = 1\,\text{V}$ and (b) $v_{SB} = 3\,\text{V}$.

6.2 BASIC TRANSISTOR AMPLIFIER CONFIGURATIONS

As we have seen, the MOSFET is a three-terminal device. Three basic single-transistor amplifier configurations can be formed, depending on which of the three transistor terminals is used as signal ground. These three basic configurations are appropriately called **common source, common drain (source follower)**, and **common gate**. These three circuit configurations correspond to the common-emitter, emitter-follower, and common-base configurations using

BJTs. The similarities and differences between the FET and BJT circuits will be discussed.

The input and output resistance characteristics of amplifiers are important in determining loading effects. These parameters, as well as voltage gain, for the three basic MOSFET circuit configurations will be determined in the following sections. The characteristics of the three types of amplifiers will then allow us to understand under what condition each amplifier is most useful.

Initially, we will consider MOSFET amplifier circuits that emphasize discrete designs, in that resistor biasing will be used. The purpose is to become familiar with basic MOSFET amplifier designs and their characteristics, using biasing techniques similar to those used in BJT amplifiers in previous chapters. In Section 6.7, we will begin to consider integrated circuit MOSFET designs that involve all-transistor circuits and current source biasing. These initial designs provide an introduction to more advanced MOS amplifier designs that will be considered in Part II of the text.

6.3 THE COMMON-SOURCE AMPLIFIER

In this section, we consider the first of the three basic circuits—the common-source amplifier. We will analyze several basic common-source circuits, and will determine small-signal voltage gain and input and output impedances.

6.3.1 A Basic Common-Source Configuration

For the circuit shown in Figure 6.13, assume that the transistor is biased in the saturation region by resistors R_1 and R_2, and that the signal frequency is sufficiently large for the coupling capacitor to act essentially as a short circuit. The signal source is represented by a Thevenin equivalent circuit, in which the signal voltage source v_i is in series with an equivalent source resistance R_{Si}. As we will see, R_{Si} should be much less than the amplifier input resistance, $R_i = R_1 \| R_2$, in order to minimize loading effects.

Figure 6.14 shows the resulting small-signal equivalent circuit. The small-signal variables, such as the input signal voltage V_i, are given in phasor form.

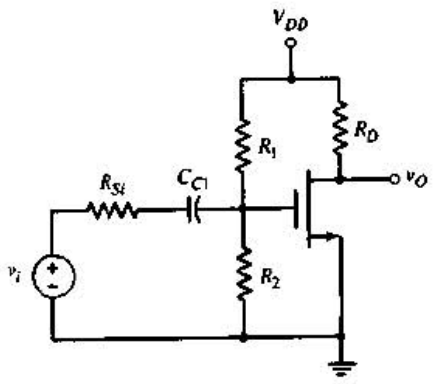

Figure 6.13 Common-source circuit with voltage divider biasing and coupling capacitor

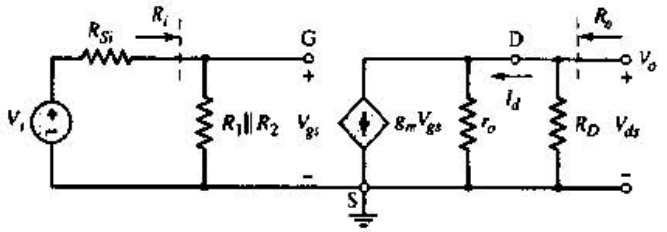

Figure 6.14 Small-signal equivalent circuit, assuming coupling capacitor acts as a short circuit

Since the source is at ground potential, there is no body effect. The output voltage is

$$V_o = -g_m V_{gs}(r_o \| R_D) \tag{6.27}$$

The input gate-to-source voltage is

$$V_{gs} = \left(\frac{R_i}{R_i + R_{Si}}\right) \cdot V_i \tag{6.28}$$

so the small-signal voltage gain is

$$A_v = \frac{V_o}{V_i} = -g_m(r_o \| R_D) \cdot \left(\frac{R_i}{R_i + R_{Si}}\right) \tag{6.29}$$

We can also relate the ac drain current to the ac drain-to-source voltage, as $V_{ds} = -I_d(R_D)$.

Figure 6.15 shows the dc load line, the transition point, and the Q-point, which is in the saturation region. As previously stated, in order to provide the maximum symmetrical output voltage swing and keep the transistor biased in the saturation region, the Q-point must be near the middle of the saturation region. At the same time, the input signal must be small enough for the amplifier to remain linear.

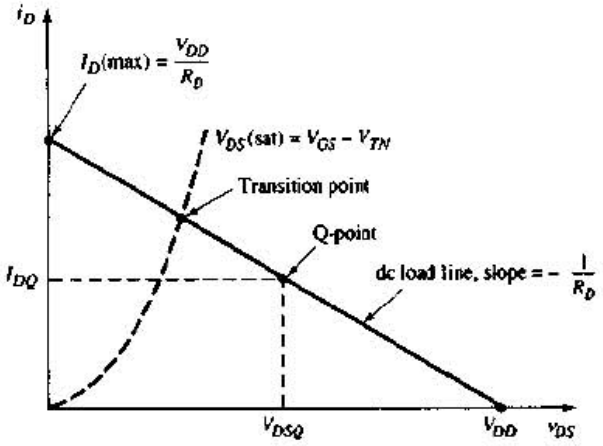

Figure 6.15 DC load line and transition point separating saturation and nonsaturation regions

The input and output resistances of the amplifier can be determined from Figure 6.14. The input resistance to the amplifier is $R_{is} = R_1 \| R_2$. Since the low-frequency input resistance looking into the gate of the MOSFET is essentially infinite, the input resistance is only a function of the bias resistors. The output resistance looking back into the output terminals is found by setting the independent input source V_i equal to zero, which means that $V_{gs} = 0$. The output resistance is therefore $R_o = R_D \| r_o$.

Example 6.3 **Objective:** Determine the small-signal voltage gain and input and output resistances of a common-source amplifier.

For the circuit shown in Figure 6.13, the parameters are: $V_{DD} = 10\,\text{V}$, $R_1 = 70.9\,\text{k}\Omega$, $R_2 = 29.1\,\text{k}\Omega$, and $R_D = 5\,\text{k}\Omega$. The transistor parameters are: $V_{TN} = 1.5\,\text{V}$, $K_n = 0.5\,\text{mA/V}^2$, and $\lambda = 0.01\,\text{V}^{-1}$. Assume $R_{Si} = 4\,\text{k}\Omega$.

Solution: **DC Calculations**: The dc or quiescent gate-to-source voltage is

$$V_{GSQ} = \left(\frac{R_2}{R_1 + R_2}\right)(V_{DD}) = \left(\frac{29.1}{70.9 + 29.1}\right)(10) = 2.91\,\text{V}$$

The quiescent drain current is

$$I_{DQ} = K_n(V_{GSQ} - V_{TN})^2 = (0.5)(2.91 - 1.5)^2 = 1\,\text{mA}$$

and the quiescent drain-to-source voltage is

$$V_{DSQ} = V_{DD} - I_{DQ}R_D = 10 - (1)(5) = 5\,\text{V}$$

Since $V_{DSQ} > V_{GSQ} - V_{TN}$, the transistor is biased in the saturation region.

Small-signal Voltage Gain: The small-signal transconductance g_m is then

$$g_m = 2K_n(V_{GSQ} - V_{TN}) = 2(0.5)(2.91 - 1.5) = 1.41\,\text{mA/V}$$

and the small-signal output resistance r_o is

$$r_o \cong [\lambda I_{DQ}]^{-1} = [(0.01)(1)]^{-1} = 100\,\text{k}\Omega$$

The amplifier input resistance is

$$R_i = R_1 \| R_2 = 70.9 \| 29.1 = 20.6\,\text{k}\Omega$$

From Figure 6.14 and Equation (6.29), the small-signal voltage gain is

$$A_v = -g_m(r_o \| R_D) \cdot \left(\frac{R_i}{R_i + R_{Si}}\right) = -(1.41)(100 \| 5)\left(\frac{20.6}{20.6 + 4}\right)$$

or

$$A_v = -5.62$$

Input and Output Resistances: As already calculated, the amplifier input resistance is

$$R_i = R_1 \| R_2 = 70.9 \| 29.1 = 20.6\,\text{k}\Omega$$

and the amplifier output resistance is

$$R_o = R_D \| r_o = 5 \| 100 = 4.76\,\text{k}\Omega$$

Comment: The resulting Q-point is in the center of the load line but not in the center of the saturation region. Therefore, this circuit does not achieve the maximum symmetrical output voltage swing in this case.

Discussion: The small-signal input gate-to-source voltage is

$$V_{gs} = \left(\frac{R_i}{R_i + R_{Si}}\right) \cdot V_i = \left(\frac{20.6}{20.6+4}\right) \cdot V_i = (0.837) \cdot V_i$$

Since R_{Si} is not zero, the amplifier input signal V_{gs} is approximately 84 percent of the signal voltage. This is again called a loading effect. Even though the input resistance to the gate of the transistor is essentially infinite, the bias resistors greatly influence the amplifier input resistance and loading effect.

Test Your Understanding

6.7 Consider the circuit in Figure 6.1 with circuit parameters $V_{DD} = 5\,\text{V}$, $R_D = 5\,\text{k}\Omega$, $V_{GSQ} = 2\,\text{V}$, and with transistor paramaeters $K_n = 0.25\,\text{mA/V}^2$, $V_{TN} = 0.8\,\text{V}$, and $\lambda = 0$. (a) Calculate the quiescent values I_{DQ} and V_{DSQ}. (b) Calculate the transconductance g_m. (c) Determine the small-signal voltage gain $A_v = v_o/v_i$. (Ans. (a) $I_{DQ} = 0.36\,\text{mA}$, $V_{DSQ} = 3.2\,\text{V}$; (b) $g_m = 0.6\,\text{mA/V}$, $r_o = \infty$; (c) $A_v = -3.0$)

6.8 For the circuit in Figure 6.1, the circuit and transistor parameters are given in Exercise 6.7. If $v_i = 0.1 \sin \omega t\,\text{V}$, determine i_D and v_{DS}. (Ans. $i_D = (0.36 + 0.06 \sin \omega t)\,\text{mA}$, $v_{DS} = (3.2 - 0.3 \sin \omega t)\,\text{V}$)

Design Example 6.4 **Objective:** Design the bias of a MOSFET such that the Q-point is in the middle of the saturation region.

Consider the circuit in Figure 6.16 with transistor parameters $V_{TN} = 1\,\text{V}$, $K_n = 1\,\text{mA/V}^2$, and $\lambda = 0.015\,\text{V}^{-1}$. Let $R_i = R_1 \| R_2 = 100\,\text{k}\Omega$. Design the circuit such that $I_{DQ} = 2\,\text{mA}$ and the Q-point is in the middle of the saturation region.

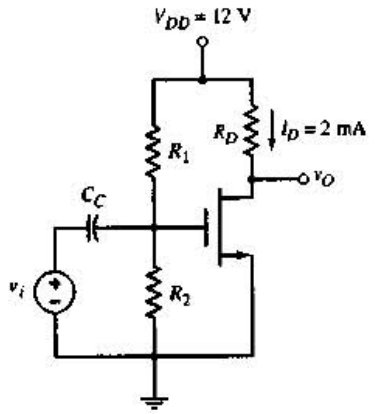

Figure 6.16 Common-source NMOS transistor circuit

Solution: The load line and the desired Q-point are given in Figure 6.17. If the Q-point is to be in the middle of the saturation region, the current at the transition point must be 4 mA.

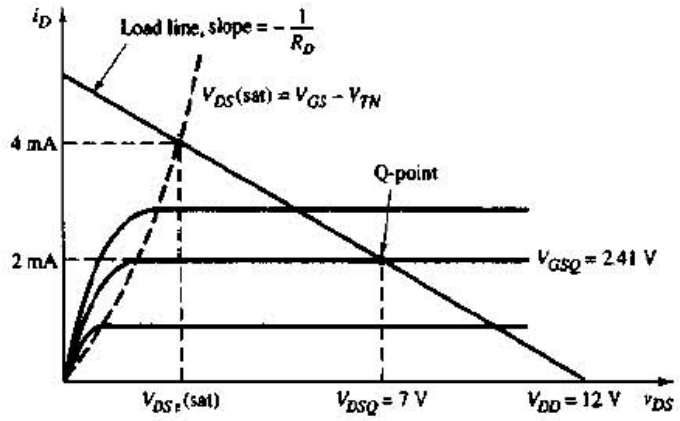

Figure 6.17 DC load line and transition point for NMOS circuit shown in Figure 6.16

We can now calculate $V_{DS}(\text{sat})$ at the transition point. The subscript t indicates transition point values. To determine V_{GSt}, we use

$$I_{Dt} = 4 = K_n(V_{GSt} - V_{TN})^2 = 1(V_{GSt} - 1)^2$$

which yields

$$V_{GSt} = 3\,\text{V}$$

Therefore

$$V_{DSt} = V_{GSt} - V_{TN} = 3 - 1 = 2\,\text{V}$$

If the Q-point is in the middle of the saturation region, then $V_{DSQ} = 7\,\text{V}$, which would yield a 10 V peak-to-peak symmetrical output voltage. From Figure 6.16, we can write

$$V_{DSQ} = V_{DD} - I_{DQ}R_D$$

or

$$R_D = \frac{V_{DD} - V_{DSQ}}{I_{DQ}} = \frac{12 - 7}{2} = 2.5\,\text{k}\Omega$$

We can determine the required quiescent gate-to-source voltage from the current equation, as follows:

$$I_{DQ} = 2 = K_n(V_{GSQ} - V_{TN})^2 = (1)(V_{GSQ} - 1)^2$$

or

$$V_{GSQ} = 2.41\,\text{V}$$

Then

$$V_{GSQ} = 2.41 = \left(\frac{R_2}{R_1 + R_2}\right)(V_{DD}) = \left(\frac{1}{R_1}\right)\left(\frac{R_1R_2}{R_1 + R_2}\right)(V_{DD})$$
$$= \frac{R_2}{R_1} \cdot V_{DD} = \frac{(100)(12)}{R_1}$$

which yields

$$R_1 = 498\,\text{k}\Omega \quad \text{and} \quad R_2 = 125\,\text{k}\Omega$$

We can then determine the small-signal equivalent circuit parameters from the Q-point values. The transconductance is $g_m = 2.82\,\text{mA/V}$, the transistor output resistance is $r_o = 33.3\,\text{k}\Omega$, and the small-signal voltage gain, assuming an ideal signal source, is

$$A_v = \frac{V_o}{V_i} = -g_m(r_o \| R_D) = -(2.82)(33.3 \| 2.5) = -6.56$$

Comment: Establishing the Q-point in the middle of the saturation region allows the maximum symmetrical swing in the output voltage, while keeping the transistor biased in the saturation region.

Design Pointer: If the circuit were to contain bypass or load capacitors, then an ac load line would be superimposed on the figure at the Q-point. Establishing the Q-point in the middle of the saturation region, then, may not be optimal in terms of obtaining the maximum symmetrical swing.

6.3.2 Common-Source Amplifier with Source Resistor

A source resistor R_S tends to stabilize the Q-point against variations in transistor parameters (Figure 6.18). If, for example, the value of the conduction parameter varies from one transistor to another, the Q-point will not vary as much if a source resistor is included in the circuit. However, as shown in the following example, a source resistor also reduces the signal gain. This same effect was observed in BJT circuits when an emitter resistor was included.

The circuit in Figure 6.18 is an example of a situation in which the body effect should be taken into account. The substrate (not shown) would normally be connected to the −5 V supply, so that the body and substrate terminals are not at the same potential. However, in the following example, we will neglect this effect.

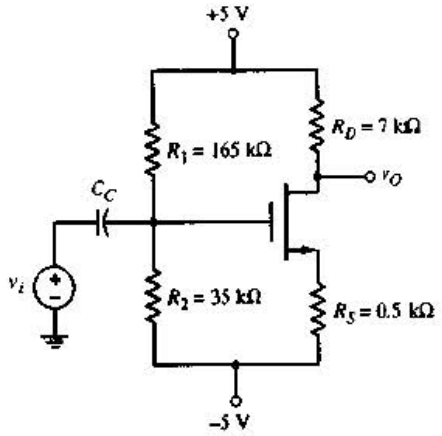

Figure 6.18 Common-source circuit with source resistor and positive and negative supply voltages

Example 6.5 **Objective:** Determine the small-signal voltage gain of a common-source circuit containing a source resistor.

Consider the circuit in Figure 6.18. The transistor parameters are $V_{TN} = 0.8$ V, $K_n = 1$ mA/V^2, and $\lambda = 0$.

Solution: From the dc analysis of the circuit, we find that $V_{GSQ} = 1.50\,\text{V}$, $I_{DQ} = 0.50\,\text{mA}$, and $V_{DSQ} = 6.25\,\text{V}$. The small-signal transconductance is

$$g_m = 2K_n(V_{GS} - V_{TN}) = 2(1)(1.50 - 0.8) = 1.4\,\text{mA/V}$$

and the small-signal resistance is

$$r_o \cong [\lambda I_{DQ}]^{-1} = \infty$$

Figure 6.19 shows the resulting small-signal equivalent circuit.

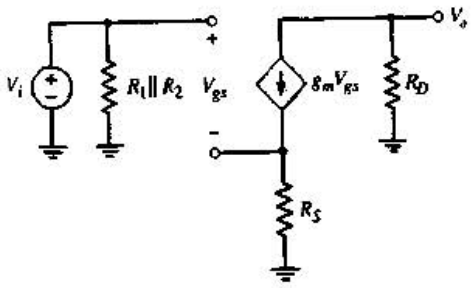

Figure 6.19 Small-signal equivalent circuit of NMOS common-source amplifier with source resistor

The output voltage is

$$V_o = -g_m V_{gs} R_D$$

Writing a KVL equation from the input around the gate–source loop, we find

$$V_i = V_{gs} + (g_m V_{gs}) R_S = V_{gs}(1 + g_m R_S)$$

or

$$V_{gs} = \frac{V_i}{1 + g_m R_S}$$

The small-signal voltage gain is

$$A_v = \frac{V_o}{V_i} = \frac{-g_m R_D}{1 + g_m R_S}$$

We may note that if g_m were large, then the small-signal voltage gain would be approximately

$$A_v \cong \frac{-R_D}{R_S}$$

Substituting the appropriate parameters into the actual voltage gain expression, we find

$$A_v = \frac{-(1.4)(7)}{1 + (1.4)(0.5)} = -5.76$$

Comment: A source resistor reduces the small-signal voltage gain. However, as discussed in the last chapter, the Q-point is more stabilized against variations in the transistor parameters. We may note that the approximate voltage gain gives $A_v \cong -R_D/R_S = -14$. Since the transconductance of MOSFETs is generally low, the approximate gain expression is a poor one at best.

Discussion: We mentioned that including a source resistor tends to stabilize the circuit characteristics against any changes in transistor parameters. If, for example, the conduction parameter K_n varies by ±20 percent, we find the following results.

K_n (mA/V^2)	g_m (mA/V)	A_v
0.8	1.17	−5.17
1.0	1.40	−5.76
1.2	1.62	−6.27

The change in K_n produces a fairly large change in g_m. The resulting change in the voltage gain is approximately ±9.5 percent. This change is larger than might be expected because the initial value of g_m is smaller than that of the bipolar circuit

Test Your Understanding

6.9 For the circuit shown in Figure 6.20, the transistor parameters are $K_p = 1$ mA/V^2, $V_{TP} = -1$ V, and $\lambda = 0$. The source-to-drain voltage is $v_{SD} = 3 + 0.46 \sin \omega t$ V, and the quiescent drain current is $I_{DQ} = 0.5$ mA. Determine R_D, V_{GG}, v_i, and the small-signal voltage gain. (Ans. $R_D = 4\,\text{k}\Omega$, $V_{GG} = 3.29$ V, $A_v = -5.64$, $v_i = +0.0816 \sin \omega t$ V)

6.10 The common-source amplifier in Figure 6.21 has transistor parameters $K_p = 2\,\text{mA/V}^2$, $V_{TP} = -2$ V, and $\lambda = 0.01\,\text{V}^{-1}$. (a) Determine I_{DQ} and V_{SDQ}. (b) Calculate the small-signal voltage gain. (Ans. (a) $I_{DQ} = 4.56$ mA, $V_{SDQ} = 7.97$ V; (b) $A_v = -6.04$)

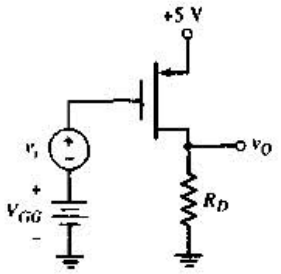

Figure 6.20 Figure for Exercise 6.9

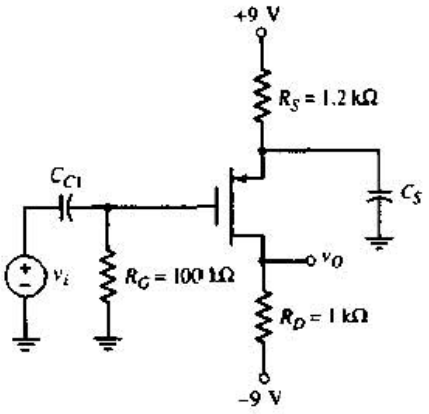

Figure 6.21 Figure for Exercise 6.10

6.3.3 Common-Source Circuit with Source Bypass Capacitor

A source bypass capacitor added to the common-source circuit with a source resistor will minimize the loss in the small-signal voltage gain, while maintaining the Q-point stability. The Q-point stability can be further increased by

replacing the source resistor with a constant-current source. The resulting circuit is shown in Figure 6.22, assuming an ideal signal source. If the signal frequency is sufficiently large so that the bypass capacitor acts essentially as an ac short-circuit, the source will be held at signal ground.

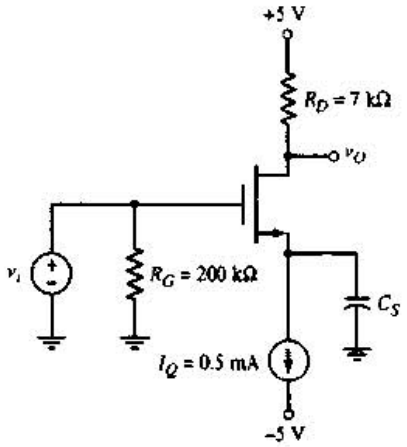

Figure 6.22 NMOS common-source circuit with source bypass capacitor

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Example 6.6 **Objective:** Determine the small-signal voltage gain of a circuit biased with a constant-current source and incorporating a source bypass capacitor.

For the circuit shown in Figure 6.22, the transistor parameters are: $V_{TN} = 0.8$ V, $K_n = 1$ mA/V^2, and $\lambda = 0$.

Solution: Since the dc gate current is zero, the dc voltage at the source terminal is $V_S = -V_{GSQ}$, and the gate-to-source voltage is determined from

$$I_{DQ} = I_Q = K_n(V_{GSQ} - V_{TN})^2$$

or

$$0.5 = (1)(V_{GSQ} - 0.8)^2$$

which yields

$$V_{GSQ} = -V_S = 1.51 \text{ V}$$

The quiescent drain-to-source voltage is

$$V_{DSQ} = V_{DD} - I_{DQ}R_D - V_S = 5 - (0.5)(7) - (-1.51) = 3.01 \text{ V}$$

The transistor is therefore biased in the saturation region.

The small-signal equivalent circuit is shown in Figure 6.23. The output voltage is

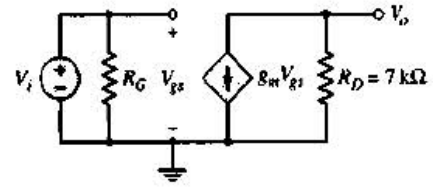

Figure 6.23 Small-signal equivalent circuit, assuming the source bypass capacitor acts as a short circuit

$$V_o = -g_m V_{gs} R_D$$

Since $V_{gs} = V_i$, the small-signal voltage gain is

$$A_v = \frac{V_o}{V_i} = -g_m R_D = -(1.4)(7) = -9.8$$

Comment: Comparing the small-signal voltage gain of 9.8 in this example to the 5.76 calculated in Example 6.5, we see that the magnitude of the gain increases when a source bypass capacitor is included.

Test Your Understanding

***D6.11** The common-source amplifier in Figure 6.24 has transistor parameters $V_{TN} = 1.5\,\text{V}$, $\frac{1}{2}\mu_n C_{ox} = 20\,\mu\text{A/V}^2$, and $\lambda = 0$. Design the circuit such that $I_{DQ} = 0.5\,\text{mA}$ and the small-signal voltage gain is $A_v = -4.0$. (Ans. For example: For $V_{GS} = 2.5\,\text{V}$, then $W/L = 25$, $R_D = 4.0\,\text{k}\Omega$)

6.12 Consider the common-source amplifier in Figure 6.25 with transistor parameters $V_{TN} = 1.8\,\text{V}$, $K_n = 0.15\,\text{mA/V}^2$, and $\lambda = 0$. (a) Calculate I_{DQ} and V_{DSQ}. (b) Determine the small-signal voltage gain. (c) Discuss the purpose of R_G and its effect on the small-signal operation of the amplifier. (Ans. (a) $I_{DQ} = 1.05\,\text{mA}$, $V_{DSQ} = 4.45\,\text{V}$; (b) $A_v = -2.65$)

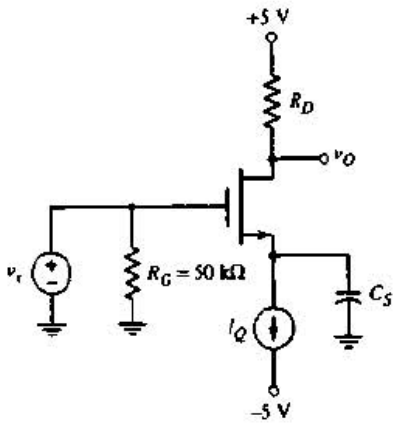

Figure 6.24 Figure for Exercise 6.11

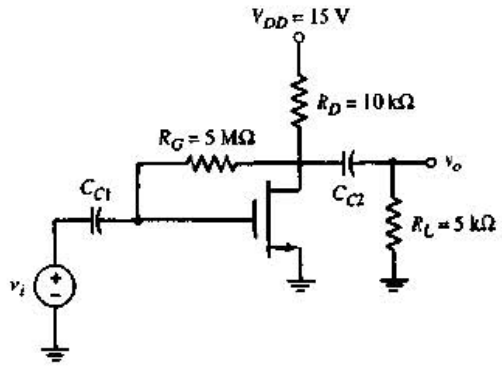

Figure 6.25 Figure for Exercise 6.12

***6.13** For the circuit in Figure 6.26, the n-channel depletion-mode transistor parameters are: $K_n = 0.8\,\text{mA/V}^2$, $V_{TN} = -2\,\text{V}$, and $\lambda = 0$. (a) Calculate I_{DQ}. (b) Find R_D such that $V_{DSQ} = 6\,\text{V}$. (c) Determine the small-signal voltage gain. (Ans. (a) $I_{DQ} = 0.338\,\text{mA}$; (b) $R_D = 7.83\,\text{k}\Omega$; (c) $A_v = -1.58$)

6.14 The parameters of the transistor shown in Figure 6.27 are: $V_{TP} = +0.8\,\text{V}$, $K_p = 0.5\,\text{mA/V}^2$, and $\lambda = 0.02\,\text{V}^{-1}$. (a) Determine R_S and R_D such that $I_{DQ} = 0.8\,\text{mA}$ and $V_{SDQ} = 3\,\text{V}$. (b) Find the small-signal voltage gain. (Ans. (a) $R_S = 5.67\,\text{k}\Omega$, $R_D = 3.08\,\text{k}\Omega$; (b) $A_v = -3.73$)

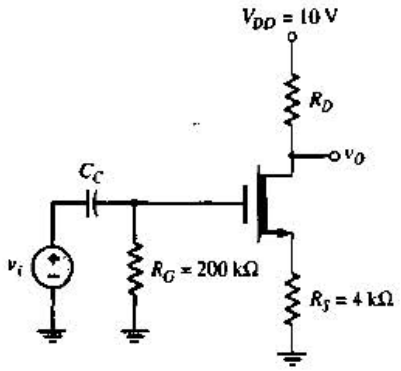

Figure 6.26 Figure for Exercise 6.13

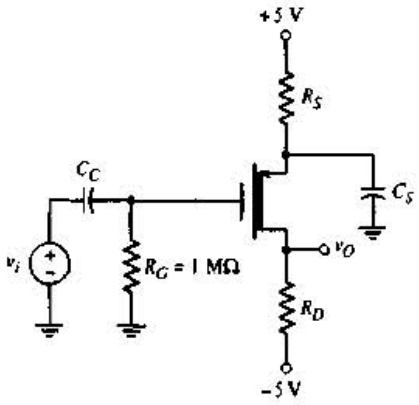

Figure 6.27 Figure for Exercise 6.14

6.4 THE SOURCE-FOLLOWER AMPLIFIER

The second type of MOSFET amplifier to be considered is the **common-drain circuit**. An example of this circuit configuration is shown in Figure 6.28. As seen in the figure, the output signal is taken off the source with respect to ground and the drain is connected directly to V_{DD}. Since V_{DD} becomes signal ground in the ac equivalent circuit, we have the name common drain. The more common name is **source follower**. The reason for this name will become apparent as we proceed through the analysis.

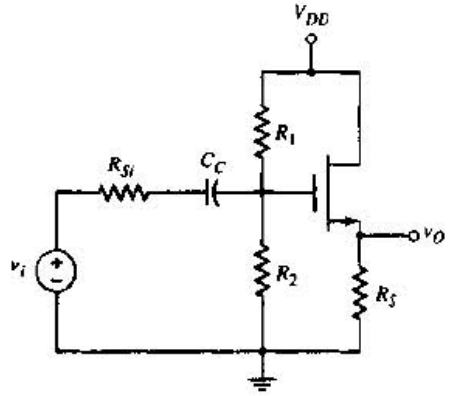

Figure 6.28 NMOS source-follower or common-drain amplifier

6.4.1 Small-Signal Voltage Gain

The dc analysis of the circuit is exactly the same as we have already seen, so we will concentrate on the small-signal analysis. The small-signal equivalent circuit, assuming the coupling capacitor acts as a short circuit, is shown in Figure 6.29(a). The drain is at signal ground, and the small-signal resistance r_o of the transistor is in parallel with the dependent current source. Figure 6.29(b) is the same equivalent circuit, but with all signal grounds at a common point. We are again neglecting the body effect. The output voltage is

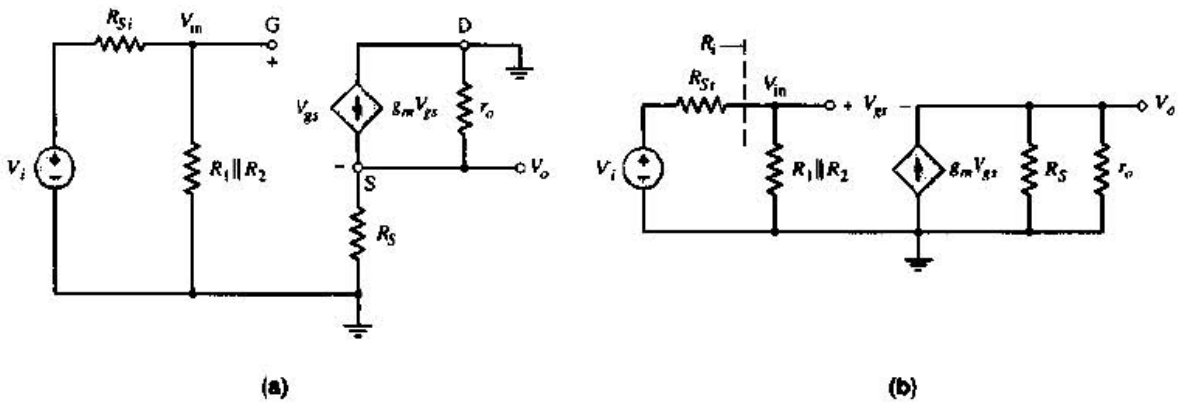

Figure 6.29 (a) Small-signal equivalent circuit of NMOS source follower and (b) small-signal equivalent circuit of NMOS source follower with all signal grounds at a common point

$$V_o = (g_m V_{gs})(R_S \| r_o) \tag{6.30}$$

Writing a KVL equation from input to output results in the following:

$$V_{in} = V_{gs} + V_o = V_{gs} + g_m V_{gs}(R_S \| r_o) \tag{6.31(a)}$$

Therefore, the gate-to-source voltage is

$$V_{gs} = \frac{V_{in}}{1 + g_m(R_S \| r_o)} = \left[\frac{\dfrac{1}{g_m}}{\dfrac{1}{g_m} + (R_S \| r_o)}\right] \cdot V_{in} \tag{6.31(b)}$$

Equation (6.31(b)) is written in the form of a voltage-divider equation, in which the gate-to-source of the NMOS device looks like a resistance with a value of $1/g_m$. More accurately, the effective resistance looking into the source terminal (ignoring r_o) is $1/g_m$. The voltage V_{in} is related to the source input voltage V_i by

$$V_{in} = \left(\frac{R_i}{R_i + R_{Si}}\right) \cdot V_i \tag{6.32}$$

where $R_i = R_1 \| R_2$ is the input resistance to the amplifier.

Substituting Equations (6.31(b)) and (6.32) into (6.30), we have the small-signal voltage gain:

$$A_v = \frac{V_o}{V_i} = \frac{g_m(R_S \| r_o)}{1 + g_m(R_S \| r_o)} \cdot \left(\frac{R_i}{R_i + R_{Si}}\right) \tag{6.33(a)}$$

or

$$A_v = \frac{R_S \| r_o}{\dfrac{1}{g_m} + R_S \| r_o} \cdot \left(\frac{R_i}{R_i + R_{Si}}\right) \tag{6.33(b)}$$

which again is written in the form of a voltage-divider equation. An inspection of Equation 6.33(b) shows that the magnitude of the voltage gain is always less than unity. This result is consistent with the results of the BJT emitter-follower circuit.

Example 6.7 **Objective:** Calculate the small-signal voltage gain of the source-follower circuit in Figure 6.28.

Assume the circuit parameters are $V_{DD} = 12\,V$, $R_1 = 162\,k\Omega$, $R_2 = 463\,k\Omega$, and $R_S = 0.75\,k\Omega$, and the transistor parameters are $V_{TN} = 1.5\,V$, $K_n = 4\,mA/V^2$, and $\lambda = 0.01\,V^{-1}$. Also assume $R_{Si} = 4\,k\Omega$.

Solution: The dc analysis results are $I_{DQ} = 7.97\,mA$ and $V_{GSQ} = 2.91\,V$. The small-signal transconductance is therefore

$$g_m = 2K_n(V_{GSQ} - V_{TN}) = 2(4)(2.91 - 1.5) = 11.3\,mA/V$$

and the small-signal transistor resistance is

$$r_o \cong [\lambda I_{DQ}]^{-1} = [(0.01)(7.97)]^{-1} = 12.5\,k\Omega$$

The amplifier input resistance is

$$R_i = R_1 \| R_2 = 162 \| 463 = 120\,k\Omega$$

The small-signal voltage gain then becomes

$$A_v = \frac{g_m(R_S \| r_o)}{1 + g_m(R_S \| r_o)} \cdot \frac{R_i}{R_i + R_{Si}} = \frac{(11.3)(0.75 \| 12.5)}{1 + (11.3)(0.75 \| 12.5)} \cdot \frac{120}{120 + 4} = +0.860$$

Comment: The magnitude of the small-signal voltage gain is less than 1. An examination of Equation (6.33(b)) shows that this is always true. Also, the voltage gain is positive, which means that the output signal voltage is in phase with the input signal voltage. Since the output signal is essentially equal to the input signal, the circuit is called a source follower.

Discussion: The expression for the voltage gain of the source follower is essentially identical to that of the bipolar emitter follower. Since the transconductance of the BJT is, in general, larger than that of the MOSFET, the voltage gain of the emitter follower will be closer to unity than that of the MOSFET source follower.

Although the voltage gain is slightly less than 1, the source follower is an extremely useful circuit because the output resistance is less than that of a common-source circuit. A small output resistance is desirable when the circuit is to act as an ideal voltage source and drive a load circuit without suffering any loading effects.

Test Your Understanding

6.15 For an NMOS source-follower circuit, the parameters are $g_m = 4\,mA/V$ and $r_o = 50\,k\Omega$. (a) Find the no load ($R_S = \infty$) small-signal voltage gain and the output resistance. (b) Determine the small-signal voltage gain when a $4\,k\Omega$ load is connected to the output. (Ans. (a) $A_v = 0.995$, $R_o \cong 0.25\,k\Omega$; (b) $A_v = 0.937$)

D6.16 The source-follower circuit in Figure 6.28 has transistor parameters $V_{TN} = +0.8\,V$, $K_n = 1\,mA/V^2$, and $\lambda = 0.015\,V^{-1}$. Let $V_{DD} = 10\,V$, $R_{Si} = 200\,\Omega$, and $R_1 + R_2 = 400\,k\Omega$. Design the circuit such that $I_{DQ} = 1.5\,mA$ and $V_{DSQ} = 5\,V$. Determine the small-signal voltage gain and the output resistance. (Ans. $R_S = 3.33\,k\Omega$, $R_1 = 119\,k\Omega$, $R_2 = 281,\,k\Omega$, $A_v = 0.884$, and $R_o = 0.36\,k\Omega$)

Design Example 6.8 **Objective:** Design a specific source follower with a p-channel enhancement-mode MOSFET.

For the circuit in Figure 6.30, the transistor parameters are $V_{TP} = -2\,\text{V}$, $k_p' = 40\,\mu\text{A/V}^2$, and $\lambda = 0$. The circuit parameters are $V_{DD} = 20\,\text{V}$ and $R_{Si} = 4\,\text{k}\Omega$.

The circuit is to be designed such that $V_{SDQ} = 10\,\text{V}$, $I_{DQ} = 2.5\,\text{mA}$, and $R_i = 50\,\text{k}\Omega$, and the transistor width-to-length ratio is to be designed such that the small-signal voltage gain is $A_v = 0.90$.

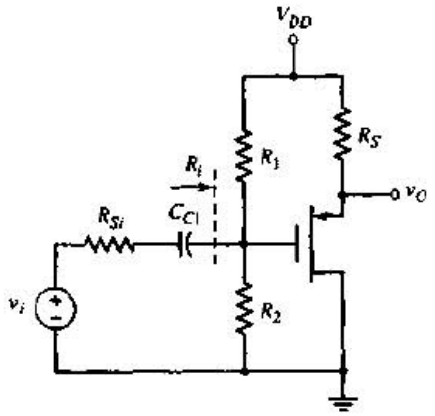

Figure 6.30 PMOS source follower

Solution: From the dc analysis, we have

$$V_{DD} = V_{SDQ} + I_{DQ}R_S$$

or

$$20 = 10 + 2.5R_S$$

The required source resistance value is therefore

$$R_S = 4\,\text{k}\Omega$$

The small-signal voltage gain of this circuit is the same as that of a source follower using an NMOS device. From Equation (6.33(a)), we have

$$A_v = \frac{V_o}{V_i} = \frac{g_m R_S}{1 + g_m R_S} \cdot \left(\frac{R_i}{R_i + R_{Si}}\right)$$

or

$$0.90 = \frac{g_m(4)}{1 + g_m(4)} \cdot \left(\frac{50}{50 + 4}\right)$$

which yields

$$0.972 = \frac{g_m(4)}{1 + g_m(4)}$$

Therefore, the required small-signal transconductance is

$$g_m = 8.68\,\text{mA/V}$$

Since the transconductance can be written as

$$g_m = 2\sqrt{K_p I_{DQ}}$$

we have

$$8.68 \times 10^{-3} = 2\sqrt{K_p(2.5 \times 10^{-3})}$$

which yields

$$K_p = 7.53 \times 10^{-3}\ \text{A/V}^2$$

The conduction parameter, which is a function of the width-to-length ratio, is

$$K_p = 7.53 \times 10^{-3} = \left(\frac{W}{L}\right)\left(\frac{1}{2}k_p'\right) = \left(\frac{W}{L}\right)\left(\frac{40 \times 10^{-6}}{2}\right)$$

which means that the width-to-length ratio is

$$\frac{W}{L} = 377$$

This is a relatively large p-channel transistor.

Completing the dc analysis, we have

$$I_{DQ} = K_p(V_{SGQ} + V_{TP})^2$$

or

$$2.5 = 7.53(V_{SGQ} - 2)^2$$

which yields a quiescent source-to-gate voltage of

$$V_{SGQ} = 2.58\ \text{V}$$

The quiescent source-to-gate voltage can also be written as

$$V_{SGQ} = (V_{DD} - I_{DQ}R_S) - \left(\frac{R_2}{R_1 + R_2}\right)(V_{DD})$$

Since

$$\left(\frac{R_2}{R_1 + R_2}\right) = \left(\frac{1}{R_1}\right)\left(\frac{R_1 R_2}{R_1 + R_2}\right) = \left(\frac{1}{R_1}\right)R_i$$

we have

$$2.58 = [20 - (2.5)(4)] - \left(\frac{1}{R_1}\right)(50)(20)$$

the bias resistor R_1 is then found to be

$$R_1 = 135\ \text{k}\Omega$$

Since

$$R_i = R_1 \| R_2 = 50\ \text{k}\Omega$$

then

$$R_2 = 79.4\ \text{k}\Omega$$

Comment: In order to achieve the desired specifications, a relatively large transconductance is required, which means that a large transistor is needed. If the load effect were reduced, that is, if R_i were made larger, the required size of the transistor could be reduced.

6.4.2 Input and Output Impedance

The input resistance R_i as defined in Figure 6.29(b), for example, is the Thevenin equivalent resistance of the bias resistors. Even though the input resistance to the gate of the MOSFET is essentially infinite, the input bias resistances do provide a loading effect. This same effect was seen in the common-source circuits.

To calculate the output resistance, we set all independent small-signal sources equal to zero, apply a test voltage to the output terminals, and measure a test current. Figure 6.31 shows the circuit we will use to determine the output resistance of the source follower shown in Figure 6.28. We set $V_i = 0$ and apply a test voltage V_x. Since there are no capacitances in the circuit, the output impedance is simply an output resistance, which is defined as

$$R_o = \frac{V_x}{I_x} \tag{6.34}$$

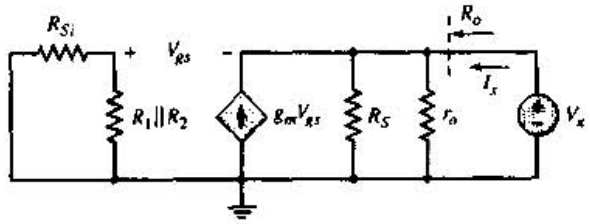

Figure 6.31 Equivalent circuit of NMOS source follower, for determining output resistance

Writing a KCL equation at the output source terminal produces

$$I_x + g_m V_{gs} = \frac{V_x}{R_S} + \frac{V_x}{r_o} \tag{6.35}$$

Since there is no current in the input portion of the circuit, we see that $V_{gs} = -V_x$. Therefore, Equation (6.35) becomes

$$I_x = V_x\left(g_m + \frac{1}{R_S} + \frac{1}{r_o}\right) \tag{6.36(a)}$$

or

$$\frac{I_x}{V_x} = \frac{1}{R_o} = g_m + \frac{1}{R_S} + \frac{1}{r_o} \tag{6.36(b)}$$

The output resistance is then

$$R_o = \frac{1}{g_m} \| R_S \| r_o \tag{6.37}$$

From Figure 6.31, we see that the voltage V_{gs} is directly across the current source $g_m V_{gs}$. This means that the effective resistance of the device is $1/g_m$. The output resistance given by Equation (6.37) can therefore be written directly. This result also means that the resistance looking into the source terminal (ignoring r_o) is $1/g_m$, as previously noted.

Example 6.9 **Objective:** Calculate the output resistance of a source-follower circuit.

Consider the circuit shown in Figure 6.28 with circuit and transistor parameters given in Example 6.7.

Solution: The results of Example 6.7 are: $R_S = 0.75\,\text{k}\Omega$, $r_o = 12.5\,\text{k}\Omega$, and $g_m = 11.3\,\text{mA/V}$. Using Figure 6.31 and Equation (6.37), we find

$$R_o = \frac{1}{g_m} \| R_S \| r_o = \frac{1}{11.3} \| 0.75 \| 12.5$$

or

$$R_o = 0.0787\,\text{k}\Omega = 78.7\,\Omega$$

Comment: The output resistance of a source-follower circuit is dominated by the transconductance parameter. Also, because the output resistance is very low, the source follower tends to act like an ideal voltage source, which means that the output can drive another circuit without significant loading effects.

Test Your Understanding

***6.17** Consider the circuit shown in Figure 6.30 with circuit parameters $V_{DD} = 5\,\text{V}$, $R_S = 5\,\text{k}\Omega$, $R_1 = 70.7\,\text{k}\Omega$, $R_2 = 9.3\,\text{k}\Omega$, and $R_{Si} = 500\,\Omega$. The transistor parameters are: $V_{TP} = -0.8\,\text{V}$, $K_p = 0.4\,\text{mA/V}^2$, and $\lambda = 0$. Calculate the small-signal voltage gain $A_v = v_o/v_i$ and the output resistance R_o seen looking back into the circuit. (Ans. $A_v = 0.817$, $R_o = 0.915\,\text{k}\Omega$)

D6.18 The transistor in the source-follower circuit shown in Figure 6.32 is biased with a constant current source. The transistor parameters are: $V_{TN} = 2\,\text{V}$, $k_n' = 40\,\mu\text{A/V}^2$, and $\lambda = 0.01\,\text{V}^{-1}$. The load resistor is $R_L = 4\,\text{k}\Omega$. (a) Design the transistor width-to-length ratio such that $g_m = 2\,\text{mA/V}$ when $I = 0.8\,\text{mA}$. What is the corresponding value for V_{GS}? (b) Determine the small-signal voltage gain and the output resistance R_o. (Ans. (a) $W/L = 62.5$, $V_{GS} = 2.8\,\text{V}$; (b) $A_v = 0.886$, $R_o \cong 0.5\,\text{k}\Omega$)

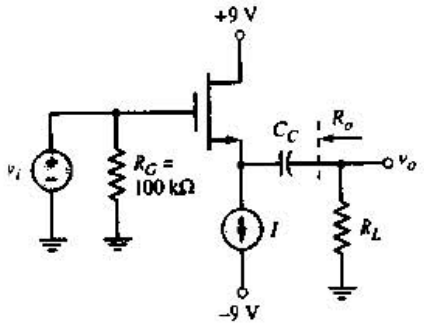

Figure 6.32 Figure for Exercise 6.18

***D6.19** The parameters of the transistor in the source-follower circuit shown in Figure 6.33 are: $V_{TP} = -2\,\text{V}$, $K_p = 2\,\text{mA/V}^2$, and $\lambda = 0.02\,\text{V}^{-1}$. Design the circuit such that $I_{DQ} = 3\,\text{mA}$. Determine the open-circuit ($R_L = \infty$) small-signal voltage gain. What

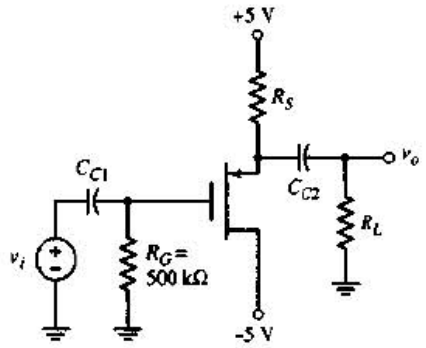

Figure 6.33 Figure for Exercise 6.19

value of R_L will result in a 10 percent reduction in the gain? (Ans. $R_S = 0.593\,\text{k}\Omega$, $A_v = 0.737$, $R_L = 1.35\,\text{k}\Omega$)

6.5 THE COMMON-GATE CONFIGURATION

The third amplifier configuration is the **common-gate circuit**. To determine the small-signal voltage and current gains, and the input and output impedances, we will use the same small-signal equivalent circuit for the transistor that was used previously. The dc analysis of the common-gate circuit is the same as that of previous MOSFET circuits.

6.5.1 Small-Signal Voltage and Current Gains

In the common-gate configuration, the input signal is applied to the source terminal and the gate is at signal ground. The common-gate configuration shown in Figure 6.34 is biased with a constant-current source I_Q. The gate resistor R_G prevents the buildup of static charge on the gate terminal, and the capacitor C_G ensures that the gate is at signal ground. The coupling capacitor C_{C1} couples the signal to the source, and coupling capacitor C_{C2} couples the output voltage to load resistance R_L.

The small-signal equivalent circuit is shown in Figure 6.35. The small-signal transistor resistance r_o is assumed to be infinite. The output voltage is

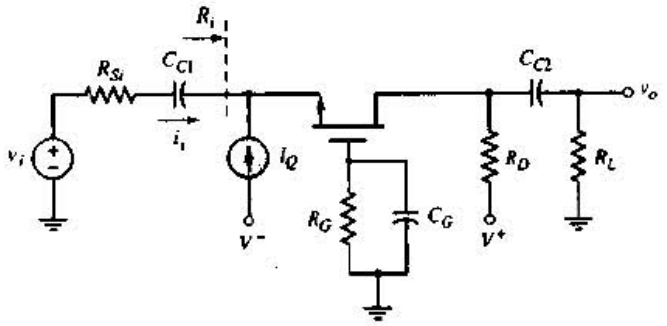

Figure 6.34 Common-gate circuit

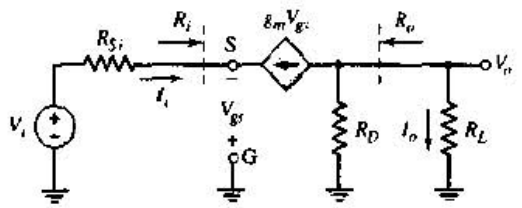

Figure 6.35 Small-signal equivalent circuit of common-gate amplifier

$$V_o = -(g_m V_{gs})(R_D \| R_L) \tag{6.38}$$

Writing the KVL equation around the input, we find

$$V_i = I_i R_{Si} - V_{gs} \tag{6.39}$$

where $I_i = -g_m V_{gs}$. The gate-to-source voltage can then be written as

$$V_{gs} = \frac{-V_i}{1 + g_m R_{Si}} \tag{6.40}$$

The small-signal voltage gain is found to be

$$A_v = \frac{V_o}{V_i} = \frac{g_m(R_D \| R_L)}{1 + g_m R_{Si}} \tag{6.41}$$

Also, since the voltage gain is positive. the output and input signals are in phase.

In many cases, the signal input to a common-gate circuit is a current. Figure 6.36 shows the small-signal equivalent common-gate circuit with a Norton equivalent circuit as the signal source. We can calculate a current gain. The output current I_o can be written

$$I_o = \left(\frac{R_D}{R_D + R_L}\right)(-g_m V_{gs}) \tag{6.42}$$

At the input we have

$$I_i + g_m V_{gs} + \frac{V_{gs}}{R_{Si}} = 0 \tag{6.43}$$

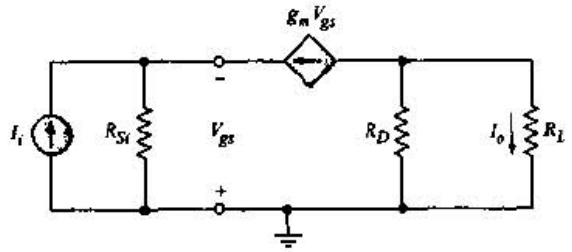

Figure 6.36 Small-signal equivalent circuit of common-gate amplifier with a Norton equivalent signal source

or

$$V_{gs} = -I_i\left(\frac{R_{Si}}{1 + g_m R_{Si}}\right) \tag{6.44}$$

The small-signal current gain is then

$$A_i = \frac{I_o}{I_i} = \left(\frac{R_D}{R_D + R_L}\right) \cdot \left(\frac{g_m R_{Si}}{1 + g_m R_{Si}}\right) \tag{6.45}$$

We may note that if $R_D \gg R_L$ and $g_m R_{Si} \gg 1$, then the current gain is essentially unity as it is for an ideal BJT common-base circuit.

6.5.2 Input and Output Impedance

In contrast to the common-source and source-follower amplifiers, the common-gate circuit has a low input resistance because of the transistor. However, if the input signal is a current, a low input resistance is an advantage. The input resistance is defined as

$$R_i = \frac{-V_{gs}}{I_i} \tag{6.46}$$

Since $I_i = -g_m V_{gs}$, the input resistance is

$$R_i = \frac{1}{g_m} \tag{6.47}$$

This result has been obtained previously.

We can find the output resistance by setting the input signal voltage equal to zero. From Figure 6.35, we see that $V_{gs} = -g_m V_{gs} R_{Si}$, which means that $V_{gs} = 0$. Consequently, $g_m V_{gs} = 0$. The output resistance, looking back from the load resistance, is therefore

$$R_o = R_D \tag{6.48}$$

Example 6.10 **Objective:** For the common-gate circuit, determine the output voltage for a given input current.

For the circuits shown in Figures 6.34 and 6.36, the circuit parameters are: $I_Q = 1\,\text{mA}$, $V^+ = 5\,\text{V}$, $V^- = -5\,\text{V}$, $R_G = 100\,\text{k}\Omega$, $R_D = 4\,\text{k}\Omega$, and $R_L = 10\,\text{k}\Omega$. The transistor parameters are: $V_{TN} = 1\,\text{V}$, $K_n = 1\,\text{mA/V}^2$, and $\lambda = 0$. Assume the input current is $100\sin\omega t\,\mu\text{A}$ and assume $R_{Si} = 50\,\text{k}\Omega$.

Solution: The quiescent gate-to-source voltage is determined from

$$I_Q = I_{DQ} = K_n(V_{GSQ} - V_{TN})^2$$

or

$$1 = 1(V_{GSQ} - 1)^2$$

which yields

$$V_{GSQ} = 2\,\text{V}$$

The small-signal transconductance is

$$g_m = 2K_n(V_{GSQ} - V_{TN}) = 2(1)(2 - 1) = 2\,\text{mA/V}$$

From Equation (6.45), we can write the output current as

$$I_o = I_i\left(\frac{R_D}{R_D + R_L}\right) \cdot \left(\frac{g_m R_{Si}}{1 + g_m R_{Si}}\right)$$

The output voltage is $V_o = I_o R_L$, so we find

$$V_o = I_i\left(\frac{R_L R_D}{R_D + R_L}\right) \cdot \left(\frac{g_m R_{Si}}{1 + g_m R_{Si}}\right)$$

$$= \left[\frac{(10)(4)}{4 + 10}\right] \cdot \left[\frac{(2)(50)}{1 + (2)(50)}\right] \cdot (0.1)\sin\omega t$$

or

$$V_o = 0.283\sin\omega t\,\text{V}$$

Comment: As with the BJT common-base circuit, the MOSFET common-gate amplifier is useful if the input signal is a current.

Test Your Understanding

RD6.20 For the circuit shown in Figure 6.34, the circuit parameters are: $V^+ = 5\,\text{V}$, $V^- = -5\,\text{V}$, $R_G = 100\,\text{k}\Omega$, $R_L = 4\,\text{k}\Omega$, and $I_Q = 0.5\,\text{mA}$. The transistor parameters are $V_{TN} = 1\,\text{V}$ and $\lambda = 0$. The circuit is driven by a signal current source I_i. Redesign R_D and g_m such that the transfer function V_o/I_i is $2.4\,\text{k}\Omega$ and the output resistance is $R_i = 350\,\Omega$. Determine V_{GSQ} and show that the transistor is biased in the saturation region. (Ans. $g_m = 2.86\,\text{mA/V}$, $R_D = 6\,\text{k}\Omega$, $V_{GSQ} = 1.35\,\text{V}$)

6.21 Consider the circuit shown in Figure 6.37 with circuit parameters $V^+ = 5\,\text{V}$, $V^- = -5\,\text{V}$, $R_S = 4\,\text{k}\Omega$, $R_D = 2\,\text{k}\Omega$, $R_L = 4\,\text{k}\Omega$ and $R_G = 50\,\text{k}\Omega$. The transistor parameters are: $K_p = 1\,\text{mA/V}^2$, $V_{TP} = -0.8\,\text{V}$, and $\lambda = 0$. Draw the small-signal equivalent circuit, determine the small-signal voltage gain $A_v = V_o/V_i$, and find the input resistance R_i. (Ans. $A_v = 2.41$, $R_i = 0.485\,\text{k}\Omega$)

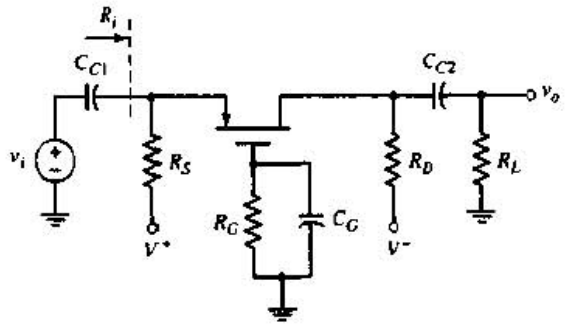

Figure 6.37 Figure for Exercise 6.21

6.6 THE THREE BASIC AMPLIFIER CONFIGURATIONS: SUMMARY AND COMPARISON

Table 6.1 is a summary of the small-signal characteristics of the three amplifier configurations.

Table 6.1 Characteristics of the three MOSFET amplifier configurations

Configuration	Voltage gain	Current gain	Input resistance	Output resistance
Common source	$A_v > 1$	—	R_{TH}	Moderate to high
Source follower	$A_v \cong 1$	—	R_{TH}	Low
Common gate	$A_v > 1$	$A_i \cong 1$	Low	Moderate to high

The common-source amplifier voltage gain is generally greater than 1. The voltage gain of the source follower is slightly less than1, and that of the common-gate circuit is generally greater than 1.

The input resistance looking directly into the gate of the common-source and source-follower circuits is essentially infinite at low to moderate signal frequencies. However, the input resistance of these discrete amplifiers is the Thevenin equivalent resistance R_{TH} of the bias resistors. In contrast, the input resistance to the common-gate circuit is generally in the range of only a few hundred ohms.

The output resistance of the source follower is generally in the range of a few hundred ohms or less. The output resistance of the common-source and common-gate configurations is dominated by the resistance R_D. In Chapters 10 and 11, we will see that the output resistance of these configurations is dominated by the resistance r_o when transistors are used as load devices in ICs.

The specific characteristics of these single-stage amplifiers are used in the design of multistage amplifiers.

6.7 SINGLE-STAGE INTEGRATED CIRCUIT MOSFET AMPLIFIERS

In the last chapter, we considered three all-MOSFET inverters and plotted the voltage transfer characteristics. All three inverters use an n-channel enhancement-mode driver transistor. The three types of load devices are an n-channel enhancement-mode device, an n-channel depletion-mode device, and a p-channel enhancement-mode device. The MOS transistor used as a load device is referred to as an **active load**. We mentioned that these three circuits can be used as amplifiers.

In this section, we revisit these three circuits and consider their amplifier characteristics. We will emphasize the small-signal equivalent circuits. This section serves as an introduction to more advanced MOS integrated circuit amplifier designs considered in Part II of the text.

6.7.1 NMOS Amplifiers with Enhancement Load

The characteristics of an n-channel enhancement load device were presented in the last chapter. Figure 6.38(a) shows an NMOS enhancement load transistor,

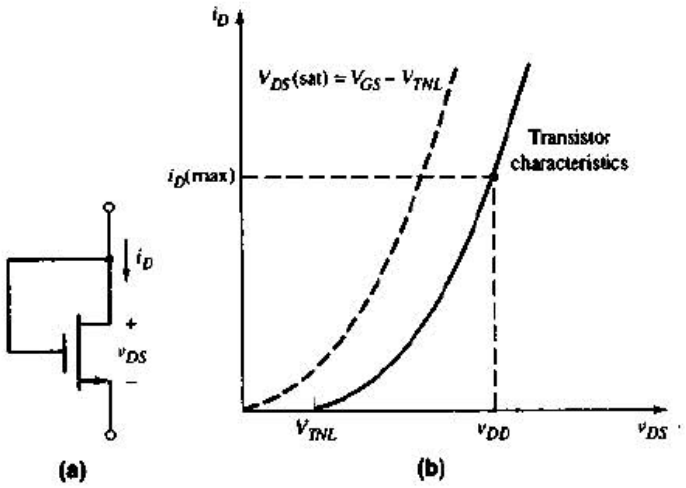

Figure 6.38 (a) NMOS enhancement-mode transistor with gate and drain connected in a load device configuration and (b) current–voltage characteristics of NMOS enhancement load transistor

and Figure 6.38(b) shows the current–voltage characteristics. The threshold voltage is V_{TNL}.

Figure 6.39(a) shows an NMOS amplifier with enhancement load. The driver transistor is M_D and the load transistor is M_L. The characteristics of transistor M_D and the load curve are shown in Figure 6.39(b). The load curve is essentially the mirror image of the i–v characteristic of the load device. Since the i–v characteristics of the load device are nonlinear, the load curve is also nonlinear. The load curve intersects the voltage axis at $V_{DD} - V_{TNL}$, which is the point where the current in the enhancement load device goes to zero. The transition point is also shown on the curve.

The voltage transfer characteristic is also useful in visualizing the operation of the amplifier. This curve is shown in Figure 6.39(c). When the enhancement-mode driver first begins to conduct, it is biased in the saturation region. For use as an amplifier, the circuit Q-point should be in this region, as shown in both Figures 6.39(b) and (c).

We can now apply the small-signal equivalent circuits to find the voltage gain. In the discussion of the source follower, we found that the equivalent resistance looking into the source terminal (with $R_S = \infty$) was $R_o = (1/g_m) \| r_o$. The small-signal equivalent circuit of the inverter is given in Figure 6.40, where the subscripts D and L refer to the driver and load transistors, respectively. We are again neglecting the body effect of the load transistor.

The small-signal voltage gain is then

$$A_v = \frac{V_o}{V_i} = -g_{mD}\left(r_{oD} \left\| \frac{1}{g_{mL}} \right\| r_{oL}\right) \tag{6.49}$$

Since, generally, $1/g_{mL} \ll r_{oL}$ and $1/g_{mD} \ll r_{oD}$, the voltage gain, to a good approximation is given by

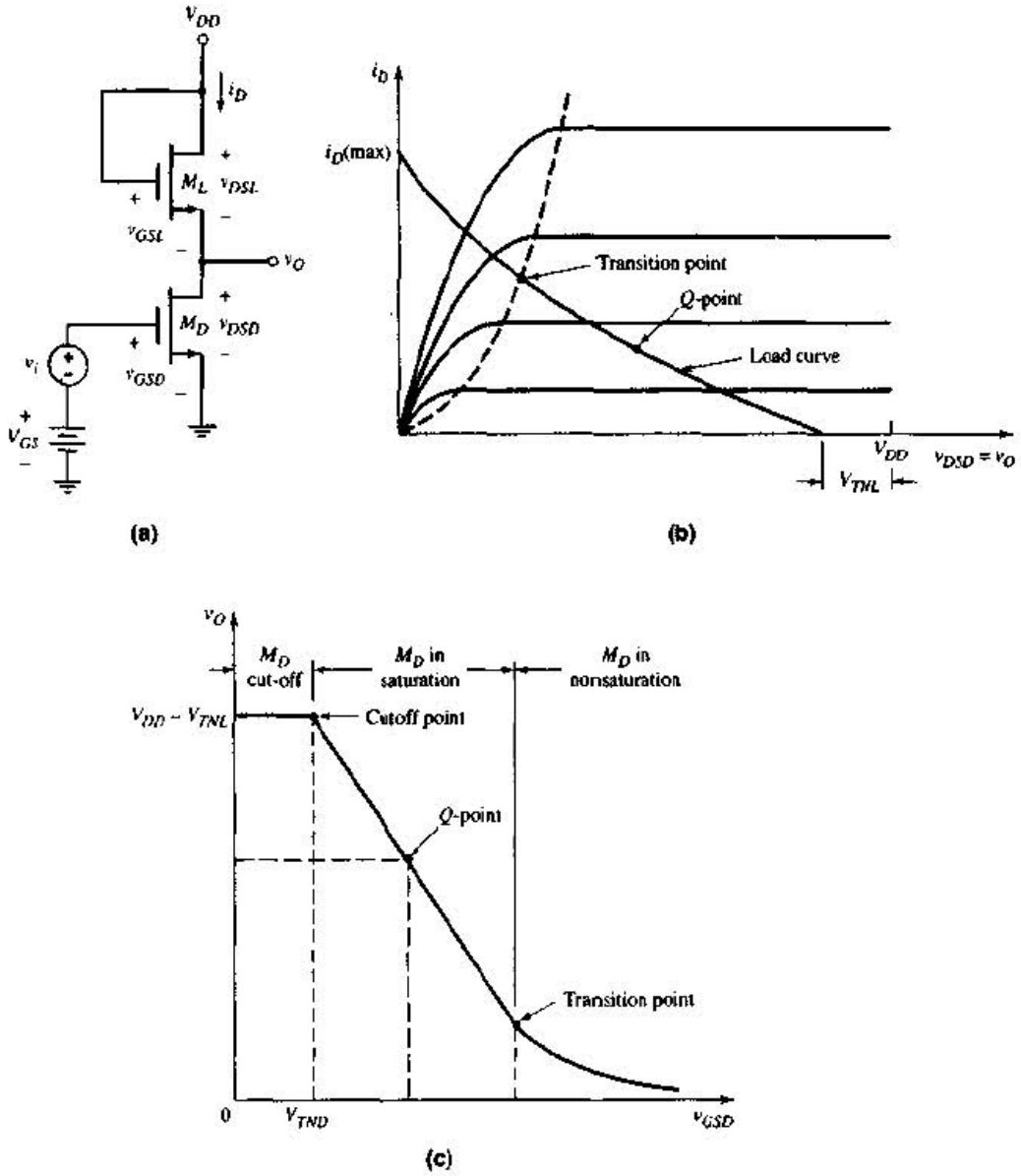

Figure 6.39 (a) NMOS amplifier with enhancement load device; (b) driver transistor characteristics and enhancement load curve with transition point; and (c) voltage transfer characteristics of NMOS amplifier with enhancement load device

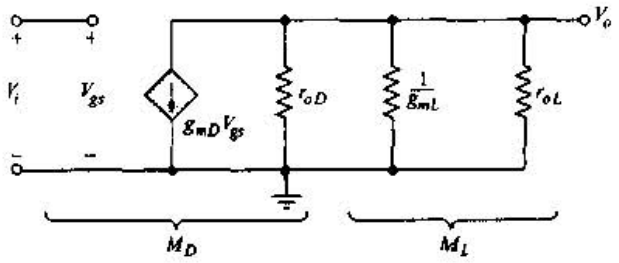

Figure 6.40 Small-signal equivalent circuit of NMOS inverter with enhancement load device

$$A_v = \frac{-g_{mD}}{g_{mL}} = -\sqrt{\frac{K_{nD}}{K_{nL}}} = -\sqrt{\frac{(W/L)_D}{(W/L)_L}} \tag{6.50}$$

The voltage gain, then, is related to the size of the two transistors.

Design Example 6.11 **Objective:** Design the small-signal voltage gain of an NMOS amplifier with enhancement load, and establish the Q-point in the middle of the saturation region.

Consider the circuit shown in Figure 6.39(a) with transistor parameters $V_{TND} = V_{TNL} = 1\,\text{V}$, $k_n' = 30\,\mu\text{A/V}^2$, and $(W/L)_L = 1$. The circuit parameter is $V_{DD} = 5\,\text{V}$.

Design the circuit such that the voltage gain is $|A_v| = 10$.

Solution: From Equation (6.50), we have

$$|A_v| = 10 = \sqrt{\frac{(W/L)_D}{(W/L)_L}}$$

Therefore, the width-to-length ratio of the driver transistor must be

$$\left(\frac{W}{L}\right)_D = (10)^2\left(\frac{W}{L}\right)_L = (100)(1) = 100$$

The conduction parameters are then

$$K_{nD} = \left(\frac{W}{L}\right)_D\left(\frac{1}{2}k_n'\right) = (100)(15) \Rightarrow 1.5\,\text{mA/V}^2$$

and

$$K_{nL} = \left(\frac{W}{L}\right)_L\left(\frac{1}{2}k_n'\right) = (1)(15) \Rightarrow 0.015\,\text{mA/V}^2$$

We can determine the transition point by setting

$$v_O = v_{GSD} - V_{TND}$$

Therefore,

$$v_{GSD} - V_{TND} = (V_{DD} - V_{TNL}) - \sqrt{\frac{K_{nD}}{K_{nL}}}(v_{GSD} - V_{TND})$$

or

$$v_{GSD} - 1 = (5 - 1) - \sqrt{\frac{1.5}{0.015}}(v_{GSD} - 1)$$

which yields transition point values of

$$v_{GSD} = 1.36\,\text{V} \quad \text{and} \quad v_{DSD} = 0.36\,\text{V}$$

Considering the resulting voltage transfer characteristics shown in Figure 6.41, the middle of the saturation region is halfway between the cutoff point ($v_{GSD} = V_{TND} = 1$ V) and the transition point ($v_{GSD} = 1.36$ V), or

$$V_{GSQ} = 1.18 \text{ V}$$

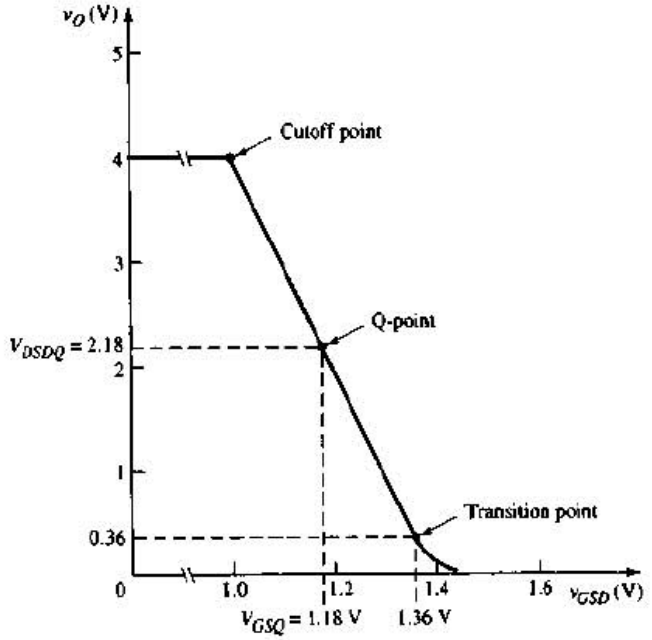

Figure 6.41 Voltage transfer characteristics and *Q*-point of NMOS amplifier with enhancement load, for Example 6.11

Comment: These results show that a very large difference is required in the sizes of the two transistors to produce a gain of 10. In fact, a gain of 10 is about the largest practical gain that can be produced by an enhancement load device. A larger small-signal gain can be obtained by using a depletion-mode MOSFET as a load device, as shown in the next section.

Design Pointer: The body effect of the load transistor was neglected in this analysis. The body effect will actually lower the small-signal voltage gain from that determined in the example.

Test Your Understanding

6.22 For the enhancement load amplifier shown in figure 6.39(a), the parameters are: $V_{TND} = V_{TNL} = 0.8$ V, $k_n' = 40\,\mu\text{A/V}^2$, $(W/L)_D = 80$, $(W/L)_L = 1$, and $V_{DD} = 5$ V. Determine the small-signal voltage gain. Determine V_{GS} such that the *Q*-point is in the middle of the saturation region. (Ans. $A_v = -8.94$, $V_{GS} = 1.01$ V)

D6.23 For the enhancement load amplifier shown in Figure 6.39(a), the parameters are: $V_{TND} = V_{TNL} = 1$ V, $k_n' = 30\,\mu\text{A/V}^2$, $(W/L)_L = 2$, and $V_{DD} = 10$ V. Design the circuit such that the small-signal voltage gain is $|A_v| = 6$ and the *Q*-point is in the center of the saturation region. (Ans. $(W/L)_D = 72$, $V_{GS} = 1.645$ V)

6.7.2 NMOS Amplifier with Depletion Load

Figure 6.42(a) shows the NMOS depletion-mode transistor connected as a load device and Figure 6.42(b) shows the current–voltage characteristics. The transition point is also indicated. The threshold voltage V_{TNL} of this device is negative, which means that the v_{DS} value at the transition point is positive. Also, the slope of the curve in the saturation region is not zero; therefore, a finite resistance r_o exists in this region.

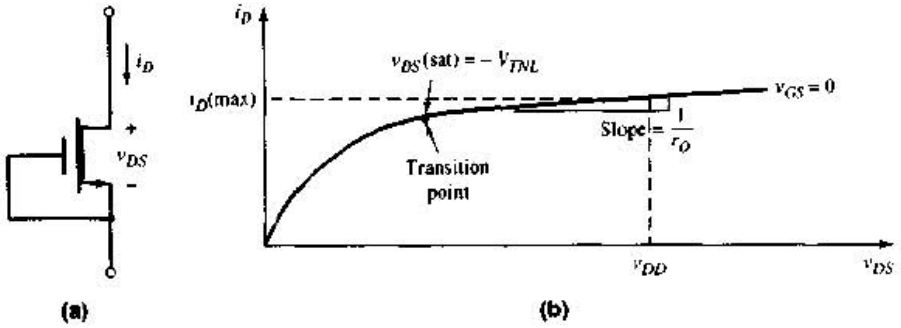

Figure 6.42 (a) NMOS depletion-mode transistor with gate and source connected in a load device configuration and (b) current–voltage characteristic of NMOS depletion load transistor

Figure 6.43(a) shows an **NMOS depletion load amplifier**. The transistor characteristics of M_D and the load curve for the circuit are shown in Figure 6.43(b). The load curve, again, is the mirror image of the i–v characteristic of the load device. Since the i–v characteristics of the load device are nonlinear, the load curve is also nonlinear. The transition points for both M_D and M_L are also indicated. Point A is the transition point for M_D, and point B is the transition point for M_L. The Q-point should be approximately midway between the two transition points.

The dc voltage V_{GSDQ} biases transistor M_D in the saturation region at the Q-point. The signal voltage v_i superimposes a sinuosoidal gate-to-source voltage on the dc value, and the bias point moves along the load curve about the Q-point. Again, both M_D and M_L must be biased in their saturation regions at all times.

The voltage transfer characteristic of this circuit is shown in Figure 6.43(c). Region III corresponds to the condition in which both transistors are biased in the saturation region. The desired Q-point is indicated.

We can again apply the small-signal equivalent circuit to find the small-signal voltage gain. Since the gate-to-source voltage of the depletion-load device is held at zero, the equivalent resistance looking into the source terminal is $R_o = r_o$. The small-signal equivalent circuit of the inverter is given in Figure 6.44, where the subscripts D and L refer to the driver and load transistors, respectively. We are again neglecting the body effect of the load device.

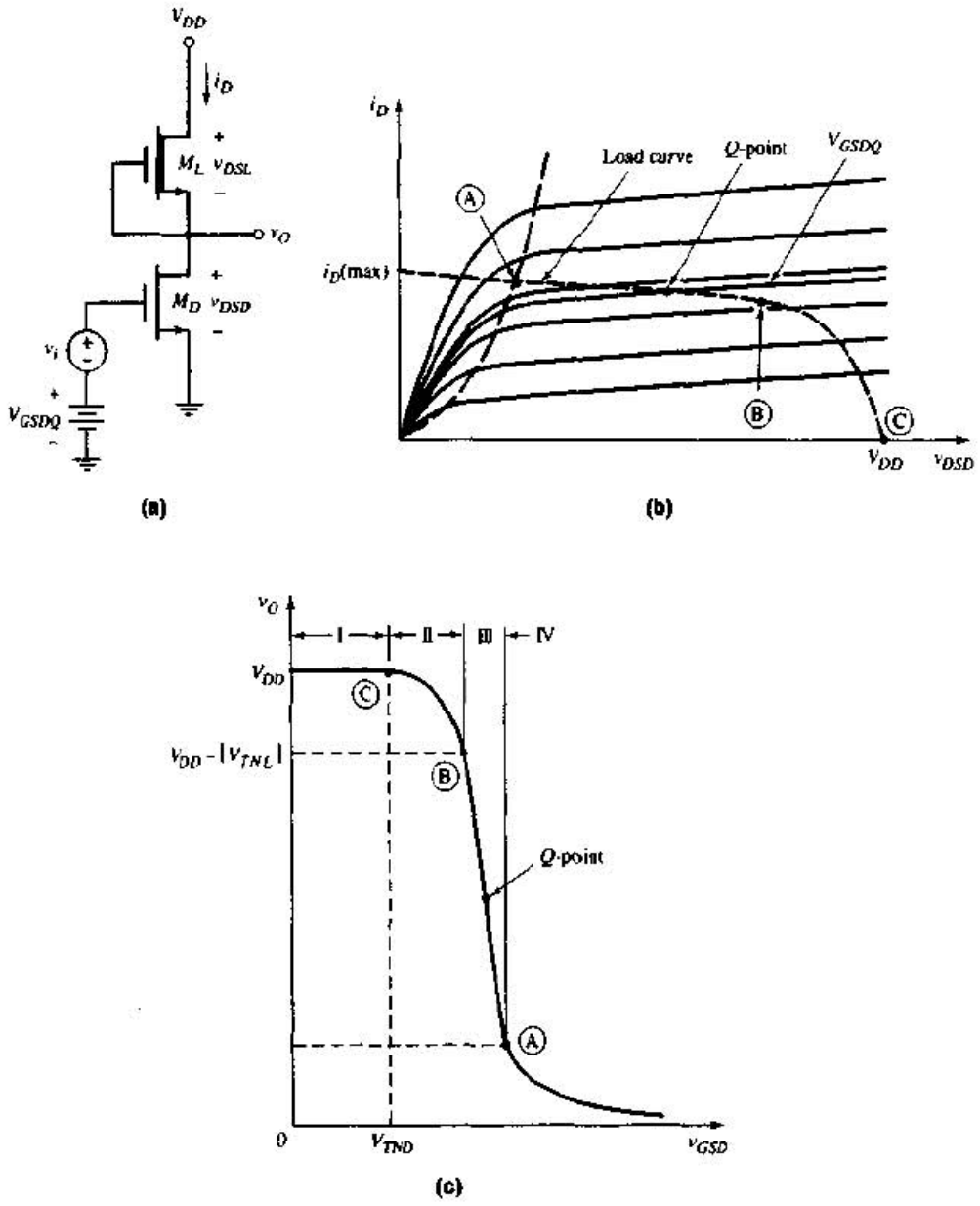

Figure 6.43 (a) NMOS amplifier with depletion load device; (b) driver transistor characteristics and depletion load curve, with transition points; and (c) voltage transfer characteristics

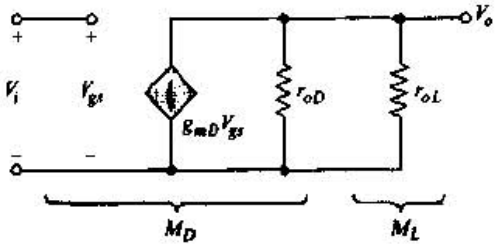

Figure 6.44 Small-signal equivalent circuit of NMOS inverter with depletion load device

The small-signal voltage gain is then

$$A_v = \frac{V_o}{V_i} = -g_{mD}(r_{oD} \| r_{oL}) \tag{6.51}$$

In this circuit, the voltage gain is directly proportional to the output resistances of the two transistors.

Example 6.12 **Objective:** Determine the small-signal voltage gain of the NMOS amplifier with depletion load.

For the circuit shown in Figure 6.43(a), assume transistor parameters of $V_{TND} = +0.8\,\text{V}$, $V_{TNL} = -1.5\,\text{V}$, $K_{nD} = 1\,\text{mA/V}^2$, $K_{nL} = 0.2\,\text{mA/V}^2$, and $\lambda_D = \lambda_L = 0.01\,\text{V}^{-1}$. Assume the transistors are biased at $I_{DQ} = 0.2\,\text{mA}$.

Solution: The transconductance of the driver is

$$g_{mD} = 2\sqrt{K_{nD} I_{DQ}} = 2\sqrt{(1)(0.2)} = 0.894\,\text{mA/V}$$

Since $\lambda_D = \lambda_L$, the output resistances are

$$r_{oD} = r_{oL} = \frac{1}{\lambda I_{DQ}} = \frac{1}{(0.01)(0.2)} = 500\,\text{k}\Omega$$

The small-signal voltage gain is then

$$A_v = -g_{mD}(r_{oD} \| r_{oL}) = -(0.894)(500 \| 500) = -224$$

Comment: The voltage gain of the NMOS amplifier with depletion load is, in general, significantly larger than that with the enhancement load device. The body effect will lower the ideal gain factor.

Discussion: One aspect of this circuit design that we have not emphasized is the dc biasing. We mentioned that both transistors need to be biased in their saturation regions. From Figure 6.43(a), this dc biasing is accomplished with the dc source V_{GSDQ}. However, because of the steep slope of the transfer characteristics (Figure 6.43(c)), applying the "correct" voltage becomes difficult. As we will see in the next section, dc biasing is generally accomplished with current source biasing.

Test Your Understanding

***6.24** For the depletion load amplifier in Figure 6.43(a), the parameters are: $V_{TND} = 0.8\,\text{V}$, $V_{TNL} = -1.2\,\text{V}$, $K_{nD} = 250\,\mu\text{A/V}^2$, $K_{nL} = 25\,\mu\text{A/V}^2$, $\lambda_D = \lambda_L = 0.01\,\text{V}^{-1}$, and $V_{DD} = 5\,\text{V}$. (a) Determine V_{GS} such that the Q-point is in the middle of the saturation region. (b) Calculate the quiescent drain current. (c) Determine the small-signal voltage gain. (Ans. (a) $V_{GS} = 1.18\,\text{V}$; (b) $I_{DQ} = 37\,\mu\text{A}$; (c) $A_v = -257$)

6.7.3 NMOS Amplifier with PMOS Load

Common-Source Amplifier

An amplifier using an n-channel enhancement-mode driver and a p-channel enhancement mode active load is shown in Figure 6.45(a) in a common-source configuration. The p-channel active load transistor M_2 is biased from M_3 and I_{Bias}. This configuration is similar to the MOSFET current source shown in Figure 5.39 in Chapter 5. With both n- and p-channel transistors in the same circuit, this circuit is now referred to as a CMOS amplifier.

The i–v characteristic curve for M_2 is shown in Figure 6.45(b). The source-to-gate voltage is a constant and is established by M_3. The driver transistor characteristics and the load curve are shown in Figure 6.45(c). The transition points of both M_1 and M_2 are shown. Point A is the transition point for M_1 and point B is the transition point for M_2. The Q-point, to establish an amplifier, should be approximately halfway between points A and B, so that both transistors are biased in their saturation regions. The voltage transfer characteristics are shown in Figure 6.45(d). Shown on the curve are the same transition points A and B and the desired Q-point.

We again apply the small-signal equivalent circuits to find the small-signal voltage gain. With v_{SG2} held constant, the equivalent resistance looking into the

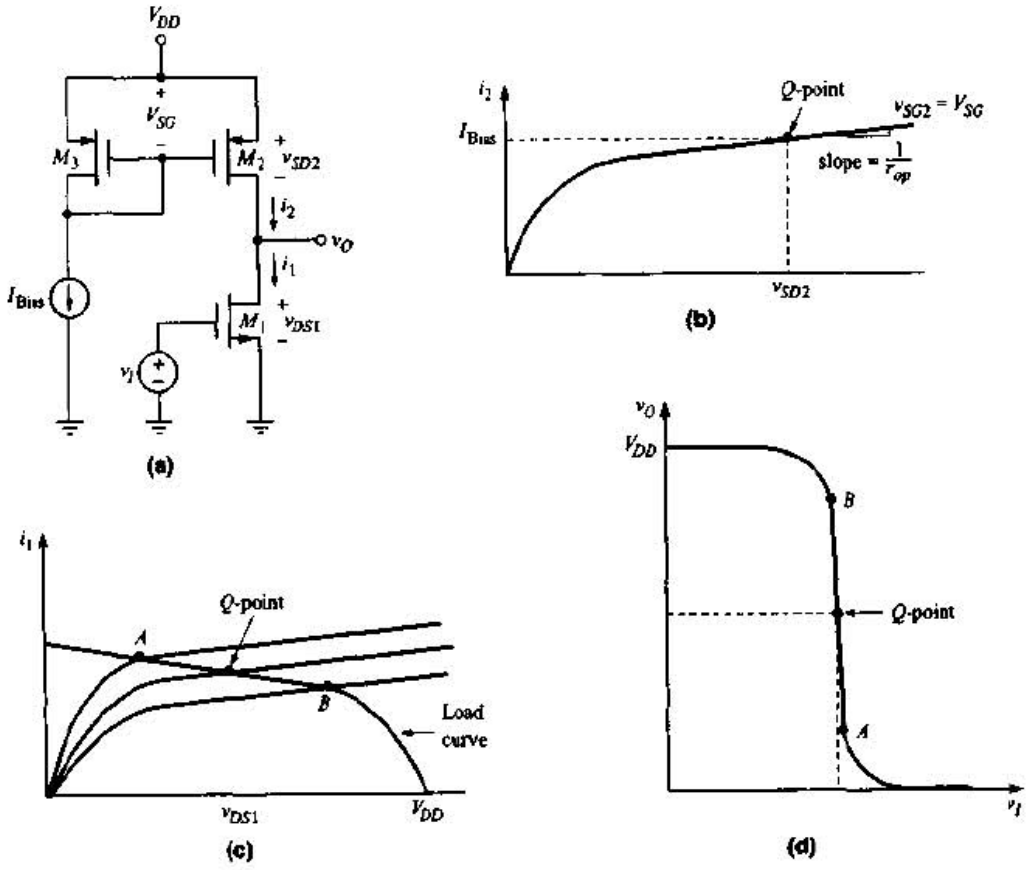

Figure 6.45 (a) CMOS common-source amplifier; (b) PMOS active load i–v characteristic, (c) driver transistor characteristics with load curve, (d) voltage transfer characteristics

drain of M_2 is just $R_o = r_{op}$. The small-signal equivalent circuit of the inverter is then as given in Figure 6.46. The subscripts n and p refer to the n-channel and p-channel transistors, respectively. We may note that the body terminal of M_1 will be tied to ground, which is the same as the source of M_1, and the body terminal of M_2 will be tied to V_{DD}, which is the same as the source of M_2. Hence, there is no body effect in this circuit.

The small-signal voltage gain is

$$A_v = \frac{V_o}{V_i} = -g_{mn}(r_{on} \| r_{op}) \tag{6.52}$$

Again for this circuit, the small-signal voltage gain is directly proportional to the output resistances of the two transistors.

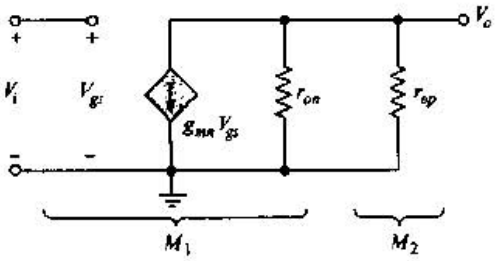

Figure 6.46 Small-signal equivalent circuit of the CMOS common-source amplifier

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Example 6.13 **Objective:** Determine the small-signal voltage gain of the CMOS amplifier.

For the circuit shown in Figure 6.45(a), assume transistor parameters of $V_{TN} = +0.8\,\text{V}$, $V_{TP} = -0.8\,\text{V}$, $k_n' = 80\,\mu\text{A/V}^2$, $k_p' = 40\,\mu\text{A/V}^2$, $(W/L)_n = 15$, $(W/L)_p = 30$, and $\lambda_n = \lambda_p = 0.01\,\text{V}^{-1}$. Also, assume $I_{\text{Bias}} = 0.2\,\text{mA}$.

Solution: The transconductance of the NMOS driver is

$$g_{mn} = 2\sqrt{K_n I_{DQ}} = 2\sqrt{\left(\frac{k_n'}{2}\right)\left(\frac{W}{L}\right)_n I_{\text{Bias}}}$$

$$= 2\sqrt{\left(\frac{0.08}{2}\right)(15)(0.2)} = 0.693\,\text{mA/V}$$

Since $\lambda_n = \lambda_p$, the output resistances are

$$r_{on} = r_{op} = \frac{1}{\lambda I_{DQ}} = \frac{1}{(0.01)(0.2)} = 500\,\text{k}\Omega$$

The small-signal voltage gain is then

$$A_v = -g_m(r_{on} \| r_{op}) = -(0.693)(500 \| 500) = -173$$

Comment: The voltage gain of the CMOS amplifier is on the same order of magnitude as the NMOS amplifier with depletion load. However, the CMOS amplifier does not suffer from the body effect.

Discussion: In the circuit configuration shown in Figure 6.45(a), we must again apply a dc voltage to the gate of M_1 to achieve the "proper" Q-point. We will show in later chapters using more sophisticated circuits how the Q-point is more easily established with current-source biasing. However, this circuit demonstrates the basic principles of the CMOS common-source amplifier.

CMOS Source-Follower and Common-Gate Amplifiers

The same basic CMOS circuit configuration can be used to form CMOS source-follower and common-gate configurations. Figure 6.47(a) and (b) show these circuits.

We see that for the source-follower circuit, the active load (M_2) is an n-channel rather than a p-channel device. The input is applied to the gate of M_1 and the output is at the source of M_1. For the common-gate amplifier, the active load (M_2) is again a p-channel device. The input is applied to the source of M_1 and the output is at the drain of M_1.

We may note that in both the source-follower and common-gate circuits, the body effect will need to be taken into account. In both circuits, the body terminal of the amplifying transistor M_1 will be connected to the most negative voltage, which is not the same as the source terminal. We will consider these types of circuits in detail in later chapters.

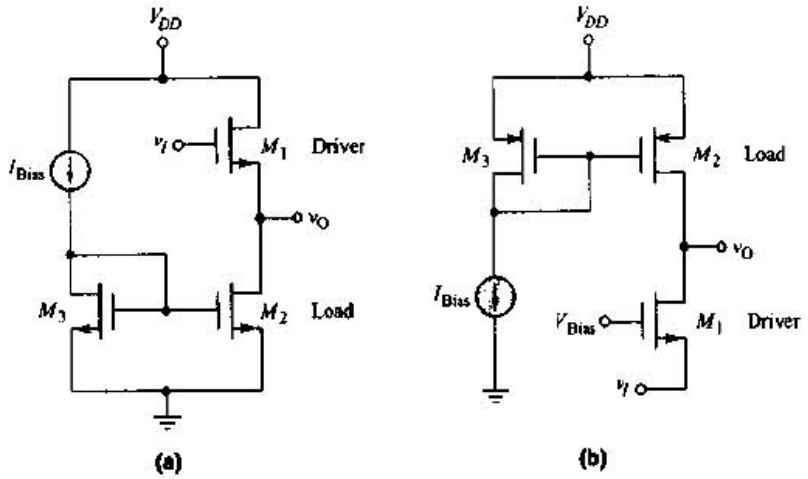

Figure 6.47 (a) CMOS source-follower amplifier; (b) CMOS common-gate amplifier

6.8 MULTISTAGE AMPLIFIERS

In most applications, a single-transistor amplifier will not be able to meet the combined specifications of a given amplification factor, input resistance, and output resistance. For example, the required voltage gain may exceed that which can be obtained in a single-transistor circuit.

Transistor amplifier circuits can be connected in series, or **cascaded**, as shown in Figure 6.48. This may be done either to increase the overall small-signal voltage gain, or provide an overall voltage gain greater than 1, with a very low output resistance. The overall voltage gain may not simply be the product of the individual amplification factors. Loading effects, in general, need to be taken into account.

There are many possible multistage configurations; we will examine a few here, in order to understand the type of analysis required.

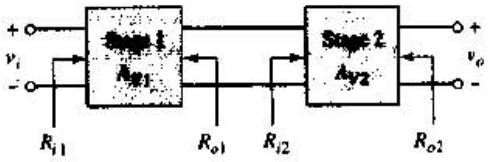

Figure 6.48 Generalized two-stage amplifier

6.8.1 DC Analysis

The circuit shown in Figure 6.49 is a cascade of a common-source amplifier followed by a source-follower amplifier. As shown previously, the common-source amplifier provides a small-signal voltage gain and the source follower has a low output impedance.

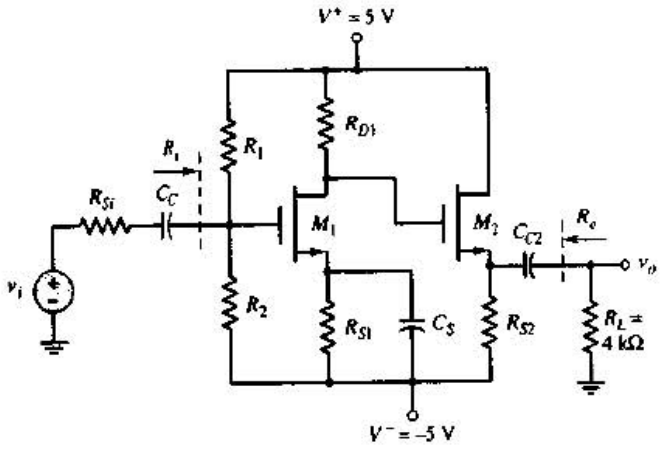

Figure 6.49 Common-source amplifier in cascade with source follower

Design Example 6.14 **Objective:** Design the biasing of a multistage MOSFET circuit to meet specific requirements.

Consider the circuit shown in Figure 6.49 with transistor parameters $K_{n1} = 500\,\mu A/V^2$, $K_{n2} = 200\,\mu A/V^2$, $V_{TN1} = V_{TN2} = 1.2\,V$, and $\lambda_1 = \lambda_2 = 0$. Design the circuit such that $I_{DQ1} = 0.2\,mA$, $I_{DQ2} = 0.5\,mA$, $V_{DSQ1} = V_{DSQ2} = 6\,V$, and $R_i = 100\,k\Omega$. Let $R_{S1} = 4\,k\Omega$.

Solution: For output transistor M_2, we have

$$V_{DSQ2} = 5 - (-5) - I_{DQ2}R_{S2}$$

or

$$6 = 10 - (0.5)R_{S2}$$

which yields $R_{S2} = 8\,k\Omega$. Also,

$$I_{DQ2} = K_{n2}(V_{GS2} - V_{TN2})^2$$

or

$$0.5 = 0.2(V_{GS2} - 1.2)^2$$

which yields

$$V_{GS2} = 2.78\,V$$

Since $V_{DSQ2} = 6\,V$, the source voltage of M_2 is $V_{S2} = -1\,V$. With $V_{GS2} = 2.78\,V$, the gate voltage on M_2 must be

$$V_{G2} = -1 + 2.78 = 1.78\,V$$

The resistor R_{D1} is then

$$R_{D1} = \frac{5 - 1.78}{0.2} = 16.1\,k\Omega$$

For $V_{DSQ1} = 6\,V$, the source voltage of M_1 is

$$V_{S1} = 1.78 - 6 = -4.22\,V$$

The resistor R_{S1} is then

$$R_{S1} = \frac{-4.22 - (-5)}{0.2} = 3.9\,k\Omega$$

For transistor M_1, we have

$$I_{DQ1} = K_{n1}(V_{GS1} - V_{TN1})^2$$

or

$$0.2 = 0.50(V_{GS1} - 1.2)^2$$

which yields

$$V_{GS1} = 1.83\,V$$

To find R_1 and R_2, we can write

$$V_{GS1} = \left(\frac{R_2}{R_1 + R_2}\right)(10) - I_{DQ1}R_{S1}$$

Since

$$\frac{R_2}{R_1+R_2}=\frac{1}{R_1}\cdot\left(\frac{R_1R_2}{R_1+R_2}\right)=\frac{1}{R_1}\cdot R_i$$

then

$$1.83=\frac{1}{R_1}(100)(10)-(0.2)(3.9)$$

which yields $R_1 = 383\,\text{k}\Omega$. From $R_i = 100\,\text{k}\Omega$, we find that $R_2 = 135\,\text{k}\Omega$.

Comment: Both transistors are biased in the saturation region, which is desired for linear amplifiers.

Figure 6.50 shows a cascode circuit with n-channel MOSFETs. Transistor M_1 is connected in a common-source configuration and M_2 is connected in a common-gate configuration. The advantage of this type of circuit is a higher frequency response, which is discussed in a later chapter.

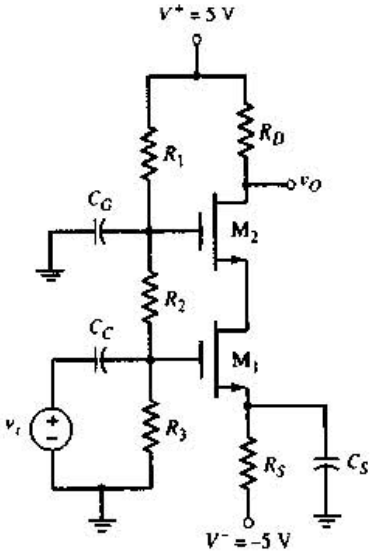

Figure 6.50 NMOS cascode circuit

Design Example 6.15 **Objective:** Design the biasing of the cascode circuit to meet specific requirements.

For the circuit shown in Figure 6.50, the transistor parameters are: $V_{TN1} = V_{TN2} = 1.2\,\text{V}$, $K_{n1} = K_{n2} = 0.8\,\text{mA/V}^2$, and $\lambda_1 = \lambda_2 = 0$. Let $R_1 + R_2 + R_3 = 300\,\text{k}\Omega$ and $R_S = 10\,\text{k}\Omega$. Design the circuit such that $I_{DQ} = 0.4\,\text{mA}$ and $V_{DSQ1} = V_{DSQ2} = 2.5\,\text{V}$.

Solution: The dc voltage at the source of M_1 is

$$V_{S1}=I_{DQ}R_S-5=(0.4)(10)-5=-1\,\text{V}$$

Since M_1 and M_2 are identical transistors, and since the same current exists in the two transistors, the gate-to-source voltage is the same for both devices. We have

$$I_D = K_n(V_{GS} - V_{TN})^2$$

or

$$0.4 = 0.8(V_{GS} - 1.2)^2$$

which yields

$$V_{GS} = 1.91\,\text{V}$$

Then,

$$V_{G1} = \left(\frac{R_3}{R_1 + R_2 + R_3}\right)(5) = V_{GS} + V_{S1}$$

or

$$\left(\frac{R_3}{300}\right)(5) = 1.91 - 1 = 0.91$$

which yields

$$R_3 = 54.6\,\text{k}\Omega$$

The voltage at the source of M_2 is

$$V_{S2} = V_{DSQ2} + V_{S2} = 2.5 - 1 = 1.5\,\text{V}$$

Then,

$$V_{G2} = \left(\frac{R_2 + R_3}{R_1 + R_2 + R_3}\right)(5) = V_{GS} + V_{S2}$$

or

$$\left(\frac{R_2 + R_3}{300}\right)(5) = 1.91 + 1.5 = 3.41\,\text{V}$$

which yields

$$R_2 + R_3 = 204.6\,\text{k}\Omega$$

and

$$R_2 = 150\,\text{k}\Omega$$

Therefore

$$R_1 = 95.4\,\text{k}\Omega$$

The voltage at the drain of M_2 is

$$V_{D2} = V_{DSQ2} + V_{S2} = 2.5 + 1.5 = 4\,\text{V}$$

The drain resistor is therefore

$$R_D = \frac{5 - V_{D2}}{I_{DQ}} = \frac{5 - 4}{0.4} = 2.5\,\text{k}\Omega$$

Comment: Since $V_{DS} = 2.5\,\text{V} > V_{GS} - V_{TN} = 1.91 - 1.2 = 0.71\,\text{V}$, each transistor is biased in the saturation region.

6.8.2 Small-Signal Analysis

The midband small-signal voltage gain of multistage amplifiers is determined by assuming that all external coupling capacitors act as short circuits and inserting the small-signal equivalent circuits for the transistors.

Example 6.16 **Objective:** Determine the small-signal voltage gain of a multistage cascade circuit.

Consider the circuit shown in Figure 6.49 with transistor and circuit parameters given in Example 6.14.

Solution: The small-signal transconductance parameters are

$$g_{m1} = 2K_{n1}(V_{GS1} - V_{TN1}) = 2(0.50)(1.83 - 1.2) = 0.63\,\text{mA/V}$$

and

$$g_{m2} = 2K_{n2}(V_{GS2} - V_{TN2}) = 2(0.2)(2.78 - 1.2) = 0.632\,\text{mA/V}$$

The small-signal equivalent circuit is shown in Figure 6.51.

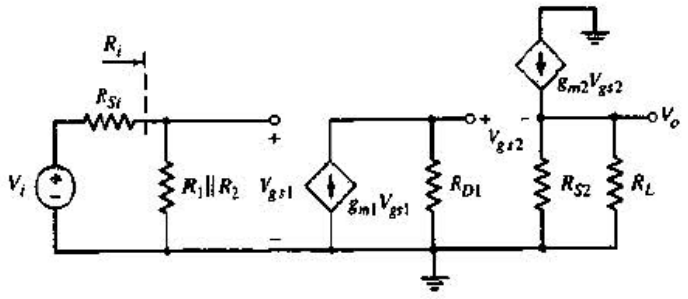

Figure 6.51 Small-signal equivalent circuit of NMOS cascade circuit

The output voltage is

$$V_o = g_{m2}V_{gs2}(R_{S2} \| R_L)$$

Also,

$$V_{gs2} + V_o = -g_{m1}V_{gs1}R_{D1}$$

where

$$V_{gs1} = \left(\frac{R_i}{R_i + R_{Si}}\right) \cdot V_i$$

Then

$$V_{gs2} = -g_{m1}R_{D1}\left(\frac{R_i}{R_i + R_{Si}}\right) \cdot V_i - V_o$$

Therefore

$$V_o = g_{m2}\left[-g_{m1}R_{D1}\left(\frac{R_i}{R_i + R_{Si}}\right) \cdot V_i - V_o\right](R_{S2} \| R_L)$$

The small-signal voltage gain is then

$$A_v = \frac{V_o}{V_i} = \frac{-g_{m1}g_{m2}R_{D1}(R_{S2}\|R_L)}{1 + g_{m2}(R_{S2}\|R_L)} \cdot \left(\frac{R_i}{R_i + R_{Si}}\right)$$

or

$$A_v = \frac{-(0.63)(0.632)(16.1)(8\|4)}{1 + (0.632)(8\|4)} \cdot \left(\frac{100}{100 + 4}\right) = -6.13$$

Comment: Since the small-signal voltage gain of the source follower is slightly less than 1, the overall gain is due essentially to the common-source input stage. Also, as shown previously, the output resistance of the source follower is small, which is desirable in many applications.

Example 6.17 **Objective:** Determine the small-signal voltage gain of a cascode circuit.

For the circuit shown in Figure 6.50, the transistor and circuit parameters are as given in Example 6.15. The input signal to the circuit is an ideal voltage source.

Solution: Since the transistors are identical, the small-signal transconductance parameters of the two transistors are equal. Therefore,

$$g_{m1} = g_{m2} = 2K_n(V_{GS} - V_{TN}) = 2(0.8)(1.91 - 1.2) = 1.14\,\text{mA/V}$$

The small-signal equivalent circuit is shown in Figure 6.52. Transistor M_1 supplies the source current of M_2 with the signal current ($g_{m1}V_i$). Transistor M_2 acts as a current follower and passes this current on to its drain terminal. The output voltage is therefore

$$V_o = -g_{m1}V_{gs1}R_D$$

Since $V_{gs1} = V_i$, the small-signal voltage gain is

$$A_v = \frac{V_o}{V_i} = -g_{m1}R_D$$

or

$$A_v = -(1.14)(2.5) = -2.85$$

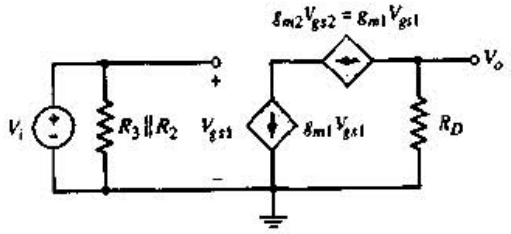

Figure 6.52 Small-signal equivalent circuit of NMOS cascode circuit

Comment: The small-signal voltage gain is essentially the same as that of a single common-source amplifier stage. The addition of a common-gate transistor will increase the frequency bandwidth, as we will see in a later chapter.

Test Your Understanding

6.25 For the cascade circuit shown in Figure 6.49, the transistor and circuit parameters are given in Example 6.15. Calculate the small-signal output resistance R_o. (The small-signal equivalent circuit is shown in Figure 6.51.) (Ans. $R_o = 1.32\,\text{k}\Omega$)

***D6.26** The supply voltages to the cascade circuit shown in Figure 6.49 are changed to $V^+ = 10\,\text{V}$ and $V^- = -10\,\text{V}$. The transistor parameters are: $K_{n1} = K_{n2} = 1\,\text{mA/V}^2$, $V_{TN1} = V_{TN2} = 2\,\text{V}$, and $\lambda_1 = \lambda_2 = 0.01\,\text{V}^{-1}$. (a) Let $R_L = 4\,\text{k}\Omega$, and design the circuit such that $I_{DQ1} = I_{DQ2} = 2\,\text{mA}$, $V_{DSQ1} = V_{DSQ2} = 10\,\text{V}$, and $R_{sig} = 200\,\text{k}\Omega$. (b) Calculate the small-signal voltage gain and the output resistance R_o. (Ans. (a) $R_{S2} = 5\,\text{k}\Omega$, $R_{D1} = 3.3\,\text{k}\Omega$, $R_{S1} = 1.71\,\text{k}\Omega$, $R_1 = 586\,\text{k}\Omega$, $R_2 = 304\,\text{k}\Omega$; (b) $A_v = -8.06$, $R_o = 0.330\,\text{k}\Omega$)

D6.27 The supply voltages to the cascode circuit shown in Figure 6.50 are changed to $V^+ = 10\,\text{V}$ and $V^- = -10\,\text{V}$. The transistor parameters are: $K_{n1} = K_{n2} = 1.2\,\text{mA/V}^2$, $V_{TN1} = V_{TN2} = 2\,\text{V}$, and $\lambda_1 = \lambda_2 = 0$. (a) Let $R_1 + R_2 + R_3 = 500\,\text{k}\Omega$, and $R_S = 10\,\text{k}\Omega$. Design the circuit such that $I_{DQ} = 1\,\text{mA}$ and $V_{DSQ1} = V_{DSQ2} = 3.5\,\text{V}$. (b) Determine the small-signal voltage gain. (Ans. (a) $R_3 = 145.5\,\text{k}\Omega$, $R_2 = 175\,\text{k}\Omega$, $R_1 = 179.5\,\text{k}\Omega$, $R_D = 3\,\text{k}\Omega$; (b) $A_v = -6.57$)

6.9 BASIC JFET AMPLIFIERS

Like MOSFETs, JFETs can be used to amplify small time-varying signals. Initially, we will develop the small-signal model and equivalent circuit of the JFET. We will then use the model in the analysis of JFET amplifiers.

6.9.1 Small-Signal Equivalent Circuit

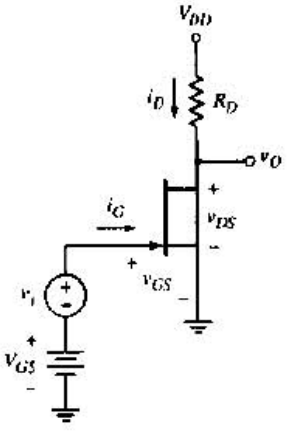

Figure 6.53 JFET common-source circuit with time-varying signal source in series with gate dc source

Figure 6.53 shows a JFET circuit with a time-varying signal applied to the gate. The instantaneous gate-to-source voltage is

$$v_{GS} = V_{GS} + v_i = V_{GS} + v_{gs} \tag{6.53}$$

where v_{gs} is the small-signal gate-to-source voltage. Assuming the transistor is biased in the saturation region, the instantaneous drain current is

$$i_D = I_{DSS}\left(1 - \frac{v_{GS}}{V_P}\right)^2 \tag{6.54}$$

where I_{DSS} is the saturation current and V_P is the pinchoff voltage. Substituting Equation (6.53) into (6.54), we obtain

$$i_D = I_{DSS}\left[\left(1 - \frac{V_{GS}}{V_P}\right) - \left(\frac{v_{gs}}{V_P}\right)\right]^2 \tag{6.55}$$

If we expand the squared term, we have

$$i_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 - 2I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)\left(\frac{v_{gs}}{V_P}\right) + I_{DSS}\left(\frac{v_{gs}}{V_P}\right)^2 \tag{6.56}$$

The first term in Equation (6.56) is the dc or quiescent drain current I_{DQ}, the second term is the time-varying drain current component, which is linearly

related to the signal voltage v_{gs}, and the third term is proportional to the square of the signal voltage. As in the case of the MOSFET, the third term produces a nonlinear distortion in the output current. To minimize this distortion, we will usually impose the following condition:

$$\left|\frac{v_{gs}}{V_P}\right| \ll 2\left(1 - \frac{V_{GS}}{V_P}\right) \tag{6.57}$$

Equation (6.57) represents the small-signal condition that must be satisfied for JFET amplifiers to be linear.

Neglecting the term v_{gs}^2 in Equation (6.56), we can write

$$i_D = I_{DQ} + i_d \tag{6.58}$$

where the time-varying signal current is

$$i_d = +\frac{2I_{DSS}}{(-V_P)}\left(1 - \frac{V_{GS}}{V_P}\right)v_{gs} \tag{6.59}$$

The constant relating the small-signal drain current and small-signal gate-to-source voltage is the transconductance g_m. We can write

$$i_d = g_m v_{gs} \tag{6.60}$$

where

$$g_m = +\frac{2I_{DSS}}{(-V_P)}\left(1 - \frac{V_{GS}}{V_P}\right) \tag{6.61}$$

Since V_P is negative for n-channel JFETs, the transconductance is positive. A relationship that applies to both n-channel and p-channel JFETs is

$$g_m = \frac{2I_{DSS}}{|V_P|}\left(1 - \frac{V_{GS}}{V_P}\right) \tag{6.62}$$

We can also obtain the transconductance from

$$g_m = \left.\frac{\partial i_D}{\partial v_{GS}}\right|_{v_{GS}=V_{GSQ}} \tag{6.63}$$

Since the transconductance is directly proportional to the saturation current I_{DSS}, the transconductance is also a function of the width-to-length ratio of the transistor.

Since we are looking into a reverse-biased pn junction, we assume that the input gate current i_g is zero, which means that the small-signal input resistance is infinite. Equation (6.54) can be expanded to take into account the finite output resistance of a JFET biased in the saturation region. The equation becomes

$$i_D = I_{DSS}\left(1 - \frac{v_{GS}}{V_P}\right)^2(1 + \lambda v_{DS}) \tag{6.64}$$

The small-signal output resistance is

$$r_o = \left(\frac{\partial i_D}{\partial v_{DS}}\right)^{-1}\Bigg|_{v_{GS}=\text{const.}} \tag{6.65}$$

Using Equation (6.64), we obtain

$$r_o = \left[\lambda I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2\right]^{-1} \tag{6.66(a)}$$

or

$$r_o \cong [\lambda I_{DQ}]^{-1} = \frac{1}{\lambda I_{DQ}} \tag{6.66(b)}$$

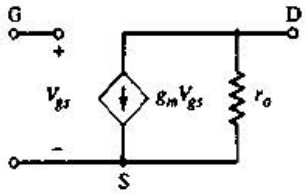

Figure 6.54 Small-signal equivalent circuit of n-channel JFET

The small-signal equivalent circuit of the n-channel JFET, shown in Figure 6.54, is exactly the same as that of the n-channel MOSFET. The small-signal equivalent circuit of the p-channel JFET is also the same as that of the p-channel MOSFET. However, the polarity of the controlling gate-to-source voltage and the direction of the dependent current source are reversed from those of the n-channel device.

6.9.2 Small-Signal Analysis

Since the small-signal equivalent circuit of the JFET is the same as that of the MOSFET, the small-signal analyses of the two types of circuits are identical. For illustration purposes, we will analyze two JFET circuits.

Example 6.18 **Objective:** Determine the small-signal voltage gain of a JFET amplifier.

Consider the circuit shown in Figure 6.55 with transistor parameters $I_{DSS} = 12\,\text{mA}$, $V_P = -4\,\text{V}$, and $\lambda = 0.008\,\text{V}^{-1}$. Determine the small-signal voltage gain $A_v = v_o/v_i$.

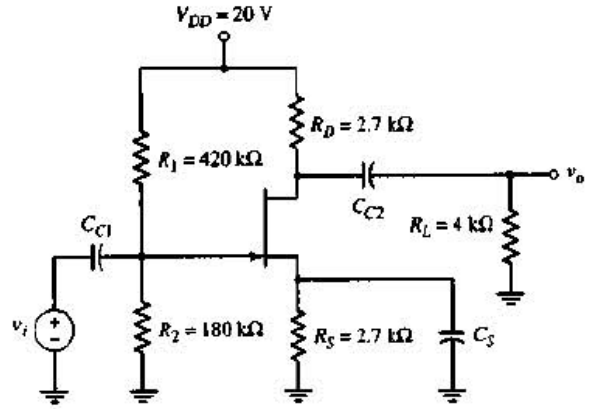

Figure 6.55 Common-source JFET circuit with source resistor and source bypass capacitor

Solution: The dc quiescent gate-to-source voltage is determined from

$$V_{GSQ} = \left(\frac{R_2}{R_1 + R_2}\right)V_{DD} - I_{DQ}R_S$$

where

$$I_{DQ} = I_{DSS}\left(1 - \frac{V_{GSQ}}{V_P}\right)^2$$

Combining these two equations produces

$$V_{GSQ} = \left(\frac{180}{180+420}\right)(20) - (12)(2.7)\left(1 - \frac{V_{GSQ}}{(-4)}\right)^2$$

which reduces to

$$2.025V_{GSQ}^2 + 17.2V_{GSQ} + 26.4 = 0$$

The appropriate solution is

$$V_{GSQ} = -2.01\text{ V}$$

The quiescent drain current is

$$I_{DQ} = I_{DSS}\left(1 - \frac{V_{GSQ}}{V_P}\right)^2 = (12)\left(1 - \frac{(-2.01)}{(-4)}\right)^2 = 2.97\text{mA}$$

The small-signal parameters are then

$$g_m = \frac{2I_{DSS}}{(-V_P)}\left(1 - \frac{V_{GS}}{V_P}\right) = \frac{2(12)}{(4)}\left(1 - \frac{(-2.01)}{(-4)}\right) = 2.98\text{ mA/V}$$

and

$$r_o = \frac{1}{\lambda I_{DQ}} = \frac{1}{(0.008)(2.97)} = 42.1\text{ k}\Omega$$

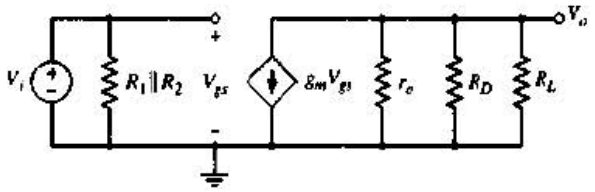

Figure 6.56 Small-signal equivalent circuit of common-source JFET, assuming bypass capacitor acts as a short circuit

The small-signal equivalent circuit is shown in Figure 6.56.

Since $V_{gs} = V_i$, the small-signal voltage gain is

$$A_v = \frac{V_o}{V_i} = -g_m(r_o \| R_D \| R_L)$$

or

$$A_v = -(2.98)(42.1 \| 2.7 \| 4) = -4.62$$

Comment: The voltage gain of JFET amplifiers is the same order of magnitude as that of MOSFET amplifiers.

Design Example 6.19 **Objective:** Design a JFET source-follower circuit with a specified small-signal voltage gain.

For the source-follower circuit shown in Figure 6.57, the transistor parameters are: $I_{DSS} = 12\,\text{mA}$, $V_P = -4\,\text{V}$, and $\lambda = 0.01\,\text{V}^{-1}$. Determine R_S and I_{DQ} such that the small-signal voltage gain is at least $A_v = v_o/v_i = 0.90$.

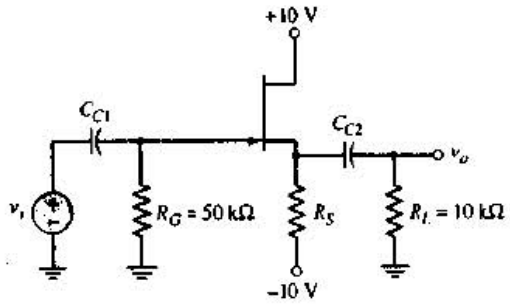

Figure 6.57 JFET source-follower circuit

Solution: The small-signal equivalent circuit is shown in Figure 6.58. The output voltage is

$$V_o = g_m V_{gs}(R_S \| R_L \| r_o)$$

Also

$$V_i = V_{gs} + V_o$$

or

$$V_{gs} = V_i - V_o$$

Therefore, the output voltage is

$$V_o = g_m(V_i - V_o)(R_S \| R_L \| r_o)$$

The small-signal voltage gain becomes

$$A_v = \frac{V_o}{V_i} = \frac{g_m(R_S \| R_L \| r_o)}{1 + g_m(R_S \| R_L \| r_o)}$$

As a first approximation, assume r_o is sufficiently large for the effect of r_o to be neglected.

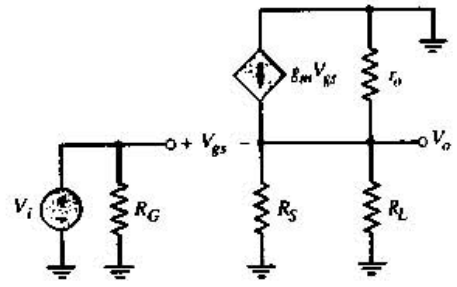

Figure 6.58 Small-signal equivalent circuit of JFET source-follower circuit

The transconductance is

$$g_m = \frac{2I_{DSS}}{(-V_P)}\left(1 - \frac{V_{GS}}{V_P}\right) = \frac{2(12)}{4}\left(1 - \frac{V_{GS}}{(-4)}\right)$$

If we pick a nominal transconductance value of $g_m = 2\,\text{mA/V}$, then $V_{GS} = -2.67\,\text{V}$ and the quiescent drain current is

$$I_{DQ} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = (12)\left(1 - \frac{(-2.67)}{(-4)}\right)^2 = 1.33\,\text{mA}$$

The value of R_S is then determined from

$$R_S = \frac{-V_{GS} - (-10)}{I_{DQ}} = \frac{2.67 + 10}{1.33} = 9.53\,\text{k}\Omega$$

Also, the value of r_o is

$$r_o = \frac{1}{\lambda I_{DQ}} = \frac{1}{(0.01)(1.33)} = 75.2\,\text{k}\Omega$$

The small-signal voltage gain, including the effect of r_o, is

$$A_v = \frac{g_m(R_S \| R_L \| r_o)}{1 + g_m(R_S \| R_L \| r_o)} = \frac{(2)(9.53 \| 10 \| 75.2)}{1 + (2)(9.53 \| 10 \| 75.2)} = 0.902$$

Comment: This particular design meets the design criteria, but the solution is not unique.

In the last example, we chose a value of transconductance and continued through the design. A more detailed examination shows that both g_m and R_S depend upon the drain current I_{DQ} in such a way that the product $g_m R_S$ is approximately a constant. This means the small-signal voltage gain is insensitive to the initial value of the transconductance.

Test Your Understanding

6.28 Reconsider the JFET amplifier shown in Figure 6.55 with transistor parameters given in Example 6.19. Determine the small-signal voltage gain if a $20\,\text{k}\Omega$ resistor is in series with the signal source v_i. (Ans. $A_v = -3.98$)

RD6.29 For the JFET amplifier shown in Figure 6.55, the transistor parameters are: $I_{DSS} = 4\,\text{mA}$, $V_P = -3\,\text{V}$, and $\lambda = 0.005\,\text{V}^{-1}$. Let $R_L = 4\,\text{k}\Omega$, $R_S = 2.7\,\text{k}\Omega$, and $R_1 + R_2 = 500\,\text{k}\Omega$. Redesign the circuit such that $I_{DQ} = 1.2\,\text{mA}$ and $V_{DSQ} = 12\,\text{V}$. Calculate the small-signal voltage gain. (Ans. $R_D = 3.97\,\text{k}\Omega$, $R_1 = 453\,\text{k}\Omega$, $R_2 = 47\,\text{k}\Omega$, $A_v = -2.87$)

***6.30** For the circuit shown in Figure 6.59, the transistor parameters are: $I_{DSS} = 6\,\text{mA}$, $|V_P| = 2\,\text{V}$, and $\lambda = 0$. **(a) Calculate the quiescent drain current and drain-to-**

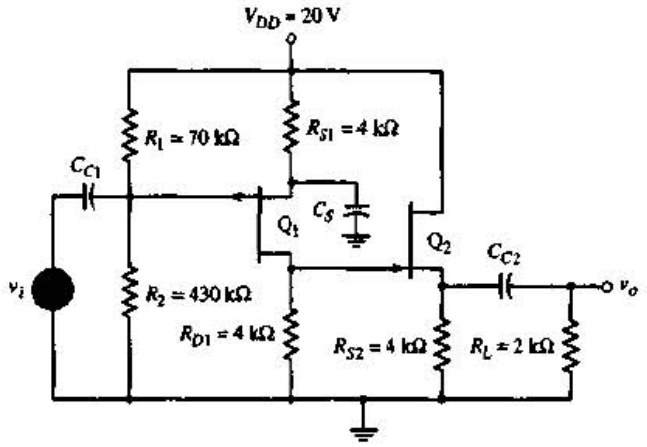

Figure 6.59 Figure for Exercise 6.30

source voltage of each transistor. (b) Determine the overall small-signal voltage gain $A_v = v_o/v_i$. (Ans. (a) $I_{DQ1} = 1$ mA, $V_{SDQ1} = 12$ V, $I_{DQ2} = 1.27$ mA, $V_{DSQ2} = 14.9$ V; (b) $A_v = -2.05$)

6.31 Reconsider the source-follower circuit shown in Figure 6.57 with transistor parameters $I_{DSS} = 8$ mA, $V_P = -3.5$ V, and $\lambda = 0.01\ \text{V}^{-1}$. (a) Design the circuit such that $I_{DQ} = 2$ mA. (b) Calculate the small-signal voltage gain if R_L approaches infinity. (c) Determine the value of R_L at which the small-signal gain is reduced by 20 percent from its value for (b). (Ans. (a) $R_S = 5.88\,\text{k}\Omega$, (b) $A_v = 0.923$, $R_L = 1.64\,\text{k}\Omega$)

6.10 SUMMARY

- The application of MOSFET transistors in linear amplifier circuits was emphasized in this chapter. A small-signal equivalent circuit for the transistor was developed, which is used in the analysis and design of linear amplifiers.
- Three basic circuit configurations were considered: the common source, source follower, and common gate. These three configurations form the basic building blocks for complex integrated circuits. The small-signal voltage gains and output resistances for these circuits were analyzed. The circuit characteristics of the three circuits were compared in Table 6.1.
- The ac analysis of circuits with enhancement load devices, with depletion load devices, and complementary (CMOS) devices were analyzed. These circuits are examples of all MOSFET circuits and act as an introduction to more complex all-MOSFET integrated circuits considered later in the text.
- The small-signal equivalent circuit of a JFET was developed and used in the analysis of several configurations of JFET amplifiers.

CHECKPOINT

After studying this chapter, the reader should have the ability to:

✔ Explain graphically the amplification process in a simple MOSFET amplifier circuit. (Section 6.1)

✔ Describe the small-signal equivalent circuit of the MOSFET and to determine the values of the small-signal parameters. (Section 6.1)

- ✔ Apply the small-signal equivalent circuit to various MOSFET amplifier circuits to obtain the time-varying circuit characteristics. (Section 6.1)
- ✔ Characterize the small-signal voltage gain and output resistance of a common-source amplifier. (Section 6.3)
- ✔ Characterize the small-signal voltage gain and output resistance of a source-follower amplifier. (Section 6.4)
- ✔ Characterize the small-signal voltage gain and output resistance of a common-gate amplifier. (Section 6.5)
- ✔ Describe the operation of an NMOS amplifier with either an enhancement load, a depletion load, or a PMOS load. (Section 6.7)
- ✔ Apply the MOSFET small-signal equivalent circuit in the analysis of multistage amplifier circuits. (Section 6.8)
- ✔ Describe the operation and analyze basic JFET amplifier circuits. (Section 6.9)

REVIEW QUESTIONS

1. Discuss, using the concept of a load line superimposed on the transistor characteristics, how a simple common-source circuit can amplify a time-varying signal.
2. How does a transistor width-to-length ratio affect the small-signal voltage gain of a common-source amplifier?
3. Discuss the physical meaning of the small-signal circuit parameter r_o.
4. How does the body effect change the small-signal equivalent circuit of the MOSFET?
5. Sketch a simple common-source amplifier circuit and discuss the general ac circuit characteristics (voltage gain and output resistance).
6. Discuss the general conditions under which a common-source amplifier would be used.
7. Why, in general, is the magnitude of the voltage gain of a common-source amplifier smaller than that of a bipolar common-emitter amplifier?
8. What are the changes in the ac characteristics of a common-source amplifier when a source resistor and a source bypass capacitor are incorporated in the design?
9. Sketch a simple source-follower amplifier circuit and discuss the general ac circuit characteristics (voltage gain and output resistance).
10. Discuss the general conditions under which a source-follower amplifier would be used.
11. Sketch a simple common-gate amplifier circuit and discuss the general ac circuit characteristics (voltage gain and output resistance).
12. Discuss the general conditions under which a common-gate amplifier would be used.
13. Compare the ac circuit characteristics of the common-source, source-follower, and common-gate circuits.
14. State the general advantage of using transistors in place of resistors in integrated circuits.
15. State at least two reasons why a multistage amplifier circuit would be required in a design compared to using a single-stage circuit.
16. Give one reason why a JFET might be used as an input device in a circuit as opposed to a MOSFET.

PROBLEMS

Section 6.1 The MOSFET Amplifier

6.1 An NMOS transistor has parameters $V_{TN} = 0.8\,\text{V}$, $k_n' = 40\,\mu\text{A/V}^2$, and $\lambda = 0$. (a) Determine the width-to-length ratio (W/L) such that $g_m = 0.5\,\text{mA/V}$ at $I_D = 0.5\,\text{mA}$ when biased in the saturation region. (b) Calculate the required value of V_{GS}.

6.2 A PMOS transistor has parameters $V_{TP} = -1.2\,\text{V}$, $k_p' = 20\,\mu\text{A/V}$, and $\lambda = 0$. (a) Determine the width-to-length ratio (W/L) such that $g_m = 50\,\mu\text{A/V}$ at $I_D = 0.1\,\text{mA}$ when biased in the saturation region. (b) Calculate the required value of V_{SG}.

6.3 An NMOS transistor is biased in the saturation region at a constant V_{GS}. The drain current is $I_D = 3\,\text{mA}$ at $V_{DS} = 5\,\text{V}$ and $I_D = 3.4\,\text{mA}$ at $V_{DS} = 10\,\text{V}$. Determine λ and r_o.

6.4 The minimum value of small-signal resistance of a PMOS transistor is to be $r_o = 100\,\text{k}\Omega$. If $\lambda = 0.012\,\text{V}^{-1}$, calculate the maximum allowed value of I_D.

6.5 Calculate the small-signal voltage gain of the circuit shown in Figure 6.1, for $g_m = 1\,\text{mA/V}$, $r_o = 50\,\text{k}\Omega$, and $R_D = 10\,\text{k}\Omega$.

***D6.6** For the circuit shown in Figure 6.1, the transistor parameters are: $V_{TN} = +0.8\,\text{V}$, $\lambda = 0.015\,\text{V}^{-1}$, and $k_n' = 60\,\mu\text{A/V}^2$. Let $V_{DD} = 10\,\text{V}$. (a) Design the transistor width-to-length ratio (W/L) and the resistance R_D such that $I_{DQ} = 0.5\,\text{mA}$ and $V_{DSQ} = 6\,\text{V}$. (b) Calculate g_m and r_o. (c) What is the small-signal voltage gain $A_v = v_o/v_i$?

***6.7** In our analyses, we assumed the small-signal condition given by Equation (6.4). Now consider Equation (6.3(b)) and let $v_{gs} = V_{gs}\sin\omega t$. Show that the ratio of the signal at frequency 2ω to the signal at frequency ω is given by $V_{gs}/[4(V_{GS} - V_{TN})]$. This ratio, expressed in a percentage, is called the **second-harmonic distortion**. [Hint: Use the trigonometric identity $\sin^2\theta = \frac{1}{2} - \frac{1}{2}\cos 2\theta$.]

6.8 Using the results of Problem 6.7, find the peak amplitude V_{gs} that produces a second-harmonic distortion of 1 percent if $V_{GS} = 3\,\text{V}$ and $V_{TN} = 1\,\text{V}$.

Section 6.3 The Common-Source Amplifier

6.9 Calculate the small-signal voltage gain of a common-source amplifier, such as that shown in Figure 6.13, assuming $g_m = 1\,\text{mA/V}$, $r_o = 50\,\text{k}\Omega$, and $R_D = 10\,\text{k}\Omega$. Also assume $R_{Si} = 2\,\text{k}\Omega$ and $R_1 \| R_2 = 50\,\text{k}\Omega$.

6.10 A common-source amplifier, such as shown in Figure 6.13 in the text, has parameters $r_o = 100\,\text{k}\Omega$ and $R_D = 5\,\text{k}\Omega$. Determine the transconductance of the transistor if the small-signal voltage gain is $A_v = -10$. Assume $R_{Si} = 0$.

6.11 For the NMOS common-source amplifier in Figure P6.11, the transistor parameters are: $V_{TN} = 2\,\text{V}$, $K_n = 1\,\text{mA/V}^2$, and $\lambda = 0$. The circuit parameters are: $V_{DD} = 12\,\text{V}$, $R_S = 2\,\text{k}\Omega$, $R_D = 3\,\text{k}\Omega$, $R_1 = 300\,\text{k}\Omega$, and $R_2 = 200\,\text{k}\Omega$. Assume $R_{Si} = 2\,\text{k}\Omega$ and assume a load resistance $R_L = 3\,\text{k}\Omega$ is capacitively coupled to the output. (a) Determine the quiescent values of I_D and V_{DS}. (b) Find the small-signal voltage gain. (c) Determine the maximum symmetrical swing in the output voltage.

6.12 In the circuit in Figure P6.11, $V_{DD} = 15\,\text{V}$, $R_D = 2\,\text{k}\Omega$, $R_L = 5\,\text{k}\Omega$, $R_S = 0.5\,\text{k}\Omega$, and $R_{in} = 200\,\text{k}\Omega$. (a) Find R_1 and R_2 such that $I_{DQ} = 3\,\text{mA}$ for $V_{TN} = 2\,\text{V}$, $K_n = 2\,\text{mA/V}^2$, and $\lambda = 0$. (b) Determine the small-signal voltage gain.

6.13 Repeat Problem 6.11 if the source resistor is bypassed by a source capacitor C_S.

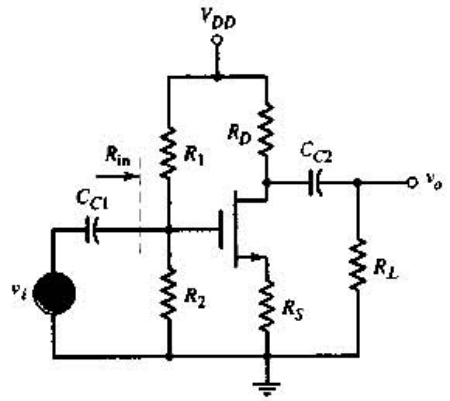

Figure P6.11

***6.14** The transistor in the common-source amplifier in Figure P6.14 has parameters $V_{TN} = 1\,\text{V}$, $K_n = 0.5\,\text{mA/V}^2$, and $\lambda = 0.01\,\text{V}^{-1}$. The circuit parameters are: $V^+ = 5\,\text{V}$, $V^- = -5\,\text{V}$, and $R_D = R_L = 10\,\text{k}\Omega$. (a) Determine I_{DQ} to achieve the maximum symmetrical swing in the output voltage. (b) Find the small-signal voltage gain.

D6.15 For the common-source amplifier in Figure P6.15, the transistor parameters are: $V_{TN} = -1\,\text{V}$, $K_n = 4\,\text{mA/V}^2$, and $\lambda = 0$. The circuit parameters are $V_{DD} = 10\,\text{V}$ and $R_L = 2\,\text{k}\Omega$. (a) Design the circuit such that $I_{DQ} = 2\,\text{mA}$ and $V_{DSQ} = 6\,\text{V}$. (b) Determine the small-signal voltage gain. (c) If $v_i = V_i \sin \omega t$, determine the maximum value of V_i such that v_o is an undistorted sine wave.

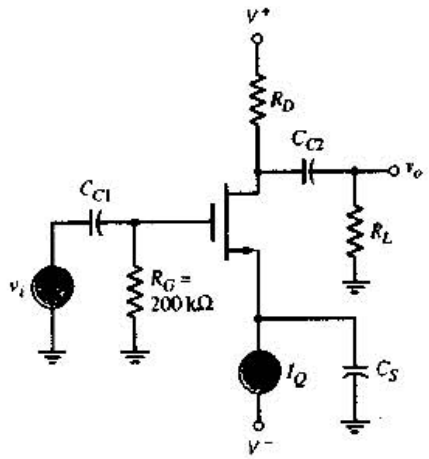

Figure P6.14

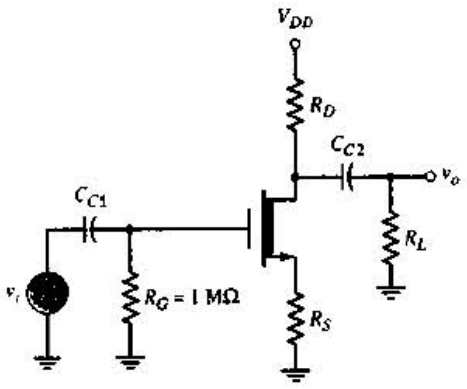

Figure P6.15

***6.16** The transistor in the common-source circuit in Figure P6.15 has the same parameters as given in Problem 6.15. The circuit parameters are $V_{DD} = 5\,\text{V}$ and $R_D = R_L = 2\,\text{k}\Omega$. (a) Find R_S and $V_{DSQ} = 2.5\,\text{V}$. (b) Determine the small-signal voltage gain.

***6.17** Consider the PMOS common-source circuit in Figure P6.17 with transistor parameters $V_{TP} = -2\,\text{V}$ and $\lambda = 0$, and circuit parameters $R_D = R_L = 10\,\text{k}\Omega$. (a) Determine the values of K_p and R_S such that $V_{SDQ} = 6\,\text{V}$. (b) Determine the resulting value of I_{DQ} and the small-signal voltage gain. (c) Can the values of K_p and R_S from

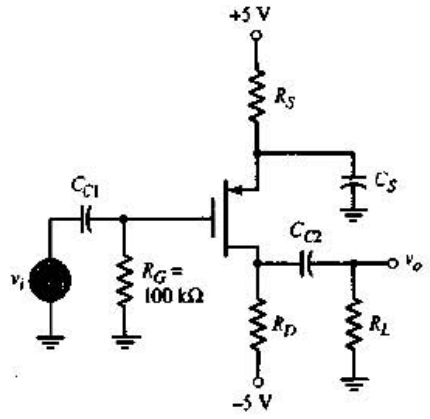

Figure P6.17

part (a) be changed to achieve a larger voltage gain, while still meeting the requirements of part (a)?

D6.18 For the common-source circuit in Figure P6.17, the PMOS transistor parameters are: $V_{TP} = -1.5\,\text{V}$, $K_p = 5\,\text{mA/V}^2$, and $\lambda = 0$. The load resistor is $R_L = 2\,\text{k}\Omega$. (a) Design the circuit such that $I_{DQ} = 1\,\text{mA}$ and $V_{SDQ} = 5\,\text{V}$. (b) Determine the small-signal voltage gain $A_v = v_o/v_i$. (c) What is the maximum symmetrical swing in the output voltage?

***D6.19** Design the common-source circuit in Figure P6.19 using an n-channel MOSFET with $\lambda = 0$. The quiescent values are to be $I_{DQ} = 6\,\text{mA}$, $V_{GSQ} = 2.8\,\text{V}$, and $V_{DSQ} = 10\,\text{V}$. The transconductance is $g_m = 2.2\,\text{mA/V}$. Let $R_L = 1\,\text{k}\Omega$, $A_v = -1$, and $R_{in} = 100\,\text{k}\Omega$. Find R_1, R_2, R_S, R_D, K_n, and V_{TN}.

***6.20** For the common-source amplifier in Figure P6.20, the transistor parameters are: $V_{TP} = -1.5\,\text{V}$, $K_p = 2\,\text{mA/V}^2$, and $\lambda = 0.01\,\text{V}^{-1}$. The circuit is to drive a load resistance of $R_L = 20\,\text{k}\Omega$. To minimize loading effects, the drain resistance should be $R_D \le 0.1R_L$. (a) Determine I_Q such that the Q-point is in the center of the saturation region. (b) Determine the open-circuit ($R_L = \infty$) small-signal voltage gain. (c) By what percentage does the small-signal voltage gain decrease when R_L is connected?

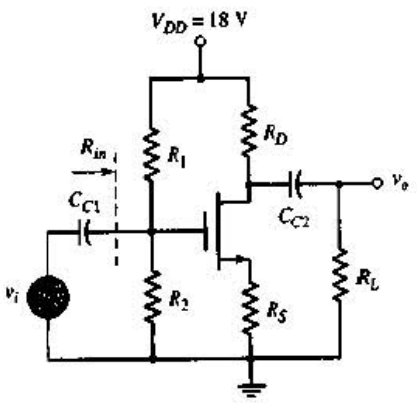

Figure P6.19

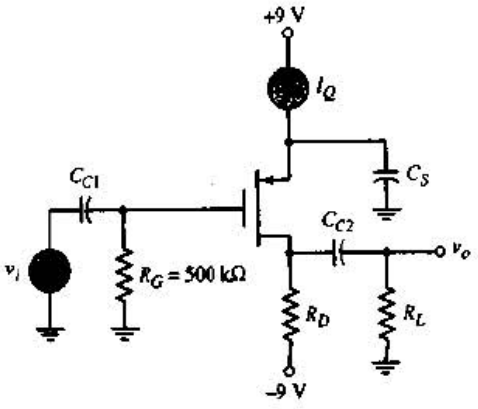

Figure P6.20

D6.21 For the circuit shown in Figure P6.21, the transistor parameters are: $V_{TP} = 2\,V$, $K_p = 0.5\,mA/V^2$, and $\lambda = 0$. (a) Design the circuit such that $I_{DQ} = 2\,mA$ and $V_{SDQ} = 6\,V$. (b) Determine the small-signal voltage gain $A_v = v_o/v_i$.

***D6.22** Design a common-source amplifier, such as that in Figure P6.22, to achieve a small-signal voltage gain of at least $A_v = v_o/v_i = -10$ for $R_L = 20\,k\Omega$ and $R_{in} = 200\,k\Omega$. Assume the Q-point is chosen at $I_{DQ} = 1\,mA$ and $V_{DSQ} = 10\,V$. Let $V_{TN} = 2\,V$, and $\lambda = 0$.

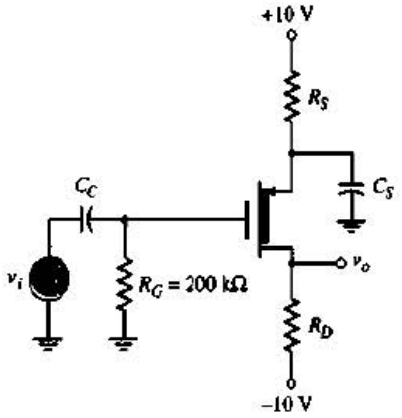

Figure P6.21

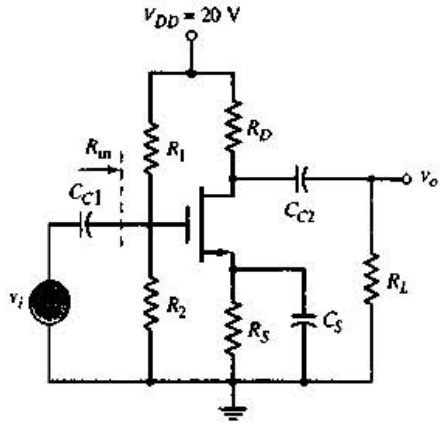

Figure P6.22

Section 6.4 The Source-Follower Amplifier

6.23 For an enhancement-mode MOSFET source follower, $g_m = 4\,mA/V$ and $r_o = 50\,k\Omega$. Determine the no-load voltage gain and the output resistance. Calculate the small-signal voltage gain when a load resistance $R_S = 2.5\,k\Omega$ is connected.

6.24 The transistor in the source-follower circuit in Figure P6.24 has parameters $K_p = 2\,mA/V^2$, $V_{TP} = -2\,V$, and $\lambda = 0.02\,V^{-1}$. The circuit parameters are: $R_L = 4\,k\Omega$, $R_S = 4\,k\Omega$, $R_1 = 1.24\,M\Omega$, and $R_2 = 396\,k\Omega$. (a) Calculate I_{DQ} and V_{SDQ}. (b) Determine the small-signal gains $A_v = v_o/v_i$ and $A_i = i_o/i_i$, and the output resistance R_o.

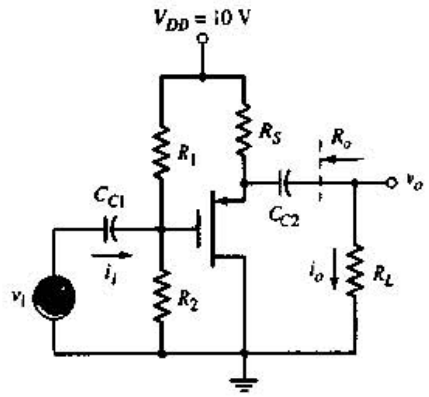

Figure P6.24

6.25 Consider the source-follower circuit in Figure P6.25 with transistor parameters $V_{TN} = 1.2\,\text{V}$, $K_n = 1\,\text{mA/V}^2$, and $\lambda = 0.01\,\text{V}^{-1}$. If $I_Q = 1\,\text{mA}$, determine the small-signal voltage gain $A_v = v_o/v_i$ and the output resistance R_o.

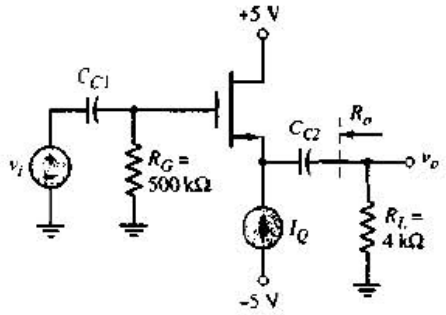

Figure P6.25

6.26 For the source-follower circuit shown in Figure P6.25, the transistor parameters are: $V_{TN} = 1\,\text{V}$, $K_n' = 60\,\mu\text{A/V}^2$, and $\lambda = 0$. The small-signal voltage gain is to be $A_v = v_o/v_i = 0.95$. (a) Determine the required width-to-length ratio (W/L) for $I_Q = 4\,\text{mA}$. (b) Determine the required I_Q if $(W/L) = 60$.

***D6.27** In the source-follower circuit in Figure P6.27 with a depletion NMOS transistor, the device parameters are: $V_{TN} = -2\,\text{V}$, $K_n = 5\,\text{mA/V}^2$, and $\lambda = 0.01\,\text{V}^{-1}$. Design the circuit such that $I_{DQ} = 5\,\text{mA}$. Find the small-signal voltage gain $A_v = v_o/v_i$ and the output resistance R_o.

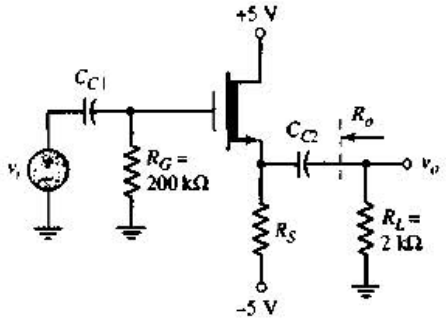

Figure P6.27

6.28 Consider the circuit in Figure P6.27. Let $R_S = 10\,\text{k}\Omega$ and $\lambda = 0$. The open-circuit voltage gain ($R_L = \infty$) is $A_v = v_o/v_i = 0.90$. Determine g_m and R_o. Determine the value of the voltage gain if a load resistor $R_L = 2\,\text{k}\Omega$ is connected.

D6.29 For the source-follower circuit in Figure P6.27, the transistor parameters are: $V_{TN} = -2\,\text{V}$, $K_n = 4\,\text{mA/V}^2$, and $\lambda = 0$. Design the circuit such that $R_o \leq 200\,\Omega$. Determine the resulting small-signal voltage gain.

6.30 The current source in the source-follower circuit in Figure P6.30 is $I_Q = 5\,\text{mA}$ and the transistor parameters are: $V_{TP} = -2\,\text{V}$, $K_p = 5\,\text{mA/V}^2$, and $\lambda = 0$. (a) Determine the output resistance R_o. (b) Determine the value of R_L that reduces the small-signal voltage gain to one-half the open-circuit ($R_L = \infty$) value.

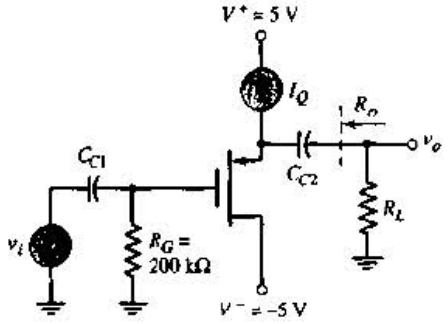

Figure P6.30

6.31 Consider the source-follower circuit shown in Figure P6.31. The most negative output signal voltage occurs when the transistor just cuts off. Show that this output voltage $v_o(\text{min})$ is given by

$$v_o(\text{min}) = \frac{-I_{DQ}R_S}{1 + \dfrac{R_S}{R_L}}$$

Show that the corresponding input voltage is given by

$$v_i(\text{min}) = -\frac{I_{DQ}}{g_m}(1 + g_m(R_S \| R_L))$$

D6.32 The transistor in the circuit in Figure P6.32 has parameters $V_{TN} = 1\,\text{V}$, $K_n = 1\,\text{mA/V}^2$, and $\lambda = 0$. The circuit parameters are $V_{DD} = 5\,\text{V}$ and $R_i = 300\,\text{k}\Omega$. (a) Design the circuit such that $I_{DQ} = 1.7\,\text{mA}$ and $V_{DSQ} = 3\,\text{V}$. (b) Determine the small-signal voltage gain $A_v = v_o/v_i$ and the output resistance R_o.

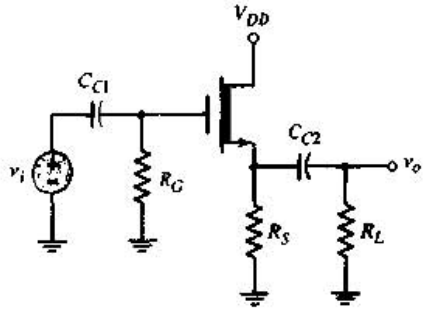

Figure P6.31

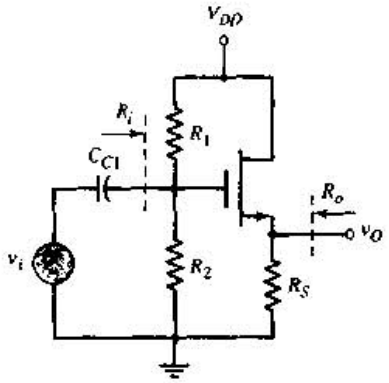

Figure P6.32

Section 6.5 The Common-Gate Configuration

6.33 For the common-gate circuit in Figure P6.33, the NMOS transistor parameters are: $V_{TN} = 1\,\text{V}$, $K_n = 3\,\text{mA/V}^2$, and $\lambda = 0$. (a) Determine I_{DQ} and V_{DSQ}. (b) Calculate g_m and r_o. (c) Find the small-signal voltage gain $A_v = v_o/v_i$.

6.34 Consider the PMOS common-gate circuit in Figure P6.34. The transistor parameters are: $V_{TP} = -1\,\text{V}$, $K_p = 0.5\,\text{mA/V}^2$, and $\lambda = 0$. (a) Determine R_S and R_D such that $I_{DQ} = 0.75\,\text{mA}$ and $V_{SDQ} = 6\,\text{V}$. (b) Determine the input impedance R_i and

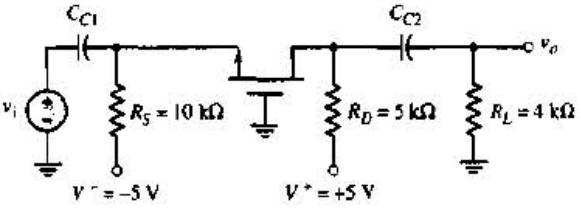

Figure P6.33

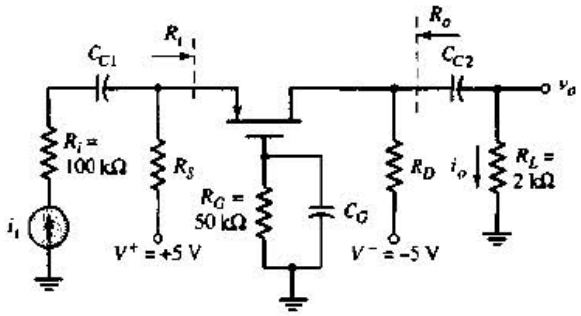

Figure P6.34

the output impedance R_o. (c) Determine the load current i_o and the output voltage v_o, if $i_i = 5 \sin \omega t\ \mu\text{A}$.

6.35 The parameters of the transistor in the circuit in Figure 6.34 in the text are: $V_{TN} = 2\ \text{V}$, $K_n = 4\ \text{mA/V}^2$, and $\lambda = 0$. The circuit parameters are: $V^+ = 10\ \text{V}$, $V^- = -10\ \text{V}$, $R_G = 100\ \text{k}\Omega$, $R_L = 2\ \text{k}\Omega$, and $I_Q = 5\ \text{mA}$. (a) Find R_D such that $V_{DSQ} = 12\ \text{V}$. (b) Calculate g_m and R_i. (c) Determine the small-signal voltage gain $A_v = v_o/v_i$.

6.36 For the common-gate amplifier in Figure 6.37 in the text, the PMOS transistor parameters are: $V_{TP} = -2\ \text{V}$, $K_p = 2\ \text{mA/V}^2$, and $\lambda = 0$. The circuit parameters are: $V^+ = 10\ \text{V}$, $V^- = -10\ \text{V}$, $R_G = 200\ \text{k}\Omega$, and $R_L = 10\ \text{k}\Omega$. (a) Determine R_S and R_D such that $I_{DQ} = 3\ \text{mA}$ and $V_{SDQ} = 10\ \text{V}$. (b) Determine the small-signal voltage gain $A_v = v_o/v_i$.

Section 6.7 Amplifiers with MOSFET Load Devices

D6.37 Consider the NMOS amplifier with saturated load in Figure 6.39(a). The transistor parameters are: $V_{TND} = V_{TNL} = 2\ \text{V}$, $k_n' = 60\ \mu\text{A/V}^2$, $\lambda = 0$, and $(W/L)_L = 0.5$. Let $V_{DD} = 10\ \text{V}$. (a) Design the circuit such that the small-signal voltage gain is $|A_v| = 5$ and the Q-point is in the center of the saturation region. (b) Determine I_{DQ} and the dc value of v_o.

***6.38** For the NMOS amplifier with depletion load in Figure 6.43(a), the transistor parameters are: $V_{TND} = 1.2\ \text{V}$, $V_{TNL} = -2\ \text{V}$, $K_{nD} = 0.5\ \text{mA/V}^2$, $K_{nL} = 0.1\ \text{mA/V}^2$, and $\lambda_D = \lambda_L = 0.02\ \text{V}^{-1}$. Let $V_{DD} = 10\ \text{V}$. (a) Determine V_{GS} such that the Q-point is in the middle of the saturation region. (b) Calculate I_{DQ} and the dc value of v_o. (c) Determine the small-signal voltage gain.

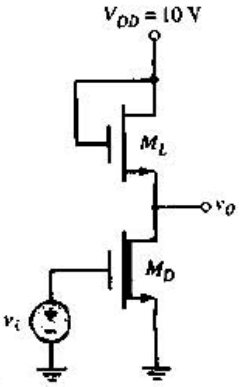

Figure P6.40

6.39 Consider a saturated load device in which the gate and drain of an enhancement mode MOSFET are connected together. The transistor drain current becomes zero when $V_{DS} = 1.5\ \text{V}$. When $V_{DS} = 3\ \text{V}$, the drain current is $0.8\ \text{mA}$. Determine the small-signal resistance at this operating point.

6.40 The parameters of the transistors in the circuit in Figure P6.40 are $V_{TND} = -1\ \text{V}$, $K_{nD} = 0.5\ \text{mA/V}^2$ for transistor M_D, and $V_{TNL} = +1\ \text{V}$, $K_{nL} = 30\ \mu\text{A/V}^2$ for transistor M_L. Assume $\lambda = 0$ for both transistors. (a) Calculate the quiescent drain current I_{DQ} and the dc value of the output voltage. (b) Determine the small-signal voltage gain $A_v = v_o/v_i$ about the Q-point.

6.41 A source-follower circuit with a saturated load is shown in Figure P6.41. The transistor parameters are $V_{TND} = 1\ \text{V}$, $K_{nD} = 1\ \text{mA/V}^2$ for M_D, and $V_{TNL} = 1\ \text{V}$, $K_{nL} = 0.1\ \text{mA/V}^2$ for M_L. Assume $\lambda = 0$ for both transistors. Let $V_{DD} = 9\ \text{V}$. (a) Determine

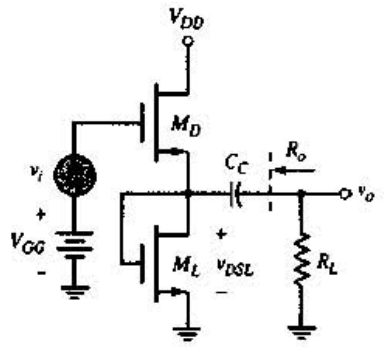

Figure P6.41

V_{GG} such that the quiescent value of v_{DSL} is 4 V. (b) Show that the small-signal open-circuit ($R_L = \infty$) voltage gain about this Q-point is given by $A_v = 1/[1 + \sqrt{K_{nL}/K_{nD}}]$. (c) Calculate the small-signal voltage gain for $R_L = 4\,\text{k}\Omega$.

6.42 For the source-follower circuit with a saturated load, as shown in Figure P6.41, assume the same transistor parameters as given in Problem 6.41. (a) Determine the small-signal voltage gain if $R_L = 10\,\text{k}\Omega$. (b) Determine the small-signal output resistance R_o.

Section 6.8 Multistage Amplifiers

***D6.43** The transistor parameters in the circuit in Figure P6.43 are: $K_{n1} = 0.1\,\text{mA/V}^2$, $K_{p2} = 1.0\,\text{mA/V}^2$, $V_{TN1} = +2\,\text{V}$, $V_{TD2} = -2\,\text{V}$, and $\lambda_1 = \lambda_2 = 0$. The circuit parameters are: $V_{DD} = 10\,\text{V}$, $R_{S1} = 4\,\text{k}\Omega$, and $R_{\text{in}} = 200\,\text{k}\Omega$. (a) Design the circuit such that $I_{DQ1} = 0.4\,\text{mA}$, $I_{DQ2} = 2\,\text{mA}$, $V_{DSQ1} = 4\,\text{V}$, and $V_{SDQ2} = 5\,\text{V}$. (b) Calculate the small-signal voltage gain $A_v = v_o/v_i$. (c) Determine the maximum symmetrical swing in the output voltage.

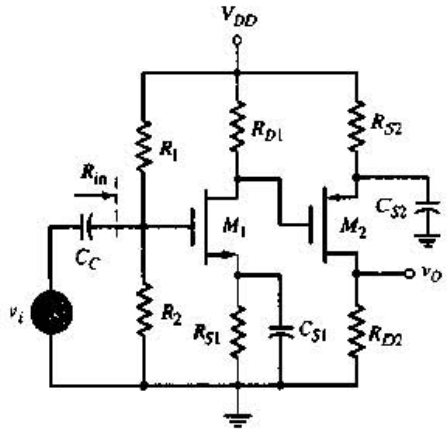

Figure P6.43

D6.44 The transistor parameters in the circuit in Figure P6.43 are the same as those given in Problem 6.43. The circuit parameters are: $V_{DD} = 10\,\text{V}$, $R_{S1} = 1\,\text{k}\Omega$, $R_{\text{in}} = 200\,\text{k}\Omega$, $R_{D2} = 2\,\text{k}\Omega$, and $R_{S2} = 0.5\,\text{k}\Omega$. (a) Design the circuit such that the Q-point of M_2 is in the center of the saturation region and $I_{DQ1} = 0.4\,\text{mA}$. (b) Determine the resulting values of I_{DQ2}, V_{SDQ2}, and V_{DSQ1}. (c) Determine the resulting small-signal voltage gain.

D6.45 Consider the circuit in Figure P6.45 with transistor parameters $K_{n1} = K_{n2} = 200\,\mu A/V^2$, $V_{TN1} = V_{TN2} = 0.8\,V$, and $\lambda_1 = \lambda_2 = 0$. (a) Design the circuit such that $V_{DSQ2} = 7\,V$ and $R_{in} = 400\,k\Omega$. (b) Determine the resulting values of I_{DQ1}, I_{DQ2}, and V_{DSQ1}. (c) Calculate the resulting small-signal voltage gain $A_v = v_o/v_i$ and the output resistance R_o.

6.46 For the circuit in Figure P6.46, the transistor parameters are: $K_{n1} = K_{n2} = 4\,mA/V^2$, $V_{TN1} = V_{TN2} = 2\,V$, and $\lambda_1 = \lambda_2 = 0$. (a) Determine I_{DQ1}, I_{DQ2}, V_{DSQ1}, and V_{DSQ2}. (b) Determine g_{m1} and g_{m2}. (c) Determine the overall small-signal voltage gain $A_v = v_o/v_i$.

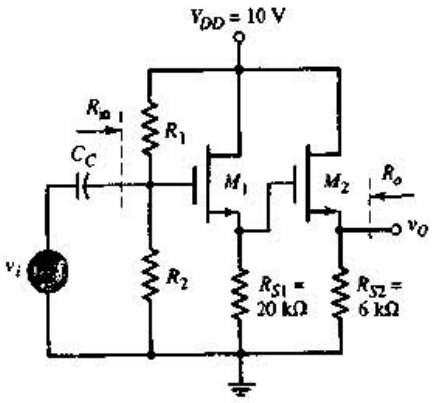

Figure P6.45

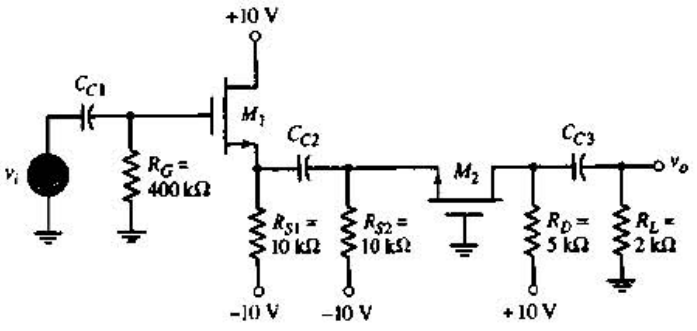

Figure P6.46

D6.47 For the cascode circuit in Figure 6.50 in the text, the transistor parameters are: $V_{TN1} = V_{TN2} = 1\,V$, $K_{n1} = K_{n2} = 2\,mA/V^2$, and $\lambda_1 = \lambda_2 = 0$. (a) Let $R_S = 1.2\,k\Omega$ and $R_1 + R_2 + R_3 = 500\,k\Omega$. Design the circuit such that $I_{DQ} = 3\,mA$ and $V_{DSQ1} = V_{DSQ2} = 2.5\,V$. (b) Determine the small-signal voltage gain $A_v = v_o/v_i$.

D6.48 The supply voltages to the cascode circuit in Figure 6.50 in the text are changed to $V^+ = 10\,V$ and $V^- = -10\,V$. The transistor parameters are: $K_{n1} = K_{n2} = 4\,mA/V^2$, $V_{TN1} = V_{TN2} = 1.5\,V$, and $\lambda_1 = \lambda_2 = 0$. (a) Let $R_S = 2\,k\Omega$, and assume the current in the bias resistors is 0.1 mA. Design the circuit such that $I_{DQ} = 5\,mA$ and $V_{DSQ1} = V_{DSQ2} = 3.5\,V$. (b) Determine the resulting small-signal voltage gain.

Section 6.9 Basic JFET Amplifiers

6.49 Consider the JFET amplifier in Figure 6.53 with transistor parameters $I_{DSS} = 6\,mA$, $V_P = -3\,V$, and $\lambda = 0.01\,V^{-1}$. Let $V_{DD} = 10\,V$. (a) Determine R_D and V_{GS} such that $I_{DQ} = 4\,mA$ and $V_{DSQ} = 6\,V$. (b) Determine g_m and r_o at the Q-point. (c) Determine the small-signal voltage gain $A_v = v_o/v_i$ where v_o is the time-varying portion of the output voltage v_O.

6.50 For the JFET amplifier in Figure P6.50, the transistor parameters are: $I_{DSS} = 2\,mA$, $V_P = -2\,V$, and $\lambda = 0$. Determine g_m, $A_v = v_o/v_i$, and $A_i = i_o/i_i$.

D6.51 The parameters of the transistor in the JFET common-source amplifier shown in Figure P6.51 are: $I_{DSS} = 8\,mA$, $V_P = -4.2\,V$, and $\lambda = 0$. Let $V_{DD} = 20\,V$ and $R_L = 16\,k\Omega$. Design the circuit such that $V_S = 2\,V$, $R_1 + R_2 = 100\,k\Omega$, and the Q-point is at $I_{DQ} = I_{DSS}/2$ and $V_{DSQ} = V_{DD}/2$.

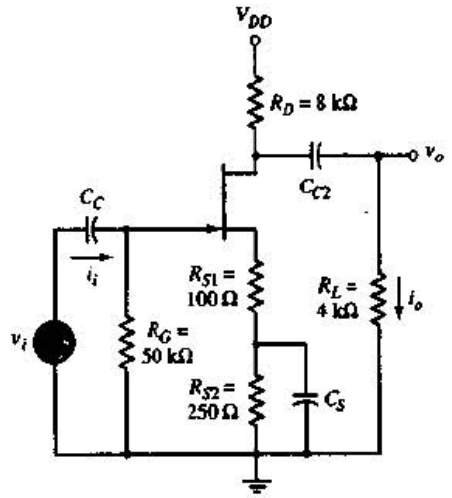

Figure P6.50

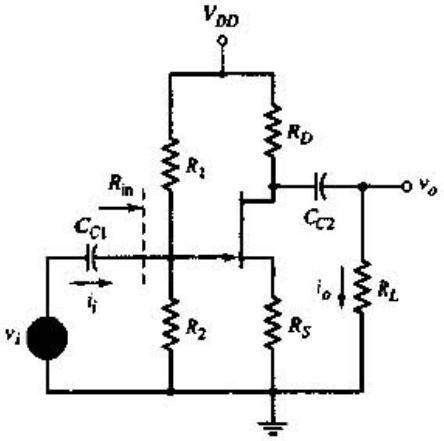

Figure P6.51

***D6.52** Consider the source-follower JFET amplifier in Figure P6.52 with transistor parameters $I_{DSS} = 10\,\text{mA}$, $V_P = -5\,\text{V}$, and $\lambda = 0.01\ \text{V}^{-1}$. Let $V_{DD} = 12\,\text{V}$ and $R_L = 0.5\,\text{k}\Omega$. (a) Design the circuit such that $R_{in} = 100\,\text{k}\Omega$, and the Q-point is at $I_{DQ} = I_{DSS}/2$ and $V_{DSQ} = V_{DD}/2$. (b) Determine the resulting small-signal voltage gain $A_v = v_o/v_i$ and the output resistance R_o.

6.53 For the p-channel JFET source-follower circuit in Figure P6.53, the transistor parameters are: $I_{DSS} = 2\,\text{mA}$, $V_P = +1.75\,\text{V}$, and $\lambda = 0$. (a) Determine I_{DQ} and V_{SDQ}. (b) Determine the small-signal gains $A_v = v_o/v_i$ and $A_i = i_o/i_i$. (c) Determine the maximum symmetrical swing in the output voltage.

D6.54 The p-channel JFET common-source amplifier in Figure P6.54 has transistor parameters $I_{DSS} = 8\,\text{mA}$, $V_P = 4\,\text{V}$, and $\lambda = 0$. Design the circuit such that $I_{DQ} = 4\,\text{mA}$, $V_{SDQ} = 7.5\,\text{V}$, $A_v = v_o/v_i = -3$, and $R_1 + R_2 = 400\,\text{k}\Omega$.

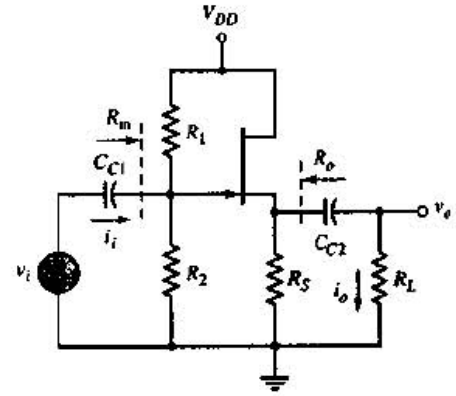

Figure P6.52

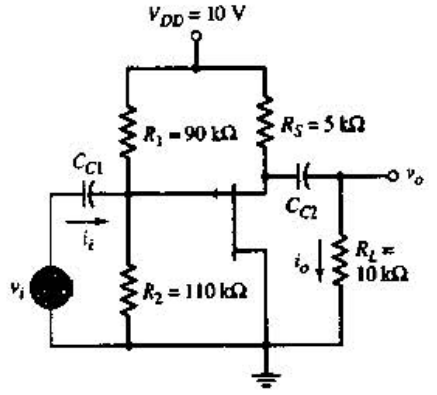

Figure P6.53

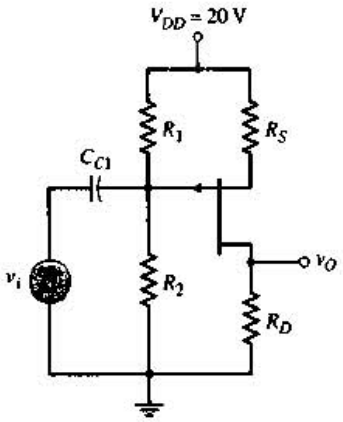

Figure P6.54

COMPUTER SIMULATION PROBLEMS

6.55 Consider the circuit in Figure 6.22 with transistor parameters given in Example 6.6. Using a computer analysis, investigate the effect of the channel-length modulation parameter λ and the body-effect parameter γ on the small-signal voltage gain.

6.56 Using a computer analysis, investigate the effect of the transistor parameters λ and γ on the small-signal voltage gain and output resistance of the source-follower circuit in Figure 6.28. The circuit and transistor parameters are given in Example 6.7.

6.57 For the common-gate circuit in Figure 6.34 the circuit and transistor parameters are as given in Example 6.10. Using a computer analysis, determine the small-signal voltage gain, current gain, input resistance R_i, and output resistance (looking into the drain of the transistor). As part of the analysis, investigate the effect of the transistor parameters λ and γ on the circuit characteristics.

6.58 Perform a computer analysis of Exercise 6.22, including the body effect. Determine the change in the small-signal voltage gain when the body effect is included. If the dc output voltage is approximately 2.5 V, determine the required change in the dc bias on the driver transistor when the body effect is included.

6.59 Repeat Problem 6.58 for Exercise 6.24.

DESIGN PROBLEMS

[Note: Each design should be correlated with a computer analysis.]

***D6.60** A discrete common-source circuit with the configuration shown in Figure 6.16 is to be designed to provide a voltage gain of 20 and a symmetrical output voltage swing. The power supply voltage is $V_{DD} = 5$ V, the output resistance of the signal source is 1 kΩ, and the transistor parameters are: $V_{TN} = 0.8$ V, $k_n' = 40\,\mu\text{A/V}^2$, and $\lambda = 0.01\ \text{V}^{-1}$. Plot W/L and R_D versus quiescent drain current. Determine W/L and R_D for $I_{DQ} = 0.1$ mA.

***D6.61** For a common-gate amplifier in Figure 6.37 the available power supplies are ±10 V, the output resistance of the signal source is 200 Ω, and the input resistance of the amplifier is to be 200 Ω. The transistor parameters are: $k_p' = 30\,\mu\text{A/V}^2$, $V_{TP} = -2$ V, and $\lambda = 0$. The output load resistance is $R_L = 5$ kΩ. Design the circuit such that the output voltage has a peak-to-peak symmetrical swing of at least 5 V.

***D6.62** A source-follower amplifier with the general configuration shown in Figure 6.32 is to be designed. The available power supplies are $\pm 12\,V$, and the transistor parameters are: $V_{TN} = 1.5\,V$, $k_n' = 40\,\mu A/V^2$, and $\lambda = 0$. The load resistance is $R_L = 100\,\Omega$. Design the circuit such that 200 mW of signal power is delivered to the load. As part of the design, a constant-current source circuit is also to be designed.

***D6.63** For an NMOS amplifier with a depletion load, such as shown in Figure 6.43(a), the available power supplies are $\pm 5\,V$, and the transistor parameters are: $V_{TN}(M_D) = +1\,V$, $V_{TN}(M_L) = -2\,V$, $k_n' = 40\,\mu A/V^2$, $\lambda = 0.01\,V^{-1}$, and $\gamma = 0.35\,V^{1/2}$. Design the circuit such that the small-signal voltage gain is at least $|A_v| = 200$ when the output is an open circuit. Use a constant-current source to establish the quiescent Q-point, and couple the signal source v_i directly to the gate of M_D.

***D6.64** For the cascode circuit shown in Figure 6.50, the transistor parameters are: $V_{TN} = 1\,V$, $k_n' = 40\,\mu A/V^2$, and $\lambda = 0$. Design the circuit such that the minimum open-circuit voltage gain is 10. Determine the maximum symmetrical swing in the output voltage.

CHAPTER

7

Frequency Response

7.0 PREVIEW

Thus far in our linear amplifier analyses, we have assumed that coupling capacitors and bypass capacitors act as short circuits to the signal voltages and open circuits to dc voltages. However, capacitors do not change instantaneously from a short circuit to an open circuit as the frequency approaches zero. We have also assumed that transistors are ideal in that output signals respond instantaneously to input signals. However, there are internal capacitances in both the bipolar transistor and field-effect transistor that affect the frequency response. The major goal of this chapter is to determine the frequency response of amplifier circuits due to circuit capacitors and transistor capacitances.

Initially, we derive transfer functions, using the complex frequency s, of several passive circuits as a basic review of frequency response. We introduce Bode plots of the transfer function magnitude and phase, and a time constant technique for determining the corner, or 3 dB, frequencies of the circuit response. The goal of this analysis is to help the reader become comfortable with basic frequency response analysis and sketching Bode plots. When there is more than one capacitor in a circuit, computer simulation becomes an attractive analysis tool for determining the frequency response.

The frequency response of electronic amplifiers is analyzed, taking into account various circuit capacitors, to determine the bandwidth of the circuit. The parameters that affect low-frequency cutoff and high-frequency cutoff are determined. These parameters become important in the design of amplifiers with specified frequency response characteristics. By knowing the position or function of a capacitor in a circuit, the reader should be able to easily identify whether the low-frequency or high-frequency characteristics will be affected.

The capacitances in the transistor structure are identified and the resulting frequency response of the transistor itself is analyzed. The combination of circuit capacitors and transistor effects results in amplifiers with specified bandwidths, or frequency ranges over which the amplifier can produce output signals. Much of the chapter deals with analysis. However, the results of the analyses will aid in the design of amplifiers with specific bandwidth requirements.

7.1 AMPLIFIER FREQUENCY RESPONSE

All amplifier gain factors are functions of signal frequency. These gain factors include voltage, current, transconductance, and transresistance. Up to this point, we have assumed that the signal frequency is high enough that coupling and bypass capacitors can be treated as short circuits and, at the same time, we have assumed that the signal frequency is low enough that parasitic, load, and transistor capacitances can be treated as open circuits. In this chapter, we consider the amplifier response over the entire frequency range.

In general, an amplifier gain factor versus frequency will resemble that shown in Figure 7.1.[1] Both the gain factor and frequency are plotted on logarithmic scales (the gain factor in terms of decibels). Three frequency ranges, low, midband, and high, are indicated. In the **low-frequency range**, $f < f_L$, the gain decreases as the frequency decreases because of coupling and bypass capacitor effects. In the **high-frequency range**, $f > f_H$, stray capacitance and transistor capacitance effects cause the gain to decrease as the frequency increases. The **midband range** is the region where coupling and bypass capacitors act as short circuits, and stray and transistor capacitances act as open circuits. In this region, the gain is almost a constant. As we will show, the gain at $f = f_L$ and at $f = f_H$ is 3 dB less than the maximum midband gain. The bandwidth of the amplifier (in Hz) is defined as $f_{BW} = f_H - f_L$.

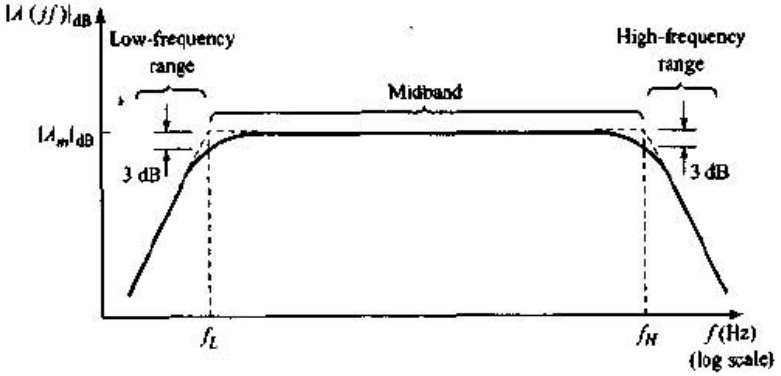

Figure 7.1 . Amplifier gain versus frequency

For an audio amplifier, for example, signal frequencies in the range of $20\,\text{Hz} < f < 20\,\text{kHz}$ need to be amplified equally so as to reproduce the sound as accurately as possible. Therefore, in the design of a good audio amplifier, the frequency f_L must be designed to be less than 20 Hz and f_H must be designed to be greater than 20 kHz.

7.1.1 Equivalent Circuits

Each capacitor in a circuit is important to only one end of the frequency spectrum. For this reason, we can develop specific equivalent circuits that

[1] In many references, the gain is plotted as a function of the radian frequency ω. All curves in this chapter, for consistency, will be plotted as a function of cyclical frequency f (Hz). We note that $\omega = 2\pi f$. The amplifier gain is also plotted in terms of decibels (dB), where $|A|_{dB} = 20 \log_{10} |A|$.

apply to the low-frequency range, to midband, and to the high-frequency range.

Midband Range

The equivalent circuits used for calculations in the midband range are the same as those considered up to this point in the text. As already mentioned, the coupling and bypass capacitors in this region are treated as short circuits. The stray and transistor capacitances are treated as open circuits. In this frequency range, there are no capacitances in the equivalent circuit. These circuits are referred to as midband equivalent circuits.

Low-Frequency Range

In this frequency range, we use a low-frequency equivalent circuit. In this range, coupling and bypass capacitors must be included in the equivalent circuit and in the amplification factor equations. The stray and transistor capacitances are treated as open circuits. The mathematical expressions obtained for the amplification factor in this frequency range must approach the midband results as f approaches the midband frequency range, since in this limit the capacitors approach short-circuit conditions.

High-Frequency Range

In the high-frequency range, we use a high-frequency equivalent circuit. In this region, coupling and bypass capacitors are treated as short circuits. The transistor and any parasitic or load capacitances must be taken into account in this equivalent circuit. The mathematical expressions obtained for the amplification factor in this frequency range must approach the midband results as f approaches the midband frequency range, since in this limit the capacitors approach open-circuit conditions.

7.1.2 Frequency Response Analysis

Using the three equivalent circuits just considered rather than a complete circuit is an approximation technique that produces useful hand-analysis results while avoiding complex transfer functions. This technique is valid if there is a large separation between f_L and f_H, that is $f_H \gg f_L$. This condition is satisfied in many electronic circuits that we will consider.

Computer simulations, such as PSpice, can take into account all capacitances and can produce frequency response curves that are more accurate than the hand-analysis results. However, the computer results do not provide any physical insight into a particular result and hence do not provide any suggestions as to design changes that can be made to improve a particular frequency response. A hand analysis can provide insight into the "whys and wherefores" of a particular response. This basic understanding can then lead to a better circuit design.

In the next section, we introduce two simple circuits to begin our frequency analysis study. We initially derive the mathematical expressions relating output voltage to input voltage (transfer function) as a function of signal frequency. From these functions, we can develop the response curves. The two frequency

response curves give the magnitude of the transfer function versus frequency and the phase of the transfer function versus frequency. The phase response relates the phase of the output signal to the phase of the input signal.

We will then develop a technique by which we can easily sketch the frequency response curves without resorting to a full analysis of the transfer function. This simplified approach will lead to a general understanding of the frequency response of electronic circuits. We will then rely on a computer simulation to provide more detailed calculations when required.

7.2 SYSTEM TRANSFER FUNCTIONS

The frequency response of a circuit is usually determined by using the **complex frequency** s. Each capacitor is represented by its complex impedance, $1/sC$, and each inductor is represented by its complex impedance, sL. The circuit equations are then formulated in the usual way. Using the complex frequency, the mathematical expressions obtained for voltage gain, current gain, input impedance, or output impedance are ratios of polynomials in s.

We will be concerned in many cases with system transfer functions. These will be in the form of ratios of, for example, output voltage to input voltage (voltage transfer function) or output current to input voltage (transconductance function). The four general transfer functions are listed in Table 7.1.

Once a transfer function is found, we can find the result of a steady-state sinusoidal excitation by setting $s = j\omega = j2\pi f$. The ratio of polynomials in s then reduces to a complex number for each frequency f. The complex number can be reduced to a magnitude and a phase.

Table 7.1 Transfer functions of the complex frequency s

Name of function	Expression
Voltage transfer function	$T(s) = V_o(s)/V_i(s)$
Current transfer function	$I_o(s)/I_i(s)$
Transresistance function	$V_o(s)/I_i(s)$
Transconductance function	$I_o(s)/V_i(s)$

7.2.1 s-Domain Analysis

In general, a transfer function in the s-domain can be expressed in the form

$$T(s) = K\frac{(s - z_1)(s - z_2)\cdots(s - z_m)}{(s - p_1)(s - p_2)\ldots(s - p_n)} \tag{7.1}$$

where K is a constant, $z_1, z_2, \ldots, z_m$ are the transfer function "zeros," and $p_1, p_2, \ldots, p_n$ are the transfer function "poles." When the complex frequency is equal to a zero, $s = z_i$, the transfer function is zero; when the complex frequency is equal to a pole, $s = p_i$, the transfer function diverges and becomes infinite. The transfer function can be evaluated for physical frequencies by replacing s with $j\omega$. In general, the resulting transfer function $T(j\omega)$ is a complex function, that is, its magnitude and phase are both functions of frequency. These topics are usually discussed in a basic circuit analysis course.

For a simple transfer function of the form

$$T(s) = \frac{K}{s + \omega_o} \tag{7.2(a)}$$

we can rearrange the terms and write the function as

$$T(s) = K_1\left(\frac{1}{1 + s\tau_1}\right) \tag{7.2(b)}$$

where τ_1 is a **time constant**. Other transfer functions may be written as

$$T(s) = K_2\left(\frac{s\tau_2}{1 + s\tau_2}\right) \tag{7.2(c)}$$

where τ_2 is also a time constant. In most cases, we will write the transfer functions in terms of the time constants.

To introduce the frequency response analysis of transistor circuits, we will examine the circuits shown in Figures 7.2 and 7.3. The voltage transfer function for the circuit in Figure 7.2 can be expressed in a voltage divider format, as follows:

$$\frac{V_o(s)}{V_i(s)} = \frac{R_P}{R_S + R_P + \dfrac{1}{sC_S}} \tag{7.3}$$

The elements R_S and C_S are in series between the input and output signals, and the element R_P is in parallel with the output signal. Equation (7.3) can be written in the form

$$\frac{V_o(s)}{V_i(s)} = \frac{sR_PC_S}{1 + s(R_S + R_P)C_S} \tag{7.4}$$

which can be rearranged and written as

$$\frac{V_o(s)}{V_i(s)} = \left(\frac{R_P}{R_S + R_P}\right)\left[\frac{s(R_S + R_P)C_S}{1 + s(R_S + R_P)C_S}\right] = K_2\left(\frac{s\tau}{1 + s\tau}\right) \tag{7.5}$$

In this equation, the time constant is

$$\tau = (R_S + R_P)C_S$$

Writing a Kirchhoff current law (KCL) equation at the output node, we can determine the voltage transfer function for the circuit shown in Figure 7.3, as follows:

$$\frac{V_o - V_i}{R_S} + \frac{V_o}{R_P} + \frac{V_o}{(1/sC_P)} = 0 \tag{7.6}$$

In this case, the element R_S is in series between the input and output signals, and the elements R_P and C_P are in parallel with the output signal. Rearranging the terms in Equation (7.6) produces

$$\frac{V_o(s)}{V_i(s)} = \left(\frac{R_P}{R_S + R_P}\right)\left[\frac{1}{1 + s\left(\dfrac{R_SR_P}{R_S + R_P}\right)C_P}\right] \tag{7.7(a)}$$

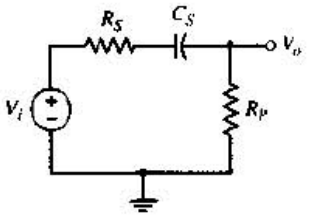

Figure 7.2 Series coupling capacitor circuit

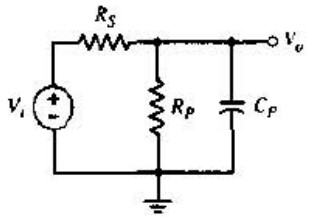

Figure 7.3 Parallel load capacitor circuit

or

$$\frac{V_o(s)}{V_i(s)} = \left(\frac{R_P}{R_S + R_P}\right)\left[\frac{1}{1 + s(R_S \| R_P)C_P}\right] \tag{7.7(b)}$$

In Equation (7.7(b)), the time constant is

$$\tau = (R_S \| R_P)C_P$$

7.2.2 First-Order Functions

In our hand analysis of transistor circuits in this chapter, we will, in general, limit ourselves to the consideration of only one capacitance at a time. We will therefore be dealing with **first-order transfer functions** that, in most cases, will have the general form of either Equation (7.5) or (7.7(b)). This simplified analysis will allow us to present the frequency responses of specific capacitances and of the transistors themselves. We will then compare our hand analysis results with more rigorous solutions, using a computer simulation.

7.2.3 Bode Plots

A simplified technique for obtaining approximate plots of the magnitude and phase of a transfer function, given the poles and zeros or the equivalent time constants, was developed by H. Bode, and the resulting diagrams are called **Bode plots**.

Bode Plot for Figure 7.2

For the transfer function in Equation (7.5), for example, if we replace s by $j\omega$ and define a time constant τ_s as

$$\tau_s = (R_S + R_P)C_S$$

we have

$$T(j\omega) = \frac{V_o(j\omega)}{V_i(j\omega)} = \left(\frac{R_P}{R_S + R_P}\right)\left[\frac{j\omega\tau_S}{1 + j\omega\tau_S}\right] \tag{7.8}$$

The magnitude of Equation (7.8) is

$$|T(j\omega)| = \left(\frac{R_P}{R_S + R_P}\right)\left[\frac{\omega\tau_S}{\sqrt{1 + \omega^2\tau_S^2}}\right] \tag{7.9(a)}$$

or

$$|T(jf)| = \left(\frac{R_P}{R_S + R_P}\right)\left[\frac{2\pi f\tau_S}{\sqrt{1 + (2\pi f\tau_S)^2}}\right] \tag{7.9(b)}$$

We can develop the Bode plot of the gain magnitude versus frequency. We may note that $|T(jf)|_{dB} = 20\log_{10}|T(jf)|$. From Equation (7.9(b)), we can write

$$|T(jf)|_{\text{dB}} = 20\log_{10}\left[\left(\frac{R_P}{R_S + R_P}\right) \cdot \frac{2\pi f \tau_S}{\sqrt{1 + (2\pi f \tau_S)^2}}\right] \tag{7.10(a)}$$

or

$$|T(jf)|_{\text{dB}} = 20\log_{10}\left(\frac{R_P}{R_S + R_P}\right) + 20\log_{10}(2\pi f \tau_S) - 20\log_{10}\sqrt{1 + (2\pi f \tau_S)^2} \tag{7.10(b)}$$

We can plot each term of Equation (7.10(b)) and then combine the three plots to form the final Bode plot of the gain magnitude.

Figure 7.4(a) is the plot of the first term of equation (7.10(b)), which is just a constant independent of frequency. We may note that, since $[R_P/(R_S + R_P)]$ is less than unity, the dB value is less than zero.

Figure 7.4(b) is the plot of the second term of Equation (7.10(b)). When $f = 1/2\pi\tau_S$, we have $20\log_{10}(1) = 0$. The slopes in Bode plot magnitudes are described in units of either dB/octave or dB/decade. An **octave** means that frequency is increased by a factor of two, and a **decade** implies that the

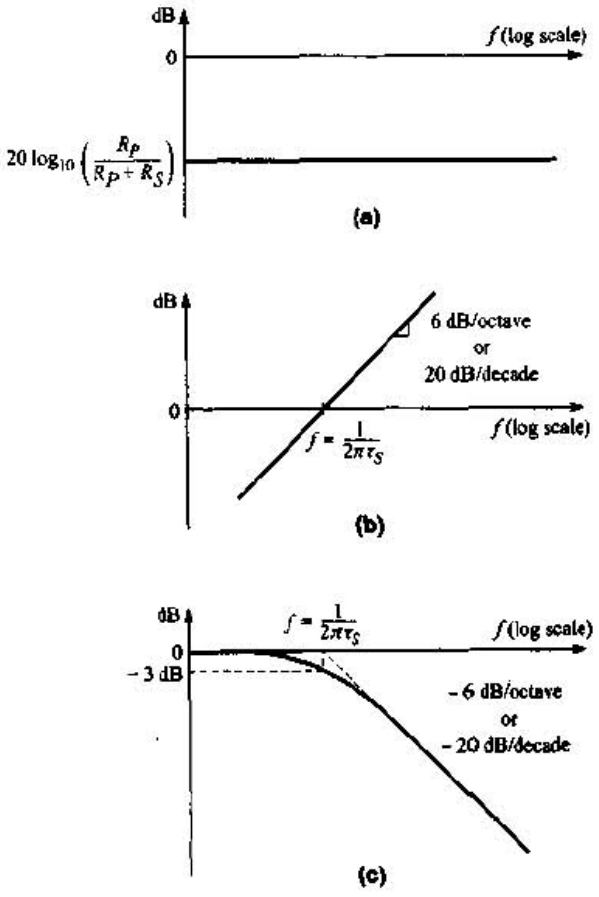

Figure 7.4 Plots of (a) the first term, (b) the second term, and (c) the third term of Equation (7.10(b))

frequency is increased by a factor of 10. The value of the function $20\log_{10}(2\pi f\tau_S)$ increases by a factor of $6.02 \cong 6$ dB for every factor of 2 increase in frequency, and the value of the function increases by a factor of 20 dB for every factor of 10 increase in frequency. Hence, we can consider a slope of 6 dB/octave or 20 dB/decade.

Figure 7.4(c) is the plot of the third term in Equation (7.10(b)). For $f \ll 1/2\pi\tau_S$, the value of the function is essentially 0 dB and when $f = 1/2\pi\tau_S$, the value is -3 dB. For $f \gg 1/2\pi\tau_S$, the function becomes $-20\log_{10}(2\pi f\tau_S)$, so the slope becomes -6 dB/octave or -20 dB/decade. A straight-line projection of this slope passes through 0 dB at $f = 1/2\pi\tau_S$. We can then approximate the Bode plot for this term by two straight line asymptotes intersecting at 0 dB and $f = 1/2\pi\tau_S$. This particular frequency is known as a **break-point frequency, corner frequency,** or **-3 dB frequency**.

The complete Bode plot of Equation (7.10(b)) is shown in Figure 7.5. For $f \gg 1/2\pi\tau_S$, the second and third terms of Equation (7.10(b)) cancel, and for $f \ll 1/2\pi\tau_S$, the large negative dB value from Figure 7.4(b) dominates.

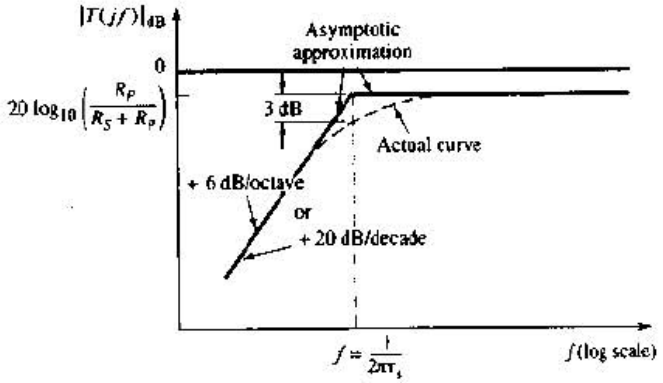

Figure 7.5 Bode plot of the voltage transfer function magnitude for the circuit in Figure 7.2

The transfer function given by Equation (7.9) is for the circuit shown in Figure 7.2. The series capacitor C_S is a coupling capacitor between the input and output signals. At a high enough frequency, capacitor C_S acts as a short circuit, and the output voltage, from a voltage divider, is

$$V_o = [R_P/(R_S + R_P)]\,V_i$$

For very low frequencies, the impedance of C_S approaches that of an open circuit, and the output voltage approaches zero. This circuit is called a **high-pass network** since the high-frequency signals are passed through to the output. We can now understand the form of the Bode plot shown in Figure 7.5.

The Bode plot of the phase function can be easily developed by recalling the relation between the rectangular and polar form of a complex number. We can write $A + jB = Ke^{j\theta}$, where $K = \sqrt{A^2 + B^2}$ and $\theta = \tan^{-1}(B/A)$. This relationship is shown in Figure 7.6.

For the function given in Equation (7.8), we can write the function in the form

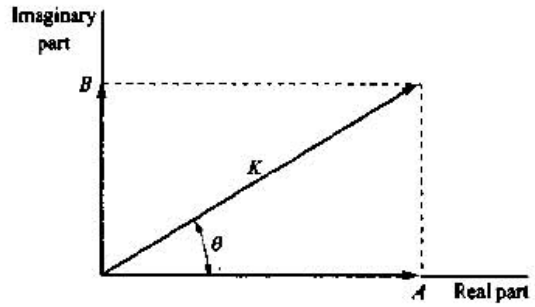

Figure 7.6 Relation between rectangular and polar forms of a complex number

$$T(jf) = \left(\frac{R_P}{R_S + R_P}\right) \cdot \left[\frac{j2\pi f\tau_S}{1 + j2\pi f\tau_S}\right] = \left[\left|\frac{R_P}{R_S + R_P}\right| e^{j\theta_1}\right] \frac{[|j2\pi f\tau_S| e^{j\theta_2}]}{[|1 + j2\pi f\tau_S| e^{j\theta_3}]} \tag{7.11(a)}$$

or

$$T(jf) = [K_1 e^{j\theta_1}] \frac{[K_2 e^{j\theta_2}]}{[K_3 e^{j\theta_3}]} = \frac{K_1 K_2}{K_3} e^{j(\theta_1 + \theta_2 - \theta_3)} \tag{7.11(b)}$$

The net phase of the function $T(jf)$ is then $\theta = \theta_1 + \theta_2 - \theta_3$.

Since the first term, $[R_P/(R_S + R_P)]$, is a positive real quantity, the phase is $\theta_1 = 0$. The second term, $(j2\pi f\tau_S)$, is purely imaginary so that the phase is $\theta_2 = 90°$. The third term is complex so that its phase is $\theta_3 = \tan^{-1}(2\pi f\tau_S)$. The net phase of the function is now

$$\theta = 90 - \tan^{-1}(2\pi f\tau_S) \tag{7.12}$$

For the limiting case of $f \to 0$, we have $\tan^{-1}(0) = 0$, and for $f \to \infty$, we have $\tan^{-1}(\infty) = 90°$. At the corner frequency of $f = 1/(2\pi\tau_S)$, the phase is $\tan^{-1}(1) = 45°$. The Bode plot of the phase of the function given in Equation (7.11(a)) is given in Figure 7.7. The actual plot as well as an asymptotic approximation is shown. The phase is especially important in feedback circuits since this can influence stability. We will see this effect in Chapter 12.

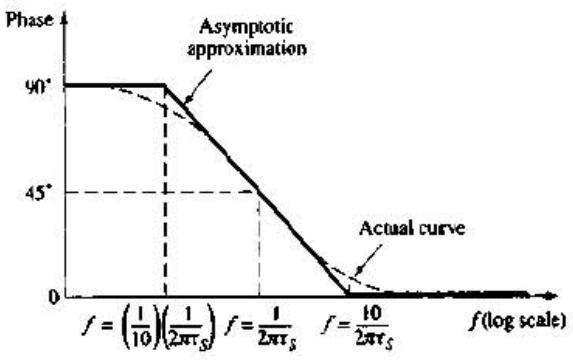

Figure 7.7 Bode plot of the voltage transfer function phase for the circuit in Figure 7.2

Bode Plot for Figure 7.3

The transfer function given by Equation (7.7(b)) is for the circuit that was shown in Figure 7.3. If we replace s by $s = j\omega = j2\pi f$ and define a time constant τ_P as $\tau_P = (R_S \| R_P)C_P$, then the transfer function is

$$T(jf) = \left(\frac{R_P}{R_S + R_P}\right)\left[\frac{1}{1 + j2\pi f \tau_P}\right] \tag{7.13}$$

The magnitude of Equation (7.13) is

$$|T(jf)| = \left(\frac{R_P}{R_S + R_P}\right) \cdot \left[\frac{1}{\sqrt{1 + (2\pi f \tau_P)^2}}\right] \tag{7.14}$$

A Bode plot of this magnitude expression is shown in Figure 7.8. The low-frequency asymptote is a horizontal line, and the high-frequency asymptote is a straight line with a slope of −20 dB/decade, or −6 dB/octave. The two asymptotes meet at the frequency $f = 1/2\pi\tau_P$, which is the corner, or 3 dB, frequency for this circuit. Again, the actual magnitude of the transfer function at the corner frequency differs from the maximum asymptotic value by 3 dB.

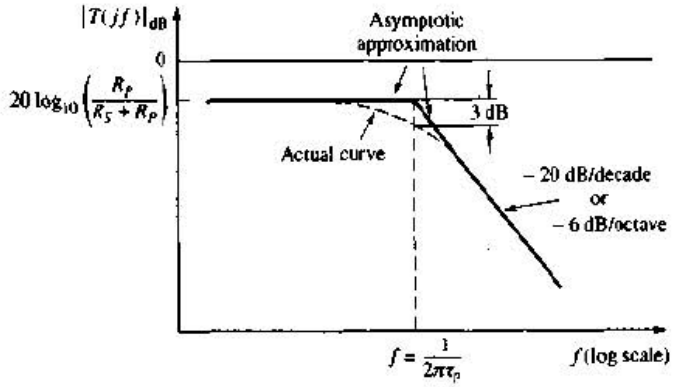

Figure 7.8 Bode plot of the voltage transfer function magnitude for the circuit in Figure 7.3

Again, the magnitude of the transfer function given by Equation (7.13) is for the circuit shown in Figure 7.3. The parallel capacitor C_P is a load, or parasitic, capacitance. At low frequencies, C_P acts as an open circuit, and the output voltage, from a voltage divider, is

$$V_o = [R_P/(R_S + R_P)]V_i$$

As the frequency increases, the magnitude of the impedance of C_P decreases and approaches that of a short circuit, and the output voltage approaches zero. This circuit is called a **low-pass network**, since the low-frequency signals are passed through to the output.

The phase of the transfer function given by Equation (7.13) is

$$\text{Phase} = -\angle \tan^{-1}(2\pi f \tau_P) \tag{7.15}$$

The Bode plot of the phase is shown in Figure 7.9. The phase is −45 degrees at the corner frequency and 0 degrees at the low-frequency asymptote, where C_P is effectively out of the circuit.

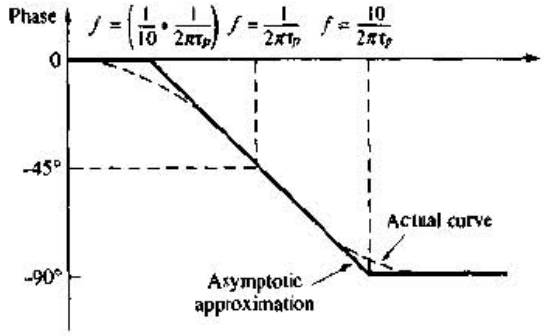

Figure 7.9 Bode plot of the voltage transfer function phase for the circuit in Figure 7.3

Example 7.1 **Objective:** Determine the corner frequencies and maximum-magnitude asymptotes of the Bode plots for a specified circuit.

For the circuits in Figures 7.2 and 7.3, the parameters are: $R_S = 1\,\text{k}\Omega$, $R_P = 10\,\text{k}\Omega$, $C_S = 1\,\mu\text{F}$, and $C_P = 3\,\text{pF}$.

Solution: (Figure 7.2) The time constant is

$$\tau_S = (R_S + R_P)C_S = (10^3 + 10 \times 10^3)(10^{-6}) = 1.1 \times 10^{-2}\,\text{s}$$

or

$$\tau_S = 11\,\text{ms}$$

The corner frequency of the Bode plot shown in Figure 7.5 is then

$$f = \frac{1}{2\pi\tau_S} = \frac{1}{(2\pi)(11 \times 10^{-3})} = 14.5\,\text{Hz}$$

The maximum magnitude is

$$\frac{R_P}{R_S + R_P} = \frac{10}{1 + 10} = 0.909$$

or

$$20\log_{10}\left(\frac{R_P}{R_S + R_P}\right) = -0.828\,\text{dB}$$

Solution: (Figure 7.3) The time constant is

$$\tau_P = (R_S \| R_P)C_P = (10^3 \| (10 \times 10^3))(3 \times 10^{-12}) = 2.73 \times 10^{-9}\,\text{s}$$

or

$$\tau_P = 2.73\,\text{ns}$$

The corner frequency of the Bode plot in Figure 7.8 is then

$$f = \frac{1}{2\pi\tau_P} = \frac{1}{(2\pi)(2.73 \times 10^{-9})} \Rightarrow 58.3\,\text{MHz}$$

The maximum magnitude is the same as just calculated: 0.909 or −0.828 dB.

Comment: Since the two capacitance values are substantially different, the two time constants differ by orders of magnitude, which means that the two corner frequencies also differ by orders of magnitude. Later in this text, we will take advantage of these differences in our analysis of transistor circuits.

Test Your Understanding

7.1 For the circuit shown in Figure 7.2, the parameters are $R_S = R_P = 4\,\text{k}\Omega$. (a) If the corner frequency is $f = 20$ Hz, determine the value of C_S. (b) Find the magnitude of the transfer function at $f = 40$ Hz, 80 Hz, and 200 Hz. (Ans. (a) $C_S = 0.995\,\mu\text{F}$ (b) $|T(j\omega)| = 0.447$, 0.485, and 0.498)

7.2 Consider the circuit shown in Figure 7.3 with parameters $R_S = R_P = 10\,\text{k}\Omega$. If the corner frequency is $f = 500\,\text{kHz}$, determine the value of C_P. (Ans. $C_P = 63.7\,\text{pF}$)

7.2.4 Short-Circuit and Open-Circuit Time Constants

The two circuits shown in Figures 7.2 and 7.3 each contain only one capacitor. The circuit in Figure 7.10 is the same basic configuration but contains both capacitors. Capacitor C_S is the coupling capacitor and is in series with the input and output; capacitor C_P is the load capacitor and is in parallel with the output and ground.

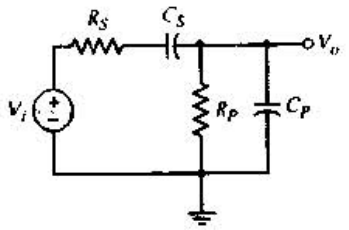

Figure 7.10 Circuit with both a series coupling and a parallel load capacitor

We can determine the voltage transfer function of this circuit by writing a KCL equation at the output node. The result is

$$\frac{V_o(s)}{V_i(s)} = \left(\frac{R_P}{R_S + R_P}\right) \times \frac{1}{\left[1 + \left(\frac{R_P}{R_S + R_P}\right)\left(\frac{C_P}{C_S}\right) + \frac{1}{s\tau_S} + s\tau_P\right]} \tag{7.16}$$

where τ_S and τ_P are the same time constants as previously defined.

Although Equation (7.16) is the exact transfer function, it is awkward to deal with in this form.

We have seen in the previous analysis, however, that C_S affects the low-frequency response and C_P affects the high-frequency response. Further, if $C_P \ll C_S$ and if R_S and R_P are of the same order of magnitude, then the corner frequencies of the Bode plots created by C_S and C_P will differ by orders of magnitude. (We actually encounter this situation in real circuits.) Con-

sequently, when a circuit contains both coupling and load capacitors, and when the values of the capacitors differ by orders of magnitude, then we can determine the effect of each capacitor individually.

At low frequencies, we can treat the load capacitor C_P as an open circuit. To find the equivalent resistance seen by a capacitor, set all independent sources equal to zero. Therefore, the effective resistance seen by C_S is the series combination of R_S and R_P. The time constant associated with C_S is

$$\tau_S = (R_S + R_P)C_S \tag{7.17}$$

Since C_P was made an open circuit, τ_S is called an **open-circuit time constant**. The subscript S is associated with the coupling capacitor, or the capacitor in series with the input and output signals.

At high frequencies, we can treat the coupling capacitor C_S as a short circuit. The effective resistance seen by C_P is the parallel combination of R_S and R_P, and the associated time constant is

$$\tau_P = (R_S \| R_P)C_P \tag{7.18}$$

which is called the **short-circuit time constant**. The subscript P is associated with the load capacitor, or the capacitor in parallel with the output and ground.

We can now define the corner frequencies of the Bode plot. The **lower corner**, or 3 dB frequency, which is at the low end of the frequency scale, is a function of the open-circuit time constant and is defined as

$$f_L = \frac{1}{2\pi\tau_S} \tag{7.19(a)}$$

The **upper corner**, or 3 dB, frequency, which is at the high end of the frequency scale, is a function of the short-circuit time constant and is defined as

$$f_H = \frac{1}{2\pi\tau_P} \tag{7.19(b)}$$

The resulting Bode plot of the magnitude of the voltage transfer function for the circuit in Figure 7.9 is shown in Figure 7.11.

This Bode plot is for a passive circuit; the Bode plots for transistor amplifiers are similar. The amplifier gain is constant over a wide frequency range, called the **midband**. In this frequency range, all capacitance effects are negligible and can be neglected in the gain calculations. At the high end of the frequency spectrum, the gain drops as a result of the load capacitance and, as we will see later, the transistor effects. At the low end of the frequency spectrum, the gain decreases because coupling capacitors and bypass capacitors do not act as perfect short circuits.

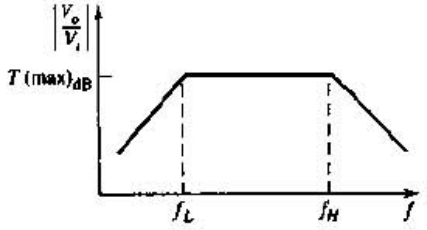

Figure 7.11 Bode plot of the voltage transfer function magnitude for the circuit in Figure 7.10

The midband range, or **bandwidth**, is defined by the corner frequencies f_L and f_H, as follows:

$$f_{BW} = f_H - f_L \tag{7.20}$$

Since $f_H \gg f_L$, as we have seen in our examples, the bandwidth is essentially given by

$$f_{BW} \cong f_H \tag{7.21}$$

Example 7.2 **Objective:** Determine the corner frequencies and bandwidth of a passive circuit containing two capacitors.

Consider the circuit shown in Figure 7.10 with parameters $R_S = 1\,\text{k}\Omega$, $R_P = 10\,\text{k}\Omega$, $C_S = 1\,\mu\text{F}$, and $C_P = 3\,\text{pF}$.

Solution: Since C_P is less than C_S by approximately six orders of magnitude, we can treat the effect of each capacitor separately. The open-circuit time constant is

$$\tau_S = (R_S + R_P)C_S = (10^3 + 10 \times 10^3)(10^{-6}) = 1.1 \times 10^{-2}\,\text{s}$$

and the short-circuit time constant is

$$\tau_P = (R_S \| R_P)C_P = [10^3 \| (10 \times 10^3)](3 \times 10^{-12}) = 2.73 \times 10^{-9}\,\text{s}$$

The corner frequencies are then

$$f_L = \frac{1}{2\pi\tau_S} = \frac{1}{2\pi(1.1 \times 10^{-2})} = 14.5\,\text{Hz}$$

and

$$f_H = \frac{1}{2\pi\tau_P} = \frac{1}{2\pi(2.73 \times 10^{-9})} \Rightarrow 58.3\,\text{MHz}$$

Finally, the bandwidth is

$$f_{BW} = f_H - f_L = 58.3\,\text{MHz} - 14.5\,\text{Hz} \cong 58.3\,\text{MHz}$$

Comment: The corner frequencies in this example are exactly the same as those determined in Example 7.1. This occurred because the two corner frequencies are far apart. The maximum magnitude of the voltage transfer function is again

$$\frac{R_P}{R_S + R_P} = \frac{10}{1 + 10} = 0.909 \Rightarrow -0.828\,\text{dB}$$

The Bode plot of the magnitude of the voltage transfer function is shown in Figure 7.12.

We will continue, in the following sections of the chapter, to use the concept of open-circuit and short-circuit time constants to determine the corner frequencies of the Bode plots of transistor circuits. An implicit assumption in this technique is that coupling and load capacitance values differ by many orders of magnitude.

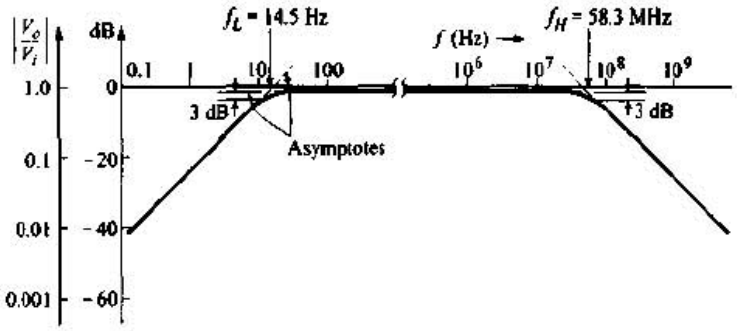

Figure 7.12 Bode plot of the magnitude of the voltage transfer function for the circuit in Figure 7.10

Test Your Understanding

7.3 For the equivalent circuit shown in Figure 7.13, the parameters are: $R_S = 1\,\text{k}\Omega$, $r_\pi = 2\,\text{k}\Omega$, $R_L = 4\,\text{k}\Omega$, $g_m = 50\,\text{mA/V}$, and $C_C = 1\,\mu\text{F}$. (a) Determine the expression for the circuit time constant. (b) Calculate the 3 dB frequency and maximum gain asymptote. (c) Sketch the Bode plot of the transfer function magnitude. (Ans. (a) $\tau = (r_\pi + R_S)C_C$, (b) $f_{3\text{dB}} = 53.1\,\text{Hz}$, $|T(j\omega)|_{\text{max}} = 133$)

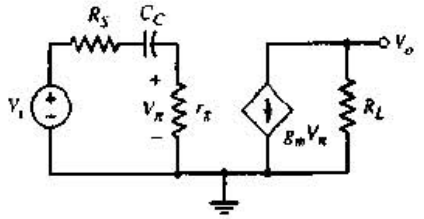

Figure 7.13 Figure for Exercise 7.3

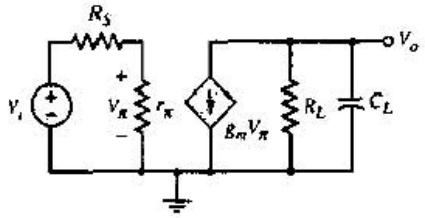

Figure 7.14 Figure for Exercise 7.4

7.4 The equivalent circuit in Figure 7.14 has circuit parameters $R_S = 0.5\,\text{k}\Omega$, $r_\pi = 1.5\,\text{k}\Omega$, $g_m = 75\,\text{mA/V}$, $R_L = 5\,\text{k}\Omega$, and $C_L = 10\,\text{pF}$. (a) Determine the expression for the circuit time constant. (b) Calculate the 3 dB frequency and maximum gain asymptote. (c) Sketch the Bode plot of the transfer function magnitude. (Ans. (a) $\tau = R_L C_L$, (b) $f_{3\text{dB}} = 3.18\,\text{MHz}$, $|T(j\omega)|_{\text{max}} = 281$)

7.5 The value of R_S in the circuit in Figure 7.10 is $R_S = 1\,\text{k}\Omega$. The midband gain is -1 dB, and the corner frequencies are $f_L = 100\,\text{Hz}$ and $f_H = 1\,\text{MHz}$. (a) Determine R_P, C_S, and C_P. (b) Determine the open-circuit and short-circuit time constants. (Ans. (a) $R_P = 8.17\,\text{k}\Omega$, $C_S = 0.174\,\mu\text{F}$, $C_P = 179\,\text{pF}$, (b) $\tau_S = 1.60\,\text{ms}$, $\tau_P = 0.160\,\mu\text{s}$)

7.6 The parameters in the circuit in Figure 7.15 are $R_S = 0.25\,\text{k}\Omega$, $r_\pi = 2\,\text{k}\Omega$, $R_L = 4\,\text{k}\Omega$, $g_m = 65\,\text{mA/V}$, $C_C = 2\,\mu\text{F}$, and $C_L = 50\,\text{pF}$. (a) Find the open-circuit and short-

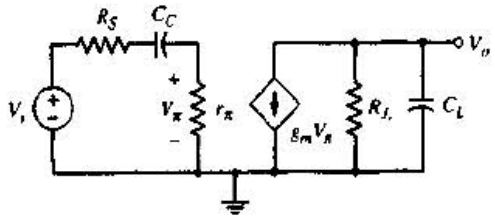

Figure 7.15 Figure for Exercise 7.6

circuit time constants. (b) Calculate the midband voltage gain. (c) Determine the upper and lower 3 dB frequencies. (d) Verify the results with a PSpice analysis. (Ans. (a) $\tau_S = 4.5\,\text{ms}$, $\tau_P = 0.2\,\mu\text{s}$, (b) $A_v = -231$, (c) $f_L = 35.4\,\text{Hz}$, $f_H = 0.796\,\text{MHz}$)

7.3 FREQUENCY RESPONSE: TRANSISTOR AMPLIFIERS WITH CIRCUIT CAPACITORS

In this section, we will analyze the basic single-stage amplifier that includes circuit capacitors. Three types of capacitors will be considered: coupling capacitor, load capacitor, and bypass capacitor. In our hand analysis, we will consider each type of capacitor individually and determine its frequency response. In the last part of this section, we will consider the effect of multiple capacitors using a PSpice analysis.

The frequency response of multistage circuits will be considered in Chapter 12 when the stability of amplifiers is considered.

7.3.1 Coupling Capacitor Effects

Input Coupling Capacitor: Common-Emitter Circuit

Figure 7.16(a) shows a bipolar common-emitter circuit with a coupling capacitor. Figure 7.16(b) shows the corresponding small-signal equivalent circuit, with the transistor small-signal output resistance r_o assumed to be infinite. This assumption is valid since $r_o \gg R_C$ and $r_o \gg R_E$ in most cases. Initially, we will use a current–voltage analysis to determine the frequency response of the circuit. Then, we will use the equivalent time constant technique.

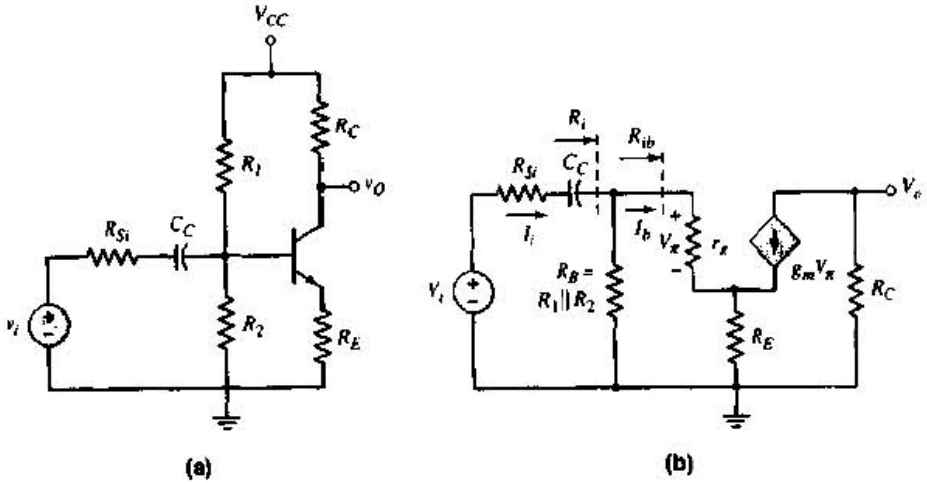

Figure 7.16 (a) Common-emitter circuit with coupling capacitor and (b) small-signal equivalent circuit

From the analysis in the previous section, we note that this circuit is a high-pass network. At high frequencies, the capacitor C_C acts as a short circuit, and the input signal is coupled through the transistor to the output. At low frequencies, the impedance of C_C becomes large and the output approaches zero.

Current–Voltage Analysis The input current can be written as

$$I_i = \frac{V_i}{R_{Si} + \dfrac{1}{sC_C} + R_i} \tag{7.22}$$

where the input resistance R_i is given by

$$R_i = R_B \| [r_\pi + (1 + \beta)R_E] = R_B \| R_{ib} \tag{7.23}$$

In writing Equation (7.23), we used the resistance reflection rule given in Chapter 3. To determine the input resistance to the base of the transistor, we multiplied the emitter resistance by the factor $(1 + \beta)$.

Using a current divider, we determine the base current to be

$$I_b = \left(\frac{R_B}{R_B + R_{ib}}\right) I_i \tag{7.24}$$

and then

$$V_\pi = I_b r_\pi \tag{7.25}$$

The output voltage is given by

$$V_o = -g_m V_\pi R_C \tag{7.26}$$

Combining Equations (7.22) through (7.26) produces

$$\begin{aligned} V_o &= -g_m R_C (I_b r_\pi) = -g_m r_\pi R_C \left(\frac{R_B}{R_B + R_{ib}}\right) I_i \\ &= -g_m r_\pi R_C \left(\frac{R_B}{R_B + R_{ib}}\right)\left(\frac{V_i}{R_{Si} + \dfrac{1}{sC_C} + R_i}\right) \end{aligned} \tag{7.27}$$

Therefore, the small-signal voltage gain is

$$A_v(s) = \frac{V_o(s)}{V_i(s)} = -g_m r_\pi R_C \left(\frac{R_B}{R_B + R_{ib}}\right)\left(\frac{sC_C}{1 + s(R_{Si} + R_i)C_C}\right) \tag{7.28}$$

which can be written in the form

$$A_v(s) = \frac{V_o(s)}{V_i(s)} = \frac{-g_m r_\pi R_C}{(R_{Si} + R_i)} \left(\frac{R_B}{R_B + R_{ib}}\right)\left(\frac{s\tau_S}{1 + s\tau_S}\right) \tag{7.29}$$

where the time constant is

$$\tau_S = (R_{Si} + R_i)C_C \tag{7.30}$$

The form of the voltage transfer function as given in Equation (7.29) is the same as that of Equation (7.5), for the coupling capacitor circuit in Figure 7.2. The Bode plot is therefore similar to that shown in Figure 7.5. The corner frequency is

$$f_L = \frac{1}{2\pi\tau_S} = \frac{1}{2\pi(R_{Si} + R_i)C_C} \tag{7.31}$$

and the maximum magnitude, in decibels, is

$$|A_v(\max)|_{\text{dB}} = 20 \log_{10}\left(\frac{g_m r_\pi R_C}{R_{Si} + R_i}\right)\left(\frac{R_B}{R_B + R_{ib}}\right) \tag{7.32}$$

Example 7.3 **Objective:** Calculate the corner frequency and maximum gain of a bipolar common-emitter circuit with a coupling capacitor.

For the circuit shown in Figure 7.16, the parameters are: $R_1 = 51.2\,\text{k}\Omega$, $R_2 = 9.6\,\text{k}\Omega$, $R_C = 2\,\text{k}\Omega$, $R_E = 0.4\,\text{k}\Omega$, $R_{Si} = 0.1\,\text{k}\Omega$, $C_C = 1\,\mu\text{F}$, and $V_{CC} = 10\,\text{V}$. The transistor parameters are: $V_{BE}(\text{on}) = 0.7\,\text{V}$, $\beta = 100$, and $V_A = \infty$.

Solution: From a dc analysis, the quiescent collector current is $I_{CQ} = 1.81\,\text{mA}$. The transconductance is therefore

$$g_m = \frac{I_{CQ}}{V_T} = \frac{1.81}{0.026} = 69.6\,\text{mA/V}$$

and the diffusion resistance is

$$r_\pi = \frac{\beta V_T}{I_{CQ}} = \frac{(100)(0.026)}{1.81} = 1.44\,\text{k}\Omega$$

The input resistance is

$$R_i = R_1 \| R_2 \| [r_\pi + (1+\beta)R_E]$$
$$= 51.2 \| 9.6 \| [1.44 + (101)(0.4)] = 6.77\,\text{k}\Omega$$

and the time constant is therefore

$$\tau_S = (R_{Si} + R_i)C_C = (0.1 \times 10^3 + 6.77 \times 10^3)(1 \times 10^{-6}) = 6.87 \times 10^{-3}\,\text{s}$$

or

$$\tau_S = 6.87\,\text{ms}$$

The corner frequency is

$$f_L = \frac{1}{2\pi\tau_S} = \frac{1}{2\pi(6.87 \times 10^{-3})} = 23.2\,\text{Hz}$$

Finally, the maximum voltage gain magnitude is

$$|A_v|_{\max} = \frac{g_m r_\pi R_C}{(R_{Si} + R_i)}\left(\frac{R_B}{R_B + R_{ib}}\right)$$

where

$$R_{ib} = r_\pi + (1+\beta)R_E = 1.44 + (101)(0.4) = 41.8\,\text{k}\Omega$$

Therefore,

$$|A_v|_{\max} = \frac{(69.6)(1.44)}{(0.1 + 6.77)}\left(\frac{8.08}{8.08 + 41.8}\right) = 4.73$$

Comment: The coupling capacitor produces a high-pass network. In this circuit, if the signal frequency is approximately two octaves above the corner frequency, the coupling capacitor acts as a short circuit.

Time Constant Technique In general, we do not need to derive the complete circuit transfer function including capacitance effects in order to complete the Bode plot and determine the frequency response. By looking at a circuit with, initially, only one capacitor, we can determine if the amplifier is a low-pass or high-pass circuit. We can then specify the Bode plot if we know the time constant and the maximum midband gain. The time constant determines the