corner frequency. The midband gain is found in the usual way when capacitances are eliminated from the circuit.

This time constant technique yields good results when all poles are real, as will be the case in this chapter. In addition, this technique does not determine the corner frequencies due to system zeros. The major benefit of using the time constant approach is that it gives infomation about which circuit elements affect the −3 dB frequency of the circuit. A coupling capacitor produces a high-pass network, so the form of the Bode plot will be the same as that shown in Figure 7.5. Also, the maximum gain is determined when the coupling capacitor acts as a short circuit, as was assumed in Chapters 4 and 6.

The time constant for the circuit is a function of the equivalent resistance seen by the capacitor. The small-signal equivalent circuit is shown in Figure 7.16(b). If we set the independent voltage source equal to zero, the equivalent resistance seen by the coupling capacitor C_C is $(R_{Si} + R_i)$. The time constant is then

$$\tau_S = (R_{Si} + R_i)C_C \tag{7.33}$$

This is the same as Equation (7.30), which was determined by using a current–voltage analysis.

Output Coupling Capacitor: Common-Source Circuit

Figure 7.17(a) shows a common-source MOSFET amplifier. We assume that the resistance of the signal generator is much less than R_G and can therefore be neglected. In this case, the output signal is connected to the load through a coupling capacitor.

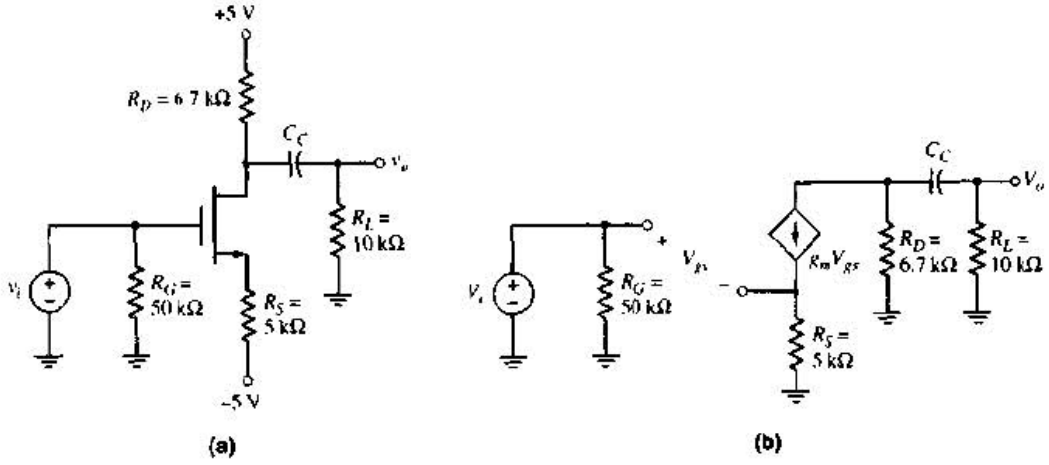


Figure 7.17 (a) Common-source circuit with output coupling capacitor and (b) small-signal equivalent circuit

The small-signal equivalent circuit, assuming r_o is infinite, is shown in Figure 7.17(b). The maximum output voltage, assuming C_C is a short circuit, is

$$|V_o|_{max} = g_m V_{gs}(R_D \| R_L) \tag{7.34}$$

and the input voltage can be written as

$$V_i = V_{gs} + g_m R_S V_{gs} \tag{7.35}$$

Therefore, the maximum small-signal gain is

$$|A_v|_{max} = \frac{g_m(R_D \| R_L)}{1 + g_m R_S} \tag{7.36}$$

Even though the coupling capacitor is in the output portion of the circuit, the Bode plot will still be that of a high-pass network, as shown in Figure 7.5. Using the time constant technique to determine the corner frequency will substantially simplify the circuit analysis, since we do not specifically need to determine the transfer function for the frequency response.

The time constant is a function of the effective resistance seen by capacitor C_C, which is determined by setting all independent sources equal to zero. Since $V_i = 0$, then $V_{gs} = 0$ and $g_m V_{gs} = 0$, and the effective resistance seen by C_C is $(R_D + R_L)$. The time constant is then

$$\tau_S = (R_D + R_L)C_C \tag{7.37}$$

and the corner frequency is $f_L = 1/2\pi\tau_S$.

Design Example 7.4 Objective: The circuit in Figure 7.17(a) is to be used as a simple audio amplifier. Design the circuit such that the lower corner frequency is $f_L = 20\,\text{Hz}$.

Solution: The corner frequency can be written in terms of the time constant, as follows:

$$f_L = \frac{1}{2\pi\tau_S}$$

The time constant is then

$$\tau_S = \frac{1}{2\pi f} = \frac{1}{2\pi(20)} \Rightarrow 7.96\,\text{ms}$$

Therefore, from Equation (7.37) the coupling capacitance is

$$C_C = \frac{\tau_S}{R_D + R_L} = \frac{7.96 \times 10^{-3}}{6.7 \times 10^3 + 10 \times 10^3} = 4.77 \times 10^{-7}\,\text{F}$$

or

$$C_C = 0.477\,\mu\text{F}$$

Comment: Using the time constant technique to find the corner frequency is substantially easier than using the circuit analysis approach.

Test Your Understanding

7.7 For the circuit in Figure 7.16(a), the parameters are: $R_{Si} = 0.1\,\text{k}\Omega$, $R_i = 20\,\text{k}\Omega$, $R_2 = 2.2\,\text{k}\Omega$, $R_E = 0.1\,\text{k}\Omega$, $R_C = 2\,\text{k}\Omega$, $C_C = 47\,\mu\text{F}$, and $V_{CC} = 10\,\text{V}$. The transistor parameters are: $V_{BE}(\text{on}) = 0.7\,\text{V}$, $\beta = 200$, and $V_A = \infty$. (a) Determine the expression for the time constant τ_S. (b) Determine the corner frequency and midband voltage gain. (Ans. (a) $\tau_S = (R_i + R_{Si})C_C$, (b) $f = 1.76\,\text{Hz}$, $A_v = -17.2$)

D7.8 Consider the circuit shown in Figure 7.17(a) with transistor parameters $V_{TN} = 2\,\text{V}$, $K_n = 0.5\,\text{mA/V}^2$, and $\lambda = 0$. The circuit parameters are $R_G = 50\,\text{k}\Omega$ and $R_L = 10\,\text{k}\Omega$. (a) Determine new values of R_S and R_D such that $I_{DQ} = 0.8\,\text{mA}$ and the quiescent drain voltage is $V_{DQ} = 0$. (b) Find the required value of C_C for a corner frequency of $f = 20\,\text{Hz}$. (Ans. (a) $R_S = 2.18\,\text{k}\Omega$, $R_D = 6.25\,\text{k}\Omega$, (b) $C_C = 0.49\,\mu\text{F}$)

Output Coupling Capacitor: Emitter-Follower Circuit An emitter follower with a coupling capacitor in the output portion of the circuit is shown in Figure 7.18(a). We assume that coupling capacitor C_{C1}, which is part of the original emitter follower, is very large, and that it acts as a short circuit to the input signal.

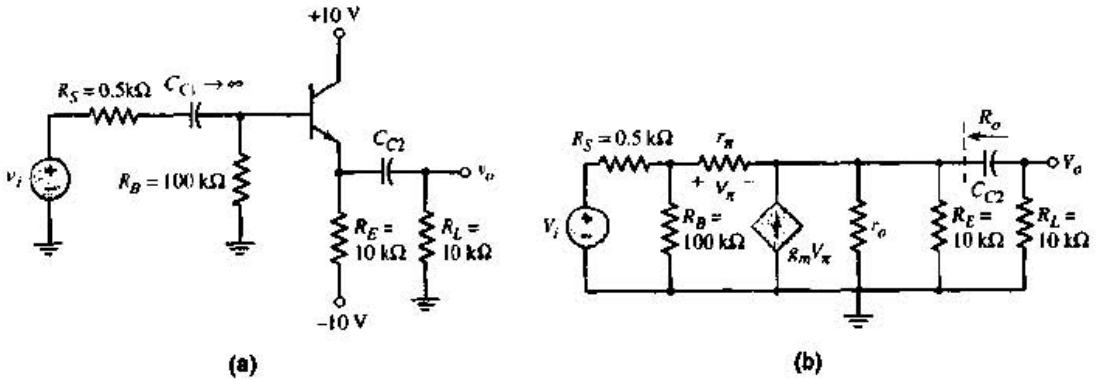


Figure 7.18 (a) Emitter-follower circuit with output coupling capacitor and (b) small-signal equivalent circuit

The small-signal equivalent circuit, including the small-signal transistor resistance r_π, is shown in Figure 7.18(b). The equivalent resistance seen by the coupling capacitor C_{C2} is $[R_o + R_L]$, and the time constant is

$$\tau_S = [R_o + R_L]C_{C2} \tag{7.38}$$

where R_o is the output resistance as defined in Figure 7.18(b). As shown in Chapter 4, the output resistance is

$$R_o = R_E \| r_o \| \left\{ \frac{[r_\pi + (R_S \| R_B)]}{1 + \beta} \right\} \tag{7.39}$$

If we combine Equations (7.39) and (7.38), the time constant expression becomes fairly complicated. However, the current–voltage analysis of this circuit including C_{C2} is even more cumbersome. The time constant technique again simplifies the analysis substantially.

Example 7.5 **Objective:** Determine the 3dB frequency of an emitter-follower amplifier circuit with an output coupling capacitor.

Consider the circuit shown in Figure 7.18(a) with transistor parameters $\beta = 100$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, and $V_A = 120\,\text{V}$. The output coupling capacitance is $C_{C2} = 1\,\mu\text{F}$.

Solution: A dc analysis shows that $I_{CQ} = 0.838\,\text{mA}$. Therefore, the small-signal parameters are: $r_\pi = 3.10\,\text{k}\Omega$, $g_m = 32.2\,\text{mA/V}$, and $r_o = 143\,\text{k}\Omega$.

From Equation (7.39), the output resistance R_o of the emitter follower is

$$R_o = R_E \| r_o \| \left\{ \frac{[r_\pi + (R_S \| R_B)]}{1+\beta} \right\}$$

$$= 10 \| 143 \| \left\{ \frac{[3.10 + (0.5 \| 100)]}{101} \right\} = 10 \| 143 \| 0.0356\,\text{k}\Omega$$

or

$$R_o \cong 35.5\,\Omega$$

From Equation (7.38), the time constant is

$$\tau_S = [R_o + R_L]C_{C2} = [35.5 + 10^4](10^{-6}) \cong 1 \times 10^{-2}\,\text{s}$$

The 3 dB frequency is then

$$f_L = \frac{1}{2\pi\tau_S} = \frac{1}{2\pi(10^{-2})} = 15.9\,\text{Hz}$$

Comment: Determining the 3 dB or corner frequency is very direct with the time constant technique.

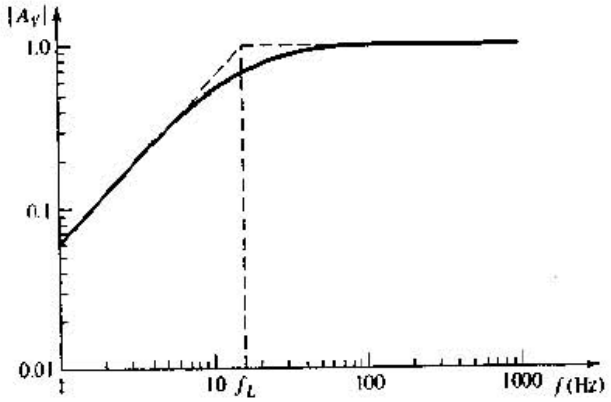


Figure 7.19 PSpice analysis results for the emitter-follower circuit in Figure 7.18(a)

Computer Verification: Based on a PSpice analysis, Figure 7.19 is a Bode plot of the voltage gain magnitude of the emitter-follower circuit shown in Figure 7.18(a). The corner frequency is essentially identical to that obtained by the time constant technique. Also, the asymptotic value of the small-signal voltage gain is $A_v = 0.988$, as expected for an emitter-follower circuit.

Problem-Solving Technique: Bode Plot of Gain Magnitude

1. For a particular capacitor in a circuit, determine whether the capacitor is producing a low-pass or high-pass circuit. From this, sketch the general shape of the Bode plot.

2. The corner frequency is found from $f = 1/2\pi\tau$ where the time constant is $\tau = R_{eq}C$. The equivalent resistance R_{eq} is the equivalent resistance seen by the capacitor.
3. The maximum gain magnitude is the midband gain. Coupling and bypass capacitors act as short circuits and load capacitors act as open circuits.

Test Your Understanding

7.9 For the emitter-follower circuit shown in Figure 7.18(a), determine the required value of C_{C2} to yield a corner frequency of 10 Hz. (Ans. $C_{C2} = 1.59\,\mu F$)

7.3.2 Load Capacitor Effects

An amplifier output may be connected to a load or to the input or another amplifier. The model of the load circuit input impedance is generally a capacitance in parallel with a resistance. In addition, there is a parasitic capacitance between ground and the line that connects the amplifier output to the load circuit.

Figure 7.20(a) shows a MOSFET common-source amplifier with a load resistance R_L and a load capacitance C_L connected to the output, and Figure 7.20(b) shows the small-signal equivalent circuit. The transistor small-signal output resistance r_o is assumed to be infinite. This circuit configuration is essentially the same as that in Figure 7.3, which is a low-pass network. At high frequencies, the impedance of C_L decreases and acts as a shunt between the output and ground, and the output voltage tends toward zero. The Bode plot is similar to that shown in Figure 7.8, with an upper corner frequency and a maximum gain asymptote.

The equivalent resistance seen by the load capacitor C_L is $R_D \| R_L$. Since we set $V_i = 0$, then $g_m V_{sg} = 0$, which means that the dependent current source does not affect the equivalent resistance.

The time constant for this circuit is

$$\tau_P = (R_D \| R_L)C_L \tag{7.40}$$

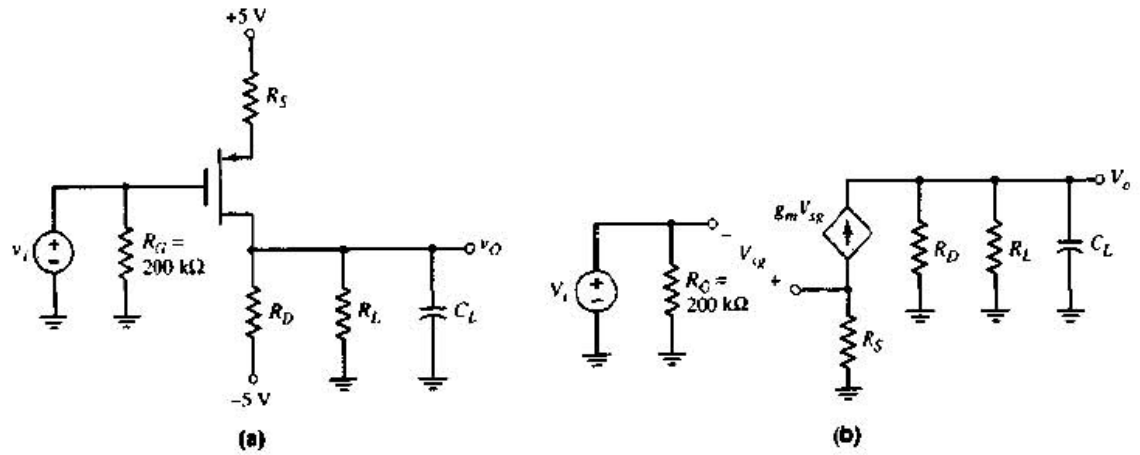


Figure 7.20 (a) MOSFET common-source circuit with a load capacitor and (b) small-signal equivalent circuit

The maximum gain asymptote, which is found by assuming C_L is an open circuit, is

$$|A_v|_{max} = \frac{g_m(R_D \| R_L)}{1 + g_m R_S} \tag{7.41}$$

Example 7.6 **Objective:** Determine the corner frequency and maximum gain asymptote of a MOSFET amplifier.

For the circuit in Figure 7.20(a), the parameters are: $R_S = 3.2\,\text{k}\Omega$, $R_D = 10\,\text{k}\Omega$, $R_L = 20\,\text{k}\Omega$, and $C_L = 10\,\text{pF}$. The transistor parameters are: $V_{TP} = -2\,\text{V}$, $K_p = 0.25\,\text{mA/V}^2$, and $\lambda = 0$.

Solution: From the dc analysis, we find that $I_{DQ} = 0.5\,\text{mA}$, $V_{SGQ} = 3.41\,\text{V}$, and $V_{SDQ} = 3.41\,\text{V}$. The transconductance is therefore

$$g_m = 2K_p(V_{SG} + V_{TP}) = 2(0.25)(3.41 - 2) = 0.705\,\text{mA/V}$$

From Equation (7.40), the time constant is

$$\tau_P = (R_D \| R_L)C_L = [(10 \times 10^3) \| (20 \times 10^3)](10 \times 10^{-12}) = 6.67 \times 10^{-8}\,\text{s}$$

or

$$\tau_P = 66.7\,\text{ns}$$

Therefore, the corner frequency is

$$f_H = \frac{1}{2\pi\tau_P} = \frac{1}{2\pi(66.7 \times 10^{-9})} \Rightarrow 2.39\,\text{MHz}$$

Finally, from Equation (7.41), the maximum gain asymptote is

$$|A_v|_{max} = \frac{g_m(R_D \| R_L)}{1 + g_m R_S} = \frac{(0.705)(10 \| 20)}{1 + (0.705)(3.2)} = 1.44$$

Comment: The Bode plot for this circuit is similar to that in Figure 7.8, and it represents a low-pass network. The relatively large value of R_S results in a low voltage gain.

Computer Simulation: Figure 7.21 shows the results of a PSpice analysis of the circuit given in Figure 7.20(a). Figure 7.21(a) is a Bode plot of the voltage gain magnitude. The

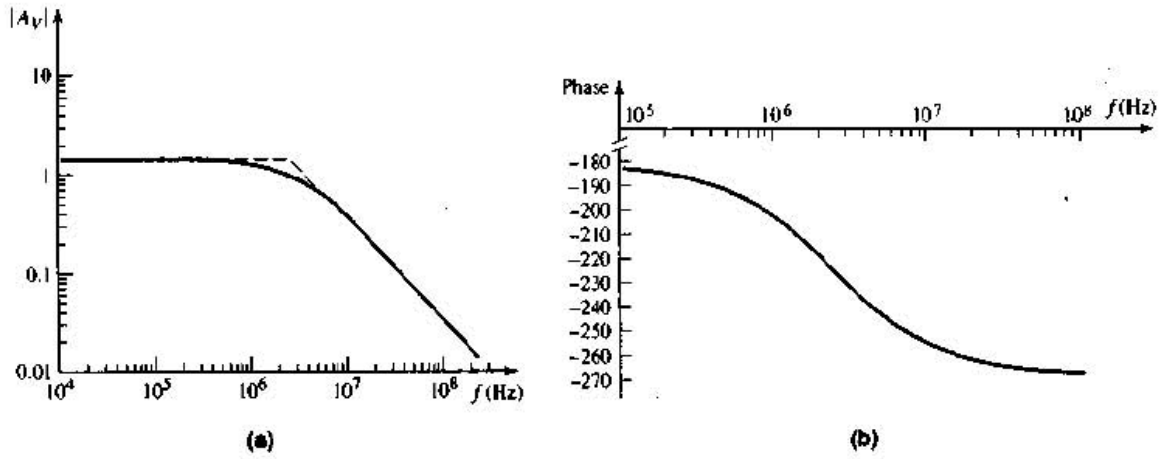


Figure 7.21 PSpice analysis results for the circuit in Figure 7.20(a): (a) voltage gain magnitude response, and (b) phase response

midband gain is 1.44 and the corner frequency is 2.4 MHz, which agrees extremely well with the hand analysis results. The phase of the voltage gain is shown in Figure 7.21(b). The midband phase is −180 degrees, as expected. Also, as the frequency increases, the phase approaches −270 degrees. As was shown in Figure 7.9, a phase change of −90 degrees is expected for a load capacitor.

Test Your Understanding

D7.10 The PMOS common-source circuit shown in Figure 7.20(a) has a load resistance $R_L = 10\,\text{k}\Omega$. The transistor parameters are: $V_{TN} = -2\,\text{V}$, $K_p = 0.5\,\text{mA/V}^2$, and $\lambda = 0$. (a) Design the circuit such that $I_{DQ} = 1\,\text{mA}$ and $V_{SDQ} = V_{SGQ}$. (b) Determine the value of C_L such that the corner frequency is $f = 1\,\text{MHz}$. (Ans. (a) $R_S = 1.59\,\text{k}\Omega$, $R_D = 5\,\text{k}\Omega$, (b) $C_L = 47.7\,\text{pF}$)

7.3.3 Coupling and Load Capacitors

A circuit with both a coupling capacitor and a load capacitor is shown in Figure 7.22(a). Since the values of the coupling capacitance and load capacitance differ by orders of magnitude, the corner frequencies are far apart and can be treated separately as discussed previously. The small-signal equivalent circuit is shown in Figure 7.22(b), assuming the transistor small-signal resistance r_o is infinite.

The Bode plot of the voltage gain magnitude is similar to that shown in Figure 7.11. The lower corner frequency f_L is given by

$$f_L = \frac{1}{2\pi\tau_S} \tag{7.42}$$

where τ_S is the time constant associated with the coupling capacitor C_C, and the upper corner frequency f_H is given by

$$f_H = \frac{1}{2\pi\tau_P} \tag{7.43}$$

where τ_P is the time constant associated with the load capacitor C_L. It should be emphasized that Equations (7.42) and (7.43) are valid only as long as the two corner frequencies are far apart.

Using the small-signal equivalent circuit in Figure 7.22(b), we set the signal source equal to zero to find the equivalent resistance associated with the coupling capacitor. The related time constant is

$$\tau_S = [R_S + (R_1 \| R_2 \| R_i)]C_C \tag{7.44}$$

where

$$R_i = r_\pi + (1 + \beta)R_E \tag{7.45}$$

Similarly, the time constant related to C_L is

$$\tau_P = (R_C \| R_L)C_L \tag{7.46}$$

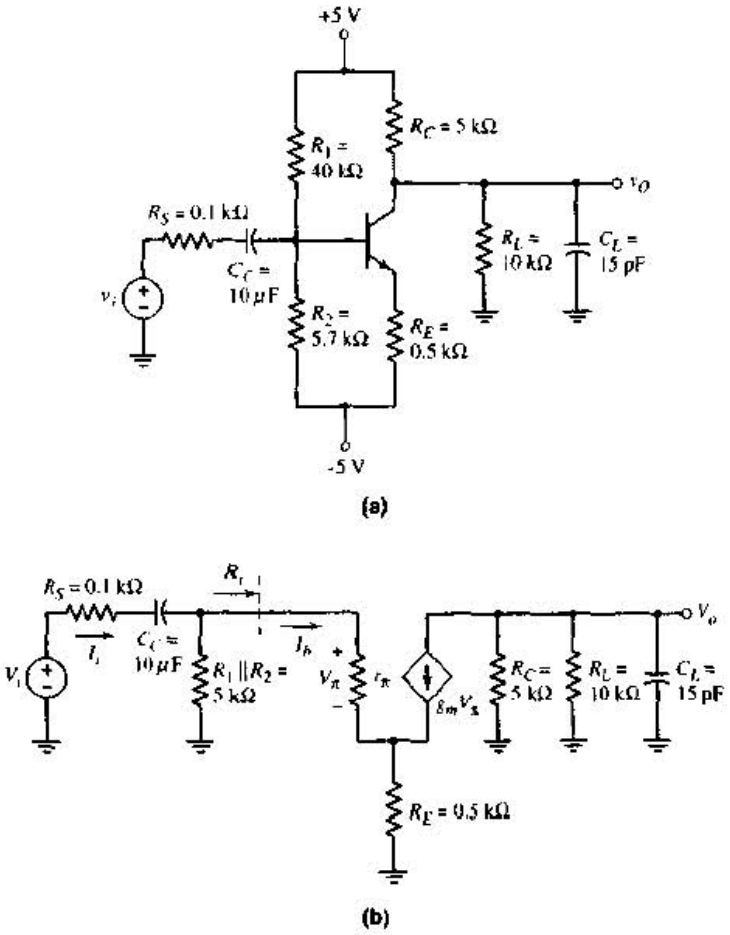


Figure 7.22 (c) Circuit with both a coupling and a load capacitor and (b) small-signal equivalent circuit

Since the two corner frequencies are far apart, the gain will reach a maximum value in the frequency range between f_L and f_H, which is the midband. We can calculate the midband gain by assuming that the coupling capacitor is a short circuit and the load capacitor is an open circuit.

From Figure 7.22(b), we see that in midband we have

$$I_i = \frac{V_i}{R_S + R_1 \| R_2 \| R_i} \tag{7.47}$$

and

$$I_b = \left(\frac{R_1 \| R_2}{(R_1 \| R_2) + R_i}\right) I_i \tag{7.48}$$

Also,

$$V_\pi = I_b r_\pi \tag{7.49}$$

and the output voltage is

$$V_o = -g_m V_\pi (R_C \| R_L) \tag{7.50}$$

Finally, combining Equations (7.47) through (7.50), we find the magnitude of the midband gain, as follows:

$$|A_v| = \left|\frac{V_o}{V_i}\right| = g_m r_\pi (R_C \| R_L)\left(\frac{R_1 \| R_2}{(R_1 \| R_2) + R_i}\right)\left(\frac{1}{[R_S + (R_1 \| R_2 \| R_i)]}\right) \tag{7.51}$$

Example 7.7 **Objective:** Determine the midband gain, corner frequencies, and bandwidth of a circuit containing both a coupling capacitor and a load capacitor.

Consider the circuit shown in Figure 7.22(a) with transistor parameters $V_{BE}(\text{on}) = 0.7\,\text{V}$, $\beta = 100$, and $V_A = \infty$.

Solution: The dc analysis of this circuit yields a quiescent collector current of $I_{CQ} = 0.99\,\text{mA}$. The transconductance is

$$g_m = \frac{I_{CQ}}{V_T} = \frac{0.99}{0.026} = 38.1\,\text{mA/V}$$

and the base diffusion resistance is

$$r_\pi = \frac{\beta V_T}{I_{CQ}} = \frac{(100)(0.026)}{0.99} = 2.63\,\text{k}\Omega$$

The input resistance R_i is therefore

$$R_i = r_\pi + (1 + \beta)R_E = 2.63 + (101)(0.5) = 53.1\,\text{k}\Omega$$

From Equation (7.51), the midband gain is

$$|A_v|_{\max} = \left|\frac{V_o}{V_i}\right|_{\max} = g_m r_\pi (R_C \| R_L)\left(\frac{R_1 \| R_2}{(R_1 \| R_2) + R_i}\right)\left(\frac{1}{[R_S + (R_1 \| R_2 \| R_i)]}\right)$$

$$= (38.1)(2.63)(5 \| 10)\left(\frac{40 \| 5.7}{(40 \| 5.7) + 53.1}\right)\left(\frac{1}{[0.1 + (40 \| 5.7 \| 53.1)]}\right)$$

or

$$|A_v|_{\max} = 6.16$$

The time constant τ_S is

$$\tau_S = (R_S + R_1 \| R_2 \| R_i)C_C$$

$$= (0.1 \times 10^3 + (5.7 \times 10^3) \| (40 \times 10^3) \| (53.1 \times 10^3))(10 \times 10^{-6}) = 4.66 \times 10^{-2}\,\text{s}$$

or

$$\tau_S = 46.6\,\text{ms}$$

and the time constant τ_P is

$$\tau_P = (R_C \| R_L)C_L = ((5 \times 10^3) \| (10 \times 10^3))(15 \times 10^{-12}) = 5 \times 10^{-8}\,\text{s}$$

or

$$\tau_P = 50\,\text{ns}$$

The lower corner frequency is

$$f_L = \frac{1}{2\pi\tau_S} = \frac{1}{2\pi(46.6 \times 10^{-3})} = 3.42\,\text{Hz}$$

and the upper corner frequency is

$$f_H = \frac{1}{2\pi\tau_P} = \frac{1}{2\pi(50 \times 10^{-9})} \Rightarrow 3.18\,\text{MHz}$$

Finally, the bandwidth is

$$f_{BW} = f_H - f_L = 3.18\,\text{MHz} - 3.4\,\text{Hz} \cong 3.18\,\text{MHz}$$

Comment: The two corner frequencies differ by approximately six orders of magnitude; therefore, considering one capacitor at a time is a valid approach.

A figure of merit for an amplifier is the **gain–bandwidth product**. Assuming the corner frequencies are far apart, the bandwidth is

$$f_{BW} = f_H - f_L \cong f_H \tag{7.52}$$

and the maximum gain is $|A_v|_{max}$. The gain–bandwidth product is therefore

$$GB = |A_v|_{max} \cdot f_H \tag{7.53}$$

Later we will show that, for a given load capacitance, this product is essentially a constant. We will also describe how trade-offs must be made between gain and bandwidth in amplifier design.

7.3.4 Bypass Capacitor Effects

In bipolar and FET discrete amplifiers, emitter and source bypass capacitors are often included so that emitter and source resistors can be used to stabilize the Q-point without sacrificing the small-signal gain. The bypass capacitors are assumed to act as short circuits at the signal frequency. However, to guide us in choosing a bypass capacitor, we must determine the circuit response in the frequency range where these capacitors are neither open nor short circuits.

Figure 7.23(a) shows a common-emitter circuit with an emitter bypass capacitor. The small-signal equivalent circuit is shown in Figure 7.23(b). We

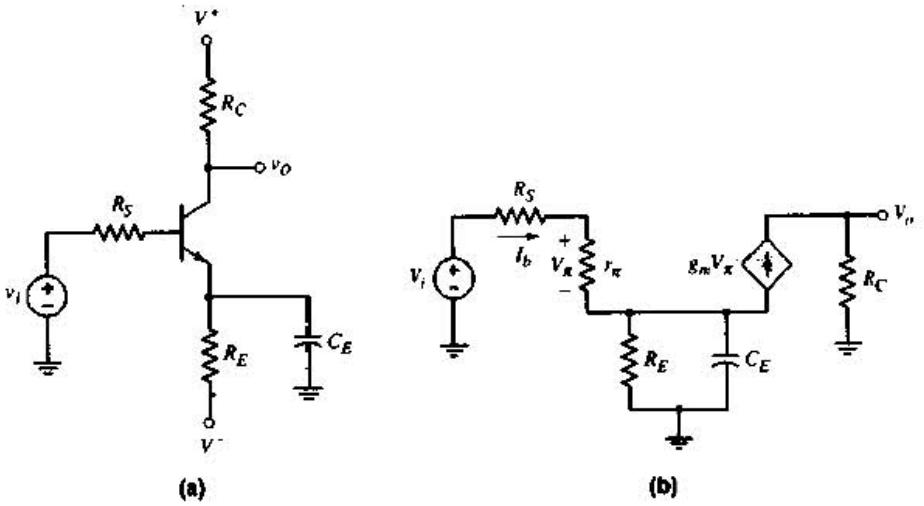


Figure 7.23 (a) Circuit with emitter bypass capacitor and (b) small-signal equivalent circuit

can find the small-signal voltage gain as a function of frequency. Using the impedance reflection rule, the small-signal input current is

$$I_b = \frac{V_i}{R_S + r_\pi + (1+\beta)\left(R_E \| \frac{1}{sC_E}\right)} \tag{7.54}$$

The total impedance in the emitter is multiplied by the factor $(1+\beta)$. The control voltage is

$$V_\pi = I_b r_\pi \tag{7.55}$$

and the output voltage is

$$V_o = -g_m V_\pi R_C \tag{7.56}$$

Combining equations produces the small-signal voltage gain, as follows:

$$A_v(s) = \frac{V_o(s)}{V_i(s)} = \frac{-g_m r_\pi R_C}{R_S + r_\pi + (1+\beta)\left(R_E \| \frac{1}{sC_E}\right)} \tag{7.57}$$

Expanding the parallel combination of R_E and $1/sC_E$ and rearranging terms, we find

$$A_v = \frac{-g_m r_\pi R_C}{[R_S + r_\pi + (1+\beta)R_E]} \times \frac{(1+sR_E C_E)}{\left\{1 + \frac{sR_E(R_S + r_\pi)C_E}{[R_S + r_\pi + (1+\beta)R_E]}\right\}} \tag{7.58}$$

Equation (7.58) can be written in terms of time constants as

$$A_v = \frac{-g_m r_\pi R_C}{[R_S + r_\pi + (1+\beta)R_E]} \left\{\frac{1+s\tau_A}{1+s\tau_B}\right\} \tag{7.59}$$

The form of this transfer function is somewhat different from what we have previously encountered in that we have both a zero and a pole.

The Bode plot of the voltage gain magnitude has two limiting horizontal asymptotes. If we set $s = j\omega$, we can then consider the limit as $\omega \to 0$ and the limit as $\omega \to \infty$. For $\omega \to 0$, C_E acts as an open circuit; for $\omega \to \infty$, C_E acts as a short circuit. From Equation (7.58), we have

$$|A_v|_{\omega \to 0} = \frac{g_m r_\pi R_C}{[R_S + r_\pi + (1+\beta)R_E]} \tag{7.60(a)}$$

and

$$|A_v|_{\omega \to \infty} = \frac{g_m r_\pi R_C}{R_S + r_\pi} \tag{7.60(b)}$$

From these results, we see that for $\omega \to 0$, R_E is included in the gain expression, and for $\omega \to \infty$, R_E is not part of the gain expression, since it has been effectively shorted out by C_E.

If we assume that the time constants τ_A and τ_B in Equation (7.59) differ substantially in magnitude, then the corner frequency due to τ_B is

$$f_B = \frac{1}{2\pi\tau_B} \tag{7.61(a)}$$

and the corner frequency due to τ_A is

$$f_A = \frac{1}{2\pi\tau_A} \tag{7.61(b)}$$

The resulting Bode plot of the voltage gain magnitude is shown in Figure 7.24.

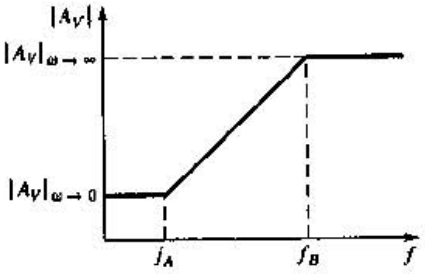


Figure 7.24 Bode plot of the voltage gain magnitude for the circuit with an emitter bypass capacitor

Example 7.8 **Objective:** Determine the corner frequencies and limiting horizontal asymptotes of a common-emitter circuit with an emitter bypass capacitor.

Consider the circuit in Figure 7.23(a) with parameters $R_E = 4\,\text{k}\Omega$, $R_C = 2\,\text{k}\Omega$, $R_S = 0.5\,\text{k}\Omega$, $C_E = 1\,\mu\text{F}$, $V^+ = 5\,\text{V}$, and $V^- = -5\,\text{V}$. The transistor parameters are: $\beta = 100$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, and $r_o = \infty$.

Solution: From the dc analysis, we find the quiescent collector current as $I_{CQ} = 1.06\,\text{mA}$. The transconductance is

$$g_m = \frac{I_{CQ}}{V_T} = \frac{1.06}{0.026} = 40.8\,\text{mA/V}$$

and the input base resistance is

$$r_\pi = \frac{\beta V_T}{I_{CQ}} = \frac{(100)(0.026)}{1.06} = 2.45\,\text{k}\Omega$$

The time constant τ_A is

$$\tau_A = R_E C_E = (4 \times 10^3)(1 \times 10^{-6}) = 4 \times 10^{-3}\,\text{s}$$

and the time constant τ_B is

$$\tau_B = \frac{R_E(R_S + r_\pi)C_E}{[R_S + r_\pi + (1+\beta)R_E]}$$
$$= \frac{(4 \times 10^3)(0.5 \times 10^3 + 2.45 \times 10^3)(1 \times 10^{-6})}{[0.5 \times 10^3 + 2.45 \times 10^3 + (101)(4 \times 10^3)]}$$

or

$$\tau_B = 2.90 \times 10^{-5}\,\text{s}$$

The corner frequencies are then

$$f_A = \frac{1}{2\pi\tau_A} = \frac{1}{2\pi(4 \times 10^{-3})} = 39.8\,\text{Hz}$$

and

$$f_B = \frac{1}{2\pi\tau_B} = \frac{1}{2\pi(2.9 \times 10^{-5})} \Rightarrow 5.49\,\text{kHz}$$

The limiting low-frequency horizontal asymptote, given by Equation (7.60(a)) is

$$|A_v|_{\omega \to 0} = \frac{g_m r_\pi R_C}{[R_S + r_\pi + (1+\beta)R_E]} = \frac{(40.8)(2.45)(2)}{[0.5 + 2.45 + (101)(4)]}$$

or

$$|A_v|_{\omega \to 0} = 0.49$$

The limiting high-frequency horizontal asymptote, given by Equation (7.60(b)) is

$$|A_v|_{\omega \to \infty} = \frac{g_m r_\pi R_C}{R_S + r_\pi} = \frac{(40.8)(2.45)(2)}{0.5 + 2.45} = 67.8$$

Comment: Comparing the two limiting values of voltage gain, we see that including a bypass capacitor produces a large high-frequency gain.

Computer Verification: The results of a PSpice analysis are given in Figure 7.25. The magnitude of the small-signal voltage gain is shown in Figure 7.25(a). The two corner frequencies are approximately 39 Hz and 5600 Hz, which agree very well with the results

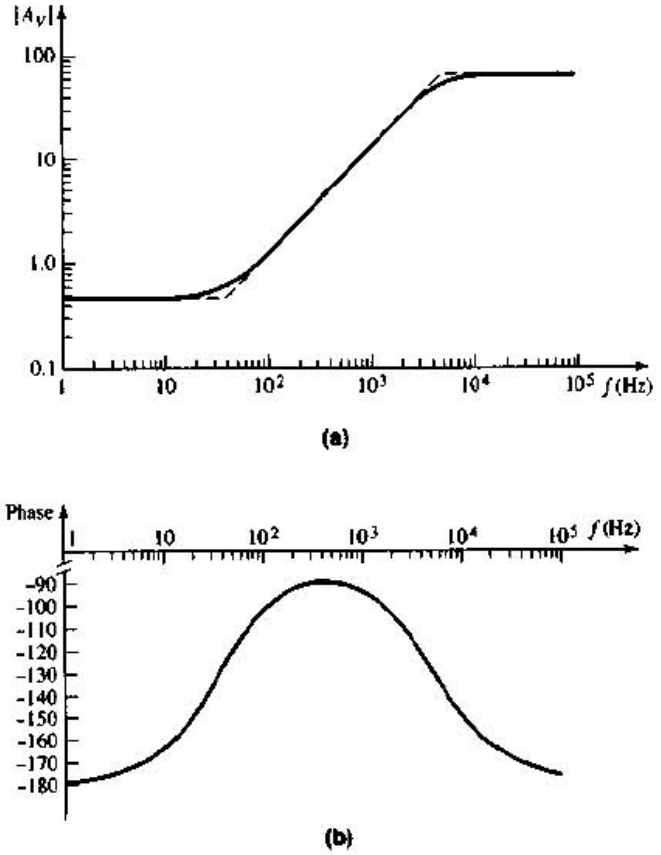


Figure 7.25 PSpice analysis results for the circuit with an emitter bypass capacitor: (a) voltage gain magnitude response and (b) phase response

from the time constant analysis. The two limiting magnitudes of 0.49 and 68 also correlate extremely well with the hand analysis results.

Figure 7.25(b) is a plot of the phase response versus frequency. At very low and very high frequencies, where the capacitor acts as either an open circuit or short circuit, the phase is −180 degrees, as expected for a common-emitter circuit. Between the two corner frequencies, the phase changes substantially, approaching −90 degrees.

The analysis of an FET amplifier with a source bypass capacitor is essentially the same as for the bipolar circuit. The general form of the voltage gain expression is the same as Equation (7.59), and the Bode plot of the gain is essentially the same as that shown in Figure 7.24.

Test Your Understanding

***7.11** The circuit shown in Figure 7.23(a) has parameters $V^+ = 10\,\text{V}$, $V^- = -10\,\text{V}$, $R_S = 0.5\,\text{k}\Omega$, $R_E = 4\,\text{k}\Omega$, and $R_C = 2\,\text{k}\Omega$. The transistor parameters are: $V_{BE}(\text{on}) = 0.7\,\text{V}$, $V_A = \infty$, and $\beta = 100$. (a) Determine the value of C_E such that the low-frequency 3 dB point is $f_B = 200\,\text{Hz}$. (b) Using the results from part (a), determine f_A. (Ans. (a) $C_E = 49.5\,\mu\text{F}$, (b) $f_A = 0.80\,\text{Hz}$)

7.3.5 Combined Effects: Coupling and Bypass Capacitors

When a circuit contains multiple capacitors, the frequency response analysis becomes more complex. In many amplifier applications, the circuit is to amplify an input signal whose frequency is confined to the midband range. In this case, the actual frequency response outside the midband range is not of interest. The end points of the midband range are defined to be those frequencies at which the gain decreases by 3 dB from the maximum midband value. These endpoint frequencies are a function of the high- and low-frequency capacitors. These capacitors introduce a pole to the amplifier transfer function.

If multiple coupling capacitors, for example, exist in a circuit, one capacitor may introduce the pole that produces the 3 dB reduction in the maximum gain at the low frequency. This pole is referred to as the **dominant pole**. A more detailed discussion of dominant poles is given in Chapter 12. At this point in the text, we will determine the frequency response of circuits containing multiple capacitors with a computer simulation.

As an example, Figure 7.26 shows a circuit with two coupling capacitors and an emitter bypass capacitor, all of which affect the circuit response at low frequencies. We could develop a transfer function that includes all the capacitors, but the analysis of such circuits is most easily handled by computer.

Figure 7.27 is the Bode plot of the voltage gain magnitude for the example circuit, taking into account the effects of the two coupling capacitors. In this case, the bypass capacitor is assumed to be a short circuit. The plots consider C_1 and C_2 individually, as well as together. As expected, with two capacitors both acting at the same time, the slope is 40 dB/decade or 12 dB/octave. Since the poles are not far apart, in the actual circuit, we cannot consider the effect of each capacitor individually.

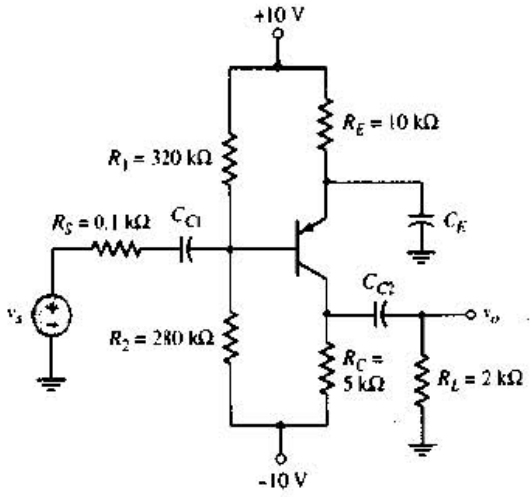


Figure 7.26 Circuit with two coupling capacitors and an emitter bypass capacitor

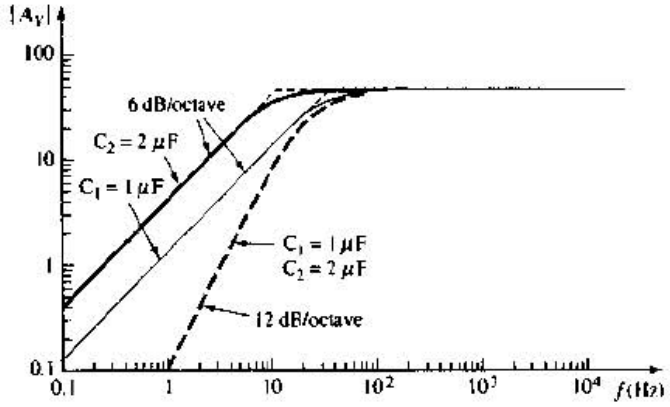


Figure 7.27 PSpice results for each coupling capacitor, and the combined effect for the circuit in Figure 7.26 ($C_E \to \infty$)

Figure 7.28 is the Bode plot of the voltage gain magnitude, taking into account the emitter bypass capacitor and the two coupling capacitors. The plot shows the effect of the bypass capacitor, the effect of the two coupling capacitors, and the net effect of the three capacitors together. When all three capacitors are taken into account, the slope is continually changing; there is no definitive corner frequency. However, at approximately $f = 150$ Hz, the curve is 3 dB below the maximum asymptotic value, and this frequency is defined as the **lower corner frequency**, or **lower cutoff frequency**.

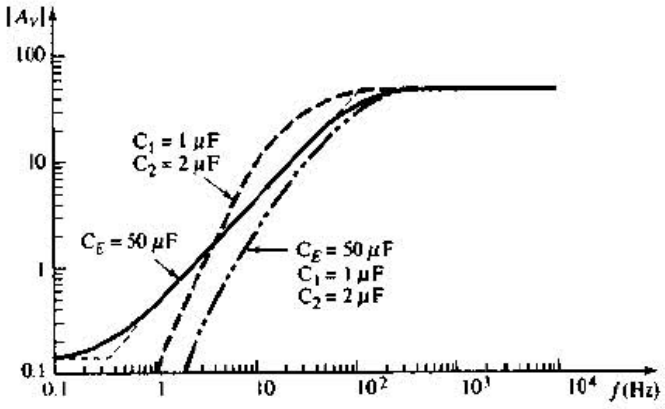


Figure 7.28 PSpice results for the two coupling capacitors, the bypass capacitor, and the combined effects

Test Your Understanding

***7.12** Consider the common-base circuit shown in Figure 7.29. Can the two coupling capacitors be treated separately? (a) From a computer analysis, determine the cutoff frequency. Assume the parameter values are $\beta = 100$ and $I_S = 2 \times 10^{-15}$ A. (b) Determine the midband small-signal voltage gain. (Ans. (a) $f_{3\,dB} = 1.2$ kHz, (b) $A_v = 118$)

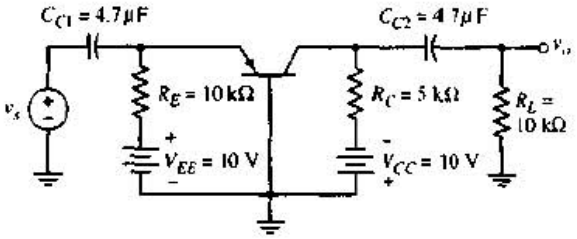


Figure 7.29 Figure for Exercise 7.12

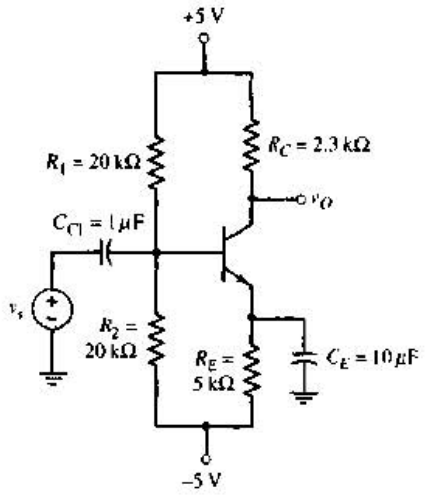


Figure 7.30 Figure for Exercise 7.13

***7.13** The common-emitter circuit shown in Figure 7.30 contains both a coupling capacitor and an emitter bypass capacitor. (a) From a computer analysis, determine the 3 dB frequency. Assume the parameter values are $\beta = 100$ and $I_S = 2 \times 10^{-15}$ A. (b) Determine the midband small-signal voltage gain. (Ans. (a) $f_{3dB} \approx 575$ Hz, (b) $|A_v|_{max} = 74.4$)

7.4 FREQUENCY RESPONSE: BIPOLAR TRANSISTOR

Thus far, we have considered the frequency response of circuits as a function of external resistors and capacitors, and we have assumed the transistor to be ideal. However, both bipolar transistors and FETs have internal capacitances that influence the high-frequency response of circuits. In this section, we will first develop an expanded small-signal hybrid-π model of the bipolar transistor, taking these capacitances into account. We will then use this model to analyze the frequency characteristics of the bipolar transistor.

7.4.1 Expanded Hybrid-π Equivalent Circuit

When a bipolar transistor is used in a linear amplifier circuit, the transistor is biased in the forward-active region, and small sinusoidal voltages and currents are superimposed on the dc voltages and currents. Figure 7.31(a) shows an npn bipolar transistor in a common-emitter configuration, along with the small-signal voltages and currents. Figure 7.31(b) is a cross section of the npn transistor in a classic integrated circuit configuration. The C, B, and E terminals are the external connections to the transistor, and the C′, B′, and E′ points are the idealized internal collector, base, and emitter regions.

To construct the equivalent circuit of the transistor, we will first consider various pairs of terminals. Figure 7.32(a) shows the equivalent circuit for the connection between the external base input terminal and the external emitter terminal. Resistance r_b is the base series resistance between the external base

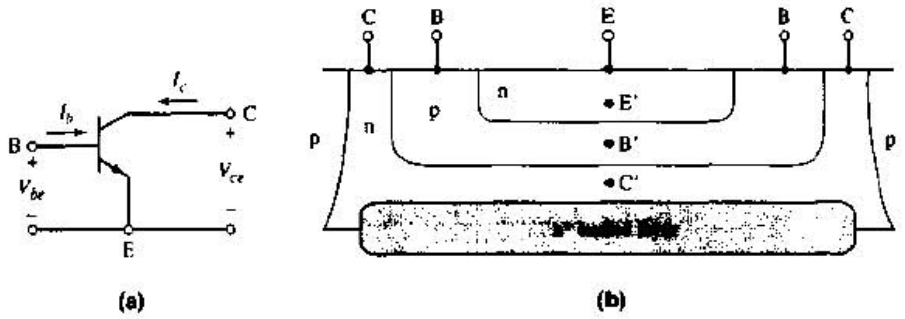


Figure 7.31 (a) Common-emitter npn bipolar transistor with small-signal currents and voltages and (b) cross section of an npn bipolar transistor, for the hybrid-π model

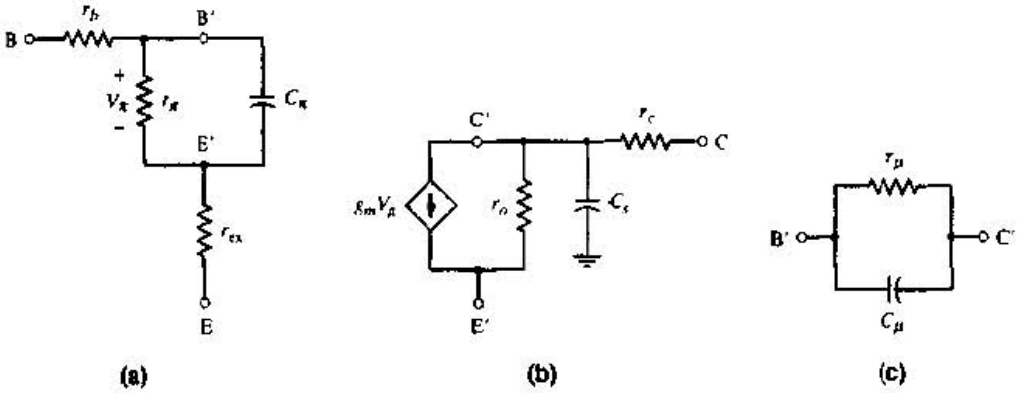


Figure 7.32 Components of the hybrid-π equivalent circuit: (a) base to emitter, (b) collector to emitter, and (c) base to collector

terminal B and the internal base region B′, the B′–E′ junction is forward biased; therefore, C_π is the forward-biased junction capacitance and r_π is the forward-biased junction diffusion resistance. Both parameters are functions of the junction current. Finally, r_{ex} is the emitter series resistance between the external emitter terminal and the internal emitter region. This resistance is usually very small, on the order of 1 to 2 Ω.

Figure 7.32(b) shows the equivalent circuit looking into the collector terminal. Resistance r_c is the collector series resistance between the external and internal collector connections, and capacitance C_s is the junction capacitance of the reverse-biased collector–substrate junction. The dependent current source, $g_m V_\pi$, is the transistor collector current controlled by the internal base–emitter voltage. Resistance r_o is the inverse of the output conductance g_o and is due primarily to the Early effect.

Finally, Figure 7.32(c) shows the equivalent circuit of the reverse-biased B′–C′ junction. Capacitance C_μ is the reverse-biased junction capacitance, and r_μ is the reverse-biased diffusion resistance. Normally, r_μ is on the order of megohms and can be neglected. The value of C_μ is usually much smaller than C_π; however, because of a phenomenon known as the Miller effect, C_μ usually cannot be neglected. (We will consider the Miller effect later in this chapter.)

The complete hybrid-π equivalent circuit for the bipolar transistor is shown in Figure 7.33. The capacitances lead to frequency effects in the transistor. One

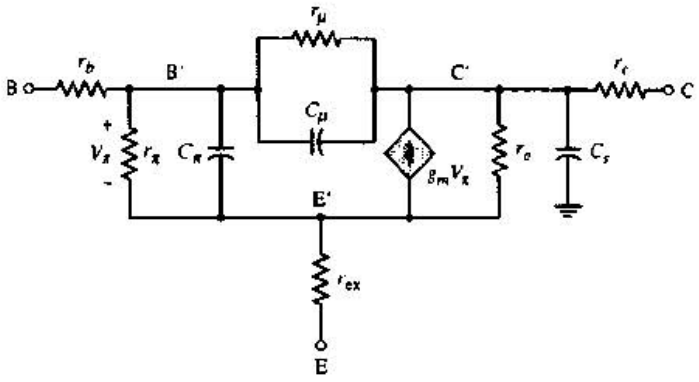


Figure 7.33 Hybrid-π equivalent circuit

result is that the gain is a function of the input signal frequency. Because of the large number of elements, a computer simulation of this complete model is easier than a hand analysis. However, we can make some simplifications in order to evaluate some fundamental frequency effects of bipolar transistors.

7.4.2 Short-Circuit Current Gain

We can begin to understand the frequency effects of the bipolar transistor by first determining the **short-circuit current gain**, after simplifying the hybrid-π model. Figure 7.34 shows a simplified equivalent circuit for the transistor, in which we neglect the parasitic resistances r_b, r_c, and r_{ex}, the B–C diffusion resistance r_μ, and the substrate capacitance C_s. Also, the collector is connected to signal ground. Keep in mind that the transistor must still be biased in the forward-active region. We will determine the small-signal current gain $A_i = I_c/I_b$.

Writing a KCL equation at the input node, we find that

$$I_b = \frac{V_\pi}{r_\pi} + \frac{V_\pi}{\dfrac{1}{j\omega C_\pi}} + \frac{V_\pi}{\dfrac{1}{j\omega C_\mu}} = V_\pi\left[\frac{1}{r_\pi} + j\omega(C_\pi + C_\mu)\right] \tag{7.62}$$

We see that V_π is no longer equal to $I_b r_\pi$, since a portion of I_b is now shunted through C_π and C_μ.

From a KCL equation at the output node, we obtain

$$\frac{V_\pi}{\dfrac{1}{j\omega C_\mu}} + I_c = g_m V_\pi \tag{7.63(a)}$$

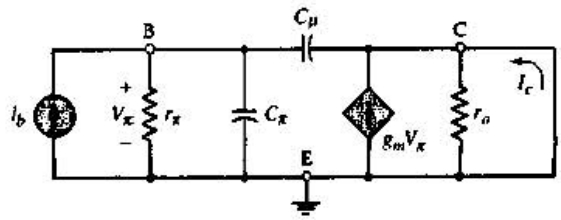


Figure 7.34 Simplified hybrid-π equivalent circuit for determining the short-circuit current gain

or

$$I_c = V_\pi(g_m - j\omega C_\mu) \tag{7.63(b)}$$

The input voltage V_π can then be written as

$$V_\pi = \frac{I_c}{(g_m - j\omega C_\mu)} \tag{7.63(c)}$$

Substituting this expression for V_π into Equation (7.62) yields

$$I_b = I_c \cdot \frac{\left[\frac{1}{r_\pi} + j\omega(C_\pi + C_\mu)\right]}{(g_m - j\omega C_\mu)} \tag{7.64}$$

The small-signal current gain usually designated as h_{fe}, becomes

$$A_i = \frac{I_c}{I_b} = h_{fe} = \frac{(g_m - j\omega C_\mu)}{\left[\frac{1}{r_\pi} + j\omega(C_\pi + C_\mu)\right]} \tag{7.65}$$

If we assume typical circuit parameter values of $C_\mu = 0.2\,\text{pF}, g_m = 50\,\text{mA/V}$, and a maximum frequency of $f = 100\,\text{MHz}$, then we see that $\omega C_\mu \ll g_m$. Therefore, to a good approximation, the small-signal current gain is

$$h_{fe} \cong \frac{g_m}{\left[\frac{1}{r_\pi} + j\omega(c_\pi + C_\mu)\right]} = \frac{g_m r_\pi}{1 + j\omega r_\pi(C_\pi + C_\mu)} \tag{7.66}$$

Since $g_m r_\pi = \beta$, then the low frequency current gain is just β, as we previously assumed. Equation (7.66) shows that, in a bipolar transistor, the magnitude and phase of the current gain are both functions of the frequency.

Figure 7.35(a) is a Bode plot of the short-circuit current gain magnitude. The corner frequency, which is also the **beta cutoff frequency** f_β in this case, is given by

$$f_\beta = \frac{1}{2\pi r_\pi(C_\pi + C_\mu)} \tag{7.67}$$

Figure 7.35(b) shows the phase of the current gain. As the frequency increases, the small-signal collector current is no longer in phase with the

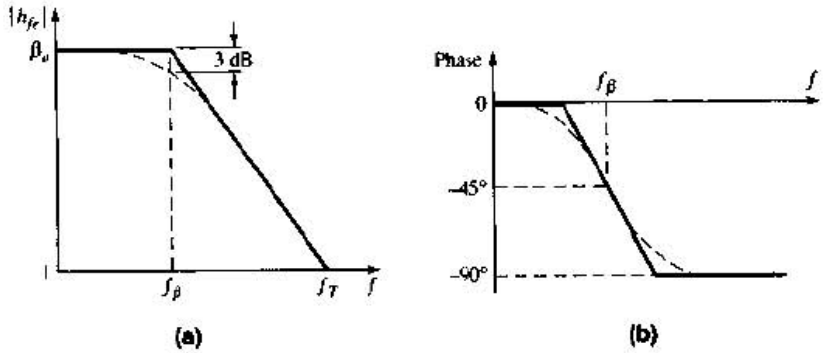


Figure 7.35 Bode plots for the short-circuit current gain: (a) magnitude and (b) phase

small-signal base current. At high frequencies, the collector current lags the input current by 90 degrees.

Example 7.9 **Objective:** Determine the 3 dB frequency of the short-circuit current gain of a bipolar transistor.

Consider a bipolar transistor with parameters $r_\pi = 2.6\,\text{k}\Omega$, $C_\pi = 2\,\text{pF}$, and $C_\mu = 0.1\,\text{pF}$.

Solution: From Equation (7.67), we have

$$f_\beta = \frac{1}{2\pi r_\pi (C_\pi + C_\mu)} = \frac{1}{2\pi(2.6 \times 10^3)(2 + 0.1)(10^{-12})}$$

or

$$f_\beta = 29.1\,\text{MHz}$$

Comment: High-frequency transistors must have small capacitances; therefore, small devices must be used.

Test Your Understanding

7.14 A bipolar transistor has parameters $\beta_o = 150$, $C_\pi = 2\,\text{pF}$, and $C_\mu = 0.3\,\text{pF}$, and is biased at $I_{CQ} = 0.5\,\text{mA}$. Determine the beta cutoff frequency. (Ans. $f_\beta = 8.87\,\text{MHz}$)

7.15 A BJT is biased at $I_{CQ} = 0.25\,\text{mA}$, and its parameters are $\beta_o = 100$ and $C_\mu = 0.1\,\text{pF}$. The beta cutoff frequency is $f_\beta = 11.5\,\text{MHz}$. Determine the capacitance C_π. (Ans. $C_\pi = 1.23\,\text{pF}$)

7.4.3 Cutoff Frequency

Figure 7.35(a) shows that the magnitude of the small-signal current gain decreases with increasing frequency. At frequency f_T, which is the **cutoff frequency**, this gain goes to 1. The cutoff frequency is a figure of merit for transistors.

From Equation (7.66), we can write the small-signal current gain in the form

$$h_{fe} = \frac{\beta_o}{1 + j\left(\frac{f}{f_\beta}\right)} \tag{7.68}$$

where f_β is the beta cutoff frequency defined by Equation (7.67). The magnitude of h_{fe} is

$$|h_{fe}| = \frac{\beta_o}{\sqrt{1 + \left(\frac{f}{f_\beta}\right)^2}} \tag{7.69}$$

At the cutoff frequency f_T, $|h_{fe}| = 1$, and Equation (7.69) becomes

$$|h_{fe}| = 1 = \frac{\beta_o}{\sqrt{1 + \left(\frac{f_T}{f_\beta}\right)^2}} \tag{7.70}$$

Normally, $\beta_o \gg 1$, which implies that $f_T \gg f_\beta$. Then Equation (7.70) can be written as

$$1 \cong \frac{\beta_o}{\sqrt{\left(\frac{f_T}{f_\beta}\right)^2}} = \frac{\beta_o f_\beta}{f_T} \tag{7.71(a)}$$

or

$$f_T = \beta_o f_\beta \tag{7.71(b)}$$

Frequency f_β is also called the bandwidth of the transistor. Therefore, from Equation (7.71(b)), the cutoff frequency f_T is the gain–bandwidth product of the transistor, or more commonly the **unity-gain bandwidth**. From Equation (7.67), the unity-gain bandwidth is

$$f_T = \beta_o \left[\frac{1}{2\pi r_\pi (C_\pi + C_\mu)}\right] = \frac{g_m}{2\pi(C_\pi + C_\mu)} \tag{7.72}$$

Since the capacitances are a function of the size of the transistor, we see again that high frequency transistors imply small device sizes.

The cutoff frequency f_T is also a function of the dc collector current I_C, and the general characteristic of f_T versus I_C is shown in Figure 7.36. The transconductance g_m is directly proportional to I_C, but only a portion of C_π is related to I_C. The cutoff frequency is therefore lower at low collector current levels. However, the cutoff frequency also decreases at high current levels, in the same way that β decreases at large currents.

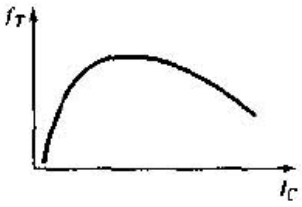


Figure 7.36 Cutoff frequency versus collector current

The cutoff frequency or unity-gain bandwidth of a transistor is usually specified on the device data sheets. Since the low-frequency current gain is also given, the beta cutoff frequency, or bandwidth, of the transistor can be determined from

$$f_\beta = \frac{f_T}{\beta_o} \tag{7.73}$$

The cutoff frequency of the general-purpose 2N2222A discrete bipolar transistor is $f_T = 300\,\text{MHz}$. For the MSC3130 discrete bipolar transistor, which has a special surface mount package, the cutoff frequency is $f_T = 1.4\,\text{GHz}$. This tells us that very small transistors fabricated in integrated circuits can have cutoff frequencies in the low GHz range.

Example 7.10 **Objective:** Calculate the bandwidth f_β and capacitance C_π of a bipolar transistor.

Consider a transistor that has parameters $f_T = 500\,\text{MHz}$ at $I_C = 1\,\text{mA}$, $\beta_o = 100$, and $C_\mu = 0.3\,\text{pF}$.

Solution: From Equation (7.73), the bandwidth is

$$f_\beta = \frac{f_T}{\beta_o} = \frac{500}{100} = 5\,\text{MHz}$$

The transconductance is

$$g_m = \frac{I_C}{V_T} = \frac{1}{0.026} = 38.5\,\text{mA/V}$$

The C_π capacitance is determined from Equation (7.72). We have

$$f_T = \frac{g_m}{2\pi(C_\pi + C_\mu)}$$

or

$$500 \times 10^6 = \frac{38.5 \times 10^{-3}}{2\pi(C_\pi + 0.3 \times 10^{-12})}$$

which yields $C_\pi = 12.0\,\text{pF}$.

Comment: Although the value of C_π may be much larger than that of C_μ, C_μ cannot be neglected in circuit applications as we will see in the next section.

The hybrid-π equivalent circuit for the bipolar transistor uses discrete or lumped elements. However, when cutoff frequencies are on the order of $f_T \cong 1\,\text{GHz}$ and the transistor is operated at microwave frequencies, other parasitic elements and distributed parameters must be included in the transistor model. For simplicity, we will assume in this text that the hybrid-π model is sufficient to model the transistor characteristics up through the beta cutoff frequency.

Test Your Understanding

7.16 For the transistor described in Example 7.10 and biased at the same Q-point, determine $|h_{fe}|$ and the phase at $f = 50\,\text{MHz}$. (Ans. $|h_{fe}| = 9.95$, Phase $= -84.3°$)

7.17 The parameters of a transistor are: $\beta_o = 120$, $f_T = 500\,\text{MHz}$, $r_x = 5\,\text{k}\Omega$, and $C_\mu = 0.2\,\text{pF}$. Determine C_π and f_β. (Ans. $f_\beta = 4.17\,\text{MHz}$, $C_\pi = 7.43\,\text{pF}$)

7.18 A BJT is biased at $I_C = 1\,\text{mA}$, and its parameters are: $\beta_o = 150$, $C_\pi = 4\,\text{pF}$, and $C_\mu = 0.5\,\text{pF}$. Determine f_β and f_T. (Ans. $f_\beta = 9.07\,\text{MHz}$, $f_T = 1.36\,\text{GHz}$)

7.4.4 Miller Effect and Miller Capacitance

As previously mentioned, the C_μ capacitance cannot in reality be ignored. The **Miller effect**, or feedback effect, is a multiplication effect of C_μ in circuit appliations.

Figure 7.37(a) is a common-emitter circuit with a signal current source at the input. We will determine the small-signal current gain $A_i = i_o/i_s$ of the circuit. Figure 7.37(b) is the small-signal equivalent circuit, assuming the frequency is sufficiently high for the coupling and bypass capacitors to act as short circuits. The transistor model is the simplified hybrid-π circuit in

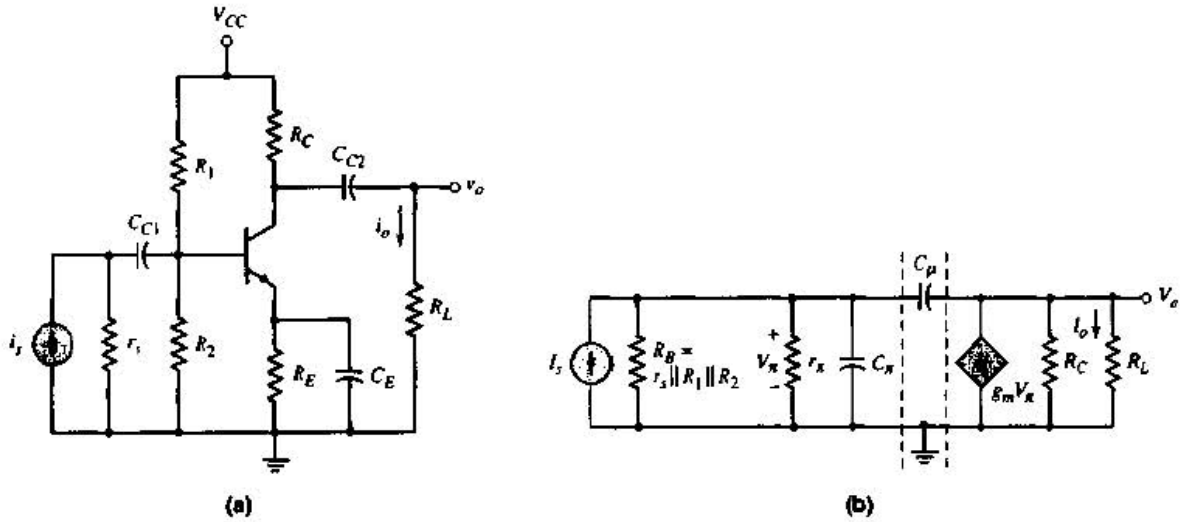


Figure 7.37 (a) Common-emitter circuit with current source input; (b) small-signal equivalent circuit with simplified hybrid-π model

Figure 7.34 (assuming $r_o = \infty$). Capacitor C_μ is a feedback element that connects the output back to the input. The output voltage and current will therefore influence the input characteristics.

We can determine the effect of C_μ on the input characteristics by finding an equivalent impedance Z_A across the plane A-A in Figure 7.38(a), producing the equivalent circuit shown in Figure 7.38(b). The current I_1 from Figure 7.38(a) can be written as

$$I_1 = \frac{V_\pi - V_o}{(1/j\omega C_\mu)} = (V_\pi - V_o)(j\omega C_\mu) \tag{7.74}$$

Summing the currents at the output gives

$$I_1 = (V_\pi - V_o)(j\omega C_\mu) = g_m V_\pi + \frac{V_o}{R_C \| R_L} \tag{7.75(a)}$$

or combining terms, we have

$$V_\pi(j\omega C_\mu - g_m) = V_o\left(\frac{1}{R_C \| R_L} + j\omega C_\mu\right) \tag{7.75(b)}$$

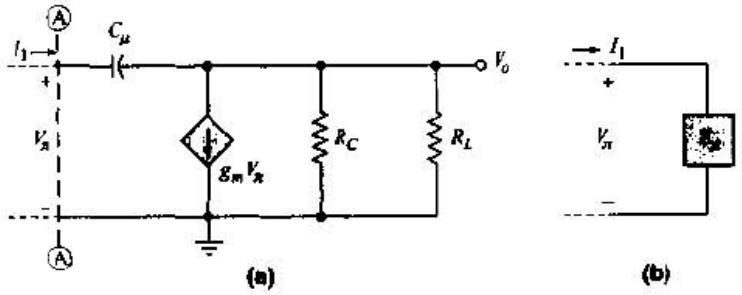


Figure 7.38 (a) Output portion of small-signal equivalent circuit; (b) equivalent impedance of this portion of the circuit

From our previous discussion of Equation (7.65), we noted that $|j\omega C_\mu| \ll g_m$ for typical transistor parameters, so the left side of Equation (7.75(b)) is just $-g_m V_\pi$. If, for example, $R_C = R_L = 4\,\text{k}\Omega$ and $C_\mu = 0.2\,\text{pF}$, then $|j\omega C_\mu| \ll 1/(R_C \| R_L)$ for $f \ll 400\,\text{MHz}$. If this condition is valid, then Equation (7.75(b)) becomes

$$-g_m V_\pi \cong V_o\left(\frac{1}{R_C \| R_L}\right) \tag{7.76(a)}$$

or

$$V_o = -g_m(R_C \| R_L)V_\pi \tag{7.76(b)}$$

Substituting this expression for V_o into Equation (7.74) yields

$$I_1 = \{V_\pi - [-g_m(R_C \| R_L)V_\pi]\}j\omega C_\mu \tag{7.77(a)}$$

or

$$I_1 = V_\pi \cdot j\omega C_\mu[1 + g_m(R_C R_L)] \tag{7.77(b)}$$

From Equation (7.77(b)), we see that the equivalent impedance Z_A in Figure 7.38(b) then corresponds to a capacitance whose value is

$$C_M = C_\mu[1 + g_m(R_C \| R_L)] \tag{7.78}$$

The small-signal equivalent circuit in Figure 7.37(b) can be redrawn as shown in Figure 7.39. Capacitance C_M is called the **Miller capacitance** and the multiplication effect of C_μ is called the **Miller effect**. [Note: If the condition $|j\omega C_\mu| \ll 1/(R_C \| R_L)$ is not valid, then the C_μ capacitance is also reflected in the output circuit.

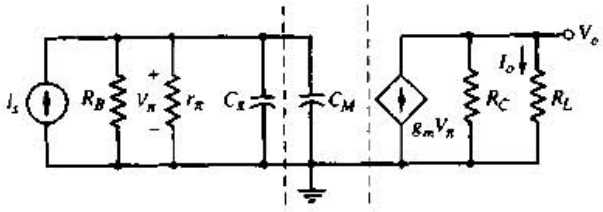


Figure 7.39 Small-signal equivalent circuit, including the equivalent Miller capacitance

From the equivalent circuit in Figure 7.39, the input capacitance is now $C_\pi + C_M$, rather than just C_π if C_μ had been ignored.

Example 7.11 **Objective:** Determine the 3 dB frequency of the current gain for the circuit shown in Figure 7.39, both with and without the effect of C_M.

The circuit parameters are: $R_C = R_L = 4\,\text{k}\Omega$, $r_\pi = 2.6\,\text{k}\Omega$, $R_B = 200\,\text{k}\Omega$, $C_\pi = 4\,\text{pF}$, $C_\mu = 0.2\,\text{pF}$, and $g_m = 38.5\,\text{mA/V}$.

Solution: The output current can be written as

$$I_o = -(g_m V_\pi)\left(\frac{R_C}{R_C + R_L}\right)$$

Also, the input voltage is

$$V_\pi = I_s\left[R_B \| r_\pi \left\| \frac{1}{j\omega C_\pi} \right\| \frac{1}{j\omega C_M}\right]$$
$$= I_s\left[\frac{R_B \| r_\pi}{1 + j\omega(R_B \| r_\pi)(C_\pi + C_M)}\right]$$

Therefore, the current gain is

$$A_i = \frac{I_o}{I_s} = -g_m\left(\frac{R_C}{R_C + R_L}\right)\left[\frac{R_B \| r_\pi}{1 + j\omega(R_B \| r_\pi)(C_\pi + C_M)}\right]$$

The 3 dB frequency is

$$f_{3\,dB} = \frac{1}{2\pi(R_B \| r_\pi)(C_\pi + C_M)}$$

Neglecting the effect of $C_\mu (C_M = 0)$, we find that

$$f_{3\,dB} = \frac{1}{2\pi[(200 \times 10^3) \| (2.6 \times 10^3)](4 \times 10^{-12})} \Rightarrow 15.5\,\text{MHz}$$

The Miller capacitance is

$$C_M = C_\mu[1 + g_m(R_C \| R_L)] = (0.2)[1 + (38.5)(4 \| 4)] = 15.6\,\text{pF}$$

Taking into account the Miller capacitance, the 3 dB frequency is

$$f_{3\,dB} = \frac{1}{2\pi(R_B \| r_\pi)(C_\pi + C_M)}$$
$$= \frac{1}{2\pi[(200 \times 10^3) \| (2.6 \times 10^3)][4 + 15.6](10^{-12})}$$

or

$$f_{3\,dB} = 3.16\,\text{MHz}$$

Comment: The Miller effect, or multiplication factor of C_μ, is 78, giving a Miller capacitance of $C_M = 15.6\,\text{pF}$. The Miller capacitance, in this case, is approximately a factor of four larger than C_π. This means that the actual transistor bandwidth is approximately five times less than the bandwidth expected if C_μ is neglected.

The Miller capacitance, from Equation (7.78), can be written in the form

$$C_M = C_\mu(1 + |A_v|) \tag{7.79}$$

where A_v is the internal base-to-collector voltage gain. The physical origin of the Miller effect is in the voltage gain factor appearing across the feedback element C_μ. A small input voltage V_π produces a large output voltage $V_o = -|A_v| \cdot V_\pi$ of the opposite polarity at the output of C_μ. Thus the voltage across C_μ is $(1 + |A_v|)V_\pi$, which induces a large current through C_μ. For this reason, the effect of C_μ on the input portion of the circuit is significant.

We can now see one of the trade-offs that can be made in an amplifier design. The tradeoff is between amplifier gain and bandwidth. If the gain is reduced, then the Miller capacitance will be reduced and the bandwidth will be increased. We will consider this tradeoff again when we consider the cascode amplifier later in the chapter.

Discussion: In Equation (7.75(b)), we assumed that $|j\omega C_\mu| \ll g_m$, which is valid even for frequencies in the 100 MHz range. Equation (7.75(b)) can then be written as

$$-g_m V_\pi = V_o\left(\frac{1}{R_C \| R_L} + j\omega C_\mu\right) \tag{7.80}$$

The right side of Equation (7.80) implies that a capacitance C_μ should be in parallel with R_C and R_L in the output portion of the equivalent circuit in Figure 7.39. For $R_C = R_L = 4\,\text{k}\Omega$ and $C_\mu = 0.2\,\text{pF}$, we indicated that this capacitance is negligible for $f \ll 400\,\text{MHz}$ [yielding Equation (7.76(a))]. However, in special circuits involving, for example, active loads, the equivalent R_C and R_L resistances may be on the order of $100\,\text{k}\Omega$. This means that the C_μ capacitance in the output part of the circuit is not negligible for frequencies even in the low-megahertz range. We will consider a few special cases in which C_μ in the output circuit is not negligible.

Test Your Understanding

***7.19** For the circuit in Figure 7.37(a), the parameters are: $R_1 = 200\,\text{k}\Omega$, $R_2 = 220\,\text{k}\Omega$, $R_C = 2.2\,\text{k}\Omega$, $R_L = 4.7\,\text{k}\Omega$, $R_E = 1\,\text{k}\Omega$, $r_x = 100\,\text{k}\Omega$, and $V_{CC} = 5\,\text{V}$. The transistor parameters are: $\beta_o = 100$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, $V_A = \infty$, $C_\pi = 10\,\text{pF}$, and $C_\mu = 2\,\text{pF}$. Using the simplified hybrid-π model shown in Figure 7.34, calculate: (a) the Miller capacitance, and (b) the 3 dB frequency. (Ans. (a) $C_M = 109\,\text{pF}$, (b) $f_{3\text{dB}} = 0.505\,\text{MHz}$)

7.5 FREQUENCY RESPONSE: THE FET

We have considered the expanded hybrid-π equivalent circuit of the bipolar transistor that models the high-frequency response of the transistor. We will now develop the high-frequency equivalent circuit of the FET that takes into account various capacitances in the device. We will develop the model for a MOSFET, but it also applies to JFETs and MESFETs.

7.5.1 High-Frequency Equivalent Circuit

We will construct the small-signal equivalent circuit of a MOSFET from the basic MOSFET geometry, as described in Chapter 5. Figure 7.40 shows a model based on the inherent capacitances and resistances in an n-channel MOSFET, as well as the elements representing the basic device equations.

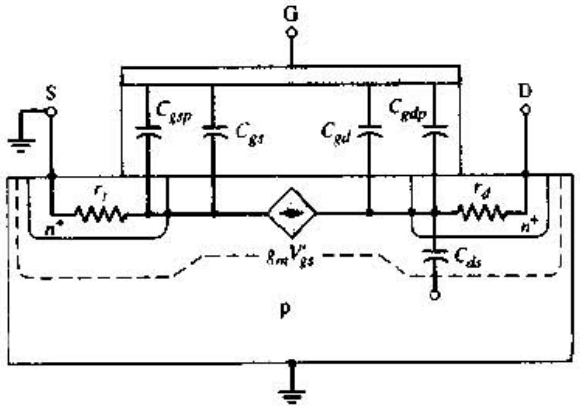


Figure 7.40 Inherent resistances and capacitances in the n-channel MOSFET structure

We make one simplifying assumption in the equivalent circuit: The source and substrate are both tied to ground.

Two capacitances connected to the gate are inherent in the transistor. These capacitances, C_{gs} and C_{gd}, represent the interaction between the gate and the channel inversion charge near the source and drain terminals, respectively. If the device is biased in the nonsaturation region and v_{DS} is small, the channel inversion charge is approximately uniform, which means that

$$C_{gs} \cong C_{gd} \cong \left(\frac{1}{2}\right) WLC_{ox}$$

where $C_{ox}(\text{F/cm}^2) = \epsilon_{ox}/t_{ox}$. The parameter ϵ_{ox} is the oxide permittivity, which for silicon MOSFETs is $\epsilon_{ox} = 3.9\epsilon_o$, where $\epsilon_o = 8.85 \times 10^{-14}$ F/cm is the permittivity of free space. The parameter t_{ox} is the oxide thickness in cm.

However, when the transistor is biased in the saturation region, the channel is pinched off at the drain and the inversion charge is no longer uniform. The value of C_{gd} essentially goes to zero, and C_{gs} approximately equals $(2/3)WLC_{ox}$. As an example, if a device has an oxide thickness of 500 Å, a channel length of $L = 5\,\mu$m, and a channel width of $W = 50\,\mu$m, the value of C_{gs} is $C_{gs} \cong 0.12$ pF. The value of C_{gs} changes as the device size changes, but typical values are in the tenths of picofarad range.

The remaining two gate capacitances, C_{gsp} and C_{gdp}, are parasitic or **overlap capacitances**, so called because, in actual devices, the gate oxide overlaps the source and drain contacts, because of tolerances or other fabrication factors. As we will see, the drain overlap capacitance C_{gdp} lowers the bandwidth of the FET. The parameter C_{ds} is the drain-to-substrate pn junction capacitance, and r_s and r_d are the series resistances of the source and drain terminals. The internal gate-to-source voltage controls the small-signal channel current through the transconductance.

The small-signal equivalent circuit for the n-channel common-source MOSFET is shown in Figure 7.41. Voltage V'_{gs} is the internal gate-to-source voltage that controls the channel current. We will assume that the gate-to-source and gate-to-drain capacitances, C_{gs} and C_{gd}, contain the parasitic overlap capacitances. One parameter, r_o, shown in Figure 7.41 is not shown in Figure 7.40. This resistance is associated with the slope of I_D versus V_{DS}. In the ideal MOSFET biased in the saturation region, I_D is independent of V_{DS}, which means that r_o is infinite. However, r_o is finite in short-channel-length

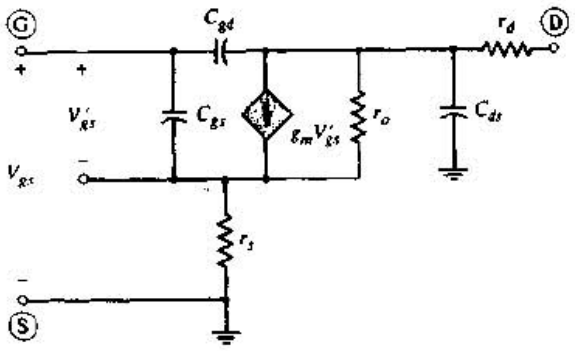


Figure 7.41 Equivalent circuit of the n-channel common-source MOSFET

devices, because of channel-length modulation, and is therefore included in the equivalent circuit.

Source resistance r_s can have a significant effect on the transistor characteristics. To illustrate, Figure 7.42 shows a simplified low-frequency equivalent circuit including r_s but not r_o. For this circuit, the drain current is

$$I_d = g_m V'_{gs} \tag{7.81}$$

and the relationship between V_{gs} and V'_{gs} is

$$V_{gs} = V'_{gs} + (g_m V'_{gs}) r_s = (1 + g_m r_s) V'_{gs} \tag{7.82}$$

From Equation (7.81), the drain current can now be written as

$$I_d = \left(\frac{g_m}{1 + g_m r_s}\right) V_{gs} = g'_m V_{gs} \tag{7.83}$$

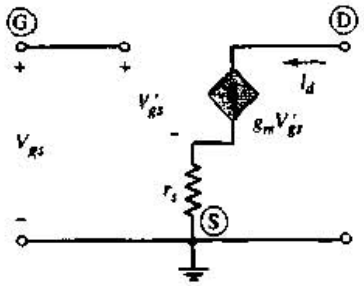


Figure 7.42 Simplified low-frequency equivalent circuit of the n-channel common-source MOSFET including source resistance r_s but not resistance r_o

Equation (7.83) shows that the source resistance reduces the effective transconductance, or the transistor gain.

The equivalent circuit of a p-channel MOSFET is exactly the same as that of an n-channel device, except that all voltage polarities and current directions are reversed. The capacitances and resistances are the same for both models.

Test Your Understanding

7.20 An n-channel MOSFET has parameters $K_n = 0.4\,\text{mA/V}^2$, $V_{TN} = 1\,\text{V}$, and $\lambda = 0$. (a) Determine the maximum source resistance such that the transconductance is reduced by no more than 20 percent from its ideal value when $V_{GS} = 3\,\text{V}$. (b) Using the value of r_s calculated in part (a), determine how much g_m is reduced from its ideal value when $V_{GS} = 5\,\text{V}$. (Ans. (a) $r_s = 156\,\Omega$, (b) 33.4%)

7.5.2 Unity-Gain Bandwidth

As for the bipolar transistor, the unity-gain frequency or bandwidth is a figure of merit for the FETs. If we neglect r_s, r_d, r_o, and C_{ds}, and connect the drain to signal ground, the resulting equivalent small-signal circuit is shown in Figure 7.43. Since the input gate impedance is no longer infinite at high frequency, we

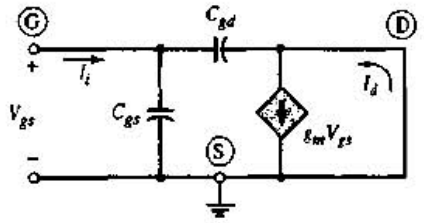


Figure 7.43 Equivalent high-frequency small-signal circuit of a MOSFET, for calculating short-circuit current gain

can define the short-circuit current gain. From that we can define and calculate the unity-gain bandwidth.

Writing a KCL equation at the input node, we find that

$$I_i = \frac{V_{gs}}{\frac{1}{j\omega C_{gs}}} + \frac{V_{gs}}{\frac{1}{j\omega C_{gd}}} = V_{gs}[j\omega(C_{gs} + C_{gd})] \tag{7.84}$$

From a KCL equation at the output node, we obtain

$$\frac{V_{gs}}{\frac{1}{j\omega C_{gd}}} + I_d = g_m V_{gs} \tag{7.85(a)}$$

or

$$I_d = V_{gs}(g_m - j\omega C_{gd}) \tag{7.85(b)}$$

Solving Equation (7.85(b)) for V_{gs} produces

$$V_{gs} = \frac{I_d}{(g_m - j\omega C_{gd})} \tag{7.86}$$

Substituting Equation (7.86) into (7.84) yields

$$I_i = I_d \cdot \frac{[j\omega(C_{gs} + C_{gd})]}{(g_m - j\omega C_{gd})} \tag{7.87}$$

Therefore, the small-signal current gain is

$$A_i = \frac{I_d}{I_i} = \frac{g_m - j\omega C_{gd}}{j\omega(C_{gs} + C_{gd})} \tag{7.88}$$

If we assume typical values of $C_{gd} = 0.05\,\text{pF}$ and $g_m = 1\,\text{mA/V}$, and a maximum frequency of $f = 100\,\text{MHz}$, we find that $\omega C_{gd} \ll g_m$. The small-signal current gain, to a good approximation, is then

$$A_i = \frac{I_d}{I_i} \cong \frac{g_m}{j\omega(C_{gs} + C_{gd})} \tag{7.89}$$

The unity-gain frequency f_T is defined as the frequency at which the magnitude of the short-circuit current gain goes to 1. From Equation (7.89) we find that

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \tag{7.90}$$

The unity-gain frequency or bandwidth is a parameter of the transistor and is independent of the circuit.

Example 7.12 **Objective:** Determine the unity-gain bandwidth of an FET.

Consider an n-channel MOSFET with parameters $K_n = 0.25\text{mA/V}^2$, $V_{TN} = 1\text{ V}$, $\lambda = 0$, $C_{gd} = 0.04\text{ pF}$, and $C_{gs} = 0.2\text{ pF}$. Assume the transistor is biased at $V_{GS} = 3\text{ V}$.

Solution: The transconductance is

$$g_m = 2K_n(V_{GS} - V_{TN}) = 2(0.25)(3-1) = 1\text{ mA/V}$$

From Equation (7.90), the unity-gain bandwidth, or frequency, is

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})} = \frac{10^{-3}}{2\pi(0.2 + 0.04) \times 10^{-12}} = 6.63 \times 10^8\text{ Hz}$$

or

$$f_T = 663\text{ MHz}$$

Comment: As with bipolar transistors, high-frequency FETs require small capacitances and a small device size.

Typically, values of C_{gs} for MOSFETs are in the range of 0.1 to 0.5 pF and values of C_{gd} are typically from 0.01 to 0.04 pF.

As previously stated, the equivalent circuit is the same for MOSFETs, JFETS, and MESFETs. For JFETs, and MESFETS, capacitances C_{gs} and C_{gd} are depletion capacitances rather than oxide capacitances. Typically, for JFETs, C_{gs} and C_{gd} are larger than for MOSFETs, while the values for MESFETs are smaller. Also, for MESFETs fabricated in gallium arsenide, the unity-gain bandwidths may be in the range of tens of GHz. For this reason, gallium arsenide MESFETs are often used in microwave amplifiers.

Test Your Understanding

7.21 For an n-channel MOSFET, the parameters are: $K_n = 0.2\text{ mA/V}^2$, $V_{TN} = 1\text{ V}$, $\lambda = 0$, $C_{gd} = 0.02\text{ pF}$, $C_{gs} = 0.25\text{ pF}$. The device is biased at $I_{DQ} = 0.4\text{ mA}$. Determine the unity-gain frequency. (Ans. $f_T = 332\text{ MHz}$)

7.22 A MOSFET has a unity-gain bandwidth of $f_T = 500\text{ MHz}$. Assume overlap capacitances of $C_{gsp} = C_{gdp} = 0.01\text{ pF}$. If the transistor is biased such that $g_m = 0.5$ mA/V, determine C_{gs}. (Assume C_{gd} is equal to the overlap capacitance.) (Ans. $C_{gs} = 0.139\text{ pF}$)

7.23 For a MOSFET, assume that $g_m = 1\text{ mA/V}$. The basic gate capacitances are $C_{gs} = 0.4\text{ pF}$, $C_{gd} = 0$, and the overlap capacitances are $C_{gsp} = C_{gdp}$. Determine the maximum overlap capacitance for a unity-gain bandwidth of 350 MHz. (Ans. $C_{gsp} = C_{gdp} = 0.0274\text{ pF}$)

7.5.3 Miller Effect and Miller Capacitance

As for the bipolar transistor, the Miller effect and Miller capacitance are factors in the high-frequency characteristics of FET circuits. Figure 7.44 is a simplified high-frequency transistor model, with a load resistor R_L connected to the output. We will determine the current gain in order to demonstrate the impact of the Miller effect.

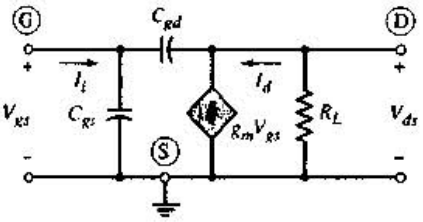


Figure 7.44 Equivalent high-frequency small-signal circuit of a MOSFET with a load resistance R_L

Writing a Kirchhoff current law (KCL) equation at the input gate node, we have

$$I_i = j\omega C_{gs} V_{gs} + j\omega C_{gd}(V_{gs} - V_{ds}) \tag{7.91}$$

where I_i is the input current. Likewise, summing currents at the output drain node, we have

$$\frac{V_{ds}}{R_L} + g_m V_{gs} + j\omega C_{gd}(V_{ds} - V_{gs}) = 0 \tag{7.92}$$

We can combine Equations (7.91) and (7.92) to eliminate voltage V_{ds}. The input current is then

$$I_i = j\omega \left\{ C_{gs} + C_{gd}\left[\frac{1 + g_m R_L}{1 + j\omega R_L C_{gd}}\right]\right\} V_{gs} \tag{7.93}$$

Normally, $(\omega R_L C_{gd})$ is much less than 1; therefore, we can neglect $(j\omega R_L C_{gd})$ and Equation (7.93) becomes

$$I_i = j\omega[C_{gs} + C_{gd}(1 + g_m R_L)]V_{gs} \tag{7.94}$$

Figure 7.45 shows the equivalent circuit described by Equation (7.94). The parameter C_M is the Miller capacitance and is given by

$$C_M = C_{gd}(1 + g_m R_L) \tag{7.95}$$

Equation (7.95) clearly shows the effect of the parasitic drain overlap capacitance. When the transistor is biased in the saturation region, as in an amplifier circuit, the major contribution to the total gate-to-drain capacitance C_{gd} is the overlap capacitance. This overlap capacitance is multiplied because of the Miller effect and may become a significant factor in the bandwidth of an amplifier. Minimizing the overlap capacitance is one of the challenges of fabrication technology.

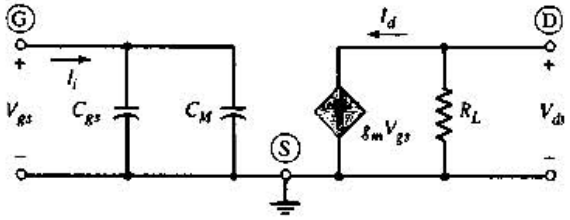


Figure 7.45 MOSFET high-frequency circuit, including the equivalent Miller capacitance

The cutoff frequency f_T of a MOSFET is defined as the frequency at which the current gain magnitude is 1, or the magnitude of the input current I_i is equal to the ideal load current I_d. From Figure 7.45, we see that

$$I_i = j\omega(C_{gs} + C_M)V_{gs} \tag{7.96}$$

and the ideal load current is

$$I_d = g_m V_{gs} \tag{7.97}$$

The magnitude of the current gain is therefore

$$|A_i| = \left|\frac{I_d}{I_i}\right| = \frac{g_m}{2\pi f(C_{gs} + C_M)} \tag{7.98}$$

Setting Equation (7.98) equal to 1, we find the cutoff frequency

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_M)} \cong \frac{g_m}{2\pi C_G} \tag{7.99}$$

where C_G is the equivalent input gate capacitance.

Example 7.13 **Objective:** Determine the Miller capacitance and cutoff frequency of an FET circuit.

The n-channel MOSFET described in Example 7.12 is biased at the same current, and a 10 kΩ load is connected to the output.

Solution: From Example 7.12, the transconductance is $g_m = 1$ mA/V. The Miller capacitance is therefore

$$C_M = C_{gd}(1 + g_m R_L) = (0.04)[1 + (1)(10)] = 0.44 \text{ pF}$$

From Equation (7.99), the cutoff frequency is

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_M)} = \frac{10^{-3}}{2\pi(0.2 + 0.44) \times 10^{-12}} = 2.49 \times 10^8 \text{ Hz}$$

or

$$f_T = 249 \text{ MHz}$$

Comment: The Miller effect and equivalent Miller capacitance reduce the cutoff frequency of an FET circuit, just as they do in a bipolar circuit.

Test Your Understanding

***7.24** For the circuit in Figure 7.46, the transistor parameters are: $K_n = 0.5\,\text{mA/V}^2$, $V_{TN} = 2\,\text{V}$, $\lambda = 0$, $C_{gd} = 0.1\,\text{pF}$, and $C_{gs} = 1\,\text{pF}$. Calculate: (a) the Miller capacitance, and (b) the 3 dB frequency of the small-signal voltage gain. (Ans. (a) $C_M = 0.617\,\text{pF}$, (b) $f_H = 10.9\,\text{MHz}$)

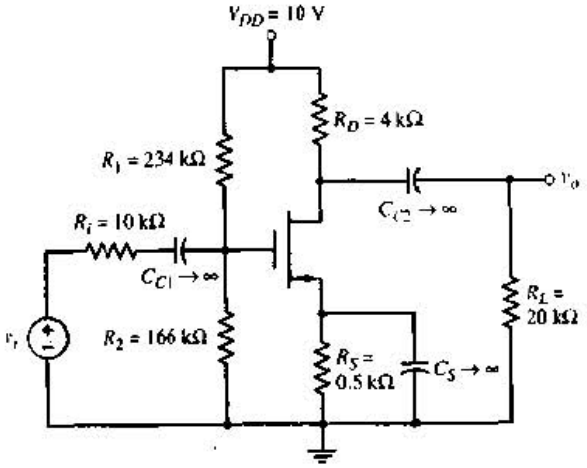


Figure 7.46 Figure for Exercise 7.24

7.6 HIGH-FREQUENCY RESPONSE OF TRANSISTOR CIRCUITS

In the last sections, we developed the high-frequency equivalent circuits for the bipolar and field-effect transistors. We also discussed the Miller effect, which occurs when transistors are operating in a circuit configuration. In this section, we will expand our analysis of the high-frequency characteristics of transistor circuits.

Initially, we will look at the high-frequency response of the common-emitter and common-source configurations. We will then examine common-base and common-gate circuits, and a cascode circuit that is a combination of the common-emitter and common-base circuits. Finally, we will analyze the high-frequency characteristics of emitter-follower and source-follower circuits. In the following examples, we will use the same basic bipolar transistor circuit so that a good comparison can be made between the three circuit configurations.

7.6.1 Common-Emitter and Common-Source Circuits

The transistor capacitances and the load capacitance in the common-emitter amplifier shown in Figure 7.47 affect the high-frequency response of the circuit. Initially, we will use a hand analysis to determine the effects of the transistor on the high-frequency response. In this analysis, we will assume that C_C and C_E

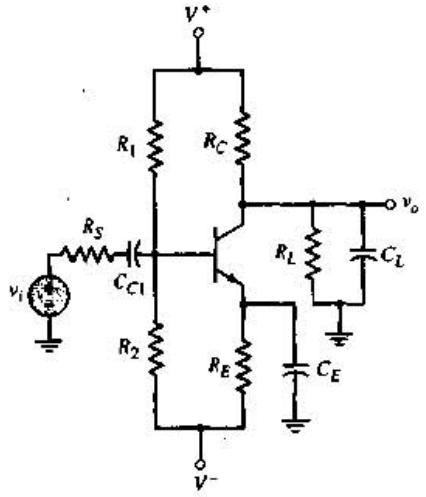


Figure 7.47 Common-emitter amplifier

are short circuits, and C_L is an open circuit. A computer analysis will then be used to determine the effect of both the transistor and load capacitances.

The high-frequency small-signal equivalent circuit of the common-emitter circuit is shown in Figure 7.48(a) in which C_L is assumed to be an open circuit. We replace the capacitor C_μ with the equivalent Miller capacitance C_M as shown in Figure 7.48(b). From our previous analysis of the Miller capacitance, we can write

$$C_M = C_\mu(1 + g_m R_L') \tag{7.100}$$

where the output resistance R_L' is $r_o \| R_C \| R_L$.

The upper 3 dB frequency can be determined by using the time constant technique. We can write

$$f_H = \frac{1}{2\pi\tau_p} \tag{7.101}$$

where $\tau_p = R_{eq}C_{eq}$. In this case, the equivalent capacitance is $C_{eq} = C_\pi + C_M$, and the equivalent resistance is the effective resistance seen by the capacitance, $R_{eq} = r_\pi \| R_B \| R_S$. The upper corner frequency is therefore

$$f_H = \frac{1}{2\pi[r_\pi \| R_B \| R_S](C_\pi + C_M)} \tag{7.102}$$

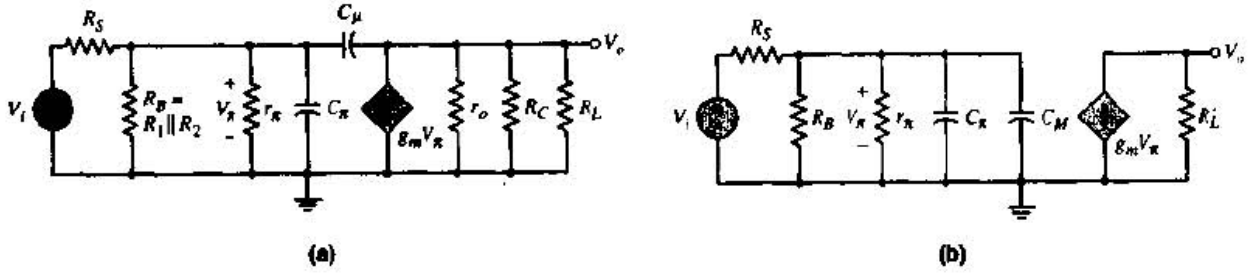


Figure 7.48 (a) High-frequency equivalent circuit of common-emitter amplifier; (b) high-frequency equivalent circuit of common-emitter amplifier, including the Miller capacitance

We determine the midband voltage gain magnitude by assuming C_π and C_M are open circuits. We find that

$$|A_v|_M = \left|\frac{V_o}{V_i}\right|_M = g_m R_L' \left[\frac{R_B \| r_\pi}{R_B \| r_\pi + R_S}\right] \tag{7.103}$$

The Bode plot of the high-frequency voltage gain magnitude is shown in Figure 7.49.

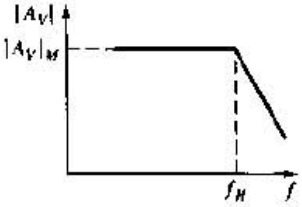


Figure 7.49 Bode plot of the high-frequency voltage gain magnitude for the common-emitter amplifier

Example 7.14 **Objective:** Determine the upper corner frequency and midband gain of a common-emitter circuit.

For the circuit in Figure 7.47, the parameters are: $V^+ = 5\,\text{V}$, $V^- = -5\,\text{V}$, $R_S = 0.1\,\text{k}\Omega$, $R_1 = 40\,\text{k}\Omega$, $R_2 = 5.72\,\text{k}\Omega$, $R_E = 0.5\,\text{k}\Omega$, $R_C = 5\,\text{k}\Omega$, and $R_L = 10\,\text{k}\Omega$. The transistor parameters are: $\beta = 150$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, $V_A = \infty$, $C_\pi = 35\,\text{pF}$, and $C_\mu = 4\,\text{pF}$.

Solution: From a dc analysis, we find that $I_{CQ} = 1.02\,\text{mA}$. The small-signal parameters are therefore

$$r_\pi = \frac{\beta V_T}{I_{CQ}} = \frac{(150)(0.026)}{1.02} = 3.82\,\text{k}\Omega$$

and

$$g_m = \frac{I_{CQ}}{V_T} = \frac{1.02}{0.026} = 39.2\,\text{mA/V}$$

The Miller capacitance is then

$$C_M = C_\mu(1 + g_m R_L') = C_\mu[1 + g_m(R_C \| R_L)]$$

or

$$C_M = (4)[1 + (39.2)(5 \| 10)] = 527\,\text{pF}$$

and the upper 3 dB frequency is therefore

$$f_H = \frac{1}{2\pi[r_\pi \| R_B \| R_S](C_\pi + C_M)}$$

$$= \frac{1}{2\pi[3.82 \| 40 \| 5.72 \| 0.1](10^3)(35 + 527)(10^{-12})}$$

or

$$f_H = 2.96\,\text{MHz}$$

Finally, the midband gain is

$$|A_v|_M = g_m R_L' \left[\frac{R_B \| r_\pi}{R_B \| r_\pi + R_S}\right]$$

$$= (39.2)(5 \| 10)\left[\frac{40 \| 5.72 \| 3.82}{40 \| 5.72 \| 3.82 + 0.1}\right]$$

or

$$|A_v|_M = 125$$

Comments: This example demonstrates the importance of the Miller effect. The feedback capacitance C_μ is multiplied by a factor of 132 (from 4 pF to 527 pF), and the resulting Miller capacitance C_M is approximately 15 times larger than C_π. The actual

corner frequency is therefore approximately 15 times smaller than it would be if C_μ were neglected.

PSpice Verification: Figure 7.50 shows the results of a PSpice analysis of this common-emitter circuit. The computer values are: $C_\pi = 35.5\,\text{pF}$ and $C_\mu = 3.89\,\text{pF}$. The curve marked "C_π only" is the circuit frequency response if C_μ is neglected; the curve marked "C_π and C_μ only" is the response due to C_π, C_μ, and the Miller effect. These curves illustrate that the bandwidth of this circuit is drastically reduced by the Miller effect.

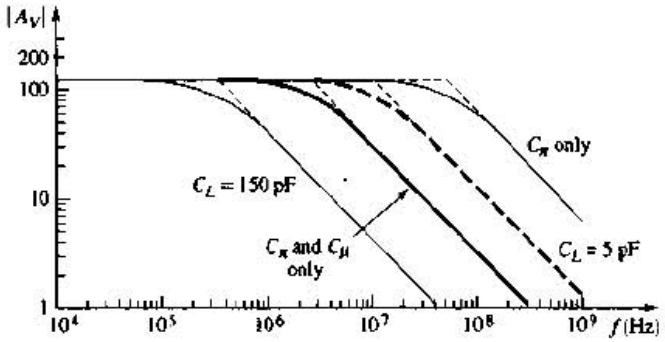


Figure 7.50 PSpice analysis results for common-emitter amplifier

The corner frequency is approximately 2.5 MHz and the midband gain is 125, which agree very well with the hand analysis results.

The curves marked "$C_L = 5\,\text{pF}$" and "$C_L = 150\,\text{pF}$" show the circuit response if the transistor is ideal, with zero C_π and C_μ capacitances and a load capacitance connected to the output. These results show that, for $C_L = 5\,\text{pF}$, the circuit response is dominated by the C_π and C_μ capacitances of the transistor. However, if a large load capacitance, such as $C_L = 150\,\text{pF}$, is connected to the output, the circuit response is dominated by the C_L capacitance.

The high-frequency response of the common-source circuit is similar to that of the common-emitter circuit, and the discussion and conclusions are the same. Capacitance C_π is replaced by C_{gs}, and C_μ is replaced by C_{gd}. The high-frequency small-signal equivalent circuit of the FET is then essentially identical to that of the bipolar transistor.

7.6.2 Common-Base, Common-Gate, and Cascode Circuits

As we have just seen, the bandwidth of the common-emitter and common-source circuits is reduced by the Miller effect. To increase the bandwidth, the Miller effect, or the C_μ multiplication factor, must be minimized or eliminated. The common-base and common-gate amplifier configurations achieve this result. We will analyze a common-base circuit; the analysis is the same for the common-gate circuit.

Common-Base Circuit

Figure 7.51 shows a common-base circuit. The circuit configuration is the same as the common-emitter circuit considered previously, except a bypass capacitor is added to the base and the input is capacitively coupled to the emitter.

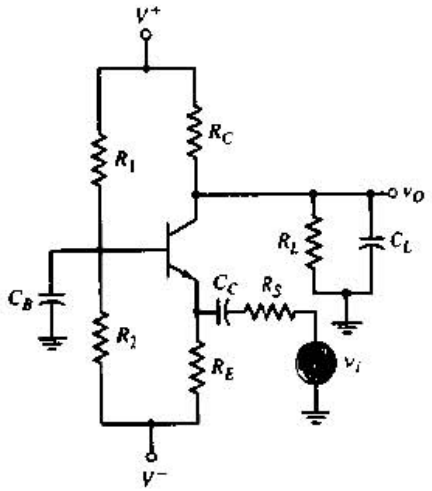


Figure 7.51 Common-base amplifier

Figure 7.52(a) shows the high-frequency equivalent circuit, with the coupling and bypass capacitors replaced by short circuits. Resistors R_1 and R_2 are then effectively short circuited. Also, resistance r_o is assumed to be infinite. Capacitance C_μ, which led to the multiplication effect, is no longer between the input and output terminals. One side of capacitor C_μ is tied to signal ground.

Writing a KCL equation at the emitter, we find that

$$I_e + g_m V_\pi + \frac{V_\pi}{(1/sC_\pi)} + \frac{V_\pi}{r_\pi} = 0 \tag{7.104}$$

Since $V_\pi = -V_e$, Equation (7.104) becomes

$$\frac{I_e}{V_e} = \frac{1}{Z_i} = \frac{1}{r_\pi} + g_m + sC_\pi \tag{7.105}$$

where Z_i is the impedance looking into the emitter. Rearranging terms, we have

$$\frac{1}{Z_i} = \frac{1 + r_\pi g_m}{r_\pi} + sC_\pi = \frac{1+\beta}{r_\pi} + sC_\pi \tag{7.106}$$

The equivalent input portion of the circuit is shown in Figure 7.52(b).

Figure 7.52(c) shows the equivalent output portion of the circuit. Again, one side of C_μ is tied to ground, which eliminates the feedback or Miller multiplication effect. We then expect the upper 3 dB frequency to be larger than that observed in the common-emitter configuration.

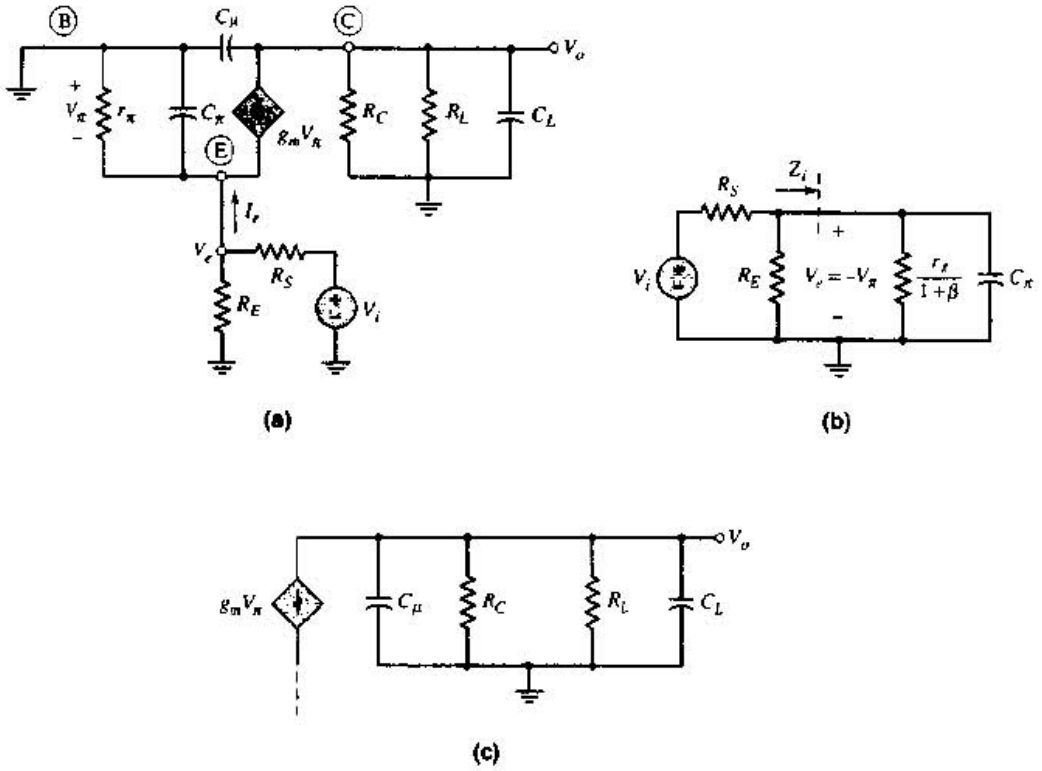


Figure 7.52 (a) High-frequency common-base equivalent circuit, (b) equivalent input circuit, and (c) equivalent output circuit

For the input portion of the circuit, the upper 3 dB frequency is given by

$$f_{H\pi} = \frac{1}{2\pi\tau_{P\pi}} \tag{7.107(a)}$$

where the time constant is

$$\tau_{P\pi} = \left[\left(\frac{r_\pi}{1+\beta}\right) \| R_E \| R_S\right] \cdot C_\pi \tag{7.107(b)}$$

In the hand analysis, we assume that C_L is an open circuit. Capacitance C_μ will also produce an upper 3 dB frequency, given by

$$f_{H\mu} = \frac{1}{2\pi\tau_{P\mu}} \tag{7.108(a)}$$

where the time constant is

$$\tau_{P\mu} = [R_C \| R_L] \cdot C_\mu \tag{7.108(b)}$$

If C_μ is much smaller than C_π, we would expect the 3 dB frequency $f_{H\pi}$ due to C_π to dominate the high-frequency response. However, the factor $r_\pi/(1+\beta)$ in the time constant $\tau_{P\pi}$ is small; therefore, the two time constants may be the same order of magnitude.

Example 7.15 **Objective:** Determine the upper corner frequencies and midband gain of a common-base circuit.

Consider the circuit shown in Figure 7.51 with circuit parameters $V^+ = 5\,\text{V}$, $V^- = -5\,\text{V}$, $R_S = 0.1\,\text{k}\Omega$, $R_1 = 40\,\text{k}\Omega$, $R_2 = 5.72\,\text{k}\Omega$, $R_E = 0.5\,\text{k}\Omega$, $R_C = 5\,\text{k}\Omega$, and $R_L = 10\,\text{k}\Omega$. (These are the same values as those used for the common-emitter circuit in Example 7.14.) The transistor parameters are: $\beta = 150$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, $V_A = \infty$, $C_\pi = 35\,\text{pF}$, and $C_\mu = 4\,\text{pF}$.

Solution: The dc analysis is the same as in Example 7.14; therefore, $I_{CQ} = 1.02\,\text{mA}$, $g_m = 39.2\,\text{mA/V}$, and $r_\pi = 3.82\,\text{k}\Omega$. The time constant associated with C_π is

$$\tau_{P\pi} = \left[\left(\frac{r_\pi}{1+\beta}\right) \| R_E \| R_S\right] \cdot C_\pi$$

$$= \left[\left(\frac{3.82}{151}\right) \| (0.5) \| (0.1)\right] \times 10^3 (35 \times 10^{-12})$$

or

$$\tau_{P\pi} = 0.679\,\text{ns}$$

The upper 3 dB frequency corresponding to C_π is therefore

$$f_{H\pi} = \frac{1}{2\pi\tau_{P\pi}} = \frac{1}{2\pi(0.679 \times 10^{-9})} \Rightarrow 234\,\text{MHz}$$

The time constant associated with C_μ in the output portion of the circuit is

$$\tau_{P\mu} = [R_C \| R_L] \cdot C_\mu = [5 \| 10] \times 10^3 (4 \times 10^{-12}) \Rightarrow 13.3\,\text{ns}$$

The upper 3 dB frequency corresponding to C_μ is therefore

$$f_{H\mu} = \frac{1}{2\pi\tau_{P\mu}} = \frac{1}{2\pi(13.3 \times 10^{-9})} \Rightarrow 12.0\,\text{MHz}$$

So in this case, $f_{H\mu}$ is the dominant pole frequency.

The magnitude of the midband voltage gain is

$$|A_v|_M = g_m(R_C \| R_L)\left[\frac{R_E \left\| \left(\frac{r_\pi}{1+\beta}\right)\right.}{R_E \left\| \left(\frac{r_\pi}{1+\beta}\right)\right. + R_S}\right]$$

$$= (39.2)(5 \| 10)\left[\frac{0.5 \left\| \left(\frac{3.82}{151}\right)\right.}{0.5 \left\| \left(\frac{3.82}{151}\right)\right. + 0.1}\right] = 25.3$$

Comment: The results of this example show that the bandwidth of the common-base circuit is limited by the capacitance C_μ in the output portion of the circuit. The bandwidth of this particular circuit is 12 MHz, which is approximately a factor of four greater than the bandwidth of the common-emitter circuit in Example 7.14.

Computer Verification: Figure 7.53 shows the results of a PSpice analysis of the common-base circuit. The computer values are $C_\pi = 35.5\,\text{pF}$ and $C_\mu = 3.89\,\text{pF}$, which are the same as those in Example 7.14. The curve marked "C_π only" is the circuit frequency response if C_μ is neglected. The curve marked "C_π and C_μ only" includes the effect of both C_π and C_μ. As the hand analysis predicted, C_μ dominates the circuit high-frequency response.

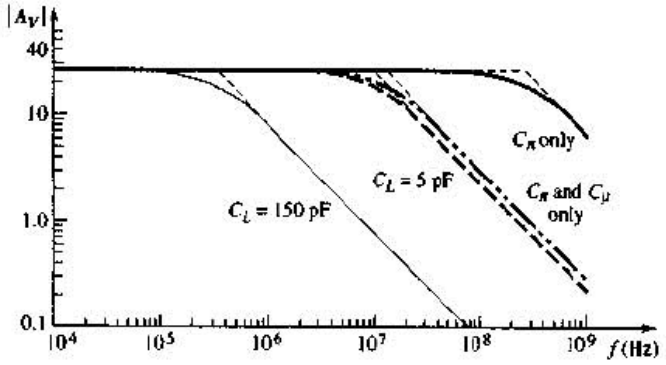


Figure 7.53 PSpice analysis results for common-base circuit

The corner frequency is approximately 13.5 MHz and the midband gain is 25.5, both of which agree very well with the hand analysis results.

The curves marked "$C_L = 5\,\text{pF}$" and "$C_L = 150\,\text{pF}$" are the circuit response if the transistor is ideal and only a load capacitance is included. These results again show that if a load capacitance of $C_L = 150\,\text{pF}$ were connected to the output, the circuit response would be dominated by this capacitance. However, if a 5 pF load capacitor were connected to the output, the circuit response would be a function of both the C_L and C_μ capacitances, since the two response characteristics are almost identical.

Cascode Circuit

The cascode circuit, as shown in Figure 7.54, combines the advantages of the common-emitter and common-base circuits. The input signal is applied to the common-emitter circuit (Q_1), and the output signal from the common emitter

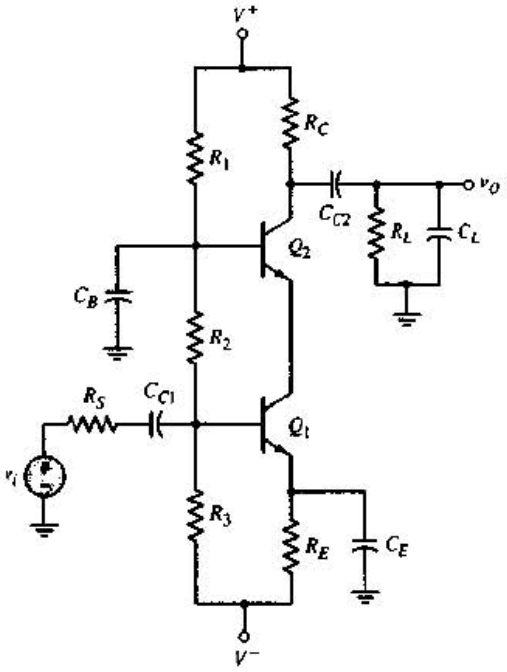


Figure 7.54 Cascode circuit

is fed into the common-base circuit (Q_2). The input impedance to the common-emitter circuit (Q_1) is relatively large, and the load resistance seen by Q_1 is the input impedance to the emitter of Q_2 and is fairly small. The low output resistance seen by Q_1 reduces the Miller multiplication factor on $C_{\mu 1}$ and therefore extends the bandwidth of the circuit.

Figure 7.55(a) shows the high-frequency small-signal equivalent circuit. The coupling and bypass capacitors are equivalent to short circuits, and resistance r_o for Q_2 is assumed to be infinite.

The input impedance to the emitter of Q_2 is Z_{ie2}. From Equation (7.106) in our previous analysis, we have

$$Z_{ie2} = \left(\frac{r_{\pi 2}}{1+\beta}\right) \left\| \left(\frac{1}{sC_{\pi 2}}\right)\right. \tag{7.109}$$

The input portion of the small-signal equivalent circuit can be transformed to that shown in Figure 7.55(b). The input impedance Z_{ie2} is again shown.

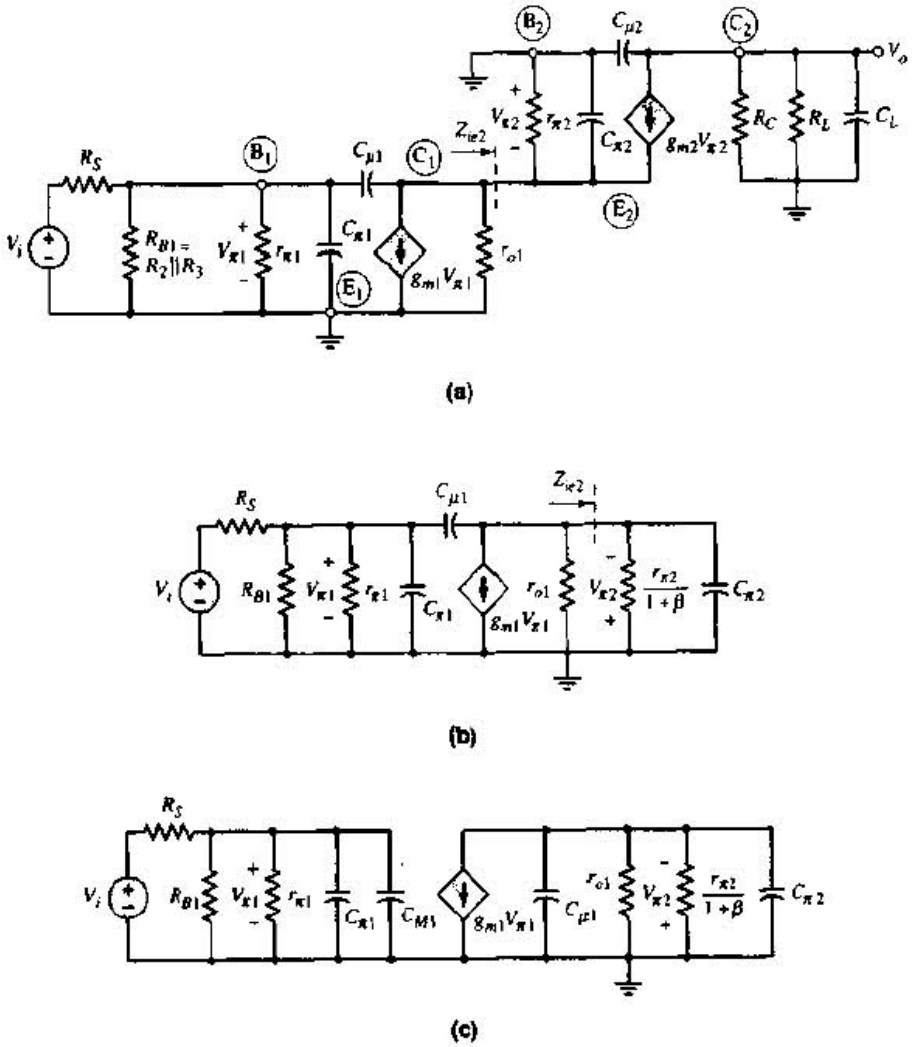


Figure 7.55 (a) High-frequency equivalent circuit of cascode configuration, (b) rearranged high-frequency equivalent circuit, and (c) variation of the high-frequency circuit, including the Miller capacitance

The input portion of the circuit shown in Figure 7.55(b) can be transformed to that given in Figure 7.55(c), which shows the Miller capacitance. The Miller capacitance C_{M1} is included in the input, and capacitance $C_{\mu 1}$ is included in the output portion of the Q_1 model. The possibility of including C_μ in the output circuit was discussed previously.

In the center of this equivalent circuit, r_{o1} is in parallel with $r_{\pi 2}/(1+\beta)$. Since r_{o1} is usually large, it can be approximated as an open circuit. The Miller capacitance is then

$$C_{M1} = C_{\mu 1}\left[1 + g_{m1}\left(\frac{r_{\pi 2}}{1+\beta}\right)\right] \tag{7.110}$$

Transistors Q_1 and Q_2 are biased with essentially the same current; therefore,

$$r_{\pi 1} \cong r_{\pi 2} \quad \text{and} \quad g_{m1} \cong g_{m2}$$

Then

$$g_{m1} r_{\pi 2} = \beta$$

which yields

$$C_{M1} \cong 2\,C_{\mu 1} \tag{7.111}$$

Equation (7.111) shows that this cascode circuit greatly reduces the Miller multiplication factor.

The time constant related to $C_{\pi 2}$ involves resistance $r_{\pi 2}/(1+\beta)$. Since this resistance is small, the time constant is small, and the corner frequency related to $C_{\pi 2}$ is very large. We can therefore neglect the effects of $C_{\mu 1}$ and $C_{\pi 2}$ in the center portion of the circuit.

The time constant for the input portion of the circuit is

$$\tau_{P\pi} = [R_S \| R_{B1} \| r_{\pi 1}](C_{\pi 1} + C_{M1}) \tag{7.112(a)}$$

where $C_{M1} = 2C_{\mu 1}$. The corresponding 3 dB frequency is

$$f_{H\pi} = \frac{1}{2\pi\tau_{P\pi}} \tag{7.112(b)}$$

Assuming C_L acts as an open circuit, the time constant of the output portion of the circuit, from Figure 7.55, is

$$\tau_{P\mu} = [R_C \| R_L](C_{\mu 2}) \tag{7.113(a)}$$

and the corresponding corner frequency is

$$f_{H\mu} = \frac{1}{2\pi\tau_{P\mu}} \tag{7.113(b)}$$

To determine the midband voltage gain we assume that all capacitances in the circuit in Figure 7.55(c) are open circuits. The output voltage is then

$$V_o = -g_{m2} V_{\pi 2}(R_C \| R_L) \tag{7.114}$$

and

$$V_{\pi 2} = g_{m1} V_{\pi 1}\left[r_{o1} \left\| \left(\frac{r_{\pi 2}}{1+\beta}\right)\right.\right] \tag{7.115}$$

We can neglect the effect of r_{o1} compared to $r_{\pi 2}/(1+\beta)$. Also, since $g_{m1} r_{\pi 2} = \beta$, Equation (7.115) becomes

$$V_{\pi 2} \cong V_{\pi 1} \tag{7.116}$$

and, from the input portion of the circuit,

$$V_{\pi 1} = \frac{R_{B1} \| r_{\pi 1}}{R_{B1} \| r_{\pi 1} + R_S} \times V_i \tag{7.117}$$

Finally, combining equations, we find the midband voltage gain is

$$A_{vM} = \frac{V_o}{V_i} = -g_{m2}(R_C \| R_L)\left[\frac{R_{B1} \| r_{\pi 1}}{R_{B1} \| r_{\pi 1} + R_S}\right] \tag{7.118}$$

If we compare Equation (7.118) to Equation (7.103) for the common-emitter circuit, we see that the expression for the midband gain of the cascode circuit is identical to that of the common-emitter circuit. The cascode circuit achieves a relatively large voltage gain, while extending the bandwidth.

Example 7.16 **Objective:** Determine the 3 dB frequencies and midband gain of a cascode circuit.

For the circuit in Figure 7.54, the parameters are: $V^+ = 10\,\text{V}$, $V^- = -10\,\text{V}$, $R_S = 0.1\,\text{k}\Omega$, $R_1 = 42.5\,\text{k}\Omega$, $R_2 = 20.5\,\text{k}\Omega$, $R_3 = 28.3\,\text{k}\Omega$, $R_E = 5.4\,\text{k}\Omega$, $R_C = 5\,\text{k}\Omega$, $R_L = 10\,\text{k}\Omega$, and $C_L = 0$. The transistor parameters are: $\beta = 150$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, $V_A = \infty$, $C_\pi = 35\,\text{pF}$, and $C_\mu = 4\,\text{pF}$.

Solution: Since β is large for each transistor, the quiescent collector current is essentially the same in each transistor and is $I_{CQ} = 1.02\,\text{mA}$. The small-signal parameters are: $r_{\pi 1} = r_{\pi 2} \equiv r_\pi = 3.82\,\text{k}\Omega$ and $g_{m1} = g_{m2} \equiv g_m = 39.2\,\text{mA/V}$.

From Equation (7.112(a)), the time consant related to the input portion of the circuit is

$$\tau_{P\pi} = [R_S \| R_{B1} \| r_{\pi 1}](C_{\pi 1} + C_{M1})$$

Since $R_{B1} = R_2 \| R_3$ and $C_{M1} = 2C_{\mu 1}$, then

$$\tau_{P\pi} = [(0.1) \| 20.5 \| 28.3 \| 3.82] \times 10^3 [35 + 2(4)] \times 10^{-12} \Rightarrow 4.16\,\text{ns}$$

The corresponding 3 dB frequency is

$$f_{H\pi} = \frac{1}{2\pi\tau_{P\pi}} = \frac{1}{2\pi(4.16 \times 10^{-9})} \Rightarrow 38.3\,\text{MHz}$$

From Equation (7.113(a)), the time constant of the output portion of the circuit is

$$\tau_{P\mu} = [R_C \| R_L]C_{\mu 2} = [5 \| 10] \times 10^3 (4 \times 10^{-12}) \Rightarrow 13.3\,\text{ns}$$

and the corresponding 3 dB frequency is

$$f_{H\mu} = \frac{1}{2\pi\tau_{P\mu}} = \frac{1}{2\pi(13.3 \times 10^{-9})} \Rightarrow 12\,\text{MHz}$$

From Equation (7.118), the midband voltage gain is

$$|A_v|_M = g_{m2}(R_C \| R_L)\left[\frac{R_{B1} \| r_{\pi 1}}{R_{B1} \| r_{\pi 1} + R_S}\right]$$
$$= (39.2)(5 \| 10)\left[\frac{(20.5 \| 28.3 \| 3.82)}{(20.5 \| 28.3 \| 3.82) + (0.1)}\right] = 126$$

Comment: As was the case for the common-base circuit, the 3 dB frequency for the cascode circuit is determined by capacitance C_μ in the output stage. The bandwidth of the cascode circuit is 12 Mz, compared to approximately 3 MHz for the common-emitter circuit. The midband voltage gains for the two circuits are essentially the same.

Computer Verification: Figure 7.56 shows the results of a PSpice analysis of the cascode circuit. From the hand analysis, the two corner frequencies are 12 Mz and 38.3 MHz. Since these frequencies are fairly close, we expect the actual response to show the effects of both capacitances. This hypothesis is verified and demonstrated in the computer analysis results. The curves marked "C_π only" and "C_π and C_μ only" are fairly close together, and their slopes are steeper than −6 dB/octave, which shows that more than one capacitor is involved in the response. At a frequency of 12 MHz, the response curve is 3 dB below the maximum asymptotic gain, and the midband gain is 120. These values closely agree with the hand analysis results.

The curves marked "$C_L = 5$ pF" and "$C_L = 150$ pF" show the circuit response if the transistor is ideal and only a load capacitance is included.

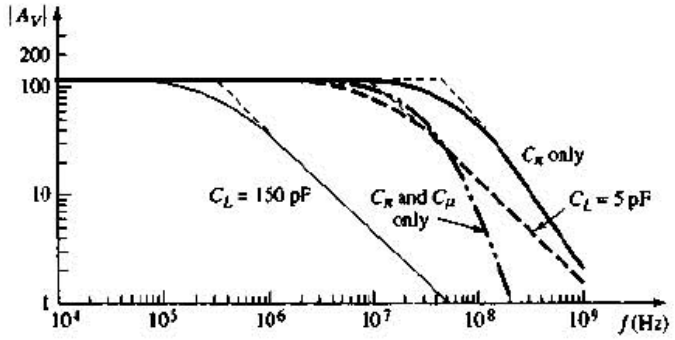


Figure 7.56 PSpice analysis results for cascode circuit

7.6.3 Emitter- and Source-Follower Circuits

In this section, we analyze the high-frequency response of the emitter follower. We will analyze the same basic circuit configuration that we have considered previously. The results and discussions also apply to the source follower.

Figure 7.57 shows an emitter-follower circuit with the output signal at the emitter capacitively coupled to a load. Figure 7.58(a) shows the high-frequency

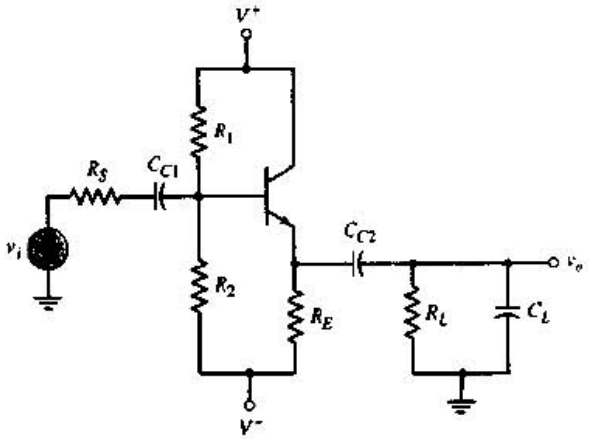


Figure 7.57 Emitter-follower circuit

small-signal equivalent circuit, with the coupling capacitors acting effectively as short circuits.

We will rearrange the circuit so that we can gain a better insight into the circuit behavior. We see that C_μ is tied to ground potential and also that r_o is in parallel with R_E and R_L. We may define

$$R_L' = R_E \| R_L \| r_o$$

In this analysis we neglect the effect of C_L. Figure 7.58(b) shows a rearrangement of the circuit.

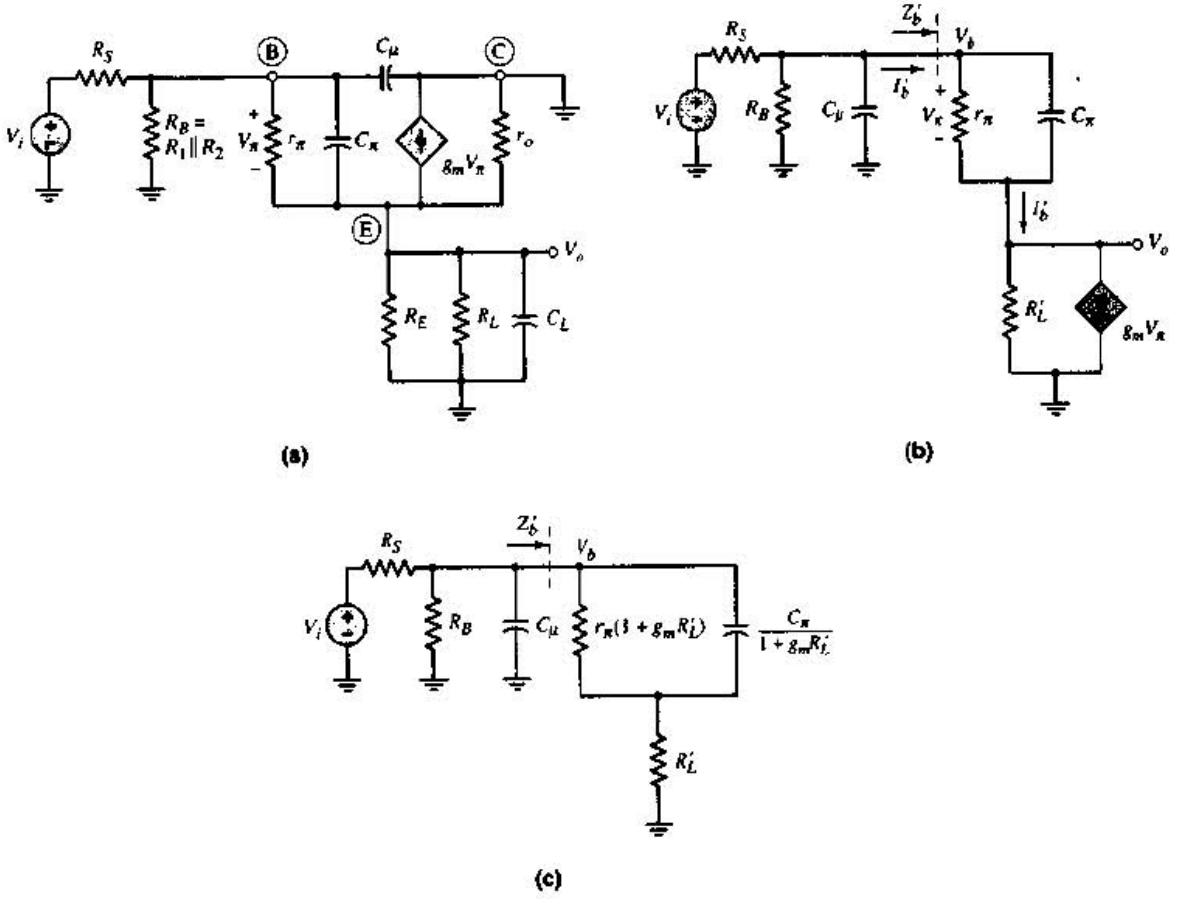


Figure 7.58 (a) High-frequency equivalent circuit of emitter follower, (b) rearranged high-frequency equivalent circuit, and (c) high-frequency equivalent circuit with effective input base impedance

We can find the impedance Z_b' looking into the base without capacitance C_μ. The current I_b' entering the parallel combination of r_π and C_π is the same as that coming out of the combination. The output voltage is then

$$V_o = (I_b' + g_m V_\pi) R_L' \tag{7.119}$$

Voltage V_π is given by

$$V_\pi = \frac{I_b'}{y_\pi} \tag{7.120}$$

where

$$y_\pi = (1/r_\pi) + sC_\pi$$

Voltage V_b is

$$V_b = V_\pi + V_o$$

Therefore,

$$Z_b' = \frac{V_b}{I_b'} = \frac{V_\pi + V_o}{I_b'} \tag{7.121}$$

Combining Equations (7.119), (7.120), and (7.121), we obtain

$$Z_b' = \frac{1}{y_\pi} + R_L' + \frac{g_m R_L'}{y_\pi} \tag{7.122(a)}$$

or

$$Z_b' = \frac{1}{y_\pi}(1 + g_m R_L') + R_L' \tag{7.122(b)}$$

Substituting the expression for y_π, we find

$$Z_b' = \frac{1}{\dfrac{1}{r_\pi} + sC_\pi} \times (1 + g_m R_L') + R_L' \tag{7.123(a)}$$

This can then be written as

$$Z_b' = \frac{1}{\dfrac{1}{r_\pi(1 + g_m R_L')} + \dfrac{sC_\pi}{(1 + g_m R_L')}} + R_L' \tag{7.123(b)}$$

Impedance Z_b' is shown in the equivalent circuit in Figure 7.58(c). Equation (7.123(b)) shows that the effect of capacitance C_π is reduced in the emitter-follower configuration.

Since the emitter-follower circuit has a zero and two poles, a detailed analysis of the circuit is very tedious. From Equations (7.119) and (7.120), we have

$$V_o = V_\pi(y_\pi + g_m)R_L' \tag{7.124}$$

which yields a zero when $y_\pi + g_m = 0$. Using the definition of y_π, the zero occurs at

$$f_o = \frac{1}{2\pi C_\pi\left(\dfrac{r_\pi}{1 + \beta}\right)} \tag{7.125}$$

Since $r_\pi/(1 + \beta)$ is small, frequency f_o is usually very high.

If we make a simplifying assumption, we can determine an approximate value of one pole. In many applications, the impedance of $r_\pi(1 + g_m R_L')$ in

parallel with $C_\pi/(1+g_m R_L')$ is large compared to R_L'. If we neglect R_L', then the time constant is

$$\tau_P = [R_S \| R_B \| (1+g_m R_L')r_\pi]\left(C_\mu + \frac{C_\pi}{1+g_m R_L'}\right) \tag{7.126(a)}$$

and the 3 dB frequency (or pole) is

$$f_H = \frac{1}{2\pi\tau_P} \tag{7.126(b)}$$

Example 7.17 **Objective:** Determine the frequency of a zero and a pole in the high-frequency response of an emitter follower.

Consider the emitter-follower circuit in Figure 7.57 with parameters $V^+ = 5\,\text{V}$, $V^- = -5\,\text{V}$, $R_S = 0.1\,\text{k}\Omega$, $R_1 = 40\,\text{k}\Omega$, $R_2 = 5.72\,\text{k}\Omega$, $R_E = 0.5\,\text{k}\Omega$, and $R_L = 10\,\text{k}\Omega$. The transistor parameters are: $\beta = 150$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, $V_A = \infty$, $C_\pi = 35\,\text{pF}$, and $C_\mu = 4\,\text{pF}$.

Solution: As in previous examples, the dc analysis yields $I_{CQ} = 1.02\,\text{mA}$. Therefore, $g_m = 39.2\,\text{mA/V}$ and $r_\pi = 3.82\,\text{k}\Omega$.

From Equation (7.125), the zero occurs at

$$f_z = \frac{1}{2\pi C_\pi\left(\frac{r_\pi}{1+\beta}\right)} = \frac{1}{2\pi(35\times10^{-12})\left(\frac{3.82\times10^3}{151}\right)} \Rightarrow 180\,\text{MHz}$$

To determine the time constant for the high-frequency pole calculation, we know that

$$1 + g_m R_L' = 1 + g_m(R_E \| R_L) = 1 + (39.2)(0.5\|10) = 19.7$$

and

$$R_B = R_1 \| R_2 = 40\|5.72 = 5\,\text{k}\Omega$$

The time constant is therefore

$$\tau_P = [R_S \| R_B \| (1+g_m R_L')r_\pi]\left(C_\mu + \frac{C_\pi}{1+g_m R_L'}\right)$$
$$= [(0.1)\|5\|(19.7)(3.82)]\times10^3\left(4+\frac{35}{19.7}\right)\times10^{-12} \Rightarrow 0.566\,\text{ns}$$

The 3 dB frequency (or pole) is then

$$f_H = \frac{1}{2\pi\tau_P} = \frac{1}{2\pi(0.566\times10^{-9})} \Rightarrow 281\,\text{MHz}$$

Comment: The frequencies for the zero and the pole are very high and are not far apart. This makes the calculations suspect. However, since the frequencies are high, the emitter follower is a wide-bandwidth circuit.

Computer Verification: Figure 7.59 shows the results of a PSpice analysis of the emitter follower. From the hand analysis, the 3 dB frequency is on the order of 281 MHz. However, the computer results show the 3 dB frequency to be approximately 400 MHz. We must keep in mind that at these high frequencies, distributed parameter

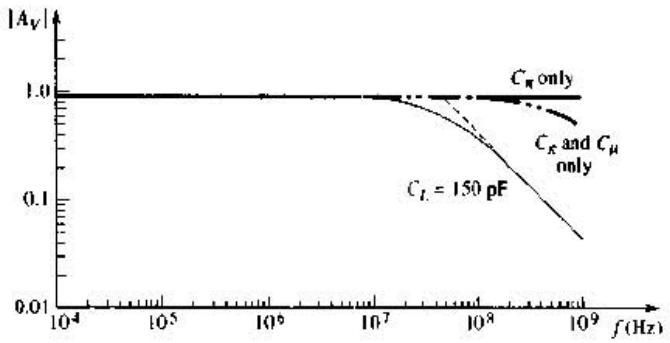


Figure 7.59 PSpice analysis results for emitter follower

effects may need to be considered in the transistor to more accurately predict the frequency response.

Also shown in the figure is the frequency response due to a 150 pF load capacitance. Comparing this result to the common-emitter circuit, for example, we see that the bandwidth of the emitter-follower circuit is approximately two orders of magnitude larger.

7.6.4 High-Frequency Amplifier Design

Our analysis shows that the frequency response, or the high-frequency cutoff point of an amplifier, depends on the transistor used, the circuit parameters, and the amplifier configuration.

We also saw that a computer simulation is easier than a hand analysis, particularly for the emitter-follower circuit. However, the parameters of the actual transistor used in the circuit must be used in the simulation if it is to predict the circuit frequency response accurately. Also, at high frequencies, additional parasitic capacitances, such as the collector–substrate capacitance, may need to be included. This was not done in our examples. Finally, in high-frequency amplifiers, the parasitic capacitances of the interconnect lines between the devices in an IC may also be a factor in the overall circuit response.

Test Your Understanding

***7.25** The transistor in the circuit in Figure 7.60 has parameters $\beta = 125$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, $V_A = 200\,\text{V}$, $C_\pi = 24\,\text{pF}$, and $C_\mu = 3\,\text{pF}$. (a) Calculate the Miller capacitance. (b) Determine the upper 3 dB frequency. (c) Determine the small-signal midband voltage gain. (Ans. (a) $C_M = 155\,\text{pF}$, (b) $f_H = 1.21\,\text{MHz}$, (c) $|A_v| = 37.3$)

***7.26** For the circuit in Figure 7.61, the transistor parameters are: $K_n = 1\,\text{mA/V}^2$, $V_{TN} = 0.8\,\text{V}$, $\lambda = 0$, $C_{gs} = 2\,\text{pF}$, and $C_{gd} = 0.2\,\text{pF}$. Determine: (a) the Miller capacitance, (b) the upper 3 dB frequency, and (c) the midband voltage gain. (d) Correlate the results from parts (b) and (c) with a computer analysis. (Ans. (a) $C_M = 1.62\,\text{pF}$, (b) $f_H = 3.38\,\text{MHz}$, (c) $|A_v| = 4.63$)

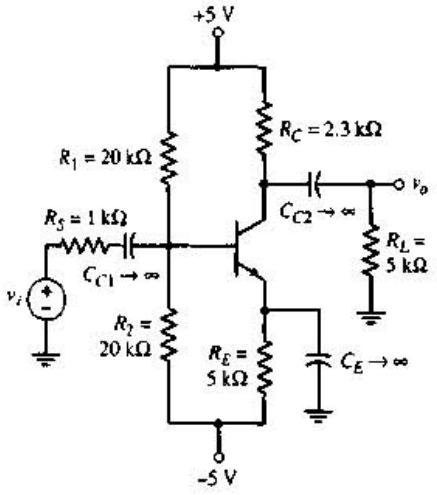


Figure 7.60 Figure for Exercise 7.25

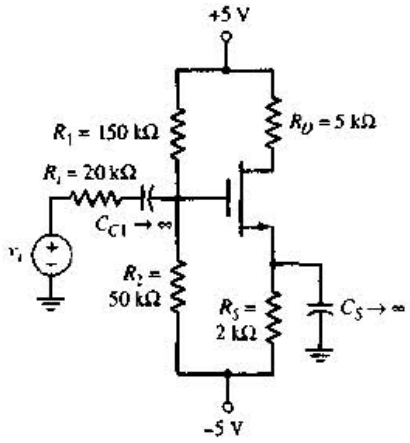


Figure 7.61 Figure for Exercise 7.26

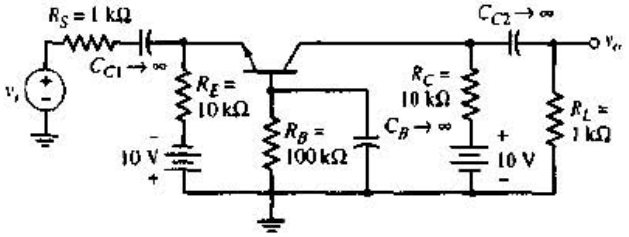


Figure 7.62 Figure for Exercise 7.27

***7.27** Consider the common-base circuit in Figure 7.62. The transistor parameters are $\beta = 100$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, $V_A = \infty$, $C_\pi = 24\,\text{pF}$, and $C_\mu = 3\,\text{pF}$. (a) Determine the upper 3 dB frequencies corresponding to the input and output portions of the equivalent circuit. (b) Calculate the small-signal midband voltage gain. (Ans. (a) $f_{H\pi} = 223\,\text{MHz}$, $f_{H\mu} = 58.3\,\text{MHz}$, (b) $A_v = 0.869$)

***7.28** For the circuit in Figure 7.63, the transistor parameters are: $V_{TN} = 1\,\text{V}$, $K_n = 1\,\text{mA/V}^2$, $\lambda = 0$, $C_{gd} = 0.4\,\text{pF}$, and $C_{gs} = 5\,\text{pF}$. Perform a computer simulation to determine the upper 3 dB frequency and the midband small-signal voltage gain. (Ans. $f_H = 64.5\,\text{MHz}$, $|A_v| = 0.127$)

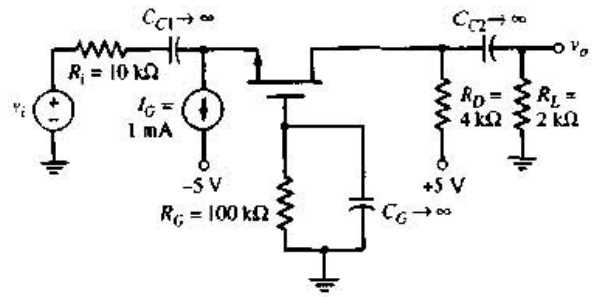


Figure 7.63 Figure for Exercise 7.28

***7.29** The cascode circuit in Figure 7.54 has parameters $V^+ = 12\,\text{V}$, $V^- = 0$, $R_1 = 58.8\,\text{k}\Omega$, $R_2 = 33.3\,\text{k}\Omega$, $R_3 = 7.92\,\text{k}\Omega$, $R_C = 7.5\,\text{k}\Omega$, $R_S = 1\,\text{k}\Omega$, $R_E = 0.5\,\text{k}\Omega$, and $R_L = 2\,\text{k}\Omega$. The transistor parameters are: $\beta = 100$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, $V_A = \infty$, $C_\pi = 24\,\text{pF}$, and $C_\mu = 3\,\text{pF}$. Let C_L be an open circuit. (a) Determine the 3 dB frequencies corresponding to the input and output portions of the equivalent circuit. (b) Calculate the small-signal midband voltage gain. (c) Correlate the results from parts (a) and (b) with a computer analysis. (Ans. (a) $f_{H\pi} = 7.17\,\text{MHz}$, $f_{H\mu} = 33.6\,\text{MHz}$, (b) $|A_v| = 22.5$)

7.7 SUMMARY

- In this chapter, we studied the frequency response of transistor circuits. We determined the effects due to circuit capacitors, including coupling, bypass, and load capacitors, and also analyzed the expanded equivalent circuits of BJTs and FETs to determine the frequency response of the transistors.
- A time constant technique was developed so that Bode plots can be constructed without the need of deriving complex transfer functions. The high and low corner frequencies or 3 dB frequencies can be determined directly from the time constants.
- Coupling and bypass capacitors affect the low-frequency characteristics of a circuit. In general, capacitance values in the microfarad range typically result in cutoff frequencies in the hertz or tens of hertz range. A load capacitor affects the high-frequency characteristics of a circuit. Load capacitances in the picofarad range typically result in cutoff frequencies in the vicinity of a megahertz or higher.
- An expanded hybrid-π model for the bipolar transistor and a high-frequency model for the field-effect transistor were developed. The capacitances included in these models result in reduced transistor gain at high frequencies. The cutoff frequency is a figure of merit for the transistor and is defined as the frequency at which the magnitude of the current gain is unity.
- The Miller effect is a multiplication of the base-collector or gate-drain capacitance due to feedback between the output and input of the transistor circuit. The bandwidth of the amplifier is reduced by this effect.
- The common-emitter (common-source) amplifier, in general, shows the greatest effect of the Miller multiplication factor, so the bandwidth of this circuit is the smallest of the three basic types of amplifiers. The common-base (common-gate) amplifier has a larger bandwidth because of a smaller Miller multiplication factor. The cascode configuration, a combination of common-emitter and common-base stages, combines the advantages of high gain and wide bandwidth. The emitter-follower (source-follower) amplifier generally has the largest bandwidth of the three basic amplifier configurations.

CHECKPOINT

After studying this chapter, the reader should have the ability to:

- ✔ Construct the Bode plots of the gain magnitude and phase from a transfer function written in terms of the complex frequency s. (Section 7.2)
- ✔ Construct the Bode plots of the gain magnitude and phase of electronic amplifier circuits, taking into account circuit capacitors, using the time constant technique. (Section 7.3)
- ✔ Determine the short-circuit current gain versus frequency of a BJT and determine the Miller capacitance of a BJT circuit using the expanded hybrid-π equivalent circuit. (Section 7.4)

✔ Determine the unity-gain bandwidth of an FET and determine the Miller capacitance of an FET circuit using the expanded small-signal equivalent circuit. (Section 7.5)

✔ Describe the relative frequency responses of the three basic amplifier configurations and the cascode amplifier. (Section 7.6)

REVIEW QUESTIONS

1. Describe the general frequency response of an amplifier and define the low-frequency, midband, and high-frequency ranges.
2. Describe the general characteristics of the equivalent circuits that apply to the low-frequency, midband, and high-frequency ranges.
3. Describe what is meant by a system transfer function in the s-domain.
4. What is the criterion that defines a corner, or 3 dB, frequency?
5. Define octave and decade.
6. Describe what is meant by the phase of the transfer function.
7. Describe the time constant technique for determining the corner frequencies.
8. Describe the general frequency response of a coupling capacitor.
9. Describe the general frequency response of a bypass capacitor.
10. Describe the general frequency response of a load capacitor.
11. Sketch the expanded hybrid-π model of the BJT.
12. Describe the short-circuit current gain versus frequency characteristics of the BJT.
13. Define the cutoff frequency for a BJT.
14. Describe the Miller effect and the Miller capacitance.
15. What effect does the Miller capacitance have on the amplifier bandwidth?
16. Sketch the expanded small-signal equivalent circuit of a MOSFET.
17. Define the cutoff frequency for a MOSFET.
18. What is the major contribution to the Miller capacitance in a MOSFET?
19. Why is there not a Miller effect in a common-base circuit?
20. Describe the configuration of a cascode amplifier.
21. Why is the bandwidth of a cascode amplifier larger, in general, than that of a simple common-emitter amplifier?
22. Why is the bandwidth of the emitter-follower amplifier the largest of the three basic BJT amplifiers?

PROBLEMS

Section 7.2 System Transfer Functions

7.1 (a) Determine the voltage transfer function $T(s) = V_o(s)/V_i(s)$ for the circuit shown in Figure P7.1. (b) Sketch the Bode magnitude plot and determine the corner frequency. (c) Determine the time response of the circuit to an input step function of magnitude V_{io}.

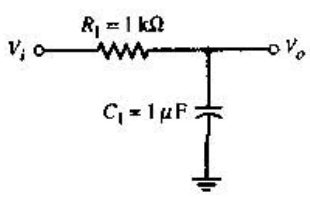


Figure P7.1

7.2 Repeat Problem 7.1 for the circuit in Figure P7.2.

***7.3** (a) Derive the voltage transfer function $T(s) = V_o(s)/V_i(s)$ for the circuit shown in Figure 7.10, taking both capacitors into account. (b) Let $R_S = R_P = 10\ \text{k}\Omega$, $C_S = 1\ \mu\text{F}$, and $C_P = 10\ \text{pF}$. Calculate the actual magnitude of the transfer function at $f_L = 1/[(2\pi)(R_S + R_P)C_S]$ and at $f_H = 1/[(2\pi)(R_S \| R_P)C_P]$. How do these magnitudes

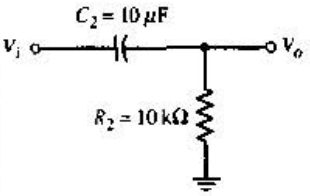


Figure P7.2

compare to the maximum magnitude of $R_P/(R_S + R_P)$? (c) Repeat part (b) for $R_S = R_P = 10\,k\Omega$ and $C_S = C_P = 0.1\,\mu F$.

7.4 (a) For the two circuits in Figure P7.4, sketch the Bode magnitude plot and Bode phase plot of the voltage transfer function. (b) Verify the results of part (a) with a computer simulation.

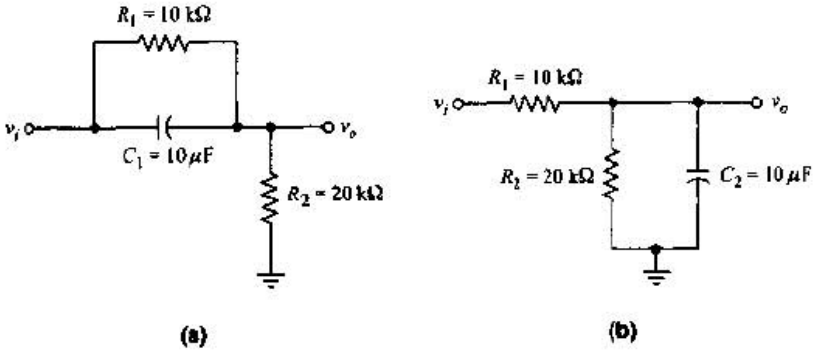


Figure P7.4

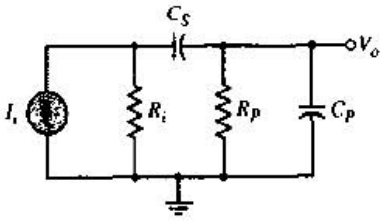


Figure P7.5

7.5 Consider the circuit in Figure P7.5 with a signal current source. The circuit parameters are $R_i = 30\,k\Omega$, $R_P = 10\,k\Omega$, $C_S = 10\,\mu F$, and $C_P = 50\,pF$. (a) Determine the open-circuit time constant associated with C_S and the short-circuit time constant associated with C_P. (b) Determine the corner frequencies and the magnitude of the transfer function $T(s) = V_o(s)/I_i(s)$ at midband. (c) Sketch the Bode magnitude plot.

7.6 A voltage transfer function is given by $T(jf) = 1/(1 + j2\pi f\tau)^2$. (a) Show that the actual response at $f = 1/(2\pi\tau)$ is approximately $-6\,dB$ below the maximum value. What is the phase angle at this frequency? (b) What is the slope of the magnitude plot for $f \gg 1/(2\pi\tau)$? What is the phase angle in this frequency range?

7.7 Sketch the Bode magnitude plots for the following functions:

$$\text{(a)}\quad T(s) = \frac{-10s}{(s+20)(s+2000)} \qquad \text{(b)}\quad T(s) = \frac{10(s+10)}{(s+1000)}$$

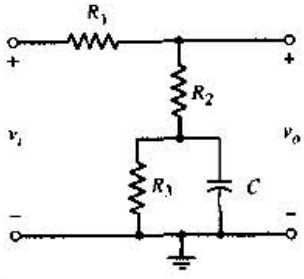


Figure P7.9

7.8 Consider the circuit shown in Figure 7.15 with parameters $R_S = 0.5\,k\Omega$, $r_\pi = 5.2\,k\Omega$, $g_m = 29\,mA/V$, and $R_L = 6\,k\Omega$. The corner frequencies are $f_L = 30\,Hz$ and $f_H = 480\,kHz$. (a) Calculate the midband voltage gain. (b) What are the open-circuit and short-circuit time constants? (c) Determine C_C and C_L.

7.9 For the circuit shown in Figure P7.9, the parameters are: $R_1 = 10\,k\Omega$, $R_2 = 10\,k\Omega$, $R_3 = 40\,k\Omega$, and $C = 10\,\mu F$. Using a computer simulation, plot the magnitude and phase of the voltage transfer function. From the computer analysis, determine the

frequency at which the magnitude of the voltage transfer function is 3 dB below the maximum asymptotic value.

7.10 The circuit shown in Figure 7.10 has parameters $R_S = 1\,\text{k}\Omega$, $R_P = 10\,\text{k}\Omega$, and $C_S = C_P = 0.01\,\mu\text{F}$. Using PSpice, plot the magnitude and phase of the voltage transfer function. Determine the maximum value of the voltage transfer function. Determine the frequencies at which the magnitude is $1/\sqrt{2}$ of the peak value.

Section 7.3 Frequency Response: Transistor Circuits

7.11 For the common-emitter circuit in Figure P7.11, the transistor parameters are: $\beta = 100$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, and $V_A = \infty$. (a) Calculate the lower corner frequency. (b) Determine the midband voltage gain. (c) Sketch the Bode plot of the voltage gain magnitude.

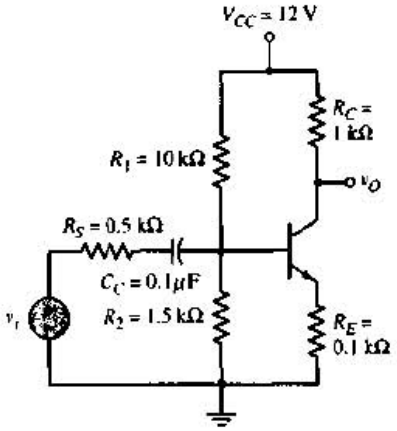


Figure P7.11

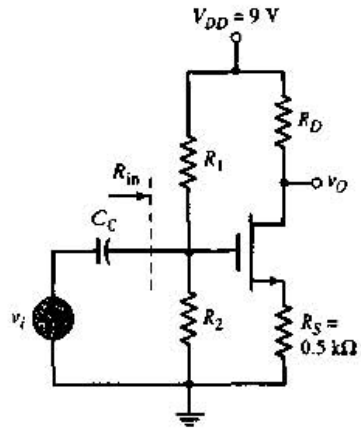


Figure P7.12

D7.12 Design the circuit shown in Figure P7.12 such that $I_{DQ} = 0.5\,\text{mA}$, $V_{DSQ} = 4.5\,\text{V}$, $R_{in} = 200\,\text{k}\Omega$, and the lower corner frequency is $f_L = 20\,\text{Hz}$. The transistor parameters are: $K_n = 0.2\,\text{mA/V}^2$, $V_{TN} = 1.5\,\text{V}$, and $\lambda = 0$. Sketch the Bode plot of the voltage magnitude and phase.

D7.13 The transistor in the circuit in Figure P7.13 has parameters $K_n = 0.5\,\text{mA/V}^2$, $V_{TN} = 1\,\text{V}$, and $\lambda = 0$. (a) Design the circuit such that $I_{DQ} = 1\,\text{mA}$ and $V_{DSQ} = 3\,\text{V}$.

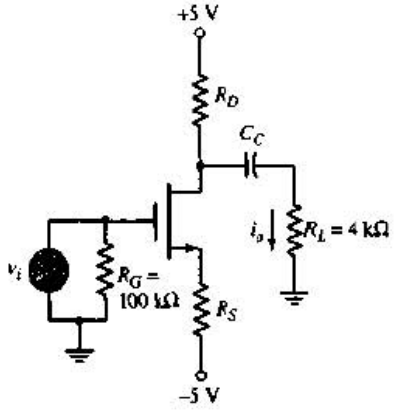


Figure P7.13

(b) Derive the expression for the transfer function $T(s) = I_o(s)/V_i(s)$. What is the expression for the circuit time constant? (c) Determine C_C such that the lower 3 dB frequency is 10 Hz. (d) Verify the results of parts (a) and (c) with a computer simulation.

***D7.14** The transistor in the circuit in Figure P7.14 has parameters $K_p = 0.5\,\text{mA/V}^2$, $V_{TP} = -2\,\text{V}$, and $\lambda = 0$. (a) Determine R_o. (b) What is the expression for the circuit time constant? (c) Determine C_C such that the lower 3 dB frequency is 20 Hz.

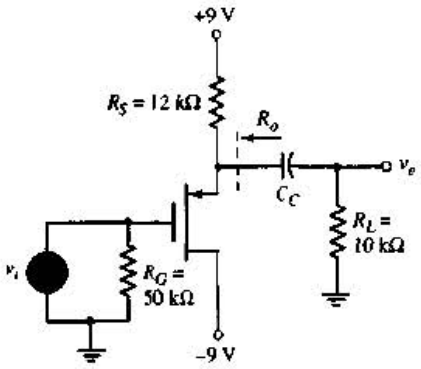


Figure P7.14

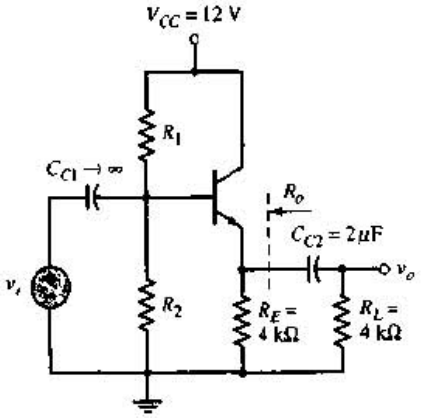


Figure P7.15

***D7.15** For the circuit in Figure P7.15, the transistor parameters are: $\beta = 120$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, and $V_A = 80\,\text{V}$. (a) Design a bias-stable circuit such that $I_{CQ} = 1\,\text{mA}$. (b) Determine the output resistance R_o. (c) What is the lower 3 dB corner frequency?

7.16 The parameters of the transistor in the circuit in Figure P7.16 are $K_p = 1\,\text{mA/V}^2$, $V_{TP} = -1.5\,\text{V}$, and $\lambda = 0$. (a) Determine the quiescent and small-signal parameters of the transistor. (b) Find the time constants associated with C_{C1} and C_{C2}. (c) Is there a dominant pole frequency? Estimate the −3 dB frequency.

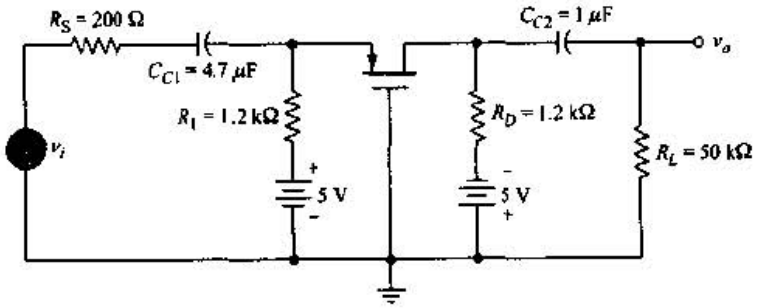


Figure P7.16

***D7.17** A MOSFET amplifier with the configuration in Figure P7.17 is to be designed for use in a telephone circuit. The magnitude of the voltage gain should be 10 in the midband range, and the midband frequency range should extend from 200 Hz to 3 kHz. [Note: A telephone's frequency range does not correspond to a high-fidelity system's.] All resistor, capacitor, and MOSFET parameters should be specified.

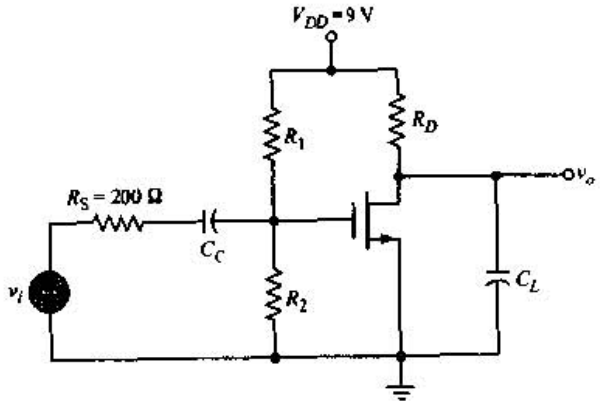


Figure P7.17

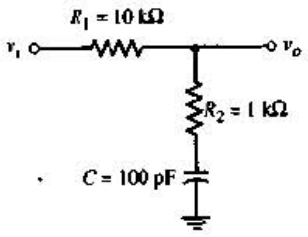


Figure P7.18

***7.18** Consider the circuit in Figure P7.18. (a) Derive the expression for the voltage transfer function $T(s) = V_o(s)/V_i(s)$. Arrange the terms in the form $T(s) \propto (1 + s\tau_A)/(1 + s\tau_B)$. (b) Sketch the Bode magnitude plot. (c) Determine the time constants and corner frequencies.

7.19 The circuit in Figure P7.19 is a simple output stage of an audio amplifier. The transistor parameters are $\beta = 200$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, and $V_A = \infty$. Determine C_C such that the lower $-3\,\text{dB}$ frequency is 15 Hz.

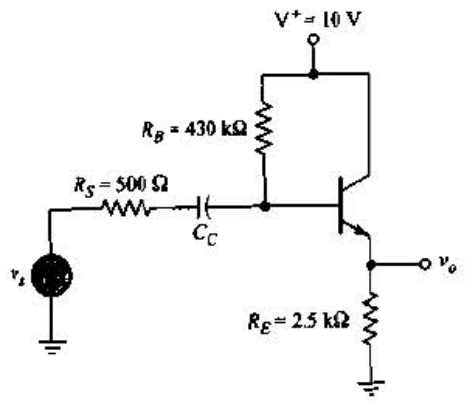


Figure P7.19

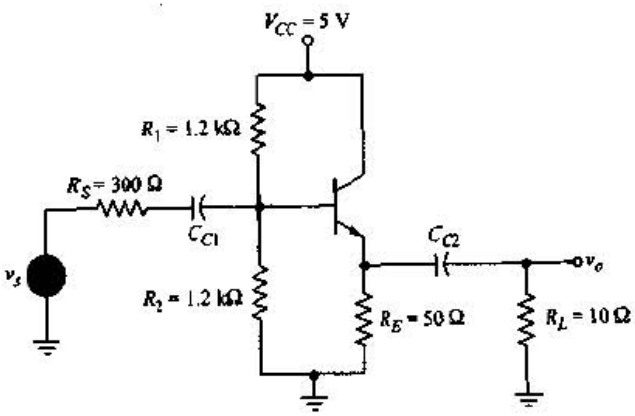


Figure P7.20

D7.20 The parameters of the transistor in the circuit in Figure P7.20 are $\beta = 100$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, and $V_A = \infty$. The time constant associated with C_{C1} is a factor of 100 larger than the time constant associated with C_{C2}. (a) Determine C_{C2} such that the $-3\,\text{dB}$ frequency associated with this capacitor is 25 Hz. (b) Determine C_{C1}.

***D7.21** For the transistor in the circuit in Figure P7.21, the parameters are: $K_n = 0.5\,\text{mA/V}^2$, $V_{TN} = 0.8\,\text{V}$, and $\lambda = 0$. (a) Design the circuit such that $I_{DQ} = 0.5\,\text{mA}$ and $V_{DSQ} = 4\,\text{V}$. (b) Determine the 3 dB frequencies. (c) If the R_S resistor is replaced by a constant-current source producing the same I_{DQ} quiescent current, determine the 3 dB corner frequencies.

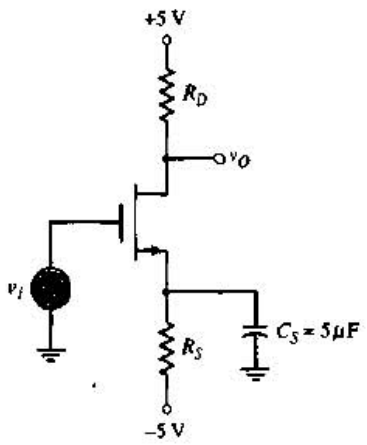


Figure P7.21

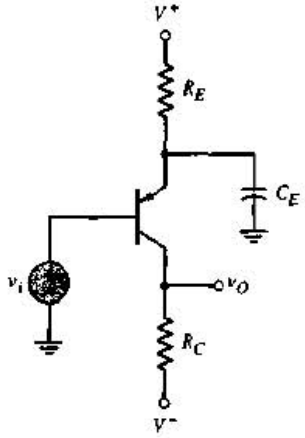


Figure P7.23

***7.22** For the circuit in Figure 7.23(a) in the text, the parameters are: $V^+ = 10\,\text{V}$, $V^- = -10\,\text{V}$, $R_S = 0$, $R_E = 5\,\text{k}\Omega$, and $R_C = 1.5\,\text{k}\Omega$. The transistor parameters are $V_{BE}(\text{on}) = 0.7\,\text{V}$ and $V_A = \infty$, and the transistor current gain β is in the range $75 \le \beta \le 125$. (a) Determine the value of C_E such that the low-frequency 3 dB point is $f_B \le 200\,\text{Hz}$. (b) From the results of part (a), determine the range in frequencies f_B and f_A.

***7.23** The common-emitter circuit in Figure P7.23 has an emitter bypass capacitor. (a) Derive the expression for the small-signal voltage gain $A_v(s) = V_o(s)/V_i(s)$. Write the expression in a form similar to that of Equation (7.59). (b) What are the expressions for the time constants τ_A and τ_B?

7.24 In the common-base circuit in Figure 7.29 in the text, the transistor parameters are: $\beta = 100$, $V_{EB}(\text{on}) = 0.7\,\text{V}$, and $V_A = \infty$. A load capacitance $C_L = 15\,\text{pF}$ is connected in parallel with R_L. Determine the upper 3 dB frequency and the small-signal midband voltage gain.

7.25 For the circuit in Figure P7.25, the transistor parameters are: $K_n = 0.5\,\text{mA/V}^2$, $V_{TN} = 2\,\text{V}$, and $\lambda = 0$. Determine the maximum value of C_L such that the bandwidth is at least $BW = 5\,\text{MHz}$. State any approximations or assumptions that you make. What is the magnitude of the small-signal midband voltage gain? Verify the results with a computer simulation.

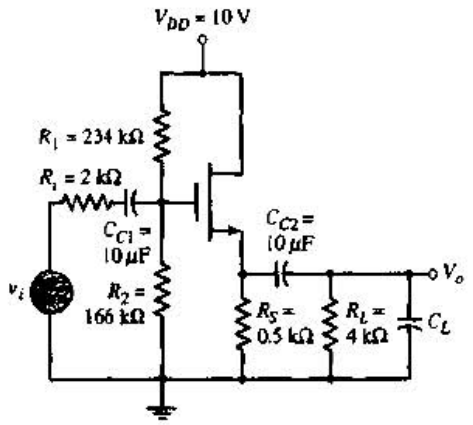


Figure P7.25

7.26 The parameters of the transistor in the circuit in Figure P7.26 are $\beta = 100$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, and $V_A = \infty$. Neglect the capacitance effects of the transistor. (a) Draw the three equivalent circuits that represent the amplifier in the low-frequency range, midband range, and the high frequency range. (b) Sketch the Bode magnitude plot. (c) Determine the values of $|A_m|_{\text{dB}}$, f_L, and f_H.

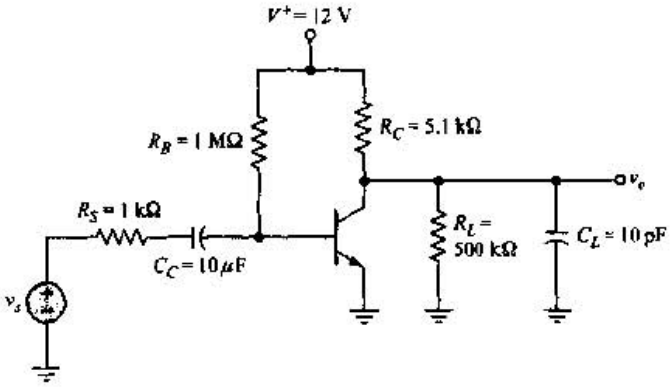


Figure P7.26

7.27 In the common-source amplifier in Figure 7.20(a) in the text, a source bypass capacitor is to be added between the source terminal and ground potential. The circuit and transistor parameters are as described in Example 7.6. (a) Derive the small-signal voltage gain expression, as a function of s, that describes the circuit behavior in the high-frequency range. (b) What is the expression for the time constant associated with the upper 3 dB frequency? (c) Determine the time constant, upper 3 dB frequency, and small-signal midband voltage gain.

***7.28** Consider the common-base circuit in Figure P7.28. Choose appropriate transistor parameters. (a) Using a computer analysis, generate the Bode plot of the voltage gain magnitude from a very low frequency to the midband frequency range. At what frequency is the voltage gain magnitude 3 dB below the maximum value? What is the slope of the curve at very low frequencies? (b) Using the PSpice analysis, determine the voltage gain magnitude, input resistance R_i, and output resistance R_o at midband.

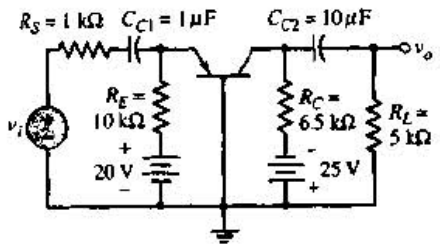


Figure P7.28

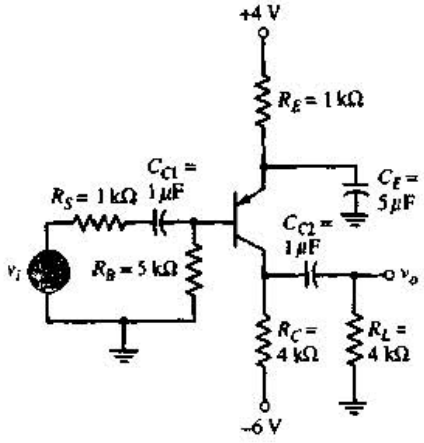


Figure P7.29

***7.29** For the common-emitter circuit in Figure P7.29, choose appropriate transistor parameters and perform a computer analysis. Generate the Bode plot of the voltage gain

magnitude from a very low frequency to the midband frequency range. At what frequency is the voltage gain magnitude 3 dB below the maximum value? Does one capacitor dominate this 3 dB frequency? If so, which one?

***7.30** For the multitransistor amplifier in Figure P7.30, choose appropriate transistor parameters. The lower 3 dB frequency is to be less than or equal to 20 Hz. Assume that all three coupling capacitors are equal. Let $C_B \to \infty$. Using a computer analysis, determine the maximum values of the coupling capacitors. Determine the slope of the Bode plot of the voltage gain magnitude at very low frequencies.

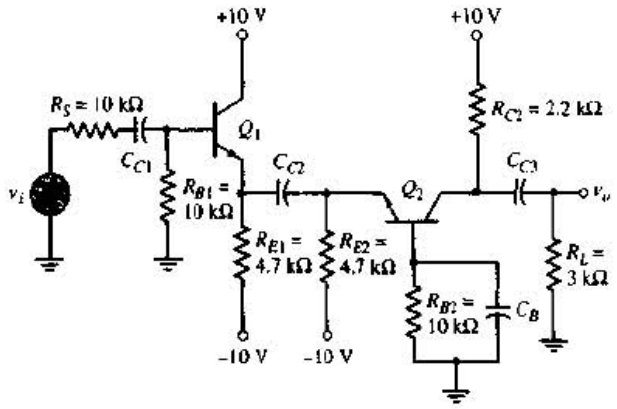


Figure P7.30

Section 7.4 Frequency Response: Bipolar Transistor

7.31 A bipolar transistor is biased at $I_{CQ} = 1$ mA and has parameters $C_\pi = 10$ pF, $C_\mu = 2$ pF, and $\beta_o = 120$. Determine f_β and f_T.

7.32 A high-frequency bipolar transistor is biased at $I_{CQ} = 0.5$ mA and has parameters $C_\mu = 0.15$ pF, $f_T = 5$ GHz, and $\beta_o = 150$. Determine C_π and f_β.

7.33 For a bipolar transistor, the unity-gain bandwidth is $f_T = 2$ GHz and the low-frequency current gain is $\beta_o = 150$. (a) Determine f_β. (b) Find the frequency at which the magnitude of h_{fe} is 10.

7.34 The circuit in Figure P7.34 is a hybrid-π equivalent circuit including the resistance r_b. (a) Derive the expression for the voltage gain transfer function $A_v(s) = V_o(s)/V_i(s)$. (b) If the transistor is biased at $I_{CQ} = 1$ mA, and if $R_L = 4\,k\Omega$ and $\beta_o = 100$, determine the midband voltage gain for (i) $r_b = 100\,\Omega$ and (ii) $r_b = 500\,\Omega$. (c) For $C_1 = 2.2$ pF, determine the -3 dB frequency for (i) $r_b = 100\,\Omega$ and (ii) $r_b = 500\,\Omega$.

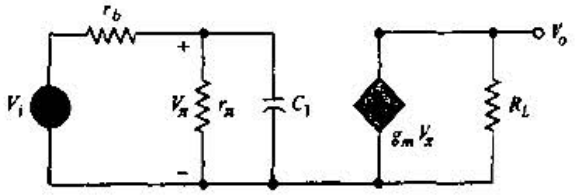


Figure P7.34

***7.35** A common-emitter equivalent circuit is shown in Figure P7.35. (a) What is the expression for the Miller capacitance? (b) Derive the expression for the voltage gain $A_v(s) = V_o(s)/V_i(s)$ in terms of the Miller capacitance and other circuit parameters. (c) What is the expression for the upper 3 dB frequency?

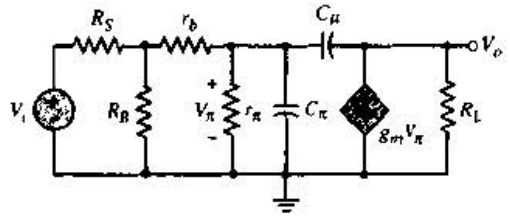


Figure P7.35

7.36 For the common-emitter circuit in Figure 7.37(a) in the text, assume that $r_s = \infty$, $R_1 \| R_2 = 5\,\text{k}\Omega$, and $R_C = R_L = 1\,\text{k}\Omega$. The transistor is biased at $I_{CQ} = 5\,\text{mA}$ and the parameters are: $\beta_o = 200$, $V_A = \infty$, $C_\mu = 5\,\text{pF}$, and $f_T = 250\,\text{MHz}$. Determine the upper 3 dB frequency for the small-signal current gain.

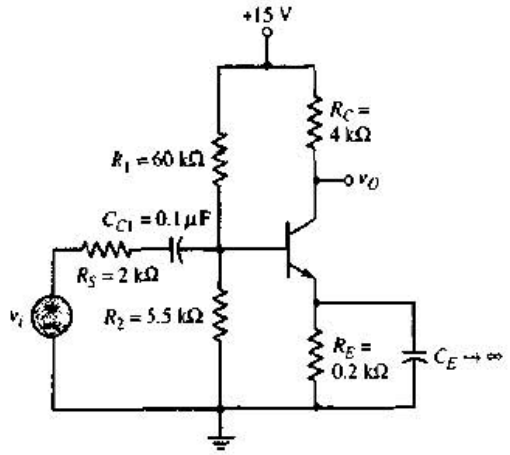


Figure P7.37

***7.37** For the common-emitter circuit in Figure P7.37, assume the emitter bypass capacitor C_E is very large, and the transistor parameters are: $\beta_o = 100$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, $V_A = \infty$, $C_\mu = 2\,\text{pF}$, and $f_T = 400\,\text{MHz}$. Determine the lower and upper 3 dB frequencies for the small-signal voltage gain. Use the simplified hybrid-π model for the transistor.

Section 7.5 Frequency Response: The FET

7.38 A MOSFET is biased at $I_{DQ} = 100\,\mu\text{A}$, and the parameters are: $(\frac{1}{2})\mu_n C_{ox} = 15\,\mu\text{A/V}^2$, $W = 40\,\mu\text{m}$, $L = 10\,\mu\text{m}$, $C_{gs} = 0.5\,\text{pF}$, and $C_{gd} = 0.05\,\text{pF}$. Determine f_T.

7.39 A common-source equivalent circuit is shown in Figure P7.39. The transistor transconductance is $g_m = 3\,\text{mA/V}$. (a) Calculate the equivalent Miller capacitance. (b) Determine the uper 3 dB frequency for the small-signal voltage gain.

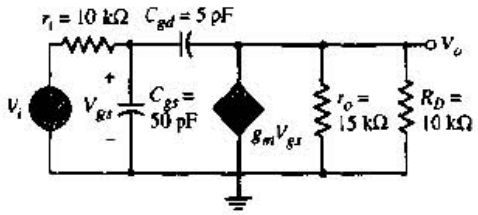


Figure P7.39

7.40 Starting with the definition of unity-gain frequency, as given by Equation (7.90), neglect the overlap capacitance, assume $C_{gd} \cong 0$ and $C_{gs} \cong (\frac{2}{3})WLC_{ox}$, and show that

$$f_T = \frac{3}{2\pi L}\sqrt{\frac{\mu_n I_D}{2C_{ox}WL}}$$

Since I_D is proportional to W, this relationship indicates that to increase f_T, the channel length L must be small.

7.41 For an ideal n-channel MOSFET, $(W/L) = 10$, $\mu_n = 400\,\text{cm}^2/\text{V-s}$, $C_{ox} = 7.25 \times 10^{-8}\,\text{F/cm}^2$, and $V_{TN} = 0.65\,\text{V}$. (a) Determine the maximum source resistance such that the transconductance g_m is reduced by no more than 20 percent from its ideal value when $V_{GS} = 5\,\text{V}$. (b) Using the value of r_s calculated in part (a), determine how much g_m is reduced from its ideal value when $V_{GS} = 3\,\text{V}$.

***7.42** Figure P7.42 shows the high-frequency equivalent circuit of an FET, including a source resistance r_s. (a) Derive an expression for the low-frequency current gain $A_i = I_o/I_i$. (b) Assuming R_i is very large, derive an expression for the current gain transfer function $A_i(s) = I_o(s)/I_i(s)$. (c) How does the magnitude of the current gain behave as r_s increases?

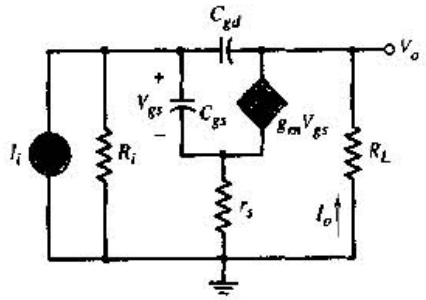


Figure P7.42

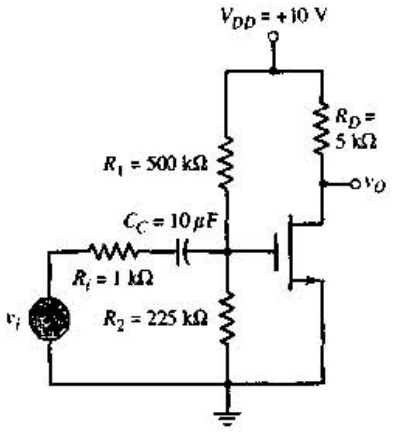


Figure P7.43

7.43 For the FET circuit in Figure P7.43, the transistor parameters are: $K_n = 1\,\text{mA/V}^2$, $V_{TN} = 2\,\text{V}$, $\lambda = 0$, $C_{gs} = 5\,\text{pF}$, and $C_{gd} = 1\,\text{pF}$. (a) Draw the simplified high-frequency equivalent circuit. (b) Calculate the equivalent Miller capacitance. (c) Determine the upper 3 dB frequency for the small-signal voltage gain and find the midband voltage gain.

Section 7.6 High-Frequency Response of Transistor Circuits

7.44 In the circuit in Figure P7.44, the transistor parameters are: $\beta = 120$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, $V_A = 100\,\text{V}$, $C_\mu = 1\,\text{pF}$, and $f_T = 600\,\text{MHz}$. (a) Determine C_π and the equivalent Miller capacitance C_M. State any approximations or assumptions that you make. (b) Find the upper 3 dB frequency and the midband voltage gain.

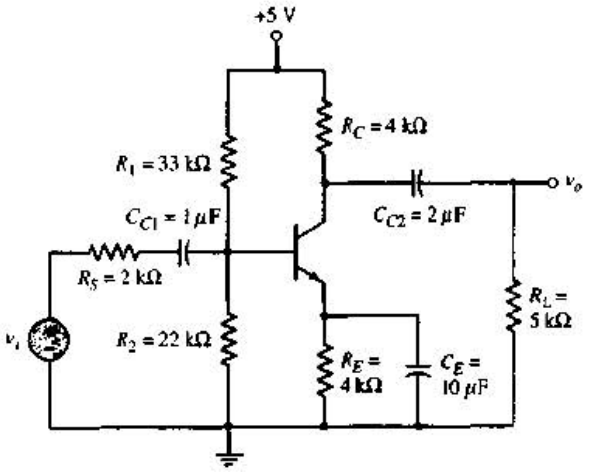


Figure P7.44

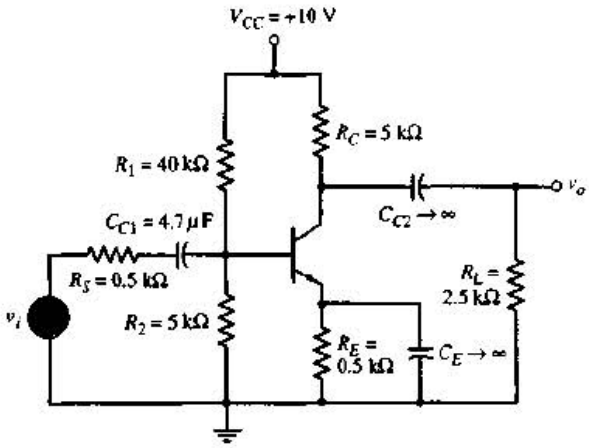


Figure P7.45

***7.45** In the circuit in Figure P7.45, the transistor parameters are: $\beta = 120$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, $V_A = \infty$, $C_\mu = 3\,\text{pF}$, and $f_T = 250\,\text{MHz}$. Assume the emitter bypass capacitor C_E and the coupling capacitor C_{C2} are very large. (a) Determine the lower and upper 3 dB frequencies. Use the simplified hybrid-π model for the transistor. (b) Sketch the Bode plot of the voltage gain magnitude.

7.46 The parameters of the transistor in the common-source circuit in Figure P7.46 are: $K_p = 2\,\text{mA/V}^2$, $V_{TP} = -2\,\text{V}$, $\lambda = 0.01\,\text{V}^{-1}$, $C_{gs} = 10\,\text{pF}$, and $C_{gd} = 1\,\text{pF}$. (a) Determine the equivalent Miller capacitance C_M. (b) Find the upper 3 dB frequency and midband voltage gain.

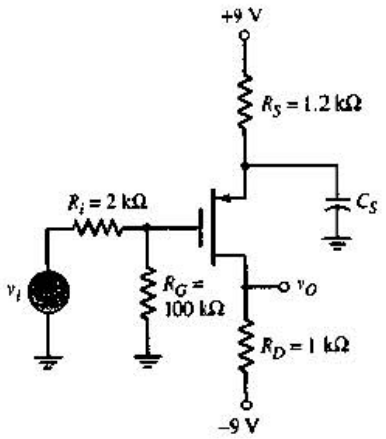


Figure P7.46

7.47 For the PMOS common-source circuit shown in Figure P7.47, the transistor parameters are: $V_{TP} = -2\,\text{V}$, $K_p = 1\,\text{mA/V}^2$, $\lambda = 0$, $C_{gs} = 15\,\text{pF}$, and $C_{gd} = 3\,\text{pF}$. (a) Determine the upper 3 dB frequency. (b) What is the equivalent Miller capacitance? State any assumptions or approximations that you make. (c) Find the midband voltage gain.

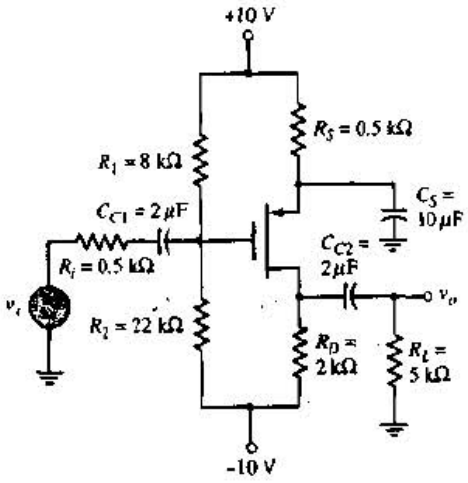


Figure P7.47

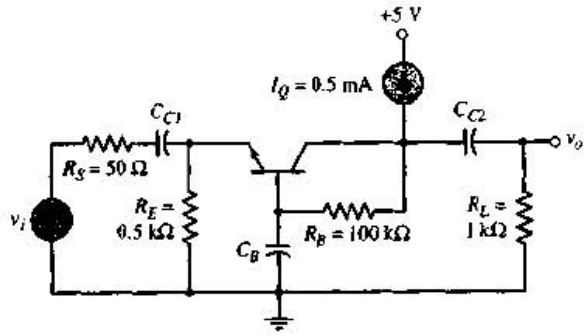


Figure P7.48

***7.48** In the common-base circuit shown in Figure P7.48, the transistor parameters are: $\beta = 100$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, $V_A = \infty$, $C_\pi = 10\,\text{pF}$, and $C_\mu = 1\,\text{pF}$. (a) Determine the upper 3 dB frequencies corresponding to the input and output portions of the equivalent circuit. (b) Calculate the small-signal midband voltage gain. (c) If a load capacitor $C_L = 15\,\text{pF}$ is connected between the output and ground, determine if the upper 3 dB frequency will be dominated by the C_L load capacitor or by the transistor characteristics.

***7.49** Repeat Problem 7.48 for the common-base circuit in Figure P7.49. Assume V_{EB} (on) = 0.7 for the pnp transistor. The remaining transistor parameters are the same as given in Problem 7.48.

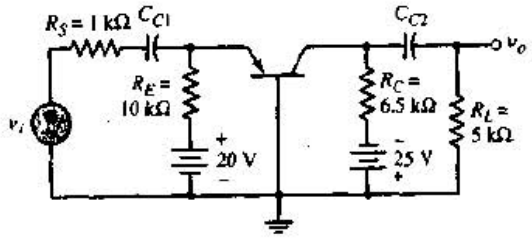


Figure P7.49

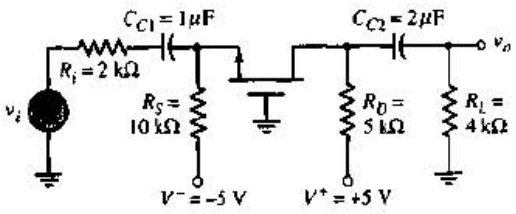


Figure P7.50

***7.50** In the common-gate circuit in Figure P7.50, the transistor parameters are: $V_{TN} = 1\,\text{V}$, $K_n = 3\,\text{mA/V}^2$, $\lambda = 0$, $C_{gs} = 15\,\text{pF}$, and $C_{gd} = 4\,\text{pF}$. Determine the upper 3 dB frequency and midband voltage gain.

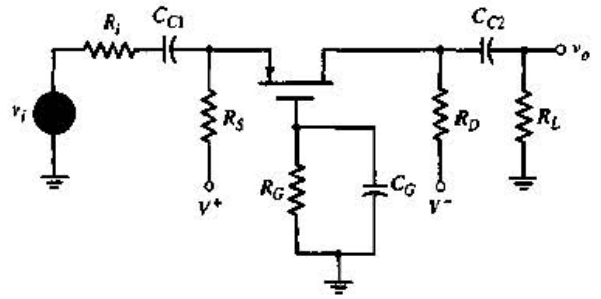


Figure P7.51

7.51 Consider the common-gate circuit in Figure P7.51 with parameters $V^+ = 5\,\text{V}$, $V^- = -5\,\text{V}$, $R_S = 4\,\text{k}\Omega$, $R_D = 2\,\text{k}\Omega$, $R_L = 4\,\text{k}\Omega$, $R_G = 50\,\text{k}\Omega$, and $R_i = 0.5\,\text{k}\Omega$. The transistor parameters are: $K_p = 1\,\text{mA/V}^2$, $V_{TP} = -0.8\,\text{V}$, $\lambda = 0$, $C_{gs} = 4\,\text{pF}$, and $C_{gd} = 1\,\text{pF}$. Determine the upper 3 dB frequency and midband voltage gain.

***7.52** For the cascode circuit in Figure 7.54 in the text, circuit parameters are the same as described in Example 7.16. The transistor parameters are: $\beta_o = 120$, $V_A = \infty$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, $C_\pi = 12\,\text{pF}$, and $C_\mu = 2\,\text{pF}$. (a) If C_L is an open circuit, determine the 3 dB frequencies corresponding to the input and output portions of the equivalent circuit. (b) Determine the midband voltage gain. (c) If a load capacitance $C_L = 15\,\text{pF}$ is connected to the output, determine if the upper 3 dB frequency is dominated by the load capacitance or by the transistor characteristics.

COMPUTER SIMULATION PROBLEMS

***7.53** An emitter-follower circuit is shown in Figure P7.53. Assume the transistor parameters are: $\beta_0 = 100$, $V_A = \infty$, $C_\pi = 35\,\text{pF}$, and $C_\mu = 4\,\text{pF}$. From a PSpice analysis, determine the upper 3 dB frequency and midband voltage gain for: (a) $R_L = 0.2\,\text{k}\Omega$, (b) $R_L = 2\,\text{k}\Omega$, and (c) $R_L = 20\,\text{k}\Omega$. Explain any differences between the results.

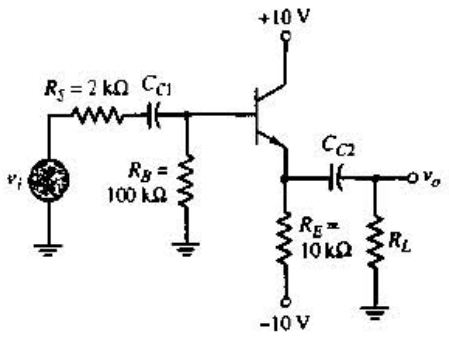


Figure P7.53

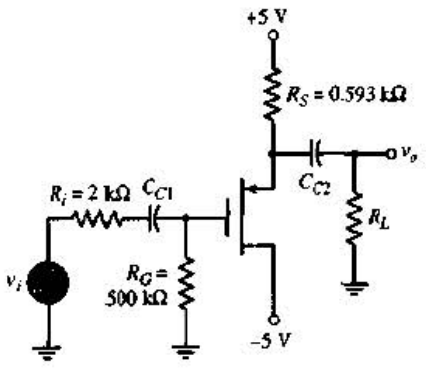


Figure P7.54

***7.54** For the source-follower circuit shown in Figure P7.54, assume the transistor parameters are: $V_{TP} = -2\,\text{V}$, $K_p = 2\,\text{mA/V}^2$, $\lambda = 0.02\,\text{V}^{-1}$, $C_{gs} = 5\,\text{pF}$, and $C_{gd} = 0.8\,\text{pF}$. From a PSpice analysis, determine the upper 3 dB frequency and midband

voltage gain for: (a) $R_L = 0.2\,\text{k}\Omega$, (b) $R_L = 2\,\text{k}\Omega$, and (c) $R_L = 20\,\text{k}\Omega$. Explain any differences between the results.

***7.55** The emitter-follower is a wide bandwidth circuit, but the voltage gain is slightly less than unity. Figure P7.55 shows a cascade configuration of an emitter follower and a common emitter. Investigate the possibility of obtaining the properties of wide bandwidth from the emitter follower and a large voltage gain from the common emitter in a single circuit. Assume the transistor parameters are identical and are: $\beta_o = 150$, $V_A = \infty$, $C_\pi = 24\,\text{pF}$, and $C_\mu = 4\,\text{pF}$. Determine the upper 3 dB frequency and midband gain. How do these results compare to those of a cascode circuit?

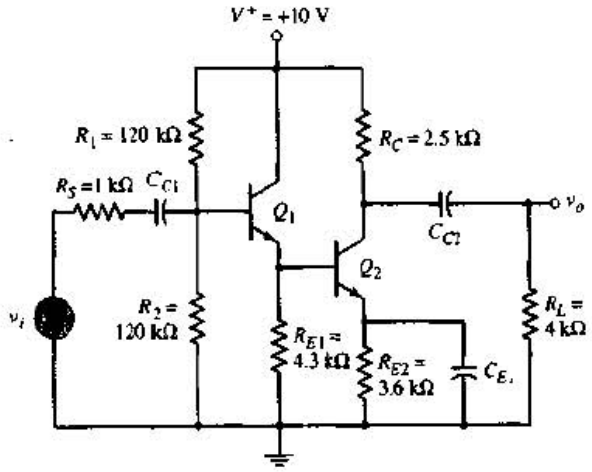


Figure P7.55

***7.56** The transistor circuit in Figure P7.56 is a Darlington pair configuration. Assume $\beta_o = 100$ and $V_A = \infty$ for each transistor, the capacitance values of Q_1 and Q_2 are identical and given by $C_\pi = 24\,\text{pF}$ and $C_\mu = 4\,\text{pF}$. From a PSpice analysis, determine the upper 3 dB frequency and midband voltage gain for: (a) $R_{E1} = 10\,\text{k}\Omega$, (b) $R_{E1} = 40\,\text{k}\Omega$, and (c) $R_{E1} = \infty$. Explain any differences between the results.

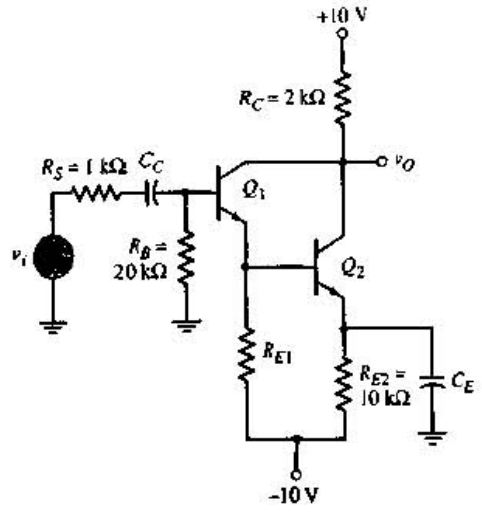
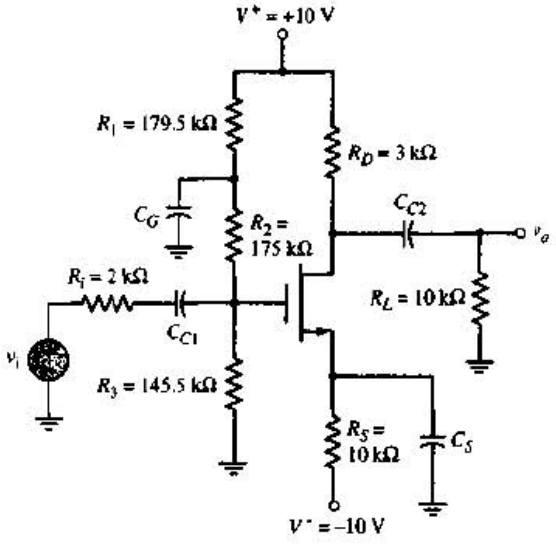


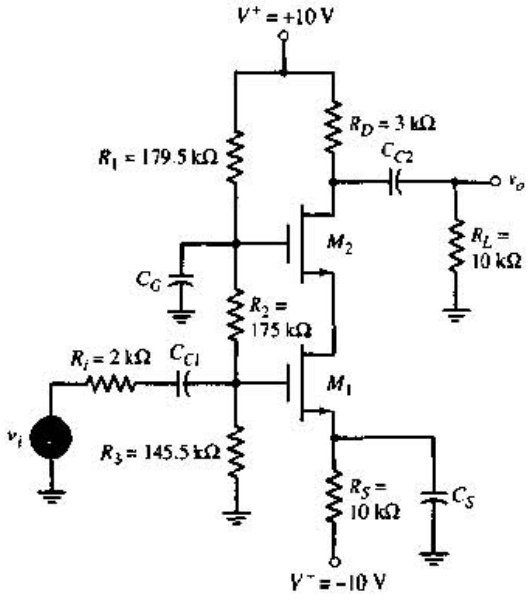
Figure P7.56

***7.57** For the common-source circuit in Figure P7.57(a) and the NMOS cascode circuit in Figure P7.57(b), all transistors have the following identical parameters: $K_n = 1.2\,\text{mA/V}^2$, $V_{TN} = 2\,\text{V}$, $\lambda = 0$, $C_{gs} = 5\,\text{pF}$, and $C_{gd} = 0.8\,\text{pF}$. From a PSpice simulation of each circuit, determine the upper 3 dB frequencies and the midband voltage gains. Compare the 3 dB frequencies and midband voltage gains.



(a)

Figure P7.57(a)



(b)

Figure P7.57(b)

***7.58** For the circuit in Figure P7.58, the transistors are identical, and the parameters are: $K_n = 4\,\text{mA/V}^2$, $V_{TN} = 2\,\text{V}$, $\lambda = 0$, $C_{gs} = 10\,\text{pF}$, and $C_{gd} = 2\,\text{pF}$. The coupling capacitors are all equal at $C_C = 4.7\,\mu\text{F}$. Using a PSpice analysis, determine the lower and upper 3 dB frequencies. What is the bandwidth and midband voltage gain? What value of load capacitance will change the bandwidth by a factor of two?

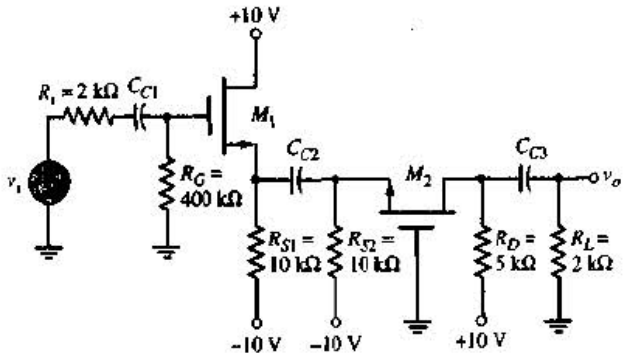


Figure P7.58

DESIGN PROBLEMS

[Note: Each design should be verified with a computer analysis.]

***D7.59** A simplified high-frequency equivalent circuit of an FET amplifier with a source resistor R_S is shown in Figure P7.59. Including the source resistor decreases the small-signal voltage gain. Investigate the amplifier bandwidth as a function of the source resistance to determine the trade-offs required between gain and bandwidth in amplifier designs. (a) Derive an approximate single-pole expression for the voltage gain $A_v(s) = V_o(s)/V_i(s)$, the midband gain, and the upper 3 dB frequency. (b) Assume the circuit parameters are: $R = 1\,\text{k}\Omega$, $R_L = 4\,\text{k}\Omega$, $C_{gs} = 5\,\text{pF}$, $C_{gd} = 1\,\text{pF}$, and $g_m = 2\,\text{mA/V}$. Determine the magnitude of the midband gain and upper 3 dB frequency for $R_S = 0$, 100, 250, and 500 Ω. (c) Plot the gain–bandwidth versus source resistance.

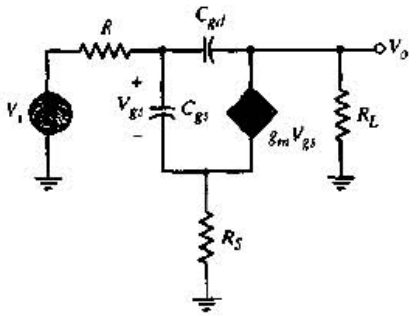


Figure P7.59

***D7.60** (a) Design a common-emitter amplifier using a 2N2222A transistor biased at $I_{CQ} = 1\,\text{mA}$ and $V_{CEQ} = 10\,\text{V}$. The available power supplies are ±15 V, the load resistance is $R_L = 20\,\text{k}\Omega$, the source resistance is $R_S = 0.5\,\text{k}\Omega$, the input and output are ac coupled to the amplifier, and the lower 3 dB frequency is to be less than 10 Hz. Design the circuit to maximize the midband gain. What is the upper 3 dB frequency? (b) Repeat the design for $I_{CQ} = 50\,\mu\text{A}$. Assume f_T is the same as the case when $I_{CQ} = 1\,\text{mA}$. Compare the midband gain and bandwidth of the two designs.

***D7.61** Design a bipolar amplifier with a midband gain of $|A_v| = 50$ and a lower 3 dB frequency of 10 Hz. The available transistors are 2N2222A, and the available power supplies are ±10 V. All transistors in the circuit should be biased at approximately 0.5 mA. The load resistance is $R_L = 5\,\text{k}\Omega$, the source resistance is $R_S = 0.1\,\text{k}\Omega$, and the input and output are ac coupled to the amplifier. Compare the bandwidth of a single-stage design to that of a cascode design.

***D7.62** A common-emitter amplifier is designed to provide a particular midband gain and a particular bandwidth, using device A from Table P7.62. Assume $I_{CQ} = 1\,\text{mA}$. Investigate the effect on midband gain and bandwidth if devices B and C are inserted into the circuit. Which device provides the largest bandwidth? What is the gain-bandwidth product in each case?

Table P7.62 Device specifications for Problem 7.62

Device	f_T (MHz)	C_μ (pF)	β	r_b (Ω)
A	350	2	100	15
B	400	5	100	10
C	500	2	50	5

***D7.63** A simplified high-frequency equivalent circuit of a common-emitter amplifier is shown in Figure P7.63. The input signal is coupled into the amplifier through C_{C1}, the output signal is coupled to the load through C_{C2}, and the amplifier provides a midband gain of $|A_m|$ and an upper 3 dB frequency of f_H. Compare this single-stage amplifier design to one in which three amplifier stages are used between the signal and load. In the three-stage amplifier, assume all parameters are the same, except g_m for each stage is one-third that of the single-stage amplifier. Compare the midband gains and the bandwidths.

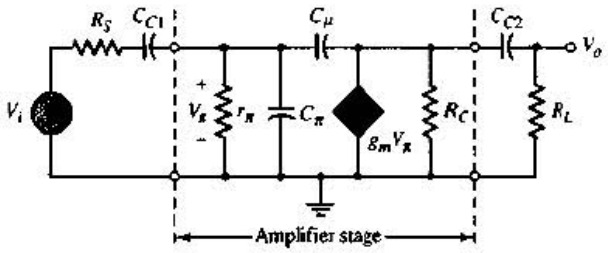


Figure P7.63

CHAPTER

8

Output Stages and Power Amplifiers

8.0 PREVIEW

In previous chapters, we dealt mainly with small-signal voltage gains, current gains, and impedance characteristics. In this chapter, we analyze and design circuits that deliver a specified power to a load. We will, therefore, be concerned with power dissipation in transistors, especially in the output stage since the output stage must deliver the signal power. Linearity in the output signal is still a priority, however. A figure of merit for the output stage linearity characteristic is the total harmonic distortion that is present.

Initially, we will look at the characteristics of power BJTs and MOSFETs. Such characteristics include the current, voltage, and power ratings of these devices, as well as the safe operating area. The heat generated in these transistors from power dissipation must be removed in order to limit the device temperature to a specified maximum rated value. This maximum device temperature is a function of the thermal resistance between the transistor and the ambient and determines the maximum safe operating power of the transistor.

One important aspect in the design of power amplifiers is that it delivers the specified power to the load efficiently. Power amplifiers are classified according to the percent of time the output transistors are conducting. Three principal classes of power amplifiers are analyzed. In our discussion, we will determine the maximum possible conversion efficiency for each type of power amplifier.

An often-used output stage for power amplifiers, called a class-AB circuit, uses complementary pairs of transistors. We will analyze several configurations of this type of output stage, in both BJT and MOSFET configurations. One principal goal of this chapter is that the reader will be able to understand the characteristics of a class AB output stage and design one to meet particular specifications.

8.1 POWER AMPLIFIERS

A multistage amplifier may be required to deliver a large amount of power to a passive load. This power may be in the form of a large current delivered to a relatively small load resistance such as an audio speaker, or may be in the form of a large voltage delivered to a relatively large load resistance such as in a

switching power supply. The output stage of the power amplifier must be designed to meet the power requirements. In this chapter, we are interested only in power amplifiers using BJTs or MOSFETS, and will not consider other types of power electronics that, for example, use thyristors.

Two important functions of the output stage are to provide a low output resistance so that it can deliver the signal power to the load without loss of gain and to maintain linearity in the output signal. A low output resistance implies the use of emitter-follower or source-follower circuit configurations. A measure of the linearity of the output signal is the **total harmonic distortion (THD)**. This figure of merit is the rms value of the harmonic components of the output signal, excluding the fundamental, expressed as a percentage of the fundamental.

A particular concern in the design of the output stage is to deliver the required signal power to the load efficiently. This specification implies that the power dissipated in the transistors of the output stage should be as small as possible. The output transistors must be capable of delivering the required current to the load, and must be capable of sustaining the required output voltage.

We will initially discuss power transistors and will then consider several output stages of power amplifiers.

8.2 POWER TRANSISTORS

In our previous discussions, we have ignored any physical transistor limitations in terms of maximum current, voltage, and power. We implicitly assumed that the transistors were capable of handling the current and voltage, and could handle the power dissipated within the transistor without suffering any damage.

However, since we are now discussing power amplifiers, we must be concerned with transistor limitations. The limitations involve: maximum rated current (on the order of amperes), maximum rated voltage (on the order of 100 V), and maximum rated power (on the order of watts or tens of watts).[1] We will consider these effects in the BJT and then in the MOSFET. The maximum power limitation is related to the maximum allowed temperature of the transistor, which in turn is a function of the rate at which heat is removed. We will therefore briefly consider heat sinks and heat flow.

8.2.1 Power BJTs

Power transistors are large-area devices. Because of differences in geometry and doping concentrations, their properties tend to vary from those of the small-signal devices. Table 8.1 compares the parameters of a general-purpose small-signal BJT to those of two power BJTs. The current gain is generally smaller in the power transistors, typically in the range of 20 to 100, and may be a strong function of collector current and temperature. Figure 8.1 shows typical current gain versus collector current characteristics for the 2N3055 power

[1] We must note that, in general, the maximum rated current and maximum rated voltage cannot occur at the same time.

Table 8.1 Comparison of the characteristics and maximum ratings of a small-signal and power BJT

Parameter	Small-Signal BJT (2N2222A)	Power BJT (2N3055)	Power BJT (2N6078)
V_{CE}(max) (V)	40	60	250
I_C(max) (A)	0.8	15	7
P_D(max) (W) (at $T = 25$°C)	1.2	115	45
β	35–100	5–20	12–70
f_T (MHz)	300	0.8	1

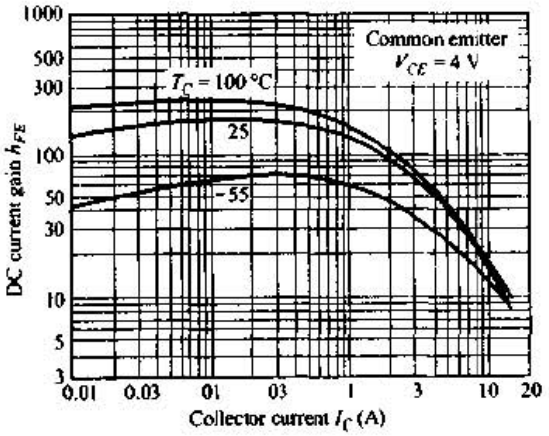


Figure 8.1 Typical dc beta characteristics (h_{FE} versus I_C) for 2N3055

BJT at various temperatures. At high current levels, the current gain tends to drop off significantly, and parasitic resistances in the base and collector regions may become significant, affecting the transistor terminal characteristics.

The **maximum rated collector current** $I_{C,\text{rated}}$ may be related to: the maximum current that the wires connecting the semiconductor to the external terminals can handle; the collector current at which the current gain falls below a minimum specified value; or the current that leads to the maximum power dissipation when the transistor is in saturation.

The maximum voltage limitation in a BJT is generally associated with avalanche breakdown in the reverse-biased base-collector junction. In the common-emitter configuration, the breakdown voltage mechanism also involves the transistor gain, as well as the breakdown phenomenon on the pn junction. Typical I_C versus V_{CE} characteristics are shown in Figure 8.2. The breakdown voltage when the base terminal is open circuited ($I_B = 0$) is V_{CEO}. From the data in Figure 8.2, this value is approximately 130 V.

When the transistor is biased in the active region, the collector current begins to increase significantly before breakdown voltage V_{CEO} is reached, and all the curves tend to merge to the same collector-emitter voltage once breakdown has occurred. The voltage at which these curves merge is denoted $V_{CE(\text{sus})}$ and is the minimum voltage necessary to sustain the transistor in breakdown. From the data in Figure 8.2, the value of $V_{CE(\text{sus})}$ is approximately 115 V.

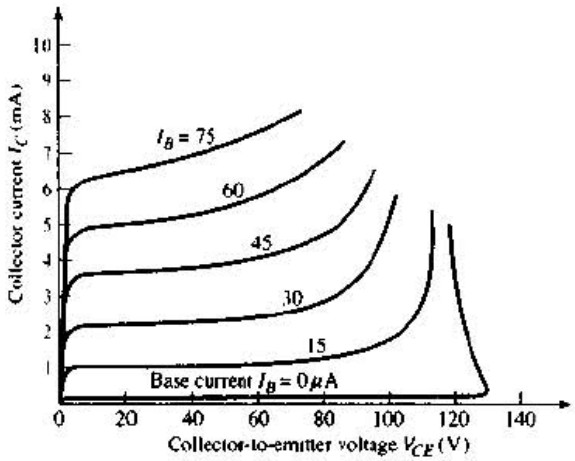


Figure 8.2 Typical collector current versus collector–emitter voltage characteristics of a bipolar transistor, showing breakdown effects

Another breakdown effect is called **second breakdown**, which occurs in a BJT operating at high voltage and a fairly high current. Slight nonuniformities in current density produce local regions of increased heating that decreases the resistance of the semiconductor material, which in turn increases the current in those regions. This effect results in positive feedback, and the current continues to increase, producing a further increase in temperature, until the semiconductor material may actually melt, creating a short circuit between the collector and emitter and producing a permanent failure.

The instantaneous power dissipation in a BJT is given by

$$p_Q = v_{CE}i_C + v_{BE}i_B \tag{8.1}$$

The base current is generally much smaller than the collector current; therefore, to a good approximation, the instantaneous power dissipation is

$$p_Q \cong v_{CE}i_C \tag{8.2}$$

The average power, which is found by integrating Equation (8.2) over one cycle of the signal, is

$$\overline{P}_Q = \frac{1}{T}\int_0^T v_{CE}i_C\,dt \tag{8.3}$$

The average power dissipated in a BJT must be kept below a specified maximum value, to ensure that the temperature of the device remains below a maximum value. If we assume that the collector current and collector–emitter voltage are dc quantities, then at the **maximum rated power** P_T for the transistor, we can write

$$P_T = V_{CE}I_C \tag{8.4}$$

The maximum current, voltage, and power limitations can be illustrated on the I_C versus V_{CE} characteristics, as shown in Figure 8.3. The average power limitation P_T is a hyperbola described by Equation (8.4). The region where the transistor can be operated safely is known as the **safe operating area (SOA)** and is bounded by $I_{C,\max}$, $V_{CE(\text{sus})}$, P_T, and the transistor's second breakdown

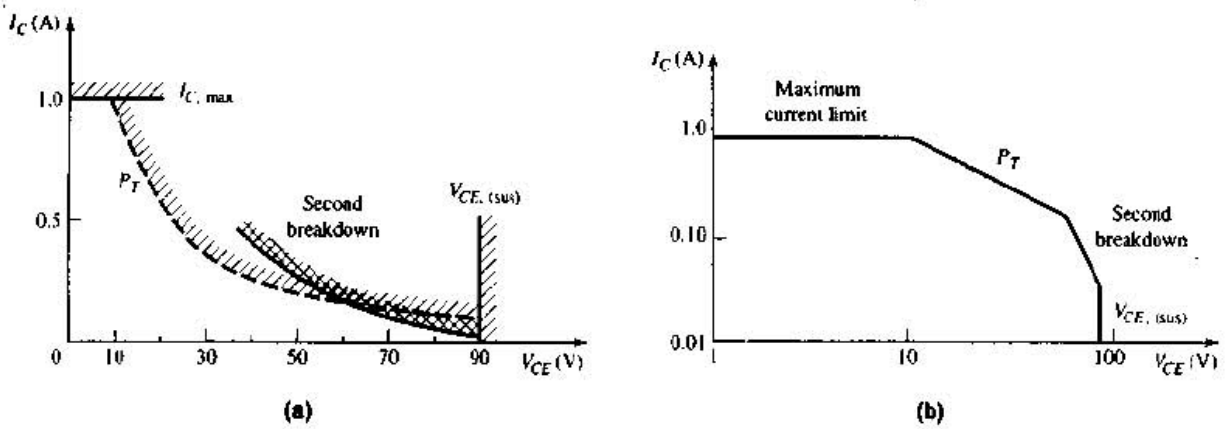


Figure 8.3 The safe operating area of a bipolar transistor plotted on: (a) linear scales and (b) logarithmic scales

characteristics curve. Figure 8.3(a) shows the safe operating area, using linear current and voltage scales; Figure 8.3(b) shows the same characteristics using logarithmic scales.

The i_C—v_{CE} operating point may move momentarily outside the safe operating area without damaging the transistor, but this depends on how far the Q-point moves outside the area and for how long. For our purposes, we will assume that the device must remain within the safe operating area at all times.

Example 8.1 **Objective:** Determine the required current, voltage, and power ratings of a power BJT.

Consider the common-emitter circuit in Figure 8.4. The parameters are $R_L = 8\,\Omega$ and $V_{CC} = 24\,\text{V}$.

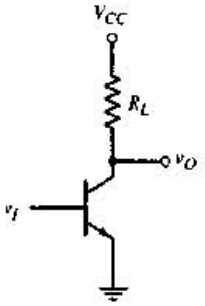


Figure 8.4 Figure for Example 8.1

Solution: For $V_{CE} \approx 0$, the maximum collector current is

$$I_C(\text{max}) = \frac{V_{CC}}{R_L} = \frac{24}{8} = 3\,\text{A}$$

For $I_C = 0$, the maximum collector–emitter voltage is

$$V_{CE}(\text{max}) = V_{CC} = 24\,\text{V}$$

The load line is given by

$$V_{CE} = V_{CC} - I_C R_L$$

and must remain within the safe operating area, as shown in Figure 8.5.

The transistor power dissipation is therefore

$$P_T = V_{CE} I_C = (V_{CC} - I_C R_L) I_C = V_{CC} I_C - I_C^2 R_L$$

The current at which the maximum power occurs is found by setting the derivative of this equation equal to zero as follows:

$$\frac{dP_T}{dI_C} = 0 = V_{CC} - 2 I_C R_L$$

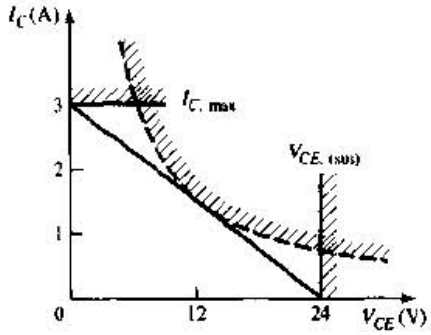


Figure 8.5 DC load line within the safe operating area

which yields

$$I_C = \frac{V_{CC}}{2R_L} = \frac{24}{2(8)} = 1.5\,\text{A}$$

The C–E voltage at the maximum power point is

$$V_{CE} = V_{CC} - I_C R_L = 24 - (1.5)(8) = 12\,\text{V}$$

The maximum power dissipation in the transistor occurs at the center of the load line. The maximum transistor power dissipation is therefore

$$P_T = V_{CE} I_C = 12(1.5) = 18\,\text{W}$$

Comment: To find a transistor for a given application, safety factors are normally used. For this example, a transistor with a current rating greater than 3 A, a voltage rating greater than 24 V, and a power rating greater than 18 W would be required.

Power transistors, which are designed to handle large currents, require large emitter areas to maintain reasonable current densities. These transistors are usually designed with narrow emitter widths to minimize the parasitic base resistance, and may be fabricated as an **interdigitated structure**, as shown in Figure 8.6. Also, emitter ballast resistors, which are small resistors in each emitter leg, are usually incorporated in the design. These resistors help maintain equal currents in each B–E junction.

8.2.2 Power MOSFETs

Table 8.2 lists the basic parameters of two n-channel power MOSFETs. The drain currents are in the ampere range and the breakdown voltages are in the hundreds of volts range. These transistors must also operate within a safe operating area as discussed for the BJTs.

Table 8.2 Characteristics of two power MOSFETs

Parameter	2N6757	2N6792
V_{DS}(max) (V)	150	400
I_D(max) (at $T = 25\,^\circ$C)	8	2
P_D (W)	75	20

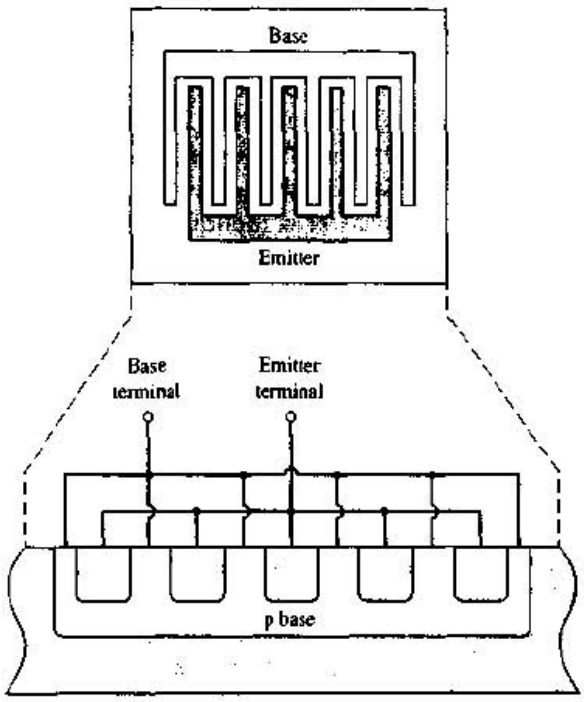


Figure 8.6 An interdigitated bipolar transistor structure showing the top view and cross-sectional view

Power MOSFETs differ from bipolar power transistors both in operating principles and performance. The superior performance characteristics of power MOSFETs are: faster switching times, no second breakdown, and stable gain and response time over a wide temperature range. Figure 8.7(a) shows the transconductance of the 2N6757 versus temperature. The variation with temperature of the MOSFET transconductance is less than the variation in the BJT current gain shown in Figure 8.1.

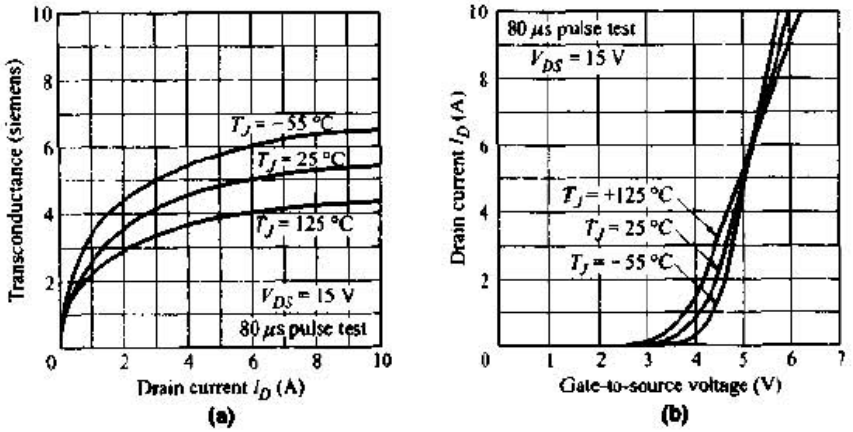


Figure 8.7 Typical characteristics for high-power MOSFETs: (a) transconductance versus drain current; (b) transfer characteristics

Also, since a MOSFET is a high input impedance, voltage-controlled device, the drive circuitry is simpler. The gate of a 10 A power MOSFET may be driven by the output of a standard logic circuit. In contrast, if the current gain of a 10 A BJT is $\beta = 10$, then a base current of 1 A is required for a collector current of 10 A. However, this required input current is much larger than the output drive capability of most logic circuits, which means that the drive circuitry for power BJTs is more complicated.

The MOSFET is a majority carrier device. Majority carrier mobility decreases with increasing temperature, which makes the semiconductor more resistive. This means that MOSFETs are more immune to the thermal runaway effects and second breakdown phenomena experienced in bipolars. Figure 8.7(b) shows typical I_D versus V_{GS} characteristics at several temperatures, clearly demonstrating that at high current levels, the current actually decreases with increasing temperature, for a given gate-to-source voltage.

Power MOSFETs are often manufactured by a vertical or double-diffused process, called VMOS or DMOS, respectively. The cross section of a VMOS device is shown in Figure 8.8(a) and the cross section of the DMOS device is shown in Figure 8.8(b). The DMOS process can be used to produce a large number of closely packed hexagonal cells on a single silicon chip, as shown in Figure 8.8(c). Also, such MOSFETs can be paralleled to form large-area devices, without the need of an equivalent emitter ballast resistance to equalize the current density. A single power MOSFET chip may contain as many as 25,000 paralleled cells.

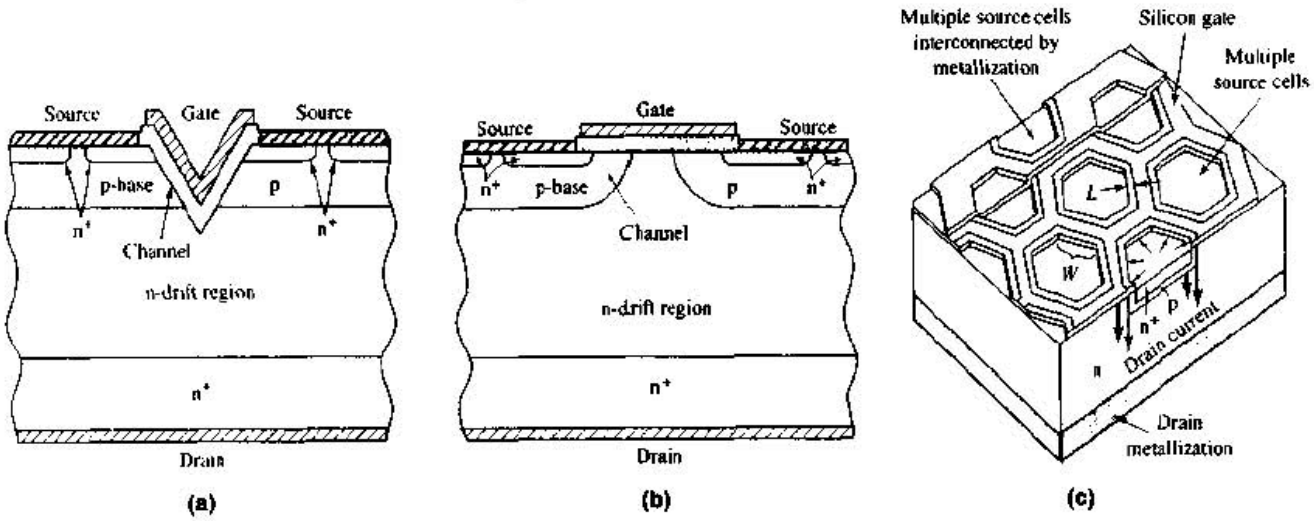


Figure 8.8 (a) Cross section of a VMOS device; (b) cross section of DMOS device; (c) HEXFET structure

Since the path between the drain and the source is essentially resistive, the **on resistance** r_{ds}(on) is an important parameter in the power capability of a MOSFET. Figure 8.9 shows a typical r_{ds}(on) characteristic as a function of drain current. Values in the tens of milliohm range have been obtained.

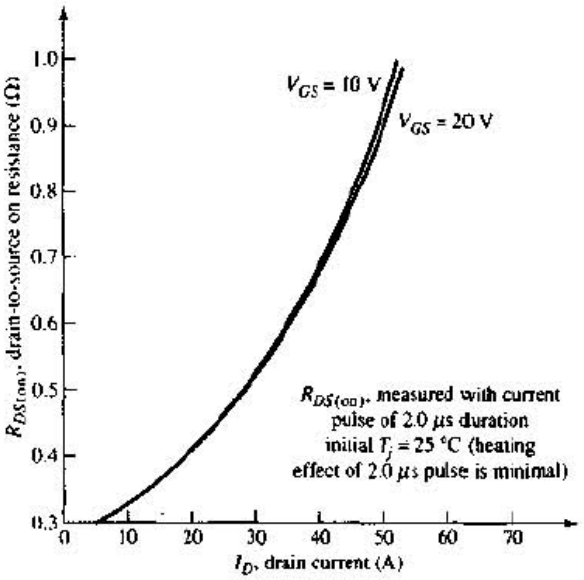


Figure 8.9 Typical drain-to-source resistance versus drain current characteristics of a MOSFET

8.2.3 Heat Sinks

The power dissipated in a transistor increases its internal temperature above the ambient temperature. If the device or junction temperature T_j becomes too high, the transistor may suffer permanent damage. Special precautions must be taken in packaging power transistors and in providing heat sinks so that heat can be conducted from the transistor. Figures 8.10(a) and (b) show two packaging schemes, and Figure 8.10(c) shows a typical heat sink.

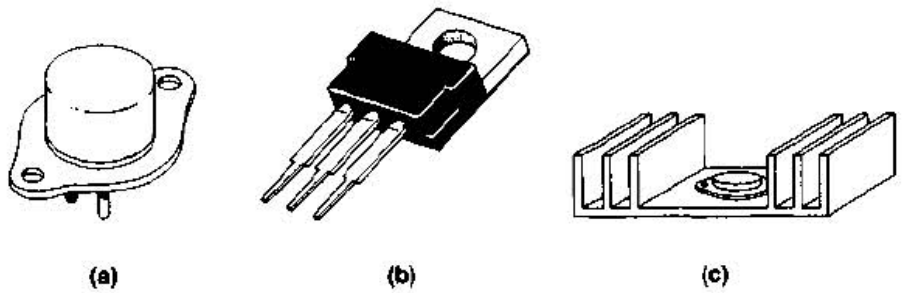


Figure 8.10 Two packaging schemes: (a) and (b) for power transistors and (c) typical heat sink

To design a heat sink for a power transistor, we must first consider the concept of **thermal resistance** θ, which has units of °C/W. The temperature difference, $T_2 - T_1$, across an element with a thermal resistance θ is

$$T_2 - T_1 = P\theta \tag{8.5}$$

where P is the thermal power through the element. Temperature difference is the electrical analog of voltage, and power or heat flow is the electrical analog of current.

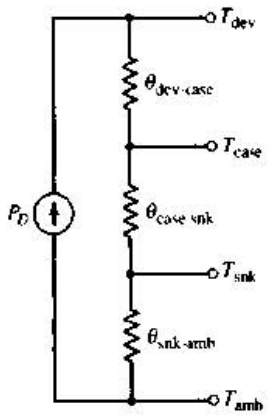


Figure 8.11 Electrical equivalent circuit for heat flow from the device to the ambient

Manufacturers' data sheets for power devices generally give the maximum operating junction or device temperature $T_{j,max}$ and the thermal resistance from the junction to the case $\theta_{jc} = \theta_{dev-case}$.[2] By definition, the thermal resistance between the case and heat sink is $\theta_{case-snk}$, and between the heat sink and ambient is $\theta_{snk-amb}$.

The temperature difference between the device and the ambient can now be written as follows, when a heat sink is used:

$$T_{dev} - T_{amb} = P_D(\theta_{dev-case} + \theta_{case-snk} + \theta_{snk-amb}) \tag{8.6}$$

where P_D is the power dissipated in the device. Equation (8.6) may also be modeled by its equivalent electrical elements, as shown in Figure 8.11. The temperature difference across the elements, such as the case and heat sink, is the dissipated power P_D multiplied by the applicable thermal resistance, which is $\theta_{case-snk}$ for this example.

If a heat sink is not used, the temperature difference between the device and ambient is written as

$$T_{dev} - T_{amb} = P_D(\theta_{dev-case} + \theta_{case-amb}) \tag{8.7}$$

where $\theta_{case-amb}$ is the thermal resistance between the case and ambient.

Example 8.2 **Objective:** Determine the maximum power dissipation in a transistor.

Consider a power MOSFET for which the thermal resistance parameters are:

$$\theta_{dev-case} = 1.75\ ^\circ C/W \qquad \theta_{case-snk} = 1\ ^\circ C/W$$

$$\theta_{snk-amb} = 5\ ^\circ C/W \qquad \theta_{case-amb} = 50\ ^\circ C/W$$

The ambient temperature is $T_{amb} = 30\ ^\circ C$, and the maximum junction or device temperature is $T_{j,max} = T_{dev} = 150\ ^\circ C$.

Solution: When no heat sink is used, the maximum device power dissipation is found from Equation (8.7) as

$$P_{D,max} = \frac{T_{j,max} - T_{amb}}{\theta_{dev-case} + \theta_{case-amb}} = \frac{150 - 30}{1.75 + 50} = 2.32\ W$$

When a heat sink is used, the maximum device power dissipation is found from Equation (8.6) as

$$P_{D,max} = \frac{T_{j,max} - T_{amb}}{\theta_{dev-case} + \theta_{case-snk} + \theta_{snk-amb}}$$
$$= \frac{150 - 30}{1.75 + 1 + 5} = 15.5\ W$$

Comment: These results illustrate that the use of a heat sink allows more power to be dissipated in the device, while keeping the device temperature at or below its maximum limit.

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[2] In this short discussion, we use a more descriptive subscript notation to help clarify the discussion.

The maximum safe power dissipation in a device is a function of: (1) the temperature difference between the junction and case, and (2) the thermal resistance between the device and the case $\theta_{dev-case}$, or

$$P_{D,max} = \frac{T_{j,max} - T_{case}}{\theta_{dev-case}} \tag{8.8}$$

A plot of $P_{D,max}$ versus T_{case}, called the **power derating curve** of the transistor, is shown in Figure 8.12. The temperature at which the power derating curve crosses the horizontal axis corresponds to $T_{j\,max}$. At this temperature, no additional temperature rise in the device can be tolerated; therefore, the allowed power dissipation must be zero, which implies a zero input signal.

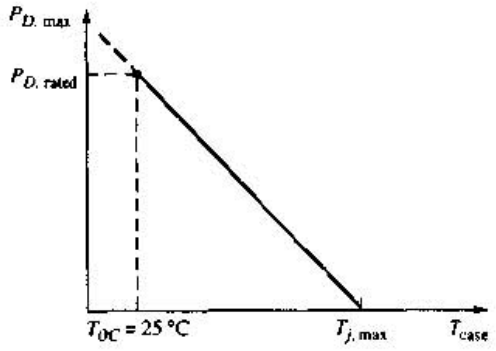

Figure 8.12 A power derating curve

The rated power of a device is generally defined as the power at which the device reaches its maximum temperature, while the case temperature remains at room or ambient temperature, that is, $T_{case} = 25\,°C$. Maintaining the case at ambient temperature implies that the thermal resistance between the case and ambient is zero, or that an infinite heat sink is used. However, with nonzero values of $\theta_{case-snk}$ and $\theta_{snk-amb}$, the case temperature rises above the ambient, and the maximum rated power of the device cannot be achieved. This effect can be seen by examining the equivalent circuit model in Figure 8.11. If the device temperature is at its maximum allowed value of $T_{dev} = T_{j,max}$, then as T_{case} increases, the temperature difference across $\theta_{dev-case}$ decreases, which means that the power through the element must decrease.

Example 8.3 **Objective:** Determine the maximum safe power dissipation in a transistor.

Consider a BJT with a rated power of 20 W and a maximum junction temperature of $T_{j,max} = 175\,°C$. The transistor is mounted on a heat sink with parameters $\theta_{case-snk} = 1\,°C/W$ and $\theta_{snk-amb} = 5\,°C/W$.

Solution: From Equation (8.8), the device-to-case thermal resistance is

$$\theta_{dev-case} = \frac{T_{j,max} - T_{OC}}{P_{D,rated}} = \frac{175 - 25}{20} = 7.5\,°C/W$$

From Equation (8.6), the maximum power dissipation is

$$P_{D,\max} = \frac{T_{j,\max} - T_{amb}}{\theta_{dev-case} + \theta_{case-snk} + \theta_{snk-amb}} = \frac{175 - 25}{7.5 + 1 + 5} = 11.1\,\text{W}$$

Comment: The actual maximum safe power dissipation in a device may be less than the rated value. This occurs when the case temperature cannot be held at the ambient temperature, because of the nonzero thermal resistance factors between the case and ambient.

Test Your Understanding

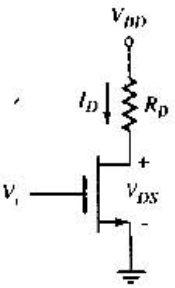

Figure 8.13 Figure for Exercise 8.1 and Example 8.4

8.1 Consider the common-source circuit shown in Figure 8.13. The parameters are $R_D = 20\,\Omega$ and $V_{DD} = 24\,\text{V}$. Determine the required current, voltage, and power ratings of the MOSFET. (Ans. $I_D(\max) = 1.2\,\text{A}$, $V_{DS}(\max) = 24\,\text{V}$, $P_D(\max) = 7.2\,\text{W}$)

8.2 Assume that the BJT in the common-emitter circuit shown in Figure 8.4 has limiting factors of: $I_{C,\max} = 2\,\text{A}$, $V_{CE(sus)} = 50\,\text{V}$, and $P_T = 10\,\text{W}$. Neglecting second breakdown effects, determine the minimum value of R_L such that the Q-point of the transistor always stays within the safe operating area for: (a) $V_{CC} = 30\,\text{V}$, and (b) $V_{CC} = 15\,\text{V}$. In each case, determine the maximum collector current and maximum transistor power dissipation. (Ans. (a) $R_L = 22.5\,\Omega$, $I_{C,\max} = 1.33\,\text{A}$, $P_{Q,\max} = 10\,\text{W}$ (b) $R_L = 7.5\,\Omega$, $I_{C,\max} = 2\,\text{A}$, $P_{Q,\max} = 7.5\,\text{W}$)

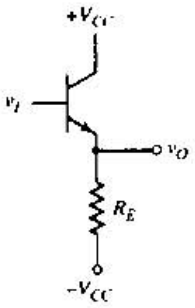

Figure 8.14 Figure for Exercise 8.3

8.3 For the emitter-follower circuit in Figure 8.14, the parameters are $V_{CC} = 10\,\text{V}$ and $R_E = 200\,\Omega$. The transistor current gain is $\beta = 150$, and the current and voltage limitations are $I_{C,\max} = 200\,\text{mA}$ and $V_{CE(sus)} = 50\,\text{V}$. Determine the minimum transistor power rating such that the transistor Q-point is always inside the safe operating area. (Ans. $P_{\max} = 0.5\,\text{W}$)

8.4 A power MOSFET with $\theta_{dev-case} = 3\,^\circ\text{C/W}$ is operating with an average drain current of $\bar{I}_D = 1\,\text{A}$ and an average drain-source voltage of $\bar{V}_{DS} = 12\,\text{V}$. The device is mounted on a heat sink with parameters $\theta_{snk-amb} = 4\,^\circ\text{C/W}$ and $\theta_{case-snk} = 1\,^\circ\text{C/W}$. If the ambient temperature is $T_{amb} = 25\,^\circ\text{C}$, determine the temperature of the: (a) device, (b) case, and (c) heat sink. (Ans. (a) 121 °C (b) 85 °C (c) 73 °C)

8.5 The rated power of a power BJT is $P_{D,rated} = 50\,\text{W}$, the maximum allowed junction temperature is $T_{j,\max} = 200\,^\circ\text{C}$, and the ambient temperature is $T_{amb} = 25\,^\circ\text{C}$. The thermal resistance between the heat sink and air is $\theta_{snk-amb} = 2\,^\circ\text{C/W}$, and that between the case and heat sink is $\theta_{case-snk} = 0.5\,^\circ\text{C/W}$. Find the maximum safe power dissipation and the temperature of the case. (Ans. $P_{D,\max} = 29.2\,\text{W}$, $T_{case} = 98\,^\circ\text{C}$)

8.3 CLASSES OF AMPLIFIERS

Power amplifiers are classified according to the percent of time the output transistors are conducting, or "turned on." The four principal classifications are: class A, class B, class AB, and class C. These classifications are illustrated in Figure 8.15, for a sinusoidal input signal. **In class-A operation,** an output transistor is biased at a quiescent current I_Q and conducts for the entire cycle of the input signal. **For class-B operation,** an output transistor conducts for only

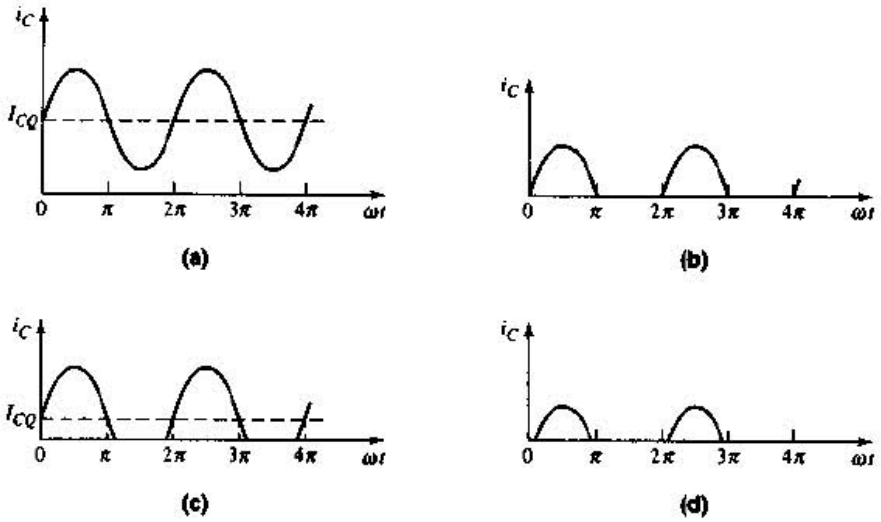

Figure 8.15 Collector current versus time characteristics: (a) class-A amplifier, (b) class-B amplifier, (c) class-AB amplifier, and (d) class-C amplifier

one-half of each sine wave input cycle. In **class-AB operation**, an output transistor is biased at a small quiescent current I_Q and conducts for slightly more than half a cycle. In contrast, in **class-C operation** an output transistor conducts for less than half a cycle. We will analyze the biasing, load lines, and efficiency of each class of power amplifier.

8.3.1 Class-A Operation

The small-signal amplifiers considered in Chapters 4 and 6 were all biased for class-A operation. A basic common-emitter configuration is shown in Figure 8.16(a). The bias circuitry has been omitted, for convenience. Also, in this **standard class-A amplifier** configuration, no inductors or transformers are used.

The dc load line is shown in Figure 8.16(b). The Q-point is assumed to be in the center of the load line, so that $V_{CEQ} = V_{CC}/2$. If a sinusoidal input signal

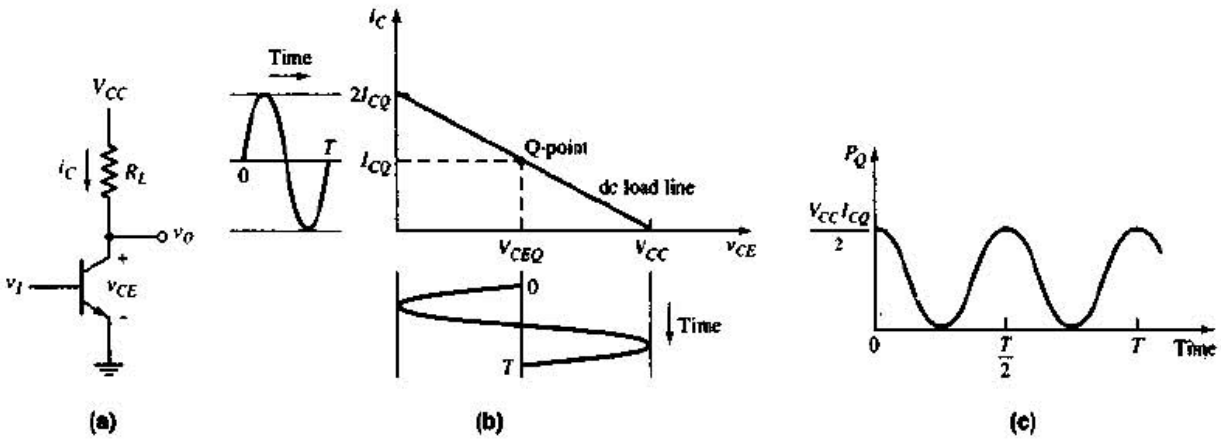

Figure 8.16 (a) Common-emitter amplifier, (b) dc load line, and (c) instantaneous power dissipation versus time in the transistor

is applied, sinusoidal variations are induced in the collector current and collector–emitter voltage. The absolute possible variations are shown in the figure, although values of $v_{CE} = 0$ and $i_C = 2I_{CQ}$ cannot actually be attained.

The instantaneous power dissipation in the transistor, neglecting the base current, is

$$p_Q = v_{CE} i_C \tag{8.9}$$

For a sinusoidal input signal, the collector current and collector-emitter voltage can be written

$$i_C = I_{CQ} + I_p \sin \omega t \tag{8.10(a)}$$

and

$$v_{CE} = \frac{V_{CC}}{2} - V_p \sin \omega t \tag{8.10(b)}$$

If we consider the absolute possible variations, then $I_p = I_{CQ}$ and $V_p = V_{CC}/2$. Therefore, the instantaneous power dissipation in the transistor, from Equation (8.9), is

$$p_Q = \frac{V_{CC} I_{CQ}}{2}(1 - \sin^2 \omega t) \tag{8.11}$$

Figure 8.16(c) is a plot of the instantaneous transistor power dissipation. Since the maximum power dissipation corresponds to the quiescent value (see Figure 8.5), the transistor must be capable of handling a continuous power dissipation of $V_{CC}I_{CQ}/2$ when the input signal is zero.

The **power conversion efficiency** is defined as

$$\eta = \frac{\text{signal load power } (\overline{P}_L)}{\text{supply power}(\overline{P}_S)} \tag{8.12}$$

where $\overline{P}_L$ is the average ac power delivered to the load and $\overline{P}_S$ is the average power supplied by the V_{CC} power source(s). For the standard class-A amplifier and sinusoidal input signals, the average ac power delivered to the load is $(\frac{1}{2})V_p I_p$. Using the absolute possible variations, we have

$$\overline{P}_L(\text{max}) = \left(\frac{1}{2}\right)\left(\frac{V_{CC}}{2}\right)(I_{CQ}) = \frac{V_{CC} I_{CQ}}{4} \tag{8.13}$$

The average power supplied by the V_{CC} source is

$$\overline{P}_S = V_{CC} I_{CQ} \tag{8.14}$$

The maximum attainable conversion efficiency is therefore

$$\eta(\text{max}) = \frac{\frac{1}{4} V_{CC} I_{CQ}}{V_{CC} I_{CQ}} \Rightarrow 25\% \tag{8.15}$$

We must keep in mind that the maximum possible conversion efficiency may change when a load is connected to the output of the amplifier. This efficiency is relatively low; therefore, standard class-A amplifiers are normally not used when signal powers greater than approximately 1 W are required.

Design Pointer: We must emphasize that in practice, a maximum signal voltage of $V_{CC}/2$ and a maximum signal current of I_{CQ} are not possible. The output signal voltage must be limited to smaller values in order to avoid transistor saturation and cutoff, and the resulting nonlinear distortion. The

calculation for the maximum possible efficiency also neglects power dissipation in the bias circuitry. Consequently, the realistic maximum conversion efficiency in a standard class-A amplifier is on the order of 20 percent or less.

Example 8.4 **Objective:** Calculate the actual efficiency of a class-A output stage.

Consider the common-source circuit in Figure 8.13. The circuit parameters are $V_{DD} = 10\,\text{V}$ and $R_D = 5\,\text{k}\Omega$, and the transistor parameters are: $K_n = 1\,\text{mA/V}^2$, $V_{TN} = 1\,\text{V}$, and $\lambda = 0$. Assume the output voltage swing is limited to the range between the transition point and $v_{DS} = 9\,\text{V}$, to minimize nonlinear distortion.

Solution: The load line is given by

$$V_{DS} = V_{DD} - I_D R_D$$

At the transition point, we have

$$V_{DS}(\text{sat}) = V_{GS} - V_{TN}$$

and

$$I_D = K_n(V_{GS} - V_{TN})^2$$

Combining these expressions, the transition point is determined from

$$V_{DS}(\text{sat}) = V_{DD} - K_n R_D V_{DS}^2(\text{sat})$$

or

$$(1)(5)V_{DS}^2(\text{sat}) + V_{DS}(\text{sat}) - 10 = 0$$

which yields

$$V_{DS}(\text{sat}) = 1.32\,\text{V}$$

To obtain the maximum symmetrical swing under the conditions specified, we want the Q-point midway between $V_{DS} = 1.32\,\text{V}$ and $V_{DS} = 9\,\text{V}$, or

$$V_{DSQ} = 5.16\,\text{V}$$

The maximum ac component of voltage across the load resistor is then

$$v_L = 3.84\sin\omega t$$

and the average power delivered to the load is

$$\overline{P}_L = \frac{1}{2}\cdot\frac{(3.84)^2}{5} = 1.47\,\text{mW}$$

The quiescent drain current is found to be

$$I_{DQ} = \frac{10 - 5.16}{5} = 0.968\,\text{mA}$$

The average power supplied by the V_{DD} source is

$$\overline{P}_S = V_{DD}I_{DQ} = (10)(0.968) = 9.68\,\text{mW}$$

and the power conversion efficiency, from Equation (8.12), is

$$\eta = \frac{\overline{P}_L}{\overline{P}_S} = \frac{1.47}{9.68} \Rightarrow 15.2\%$$

Comment: By limiting the swing in the drain–source voltage, to avoid nonsaturation and cutoff and the resulting nonlinear distortion, we reduce the output stage power conversion efficiency considerably, compared to the theoretical maximum possible value of 25 percent for the standard class-A amplifier.

Class-A operation also applies to the emitter-follower, common-base, source-follower, and common-gate configurations. As previously stated, the circuits considered in Figures 8.13 and 8.16(a) are standard class-A amplifiers in that no inductors or transformers are used. Later in this chapter, we will analyze inductively coupled and transformer-coupled power amplifiers that also operate in the class-A mode. We will show that, for these circuits, the maximum conversion efficiency is 50 percent.

Test Your Understanding

8.6 Consider the common-emitter output stage shown in Figure 8.16(a). Let $V_{CC} = 15\,\text{V}$ and $R_L = 1\,\text{k}\Omega$, and assume the Q-point is in the center of the load line. (a) Find the quiescent power dissipated in the transistor. (b) If the sinusoidal output signal is limited to a 13 V peak-to-peak value, determine: the average signal power delivered to the load, the power conversion efficiency, and the average power dissipated in the transistor. (Ans. (a) $P_Q = 56.3\,\text{mW}$ (b) $\overline{P}_L = 21.1\,\text{mW}$, $\eta = 18.7\%$, $\overline{P}_Q = 35.2\,\text{mW}$)

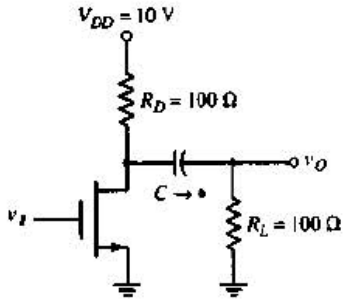

Figure 8.17 Figure for Exercise 8.7

***8.7** For the common-source circuit shown in Figure 8.17, the Q-point is $V_{DSQ} = 4\,\text{V}$. (a) Find I_{DQ}. (b) The minimum value of the instantaneous drain current must be no less than $(\frac{1}{10})I_{DQ}$, and the minimum value of the instantaneous drain-source voltage must be no less than $v_{DS} = 1.5\,\text{V}$. Determine the maximum peak-to-peak amplitude of a symmetrical sinusoidal output voltage. (c) For the conditions of part (b), calculate the power conversion efficiency, where the signal power is the power delivered to R_L. (Ans. (a) $I_{DQ} = 60\,\text{mA}$ (b) $V_{p\text{-}p} = 5.0\,\text{V}$ (c) $\overline{P}_L = 31.25\,\text{mW}$, $\eta = 5.2\%$)

8.3.2 Class-B Operation

Figure 8.18 shows an output stage that consists of a complementary pair of bipolar transistors. When the input voltage is $v_I = 0$, both transistors are cut off and the output voltage is $v_O = 0$. If we assume a B–E cut-in voltage of 0.6 V, then the output voltage v_O remains zero as long as the input voltage is in the range $-0.6 \le v_I \le +0.6\,\text{V}$.

If v_I becomes positive and is greater than 0.6 V, then Q_n turns on and operates as an emitter follower. The load current i_L is positive and is supplied

through Q_n, and the B–E junction of Q_p is reverse biased. If v_I becomes negative by more than 0.6 V, then Q_p turns on and operates as an emitter follower. Transistor Q_p is a sink for the load current, which means that i_L is negative.

This circuit is called a **complementary push–pull** output stage. Transistor Q_n conducts during the positive half of the input cycle, and Q_p conducts during the negative half-cycle. The transistors do not both conduct at the same time.

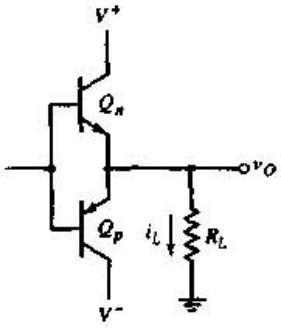

Figure 8.18 Basic complementary push–pull output stage

Crossover Distortion

Figure 8.19 shows the voltage transfer characteristics for this circuit. When either transistor is conducting, the voltage gain, which is the slope of the curve, is essentially unity as a result of the emitter follower. Also, there is a range of input voltage around zero volts where both transistors are cut off and v_O is zero. This portion of the curve is called the **dead band**, and it produces a **crossover distortion**, as illustrated in Figure 8.20, for a sinuosidal input signal. (Crossover distortion can be virtually eliminated by biasing both Q_n and Q_p with a small quiescent collector current when v_I is zero. This techique is discussed in the next section.)

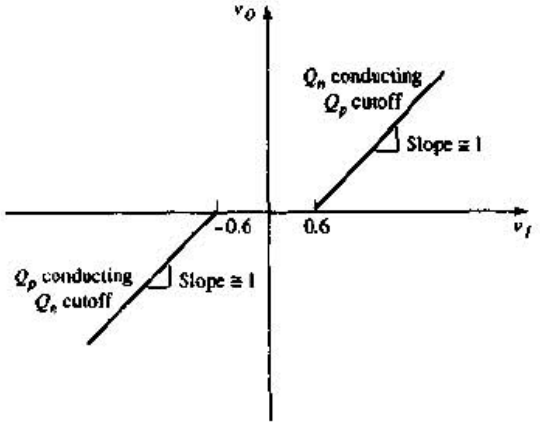

Figure 8.19 Voltage transfer characteristics of basic complementary push–pull output stage

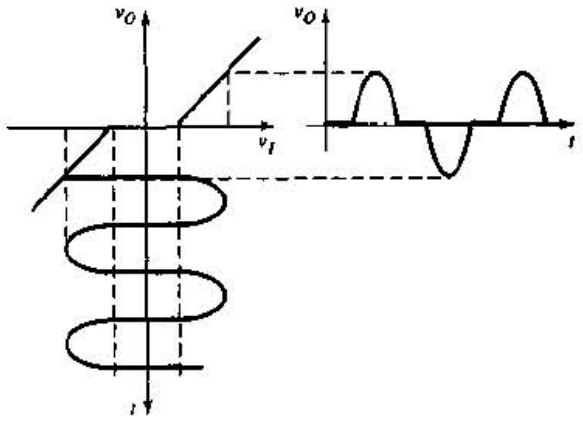

Figure 8.20 Crossover distortion of basic complementary push–pull output stage

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Example 8.5 **Objective:** Determine the total harmonic distortion (THD) of the class B complementary push–pull output stage in Figure 8.18.

A PSpice analysis was performed, which yielded the harmonic content of the output signal.

Solution: A 1 kHz sinusoidal signal with an amplitude of 2 V was applied to the input of the circuit shown in Figure 8.18. The circuit was biased at ±10 V. The transistors used in the circuit were 2N3904 npn and 2N3906 pnp devices. A 1 kΩ load was connected to the output.

The harmonic content for the first nine harmonics is shown in Table 8.3. We see that the output is rich in odd harmonics with the 3 kHz third harmonic being 18 percent as large as the 1 kHz principal output signal. The total harmonic distortion is 19.7 percent, which is large.

Table 8.3 Harmonic content for Example 8.5

Frequency (Hz)	Fourier component	Normalized component	Phase (degrees)
1.000E+03	1.151E+00	1.000E+00	-1.626E-01
2.000E+03	6.313E-03	5.485E-03	-9.322E+01
3.000E+03	2.103E-01	1.827E-01	-1.793E+02
4.000E+03	4.984E-03	4.331E-03	-9.728E+01
5.000E+03	8.064E-02	7.006E-02	-1.792E+02
6.000E+03	3.456E-03	3.003E-03	-9.702E+01
7.000E+03	2.835E-02	2.464E-02	1.770E+02
8.000E+03	2.019E-03	1.754E-03	-8.029E+01
9.000E+03	6.679E-03	5.803E-03	1.472E+02

TOTAL HARMONIC DISTORTION = 1.974899E+01 PERCENT

Comment: These results show the obvious effects of the dead band region. If the input signal amplitude increases, the total harmonic distortion decreases, but if the amplitude decreases, the total harmonic distortion will increase above the 19 percent value.

Power Efficiency

If we consider an idealized version of the circuit in Figure 8.18 in which the base–emitter turn-on voltages are zero, then each transistor would conduct for exactly one-half cycle of the sinusoidal input signal. This circuit would be a class-B output stage, and the output voltage and load current would be replicas of the input signal. The collector–emitter voltages would also show the same sinusoidal variation.

Figure 8.21 illustrates the applicable dc load line. The Q-point is at zero collector current, or at cutoff for both transistors. The quiescent power dissipation in each transistor is then zero.

The output voltage for this idealized class-B output stage can be written

$$v_O = V_p \sin \omega t \tag{8.16}$$

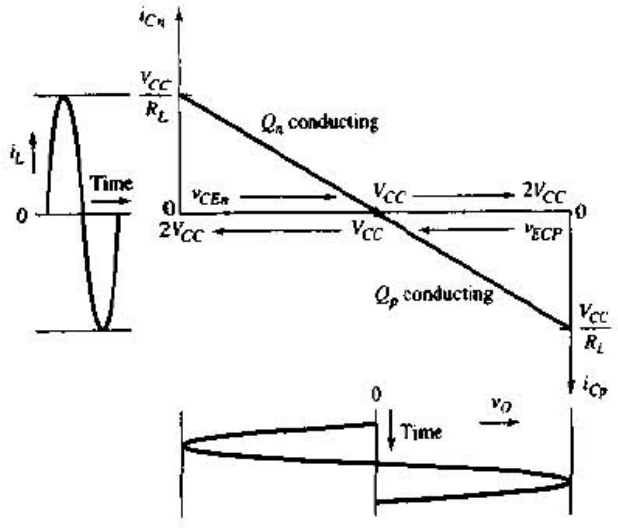

Figure 8.21 Effective load line of the class-B output stage

where the maximum possible value of V_p is V_{CC}.

The instantaneous power dissipation in Q_n is

$$p_{Qn} = v_{CEn} i_{Cn} \tag{8.17}$$

and the collector current is

$$i_{Cn} = \frac{V_p}{R_L} \sin \omega t \tag{8.18(a)}$$

for $0 \leq \omega t \leq \pi$, and

$$i_{Cn} = 0 \tag{8.18(b)}$$

for $\pi \leq \omega t \leq 2\pi$, where V_p is the peak output voltage.

From Figure 8.21, we see that the collector–emitter voltage can be written as

$$v_{CEn} = V_{CC} - V_p \sin \omega t \tag{8.19}$$

Therefore, the total instantaneous power dissipation in Q_n is

$$p_{Qn} = (V_{CC} - V_p \sin \omega t)\left(\frac{V_p}{R_L} \sin \omega t\right) \tag{8.20}$$

for $0 \leq \omega t \leq \pi$, and

$$p_{Qn} = 0$$

for $\pi \leq \omega t \leq 2\pi$. The average power dissipation is therefore

$$\overline{P}_{Qn} = \frac{V_{CC} V_p}{\pi R_L} - \frac{V_p^2}{4R_L} \tag{8.21}$$

The average power dissipation in transistor Q_p is exactly the same as that for Q_n, because of symmetry.

A plot of the average power dissipation in each transistor, as a function of V_p, is shown in Figure 8.22. The power dissipation first increases with increasing output voltage, reaches a maximum, and finally decreases with increasing V_p. We determine the maximum average power dissipation by setting the derivative of $\overline{P}_{Qn}$ with respect to V_p equal to zero, producing

$$\overline{P}_{Qn}(\max) = \frac{V_{CC}^2}{\pi^2 R_L} \tag{8.22}$$

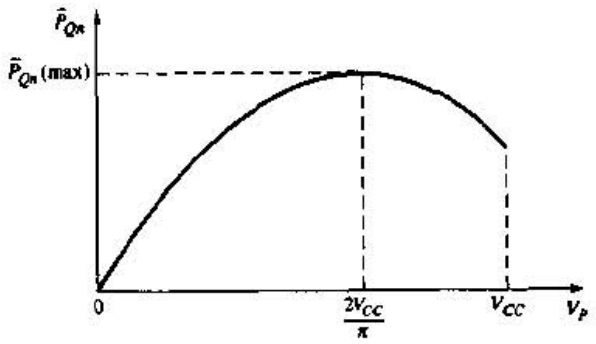

Figure 8.22 Average power dissipation in each transistor versus peak output voltage for class-B output stage

which occurs when

$$V_p|_{\overline{P}_{Q_n}(\max)} = \frac{2V_{CC}}{\pi} \tag{8.23}$$

The average power delivered to the load is

$$\overline{P}_L = \frac{1}{2} \cdot \frac{V_p^2}{R_L} \tag{8.24}$$

Since the current supplied by each power supply is half a sine wave, the average current is $V_p/(\pi R_L)$. The average power supplied by each source is therefore

$$\overline{P}_{S+} = \overline{P}_{S-} = V_{CC}\left(\frac{V_p}{\pi R_L}\right) \tag{8.25}$$

and the total average power supplied by the two sources is

$$\overline{P}_S = 2V_{CC}\left(\frac{V_p}{\pi R_L}\right) \tag{8.26}$$

From Equation (8.12), the conversion efficiency is

$$\eta = \frac{\frac{1}{2} \cdot \frac{V_p^2}{R_L}}{2V_{CC}\left(\frac{V_p}{\pi R_L}\right)} = \frac{\pi}{4} \cdot \frac{V_p}{V_{CC}} \tag{8.27}$$

The maximum possible efficiency, which occurs when $V_p = V_{CC}$, is

$$\eta(\max) = \frac{\pi}{4} \Rightarrow 78.5\% \tag{8.28}$$

This maximum efficiency value is substantially larger than that of the standard class-A amplifier.

From Equation (8.24), we find the maximum possible average power that can be delivered to the load, as follows:

$$\overline{P}_L(\max) = \frac{1}{2} \cdot \frac{V_{CC}^2}{R_L} \tag{8.29}$$

The actual conversion efficiency obtained in practice is less than the maximum value because of other circuit losses, and because the peak output voltage must remain less than V_{CC} to avoid transistor saturation. As the output voltage amplitude increases, output signal distortion also increases. To limit this distortion to an acceptable level, the peak output voltage is usually limited to several volts below V_{CC}. From Figure 8.22 and Equation (8.23), we see that the maximum transistor power dissipation occurs when $V_p = 2V_{CC}/\pi$. At this peak output voltage, the conversion efficiency of the class-B amplifier is, from Equation (8.27),

$$\eta = \frac{\pi}{4V_{CC}} \cdot V_p = \left(\frac{\pi}{4V_{CC}}\right) \cdot \left(\frac{2V_{CC}}{\pi}\right) = \frac{1}{2} \Rightarrow 50\% \tag{8.30}$$

Test Your Understanding

8.8 Design an idealized class-B output stage, as shown in Figure 8.18, to deliver an average of 25 W to an 8 Ω speaker. The peak output voltage must be no larger than 80 percent of supply voltages V_{CC}. Determine: (a) the required value of V_{CC}, (b) the peak current in each transistor, (c) the average power dissipated in each transistor, and (d) the power conversion efficiency. (Ans. (a) $V_{CC} = 25$ V (b) $I_p = 2.5$ A (c) $\overline{P}_Q = 7.4$ W (d) $\eta = 62.8\%$)

8.9 For the idealized class-B output stage shown in Figure 8.18, the parameters are $V_{CC} = 5$ V and $R_L = 100\,\Omega$. The measured output signal is $v_o = 4 \sin \omega t$ (V). Determine: (a) the average signal load power, (b) the peak current in each transistor, (c) the average power dissipated in each transistor, and (d) the power conversion efficiency. (Ans. (a) $\overline{P}_L = 80$ mW (b) $I_p = 40$ mA (c) $\overline{P}_Q = 23.7$ mW (d) $\eta = 62.8\%$)

8.3.3 Class-AB Operation

Crossover distortion can be virtually eliminated by applying a small quiescent bias on each output transistor, for a zero input signal. This is called a class-AB output stage and is shown schematically in the circuit in Figure 8.23. If Q_n and Q_p are matched, then for $v_I = 0$, $V_{BB}/2$ is applied to the B–E junction of Q_n, $V_{BB}/2$ is applied to the E–B junction of Q_p, and $v_O = 0$. The quiescent collector currents in each transistor are given by

$$i_{Cn} = i_{Cp} = I_S e^{V_{BB}/2V_T} \tag{8.31}$$

As v_I increases, the voltage at the base of Q_n increases and v_O increases. Transistor Q_n operates as an emitter follower, supplying the load current to R_L. The output voltage is given by

$$v_O = v_I + \frac{V_{BB}}{2} - v_{BEn} \tag{8.32}$$

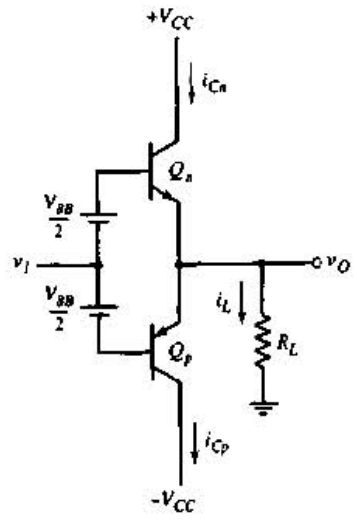

Figure 8.23 Bipolar class-AB output stage

and the collector current of Q_n (neglecting base currents) is

$$i_{Cn} = i_L + i_{Cp} \tag{8.33}$$

Since i_{Cn} must increase to supply the load current, v_{BEn} increases. Assuming V_{BB} remains constant, as v_{BEn} increases, v_{EBp} decreases resulting in a decrease in i_{Cp}.

As v_I goes negative, the voltage at the base of Q_p decreases and v_O decreases. Transistor Q_p operates as an emitter follower, sinking current from the load. As i_{Cp} increases, v_{EBp} increases, causing a decrease in v_{BEn} and i_{Cn}.

Figure 8.24(a) shows the voltage transfer characteristics for this class-AB output stage. If v_{BEn} and v_{EBp} do not change significantly, then the voltage gain, or the slope of the transfer curve, is essentially unity. A sinusoidal input signal voltage and the resulting collector currents and load current are shown in Figures 8.24(b), (c), and (d). Each transistor conducts for more than one-half cycle, which is the definition of class-AB operation.

There is a relationship between i_{Cn} and i_{Cp}. We know that

$$v_{BEn} + v_{EBp} = V_{BB} \tag{8.34(a)}$$

which can be written

$$V_T \ln\left(\frac{i_{Cn}}{I_S}\right) + V_T \ln\left(\frac{i_{Cp}}{I_S}\right) = 2V_T \ln\left(\frac{I_{CQ}}{I_S}\right) \tag{8.34(b)}$$

Combining terms in Equation (8.34(b)), we find

$$i_{Cn} i_{Cp} = I_{CQ}^2 \tag{8.35}$$

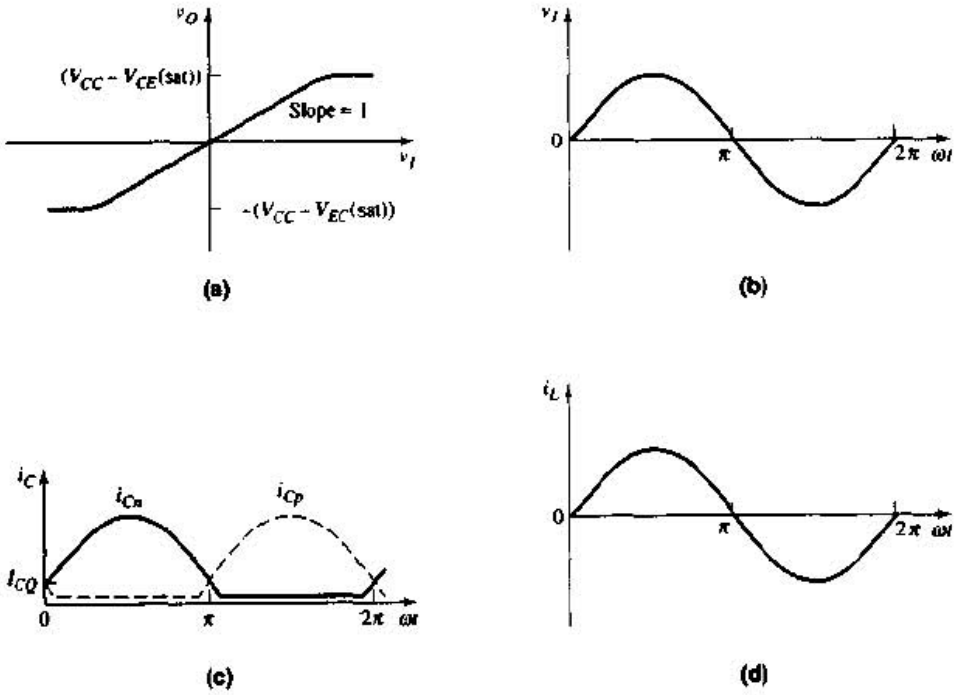

Figure 8.24 Characteristics of a class-AB output stage: (a) voltage transfer curve, (b) sinusoidal input signal, (c) collector currents, and (d) output current

The product of i_{Cn} and i_{Cp} is a cosntant; therefore, if i_{Cn} increases, i_{Cp} decreases, but does not go to zero.

Since, for a zero input signal, quiescent collector currents exist in the output transistors, the average power supplied by each source and the average power dissipated in each transistor are larger than for a class-B configuration. This means that the power conversion efficiency for a class-AB output stage is less than that for an idealized class-B circuit. In addition, the required power handling capability of the transistors in a class-AB circuit must be slightly larger than in a class-B circuit. However, since the quiescent collector currents I_{CQ} are usually small compared to the peak current, this increase in power dissipation is not great. The advantage of eliminating crossover distortion in the class-AB output stage greatly outweighs the slight disadvantage of reduced conversion efficiency and increased power dissipation.

Example 8.6 **Objective:** Determine the total harmonic distortion (THD) of the class AB complementary push–pull output stage shown in Figure 8.23.

A PSpice analysis was performed, which yielded the harmonic content of the output signal.

Solution: A 1 kHz sinusoidal signal with an amplitude of 2 V was applied to the input of the circuit. The bias voltages $V_{BB}/2$ were varied. The circuit was biased at ±10 V and a 1 kΩ load was connected to the output. Shown in Table 8.4 are the $V_{BB}/2$ bias voltages applied, the quiescent transistor currents, and the total harmonic distortion (THD).

Table 8.4 Quiescent collector currents and total harmonic distortion of class-AB circuit

$V_{BB}/2$ (V)	I_{CQ} (mA)	THD (%)
0.60	0.048	1.22
0.65	0.33	0.244
0.70	2.20	0.0068
0.75	13.3	0.0028

Discussion: With a peak input voltage of 2 V and a 1 kΩ load, the peak load current is on the order of 2 mA. From the results shown in Table 8.4, the THD decreases as the ratio of quiescent transistor current to peak load current increases. In other words, for a given input voltage, the smaller the variation in collector current when the signal is applied compared to the quiescent collector current, the smaller the distortion. However, there is a trade-off. As the quiescent transistor current increases, the power efficiency is reduced. The circuit should be designed such that the transistor quiescent current is the smallest value while meeting the maximum total harmonic distortion specification.

Comment: We see that the class-AB output stage results in a much smaller THD value than the class-B circuit, but as with most circuits, there are no uniquely specified bias voltages.

A class-AB output stage using enhancement-mode MOSFETs is shown in Figure 8.25. If M_n and M_p are matched, and if $v_I = 0$, then $V_{BB}/2$ is applied across the gate–source terminals of M_n and the source–gate terminals of M_p. The quiescent drain currents established in each transistor are given by

$$i_{Dn} = i_{Dp} = I_{DQ} = K\left(\frac{V_{BB}}{2} - |V_T|\right)^2 \tag{8.36}$$

As v_I increases, the voltage at the gate of M_n increases and v_O increases. Transistor M_n operates as a source follower, supplying the load current to R_L. Since i_{Dn} must increase to supply the load current, v_{GSn} must also increase. Assuming V_{BB} remains constant, an increase in v_{GSn} implies a decrease in v_{SGp} and a resulting decrease in i_{Dp}. As v_I goes negative, the voltage at the base of M_p decreases and v_O decreases. Transistor M_p then operates as a source follower, sinking current from the load.

Example 8.7 **Objective:** Determine the required biasing in a MOSFET class-AB output stage.

The circuit is shown in Figure 8.25. The parameters are $V_{DD} = 10\,\text{V}$ and $R_L = 20\,\Omega$. The transistors are matched, and the parameters are $K = 0.20\,\text{A/V}^2$ and $|V_T| = 1\,\text{V}$. The quiescent drain current is to be 20 percent of the load current when $v_O = 5\,\text{V}$.

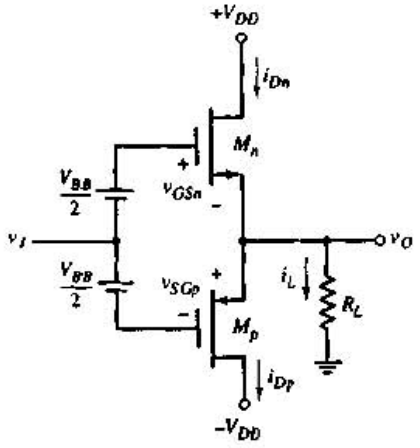

Figure 8.25 MOSFET class-AB output stage

Solution: For $v_O = 5\,\text{V}$,

$$i_L = 5/20 = 0.25\,\text{A}$$

Then, for $I_Q = 0.05\,\text{A}$ when $v_O = 0$, we have

$$I_{DQ} = 0.05 = K\left(\frac{V_{BB}}{2} - |V_T|\right)^2 = (0.20)\left(\frac{V_{BB}}{2} - 1\right)^2$$

which yields

$$V_{BB}/2 = 1.50\,\text{V}$$

The input voltage for v_O positive is

$$v_I = v_O + v_{GSn} - \frac{V_{BB}}{2}$$

For $v_O = 5\,\text{V}$ and $i_{Dn} \cong i_L = 0.25\,\text{A}$, we have

$$v_{GSn} = \sqrt{\frac{i_{Dn}}{K}} + |V_T| = \sqrt{\frac{0.25}{0.20}} + 1 = 2.12\,\text{V}$$

The source-to-gate voltage of M_p is

$$v_{SGp} = V_{BB} - V_{GSn} = 3 - 2.12 = 0.88\,\text{V}$$

which means that M_p is cut off and $i_{Dn} = i_L$. Finally, the input voltage is

$$v_I = 5 + 2.12 - 1.5 = 5.62\,\text{V}$$

Comment: Since $v_I > v_O$, the voltage gain of this output stage is less than unity, as expected.

Voltage V_{BB} can be established in a MOSFET class-AB circuit by using additional enhancement-mode MOSFETs and a constant current I_{Bias}. This will be considered in a problem at the end of the chapter.

Test Your Understanding

***8.10** Consider the MOSFET class-AB output stage shown in Figure 8.25, with the circuit and transistor parameters as given in Example 8.7. Let $V_{BB} = 3.0\,\text{V}$. Determine the small-signal voltage gain $A_v = dv_O/dv_I$ evaluated at: (a) $v_O = 0$, and (b) $v_O = 5.0\,\text{V}$. (Ans. (a) $A_v = 0.889$ (b) $A_v = 0.899$)

8.3.4 Class-C Operation

The transistor circuit ac load line, including an extension beyond cutoff, is shown in Figure 8.26. For class-C operation, the transistor has a reverse-biased B–E voltage at the Q-point. This effect is illustrated in Figure 8.26. Note that

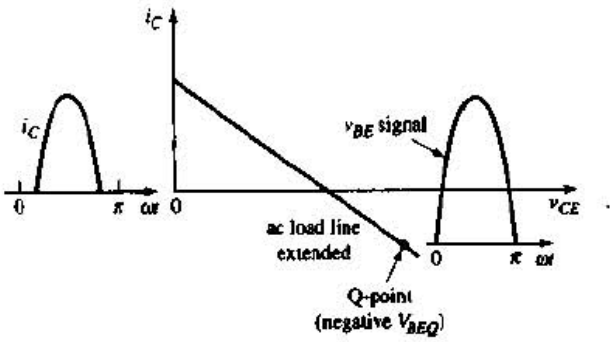

Figure 8.26 Effective ac load line of a class-C amplifier

the collector current is not negative, but is zero at the quiescent point. The transistor conducts only when the input signal becomes sufficiently positive during its positive half-cycle. The transistor therefore conducts for less than a half-cycle, which defines class-C operation.

Class-C amplifiers are capable of providing large amounts of power, with conversion efficiencies larger than 78.5 percent. These amplifiers are normally used for radio-frequency (RF) circuits, with tuned *RLC* loads that are commonly used in radio and television transmitters. The *RLC* circuits convert drive current pulses into sinusoidal signals. Since this is a specialized area, we will not analyze these circuits here.

8.4 CLASS-A POWER AMPLIFIERS

The standard class-A amplifier was analyzed previously, and the maximum possible power conversion efficiency was found to be 25 percent. This conversion efficiency can be increased with the use of inductors and transformers.

8.4.1 Inductively Coupled Amplifier

Delivering a large power to a load generally requires both a large voltage and a high current. In a common-emitter circuit, this requirement can be met by replacing the collector resistor with an inductor, as shown in Figure 8.27(a). The inductor is a short circuit to a dc current, but acts as an open circuit to an ac signal operating at a sufficiently high frequency. The entire ac current is therefore coupled to the load. We assume that $\omega L \gg R_L$ at the lowest signal frequency.

The dc and ac load lines are shown in Figure 8.27(b). We assume that the resistance of the inductor is negligible, and that the emitter resistor value is small. The quiescent collector–emitter voltage is then approximately $V_{CEQ} \cong V_{CC}$. The ac collector current is

$$i_c = \frac{-v_{ce}}{R_L} \tag{8.37}$$

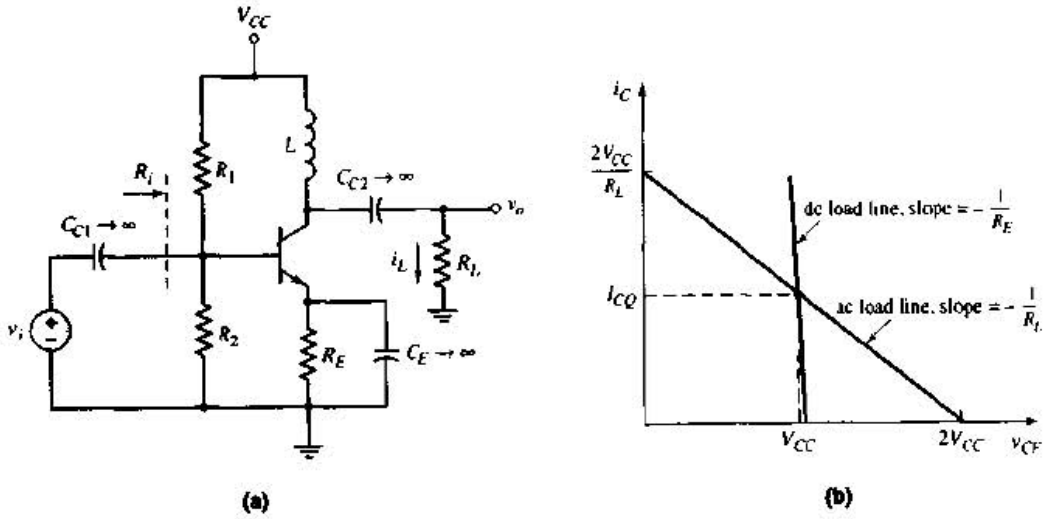

Figure 8.27 (a) Inductively coupled class-A amplifier and (b) dc and ac load lines

To obtain the maximum symmetrical output-signal swing, which will in turn produce the maximum power, we want

$$I_{CQ} \cong \frac{V_{CC}}{R_L} \tag{8.38}$$

For this condition, the ac load line intersects the v_{CE} axis at $2V_{CC}$.

The use of an inductor or storage device results in an output ac voltage swing that is larger than V_{CC}. The polarity of the induced voltage across the inductor may be such that the voltage adds to V_{CC}, producing an output voltage that is larger than V_{CC}.

The absolute maximum amplitude of the signal current in the load is I_{CQ}; therefore, the maximum possible average signal power delivered to the load is

$$\overline{P}_L(\max) = \frac{1}{2} I_{CQ}^2 R_L = \frac{1}{2} \cdot \frac{V_{CC}^2}{R_L} \tag{8.39}$$

If we neglect the power dissipation in the bias resistors R_1 and R_2, the average power supplied by the V_{CC} source is

$$\overline{P}_S = V_{CC} I_{CQ} = \frac{V_{CC}^2}{R_L} \tag{8.40}$$

The maximum possible power conversion efficiency is then

$$\eta(\max) = \frac{\overline{P}_L(\max)}{\overline{P}_S} = \frac{\frac{1}{2} \cdot \frac{V_{CC}^2}{R_L}}{\frac{V_{CC}^2}{R_L}} = \frac{1}{2} \Rightarrow 50\% \tag{8.41}$$

This demonstrates that, in a standard class-A amplifier, replacing the collector resistor with an inductor doubles the maximum possible power conversion efficiency.

8.4.2 Transformer-Coupled Common-Emitter Amplifier

The design of an inductively coupled amplifier to achieve high power conversion efficiency may be difficult, depending on the relationship between the supply voltage V_{CC} and the load resistance R_L. The effective load resistance can be optimized by using a transformer with the proper turns ratio.

Figure 8.28(a) shows a common-emitter amplifier with a transformer-coupled load in the collector circuit.

The dc and ac load lines are shown in Figure 8.28(b). If we neglect any resistance in the transformer and assume that R_E is small, the quiescent collector–emitter voltage is

$$V_{CEQ} \cong V_{CC}$$

The transformed load resistance is

$$R_L' = a^2 R_L \tag{8.42}$$

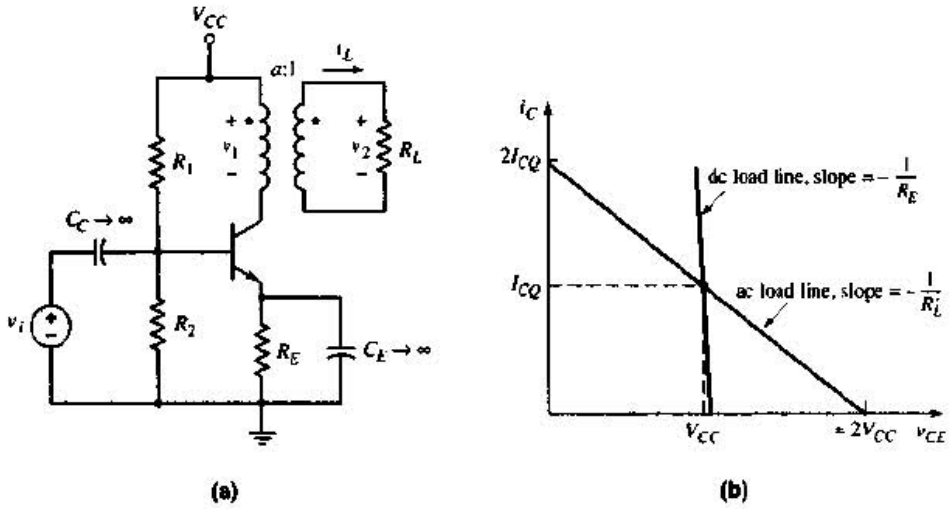

Figure 8.28 (a) Transformer-coupled common-emitter amplifier and (b) dc and ac load lines

where a is the ratio of primary to secondary turns, or simply the turns ratio. The turns ratio is designed to produce the maximum symmetrical swing in the output current and voltage; therefore,

$$R_L' = \frac{2V_{CC}}{2I_{CQ}} = \frac{V_{CC}}{I_{CQ}} = a^2 R_L \tag{8.43}$$

The maximum average power delivered to the load is equal to the maximum average power delivered to the primary of the ideal transformer, as follows:

$$\overline{P}_L(\text{max}) = \frac{1}{2} V_{CC} I_{CQ} \tag{8.44}$$

where V_{CC} and I_{CQ} are the maximum possible amplitudes of the sinusoidal signals. If we neglect the power dissipation in the bias resistors R_1 and R_2, the average power supplied by the V_{CC} source is

$$\overline{P}_S = V_{CC} I_{CQ}$$

and the maximum possible power conversion efficiency is again

$$\eta(\text{max}) = 50\%$$

Test Your Understanding

***D8.11** For the inductively coupled amplifier shown in Figure 8.27(a), the parameters are: $V_{CC} = 12\,\text{V}$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, $R_E = 0.1\,\text{k}\Omega$, $R_L = 1.5\,\text{k}\Omega$, and $\beta = 75$. (a) Design R_1 and R_2 for maximum symmetrical swing in the output current and voltage. (Let $R_{TH} = (1+\beta)R_E$.) (b) If the peak output voltage amplitude is limited to $0.9V_{CC}$, and the peak output current amplitude is limited to $0.9I_{CQ}$, determine the average power delivered to the load, the average power dissipated in the transistor, and the power conversion efficiency. (Ans. (a) $R_1 = 39.1\,\text{k}\Omega$, $R_2 = 9.43\,\text{k}\Omega$ (b) $\overline{P}_L = 38.9\,\text{mW}$, $\overline{P}_Q = 57.1\,\text{mW}$, $\eta = 40.5\%$)

8.4.3 Transformer-Coupled Emitter-Follower Amplifier

Since the emitter follower has a low output impedance, it is often used as the output stage of an amplifier. A transformer-coupled emitter follower is shown in Figure 8.29(a). The dc and ac load lines are shown in Figure 8.29(b). As before, the resistance of the transformer is assumed to be negligible.

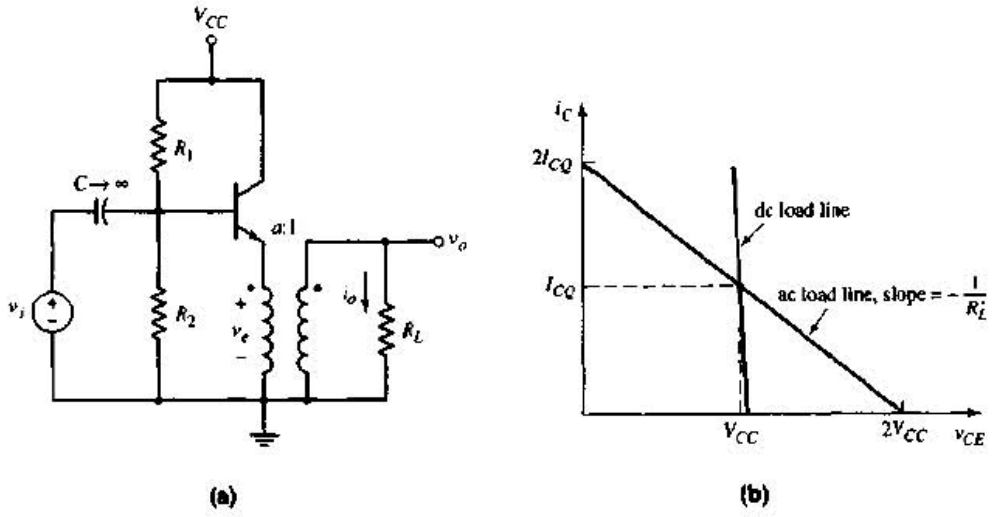

Figure 8.29 (a) Transformer-coupled emitter-follower amplifier and (b) dc and ac load lines

The transformed load resistance is again $R_L' = a^2 R_L$. By correctly designing the turns ratio, we can achieve the maximum symmetrical swing in the output voltage and current.

The average power delivered to the load is

$$\overline{P}_L = \frac{1}{2} \cdot \frac{V_p^2}{R_L} \tag{8.45}$$

where V_p is the peak amplitude of the sinusoidal output voltage. The maximum peak amplitude of the emitter voltage is V_{CC}, so that the maximum peak amplitude of the output signal is

$$V_p(\max) = V_{CC}/a$$

The maximum average output signal power is therefore

$$\overline{P}_L(\max) = \frac{1}{2} \cdot \frac{[V_p(\max)]^2}{R_L} = \frac{V_{CC}^2}{2a^2 R_L} \tag{8.46}$$

The maximum power conversion efficiency for this circuit is also 50 percent.

Design Example 8.8 Objective: Design a transformer-coupled emitter-follower amplifier to deliver a specified signal power.

Consider the circuit shown in Figure 8.29(a), with parameters $V_{CC} = 24\,\text{V}$ and $R_L = 8\,\Omega$. The average power delivered to the load is to be 5 W, the peak amplitude of the signal emitter current is to be no more than $0.9I_{CQ}$, and that of the signal emitter voltage is to be no more than $0.9V_{CC}$. Let $\beta = 100$.

Solution: The average power delivered to the load is given by Equation (8.45). The peak output voltage must therefore be

$$V_p = \sqrt{2R_L\overline{P}_L} = \sqrt{2(8)(5)} = 8.94\,\text{V}$$

and the peak output current is

$$I_p = \frac{V_p}{R_L} = \frac{8.94}{8} = 1.12\,\text{A}$$

Since

$$V_e = 0.9V_{CC} = aV_p$$

then

$$a = \frac{0.9V_{CC}}{V_p} = \frac{(0.9)(24)}{8.94} = 2.42$$

Also, since

$$I_e = 0.9I_{CQ} = I_p/a$$

then

$$I_{CQ} = \frac{1}{0.9}\cdot\frac{I_p}{a} = \frac{1.12}{(0.9)(2.42)} = 0.514\,\text{A}$$

The maximum power dissipated in the transistor, for this class-A operation, is

$$P_Q = V_{CC}I_{CQ} = (24)(0.514) = 12.3\,\text{W}$$

so the transistor must be capable of handling this power.

Bias resistors R_1 and R_2 are found from a dc analysis. The Thevenin equivalent voltage is

$$V_{TH} = I_{BQ}R_{TH} + V_{BE}(\text{on})$$

where

$$R_{TH} = R_1 \| R_2 \qquad \text{and} \qquad V_{TH} = [R_2/(R_1 + R_2)]\cdot V_{CC}$$

We also have

$$I_{BQ} = \frac{I_{CQ}}{\beta} = \frac{0.514}{100} \Rightarrow 5.14\,\text{mA}$$

Since $V_{TH} < V_{CC}$ and $I_{BQ} \approx 5\,\text{mA}$, then R_{TH} cannot be unduly large. However, if R_{TH} is small, then the power dissipation in R_1 and R_2 becomes unacceptably high. We choose $R_{TH} = 2.5\,\text{k}\Omega$, so that

$$V_{TH} = \frac{1}{R_1}(R_{TH})V_{CC} = \frac{1}{R_1}(2.5)(24) = (5.14)(2.5) + 0.7$$

Therefore, $R_1 = 4.43\,\text{k}\Omega$ and $R_2 = 5.74\,\text{k}\Omega$.

Comment: The average power delivered by V_{CC} (neglecting bias resistor effects) is $\overline{P}_S = V_{CC}I_{CQ} = 12.3\,\text{W}$, which means that the power conversion efficiency is $\eta = 5/12.3 \Rightarrow 40.7\%$. The efficiency will always be less than the 50% maximum value, if transistor saturation and distortion are to be minimized.

Test Your Understanding

***D8.12** A transformer-coupled emitter-follower amplifier is shown in Figure 8.29(a). The parameters are: $V_{CC} = 18\,\text{V}$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, $\beta = 100$, $a = 10$, and $R_L = 8\,\Omega$. (a) Design R_1 and R_2 to deliver the maximum power to the load. The input resistance seen by the v_i source is to be $1.5\,\text{k}\Omega$. (b) If the peak amplitude of the emitter voltage v_E is limited to $0.9V_{CC}$, and the peak amplitude of the emitter current i_E is limited to $0.9I_{CQ}$, determine the maximum amplitude of the output signal voltage, and the average power delivered to the load. (Ans. (a) $R_1 = 26.4\,\text{k}\Omega$, $R_2 = 1.62\,\text{k}\Omega$ (b) $V_p = 1.62\,\text{V}$, $I_p = 203\,\text{mA}$, $\overline{P}_L = 0.164\,\text{W}$)

8.5 CLASS-AB PUSH–PULL COMPLEMENTARY OUTPUT STAGES

A class-AB output stage eliminates the crossover distortion that occurs in a class-B circuit. In this section, we will analyze several circuits that provide a small quiescent bias to the output transistors. Such circuits are used as the output stage of power amplifiers, as well as the output stage of operational amplifiers, and will be discussed in Chapter 13.

8.5.1 Class-AB Output Stage with Diode Biasing

In a class-AB circuit, the V_{BB} voltage that provides the quiescent bias for the output transistors can be established by voltage drops across diodes, as shown in Figure 8.30. A constant current I_{Bias} is used to establish the required voltage across the pair of diodes, or the diode-connected transistors, D_1 and D_2. Since D_1 and D_2 are not necessarily matched with Q_n and Q_p, the quiescent transistor currents may not be equal to I_{Bias}.

As the input voltage increases, the output voltage increases, causing an increase in i_{Cn}. This in turn produces an increase in the base current i_{Bn}. Since

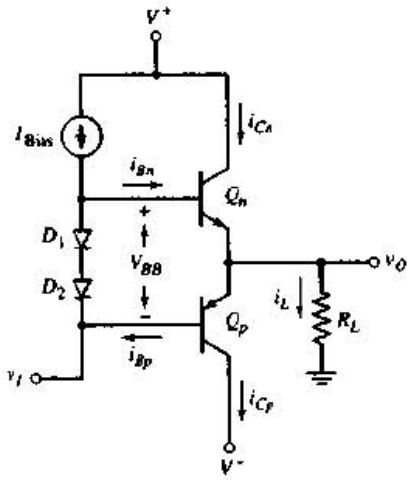

Figure 8.30 Class-AB output stage with quiescent bias established by diodes

the increase base current is supplied by I_{Bias}, the current through D_1 and D_2, and hence the voltage V_{BB}, decreases slightly. Since voltage V_{BB} does not remain constant in this circuit, the relationship between i_{Cn} and i_{Cp}, as given by Equation (8.35), is not precisely valid for this situation. The analysis in the previous section must therefore be modified slightly, but the basic operation of this class-AB circuit is the same.

Design Example 8.9 Objective: Design the class-AB output stage in Figure 8.30 to meet specific design criteria.

Assume $I_{SD} = 3 \times 10^{-14}$ A for D_1 and D_2, $I_{SQ} = 10^{-13}$ A for Q_n and Q_p, and $\beta_n = \beta_p = 75$. Let $R_L = 8\,\Omega$. The average power delivered to the load is to be 5 W. The peak output voltage is to be no more than 80 percent of V_{CC}, and the minimum value of diode current I_D is to be no less than 5 mA.

Solution: The average power delivered to the load, from Equation (8.24), is

$$\overline{P}_L = \frac{1}{2}\cdot\frac{V_p^2}{R_L}$$

Therefore,

$$V_p = \sqrt{2R_L\overline{P}_L} = \sqrt{2(8)(5)} = 8.94\,\text{V}$$

The supply voltages must then be

$$V_{CC} = \frac{V_p}{0.8} = \frac{8.94}{0.8} = 11.2\,\text{V}$$

At this peak output voltage, the emitter current of Q_n is approximately equal to the load current, or

$$i_{En} \cong i_L(\text{max}) = \frac{V_p(\text{max})}{R_L} = \frac{8.94}{8} = 1.12\,\text{A}$$

and the base current is

$$i_{Bn} = \frac{i_{En}}{1+\beta_n} = \frac{1.12}{76} \Rightarrow 14.7\,\text{mA}$$

For a minimum $I_D = 5$ mA, we can choose $I_{Bias} = 20$ mA. For a zero input signal, neglecting base currents, we find that

$$V_{BB} = 2V_T \ln\left(\frac{I_D}{I_{SD}}\right) = 2(0.026)\ln\left(\frac{20\times10^{-3}}{3\times10^{-14}}\right) = 1.416\,\text{V}$$

The quiescent collector currents are then

$$I_{CQ} = I_{SQ}e^{(V_{BB}/2)/V_T} = 10^{-13}e^{1.416/2(0.026)} \Rightarrow 67.0\,\text{mA}$$

For $v_O = 8.94$ V and $i_L = 1.12$ A, the base current is $i_{Bn} = 14.7$ mA, and

$$I_D = I_{Bias} - i_{Bn} = 5.3\,\text{mA}$$

The new value of V_{BB} is then

$$V'_{BB} = 2V_T \ln\left(\frac{I_D}{I_{SD}}\right) = 2(0.026)\ln\left(\frac{5.3\times10^{-3}}{3\times10^{-14}}\right) = 1.347\,\text{V}$$