The B–E voltage of Q_n is

$$v_{BEn} = V_T \ln\left(\frac{i_{Cn}}{I_{SQ}}\right) = (0.026)\ln\left(\frac{1.12}{10^{-13}}\right) = 0.781\,\text{V}$$

The emitter-base voltage of Q_p is then

$$v_{EBp} = V'_{BB} - v_{BEn} = 1.347 - 0.781 = 0.566\,\text{V}$$

and

$$i_{Cp} = I_{SQ}e^{v_{EBp}/V_T} = (10^{-13})e^{0.566/0.026} \Rightarrow 0.285\,\text{mA}$$

Comment: When the output goes positive, the current in Q_p decreases significantly, as expected, but it does not go to zero. There is a factor of approximately 10^3 difference in the currents between Q_n and Q_p.

Design Pointer: If the output signal currents are large, the base currents in the output transistors may become significant compared to the bias current through the diodes D_1 and D_2. The change in the diode bias current should be minimized in order to keep the small-signal voltage gain of the output stage close to unity.

Test Your Understanding

***8.13** Consider the class-AB output stage in Figure 8.30. The circuit is biased with $V^+ = 12\,\text{V}$, $V^- = -12\,\text{V}$, and the load resistance is $R_L = 75\,\Omega$. The device parameters are: $I_{SD} = 5 \times 10^{-13}\,\text{A}$ for D_1 and D_2, and $I_{SQ} = 2 \times 10^{-13}\,\text{A}$ for Q_n and Q_p. (a) Neglecting base currents, determine the required value of I_{Bias} such that the quiescent currents in Q_n and Q_p are $I_{CQ} = 5\,\text{mA}$. (b) Assuming $\beta_n = \beta_p = 60$, determine i_{Cn}, i_{Cp}, v_{BEn}, v_{EBp}, and I_D when $v_O = 2\,\text{V}$. (c) Repeat part (b) for $v_O = 10\,\text{V}$. (Ans. (a) $I_{\text{Bias}} = 12.5\,\text{mA}$ (b) $i_{Cn} = 27.1\,\text{mA}$, $I_D = 12.05\,\text{mA}$, $v_{BEn} = 0.6664\,\text{V}$, $v_{EBp} = 0.5766\,\text{V}$, $i_{Cp} = 0.856\,\text{mA}$ (c) $i_{Cn} = 131\,\text{mA}$, $I_D = 10.3\,\text{mA}$, $v_{BEn} = 0.7074\,\text{V}$, $v_{EBp} = 0.5276\,\text{V}$, $i_{Cp} = 0.130\,\text{mA}$)

8.5.2 Class-AB Biasing Using the V_{BE} Multiplier

An alternative biasing scheme, which provides more flexibility in the design of the output stage, is shown in Figure 8.31. The bias circuit that provides voltage V_{BB} consists of transistor Q_1 and resistors R_1 and R_2, biased by a constant-current source I_{Bias}.

If we neglect the base current in Q_1, then

$$I_R = \frac{V_{BE1}}{R_2} \tag{8.47}$$

and voltage V_{BB} is

$$V_{BB} = I_R(R_1 + R_2) = V_{BE1}\left(1 + \frac{R_1}{R_2}\right) \tag{8.48}$$

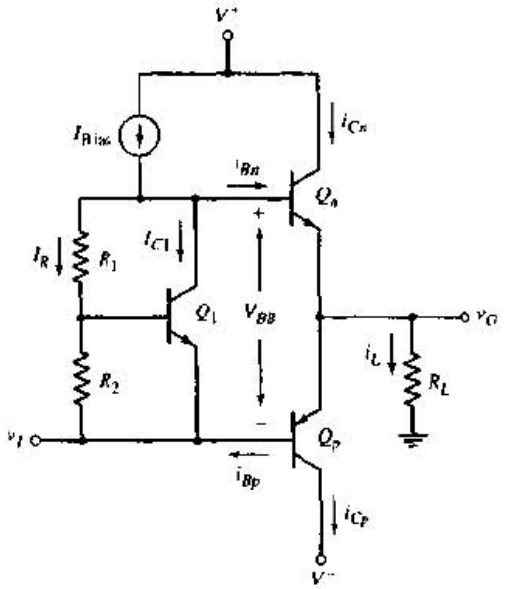

Figure 8.31 Class-AB output stage with V_{BE} multiplier bias circuit

Since voltage V_{BB} is a multiplication of the junction voltage V_{BE1}, the circuit is called a V_{BE} **multiplier**. The multiplication factor can be designed to yield the required value of V_{BB}.

A fraction of the constant current I_{Bias} flows through Q_1, so that

$$V_{BE1} = V_T \ln\left(\frac{I_{C1}}{I_{S1}}\right) \tag{8.49}$$

Also, the quiescent bias currents i_{Cn} and i_{Cp} are normally small; therefore, we can neglect i_{Bn} and i_{Bp}. Current I_{Bias} divides between I_R and I_{C1}, satisfying both Equations (8.47) and (8.49).

As v_I increases, v_O becomes positive, and i_{Cn} and i_{Bn} increase, which reduces the collector current in Q_1. However, the logarithmic dependence of I_{C1}, shown in Equation (8.49), means that V_{BE1} and, in turn V_{BB} remain essentially constant as the output voltage changes.

Design Example 8.10 Objective: Design a Class-AB output stage using the V_{BE} multiplier circuit to meet a specified total harmonic distortion.

Assume the circuit in Figure 8.31, biased at $V^+ = 15\,\text{V}$ and $V^- = -15\,\text{V}$, is the output stage of an audio amplifier that is to drive another power amplifier whose input resistance is $1\,\text{k}\Omega$. The maximum peak sinusoidal output voltage is to be 10 V and the total harmonic distortion is to be less than 0.1 percent.

Solution: Standard 2N3904 and 2N3906 transistors are to be used. From the results of Example 8.6, the THD is a function of the output transistor quiescent currents. For the basic circuit in Figure 8.23, the THD is found to be 0.097 percent for $V_{BB} = 1.346\,\text{V}$, quiescent collector currents of 0.88 mA, and a peak sinusoidal output voltage of 10 V.

Figure 8.32 is the PSpice circuit schematic. For a peak output voltage of 10 V, the peak load current is 10 mA. Assuming $\beta \cong 100$, the peak base current is 0.1 mA. A bias current of 1 mA is chosen to bias the V_{BE} multiplier. The peak 0.1 mA base current, then, will not greatly disturb the current through the multiplier circuit.

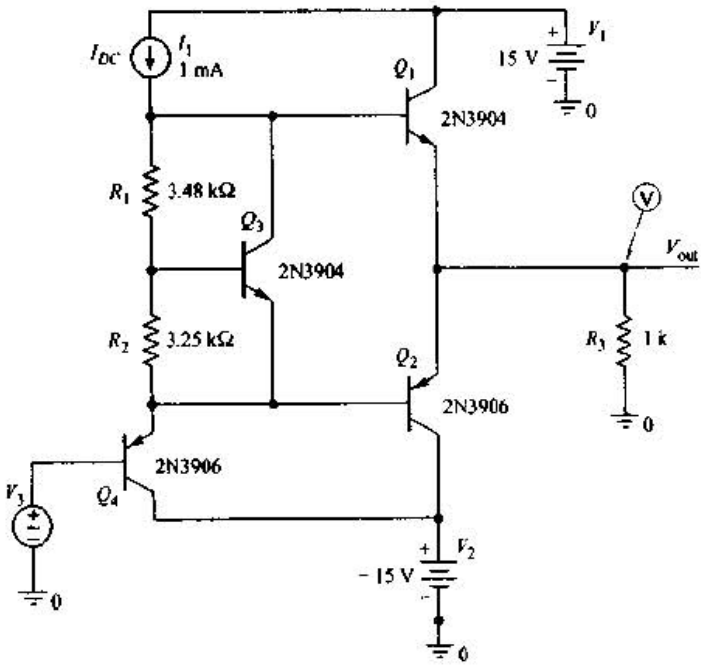

Figure 8.32 PSpice circuit schematic for Example 8.10

We may select $I_R = 0.2$ mA (current through R_1 and R_2) and $I_{C3} = 0.8$ mA. We then have

$$R_1 + R_2 = \frac{V_{BB}}{I_R} = \frac{1.346}{0.2} = 6.73\,\text{k}\Omega$$

For the 2N3904, we find that $V_{BE} \cong 0.65$ V for a quiescent collector current of approximately 0.8 mA. Therefore

$$R_2 = \frac{V_{BE3}}{I_R} = \frac{0.65}{0.2} = 3.25\,\text{k}\Omega$$

so that $R_1 = 3.48\,\text{k}\Omega$.

From the PSpice results, we find that the voltage at the base of Q_1 to be 0.6895 V and the voltage at the base of Q_2 to be −0.6961 V, which means that $V_{BB} = 1.3856$ V. This voltage is slightly greater than the design value of $V_{BB} = 1.346$ V. Listed below are the quiescent transistor parameters. The quiescent collector currents of the output transistors are 1.88 mA, approximately twice the design value of 0.88 mA. The total harmonic distortion is 0.0356 percent, which is well within the design specification.

NAME	Q_Q1	Q_Q2	Q_Q3	Q_Q4
MODEL	Q2N3904	Q2N3906	Q2N3904	Q2N3906
IB	1.12E-05	-5.96E-06	6.01E-06	-3.20E-06
IC	1.88E-03	-1.88E-03	7.80E-04	-9.92E-04
VBE	6.78E-01	-7.08E-01	6.59E-01	-6.92E-01
VBC	-1.43E+01	1.43E+01	-7.27E-01	1.36E+01
VCE	1.50E+01	-1.50E+01	1.39E+00	-1.43E+01
BETADC	1.67E+02	3.15E+02	1.30E+02	3.10E+02
GM	7.11E-02	7.15E-02	2.98E-02	3.80E-02
RPI	2.66E+03	4.34E+03	5.01E+03	8.09E+03

Comment: Since the resulting V_{BB} voltage is slightly larger than the design value, the quiescent output transistor currents are approximately double the design value. Although the THD specification is met, the larger collector currents mean a larger quiescent power dissipation. For this reason, the circuit may need to be redesigned slightly to lower the quiescent currents.

8.5.3 Class-AB Output Stage with Input Buffer Transistors

The output stage in Figure 8.33 is a class-AB configuration composed of the complementary transistor pair Q_3 and Q_4. Resistors R_1 and R_2 and the emitter-follower transistors Q_1 and Q_2 establish the quiescent bias required in this configuration. Resistors R_3 and R_4, used in conjunction with short-circuit protection devices not shown in the figure, also provide thermal stability for the output transistors. The input signal v_I may be the output of a low-power

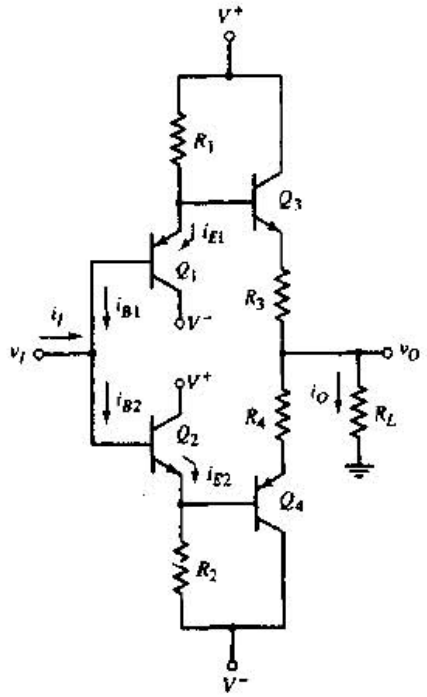

Figure 8.33 Class-AB output stage with input buffer transistors

amplifier. Also, since this is an emitter follower, the output voltage is approximately equal to the input voltage.

When the input voltage v_I increases from zero, the base voltage of Q_3 increases, and the output voltage v_O increases. The load current i_O is positive, and the emitter current in Q_3 increases to supply the load current, which causes an increase in the base current into Q_3. Since the base voltage of Q_3 increases, the voltage drop across R_1 decreases, resulting in a smaller current in R_1. This means that i_{E1} and i_{B1} also decrease. As v_I increases, the voltage across R_2 increases, and i_{E2} and i_{B2} increase. A net input current i_I is then produced, to account for the reduction in i_{B1} and the increase in i_{B2}.

The net input current is

$$i_I = i_{B2} - i_{B1} \tag{8.50}$$

Neglecting the voltage drops across R_3 and R_4 and the base currents in Q_3 and Q_4, we have

$$i_{B2} = \frac{(v_I - V_{BE}) - V^-}{(1 + \beta_n)R_2} \tag{8.51(a)}$$

and

$$i_{B1} = \frac{V^+ - (v_I + V_{EB})}{(1 + \beta_p)R_1} \tag{8.51(b)}$$

where β_n and β_p are the current gains of the npn and pnp transistors, respectively. If $V^+ = -V^-$, $V_{BE} = V_{EB}$, $R_1 = R_2 \equiv R$, and $\beta_n = \beta_p \equiv \beta$, then combining Equations (8.51(a)), (8.51(b)), and (8.50) produces

$$i_I = \frac{(v_I - V_{BE} - V^-)}{(1 + \beta)R} - \frac{(V^+ - v_I - V_{EB})}{(1 + \beta)R} = \frac{2v_I}{(1 + \beta)R} \tag{8.52}$$

Since the voltage gain of this output stage is approximately unity, the output current is

$$i_O = \frac{v_O}{R_L} \cong \frac{v_I}{R_L} \tag{8.53}$$

Using Equations (8.52) and (8.53), we find the current gain of this output stage to be

$$A_i = \frac{i_O}{i_I} = \frac{(1 + \beta)R}{2R_L} \tag{8.54}$$

With β in the numerator, this current gain should be substantial. A large current gain is desirable, since the output stage of power amplifiers must provide the current necessary to meet the power requirements.

Example 8.11 **Objective:** Determine the currents and the current gain for the output stage with input buffer transistors.

For the circuit in Figure 8.33, the parameters are: $R_1 = R_2 = 2\,\text{k}\Omega$, $R_L = 100\,\Omega$, $R_3 = R_4 = 0$, and $V^+ = -V^- = 15\,\text{V}$. Assume all transistors are matched, with $\beta = 60$ and $V_{BE}(\text{npn}) = V_{EB}(\text{pnp}) = 0.6\,\text{V}$.

Solution: For $v_I = 0$,

$$i_{R1} = i_{R2} \cong i_{E1} = i_{E2} = \frac{15 - 0.6}{2} = 7.2\,\text{mA}$$

Assuming all transistors are matched, the bias currents in Q_3 and Q_4 are also approximately 7.2 mA, since the base–emitter voltages of Q_1 and Q_3 are equal and those of Q_2 and Q_4 are equal.

Solution: For $v_I = 10\,\text{V}$, the output current is approximately

$$i_O = \frac{v_O}{R_L} \cong \frac{10}{0.1} = 100\,\text{mA}$$

The emitter current in Q_3 is essentially equal to the load current, which means that the base current in Q_3 is approximately

$$i_{B3} = 100/61 = 1.64\,\text{mA}$$

The current in R_1 is

$$i_{R1} = \frac{15 - (10 + 0.6)}{2} = 2.2\,\text{mA}$$

which means that

$$i_{E1} = i_{R1} - i_{B3} = 0.56\,\text{mA}$$

and

$$i_{B1} = i_{E1}/(1 + \beta) = 0.56/61 \Rightarrow 9.18\,\mu\text{A}$$

Since Q_4 tends to turn off when v_O increases, we have

$$i_{E2} \cong i_{R2} = \frac{10 - 0.6 - (-15)}{2} = 12.2\,\text{mA}$$

and

$$i_{B2} = i_{E2}/(1 + \beta) = 12.2/61 \Rightarrow 200\,\mu\text{A}$$

The input current is then

$$i_I = i_{B2} - i_{B1} = 200 - 9.18 \cong 191\,\mu\text{A}$$

The current gain is then

$$A_i = \frac{i_O}{i_I} = \frac{100}{0.191} = 524$$

From Equation (8.54), the predicted current gain is

$$A_i = \frac{i_O}{i_I} = \frac{(1 + \beta)R}{2R_L} = \frac{(61)(2)}{2(0.1)} = 610$$

Comment: Since the current gain determined from Equation (8.54) neglects base currents in Q_3 and Q_4, the actual current gain is less than the predicted value, as expected. The input current of 191 μA can easily be supplied by a low-power amplifier.

Test Your Understanding

***8.14** Consider the class-AB output stage in Figure 8.33. The parameters are: $V^+ = -V^- = 12\,\text{V}$, $R_1 = R_2 = 250\,\Omega$, $R_L = 8\,\Omega$, and $R_3 = R_4 = 0$. Assume all transistors are matched, with $\beta = 40$ and $V_{BE}(\text{npn}) = V_{EB}(\text{pnp}) = 0.7\,\text{V}$. (a) For $v_I = 0$, determine i_{E1}, i_{E2}, i_{B1}, and i_{B2}. (b) For $v_I = 5\,\text{V}$, find i_O, i_{E1}, i_{E2}, i_{B1}, i_{B2}, and i_I. (c) Using the

results of part (b), determine the current gain of the output stage. Compare this value to that found using Equation (8.54). (Ans. (a) $i_{E1} = i_{E2} = 44.1\,\text{mA}$, $i_{B1} = i_{B2} = 1.08\,\text{mA}$ (b) $i_O = 0.625\,\text{A}$, $i_{E1} = 10.0\,\text{mA}$, $i_{B1} = 0.244\,\text{mA}$, $i_{E2} = 65.2\,\text{mA}$, $i_{B2} = 1.59\,\text{mA}$, $i_I = 1.35\,\text{mA}$ (c) $A_i = 463$, from Equation (8.54) $A_i = 641$)

8.5.4 Class-AB Output Stage Utilizing the Darlington Configuration

The complementary push–pull output stage uses npn and pnp bipolar transistors. Usually in IC design, the pnp transistors are fabricated as lateral devices with low β values that are typically in the range of 5 to 10, and the npn transistors are fabricated as vertical devices with β values on the order of 200. This means that the npn and pnp transistors are not well matched, as we have assumed in our analyses.

Consider the two-transistor configuration shown in Figure 8.34(a). Assume the transistor current gains are β_n and β_p for the npn and pnp transistors, respectively. We can write

$$i_{Cp} = i_{Bn} = \beta_p i_{Bp} \tag{8.55}$$

and

$$i_2 = (1 + \beta_n) i_{Bn} = (1 + \beta_n)\beta_p i_{Bp} \cong \beta_n \beta_p i_{Bp} \tag{8.56}$$

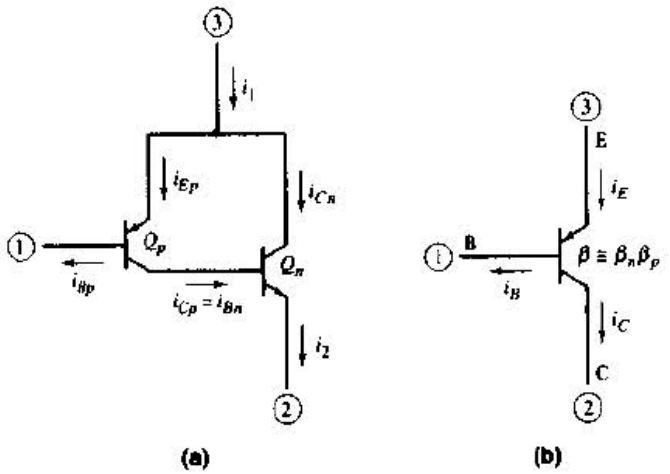

Figure 8.34 (a) A two-transistor configuration of an equivalent pnp transistor; (b) the equivalent pnp transistor

Terminal 1 acts as the base of the composite three-terminal device, terminal 2 acts as the collector, and terminal 3 is the emitter. The current gain of the device is then approximately $\beta_n \beta_p$. The equivalent circuit is shown in Figure 8.34(b). We can use the two-transistor configuration in Figure 8.34(a) as a single equivalent pnp transistor with a current gain on the same order of magnitude as that of an npn device.

In Figure 8.35, the output stage uses Darlington pairs to provide the necessary current gain. Transistors Q_1 and Q_2 constitute the npn Darlington

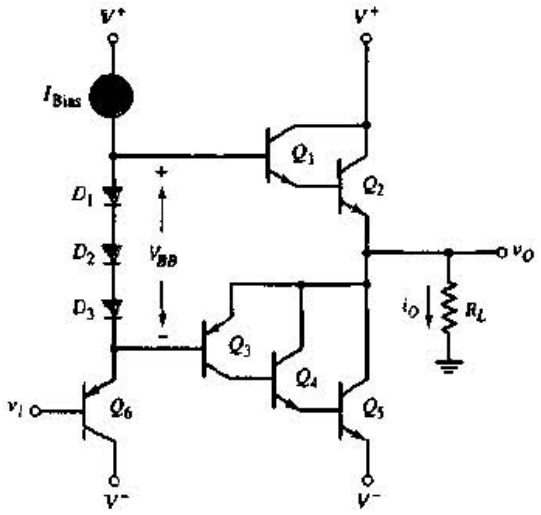

Figure 8.35 Class-AB output stage with Darlington pairs

emitter-follower that sources current to the load. Transistors Q_3, Q_4, and Q_5 constitute a composite pnp Darlington emitter follower that sinks current from the load. The three diodes D_1, D_2, and D_3 establish the quiescent bias for the output transistors.

The effective current gain of the three-transistor configuration Q_3–Q_4–Q_5 is essentially the product of the three individual gains. With the low current gain of the pnp device Q_3, the overall current gain of the Q_3–Q_4–Q_5 configuration is similar to that of the Q_1–Q_2 pair.

Test Your Understanding

8.15 From Figure 8.35, show that the overall current gain of the three-transistor configuration composed of Q_3, Q_4, and Q_5 is approximately $\beta = \beta_3\beta_4\beta_5$.

8.6 SUMMARY

- In this chapter, we analyzed and designed amplifiers and output stages capable of delivering a substantial amount of power to a load.
- The current, voltage, and power ratings of BJTs and MOSFETs were considered, and the safe operating area for the transistors was defined in terms of these limiting parameters. The maximum power rating of a transistor is related to the maximum allowed device temperature at which the device can operate without being damaged.
- In a class-A amplifier, the output transistor conducts 100 percent of the time. The theoretical maximum power conversion efficiency for a standard class-A amplifier is 25 percent. This efficiency can be theoretically increased to 50 percent by incorporating inductors or transformers in the class-A circuit.
- Class-B output stages are composed of complementary pairs of transistors operating in a push–pull manner. In an ideal class-B operation, each output transistor conducts 50 percent of the time. For an idealized Class-B output stage, the theoretical max-

imum power conversion efficiency is 78.5 percent. However, practical class-B output stages tend to suffer from crossover distortion effects when the output is in the vicinity of zero volts.

- The class-AB output stage is similar to the class-B circuit, except that each output transistor is provided with a small quiescent bias and conducts more than 50 percent of the time. The power conversion efficiency of a class-AB output stage is less than that of the ideal class-B circuit, but is substantially larger than that of the class-A circuit.

CHECKPOINT

After studying this chapter, the reader should have the ability to:

- ✔ Describe what factors are related to the maximum transistor current and maximum transistor voltage. (Section 8.2)
- ✔ Define the safe operating area of a transistor and define the power derating curve. (Section 8.2)
- ✔ Define the power conversion efficiency of an output stage. (Section 8.3)
- ✔ Describe the operation of a class-A output stage. (Section 8.3)
- ✔ Describe the operation of an ideal class-B output stage and discuss the concept of crossover distortion. (Section 8.3)
- ✔ Describe and design a class-AB output stage and discuss why crossover distortion is essentially eliminated. (Sections 8.3 and 8.5)

REVIEW QUESTIONS

1. Discuss the limiting factors for the maximum rated current in a BJT and MOSFET.
2. Discuss the limiting factors for the maximum rated voltage in a BJT and MOSFET.
3. Discuss the safe operating area of a transistor.
4. Why is an interdigitated structure typically used in a high-power BJT design?
5. Discuss the role of thermal resistance between various junctions in a high-power transistor structure.
6. Define and describe the power derating curve for a transistor.
7. Define class-A, class-B, and class-AB operation.
8. Define power conversion efficiency for an output stage.
9. Describe the operation of a class-A output stage.
10. Describe the operation of a class-B output stage.
11. Discuss crossover distortion.
12. What is meant by *harmonic* distortion?
13. Describe the operation of a class-AB output stage and why a class-AB output stage is important.
14. Describe the operation of a transformer-coupled class-A common-emitter amplifier.
15. Sketch a class-AB complementary BJT push–pull output stage using a V_{BE} multiplier circuit.
16. What are the advantages of a Darlington pair configuration?
17. Sketch a two-transistor configuration using npn and pnp BJTs that are equivalent to a single pnp BJT.

PROBLEMS

Section 8.2 Power Transistors

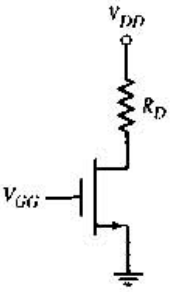

Figure P8.1

8.1 The maximum current, voltage, and power ratings of a power transistor are: 5 A, 80 V, and 25 W, respectively. (a) Sketch and label the safe operating area for this transistor, using linear current and voltage scales. (b) For the common-source circuit in Figure P8.1, determine the value of R_D, and sketch the load line that produces a maximum power in the transistor for: (i) $V_{DD} = 80$ V and (ii) $V_{DD} = 50$ V.

8.2 The common-emitter circuit in Figure P8.2 is biased at $V_{CC} = 24$ V. The maximum transistor power is $P_{D,max} = 20$ W and the current gain is $\beta = 80$. (a) Determine R_L and R_B such that the maximum power is delivered to the load R_L. (b) Find the value of V_p for the input signal that delivers the maximum power. State any assumptions.

D8.3 For the transistor in the common-emitter circuit in Figure P8.2, the parameters are: $\beta = 100$, $P_{D,max} = 2.5$ W, $V_{CE(sus)} = 25$ V, and $I_{C,max} = 500$ mA. Let $R_L = 100\,\Omega$. (a) Design V_{CC} and R_B to deliver the maximum power to the load. (b) Using the results of part (a), calculate the maximum undistorted ac power that can be delivered to R_L.

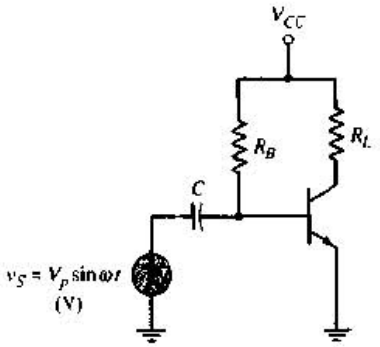

Figure P8.2

8.4 Sketch the safe operating region for a MOSFET. Label three arbitrary points on the maximum hyperbola. Assume each of the labeled points is a Q-point and draw a tangent load line through each point. Discuss the advantages or disadvantages of each point relative to the maximum possible signal amplitude.

8.5 A power MOSFET is connected in a common-source configuration as shown in Figure P8.1. The parameters are: $I_{D,max} = 4$ A, $V_{DS,max} = 50$ V, $P_{D,max} = 35$ W, $V_{TN} = 4$ V, and $K_n = 0.25\,\text{A/V}^2$. The circuit parameters are $V_{DD} = 40$ V and $R_L = 10\,\Omega$. (a) Sketch and label the safe operating area for this transistor, using linear current and voltage scales. Also sketch the load line on the same graph. (b) Calculate the power dissipated in the transistor for $V_{GG} = 5, 6, 7, 8$, and 9 V. (c) Is there a possibility of damaging the transistor? Explain.

D8.6 Consider the common-source circuit shown in Figure P8.6. The transistor parameters are $V_{TN} = 4$ V and $K_n = 0.2\,\text{A/V}^2$. (a) Design the bias circuit such that the Q-point is in the center of the load line. (b) What is the power dissipated in the transistor at the Q-point? (c) Determine the minimum rated $I_{D,max}$, $V_{DS,max}$, and $P_{D,max}$ values. (d) If $v_i = 0.5 \sin \omega t$ V, calculate the ac power delivered to R_L, and determine the average power dissipated in the transistor.

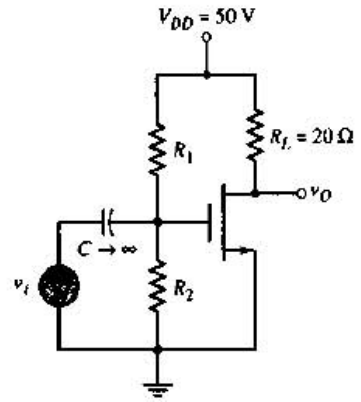

Figure P8.6

8.7 A particular transistor is rated for a maximum power dissipation of 60 W if the case temperature is at 25 °C. Above 25 °C, the allowed power dissipation is reduced by 0.5 W/°C. (a) Sketch the power derating curve. (b) What is the maximum allowed junction temperature? (c) What is the value of $\theta_{dev-case}$?

8.8 A MOSFET has a rated power of 50 W and a maximum specified junction temperature of 150 °C. The ambient is $T_{amb} = 25$ °C. Find the relationship between the actual operating power and $\theta_{case-amb}$.

8.9 For a power MOSFET, $\theta_{dev-case} = 1.75$ °C/W, the drain current is $I_D = 4$ A, and the average drain-to-source voltage is 5 V. The device is mounted on a heat sink with parameters $\theta_{snk-amb} = 3$ °C/W and $\theta_{case-snk} = 0.8$ °C/W. If the ambient temperature is $T_{amb} = 25$ °C, determine the temperature of: (a) device, (b) case, and (c) heat sink.

8.10 A BJT must dissipate 25 W of power. The maximum junction temperature is $T_{j,max} = 200$ °C, the ambient temperature is 25 °C, and the device-to-case thermal resistance is 3 °C/W. Determine the maximum permissible thermal resistance between the case and ambient.

8.11 A BJT has a rated power of 15 W and a maximum junction temperature of 175 °C. The ambient temperature is 25 °C, and the thermal resistance parameters are: $\theta_{snk-amb} = 4$ °C/W and $\theta_{case-snk} = 1$ °C/W. Determine the actual power that can be safely dissipated in the transistor.

Section 8.3 Classes of Amplifiers

8.12 For the class-A amplifier shown in Figure 8.16(a), show that the maximum theoretical conversion efficiency for a symmetrical square-wave input signal is 50 percent.

***D8.13** A class-A emitter follower biased with a constant-current source is shown in Figure P8.13. Assume the circuit parameters are: $V^+ = 10$ V, $V^- = -10$ V, and $R_L = 1$ kΩ. The transistor parameters are: $\beta = 200$, $V_{BE} = 0.7$ V, and $V_{CE}(\text{sat}) = 0.2$ V. (a) Determine the value of R that will produce the maximum possible output signal swing. What is the value of I_Q, and the maximum and minimum values of i_{E1} and i_L? (b) Using the results of part (a), calculate the conversion efficiency.

8.14 The circuit parameters for the class-A emitter follower shown in Figure P8.13 are: $V^+ = 12$ V, $V^- = -12$ V, and $R_L = 100\,\Omega$. The transistor parameters are: $\beta = 200$, $V_{BE} = 0.7$ V, and $V_{CE}(\text{sat}) = 0.2$ V. The output voltage is to vary between +10 V and −10 V. (a) Find the minimum required I_Q and the value of R. (b) For $v_O = 0$, find the

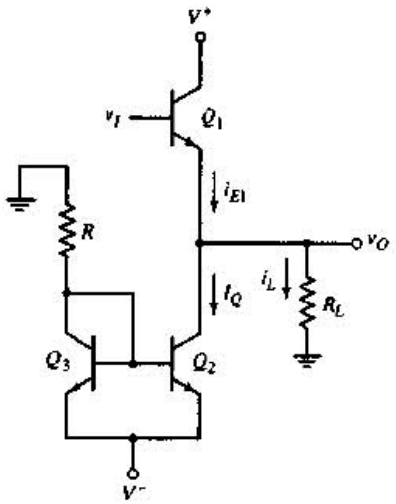

Figure P8.13

power dissipated in the transistor Q_1, and the power dissipated in the current source (Q_2, Q_3, and R). (c) Determine the conversion efficiency for a symmetrical sine-wave output voltage with a peak value of 10 V.

8.15 For the idealized class-B output stage in Figure 8.18, show that the maximum theoretical conversion efficiency for a symmetrical square-wave input signal is 100 percent.

8.16 Consider the class-B output stage with complementary MOSFETs shown in Figure P8.16. The transistor parameters are $V_{TN} = V_{TP} = 0$ and $K_n = K_p = 0.4\,\text{mA/V}^2$. Let $R_L = 5\,\text{k}\Omega$. (a) Find the maximum output voltage such that M_n remains biased in the saturation region. What are the corresponding values of i_L and v_I for this condition? (b) Determine the conversion efficiency for a symmetrical sine-wave output signal with the peak value found in part (a).

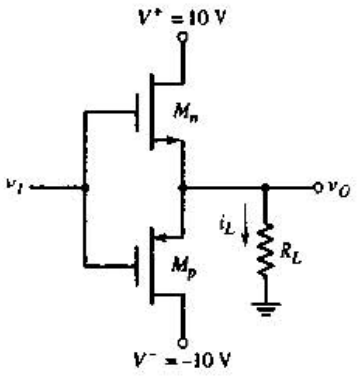

Figure P8.16

8.17 Using the same transistor parameters listed in Problem 8.16 for the circuit shown in Figure P8.16, plot v_O versus v_I for $-10 \le v_I \le +10\,\text{V}$. What is the voltage gain (slope of the curve) at $v_I = 0$ and at $v_I = 10\,\text{V}$?

***8.18** A simplified class-AB output stage with BJTs is shown in Figure 8.23. The circuit parameters are $V_{CC} = 10\,\text{V}$ and $R_L = 100\,\Omega$. The parameter I_S for each transis-

tor is $I_S = 5 \times 10^{-13}$ A. (a) Determine the value of V_{BB} such that $i_{Cn} = i_{Cp} = 5$mA when $v_I = 0$. What is the power dissipated in each transistor? (b) For $v_O = -8$ V, determine i_L, i_{Cn}, i_{Cp}, and v_I. What is the power dissipated in Q_n, Q_p, and R_L?

***8.19** A simplified class-AB output stage with enhancement-mode MOSFETs is shown in Figure 8.25. The circuit parameters are $V_{DD} = 10$ V and $R_L = 1$ kΩ. The transistor parameters are $V_{TN} = -V_{TP} = 2$ V and $K_n = K_p = 2$ mA/V^2. (a) Determine the value of V_{BB} such that $i_{Dn} = i_{Dp} = 0.5$ mA when $v_I = 0$. What is the power dissipated in each transistor? (b) Determine the maximum output voltage such that M_n remains biased in the saturation region. What are the values of i_{Dn}, i_{Dp}, i_L, and v_I for this case? Calculate the power dissipated in M_n, M_p, and R_L.

8.20 Consider the class-AB output stage in Figure P8.20. The diodes and transistors are matched, with parameters $I_S = 6 \times 10^{-12}$ A, and $\beta = 40$. (a) Determine R_1 such that the miminum current in the diodes is 25 mA when $v_O = 24$ V. Find i_N and i_P for this condition. (b) Using the results of part (a), determine the diode and transistor currents when $v_O = 0$.

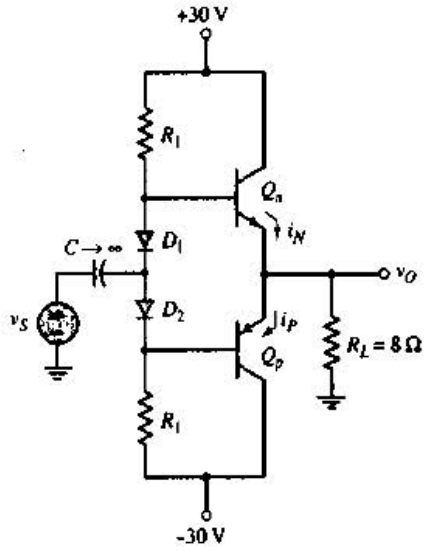

Figure P8.20

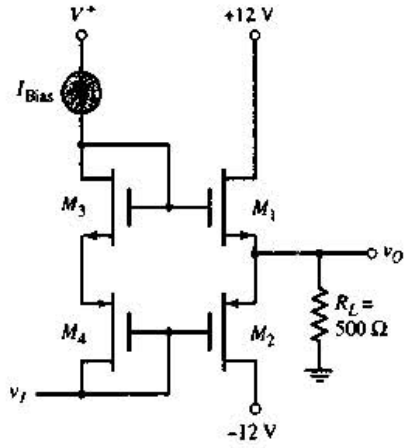

Figure P8.21

***8.21** An enhancement-mode MOSFET class-AB output stage is shown in Figure P8.21. The threshold voltage of each transistor is $V_{TN} = -V_{TP} = 1$V and the conduction parameters of the output transistors are $K_{n1} = K_{p2} = 5$ mA/V^2. Let $I_{Bias} = 200\,\mu$A. (a) Determine $K_{n3} = K_{p4}$ such that the quiescent drain currents in M_1 and M_2 are 5 mA. (b) Using the results of part (a), find the small-signal voltage gain $A_v = dv_O/dv_I$ evaluated at: (i) $v_O = 0$, and (ii) $v_O = 5$ V.

D8.22 Consider the MOSFET class-AB output stage in Figure 8.25. The parameters are: $V_{DD} = 10$ V and $R_L = 100\,\Omega$. For transistors M_n and M_p, $V_{TN} = -V_{TP} = 1$ V. The peak amplitude of the output voltage is limited to 5 V. Design the circuit such that the small-signal voltage gain is $A_v = dv_O/dv_I = 0.95$ when $v_O = 0$.

Section 8.4 Class-A Power Amplifiers

D8.23 Design an inductively coupled common-emitter amplifier, such as that in Figure 8.27(a), to provide a small-signal voltage gain of $A_v = -12$. The circuit and transistor parameters are: $R_i = 6\,\text{k}\Omega$, $R_L = 2\,\text{k}\Omega$, $V_{CC} = 10\,\text{V}$, $\beta = 180$, and $V_{BE} = 0.7\,\text{V}$. Determine the maximum power that can be delivered to the load, and the conversion efficiency.

D8.24 For the inductively coupled amplifier in Figure 8.27(a), the parameters are: $V_{CC} = 15\,\text{V}$, $R_E = 0.1\,\text{k}\Omega$, and $R_L = 1\,\text{k}\Omega$. The transistor parameters are $\beta = 100$ and $V_{BE} = 0.7\,\text{V}$. Design R_1 and R_2 to deliver the maximum power to the load. What is the maximum power that can be delivered to the load?

8.25 Consider the transformer-coupled common-emitter circuit shown in Figure P8.25. The parameters are: $V_{CC} = 10\,\text{V}$, $R_L = 8\,\Omega$, $n_1 : n_2 = 3 : 1$, $R_1 = 0.73\,\text{k}\Omega$, $R_2 = 1.55\,\text{k}\Omega$, and $R_E = 20\,\Omega$. The transistor parameters are $\beta = 25$ and $V_{BE}(\text{on}) = 0.7\,\text{V}$. The amplitude of the sinusoidal input voltage is 17 mV. Determine the ac power delivered to the load, and the conversion efficiency.

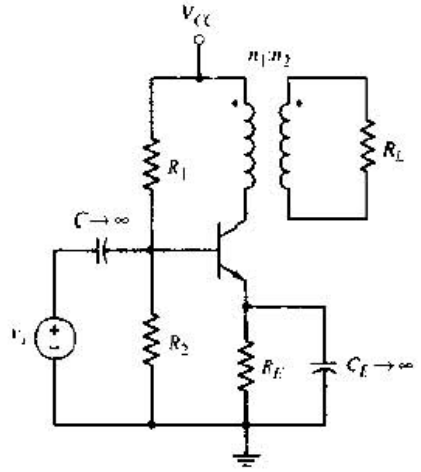

Figure P8.25

8.26 The parameters for the transformer-coupled common-emitter circuit in Figure P8.25 are $V_{CC} = 36\,\text{V}$ and $n_1 : n_2 = 4 : 1$. The signal power delivered to the load is 2 W. Determine: (a) the rms voltage across the load; (b) the rms voltage across the transformer primary; and (c) the primary and secondary currents. (d) If $I_{CQ} = 150\,\text{mA}$, what is the conversion efficiency?

8.27 A BJT emitter follower is coupled to a load with an ideal transformer, as shown in Figure P8.27. The bias circuit is not shown. The transistor current gain is $\beta = 49$, and the transistor is biased such that $I_{CQ} = 100\,\text{mA}$. (a) Derive the expressions for the voltage transfer functions v_e/v_i and v_o/v_i. (b) Find $n_1 : n_2$ for maximum ac power transfer to R_L. (c) Determine the small-signal output resistance looking back into the emitter.

D8.28 Consider the transformer-coupled emitter follower in Figure P8.28. Assume an ideal transformer. The transistor parameters are $\beta = 100$ and $V_{BE} = 0.7\,\text{V}$. (a) Design the circuit to provide a current gain at $A_i = i_o/i_i = 80$. (b) If the magnitude of the signal emitter current is limited to $0.9\,I_{CQ}$ to prevent distortion, determine the power delivered to the load, and the conversion efficiency.

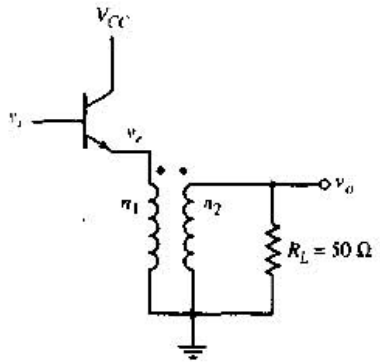

Figure P8.27

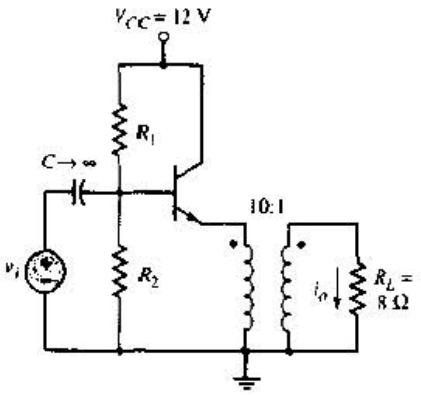

Figure P8.28

D8.29 A class-A transformer-coupled emitter follower must deliver 2 W to an 8 Ω speaker. Let $V_{CC} = 18$ V, $\beta = 100$, and $V_{BE} = 0.7$ V. (a) Determine the required transformer ratio $n_1 : n_2$. (b) Determine the minimum transistor power rating.

D8.30 Repeat Problem 8.28 if the primary side of the transformer has a resistance of 100 Ω.

Section 8.5 Class-AB Push–Pull Complementary Output Stages

8.31 The transistors in the output stage in Figure 8.33 are all matched. Their parameters are $\beta = 60$ and $I_S = 5 \times 10^{-13}$ A. Resistors R_1 and R_2 are replaced by 3 mA ideal current sources, and $R_3 = R_4 = 0$. Let $V^+ = 10$ V and $V^- = -10$ V. (a) Determine the quiescent collector currents in the four transistors for $v_I = v_O = 0$. (b) For a load resistance of $R_L = 20\,\Omega$ and a peak output voltage of 6 V, determine the current gain and voltage gain of the circuit.

***8.32** Consider the circuit in Figure 8.33. The supply voltages are $V^+ = 10$ V and $V^- = -10$ V, and the R_3 and R_4 resistor values are zero. The transistor parameters are: $\beta_1 = \beta_2 = 120$, $\beta_3 = \beta_4 = 50$, $I_{S1} = I_{S2} = 2 \times 10^{-13}$ A, and $I_{S3} = I_{S4} = 2 \times 10^{-12}$ A. (a) The range in output current is $-1 \le i_O \le +1$ A. Determine the values of R_1 and R_2 such that the currents in Q_1 and Q_2 do not vary by more than 2 : 1. (b) Using the results of part (a), determine the quiescent collector currents in the four transistors for $v_I = v_O = 0$. (c) Calculate the output resistance, excluding R_L, for a quiescent output voltage of zero. Assume the source resistance of v_I is zero.

8.33 Using the parameters given in Example 8.11 for the circuit in Figure 8.33, calculate the input resistance when the quiescent output voltage is zero.

D8.34 (a) Redesign the class-AB output stage in Figure 8.33 using enhancement-mode MOSFETs. Let $R_3 = R_4 = 0$. (b) Assume the MOSFETs are all matched, and their parameters are $K = 10\,\text{mA/V}^2$ and $V_{TN} = -V_{TP} = 2$ V. Let $V^+ = 10$ V and $V^- = -10$ V. Find R_1 and R_2 such that the quiescent current in each transistor is 5 mA. (c) If $R_L = 100\,\Omega$, determine the current in each transistor; determine the power delivered to the load if $v_O = 5$ V.

8.35 Figure P8.35 shows a composite pnp Darlington emitter follower that sinks current from a load. Parameter I_Q is the equivalent bias current and Z is the equivalent impedance in the base of Q_1. Assume the transistor parameters are: β(pnp) = 10, β(npn) = 50, $V_{AP} = 50$ V, and $V_{AN} = 100$ V, where V_{AP} and V_{AN} are the Early voltages of the pnp and npn devices, respectively. Calculate the output resistance R_o.

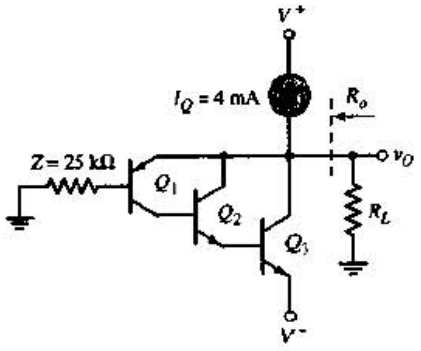

Figure P8.35

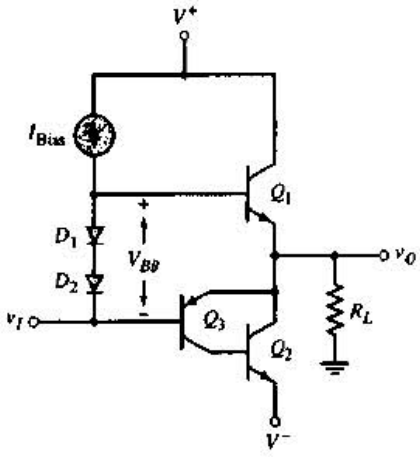

Figure P8.36

***8.36** Consider the class-AB output stage in Figure P8.36. The parameters are: $V^+ = 12\,\text{V}$, $V^- = -12\,\text{V}$, $R_L = 100\,\Omega$, and $I_{\text{Bias}} = 5\,\text{mA}$. The transistor and diode parameters are $I_S = 10^{-13}\,\text{A}$. The transistor current gains are $\beta_n = 100$ and $\beta_p = 20$ for the npn and pnp devices, respectively. (a) For $v_O = 0$, determine V_{BB}, and the quiescent collector current and base–emitter voltage for each transistor. (b) Repeat part (a) for $v_O = 10\,\text{V}$. What is the power delivered to the load and what is the power dissipated in each transistor?

***8.37** For the class-AB output stage in Figure 8.35, the parameters are: $V^+ = 24\,\text{V}$, $V^- = -24\,\text{V}$, $R_L = 20\,\Omega$, and $I_{\text{Bias}} = 10\,\text{mA}$. The diode and transistor parameters are $I_S = 2 \times 10^{-12}\,\text{A}$. The transistor current gains are $\beta_n = 20$ and $\beta_p = 5$ for the npn and pnp devices, respectively. (a) For $v_O = 0$, determine V_{BB}, and the quiescent collector and base–emitter voltage for each transistor. (b) An average power of 10 watts is to be delivered to the load. Determine the quiescent collector current in each transistor and the instantaneous power dissipated in Q_2, Q_5, and R_L when the output voltage is at its peak negative amplitude.

COMPUTER SIMULATION PROBLEMS

8.38 (a) Simulate the class-B output stage in Figure 8.18 and plot the voltage transfer function to demonstrate the crossover distortion region. (b) Repeat part (a) for the class-AB output stage shown in Figure 8.30. Use diode-connected transistors for D_1 and D_2 and assume all devices are matched. Has the crossover distortion region been eliminated?

8.39 Verify the design of the class-AB output stage in Example 8.9 with a computer analysis.

8.40 (a) Simulate the class-AB output stage shown in Figure 8.33, using parameters $V^+ = -V^- = 15\,\text{V}$, $R_1 = R_2 = 2\,\text{k}\Omega$, $R_L = 100\,\Omega$, and $R_3 = R_4 = 0$. Assume all transistors are matched, with parameters $I_S = 10^{-13}\,\text{A}$ and $\beta = 60$. Plot v_O versus v_I and i_O versus i_I for $-10 \le v_I \le +10\,\text{V}$. Determine the voltage and current gains. (b) Repeat part (a) for $R_3 = R_4 = 20\,\Omega$.

8.41 Consider the class-AB output stage shown in Figure 8.33. The parameters are: $V^+ = -V^- = 15\,\text{V}$, $R_1 = R_2 = 2\,\text{k}\Omega$, $R_L = 8\,\Omega$, and $R_3 = R_4 = 0$. Assume all transis-

tors are matched, with $I_S = 10^{-13}$ A and $\beta = 60$. Assume the input voltage is given by $v_I = V_p \sin \omega t$. Determine the average power delivered to the load, and the average power dissipated in Q_3 and Q_4, for $0 \leq V_p \leq 13$ V.

DESIGN PROBLEMS

[Note: Each design should be correlated with a computer analysis.]

***D8.42** Design an audio amplifier to deliver an average of 60 W to an 8 Ω speaker. The bandwidth is to cover the range from 10 Hz to 15 kHz. Specify minimum current gains, and current, voltage, and power ratings of all transistors.

***D8.43** Design a class-A transformer-coupled emitter-follower amplifier to deliver an average power of 20 W to an 8 Ω speaker. The ambient temperature is 25 °C, and the maximum junction temperature is $T_{j,\max} = 125$ °C. Assume the thermal resistance values are: $\theta_{dev-case} = 3.6$ °C/W, $\theta_{case-snk} = 0.5$ °C/W, and $\theta_{snk-amb} = 4.5$ °C/W. Specify the power supply voltage, transformer turns ratio, bias resistor values, and transistor current, voltage, and power ratings.

***D8.44** Design the class-AB output stage with the V_{BE} multiplier shown in Figure 8.31 to deliver an average of 5 W to an 8 Ω load. The peak output voltage must be no more than 80 percent of V^+. Let $V^- = -V^+$. Specify the circuit and transistor parameters.

Industry Insight

LINLEY GUMM
Principal Engineer
Tektronix, Inc.

"Virtually every electronics designer uses the principles in this part. These are core principles; they are used at some level in every design, analog or digital. They must be mastered before the design of specialized electronics used by advanced professionals can be understood or attempted.

Of course, analog circuit designers use the contents of this part daily. As an example, I recently designed the baseband analog subsystem for a digitally based cellular telephone test system. It consisted of a digital-to-analog converter, followed by a multistage active and passive filter. The design used operational amplifiers in many configurations. Designing the system required the basic operational amplifier principles illustrated in Chapter 9, a knowledge of how they are internally configured, as given in Chapter 13, and the nonideal effects described in Chapter 14. The active filter uses several combinations of the active filters shown in Chapter 15. Feedback was used around every individual stage, plus around the whole filter. Each of these paths required analysis using the principles shown in Chapter 12. The accuracy of the system was based on a voltage reference IC that is similar to the voltage regulators shown in Chapter 13. This is not to say that the rest of the circuits shown in this part are not useful. They are also very important and are frequently used in my other designs.

Many have concluded that analog circuits are obsolete and are not worth studying. It must be remembered that, at base, every electronic circuit is analog! The logic gate, the basic element of digital design, is an analog circuit using the circuit elements and principles described here. Beyond that, every digital system in the world uses analog subsystems for conditioning their input and output signals. Far from being obsolete, analog circuits are experiencing a resurgence of interest, as they are used to provide the physical layers of the digital communications systems that are transforming the world in which we live. These principles are important and will continue to be. Learn them well, because they provide the basis for understanding everything electronic."

PART

II

ANALOG ELECTRONICS

Part I of this text dealt with the basic electronic devices, and the fundamental circuit configurations and characteristics. Part II deals with more complex analog circuits, of which amplifiers are a very significant category.

Chapter 9 introduces the ideal op-amp and related circuits. The op-amp is one of the most common analog integrated circuits. IC biasing techniques, which primarily use constant-current sources, are described in Chapter 10. One of the most widely used amplifier configurations is the differential amplifier, which is analyzed in Chapter 11. Chapter 12 covers the fundamentals of feedback, which is used extensively in analog circuits to set or control gain values more precisely, and to alter, in a favorable way, input and output impedances.

More complex analog integrated circuits, including circuits that form operational amplifiers, are discussed in Chapter 13. These circuits are composed of fundamental configurations, such as the diff-amp, constant-current source, active load, and output stage, all of which have been previously analyzed. Then, Chapter 14 considers the non-ideal effects in these operational amplifiers, and discusses the impacts of such effects on op-amp applications. Integrated circuit applications and designs are considered in Chapter 15. Such applications include: active filters, tuned amplifiers, and oscillators.

CHAPTER

9

The Ideal Operational Amplifier

9.0 PREVIEW

An operational amplifier (op-amp) is an integrated circuit that amplifies the difference between two input voltages and produces a single output. The op-amp is prevalent in analog electronics, and can be thought of as another electronic device, in much the same way as the bipolar or field-effect transistor.

The term operational amplifier comes from the original applications of the device in the early 1960s. Op-amps, in conjunction with resistors and capacitors, were used in analog computers to perform mathematical operations to solve differential and integral equations. The application of op-amps has expanded significantly since those early days.

The main reason for postponing the discussion of op-amp circuits until now is that we can use a relatively simple transistor circuit to develop the ideal characteristics of the op-amp, instead of simply stating the ideal parameters as postulates. Once the ideal properties have been developed, the reader can then be more comfortable applying these ideal characteristics in the design of op-amp circuits. Just as we developed equivalent circuits of transistors that include dependent sources representing gain factors, we will develop a basic op-amp equivalent circuit with a dependent source that represents the device gain that can be used to determine some of the nonideal properties of op-amp circuits.

Op-amps are used extensively in the design of electronic circuits and systems because of their relatively low cost and versatility, and because integrated circuit op-amp characteristics approach the ideal. We will consider, in this chapter, a few of the many applications of op-amps. By the end of the chapter, the reader should be able to design fairly sophisticated circuits using op-amps. (See the Overview of Electronic Design section in this chapter.)

9.1 THE OPERATIONAL AMPLIFIER

The integrated circuit operational amplifier evolved soon after development of the first bipolar integrated circuit. The μA-709 was introduced by Fairchild Semiconductor in 1965 and was one of the first widely used general purpose op-amps. The now classic μA-741, also by Fairchild, was introduced in the late 1960s. Since then, a vast array of op-amps with improved characteristics, using

both bipolar and MOS technologies, have been designed. Most op-amps are very inexpensive (less than a dollar) and are available from a wide range of suppliers.

From a signal point of view, the op-amp has two input terminals and one output terminal, as shown in the small-signal circuit symbol in Figure 9.1(a). The op-amp also requires dc power, as do all transistor circuits, so that the transistors are biased in the active region. Also, most op-amps are biased with both a positive and a negative voltage supply, as indicated in Figure 9.1(b). As

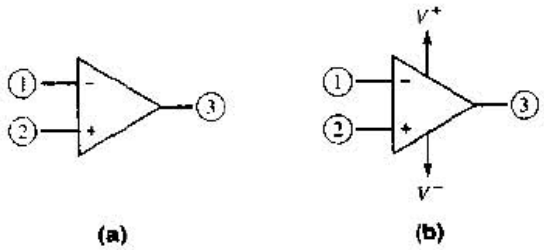

Figure 9.1 (a) Small-signal circuit symbol of the op-amp; (b) op-amp with positive and negative supply voltages

before, the positive voltage is indicated by V^+ and the negative voltage by V^-.

There are normally 20 to 30 transistors that make up an op-amp circuit. The typical IC op-amp has parameters that approach the ideal characteristics. For this reason, then, we can treat the op-amp as a "simple" electronic device, which means that it is quite easy to design a wide range of circuits using the IC op-amp.

In this chapter, we develop the ideal set of op-amp parameters and then consider the analysis and design of a wide variety of op-amp circuits, which will aid in our understanding of the design process of electronic circuits. We generally assume, in this chapter, that the op-amp is ideal. In the following chapters, we consider the differential amplifier, current-source biasing, and feedback, which leads to the development of the actual operational amplifier circuit in Chapter 13. Once the actual op-amp circuit is studied, then the source of nonideal characteristics can be understood. The effect of nonideal op-amp parameters is then considered in Chapter 14. Additional op-amp applications are given in Chapter 15.

9.1.1 Ideal Parameters

The ideal op-amp senses the difference between two input signals and amplifies this difference to produce an output signal. The terminal voltage is the voltage at a terminal measured with respect to ground. The ideal op-amp equivalent circuit is shown in Figure 9.2(a).

Ideally, the input impedance is infinite, which means that the input current is zero. The output terminal of the ideal op-amp acts as the output of an ideal voltage source, meaning that the small-signal output impedance is zero.

The parameter A_{od} shown in the equivalent circuit is the **differential gain** of the op-amp. The output is out of phase with respect to v_1 and in phase with respect to v_2. Terminal (1) then is **the inverting input terminal**, designated by the

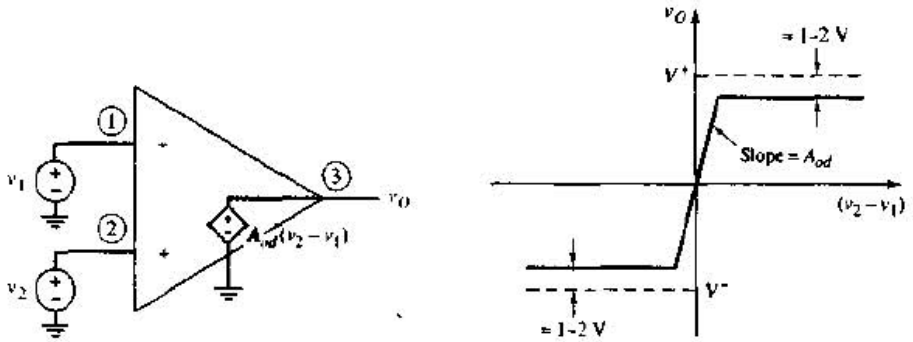

Figure 9.2 (a) Ideal op-amp equivalent circuit and (b) op-amp transfer characteristics

"−" notation, and terminal (2) is the **noninverting input terminal**, designated by the "+" notation.

Since the ideal op-amp responds only to the difference between the two input signals v_1 and v_2, the ideal op-amp maintains a zero output signal for $v_1 = v_2$. When $v_1 = v_2 \neq 0$, there is what is called a **common-mode input signal**. For the ideal op-amp, the common-mode output signal is zero. This characteristic is referred to as **common-mode rejection**.

Because the device is biased with both positive and negative power supplies, most op-amps are direct-coupled devices (i.e., no coupling capacitors are used on the input). Therefore, the input voltages v_1 and v_2 shown in Figure 9.2(a) can be dc voltages, which will produce a dc output voltage v_O.

Since the op-amp is composed of transistors biased in the active region by the dc input voltages V^+ and V^-, the output voltage is limited. When v_O approaches V^+, it will saturate, or be limited to a value nearly equal to V^+, since it cannot go above the positive bias voltage. Similarly, when the output voltage approaches V^-, it will saturate at a value nearly equal to V^-. The actual saturation voltages vary from one op-amp to another, but in general the output volage is limited to $V^- + \Delta V < v_O < V^+ - \Delta V$, where ΔV is generally between 1 and 2 V. Figure 9.2(b) is a simplified voltage transfer characteristic for the op-amp, showing this saturation effect.

The ideal op-amp is being considered in this chapter, in order to gain an appreciation of the properties and characteristics of op-amp circuits. Two important op-amp parameters are: the differential gain A_{od} and the bandwidth, or frequency response. The differential gain A_{od} is very large, ideally infinite. We will see how this property produces ideal op-amp circuit characteristics. The bandwidth or frequency response of op-amps is discussed in Chapter 13.

9.1.2 Development of the Ideal Parameters

To develop the ideal op-amp parameters, we start with the MOSFET small-signal equivalent circuit and apply this model to a particular circuit. Figure 9.3(a) shows an n-channel enhancement-mode MOSFET, and Figure 9.3(b) is the simplified low-frequency small-signal equivalent circuit. In our analysis, the transistor small-signal output resistance r_o is assumed to be infinite.

Figure 9.4 shows the MOSFET equivalent circuit with two external circuit resistors, R_1 and R_F, and an input voltage v_I. Resistor R_F is a **feedback resistor**

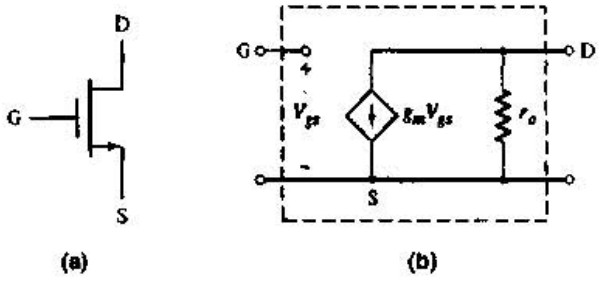

Figure 9.3 (a) n-channel enhancement-mode MOSFET and (b) small-signal equivalent circuit

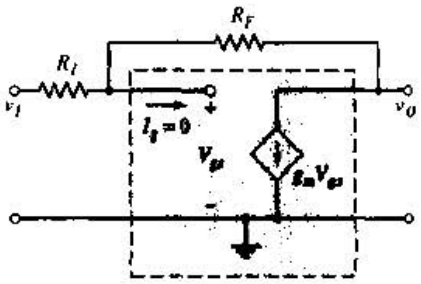

Figure 9.4 Simplified small-signal equivalent circuit of a MOSFET with input and feedback resistors

that connects the output back to the input of the transistor. This circuit is therefore called a feedback circuit. In this example, we use a single transistor as the basic amplifier of the feedback circuit.

Writing a KCL equation at the gate terminal, we obtain

$$\frac{v_I - V_{gs}}{R_I} = \frac{V_{gs} - v_O}{R_F} \tag{9.1(a)}$$

which can be arranged as

$$\frac{v_I}{R_I} + \frac{v_O}{R_F} = V_{gs}\left(\frac{1}{R_I} + \frac{1}{R_F}\right) \tag{9.1(b)}$$

Since the input impedance to the transistor is infinite, the current into the device is zero.

A KCL equation at the output node yields

$$\frac{V_{gs} - v_O}{R_F} = g_m V_{gs} \tag{9.2(a)}$$

which can be solved for V_{gs}, as follows:

$$V_{gs} = \frac{v_O}{R_F} \cdot \frac{1}{\left(\frac{1}{R_F} - g_m\right)} \tag{9.2(b)}$$

Substituting Equation (9.2(b)) into (9.1(b)) results in the overall voltage gain of the circuit

$$\frac{v_O}{v_I} = -\frac{R_F}{R_I} \cdot \frac{\left(1 - \frac{1}{g_m R_F}\right)}{\left(1 + \frac{1}{g_m R_F}\right)} \tag{9.3}$$

If we let the gain g_m of the basic amplifier (i.e., the transistor) go to infinity, then the overall voltage gain becomes

$$\frac{v_O}{v_I} = -\frac{R_F}{R_I} \tag{9.4}$$

Equation (9.4) shows that the overall voltage gain is the ratio of two external circuit resistors, which is one result of using an ideal op-amp. The negative sign indicates a 180 degree phase shift between the input and the output, which

means that the input to the transistor corresponds to the inverting terminal of an op-amp. The voltage gain given by Equations (9.3) and (9.4) is called a **closed-loop voltage gain**, since feedback is incorporated into the circuit. Conversely, the voltage gain A_{od} is an **open-loop gain**.

Voltage V_{gs} at the input of the basic amplifier (transistor) is given by Equation (9.2(b)). Again, if we let the gain g_m go to infinity, then $V_{gs} \cong 0$; that is, the voltage at the input terminal to the basic amplifier is almost at ground potential. This terminal is said to be at **virtual ground**, which is another characteristic that we will observe in ideal op-amp circuits.

The output resistance of this circuit can be determined from the equivalent circuit shown in Figure 9.5. The input signal source is set at zero. A KCL equation at the output node, written in phasor notation, is

$$I_x = g_m V_{gs} + \frac{V_x}{R_1 + R_F} \tag{9.5}$$

Voltage V_{gs} can be written in terms of the test voltage V_x, as

$$V_{gs} = V_x\left(\frac{R_1}{R_1 + R_F}\right) \tag{9.6}$$

Substituting Equation (9.6) into (9.5), we find that

$$\frac{I_x}{V_x} = \frac{1}{R_o} = \frac{1 + g_m R_1}{R_1 + R_F} \tag{9.7}$$

If the gain g_m goes to infinity, then $1/R_o \to \infty$, or $R_o \to 0$. The output resistance of the circuit with negative feedback included goes to zero. This is also a property of an ideal op-amp circuit.

A simplified MOSFET model with a large gain has thus provided the properties of an ideal op-amp.

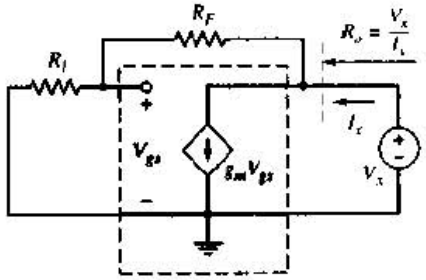

Figure 9.5 Equivalent circuit determining output resistance

9.1.3 Analysis Method

Usually, an op-amp is not used in the open-loop configuration shown in Figure 9.2(a). Instead, feedback is added to close the loop between the output and the input. In this chapter, we will limit our discussion to **negative feedback**, in which the connection from the output goes to the inverting terminal, or terminal (1). As we will see later, this configuration produces stable circuits; positive feedback, in which the output is connected to the noninverting terminal, can be used to produce oscillators.

The ideal op-amp characteristics resulting from our negative feedback analysis are shown in Figure 9.6 and summarized below.

1. The internal differential gain A_{od} is considered to be infinite.
2. The differential input voltage $(v_2 - v_1)$ is assumed to be zero. If A_{od} is very large and if the output voltage v_O is finite, then the two input voltages must be nearly equal.
3. The effective input resistance to the op-amp is assumed to be infinite, so the two input currents, i_1 and i_2, are essentially zero.
4. The output resistance R_o is assumed to be zero in the ideal case, so the output voltage is connected directly to the dependent voltage source, and the output voltage is independent of any load connected to the output.

We use these ideal characteristics in the analysis and design of op-amp circuits.

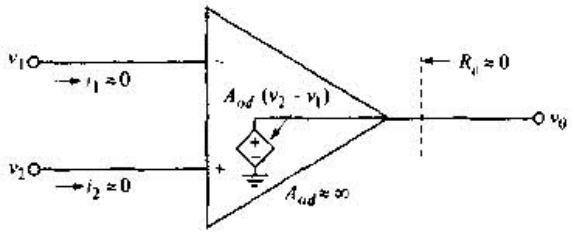

Figure 9.6 Parameters of the ideal op-amp

9.1.4 PSpice Modeling

Three general purpose op-amps are included in the PSpice library. The PSpice circuit simulation uses a macromodel, which is a simpified version of the op-amp, to model the op-amp characteristics. For example, the μA-741 op-amp has parameters $R_i = 2\,\text{M}\Omega$, $R_o = 75\,\Omega$, $A_{od} = 2 \times 10^5$, and a unity-gain bandwidth of $f_{BW} = 1\,\text{MHz}$. This device is also capable of producing output voltages of $\pm 14\,\text{V}$ with dc power supply voltages of $\pm 15\,\text{V}$. We will see in several examples as to whether these nonideal parameters affect actual circuit properties.

9.2 INVERTING AMPLIFIER

One of the most widely used op-amp circuits is the **inverting amplifier**. Figure 9.7 shows the closed-loop configuration of this circuit. We must keep in mind that the op-amp is biased with dc voltages, although those connections are seldom explicitly shown.

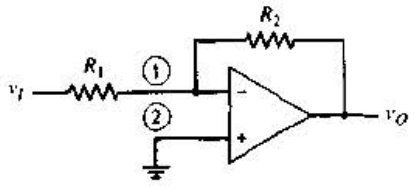

Figure 9.7 Inverting op-amp circuit

9.2.1 Basic Amplifier

We analyze the circuit in Figure 9.7 by considering the ideal equivalent circuit shown in Figure 9.8. **The closed-loop voltage gain**, or simply the voltage gain, is defined as

$$A_v = \frac{v_O}{v_I} \tag{9.8}$$

We stated that if the open-loop gain A_{od} is very large, then the two inputs v_1 and v_2 must be nearly equal. Since v_2 is at ground potential, voltage v_1 must also be approximately zero volts. We must point out, however, that having v_1 be essentially at ground potential does not imply that terminal (1) is grounded. Rather, terminal (1) is said to be at **virtual ground**; that is, it is essentially zero volts, but it does not provide a current path to ground.

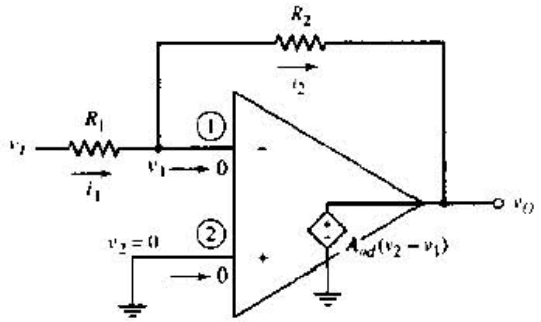

Figure 9.8 Inverting op-amp equivalent circuit

From Figure 9.8, we can write

$$i_1 = \frac{v_I - v_1}{R_1} = \frac{v_I}{R_1} \tag{9.9}$$

Since the current into the op-amp is assumed to be zero, current i_1 must flow through resistor R_2 to the output terminal, which means that $i_1 = i_2$.

The output voltage is given by

$$v_O = v_1 - i_2 R_2 = 0 - \left(\frac{v_I}{R_1}\right) R_2 \tag{9.10}$$

Therefore, the closed-loop voltage gain is

$$A_v = \frac{v_O}{v_I} = -\frac{R_2}{R_1} \tag{9.11}$$

For the ideal op-amp, the closed-loop voltage gain is a function of the ratio of two resistors; it is not a function of the transistor parameters within the op-amp circuit. Again, the minus sign implies a phase reversal. If the input voltage v_I is positive, then, because v_1 is essentially at ground potential, the output voltage v_O must be negative, or below ground potential. Also note that if the output terminal is open-circuited, current i_2 must flow back into the op-amp. However, since the output impedance for the ideal case is zero, the output

voltage is not a function of this current that flows back into the op-amp and is not dependent on the load.

We can also determine the input resistance seen by the voltage source v_I. Because of the virtual ground, we have, from Equation (9.9)

$$i_1 = v_I/R_1$$

The **input resistance** is then defined as

$$R_i = \frac{v_I}{i_1} = R_1 \tag{9.12}$$

This shows that the input resistance seen by the source is a function of R_1 only, and is a result of the "virtual ground" concept. Figure 9.9 summarizes our analysis of the inverting amplifier circuit.

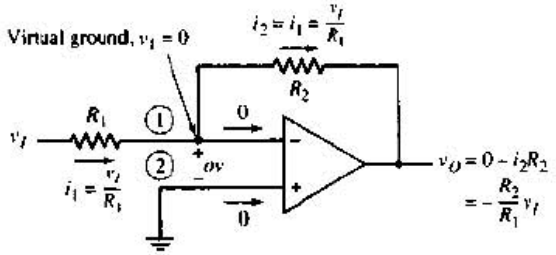

Figure 9.9 Currents and voltages in the inverting op-amp

Design Example 9.1 **Objective:** Design an inverting amplifier with a closed-loop voltage gain of $A_f = -5$.

Assume the op-amp is driven by a sinusoidal source, $v_S = 0.1 \sin \omega t$ volts, which has a source resistance of $R_S = 1\,\text{k}\Omega$ and which can supply a maximum current of $5\,\mu\text{A}$. Assume that frequency ω is low, which means that any frequency effects can be neglected.

Solution: The signal source resistance is in series with the input resistor R_1 (Figure 9.9), so

$$i_1 = \frac{v_S}{R_S + R_1}$$

If $i_1(\text{max}) = 5\,\mu\text{A}$, then we can write

$$R_1(\text{min}) + R_S = \frac{v_S(\text{max})}{i_1(\text{max})} = \frac{0.1}{5 \times 10^{-6}} \Rightarrow 20\,\text{k}\Omega$$

The resistance R_1, then, should be $19\,\text{k}\Omega$. The closed-loop gain is given by

$$A_f = \frac{-R_2}{R_S + R_1} = -5$$

where again, the source resistance must be taken into account. We then have

$$R_2 = 5(R_S + R_1) = 5(20) = 100\,\text{k}\Omega$$

Comment An inverting op-amp with $R_1 = 19\,\text{k}\Omega$ and $R_2 = 100\,\text{k}\Omega$ will satisfy the specified requirements. We note that the resistance of the source must be taken into account.

Computer Verification: Figure 9.10(a) shows the PSpice circuit schematic used in the computer simulation and Figure 9.10(b) shows the 100 mV sinusoidal input signal. Figure 9.10(c) is the output signal which shows that a gain of 5 (magnitude) has been achieved and also shows that the output signal is 180 degrees out of phase with respect to the input signal. Finally, the input current is shown in Figure 9.10(d) with a maximum value of 5 μA. The actual circuit characteristics are not influenced to any great extent by the nonideal parameters of the μA-741 op-amp used in the circuit simulation.

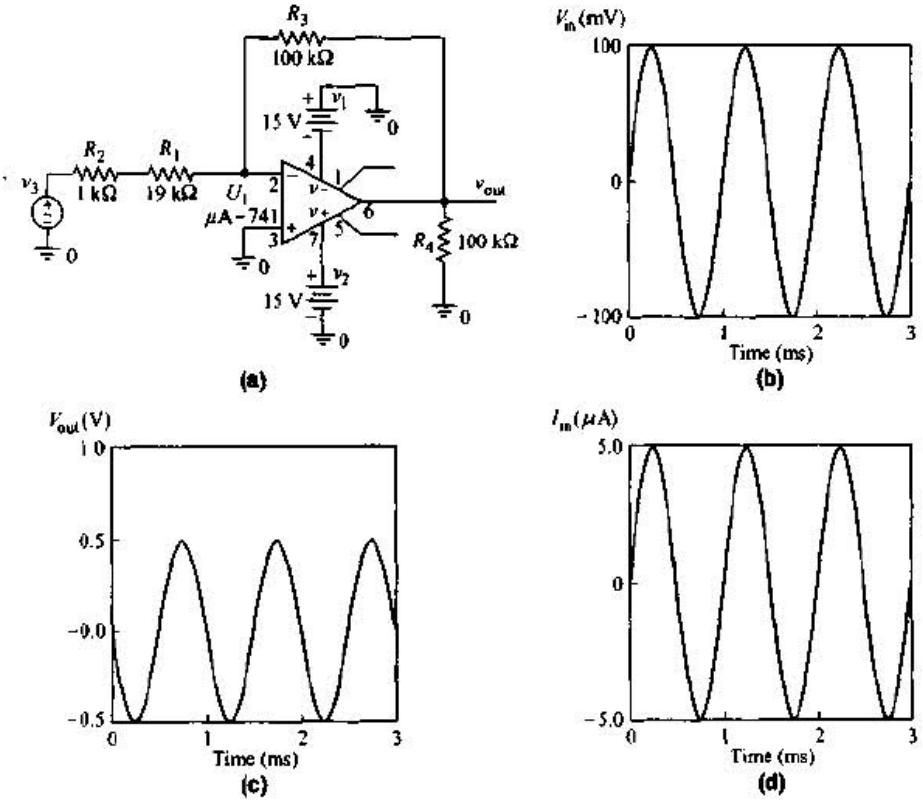

Figure 9.10 (a) PSpice circuit schematic, (b) input signal, (c) output signal, and (d) input current signal for Example 9.1

Problem-Solving Technique: Ideal Op-Amp Circuits

1. If the noninverting terminal of the op-amp is at ground potential, then the inverting terminal is at virtual ground. Sum currents at this node, assuming zero current enters the op-amp itself.
2. If the noninverting terminal of the op-amp is not at ground potential, then the inverting terminal voltage is equal to that at the noninverting terminal. Sum currents at the inverting terminal node, assuming zero current enters the op-amp itself.
3. For the ideal op-amp circuit, the output voltage is determined from either step 1 or step 2 above and is independent of any load connected to the output terminal.

Test Your Understanding

9.1 In the ideal inverting op-amp in Figure 9.9, let $R_1 = 10\,k\Omega$ and $R_2 = 100\,k\Omega$. Determine A_v, v_O, i_1, i_2, and the input resistance when $v_I = 0.25\,V$. (Ans. $A_v = -10$, $v_O = -2.5\,V$, $i_1 = i_2 = 25\,\mu A$, and $R_i = 10\,k\Omega$)

RD9.2 Redesign the ideal inverting op-amp such that the closed-loop voltage gain is $A_v = -15$ and the input resistance is $R_i = 20\,k\Omega$. (Ans. $R_1 = 20\,k\Omega$, $R_2 = 300\,k\Omega$)

9.3 Consider Example 9.1. Suppose the source resistance is not a constant, but varies within the range $0.7k\Omega \leq R_S \leq 1.3\,k\Omega$. Using the results of Example 9.1, what is the range in (a) the voltage gain A_v and (b) the input current i_1. (c) Is the specified maximum input current still maintained? (Ans. (a) $4.926 \leq A_v \leq 5.076$, (b) $4.926 \leq i_1 \leq 5.076\,\mu A$)

9.2.2 Amplifier with a T-Network

Assume that an inverting amplifier is to be designed having a closed-loop voltage gain of $A_v = -100$ and an input resistance of $R_i = R_1 = 50\,k\Omega$. The feedback resistor R_2 would then have to be $5M\Omega$. However this resistance value is too large for most practical circuits.

Consider the op-amp circuit shown in Figure 9.11 with a T-network in the feedback loop. The analysis of this circuit is similar to that of the inverting op-amp circuit of Figure 9.9. At the input, we have

$$i_1 = \frac{v_I}{R_1} = i_2 \tag{9.13}$$

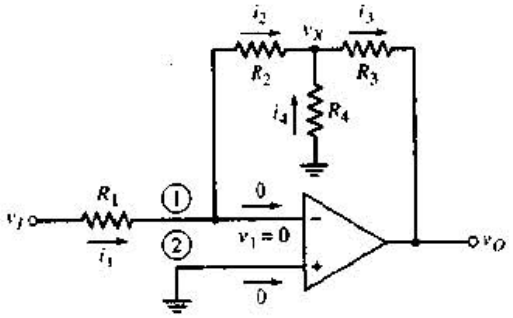

Figure 9.11 Inverting op-amp with T-network

We can also write that

$$v_X = 0 - i_2 R_2 = -v_I\left(\frac{R_2}{R_1}\right) \tag{9.14}$$

If we sum the currents at the node v_X, we have

$$i_2 + i_4 = i_3$$

which can be written

$$-\frac{v_X}{R_2} - \frac{v_X}{R_4} = \frac{v_X - v_O}{R_3} \tag{9.15}$$

or

$$v_X\left(\frac{1}{R_2}+\frac{1}{R_4}+\frac{1}{R_3}\right)=\frac{v_O}{R_3} \tag{9.16}$$

Substituting the expression for v_X from Equation (9.14), we obtain

$$-v_I\left(\frac{R_2}{R_1}\right)\left(\frac{1}{R_2}+\frac{1}{R_4}+\frac{1}{R_3}\right)=\frac{v_O}{R_3} \tag{9.17}$$

The closed-loop voltage gain is therefore

$$A_v=\frac{v_O}{v_I}=-\frac{R_2}{R_1}\left(1+\frac{R_3}{R_4}+\frac{R_3}{R_2}\right) \tag{9.18}$$

The advantage of using a T-network is demonstrated in the following example.

Design Example 9.2 Objective: An op-amp with a T-network is to be used as a preamplifier for a microphone. The maximum microphone output voltage is 12 mV (rms) and the microphone has an output resistance of 1 kΩ.

The op-amp circuit is to be designed such that the maximum output voltage is 1.2 V(rms). The input amplifier resistance should be fairly large, but all resistance values should be less than 500 kΩ.

Solution: We need a voltage gain of

$$|A_v|=\frac{1.2}{0.012}=100$$

Equation (9.18) can be written in the form

$$A_v=-\frac{R_2}{R_1}\left(1+\frac{R_3}{R_4}\right)-\frac{R_3}{R_1}$$

If, for example, we arbitrarily choose $\frac{R_2}{R_1}=\frac{R_3}{R_1}=8$, then

$$-100=-8\left(1+\frac{R_3}{R_4}\right)-8$$

which yields

$$\frac{R_3}{R_4}=10.5$$

The effective R_1 must include the R_S resistance of the microphone. If we set $R_1=49\,\text{k}\Omega$ so that $R_{1\text{eff}}=50\,\text{k}\Omega$, then

$$R_2=R_3=400\,\text{k}\Omega$$

and

$$R_4=38.1\,\text{k}\Omega$$

Comment: As required, all resistor values are less than 500 kΩ. Also the resistance ratios in the closed-loop gain equation are approximately equal. As with most design problems, there is no unique solution.

Design Pointer: If we need to use standard resistance values in our design, then, using Appendix D, we can choose $R_1 = 51\,\text{k}\Omega$ so that $R_{1,\text{eff}} = 52\,\text{k}\Omega$, and we can choose $R_2 = R_3 = 390\,\text{k}\Omega$. Then, using Equation (9.18), we have

$$A_v = -100 = \frac{-R_2}{R_{1,\text{eff}}}\left(1 + \frac{R_3}{R_4}\right) - \frac{R_3}{R_{1,\text{eff}}} = \frac{-390}{52}\left(1 + \frac{390}{R_4}\right) - \frac{390}{52}$$

which yields $R_4 = 34.4\,\text{k}\Omega$. We could, for example, use a $50\,\text{k}\Omega$ potentiometer for R_4 and set the value at $34.4\,\text{k}\Omega$ to produce a gain of 100. The use of a potentiometer will also allow us to adjust the voltage gain of the circuit to take into account tolerance variations in resistor values.

The amplifier with a T-network allows us to obtain a large gain using reasonably sized resistors.

Test Your Understanding

D9.4 Design an ideal inverting op-amp with a T-network that has a closed-loop voltage gain of $A_v = -50$ and an input resistance of $10\,\text{k}\Omega$. All resistors must be no larger than $50\,\text{k}\Omega$. Verify your design with a PSpice analysis. (Ans. For example: $R_1 = 10\,\text{k}\Omega$, $R_2 = R_3 = 50\,\text{k}\Omega$, and $R_4 = 6.25\,\text{k}\Omega$)

9.2.3 Effect of Finite Gain

A **finite open-loop gain** A_{od}, also called the finite differential-mode gain, affects the closed-loop gain of an inverting amplifier. We will consider nonideal effects in op-amps in a later chapter; here, we will determine the magnitude of A_{od} required to approach the ideal case.

Consider the inverting op-amps shown in Figure 9.12. As before, we assume an infinite input resistance at terminals (1) and (2), which means the input currents to the op-amp are zero.

The current through R_1 can be written as

$$i_1 = \frac{v_I - v_1}{R_1} \tag{9.19}$$

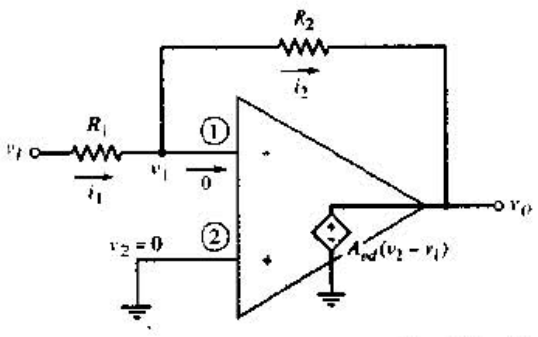

Figure 9.12 Equivalent circuit of the inverting op-amp with a finite differential-mode gain

and the current through R_2 is

$$i_2 = \frac{v_1 - v_O}{R_2} \tag{9.20}$$

The output voltage is now given by

$$v_O = -A_{od} v_1$$

so that the terminal (1) voltage can be written as

$$v_1 = -\frac{v_O}{A_{od}} \tag{9.21}$$

Combining Equations (9.21), (9.19), and (9.20), and setting $i_1 = i_2$, we obtain

$$i_1 = \frac{v_I + \dfrac{v_O}{A_{od}}}{R_1} = i_2 = \frac{-\dfrac{v_O}{A_{od}} - v_O}{R_2} \tag{9.22}$$

Solving for the closed-loop voltage gain, we find that

$$A_v = \frac{v_O}{v_I} = -\frac{R_2}{R_1} \frac{1}{\left[1 + \dfrac{1}{A_{od}}\left(1 + \dfrac{R_2}{R_1}\right)\right]} \tag{9.23}$$

Equation (9.23) shows that if $A_{od} \to \infty$, the ideal closed-loop voltage gain reduces to that given by Equation (9.11).

Example 9.3 **Objective:** Determine the deviation from the ideal due to a finite differential gain.

Consider an inverting op-amp with $R_1 = 10\,\text{k}\Omega$ and $R_2 = 100\,\text{k}\Omega$. Determine the closed-looop gain for: $A_{od} = 10^2$, 10^3, 10^4, 10^5, and 10^6. Calculate the percent deviation from the ideal gain.

Solution: The ideal closed-loop gain is

$$A_v = -\frac{R_2}{R_1} = -\frac{100}{10} = -10$$

If $A_{od} = 10^2$, we have, from Equation (9.3),

$$A_v = -\frac{100}{10} \cdot \frac{1}{\left[1 + \dfrac{1}{10^2}\left(1 + \dfrac{100}{10}\right)\right]} = \frac{-10}{(1 + 0.11)} = -9.01$$

which is a 9.9 percent deviation from the ideal. For the other differential gain values we have the following results:

A_{od}	A_v	Deviation (%)
10^2	−9.01	9.9
10^3	−9.89	1.1
10^4	−9.989	0.11
10^5	−9.999	0.01
10^6	−9.9999	0.001

Comment: For this case, the open-loop gain must be on the order of at least 10^3 in order to be within 1 percent of the ideal gain. If the ideal closed-loop gain changes, a

new value of open-loop gain must be determined in order to meet the specified requirements. As we will see in Chapter 14, at low frequencies, most op-amp circuits have gains on the order of 10^5, so achieving the required accuracy is not difficult.

Test Your Understanding

9.5 An op-amp is ideal, except that its open-loop differential voltage gain is limited to $A_{od} = 10^3$. The voltages at two of the three signal terminals are measured. Determine the voltage at the third signal terminal for: (a) $v_2 = 0$ V and $v_O = 5$ V; (b) $v_1 = 5$ V and $v_O = -10$ V; (c) $v_1 = 0.001$ V and $v_2 = -0.001$ V; (d) $v_2 = 3$ V and $v_O = 3$ V. (Ans. (a) $v_1 = -5$ mV, (b) $v_2 = 4.99$ V, (c) $v_O = -2$ V, and (d) $v_1 = 2.997$ V)

D9.6 An inverting op-amp is ideal, except that the differential voltage gain is finite and is $A_{od} = 5 \times 10^3$. Design the circuit such that the closed-loop voltage gain is $A_v = -12.0$ and the input resistor is $R_1 = 25\,\text{k}\Omega$. Determine the required value of R_2. (Ans. $R_2 = 300.78\,\text{k}\Omega$)

9.3 SUMMING AMPLIFIER

To analyze the op-amp circuit shown in Figure 9.13(a), we will use the superposition theorem and the concept of virtual ground. Using the superposition theorem, we will determine the output voltage due to each input acting alone.

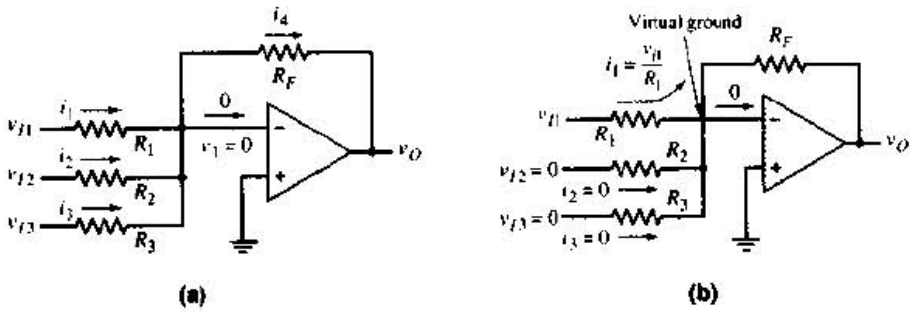

Figure 9.13 (a) Summing op-amp amplifier circuit and (b) currents and voltages in the summing amplifier

We will then algebraically sum these terms to determine the total output.

If we set $v_{I2} = v_{I3} = 0$, the current i_1 is

$$i_1 = \frac{v_{I1}}{R_1} \tag{9.24}$$

Since $v_{I2} = v_{I3} = 0$ and the inverting terminal is at virtual ground, the currents i_2 and i_3 must both be zero. Current i_1 does not flow through either R_2 or R_3, but the entire current must flow through the feedback resistor R_F, as indicated in Figure 9.13(b). The output voltage due to v_{I1} acting alone is

$$v_O(v_{I1}) = -i_1 R_F = -\left(\frac{R_F}{R_1}\right) v_{I1} \tag{9.25}$$

Similarly, the output voltages due to v_{I2} and v_{I3} acting individually are

$$v_O(v_{I2}) = -i_2 R_F = -\left(\frac{R_F}{R_2}\right) v_{I2} \tag{9.26}$$

and

$$v_O(v_{I3}) = -i_3 R_F = -\left(\frac{R_F}{R_3}\right) v_{I3} \tag{9.27}$$

The total output voltage is the algebraic sum of the individual output voltages, or

$$v_O = v_O(v_{I1}) + v_O(v_{I2}) + v_O(v_{I3}) \tag{9.28}$$

which becomes

$$v_O = -\left(\frac{R_F}{R_1} v_{I1} + \frac{R_F}{R_2} v_{I2} + \frac{R_F}{R_3} v_{I3}\right) \tag{9.29}$$

The output voltage is the sum of the three input voltages, with different weighting factors. This circuit is therefore called the **inverting summing amplifier**. The number of input terminals and input resistors can be changed to add more or fewer voltages.

A special case occurs when the three input resistances are equal. When $R_1 = R_2 = R_3 = R$, then

$$v_O = -\frac{R_F}{R}(v_{I1} + v_{I2} + v_{I3}) \tag{9.30}$$

This means that the output voltage is the sum of the input voltages, with a single amplification factor.

Up to this point, we have seen that op-amps can be used to multiply a signal by a constant and sum a number of signals with prescribed weights. These are mathematical operations. Later in the chapter, we will see that op-amps can also be used to integrate and differentiate. These circuits are the building blocks needed to perform analog computations—hence the original name of operational amplifier. Op-amps, however, are versatile and can do much more than just perform mathematical operations, as we will continue to observe through the remainder of the chapter.

Design Example 9.4 **Objective:** Design the summing amplifier to produce a specified output signal.

The output signal generated from a BJT emitter-follower amplifier is $v_{O1} = (5 - 0.5\sin\omega t)$ V and the effective output resistance is $R_o = 50\,\Omega$. Design a summing amplifier such that its output signal is $v_O = 2\sin\omega$ V. One input to the summing amplifier is to be the output of the BJT emitter follower. (Assume that the frequency ω goes very low, making the use of a coupling capacitor impractical.)

Solution: In this case, we only need two inputs to a summing amplifier, as shown in Figure 9.13. We can apply -5 V to one input of the summing amplifier to cancel the $+5$ V from the emitter-follower signal. Assume the input signal v_{I1} is from the emitter follower, the input v_{I2} is -5 V, and $v_{I3} = 0$. If we make $R_1 = 5\,\text{k}\Omega$, then the effect of the

output resistance, $R_o = 50\,\Omega$, can be neglected (to within 1 percent of the ideal). The gain needs to be

$$A_v = \frac{-R_F}{R_1} = \frac{2}{-0.5} = -4$$

The feedback resistor must then be $R_F = 20\,\text{k}\Omega$. We set the input signal $v_{I2} = -5\,\text{V}$ with $R_2 = 5\,\text{k}\Omega$.

Comment: In this example, we have used a summing amplifier to amplify a time-varying signal and eliminate a dc offset voltage.

Test Your Understanding

9.7 Consider an ideal summing amplifier as shown in Figure 9.13(a), with $R_1 = 10\,\text{k}\Omega$, $R_2 = 20\,\text{k}\Omega$, $R_3 = 30\,\text{k}\Omega$, and $R_F = 40\,\text{k}\Omega$. Determine the output voltage v_O if $v_{I1} = 250\,\mu\text{V}$, $v_{I2} = 200\,\mu\text{V}$, and $v_{I3} = 75\,\mu\text{V}$. (Ans. $v_O = -1.5\,\text{mV}$)

D9.8 Design a summing amplifier that will produce an output voltage of $v_O = -(7v_{I1} + 14v_{I2} + 3.5v_{I3} + 10v_{I4})$. The maximum allowable resistance value is $280\,\text{k}\Omega$. (Ans. For example: $R_F = 280\,\text{k}\Omega$, $R_1 = 40\,\text{k}\Omega$, $R_2 = 20\,\text{k}\Omega$, $R_3 = 80\,\text{k}\Omega$, and $R_4 = 28\,\text{k}\Omega$)

D9.9 Design the summing amplifier in Figure 9.13 to produce the average (magnitude) of three input voltages, i.e., $v_O = (v_{I1} + v_{I2} + v_{I3})/3$. The amplifier is to be designed such that each input signal sees the maximum possible input resistance under the condition that the maximum allowed resistance in the circuit is 1 M. (Ans. $R_1 = R_2 = R_3 = 1\,\text{M}\Omega$, $R_F = 333\,\text{k}\Omega$)

9.4 NONINVERTING AMPLIFIER

In our previous discussions, the feedback element was connected between the output and the inverting terminal. However, a signal can be applied to the noninverting terminal while still maintaining negative feedback.

9.4.1 Basic Amplifier

Figure 9.14 shows the basic **noninverting amplifier**. The input signal v_I is applied directly to the noninverting terminal, while one side of resistor R_1 is connected to the inverting terminal and the other side is at ground.

Previously, when v_2 was at ground potential, we argued that v_1 was also essentially at ground potential, and we stated that terminal (1) was at virtual ground. The same principle applies to the circuit in Figure 9.14, with slightly different terminology. The negative feedback connection forces the terminal voltages v_1 and v_2 to be essentially equal. Such a condition is referred to as a **virtual short**. This condition exists since a change in v_2 will cause the output voltage v_O to change in such a way that v_1 is forced to track v_2. The virtual short means that the voltage difference between v_1 and v_2 is, for all practical purposes, zero. However, unlike a true short circuit, there is no current flow

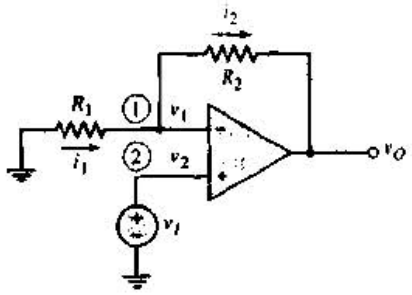

Figure 9.14 Noninverting op-amp circuit

directly from one terminal to the other. We use the virtual short concept, i.e. $v_1 = v_2$, as an ideal op-amp characteristic and use this property in our circuit analysis.

The analysis of the noninverting amplifier is essentially the same as for the inverting amplifier. We assume that no current enters the input terminals. Since $v_1 = v_2$, then $v_1 = v_I$, and current i_1 is given by

$$i_1 = -\frac{v_1}{R_1} = -\frac{v_I}{R_1} \tag{9.31}$$

Current i_2 is given by

$$i_2 = \frac{v_1 - v_O}{R_2} = \frac{v_I - v_O}{R_2} \tag{9.32}$$

As before, $i_1 = i_2$, so that

$$-\frac{v_I}{R_1} = \frac{v_I - v_O}{R_2} \tag{9.33}$$

Solving for the closed-loop voltage gain, we find

$$A_v = \frac{v_O}{v_I} = 1 + \frac{R_2}{R_1} \tag{9.34}$$

From this equation, we see that the output is in phase with the input, as expected. Also note that the gain is always greater than unity.

The input signal v_I is connected directly to the noninverting terminal; therefore, since the input current is essentially zero, the input impedance seen by the source is very large, ideally infinite. The ideal equivalent circuit of the noninverting op-amp is shown in Figure 9.15.

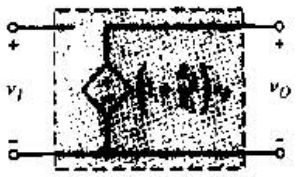

Figure 9.15 Equivalent circuit of ideal noninverting op-amp

9.4.2 Voltage Follower

An interesting property of the noninverting op-amp occurs when $R_1 = \infty$, an open circuit. The closed-loop gain then becomes

$$A_v = \frac{v_O}{v_I} = 1 \tag{9.35}$$

Since the output voltage follows the input, this op-amp circuit is called a **voltage follower**. The closed-loop gain is independent of resistor R_2 (except when $R_2 = \infty$), so we can set $R_2 = 0$ to create a short circuit.

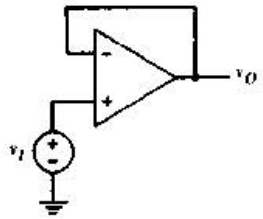

Figure 9.16 Voltage-follower op-amp

The voltage-follower op-amp circuit is shown in Figure 9.16. At first glance, it might seem that this circuit, with unity voltage gain, would be of little value. However, other terms used for the voltage follower are **impedance transformer** or **buffer**. The input impedance is essentially infinite, and the output impedance is essentially zero. If, for example, the output impedance of a signal source is large, a voltage follower inserted between the source and a load will prevent loading effects, that is, it will act as a buffer between the source and the load.

Consider the case of a voltage source with a 100 kΩ output impedance driving a 1 kΩ load impedance, as shown in Figure 9.17(a). This situation may occur if the source is a transducer. (We will see an example of this later in the chapter when we consider a temperature-sensitive resistor, or thermistor, in a bridge circuit.) The ratio of output voltage to input voltage is

$$\frac{v_O}{v_I} = \frac{R_L}{R_L + R_S} = \frac{1}{1 + 100} \cong 0.01$$

This equation indicates that, for this case, there is a severe loading effect, or **attenuation**, in the signal voltage.

Figure 9.17(b) shows a voltage follower inserted between the source and the load. Since the input impedance to the noninverting terminal is usually much greater than 100 kΩ, then $v_O \cong v_I$ and the loading effect is eliminated.

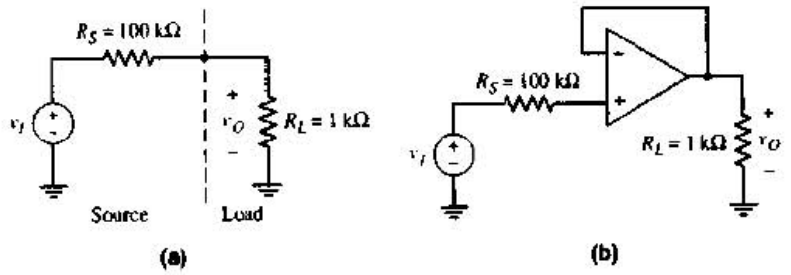

Figure 9.17 (a) Source with a 100 kΩ output resistance driving a 1 kΩ load and (b) source with a 100 kΩ output resistance, voltage follower, and 1 kΩ load

Test Your Understanding

D9.10 Design a noninverting amplifier with a closed-loop gain of $A_v = 5$. The output voltage is limited to $-10\text{ V} \le v_O \le +10\text{ V}$, and the maximum current in any resistor is limited to 50 μA. (Ans. $R_1 = 40\text{ kΩ}$, $R_2 = 160\text{ kΩ}$)

***9.11** The noninverting op-amp in Figure 9.14 has a finite differential gain of A_{od}. Show that the closed-loop gain is

$$A_v = \frac{v_O}{v_I} = \frac{\left(1 + \dfrac{R_2}{R_1}\right)}{\left[1 + \dfrac{1}{A_{od}}\left(1 + \dfrac{R_2}{R_1}\right)\right]}$$

9.12 Use superposition to determine the output voltage v_O in the ideal op-amp circuit in Figure 9.18. (Ans. $v_O = 10v_{I1} + 5v_{I2}$)

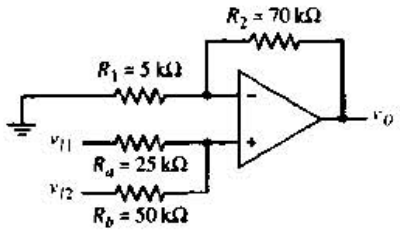

Figure 9.18 Figure for Exercise 9.12

9.5 OP-AMP APPLICATIONS

The summing amplifier is one example of special functional capabilities that can be provided by the op-amp. In this section, we will look at other examples of op-amp versatility.

9.5.1 Current-to-Voltage Converter

In some situations, the output of a device or circuit is a current. An example is the output of a photodiode or photodetector. We may need to convert this output current to an output voltage.

Consider the circuit in Figure 9.19. The input resistance R_i at the virtual ground node is

$$R_i = \frac{v_I}{i_I} \approx 0 \tag{9.36}$$

In most cases, we can assume that $R_S \gg R_i$; therefore, current i_1 is essentially equal to the signal current i_S. Then,

$$i_2 = i_1 = i_S \tag{9.37}$$

and

$$v_O = -i_2 R_F = -i_S R_F \tag{9.38}$$

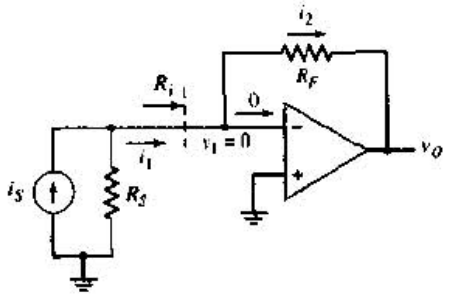

Figure 9.19 Current-to-voltage converter

The output voltage is directly proportional to the signal current, and the feedback resistance R_F is the magnitude of the ratio of the output voltage to the signal current.

Test Your Understanding

D9.13 A current source has an output impedance of $R_S = 100\,\text{k}\Omega$. Design a current-to-voltage converter with an output voltage of $v_O = -10\,\text{V}$ when the signal current is $i_S = 100\,\mu\text{A}$. (Ans. Figure 9.19 with $R_F = 100\,\text{k}\Omega$)

9.5.2 Voltage-to-Current Converter

The complement of the current-to-voltage converter is the voltage-to-current converter. For example, we may want to drive a coil in a magnetic circuit with a given current, using a voltage source. We could use the inverting op-amp shown in Figure 9.20. For this circuit,

$$i_2 = i_1 = \frac{v_I}{R_1} \tag{9.39}$$

which means that current i_2 is directly proportional to input voltage v_I and is independent of the load impedance or resistance R_2. However, one side of the load device might need to be at ground potential, so the circuit in Figure 9.20 would not be practical for such applications.

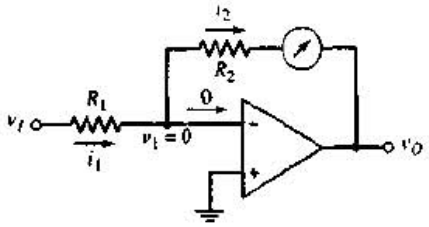

Figure 9.20 Simple voltage-to-current converter

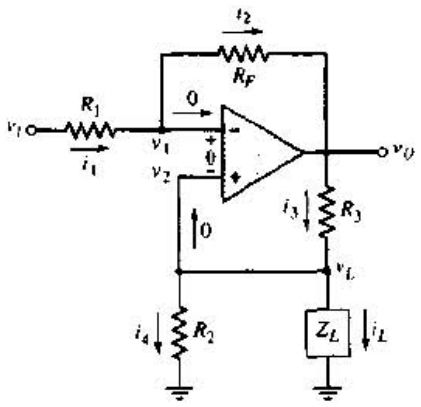

Figure 9.21 Voltage-to-current converter

Consider the circuit in Figure 9.21. In this case, one terminal of the load device, which has an impedance of Z_L, is at ground potential. The inverting terminal (1) is not at virtual ground. From the virtual short concept, $v_1 = v_2$. We also note that $v_1 = v_2 = v_L = i_L Z_L$. Equating the currents i_1 and i_2, we have

$$\frac{v_I - i_L Z_L}{R_1} = \frac{i_L Z_L - v_O}{R_F} \tag{9.40}$$

Summing the currents at the noninverting terminal gives

$$\frac{v_O - i_L Z_L}{R_3} = i_L + \frac{i_L Z_L}{R_2} \tag{9.41}$$

Solving for $(v_O - i_L Z_L)$ from Equation (9.40) and substituting into Equation (9.41) produces

$$\frac{R_F}{R_1} \cdot \frac{(i_L Z_L - v_I)}{R_3} = i_L + \frac{i_L Z_L}{R_2} \tag{9.42}$$

Combining terms in i_L, we obtain

$$i_L\left(\frac{R_F Z_L}{R_1 R_3} - 1 - \frac{Z_L}{R_2}\right) = v_I\left(\frac{R_F}{R_1 R_3}\right) \tag{9.43}$$

In order to make i_L independent of Z_L, we can design the circuit such that the coefficient of Z_L is zero, or

$$\frac{R_F}{R_1 R_3} = \frac{1}{R_2} \tag{9.44}$$

Equation (9.43) then reduces to

$$i_L = -v_I\left(\frac{R_F}{R_1 R_3}\right) = \frac{-v_I}{R_2} \tag{9.45}$$

which means that the load current is proportional to the input voltage and is independent of the load impedance Z_L, as long as the output voltage remains between allowed limits.

We may note that the input resistance seen by the source v_I is finite, and is actually a function of the load impedance Z_L. For a constant i_L, a change in Z_L produces a change in $v_L = v_2 = v_1$, which causes a change in i_1. A voltage follower may be inserted between the voltage source v_I and the resistor R_1 to eliminate any loading effects due to a variable input resistance.

Example 9.5 **Objective:** Determine a load current in a voltage-to-current converter.

Consider the circuit in Figure 9.21. Let $Z_L = 100\,\Omega$, $R_1 = 10\,\text{k}\Omega$, $R_2 = 1\,\text{k}\Omega$, $R_3 = 1\,\text{k}\Omega$, and $R_F = 10\,\text{k}\Omega$. If $v_I = -5\,\text{V}$, determine the load current i_L and the output voltage v_O.

Solution: We note first that the condition expressed by Equation (9.44) is satisfied; that is,

$$\frac{1}{R_2} = \frac{R_F}{R_1 R_3} = \frac{10}{(10)(1)} \rightarrow \frac{1}{1}$$

The load current is

$$i_L = \frac{-v_I}{R_2} = \frac{-(-5)}{1\,\text{k}\Omega} = 5\,\text{mA}$$

and the voltage across the load is

$$v_L = i_L Z_L = (5 \times 10^{-3})(100) = 0.5\,\text{V}$$

Currents i_4 and i_3 are

$$i_4 = \frac{v_L}{R_2} = \frac{0.5}{1} = 0.5\,\text{mA}$$

and

$$i_3 = i_4 + i_L = 0.5 + 5 = 5.5\,\text{mA}$$

The output voltage is then

$$v_O = i_3 R_3 + v_L = (5.5 \times 10^{-3})(10^3) + 0.5 = 6\,\text{V}$$

We could also calculate i_1 and i_2 as

$$i_1 = i_2 = -0.55\,\text{mA}$$

Comment: In this example, we implicitly assume that the op-amp is not in saturation, which means that the applied dc bias voltage must be greater than 6 V. In addition, since currents i_2 (which is negative) and i_3 must be supplied by the op-amp, we are assuming that the op-amp is capable of supplying 6.05 mA.

Computer Verification: The PSpice circuit schematic of the voltage-to-current converter is shown in Figure 9.22(a). The input voltage was varied between 0 and −10 V. Figure 9.22(b) shows the current through the 100 Ω load and Figure 9.22(c) shows the

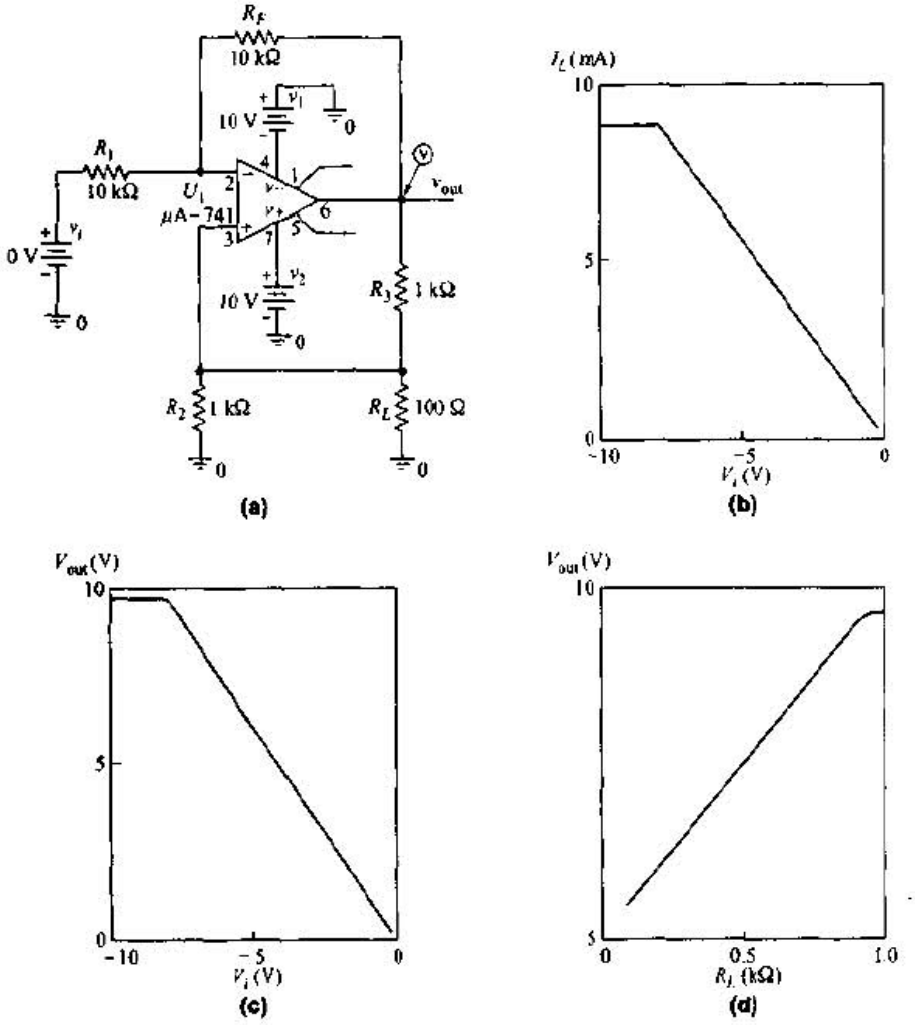

Figure 9.22 (a) PSpice circuit schematic; (b) load current and (c) op-amp output voltage versus input voltage; (d) op-amp output voltage versus load resistance for $v_I = -5$ V

op-amp output voltage as a function of the input voltage. At approximately $v_I = -7.5\,\text{V}$, the op-amp saturates, so the load current and output voltage no longer increase with input voltage. This result demonstrates that the ideal voltage-to-current conversion is valid only if the op-amp is operating in its linear region. Figure 9.22(d) shows the output voltage as a function of load resistance for an input voltage of $v_I = -5\,\text{V}$. At a load resistance greater than approximately $900\,\Omega$, the op-amp saturates. The range over which the op-amp remains linear could be increased by increasing the bias to $\pm 15\,\text{V}$, for example.

Test Your Understanding

9.14 Consider the voltage-to-current converter shown in Figure 9.21. The load impedance is $Z_L = 200\,\Omega$ and the input voltage is $v_I = -3\,\text{V}$. Determine i_L and v_O if $R_1 = 10\,\text{k}\Omega$, $R_2 = 1.5\,\text{k}\Omega$, $R_3 = 3\,\text{k}\Omega$, and $R_F = 20\,\text{k}\Omega$. (Ans. $i_L = 2\,\text{mA}$, $v_O = 7.2\,\text{V}$)

D9.15 Design the voltage-to-current converter shown in Figure 9.21 such that the load current in a $500\,\Omega$ load can be varied between 0 and 1 mA with an input voltage between 0 and $-5\,\text{V}$. Assume the op-amp is biased at $\pm 10\,\text{V}$. (Ans. $R_2 = 5\,\text{k}\Omega$; for example, let $R_3 = 7\,\text{k}\Omega$, $R_1 = 10\,\text{k}\Omega$, $R_F = 14\,\text{k}\Omega$)

9.5.3 Difference Amplifier

An ideal difference amplifier amplifies only the difference between two signals; it rejects any common signals to the two input terminals. For example, a microphone system amplifies an audio signal applied to one terminal of a difference amplifier, and rejects any 60 Hz noise signal or "hum" existing on both terminals. The basic op-amp also amplifies the difference between two input signals. However, we would like to make a difference amplifier, in which the output is a function of the ratio of resistors, as we had for the inverting and noninverting amplifiers.

Consider the circuit shown in Figure 9.23(a), with inputs v_{I1} and v_{I2}. To analyze the circuit, we will use superposition and the virtual short concept. Figure 9.23(b) shows the circuit with input $v_{I2} = 0$. There are no currents in R_3 and R_4; therefore, $v_{2a} = 0$. The resulting circuit is the inverting amplifier previously considered, for which

$$v_{O1} = -\frac{R_2}{R_1} v_{I1} \tag{9.46}$$

Figure 9.23(c) shows the circuit with $v_{I1} = 0$. Since the current into the op-amp is zero, R_3 and R_4 form a voltage divider. Therefore,

$$v_{2b} = \frac{R_4}{R_3 + R_4} v_{I2} \tag{9.47}$$

From the virtual short concept, $v_{1b} = v_{2b}$ and the circuit becomes a noninverting amplifier, for which

$$v_{O2} = \left(1 + \frac{R_2}{R_1}\right) v_{1b} = \left(1 + \frac{R_2}{R_1}\right) v_{2b} \tag{9.48}$$

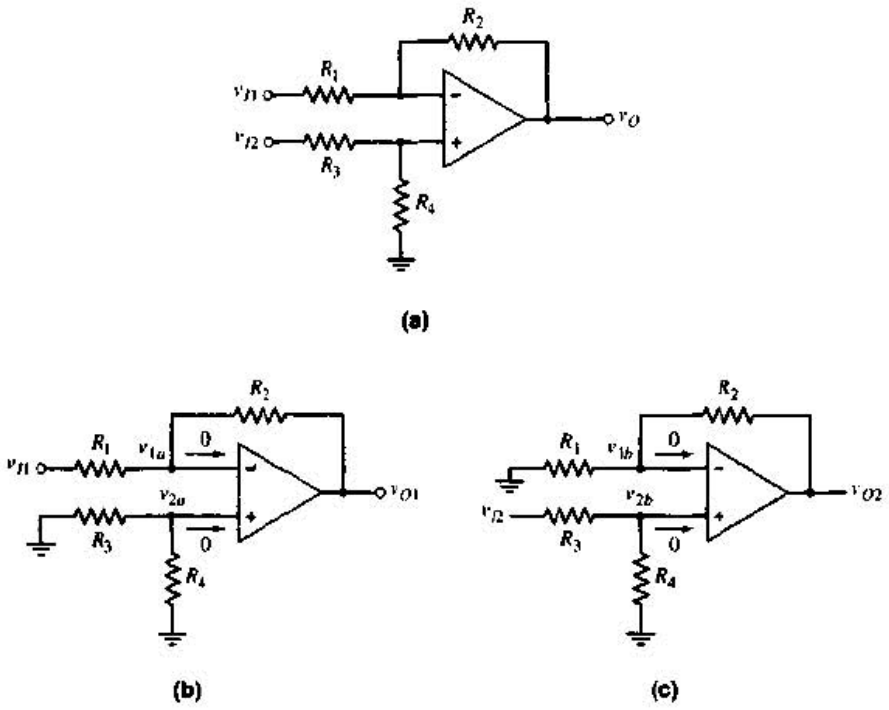

Figure 9.23 (a) Op-amp difference amplifier, (b) difference amplifier with $v_{I2} = 0$ and (c) difference amplifier with $v_{I1} = 0$

Substituting Equation (9.47) into (9.48), we obtain

$$v_{O2} = \left(1 + \frac{R_2}{R_1}\right)\left(\frac{R_4}{R_3 + R_4}\right)v_{I2} \tag{9.49(a)}$$

which can be rearranged as follows:

$$v_{O2} = (1 + R_2/R_1)\left(\frac{R_4/R_3}{1 + R_4/R_3}\right)v_{I2} \tag{9.49(b)}$$

Since the net output voltage is the sum of the individual terms, we have

$$v_O = v_{O1} + v_{O2} \tag{9.50(a)}$$

or

$$v_O = \left(1 + \frac{R_2}{R_1}\right)\left(\frac{\frac{R_4}{R_3}}{1 + \frac{R_4}{R_3}}\right)v_{I2} - \left(\frac{R_2}{R_1}\right)v_{I1} \tag{9.50(b)}$$

A property of the ideal difference amplifier is that the output voltage is zero when $v_{I1} = v_{I2}$. An inspection of Equation (9.50(b)) shows that this condition is met if

$$\frac{R_4}{R_3} = \frac{R_2}{R_1} \tag{9.51}$$

The output voltage is then

$$v_O = \frac{R_2}{R_1}(v_{I2} - v_{I1}) \tag{9.52}$$

which indicates that this amplifier has a differential gain of $A_d = R_2/R_1$. This factor is a closed-loop differential gain, rather than the open-loop differential gain A_{od} of the op-amp itself.

As previously stated, another important characteristic of electronic circuits is the input resistance. The **differential input resistance** of the differential amplifier can be determined by using the circuit shown in Figure 9.24. In the figure, we have imposed the condition given in Equation (9.51) and have set $R_1 = R_3$ and $R_2 = R_4$. The input resistance is then defined as

$$R_i = \frac{V_I}{i} \tag{9.53}$$

Taking into account the virtual short concept, we can write a loop equation, as follows:

$$v_I = iR_1 + iR_1 = i(2R_1) \tag{9.54}$$

Therefore, the input resistance is

$$R_i = 2R_1 \tag{9.55}$$

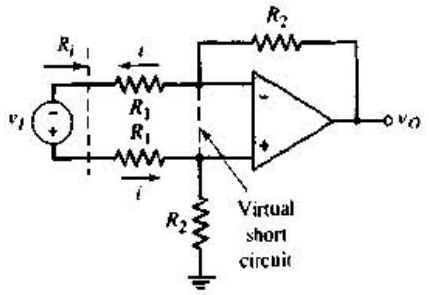

Figure 9.24 Circuit for measuring differential input resistance of op-amp difference amplifier

Design Example 9.6 Objective: Design a difference amplifier with a specified gain and minimum differential input resistance.

Consider the difference amplifier in Figure 9.23(a). Design the circuit such that the differential gain is 30 and the minimum differential input resistance is $R_i = 50\,\text{k}\Omega$.

Solution: From Equation (9.55), the differential input resistance is

$$R_i = 2R_1 = 50\,\text{k}\Omega$$

Therefore,

$$R_1 = R_3 = 25\,\text{k}\Omega$$

Since the differential gain is

$$R_2/R_1 = 30$$

we must have

$$R_2 = R_4 = 750\,\text{k}\Omega$$

Comment: This example illustrates a disadvantage of this difference amplifier design. It cannot achieve both high gain and high input impedance without using extremely large resistance values.

In the ideal difference amplifier, the output v_O is zero when $v_{I1} = v_{I2}$. However, an inspection of Equation (9.50(b)) shows that this condition is not satisfied if $R_4/R_3 \neq R_2/R_1$. When $v_{I1} = v_{I2}$, the input is called a **common-mode input signal**. The common-mode input voltage is defined as

$$v_{cm} = (v_{I1} + v_{I2})/2 \tag{9.56}$$

The common-mode gain is then defined as

$$A_{cm} = \frac{v_O}{v_{cm}} \tag{9.57}$$

Ideally, when a common-mode signal is applied, $v_O = 0$ and $A_{cm} = 0$.

A nonzero common-mode gain may be generated in actual op-amp circuits. This is discussed in Chapter 14.

A figure of merit for a difference amplifier is the **common-mode rejection ratio (CMRR)**, which is defined as the magnitude of the ratio of differential gain to common-mode gain, or

$$\text{CMRR} = \left|\frac{A_d}{A_{cm}}\right| \tag{9.58}$$

Usually, the CMRR is expressed in decibels, as follows:

$$\text{CMRR(dB)} = 20 \log_{10}\left|\frac{A_d}{A_{cm}}\right| \tag{9.59}$$

Ideally, the common-mode rejection ratio is infinite. In an actual differential amplifier, we would like the common-mode rejection ratio to be as large as possible.

Example 9.7 **Objective:** Calculate the common-mode rejection ratio of a difference amplifier.

Consider the difference amplifier shown in Figure 9.23(a). Let $R_2/R_1 = 10$ and $R_4/R_3 = 11$. Determine CMRR(dB).

Solution: From Equation (9.50(b)), we have

$$v_O = (1 + 10)\left(\frac{11}{1 + 11}\right)v_{I2} - (10)v_{I1}$$

or

$$v_O = 10.0833v_{I2} - 10v_{I1} \tag{9.60}$$

The differential-mode input voltage is defined as

$$v_d = v_{I2} - v_{I1}$$

and the common-mode input voltage is defined as

$$v_{cm} = (v_{I1} + v_{I2})/2$$

Combining these two equations produces

$$v_{I1} = v_{cm} - \frac{v_d}{2} \tag{9.61(a)}$$

and

$$v_{I2} = v_{cm} + \frac{v_d}{2} \tag{9.61(b)}$$

If we substitute Equations (9.61(a)) and (9.61(b)) in Equation (9.60), we obtain

$$v_O = (10.0833)\left(v_{cm} + \frac{v_d}{2}\right) - (10)\left(v_{cm} - \frac{v_d}{2}\right)$$

or

$$v_O = 10.042v_d + 0.0833v_{cm} \tag{9.62}$$

The output voltage is also

$$v_O = A_d v_d + A_{cm} v_{cm} \tag{9.63}$$

If we compare Equations (9.62) and (9.63), we see that

$$A_d = 10.042 \quad \text{and} \quad A_{cm} = 0.0833$$

Therefore, from Equation (9.59), the common-mode rejection ratio, is

$$\text{CMRR(dB)} = 20\log_{10}\left(\frac{10.042}{0.0833}\right) = 41.6\,\text{dB}$$

Comment: For good differential amplifiers, typical CMRR values are in the range of 80-100 dB. This example shows how close the ratios R_2/R_1 and R_4/R_3 must be in order to achieve a CMRR value in that range.

Computer Verification: A PSpice analysis was performed on the differential amplifier in this example with a μA-741 op-amp. For input voltages of $v_{I1} = -50\,\text{mV}$ and $v_{I2} = +50\,\text{mV}$, the output voltage is $v_O = 1.0043\,\text{V}$, which gives a differential voltage gain of 10.043. For input voltages of $v_{I1} = v_{I2} = 5\,\text{V}$, the output voltage is $v_O = 0.4153\,\text{V}$, which gives a common-mode voltage gain of $A_{cm} = 0.4153/5 = 0.0831$. The common-mode rejection ratio is then CMRR = 10.043/0.0831 = 120.9 ⇒ 41.6 dB, which agrees with the hand analysis. This result demonstrates that at this point, the nonideal characteristics of the μA-741 op-amp do not affect these results.

Test Your Understanding

D9.16 Design a difference amplifier with a differential input impedance of $R_i = 5\,\text{k}\Omega$, a differential voltage gain of 100, and a common-mode gain of zero. (Ans. $R_1 = 2.5\,\text{k}\Omega$, $R_2 = 250\,\text{k}\Omega$)

***9.17** In the difference amplifier shown in Figure 9.23(a), $R_1 = R_3 = 10\,\text{k}\Omega$, $R_2 = 20\,\text{k}\Omega$, and $R_4 = 21\,\text{k}\Omega$. Determine v_O when: (a) $v_{I1} = +1\,\text{V}$, $v_{I2} = -1\,\text{V}$; and (b) $v_{I1} = v_{I2} = +1\,\text{V}$. (c) Determine the common-mode gain. (d) Determine the CMRR(dB). (Ans. (a) $v_O = -4.032\,\text{V}$, (b) $v_O = 0.0323\,\text{V}$, (c) $A_{cm} = 0.0323$, (d) CMRR(db) = 35.9 dB)

9.5.4 Instrumentation Amplifier

We saw in the last section that it is difficult to obtain a high input impedance and a high gain in a difference amplifier with reasonable resistor values. One solution is to insert a voltage follower between each source and the corresponding input. However, a disadvantage of this design is that the gain of the amplifier cannot easily be changed. We would need to change two resistance values and still maintain equal ratios between R_2/R_1 and R_4/R_3. Optimally, we would like to be able to change the gain by changing only a single resistance value. The circuit in Figure 9.25, called an instrumentation amplifier, allows this flexibility. Note that two noninverting amplifiers, A_1 and A_2, are used as the input stage, and a difference amplifier, A_3 is the second, or amplifying, stage.

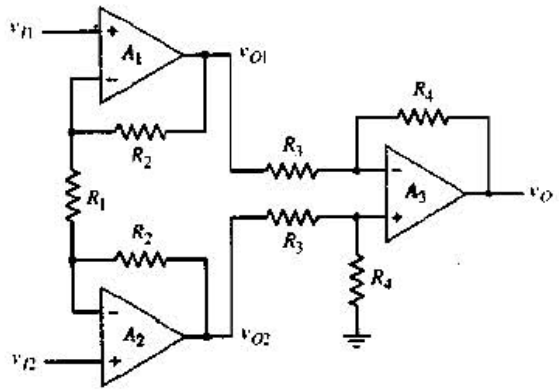

Figure 9.25 Instrumentation amplifier

We begin the analysis using the virtual short concept. The voltages at the inverting terminals of the voltage followers are equal to the input voltages. The currents and voltages in the amplifier are shown in Figure 9.26. The current in resistor R_1 is then

$$i_1 = \frac{v_{I1} - v_{I2}}{R_1} \tag{9.64}$$

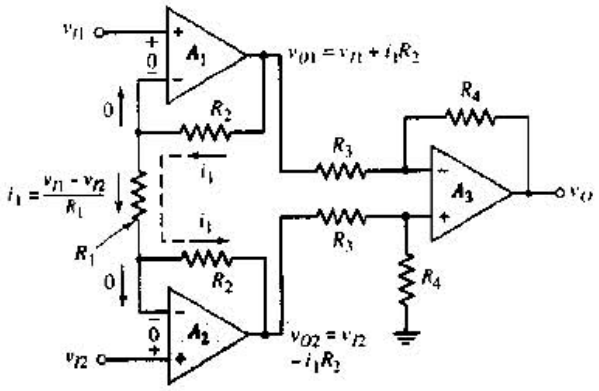

Figure 9.26 Voltages and currents in instrumentation amplifier

The current in resistors R_2 is also i_1, as shown in the figure, and the output voltages of op-amps A_1 and A_2 are, respectively,

$$v_{O1} = v_{I1} + i_1 R_2 = \left(1 + \frac{R_2}{R_1}\right)v_{I1} - \frac{R_2}{R_1}v_{I2} \tag{9.65(a)}$$

and

$$v_{O2} = v_{I2} - i_1 R_2 = \left(1 + \frac{R_2}{R_1}\right)v_{I2} - \frac{R_2}{R_1}v_{I1} \tag{9.65(b)}$$

From previous results, the output of the difference amplifier is given as

$$v_O = \frac{R_4}{R_3}(v_{O2} - v_{O1}) \tag{9.66}$$

Substituting Equations (9.65(a)) and (9.65(b)) into Equation (9.66), we find the output voltage, as follows:

$$v_O = \frac{R_4}{R_3}\left(1 + \frac{2R_2}{R_1}\right)(v_{I2} - v_{I1}) \tag{9.67}$$

Since the input signal voltages are applied directly to the noninverting terminals of A_1 and A_2, the input impedance is very large, ideally infinite, which is one desirable characteristic of the instrumentation amplifier. Also, the differential gain is a function of resistor R_1, which can easily be varied by using a potentiometer, thus providing a variable amplifier gain with the adjustment of only one resistance.

Example 9.8 **Objective:** Determine the range required for resistor R_1, to realize a differential gain adjustable from 5 to 500.

The instrumentation amplifier circuit is shown in Figure 9.25. Assume that $R_4 = 2R_3$, so that the difference amplifier gain is 2.

Solution: Assume that resistance R_1 is a combination of a fixed resistance R_{1f} and a variable resistance R_{1v}, as shown in Figure 9.27. The fixed resistance ensures that the gain is limited to a maximum value, even if the variable resistance is set equal to zero. Assume the variable resistance is a 100 kΩ potentiometer.

From Equation (9.67), the maximum differential gain is

$$500 = 2\left(1 + \frac{2R_2}{R_{1f}}\right)$$

and the minimum differential gain is

$$5 = 2\left(1 + \frac{2R_2}{R_{1f} + 100}\right)$$

From the maximum gain expression, we find that

$$2R_2 = 249R_{1f}$$

Substituting this R_2 value into the minimum gain expression, we have

$$1.5 = \frac{2R_2}{R_{1f} + 100} = \frac{249R_{1f}}{R_{1f} + 100}$$

The resulting value of R_{1f} is $R_{1f} = 0.606\,\text{k}\Omega$, which yields $R_2 = 75.5\,\text{k}\Omega$.

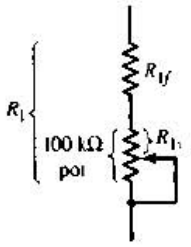

Figure 9.27 Equivalent resistance R_1 in instrumentation amplifier

Comment: We can select standard resistance values that are close to the values calculated, and the range of the gain will be approximately in the desired range.

Test Your Understanding

9.18 For the instrumentation amplifier in Figure 9.25, the parameters are: $R_3 = R_4 = 20\,\text{k}\Omega$, and $R_2 = 100\,\text{k}\Omega$. Resistance R_1 is a series combination of a fixed resistance of 1 kΩ and a 50 kΩ potentiometer. Determine the range of the differential voltage gain. (Ans. $4.92 \le A_d \le 201$)

***9.19** All parameters associated with the instrumentation amplifier in Figure 9.25 are as given in Exercise 9.18, except that resistor R_2 associated with the A_1 op-amp is $R_2 = 100\,\text{k}\Omega \pm 5\%$. (a) Determine the maximum and minimum possible values of the common-mode gain. (b) Determine the maximum and minimum possible values of the differential-mode gain. (c) Determine the minimum CMRR(dB). (Ans. (a) $A_{cm} = 0$, (b) $A_d(\text{min}) = 4.82$, $A_d(\text{max}) = 206$, (c) CMRR = ∞)

D9.20 Design the instrumentation amplifier in Figure 9.25 such that the variable differential voltage gain is in the range of 2 to 1000

9.5.5 Integrator and Differentiator

In the op-amp circuits previously considered, the elements exterior to the op-amp have been resistors. Other elements can be used, with differing results. Figure 9.28 shows a generalized inverting amplifier for which the voltage transfer function has the same general form as before, that is,

$$\frac{v_O}{v_I} = -\frac{Z_2}{Z_1} \tag{9.68}$$

where Z_1 and Z_2 are generalized impedances. Two special circuits can be developed from this generalized inverting amplifier.

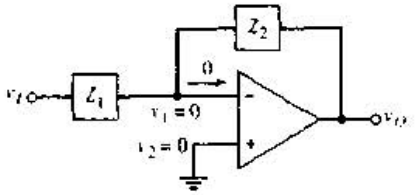

Figure 9.28 Generalized inverting amplifier

In the first, Z_1 corresponds to a resistor and Z_2 to a capacitor. The impedances are then $Z_1 = R_1$ and $Z_2 = 1/sC_2$, where s again is the complex frequency. The output voltage is

$$v_O = -\frac{Z_2}{Z_1}v_I = \frac{-1}{sR_1C_2}v_I \tag{9.69}$$

Equation (9.69) represents integration in the time domain. If V_C is the voltage across the capacitor at $t = 0$, the output voltage is

$$v_O = V_C - \frac{1}{R_1 C_2}\int_0^t v_I(t')dt' \tag{9.70}$$

where t' is the variable of integration. Figure 9.29 summarizes these results.

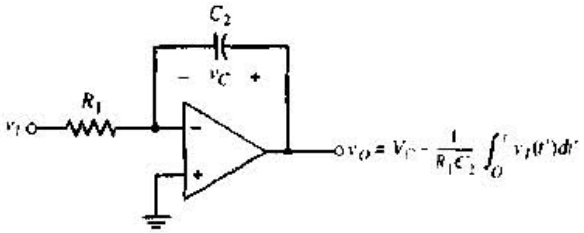

Figure 9.29 Op-amp integrator

Equation (9.70) is the output response of the integrator circuit, shown in Figure 9.29, for any input voltage v_I. Note that if $v_I(t)$ is a finite step function, output v_O will be a linear function of time. The output v_O will be a ramp function and will eventually saturate at a voltage near either the positive or negative supply voltage. We will use the integrator in filter circuits, which are covered in Chapter 15.

We will show in Chapter 14 that nonzero bias currents into the op-amp greatly influence the characteristics of this circuit. A dc current through the capacitor will cause the output voltage to linearly change with time until the positive or negative supply voltage is reached. In many applications, a transistor switch needs to be added in parallel with the capacitor to periodically set the capacitor voltage to zero.

The second generalized inverting op-amp uses a capacitor for Z_1 and a resistor for Z_2, as shown in Figure 9.30. The impedances are $Z_1 = 1/sC_1$ and $Z_2 = R_2$, and the voltage transfer function is

$$\frac{v_O}{v_I} = -\frac{Z_2}{Z_1} = -sR_2C_1 \tag{9.71(a)}$$

The output voltage is

$$v_O = -sR_2C_1v_I \tag{9.71(b)}$$

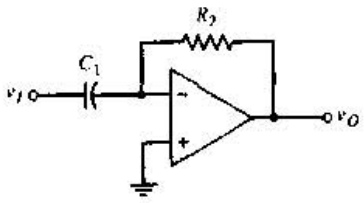

Figure 9.30 Op-amp differentiator

Equation (9.71(b)) represents differentiation in the time domain, as follows:

$$v_O(t) = -R_2C_1\frac{dv_I(t)}{dt} \tag{9.72}$$

The circuit in Figure 9.30 is therefore a differentiator.

Differentiator circuits are more susceptible to noise than are the integrator circuits. Input noise fluctuations of small amplitudes may have large derivatives. When differentiated, these noise fluctuations may generate large noise signals at the output, creating a poor output signal to noise ratio. This problem may be alleviated by placing a resistor in series with the input capacitor. This modified circuit then differentiates low-frequency signals but has a constant high-frequency gain.

Example 9.9 **Objective:** Determine the time constant required in an integrator.

Consider the integrator shown in Figure 9.29. Assume that voltage V_C across the capacitor is zero at $t = 0$. A step input voltage of $v_I = -1\,\text{V}$ is applied at $t = 0$. Determine the time constant required such that the output reaches $+10\,\text{V}$ at $t = 1\,\text{ms}$.

Solution: From Equation (9.70), we have

$$v_o = \frac{-1}{R_1C_2}\int_0^t(-1)dt' = \frac{1}{R_1C_2}t'\Big|_0^t = \frac{t}{R_1C_2}$$

At $t = 1\,\text{ms}$, we want $v_O = 10\,\text{V}$. Therefore,

$$10 = \frac{10^{-3}}{R_1C_2}$$

which means the time constant is $R_1C_2 = 0.1\,\text{ms}$.

Comment: As an example, for a time constant of 0.1 ms, we could have $R_1 = 10\,\text{k}\Omega$ and $C_2 = 0.01\,\mu\text{F}$, which are reasonable values of resistance and capacitance.

Test Your Understanding

9.21 An integrator with input and output voltages that are zero at $t = 0$ is driven by the input signal shown in Figure 9.31. The resistance and capacitance in the circuit are $R_1 = 10\,\text{k}\Omega$ and $C_2 = 0.1\,\mu\text{F}$. Sketch and label the resulting output waveform.

D9.22 An integrator is driven by the series of pulses shown in Figure 9.32. At the end of the tenth pulse, the output voltage is to be $v_O = -5\,\text{V}$. Assume $V_C = 0$ at $t = 0$.

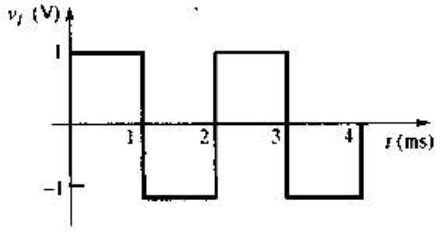

Figure 9.31 Figure for Exercise 9.21

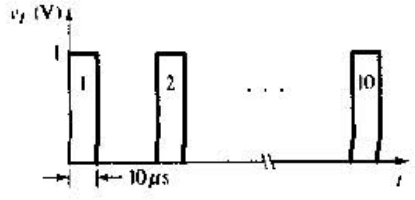

Figure 9.32 Figure for Exercise 9.22

Determine the time constant and values of R_1 and C_2 that will meet these specifications. (Ans. $\tau = 20\,\mu s$; for example, let $C_2 = 0.01\,\mu F$, $R_1 = 2\,k\Omega$)

9.5.6 Nonlinear Circuit Applications

Up to this point in the chapter, we have used linear passive elements in conjunction with the op-amp. Many useful circuits can be fabricated if nonlinear elements, such as diodes or transistors, are used in the op-amp circuits. We will consider three simple examples to illustrate the types of nonlinear characteristics that can be generated and to illustrate the general analysis technique.

Precision Half-Wave Rectifier

An op-amp and diode are combined as shown in Figure 9.33 to form a precision half-wave rectifier. For $v_I > 0$, the circuit behaves as a voltage follower. The output voltage is $v_O = v_I$, the load current i_L is positive, and a positive diode current is induced such that $i_D = i_L$. The feedback loop is closed through the forward-biased diode. The output voltage of the op-amp, v_{O1}, adjusts itself to exactly absorb the forward voltage drop of the diode.

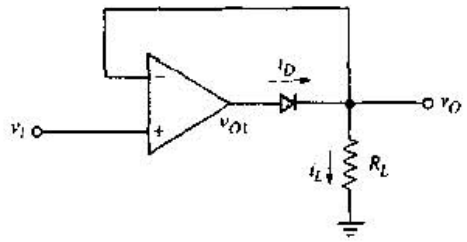

Figure 9.33 Precision half-wave rectifier circuit

For $v_I < 0$, the output voltage tends to go negative, which tends to produce negative load and diode currents. However, a negative diode current cannot exist, so the diode cuts off, the feedback loop is broken, and $v_O = 0$.

The voltage transfer characteristics are shown in Figure 9.34. The rectification is precise in that, even at small positive input voltages, $v_O = v_I$ and we do not observe a diode cut-in voltage.

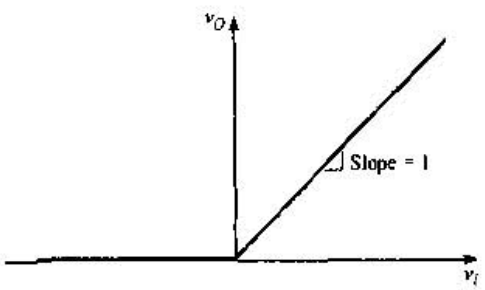

Figure 9.34 Voltage transfer characteristics of precision half-wave rectifier

A potential problem in this circuit exists for $v_I < 0$. The feedback loop is broken so that the op-amp output voltage v_{O1} will saturate near the negative supply voltage. When v_I switches positive, it will take time for the internal circuit to recover, so the response time of the output voltage may be relatively slow. In addition, for $v_I < 0$ and $v_O = 0$, there is now a voltage difference applied across the input terminals of the op-amp. Most op-amps provide input voltage protection so the op-amp will not be damaged in this case. However, if the op-amp does not have input protection, the op-amp may be damaged if the input voltage is larger than 5 or 6 V.

Log Amplifier

Consider the circuit in Figure 9.35. The diode is to be forward biased, so the input signal voltage is limited to positive values. The diode current is

$$i_D = I_S\left(e^{v_D/V_T} - 1\right) \tag{9.73(a)}$$

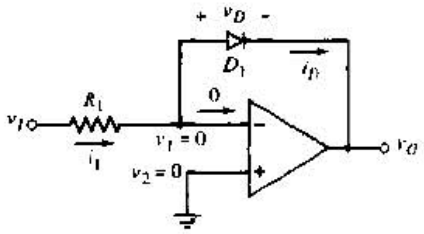

Figure 9.35 Simple log amplifier

If the diode is sufficiently forward biased, the (-1) term is negligible, and

$$i_D \cong I_S e^{v_D/V_T} \tag{9.73(b)}$$

The input current can be written

$$i_1 = \frac{v_I}{R_1} \tag{9.74}$$

and the output voltage, since v_1 is at virtual ground, is given by

$$v_O = -v_D \tag{9.75}$$

Noting that $i_1 = i_D$, we can write

$$i_1 = \frac{v_I}{R_1} = i_D = I_S e^{-v_O/V_T} \tag{9.76}$$

If we take the natural log of both sides of this equation, we obtain

$$\ln\left(\frac{v_I}{I_S R_1}\right) = -\frac{v_O}{V_T} \tag{9.77(a)}$$

or

$$v_O = -V_T \ln\left(\frac{v_I}{I_S R_1}\right) \tag{9.77(b)}$$

Equation (9.77(b)) indicates that, for this circuit, the output voltage is proportional to the log of the input voltage. One disadvantage of this circuit is that the reverse-saturation current I_S is a strong function of temperature, and it varies substantially from one diode to another. A more sophisticated circuit uses bipolar transistors to eliminate the I_S parameter in the log term. This circuit will not be considered here.

Antilog or Exponential Amplifier

The complement, or inverse function, of the log amplifier is the antilog, or exponential, amplifier. A simple example using a diode is shown in Figure 9.36. Since v_1 is at virtual ground, we can write for $v_I > 0$

$$i_D \cong I_S e^{v_I/V_T} \tag{9.78}$$

and

$$v_O = -i_2 R = -i_D R \tag{9.79(a)}$$

or

$$v_O = -I_S R \cdot e^{v_I/V_T} \tag{9.79(b)}$$

The output voltage is an exponential function of the input voltage. Again, there are more sophisticated circuits that perform this function, but they will not be considered here.

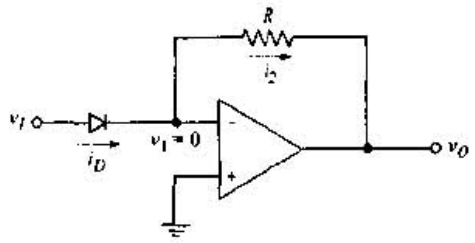

Figure 9.36 A simple antilog, or exponential, amplifier

9.6 OP-AMP CIRCUIT DESIGN

Up to this point, we have mainly been concerned with analyzing op-amp circuits. In this section, we will design three specific circuits.

9.6.1 Summing Op-Amp Circuit Design

In an inverting summing op-amp, each input is connected to the inverting terminal through a resistor. The summing op-amp can be designed such that the output is

$$v_O = -a_1 v_{I1} - a_2 v_{I2} + a_3 v_{I3} + a_4 v_{I4} \tag{9.80}$$

where the coefficients a_i are all positive. In one design, we could apply voltages v_{I3} and v_{I4} to inverter amplifiers and use the summing op-amp considered

previously. This design would require three such op-amps. Alternatively, we could use the results of Exercise 9.12 to design a summing circuit that uses only one op-amp and is more versatile.

Consider the circuit shown in Figure 9.37. Resistor R_C provides more versatility in the design. When we consider nonideal effects, such as bias currents, in op-circuits, in Chapter 14, we will impose a design constraint on the relationship between the resistors connected to the inverting and noninverting terminals. In this section, we will continue to use the ideal op-amp.

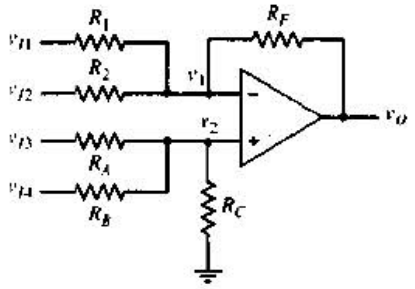

Figure 9.37 Generalized op-amp summing amplifier

To determine the output voltage of our circuit, we use superposition. The inputs v_{I1} and v_{I2} produce the usual outputs, as follows:

$$v_O(v_{I1}) = -\frac{R_F}{R_1} v_{I1} \tag{9.81(a)}$$

and

$$v_O(v_{I2}) = -\frac{R_F}{R_2} v_{I2} \tag{9.81(b)}$$

We then determine the output due to v_{I3}, with all other inputs set equal to zero. We can write

$$v_2(v_{I3}) = \frac{R_B \| R_C}{R_A + R_B \| R_C} v_{I3} = v_1(v_{I3}) \tag{9.82}$$

Since $v_{I1} = v_{I2} = 0$, the voltage $v_2(v_{I3})$ is the input to a noninverting op-amp with R_1 and R_2 in parallel.

Then,

$$v_O(v_{I3}) = (1 + \frac{R_F}{R_1 \| R_2}) v_1(v_{I3}) = \left(1 + \frac{R_F}{R_1 \| R_2}\right)\left(\frac{R_B \| R_C}{R_A + R_B \| R_C}\right) v_{I3} \tag{9.83}$$

which can be rearranged as follows:

$$v_O(v_{I3}) = \left(1 + \frac{R_F}{R_N}\right)\left(\frac{R_P}{R_A}\right) v_{I3} \tag{9.84}$$

Here, we define

$$R_N = R_1 \| R_2 \tag{9.85(a)}$$

and

$$R_P = R_A \| R_B \| R_C \tag{9.85(b)}$$

The output voltage due to v_{I4} is similarly determined and is

$$v_O(v_{I4}) = \left(1 + \frac{R_F}{R_N}\right)\left(\frac{R_P}{R_B}\right)v_{I4} \tag{9.86}$$

The total output voltage is then the sum of the individual terms, or

$$v_O = -\frac{R_F}{R_1}v_{I1} - \frac{R_F}{R_2}v_{I2} + \left(1 + \frac{R_F}{R_N}\right)\left[\frac{R_P}{R_A}v_{I3} + \frac{R_P}{R_B}v_{I4}\right] \tag{9.87}$$

This form of the output voltage is the same as the desired output given by Equation (9.80).

Design Example 9.10 **Objective:** Design a summing op-amp to produce the output

$$v_O = -10v_{I1} - 4v_{I2} + 5v_{I3} + 2v_{I4}$$

The smallest resistor value allowable is 20 kΩ.

Solution: First we determine the values of resistors R_1, R_2, and R_F, and then we can determine the inverting terms. We know that

$$\frac{R_F}{R_1} = 10 \quad \text{and} \quad \frac{R_F}{R_2} = 4$$

Resistor R_1 will be the smallest value, so we can set $R_1 = 20\,\text{k}\Omega$. Then,

$$R_F = 200\,\text{k}\Omega \quad \text{and} \quad R_2 = 50\,\text{k}\Omega$$

The multiplying factor in the noninverting terms becomes

$$\left(1 + \frac{R_F}{R_1 \| R_2}\right) = \left(1 + \frac{200}{20\|50}\right) = 15$$

We then need

$$(15)\left(\frac{R_P}{R_A}\right) = 5 \quad \text{and} \quad (15)\left(\frac{R_P}{R_B}\right) = 2$$

If we take the ratio of these two expressions, we have

$$\frac{R_B}{R_A} = \frac{5}{2}$$

If we choose $R_A = 80\,\text{k}\Omega$, then $R_B = 200\,\text{k}\Omega$, $R_P = 26.67\,\text{k}\Omega$, and R_C becomes $R_C = 50\,\text{k}\Omega$.

Comment: We could change the number of inputs to either the inverting or noninverting terminal, depending on the desired output versus input voltage response.

Test Your Understanding

***D9.23** Design a summing op-amp to produce the output $v_O = v_{I1} + 10v_{I2} - 25v_{I3} - 80v_{I4}$.

9.6.2 Reference Voltage Source Design

In Chapter 2, we discussed the use of Zener diodes to provide a constant or reference voltage source. A limitation, however, was that the reference voltage could never be greater than the Zener voltage. Now, we can combine a Zener diode with an op-amp to provide more flexibility in the design of reference voltage sources.

Consider the circuit shown in Figure 9.38. Voltage source V^+ and resistor R_S bias the Zener diode in the breakdown region. The op-amp is then used as a noninverting amplifier. The output voltage is

$$V_O = \left(1 + \frac{R_2}{R_1}\right) V_Z \tag{9.88}$$

The output current to the load circuit is supplied by the op-amp. A change in the load current will not produce a change in the Zener diode current; consequently, voltage regulation is much improved compared to the simple Zener diode voltage source previously considered.

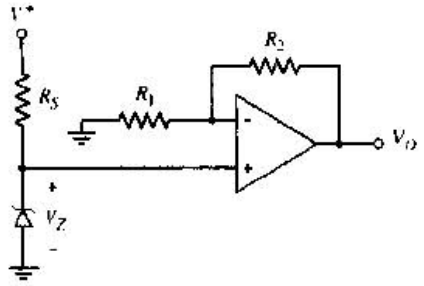

Figure 9.38 Simple op-amp voltage reference circuit

Since the incremental Zener resistance is not zero, the Zener diode voltage is a slight function of the diode current. The circuit shown in Figure 9.39 is less affected by variations in V_S, since V_S is used only to start up the circuit. The Zener diode begins to conduct when

$$\frac{R_4}{R_3 + R_4} V_S > V_Z + V_D \cong V_Z + 0.7 \tag{9.89}$$

At this specific voltage, we have

$$V_O = \left(1 + \frac{R_2}{R_1}\right) V_Z \tag{9.90}$$

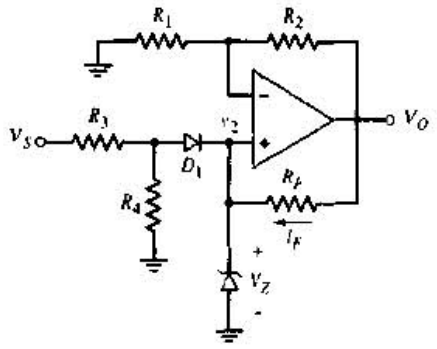

Figure 9.39 Op-amp voltage reference circuit

and

$$I_F = \frac{V_O - V_Z}{R_F} = \frac{R_2 V_Z}{R_1 R_F} \tag{9.91}$$

If V_S decreases and diode D_1 becomes reverse biased, the Zener diode continues to conduct; the Zener diode current is then constant. However, if diode D_1 is conducting, the circuit can be designed such that variations in Zener diode current will be small.

Design Example 9.11 **Objective:** Design a voltage reference source with an output of 10.0 V. Use a Zener diode with a breakdown voltage of 5.6 V. Assume the voltage regulation will be within specifications if the Zener diode is biased between 1 1.2 mA.

Solution: Consider the circuit shown in Figure 9.39. For this example, we need

$$\frac{V_O}{V_Z} = \left(1 + \frac{R_2}{R_1}\right) = \frac{10.0}{5.6}$$

Therefore,

$$\frac{R_2}{R_1} = 0.786$$

We know that

$$I_F = \frac{V_O - V_Z}{R_F}$$

If we set I_F equal to the minimum bias current, we have

$$1\,\text{mA} = \frac{10 - 5.6}{R_F}$$

which means that $R_F = 4.4\,\text{k}\Omega$. If we choose $R_2 = 30\,\text{k}\Omega$, then $R_1 = 38.17\,\text{k}\Omega$.

Resistors R_3 and R_4 can be determined from Figure 9.40. The maximum Zener current supplied by V_S, R_3, and R_4 should be no more than 0.2 mA. We set the current through D_1 equal to 0.2 mA, for $V_S = 10\,\text{V}$. We then have

$$V_2' = V_Z + 0.7 = 5.6 + 0.7 = 6.3\,\text{V}$$

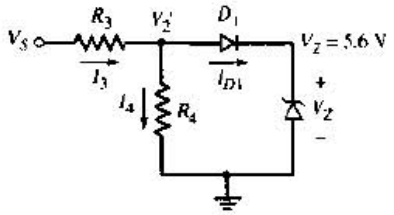

Figure 9.40 Input circuit of the op-amp voltage reference circuit

Also,

$$I_4 = \frac{V_2'}{R_4} = \frac{6.3}{R_4}$$

and

$$I_3 = \frac{V_S - V_2'}{R_3} = \frac{10 - 6.3}{R_3} = \frac{3.7}{R_3}$$

If we set $I_4 = 0.2\,\text{mA}$, then

$$I_3 = 0.4\,\text{mA} \qquad R_3 = 9.25\,\text{k}\Omega \qquad R_4 = 31.5\,\text{k}\Omega$$

Comment: Voltage V_S is used as a start-up source. Once the Zener diode is biased in breakdown, the output will be maintained at 10.0 V, even if V_S is reduced to zero.

Test Your Understanding

9.24 Consider the op-amp voltage reference circuit in Figure 9.39 with parameters given in Example 9.11. Initially set $V_S = 10\,\text{V}$ and then plot, using PSpice, v_O and I_F versus V_S as V_S decreases from 10 to 0 V. Bias the op-amp at ±15 V.

9.6.3 Difference Amplifier and Bridge Circuit Design

A transducer is a device that transforms one form of energy into another form. One type of transducer uses nonelectrical inputs to produce electrical outputs. For example, a microphone converts acoustical energy into electrical energy. A pressure transducer is a device in which, for example, a resistance is a function of pressure, so that pressure can be converted to an electrical signal. Often, the output characteristics of these transducers are measured with a bridge circuit.

Figure 9.41 shows a bridge circuit. Resistance R_3 represents the transducer, and parameter δ is the deviation of R_3 from R_2 due to the input response of the transducer. The output voltage v_{O1} is a measure of δ. If v_{O1} is an open-circuit voltage, then

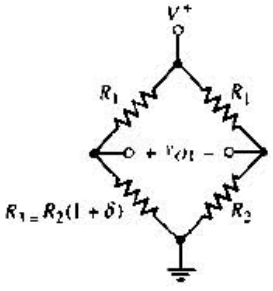

Figure 9.41 Bridge circuit

$$v_{O1} = \left[\frac{R_2(1+\delta)}{R_2(1+\delta)+R_1} - \frac{R_2}{R_1+R_2}\right]V^+ \tag{9.92}$$

which reduces to

$$v_{O1} = \delta\left(\frac{R_1 \| R_2}{R_1+R_2}\right)V^+ \tag{9.93}$$

Since neither side of voltage v_{O1} is at ground potential, we must connect v_{O1} to an instrumentation amplifier. In addition, v_{O1} is directly proportional to supply voltage V^+; therefore, this bias should be a well-defined voltage reference.

Design Example 9.12 **Objective:** Design an amplifier system that will produce an output voltage of ±5 V when the resistance R_3 deviates by ±1% from the value of R_2. This would occur, for example, in a system where R_3 is a thermistor whose resistance is given by

$$R_3 = 200\left[1 + \frac{(0.040)(T - 300)}{300}\right] \text{k}\Omega$$

where T is the absolute temperature. For R_3 to vary by ±1% means the temperature is in the range $225 \leq T \leq 375\,^{\circ}\text{K}$.

Consider biasing the bridge circuit at $V^+ = 7.5$ V using a 5.6 V Zener diode. Assume ±10 V is available for biasing the op-amp and reference voltage source, and that $R_1 = R_2 = 200\,\text{k}\Omega$.

Solution: With $R_1 = R_2$, from Equation (9.93), we have

$$v_{O1} = \left(\frac{\delta}{4}\right)V^+$$

For $V^+ = 7.5$ V and $\delta = 0.01$, the maximum output of the bridge circuit is $v_{O1} = 0.01875$ V. If the output of the amplifier system is to be +5 V, the gain of the instrumentation amplifier must be $5/0.01875 = 266.7$. Consider the instrumentation amplifier shown in Figure 9.25. The output voltage is given by Equation (9.67), which can be written

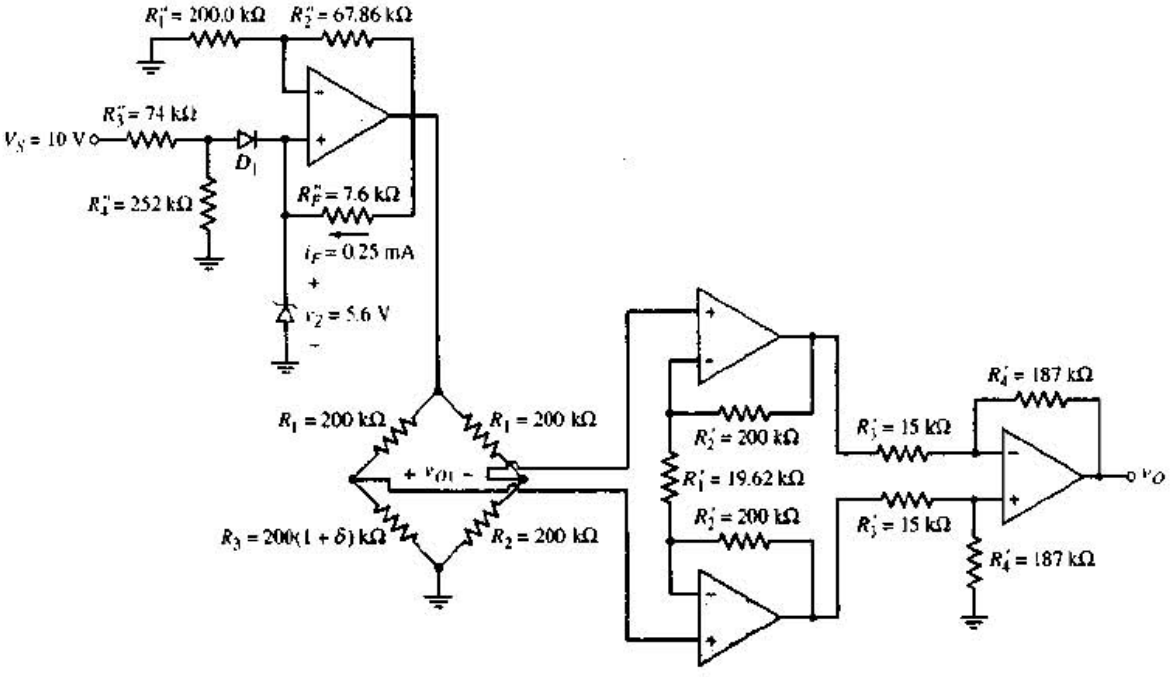

Figure 9.42 Complete amplifier system

$$\frac{v_O}{v_{O1}} = \frac{R_4'}{R_3'}\left(1 + \frac{2R_2'}{R_1'}\right) = 266.7$$

We would like the ratios R_4'/R_3' and R_2'/R_1' to be the same order of magnitude. If we let $R_3' = 15.0\,\text{k}\Omega$ and $R_4' = 187.0\,\text{k}\Omega$, then $R_4'/R_3' = 12.467$ and $R_2'/R_1' = 10.195$. If we set $R_2' = 200.0\,\text{k}\Omega$, then $R_1' = 19.62\,\text{k}\Omega$.

Resistance R_1' can be a combination of a fixed resistance in series with a potentiometer, to permit adjustment of the gain.

Comment: The complete design of this instrumentation amplifier is shown in Figure 9.42. Correlation of the reference voltage source design is left as an exercise.

Design Pointer: The design of fairly sophisticated op-amp circuits is quite straightforward when the ideal op-amp parameters are used.

Test Your Understanding

D9.25 Consider the bridge circuit in Figure 9.43. The resistance is $R = 10\,\text{k}\Omega$ and the maximum ΔR is $50\,\Omega$. The bridge circuit is to be biased with $V^+ = 3.5\,\text{V}$. Design an amplifier system such that the output is 5.0 V when $\Delta R = 50\,\Omega$. Use reasonable resistance values.

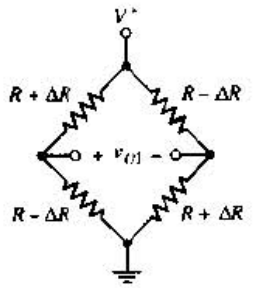

Figure 9.43 Figure for Exercise 9.25

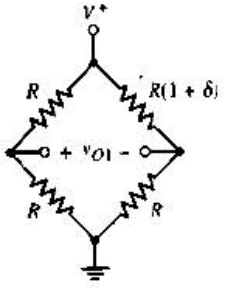

Figure 9.44 Figure for Exercise 9.26

D9.26 Consider the bridge circuit in Figure 9.44. The resistance is $R = 100\,\text{k}\Omega$, and the bridge circuit is to be biased with $V^+ = 5.0\,\text{V}$. Design an amplifier system such that the output varies from +5 V to −5 V as δ varies from +0.01 to −0.01. Use reasonable resistance values.

9.7 SUMMARY

- In this chapter, we considered the ideal operational amplifier (op-amp) and various op-amp applications. The op-amp is a three-terminal device (three signal terminals) that ideally amplifies only the difference between two input signals. The op-amp, then, is a high-gain differential amplifier.
- The ideal op-amp model has infinite input impedance (zero input bias currents), infinite differential voltage gain (zero voltage between the two input terminals), and zero output impedance.
- Two basic op-amp circuits are the inverting amplifier and the noninverting amplifier. In the ideal model of the op-amp, the voltage gain of these circuits is just a function of the ratio of resistors.

- Other amplifier configurations considered were the summing amplifier, voltage follower, current-to-voltage converter, and voltage-to-current converter.
- If a capacitor is included as a feedback element, the output voltage is the integral of the input voltage. If a capacitor is included as an input element, the output voltage is the derivative of the input voltage. Nonlinear feedback elements, such as a diode or transistor, produce nonlinear transfer functions such as a logarithmic function.

CHECKPOINT

After studying this chapter, the reader should have the ability to:

✔ Analyze various op-amp circuits using the ideal op-amp model. (Sections 9.2, 9.3, 9.4, and 9.5)

✔ Analyze various op-amp circuits, taking into account the finite gain of the op-amp. (Section 9.2)

✔ Understand and describe the characteristics and operation of various op-amp circuits, such as the difference amplifier and instrumentation amplifier. (Section 9.5)

✔ Design various op-amp circuits to perform specific functions using the ideal op-amp model. (Section 9.6)

REVIEW QUESTIONS

1. Describe the ideal op-amp model and describe the implications of this ideal model in terms of input currents and voltages.
2. Describe the op-amp model including the effect of a finite op-amp voltage gain.
3. Describe the operation and characteristics of the inverting amplifier.
4. What is the concept of virtual ground?
5. When a finite op-amp gain is taken into account, is the magnitude of the resulting amplifier voltage gain less than or greater than the ideal value?
6. What is the significance of a zero output resistance?
7. Describe the operation and characteristics of a summing amplifier.
8. Describe the operation and characteristics of a noninverting amplifier.
9. Describe a voltage follower.
10. What is the input resistance of an ideal current-to-voltage converter?
11. Describe the operation and characteristics of a difference amplifier.
12. Describe the operation and characteristics of an instrumentation amplifier.

PROBLEMS

Section 9.2 Inverting Amplifier

9.1 Assume the op-amps in Figure P9.1 are ideal. Find the voltage gain $A_v = v_O/v_I$ and the input resistance R_i of each circuit.

9.2 Consider an ideal inverting op-amp with $R_2 = 100\,\text{k}\Omega$ and $R_1 = 10\,\text{k}\Omega$. (a) Determine the ideal voltage gain and input resistance R_i. (b) Repeat part (a) for a second $100\,\text{k}\Omega$ resistor connected in parallel with R_2. (c) Repeat part (a) for a second $10\,\text{k}\Omega$ resistance connected in series with R_1.

D9.3 Design an inverting op-amp circuit with a voltage gain of $A_v = v_O/v_I = -12$ and an input resistance of $R_i = 25\,\text{k}\Omega$.

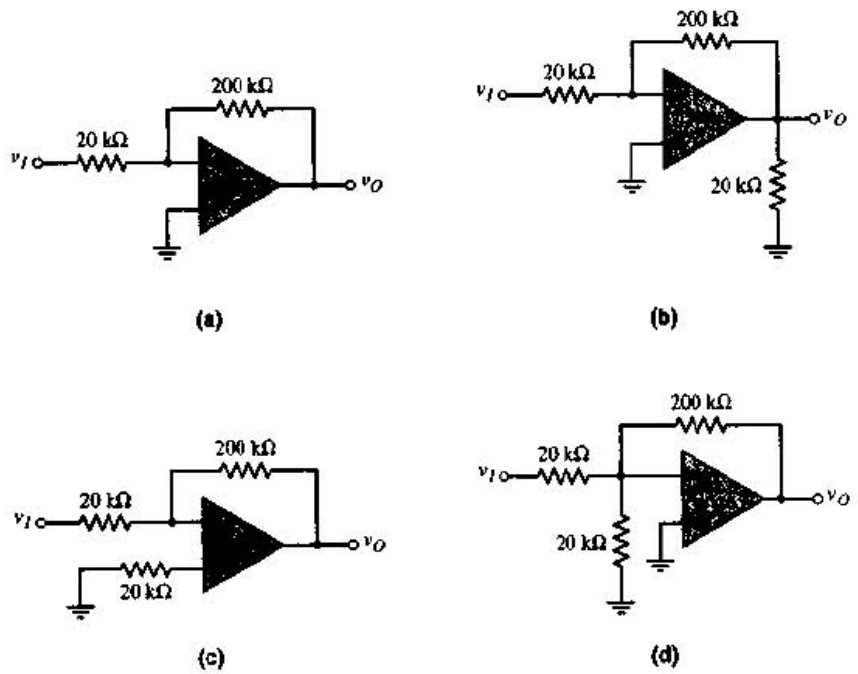

Figure P9.1

D9.4 Design an inverting op-amp circuit with a voltage gain of $A_v = v_O/v_I = -8$. When the input voltage is $v_I = -1$ V, the maximum current in R_1 and R_2 must be no larger than 15 μA. Determine the minimum values of R_1 and R_2.

D9.5 Design an inverting op-amp circuit with a voltage gain of $A_v = v_O/v_I = -30$ and an input resistance that is the largest value possible but under the constraint that the largest resistance value is limited to 1 MΩ.

9.6 (a) In an inverting op-amp circuit, the nominal resistance values are $R_2 = 300\,\text{k}\Omega$ and $R_1 = 15\,\text{k}\Omega$. The tolerance of each resistor is ±5%, which means that each resistance can deviate from its nominal value by ±5%. What is the maximum deviation in the voltage gain from its nominal value? (b) Repeat part (a) if the resistor tolerance is reduced to ±1%.

9.7 The input to the circuit in Figure P9.7 is $v_I = 10 \sin \omega t$ mV. (a) What is the output voltage v_O? (b) Determine the currents i_2, i_L, and i_O.

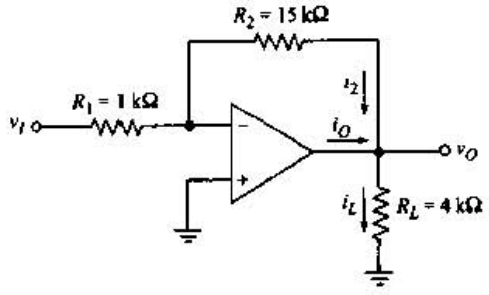

Figure P9.7

D9.8 Design an inverting amplifier to provide a nominal closed-loop voltage gain of $A_v = -30$. The maximum input voltage signal is 25 mV with a source resistance in the range $1\,\text{k}\Omega \le R_S \le 2\,\text{k}\Omega$. The variable source resistance should introduce no more than a 5 percent difference in the gain factor. What is the range in output voltage?

9.9 Consider two inverting op-amp circuits connected in cascade, as shown in Figure P9.9. Let $R_1 = 10\,\text{k}\Omega$, $R_2 = 50\,\text{k}\Omega$, $R_3 = 25\,\text{k}\Omega$, and $R_4 = 150\,\text{k}\Omega$. If $v_I = 0.15$ V, calculate v_{O1}, v_O, i_1, i_2, i_3, and i_4. Discuss the current sum and the current directions at the node v_{O1}.

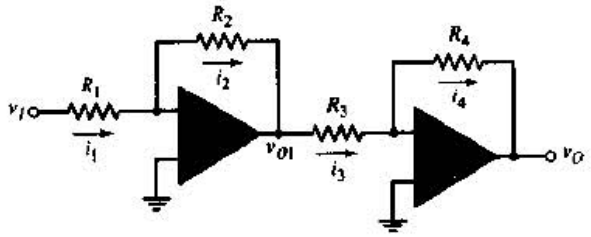

Figure P9.9

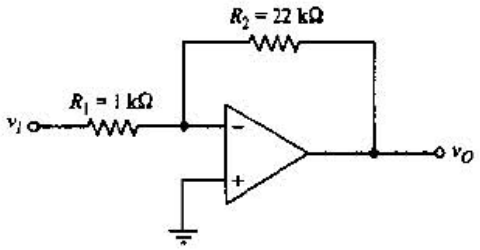

Figure P9.10

***9.10** Consider the circuit shown in Figure P9.10. (a) Determine the ideal voltage gain. (b) Find the actual voltage gain if the open-loop gain is $A_{od} = 150{,}000$. (c) Determine the required valued of A_{od} in order that the actual voltage gain be within 1 percent of the ideal value.

9.11 For the ideal noninverting op-amp with T-network, shown in Figure 9.11, the circuit parameters are $R_1 = R_3 = R_4 = 100\,\text{k}\Omega$. Determine R_2 such that: (a) $A_v = v_O/v_I = -10$, and (b) $A_v = v_O/v_I = -100$.

D9.12 Consider the ideal inverting op-amp circuit with T-network in Figure 9.11. (a) Design the circuit such that the input resistance is $500\,\text{k}\Omega$ and the gain is $A_v = -80$. Do not use resistor values greater than $500\,\text{k}\Omega$. (b) For the design in part (a), determine the current in each resistor if $v_I = -0.05$ V.

9.13 For the op-amp circuit shown in Figure P9.13, determine the gain $A_v = v_O/v_I$. Compare this result to the gain of the circuit shown in Figure 9.11, assuming all resistor values are equal.

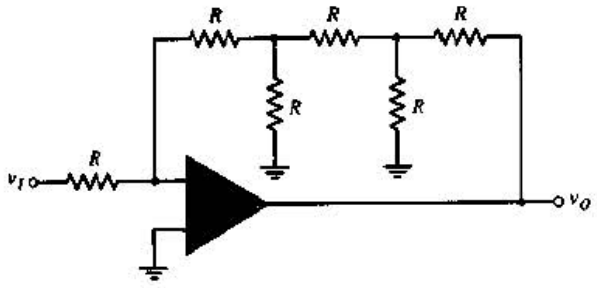

Figure P9.13

***9.14** The inverting op-amp circuit in Figure 9.8 has parameters $R_1 = 10\,\text{k}\Omega$, $R_2 = 50\,\text{k}\Omega$, and $A_{od} = 2 \times 10^5$. The input voltage is from an ideal voltage source whose value is $v_I = 100$ mV. (a) Calculate the closed-loop voltage gain, (b) the output voltage, and (c) the error in the output voltage due to the finite open-loop gain.

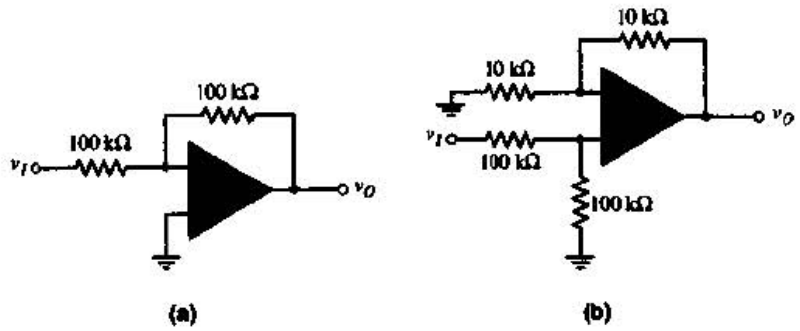

Figure P9.15

***9.15** Consider the two op-amp circuits in Figure P9.15. If the open-loop differential gain for each op-amp is $A_{od} = 10^3$, determine the output voltage v_O when $v_I = 2\,\text{V}$.

***9.16** The circuit in Figure P9.16 is similar to the inverting amplifier except the resistor R_3 has been added. (a) Derive the expression for v_O in terms of v_I and the resistors. (b) Derive the expression for i_3 in terms of v_I and the resistors.

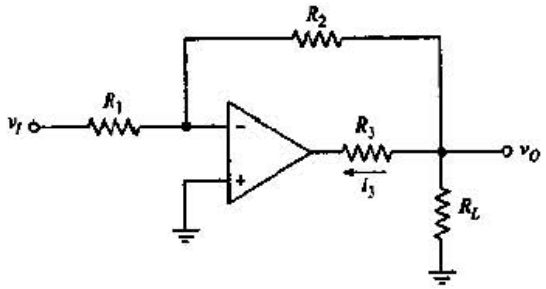

Figure P9.16

***D9.17** Design the amplifier in Figure P9.17 such that the output voltage varies between ±10 V as the wiper arm of the potentiometer changes from −10 V to +10 V. What is the purpose of including R_3 and R_4 instead of connecting R_1 directly to the wiper arm?

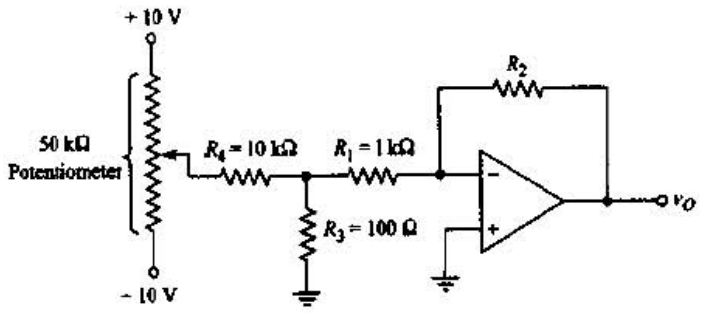

Figure P9.17

9.18 Assume an op-amp is ideal, except for having a finite open-loop differential gain. Measurements were made with the op-amp in the open-loop mode. Determine the open-loop gain and complete the following table, which shows the results of those measurements.

v_1	v_2	v_O
−1 mV	+1 mV	1 V
+1 mV		1 V
	1 V	5 V
−1 V	−1 V	
−0.5 V		−3 V

Section 9.3 Summing Amplifier

9.19 Consider the ideal inverting summing amplifier in Figure 9.13(a). Let $R_1 = 20\,\text{k}\Omega$, $R_2 = 40\,\text{k}\Omega$, $R_3 = 60\,\text{k}\Omega$, and $R_F = 80\,\text{k}\Omega$. (a) Determine v_O if $v_{I1} = 0.5\,\text{V}$, $v_{I2} = -1\,\text{V}$, and $v_{I3} = 2\,\text{V}$. (b) Determine v_{I3} if $v_{I1} = 1\,\text{V}$, $v_{I2} = 0.25\,\text{V}$, and $v_O = -5.2\,\text{V}$.

D9.20 Design an ideal inverting summing amplifier to produce an output voltage of $v_O = -2(4v_{I1} + v_{I2} + 2.5v_{I3})$. Design the circuit to produce the largest possible input resistance, assuming the largest usable resistance value is $500\,\text{k}\Omega$.

D9.21 Design an ideal inverting summing amplifier to produce an output voltage of $v_O = -4v_{I1} - 0.5v_{I2}$. The input voltages are limited to the range $-2 \le v_I \le 2\,\text{V}$, and the current in any resistor is limited to a maximum value of $100\,\mu\text{A}$.

9.22 Consider the summing amplifier in Figure 9.13 with $R_F = 10\,\text{k}\Omega$, $R_1 = 1\,\text{k}\Omega$, $R_2 = 5\,\text{k}\Omega$, and $R_3 = 10\,\text{k}\Omega$. If v_{I1} is a 1 kHz sine wave with an rms value of 50 mV, if v_{I2} is a 100 Hz square wave with an amplitude of $\pm 1\,\text{V}$, and if $v_{I3} = 0$, sketch the output voltage v_O.

9.23 The parameters for the summing amplifier in Figure 9.13 are $R_F = 20\,\text{k}\Omega$, $R_1 = 10\,\text{k}\Omega$, $R_2 = 5\,\text{k}\Omega$, and $R_3 = 2\,\text{k}\Omega$. Determine the voltage v_{I1} to ensure the output voltage is symmetrical about 0 V for $v_{I2} = 2 + 100\sin\omega t$ mV and $v_{I3} = 0$.

9.24 A summing amplifier can be used as a digital-to-analog converter (DAC). An example of a 4-bit DAC is shown in Figure P9.24. When switch S_3 is connected to the −5 V supply, the most significant bit is $a_3 = 1$; when S_3 is connected to ground, the most

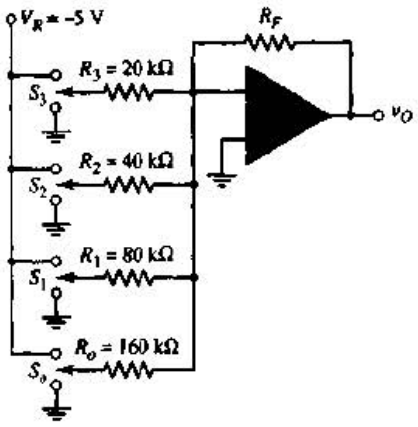

Figure P9.24

significant bit is $a_3 = 0$. The same condition applies to the other switches S_2, S_1, and S_o, corresponding to bits a_2, a_1, and a_o, where a_o is the least significant bit. (a) Show that the output voltage is given by

$$v_O = \frac{R_F}{10}\left[\frac{a_3}{2} + \frac{a_2}{4} + \frac{a_1}{8} + \frac{a_o}{16}\right] \quad (5)$$

where R_F is in kΩ. (b) Find the value of R_F such that $v_O = 2.5$ V when the digital input is $a_3a_2a_1a_o = 1000$. (c) Using the results of part (b), find v_o for: (i) $a_3a_2a_1a_o = 0001$, and (ii) $a_3a_2a_1a_o = 1111$.

9.25 For the circuit in Figure P9.25, (a) derive the expression for v_O in terms of v_{I1} and v_{I2}, and (b) find v_O if $v_{I1} = 1 + 2\sin\omega t$ mV and $v_{I2} = -10$ mV.

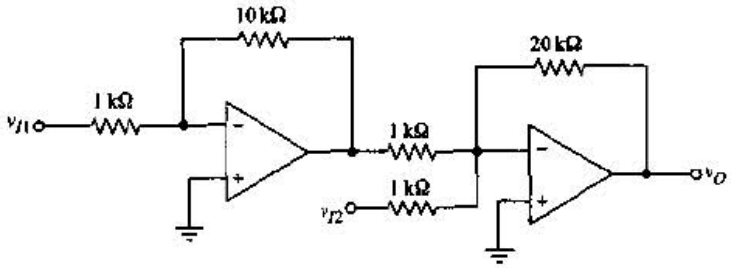

Figure P9.25

***9.26** Consider the summing amplifier in Figure 9.13(a). Assume the op-amp has a finite open-loop differential gain A_{od}. Using the principle of superposition, show that the output voltage is given by

$$v_O = \frac{-1}{1 + \dfrac{(1 + R_F/R_P)}{A_{od}}}\left[\frac{R_F}{R_1}v_{I1} + \frac{R_F}{R_2}v_{I2} + \frac{R_F}{R_3}v_{I3}\right]$$

where $R_P = R_1 \| R_2 \| R_3$. Demonstrate how the expression will change if more or fewer inputs are included.

Section 9.4 Noninverting Amplifier

D9.27 Design an ideal noninverting op-amp with a closed-loop voltage gain of $A_v = 10$. When $v_I = 0.8$ V, the current in any resistor is limited to a maximum of 100 μA.

9.28 For the circuit in Figure P9.28, the input voltage is $v_I = 5$ V. (a) If $v_O = 2.5$ V, determine the finite open-loop differential gain of the op-amp. (b) If the open-loop differential gain of the op-amp is 5000, determine v_O.

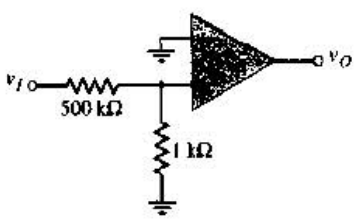

Figure P9.28

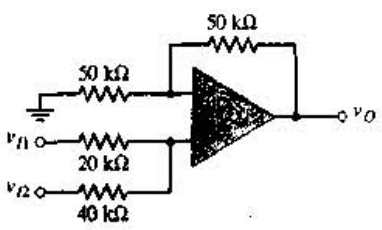

Figure P9.29

9.29 Determine v_O as a function of v_{I1} and v_{I2} for the ideal noninverting op-amp circuit in Figure P9.29.

9.30 Consider the ideal noninverting op-amp in Figure P9.30. Determine v_O as a function of v_{I1} and v_{I2}.

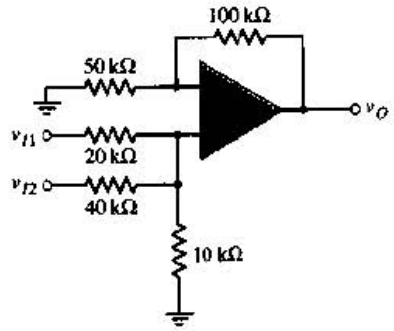

Figure P9.30

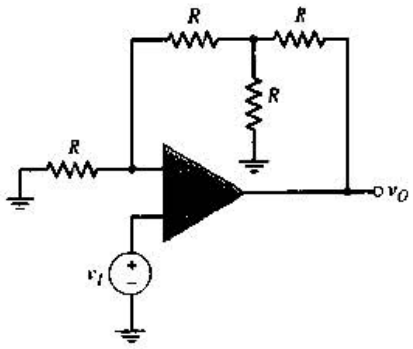

Figure P9.31

9.31 Determine the gain $A_v = v_O/v_I$ for the ideal op-amp circuit in Figure P9.31.

9.32 For the amplifier in Figure P9.32, determine (a) the ideal closed-loop voltage gain, (b) the actual closed-loop voltage gain if the open-loop gain is $A_{od} = 150{,}000$, and (c) the open-loop gain such that the actual closed-loop gain is within 1 percent of the ideal.

9.33 For the voltage follower in Figure 9.16, determine the closed-loop gain if the open-loop differential gain is $A_{od} = 10^4$, 10^3, 10^2, and 10.

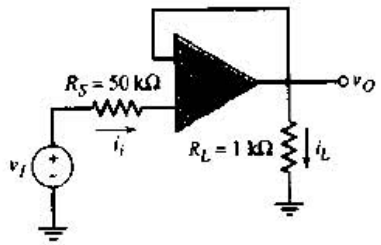

Figure P9.32

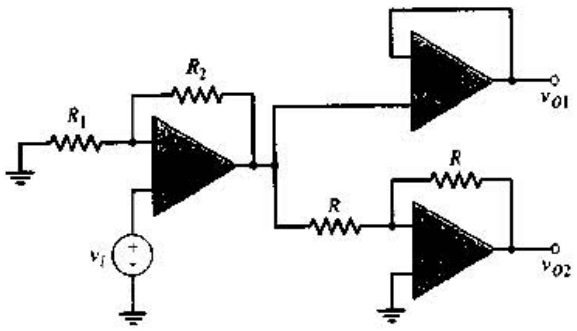

Figure P9.34

9.34 Consider the ideal op-amp circuit shown in Figure P9.34. Determine the voltage gains $A_{v1} = v_{O1}/v_I$ and $A_{v2} = v_{O2}/v_I$. What is the relationship between v_{O1} and v_{O2}?

9.35 (a) Assume the op-amp in the circuit in Figure P9.35 is ideal. Determine i_L as a function of v_I. (b) Let $R_1 = 9\,\text{k}\Omega$ and $R_L = 1\,\text{k}\Omega$. If the op-amp is biased at ± 10 V, determine the maximum value of v_I and i_L before the op-amp saturates.

9.36 The input voltage is $v_I = 6$ V for each ideal op-amp circuit shown in Figure P9.36. Determine each output voltage.

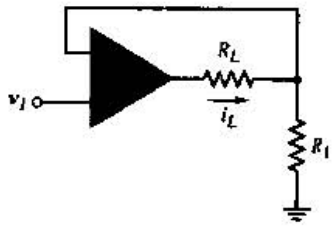

Figure P9.35

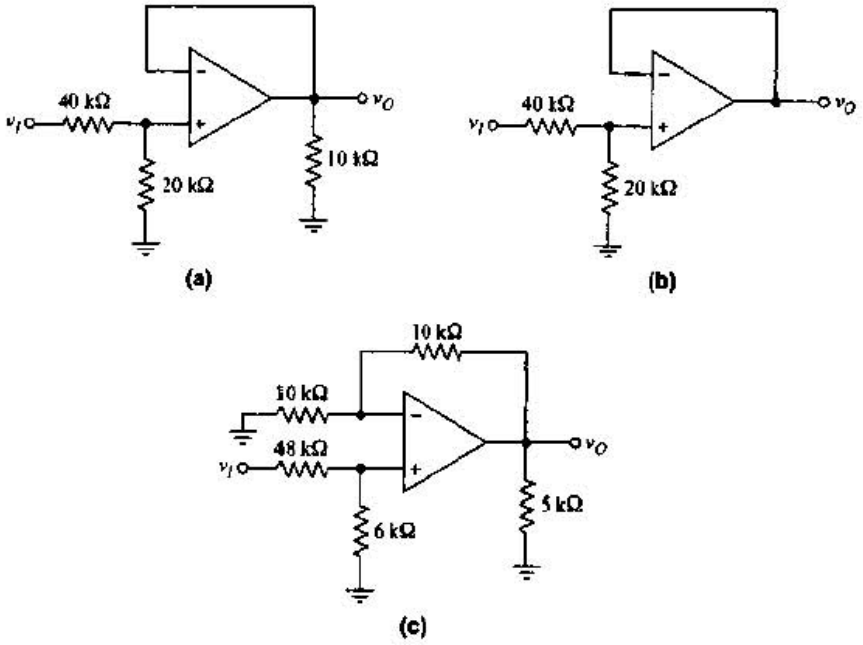

Figure P9.36

Section 9.5 Op-Amp Applications

***9.37** A current-to-voltage converter is shown in Figure P9.37. The current source has a finite output resistance R_S, and the op-amp has a finite open-loop differential gain A_{od}. (a) Show that the input resistance is given by

$$R_{in} = \frac{R_F}{1 + A_{od}}$$

(b) If $R_F = 10\,\text{k}\Omega$ and $A_{od} = 1000$, determine the range of R_S such that the output voltage deviates from its ideal value by less than 1 percent.

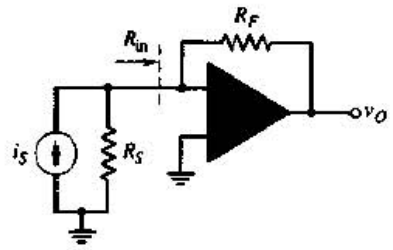

Figure P9.37

***D9.38** Figure P9.38 shows a phototransistor that converts light intensity into an output current. The transistor must be biased as shown. The transistor output versus input characteristics are shown. Design a current-to-voltage converter to produce an output voltage between 0 and 8 V for an input light intensity between 0 and 20 mW/cm^2. Power supplies of +10 V and −10 V are available.

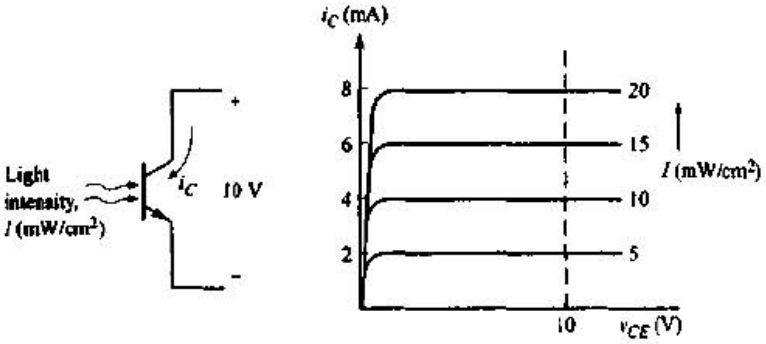

Figure P9.38

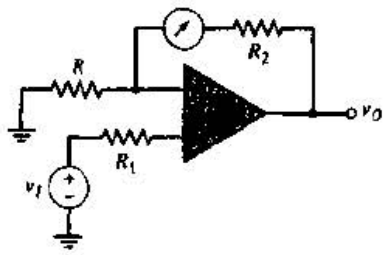

Figure P9.39

D9.39 The circuit in Figure P9.39 is an analog voltmeter in which the meter reading is directly proportional to the input voltage v_I. Design the circuit such that a 1 mA full-scale reading corresponds to $v_I = 10$ V. Resistance R_2 corresponds to the meter resistance, and R_1 corresponds to the source resistance. How do these resistances influence the design?

D9.40 Consider the voltage-to-current converter in Figure 9.21. Design the circuit such that the current in a 100 Ω load can be varied between 0 and 10 mA with an input voltage between 0 and −10 V. Assume the op-amp is biased at ±15 V.

D9.41 The circuit in Figure P9.41 is used to drive an LED with a voltage source. The circuit can also be thought of as a current amplifier in that, with the proper design, $i_D > i_1$. (a) Derive the expression for i_D in terms of i_1 and the resistors. (b) Design the circuit such that $i_D = 12$ mA and $i_1 = 1$ mA for $v_I = 5$ V.

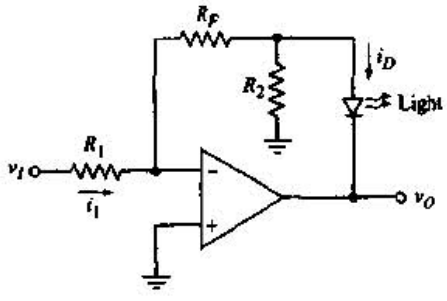

Figure P9.41

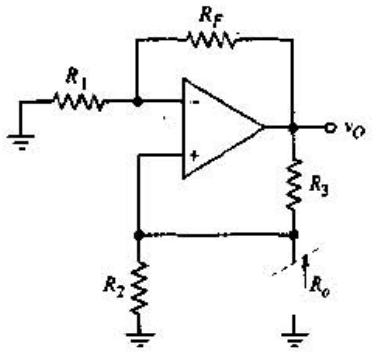

Figure P9.42

***9.42** Figure P9.42 is used to calculate the resistance seen by the load in the voltage-to-current converter given in Figure 9.21. (a) Show that the output resistance is given by

$$R_o = \frac{R_1 R_2 R_3}{R_1 R_3 - R_2 R_F}$$

(b) Using the parameters given in Example 9.5, determine R_o. Is this result unexpected? (c) Consider the design specification given by Equation (9.44). What is the expected value of R_o?

9.43 For the op-amp difference amplifier in Figure 9.23(a), let $R_1 = R_3$ and $R_2 = R_4$. A load resistor $R_L = 5\,\text{k}\Omega$ is connected between v_O and ground. The circuit has a differential voltage gain of $A_d = 5$, and the minimum resistance seen by the signal sources v_{I1} and v_{I2} is $25\,\text{k}\Omega$. If the load current is $i_L = 0.5\,\text{mA}$ when $v_{I1} = 2\,\text{V}$, determine v_{I2}.

***9.44** The circuit in Figure P9.44 is a representation of the common-mode and differential-mode input signals to a difference amplifier. The output voltage can be written as

$$v_O = A_d v_d + A_{cm} v_{cm}$$

where A_d is the differential-mode gain and A_{cm} is the common-mode gain. (a) Setting $v_d = 0$, show that the common-mode gain is given by

$$A_{cm} = \frac{\left(\frac{R_4}{R_3} - \frac{R_2}{R_1}\right)}{(1 + R_4/R_3)}$$

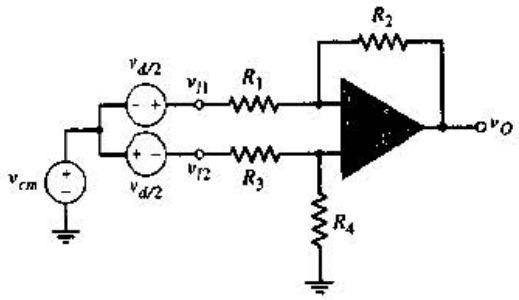

Figure P9.44

(b) If $R_1 = 10\,\text{k}\Omega \pm 5\%$, $R_3 = 10\,\text{k}\Omega \pm 5\%$, $R_2 = 50\,\text{k}\Omega \pm 5\%$, and $R_4 = 50\,\text{k}\Omega \pm 5\%$, determine the maximum value of $|A_{cm}|$.

***9.45** Consider the adjustable gain difference amplifier in Figure P9.45. Variable resistor R_V is used to vary the gain. Show that the output voltage v_O, as a function of v_{I1} and v_{I2}, is given by

$$v_O = \frac{2R_2}{R_1}\left(1 + \frac{R_2}{R_V}\right)(v_{I2} - v_{I1})$$

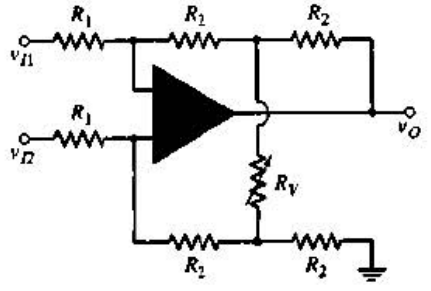

Figure P9.45

9.46 Consider the instrumentation amplifier in Figure 9.25. The circuit parameters are: $R_1 = 10\,\text{k}\Omega$, $R_2 = 50\,\text{k}\Omega$, $R_3 = 20\,\text{k}\Omega$, and $R_4 = 30\,\text{k}\Omega$. Let $v_{I2} = 25\sin\omega t\,\text{mV}$ and $v_{I1} = -25\sin\omega t\,\text{mV}$. Find v_{O1}, v_{O2}, v_O, and the current in each resistor.

9.47 The instrumentation amplifier in Figure 9.25 has the same circuit parameters and input voltages as given in Problem 9.46, except that R_1 is replaced by a fixed resistance R_{1f} in series with a potentiometer, as shown in Figure 9.27. Determine the values of R_{1f} and the potentiometer resistance if the magnitude of the output has a minimum value of $|v_O| = 0.1\,\text{V}$ and a maximum value of $|v_O| = 5\,\text{V}$.

D9.48 Design the instrumentation amplifier in Figure 9.25 to have a variable differential gain in the range 0.5–200. Use a $50\,\text{k}\Omega$ potentiometer.

9.49 All parameters associated with the instrumentation amplifier in Figure 9.25 are the same as given in Exercise 9.18, except that resistor R_3, which is connected to the inverting terminal of A3, is $R_3 = 20\,\text{k}\Omega \pm 5\%$. Determine the maximum common-mode gain.

9.50 For the integrator in Figure 9.29, the circuit parameters are $R_1 = 50\,\text{k}\Omega$ and $C_2 = 0.1\,\mu\text{F}$. The input signal is $v_I = 0.5\sin\omega t\,\text{V}$. (a) At what frequency will the input and output signals have equal amplitudes? At this frequency, what is the phase of the output signal with respect to the input? (b) At what frequency will the output signal amplitude be: (i) $|v_O| = 1\,\text{V}$, and (ii) $|v_O| = 0.1\,\text{V}$?

9.51 For the ideal integrator, the RC time constant is $RC = 200\,\text{ms}$. Assume that the capacitor is initially uncharged. (a) Determine the output voltage 2 seconds after applying a voltage of 0.5 V to the input. (b) How long will it take to reach $-15\,\text{V}$?

9.52 The circuit in Figure P9.52 is a first-order low-pass active filter. (a) Derive the voltage transfer function $A_v = v_O/v_I$ as a function of frequency. (b) What is the voltage gain at dc ($\omega = 0$)? (c) At what frequency is the magnitude of the gain a factor of $\sqrt{2}$ less than the dc value? (This is the $-3\,\text{dB}$ frequency.)

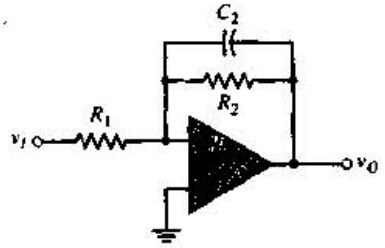

Figure P9.52

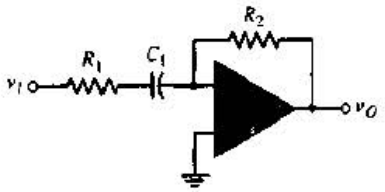

Figure P9.53

9.53 The circuit shown in Figure P9.53 is a first-order high-pass active filter. (a) Derive the voltage transfer function $A_v = v_O/v_I$ as a function of frequency. (b) What is the voltage gain as the frequency becomes large? (c) At what frequency is the magnitude of the gain a factor of $\sqrt{2}$ less than the high-frequency limiting value?

9.54 Consider the voltage reference circuit shown in Figure P9.54. Determine v_O, i_2, and i_Z.

9.55 Consider the circuit in Figure 9.35. The diode parameter is $I_S = 10^{-14}\,\text{A}$ and the resistance is $R_1 = 10\,\text{k}\Omega$. Plot v_O versus v_I over the range $20\,\text{mV} \le v_I \le 2\,\text{V}$. (Plot v_I on a log scale.)

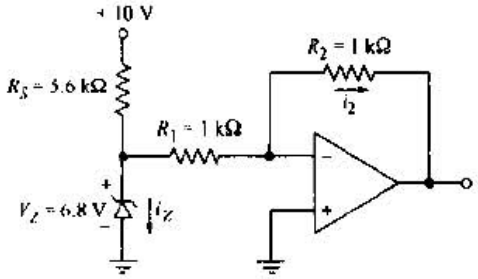

Figure P9.54

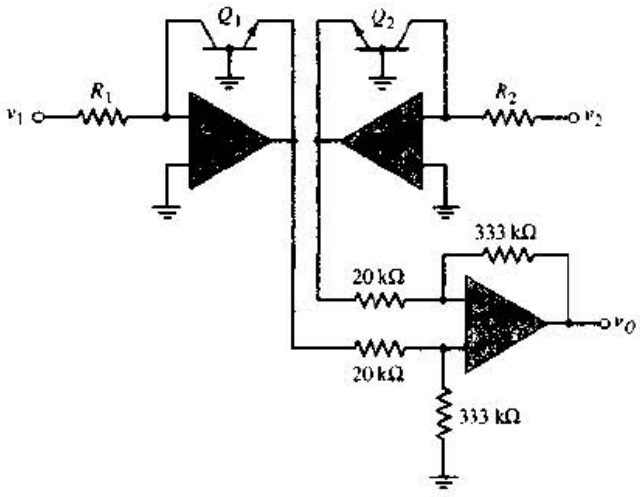

Figure P9.56

***9.56** In the circuit in Figure P9.56, assume that Q_1 and Q_2 are identical transistors. If $T = 300\,^{\circ}\text{K}$, show that the output voltage is

$$v_O = 1.0 \log_{10}\left(\frac{v_2 R_1}{v_1 R_2}\right)$$

9.57 Consider the circuit in Figure 9.36. The diode parameter is $I_S = 10^{-14}\,\text{A}$ and the resistance is $R_1 = 10\,\text{k}\Omega$. Plot v_O versus v_I for $0.30 \le v_I \le 0.60\,\text{V}$. (Plot v_O on a log scale.)

Section 9.6 Op-Amp Circuit Design

***D9.58** Design an op-amp summer to produce the output voltage $v_O = 2v_{I1} - 10v_{I2} + 3v_{I3} - v_{I4}$. Assume the largest resistor value is $500\,\text{k}\Omega$, and the input impedance seen by each source is the largest value possible.

***9.59** Design an op-amp summer to produce the output voltage $v_O = 6v_{I1} + 3v_{I2} + 5v_{I3} - v_{I4} - 2v_{I5}$. The largest resistor value is $250\,\text{k}\Omega$.

***9.60** Design a voltage reference source as shown in Figure 9.39, with an output of 9.0 V, using a Zener diode with a breakdown voltage of 5.6 V. Assume the voltage regulation will be within specifications if the Zener diode is biased between 0.8 and 0.9 mA.

***D9.61** Consider the voltage reference circuit in Figure P9.61. Using a Zener diode with a breakdown voltage of 5.6 V, design the circuit to produce an output voltage of 10 V. Assume the input voltage is 12 V and the Zener diode current is $I_Z = 1\,\text{mA}$.

***D9.62** Consider the bridge circuit in Figure P9.62. The resistor R_T is a thermistor with values of $10\,\text{k}\Omega$ at $T = 300\,^{\circ}\text{K}$ and $12\,\text{k}\Omega$ at $T = 250\,^{\circ}\text{K}$. Assume that the thermistor resistance is linear with temperature, and that the bridge is biased at $V^+ = 10\,\text{V}$. Design an amplifier system with an output of 0 V at $T = 250\,^{\circ}\text{K}$ and 5 V at $T = 300\,^{\circ}\text{K}$.

***D9.63** Consider the bridge circuit in Figure 9.43. Resistance R is $R = 50\,\text{k}\Omega$ and the bias is $V^+ = 10\,\text{V}$. Design an amplifier system such that the output varies from 0 V to 5 V as δ varies from 0 to +0.02.

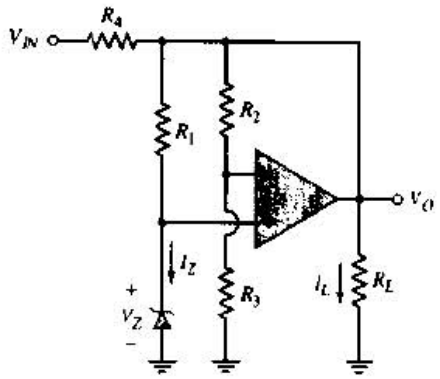

Figure P9.61

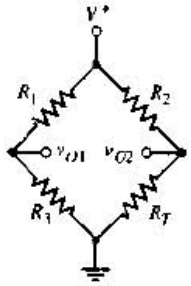

Figure P9.62

COMPUTER SIMULATION PROBLEMS

9.64 Assume the input signal to the op-amp integrator is a 500 Hz square wave with amplitudes of ±0.5 V. Design the integrator such that the steady-state output signal is a triangular wave with peak values of 0 and −5 V. Verify the design with a computer analysis.

9.65 The parameters of the filter circuit in Figure P9.52 are $R_1 = 5\,\text{k}\Omega$, $R_2 = 50\,\text{k}\Omega$, and $C_2 = 0.03\,\mu\text{F}$. Using a computer simulation plot v_O versus frequency over the range $1\,\text{Hz} \leq f \leq 10\,\text{kHz}$. Determine the corner frequency.

9.66 The parameters of the filter circuit shown in Figure P9.53 are $R_1 = 50\,\text{k}\Omega$, $R_2 = 500\,\text{k}\Omega$, and $C_1 = 50\,\text{pF}$. Using a computer simulation, plot v_O versus frequency over the range $10\,\text{kHz} \leq f \leq 10\,\text{MHz}$. Determine the corner frequency.

9.67 Verify that the design given in Example 9.12 meets the specifications.

CHAPTER

10

Integrated Circuit Biasing and Active Loads

10.0 PREVIEW

The biasing techniques in Chapters 3 through 6 for BJT and FET amplifiers for the most part used voltage-divider resistor networks. While this technique can be used for discrete circuits, it is not suitable for integrated circuits. Resistors require relatively large areas on an IC compared to transistors; therefore, a resistor-intensive circuit would necessitate a large chip area. Also, the resistor biasing technique uses coupling and bypass capacitors extensively. On an IC, it is almost impossible to fabricate capacitors in the microfarad range, as would be required for the coupling capacitors.

Biasing transistors and transistor circuits in ICs is considerably different from that in discrete transistor designs. Essentially, biasing integrated circuit amplifiers involves the use of constant-current sources. In this chapter, we will analyze and design both bipolar and FET circuits that form these constant-current sources. We will begin to see for the first time in this chapter the use of matched or identical transistor characteristics as a specific design parameter. Transistors can easily be fabricated in ICs with matched or identical parameters. A principal goal of this chapter is to help the reader understand how matched transistor characteristics are used in design and to be able to design BJT and MOSFET current source circuits.

Transistors are also used as load devices in amplifier circuits. These transistors, called active loads, replace the discrete collector and drain resistors in BJT and FET circuits. Using an active load eliminates resistors from the IC and achieves a higher small-signal voltage gain. The active load is essentially an "upside down" constant-current source, so an initial discussion of active loads is entirely appropriate in this chapter.

10.1 BIPOLAR TRANSISTOR CURRENT SOURCES

As we saw in previous chapters, when the bipolar transistor is used as a linear amplifying device, it must be biased in the forward-active mode. The bias may be a current source that establishes the quiescent collector current as shown in Figure 10.1. We now need to consider the types of circuits that

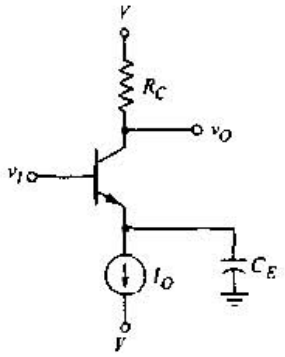

Figure 10.1 Bipolar circuit with current-source biasing

can be designed to establish the bias current I_O. We will discuss a simple two-transistor current-source circuit and then two improved versions of the constant-current source. We will then analyze another current-source circuit, known as the Widlar current source. Finally, we will discuss a multitransistor current source.

10.1.1 Two-Transistor Current Source

The **two-transistor current source**, also called a **current mirror**, is the basic building block in the design of integrated circuit current sources. Figure 10.2(a) shows the basic current-source circuit, which consists of two *matched* or *identical* transistors, Q_1 and Q_2, operating at the same temperature, with their base terminals and emitter terminals connected together. The B–E voltage is therefore the same in the two transistors. Transistor Q_1 is connected as a diode; consequently, when the supply voltages are applied, the B–E junction of Q_1 is forward biased and a reference current I_{REF} is established. Although there

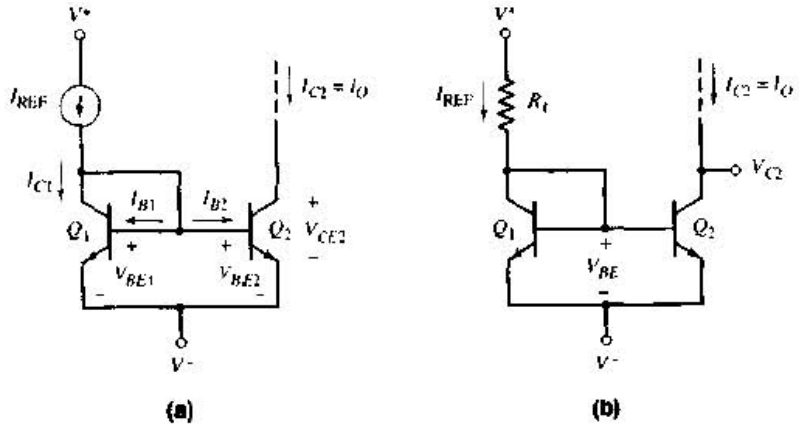

Figure 10.2 (a) Basic two-transistor current source; (b) two-transistor current source with reference resistor R_1

is a specific relationship between I_{REF} and V_{BE1}, we can think of V_{BE1} as being the result of I_{REF}. Once V_{BE1} is established, it is applied to the B–E junction of Q_2. The applied V_{BE2} turns Q_2 on and generates the load current I_O, which is used to bias a transistor or transistor circuit.

The reference current in the two-transistor current source can be established by connecting a resistor to the positive voltage source, as shown in Figure 10.2(b). The reference current is then

$$I_{REF} = \frac{V^+ - V_{BE} - V^-}{R_1} \tag{10.1}$$

where V_{BE} is the B–E voltage corresponding to the collector current, which is essentially equal to I_{REF}.

Connecting the base and collector terminals of a bipolar transistor effectively produces a two-terminal device with I–V characteristics that are identical to the i_C versus v_{BE} characteristic of the BJT. For $v_{CB} = 0$, the transistor is still biased in the forward-active mode, and the base, collector, and emitter currents are related through the current gain β. In constant-current source circuits, β is a dc term that is the ratio of the dc collector current to the dc base current. However, as discussed in Chapter 4, we assume the dc leakage currents are negligible; therefore, the dc beta and ac beta are essentially the same. We do not distinguish between the two values.

Current Relationships

Figure 10.2(a) shows the currents in the two-transistor current source. Since V_{BE} is the same in both devices, and the transistors are identical, then $I_{B1} = I_{B2}$ and $I_{C1} = I_{C2}$. Transistor Q_2 is assumed to be biased in the forward-active region. If we sum the currents at the collector node of Q_1, we have

$$I_{REF} = I_{C1} + I_{B1} + I_{B2} = I_{C1} + 2I_{B2} \tag{10.2}$$

Replacing I_{C1} by I_{C2} and noting that $I_{B2} = I_{C2}/\beta$, Equation (10.2) becomes

$$I_{REF} = I_{C2} + 2\frac{I_{C2}}{\beta} = I_{C2}\left(1 + \frac{2}{\beta}\right) \tag{10.3}$$

The output current is then

$$I_{C2} = I_O = \frac{I_{REF}}{1 + \dfrac{2}{\beta}} \tag{10.4}$$

Equation (10.4) gives the ideal output current of the two-transistor current source, taking into account the finite current gain of the transistors. Implicit in Equation (10.4) is that Q_2 is biased in the forward-active region (the base–collector junction is zero or reverse biased, meaning $V_{CE2} > V_{BE2}$[1]) and the Early voltage is infinite, or $V_A = \infty$. We will consider the effects of a finite Early voltage later in this chapter.

[1] In actual circuits, the collector–emitter voltage may decrease to values as low as 0.2 or 0.3 V, and the circuit will still behave as a constant-current source.

Design Example 10.1 Objective: Design a two-transistor current source to provide a specific output current.

Consider the circuit shown in Figure 10.2(b). The transistor parameters are: $V_{BE}(\text{on}) = 0.6\,\text{V}$, $\beta = 100$, and $V_A = \infty$. The output current is to be $200\,\mu\text{A}$ with $V^+ = 5\,\text{V}$ and $V^- = 0$.

Solution: The reference current can be written as

$$I_{\text{REF}} = I_O\left(1 + \frac{2}{\beta}\right) = (200)\left(1 + \frac{2}{100}\right) = 204\,\mu\text{A}$$

From Equation (10.1), resistor R_1 is found to be

$$R_1 = \frac{V^+ - V_{BE}}{I_{\text{REF}}} = \frac{5 - 0.6}{0.204} = 21.6\,\text{k}\Omega$$

Comment: In this example, we assumed a B–E voltage of 0.6 V. This approximation is satisfactory for many cases in which the B–E voltage is the same for all transistors in the current source. In other cases, we need to determine the B–E voltage corresponding to a particular collector current.

Design Pointer: We see in this example that, for $\beta = 100$, the reference and load currents are within 2 percent of each other in this two-transistor current source. In most circuit applications, we can use the approximation that $I_O \cong I_{\text{REF}}$.

Test Your Understanding

10.1 Consider the two-transistor current source shown in Figure 10.2(b). The circuit parameters are: $V^+ = 10\,\text{V}$, $V^- = 0$, and $R_1 = 15\,\text{k}\Omega$, and the transistor parameters are: $V_{BE}(\text{on}) = 0.7\,\text{V}$, $\beta = 75$, and $V_A = \infty$. Determine I_{REF} and I_O. (Ans. $I_{\text{REF}} = 0.62\,\text{mA}$, $I_O = 0.604\,\text{mA}$)

D10.2 For the current source shown in Figure 10.2(b), the circuit parameters are $V^+ = 5$ and $V^- = -5\,\text{V}$, and the transistor parameters are: $V_{BE}(\text{on}) = 0.7\,\text{V}$, $\beta = 100$, and $V_A = \infty$. Design the circuit such that $I_O = 0.75\,\text{mA}$. What is the value of I_{REF}? (Ans. $I_{\text{REF}} = 0.765\,\text{mA}$, $R_1 = 12.2\,\text{k}\Omega$)

Output Resistance

In our previous analysis, we assumed the Early voltage was infinite, so that $r_O = \infty$. In actual transistors, the Early voltage is finite, which means that the collector current is a function of the collector–emitter voltage. The stability of a load current generated in a constant-current source is a function of the output resistance looking back into the output transistor.

Figure 10.3 shows the dc equivalent circuit of a simple transistor circuit biased with a two-transistor current source. The voltage V_l applied to the base of Q_o is a dc voltage. If the value of V_l changes, the collector–emitter voltage V_{CE2} changes since the B–E voltage of Q_o is essentially a constant. A variation in V_{CE2} in turn changes the output current I_O, because of the Early

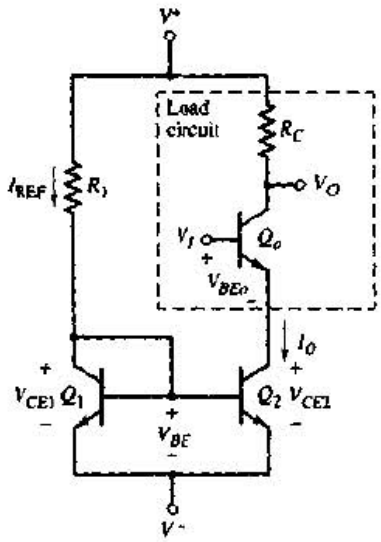

Figure 10.3 The dc equivalent circuit of simple amplifier biased with two-transistor current source

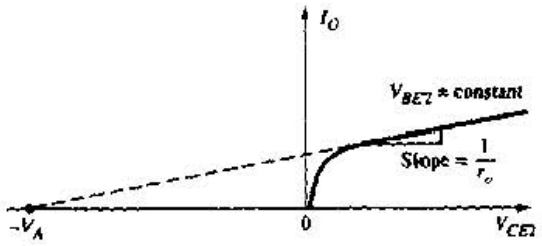

Figure 10.4 Output current versus collector–emitter voltage, showing the Early voltage

effect. Figure 10.4 shows that I_O versus V_{CE2} characteristic at a constant B–E voltage.

The ratio of load current to reference current, taking the Early effect into account, is

$$\frac{I_O}{I_{REF}} = \frac{1}{\left(1+\frac{2}{\beta}\right)} \times \frac{\left(1+\frac{V_{CE2}}{V_A}\right)}{\left(1+\frac{V_{CE1}}{V_A}\right)} \tag{10.5}$$

where V_A is the Early voltage and the factor $(1 + 2/\beta)$ accounts for the finite gain. From the circuit configuration, we see that $V_{CE1} = V_{BE}$, which is essentially a constant.

From Figure 10.3, the collector–emitter voltage of Q_2 can be written

$$V_{CE2} = V_I - V_{BEo} - V^- \tag{10.6}$$

If the dc voltage V_I at the base of Q_o changes, then V_{CE2} changes. A change in the dc bias conditions in the load circuit affects the collector–emitter voltage of Q_2.

The differential change in I_O with respect to a change in V_{CE2}, is, from Equation (10.5),

$$\frac{dI_O}{dV_{CE2}} = \frac{I_{REF}}{\left(1+\frac{2}{\beta}\right)} \times \frac{1}{V_A} \times \frac{1}{\left(1+\frac{V_{BE}}{V_A}\right)} \tag{10.7}$$

If we assume $V_{BE} \ll V_A$, then Equation (10.7) becomes

$$\frac{dI_O}{dV_{CE2}} \cong \frac{I_O}{V_A} = \frac{1}{r_o} \tag{10.8}$$

where r_o is the small-signal output resistance looking into the collector of Q_2.

Example 10.2 **Objective:** Determine the change in load current produced by a change in collector–emitter voltage in a two-transistor current source.

Consider the circuit shown in Figure 10.3. The circuit parameters are: $V^+ = 5\,\text{V}$, $V^- = -5\,\text{V}$, and $R_1 = 9.3\,\text{k}\Omega$. Assume the transistor parameters are: $\beta = 50$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, and $V_A = 80\,\text{V}$. Determine the change in I_O as V_{CE2} changes from 0.7 V to 5 V.

Solution: The reference current is

$$I_{REF} = \frac{V^+ - V_{BE}(\text{on}) - V^-}{R_1} = \frac{5 - 0.7 - (-5)}{9.3} = 1.0\,\text{mA}$$

For $V_{CE2} = 0.7\,\text{V}$, transistors Q_1 and Q_2 are identically biased. From Equation (10.5), we then have

$$I_O = \frac{I_{REF}}{1+\frac{2}{\beta}} = \frac{1.0}{1+\frac{2}{50}} = 0.962\,\text{mA}$$

From Equation (10.8), the small-signal output resistance is

$$r_o = \frac{V_A}{I_O} = \frac{80}{0.962} = 83.2\,\text{k}\Omega$$

The change in load current is determined from

$$\frac{dI_O}{dV_{CE2}} = \frac{1}{r_o}$$

or

$$dI_O = \frac{1}{r_o} dV_{CE2} = \frac{1}{83.2}(5 - 0.7) = 0.052\,\text{mA}$$

The percent change in output current is therefore

$$\frac{dI_O}{I_O} = \frac{0.052}{0.962} = 0.054 \Rightarrow 5.4\%$$

Comment: Although in many circuits a 5 percent change in bias current is insignificant, there are cases, such as digital-to-analog converters, in which the bias current must be held to very tight tolerances. The stability of the load current can be significantly affected by a change in collector–emitter voltage. The stability is a function of the output impedance of the current source.

Test Your Understanding

10.3 Consider the circuit shown in Figure 10.3. The circuit parameters are: $V^+ = 5\,V$, $V^- = -5\,V$, and $R_L = 12\,k\Omega$. The transistor parameters are $\beta = 75$ and $V_{BE}(on) = 0.7\,V$. The percentage change in load current $\Delta I_O/I_O$ must be no more than 2 percent for a change in V_{CE2} from 1 V to 5 V. Determine the minimum required value of Early voltage. (Ans. $V_A \cong 200\,V$)

Mismatched Transistors

In practice, transistors Q_1 and Q_2 may not be exactly identical. If $\beta \gg 1$, we can neglect base currents. The current–voltage relationship for the circuit in Figure 10.2(b) is then

$$I_{REF} \cong I_{C1} = I_{S1} e^{V_{BE}/V_T} \qquad \textbf{(10.9(a))}$$

and

$$I_O = I_{C2} = I_{S2} e^{V_{BE}/V_T} \qquad \textbf{(10.9(b))}$$

Here, we are neglecting the Early effect. The parameters I_{S1} and I_{S2} contain both the electrical and geometric parameters of Q_1 and Q_2. If Q_1 and Q_2 are not identical, then $I_{S1} \neq I_{S2}$.

Combining Equations (10.9(a)) and (10.9(b)), we obtain the relationship between the bias and reference currents, neglecting base currents, as follows:

$$I_O = I_{REF}\left(\frac{I_{S2}}{I_{S1}}\right) \qquad \textbf{(10.10)}$$

Any deviation in bias current from the ideal, as a function of mismatch between Q_1 and Q_2, is directly related to the ratio of the reverse-saturation currents I_{S1} and I_{S2}. The parameter I_S is a strong function of temperature. The temperatures of Q_1 and Q_2 must be the same in order for the circuit to operate properly. Therefore, Q_1 and Q_2 must be close to one another on the semiconductor chip. If Q_1 and Q_2 are not maintained at the same temperature, then the relationship between I_O and I_{REF} is a function of temperature, which is undesirable.

Also, the parameters I_{S1} and I_{S2} are functions of the cross-sectional area of the B–E junctions. Therefore, we can use Equation (10.10) to our advantage. By using different sizes of transistors, we can design the circuit such that $I_O \neq I_{REF}$. This is discussed further later in this chapter.

10.1.2 Improved Current-Source Circuits

In many IC designs, critical current-source characteristics are the changes in bias current with variations in β and with changes in the output transistor collector voltage. In this section, we will look at two constant-current circuits that have improved load current stability against changes in β and changes in output collector voltage.

Basic Three-Transistor Current Source

A basic three-transistor current source is shown in Figure 10.5. We again assume that all transistors are identical; therefore, since the B–E voltage is the same for Q_1 and Q_2, $I_{B1} = I_{B2}$ and $I_{C1} = I_{C2}$. Transistor Q_3 supplies the base currents to Q_1 and Q_2, so these base currents should be less dependent on the reference current. Also, since the current in Q_3 is substantially smaller than that in either Q_1 or Q_2, we expect the current gain of Q_3 to be less than those of Q_1 and Q_2. We define the current gains of Q_1 and Q_2 as $\beta_1 = \beta_2 \equiv \beta$, and the current gain of Q_3 as β_3. Summing the currents at the collector node of Q_1, we obtain

$$I_{\text{REF}} = I_{C1} + I_{B3} \tag{10.11}$$

Since

$$I_{B1} = I_{B2} = 2I_{B2} = I_{E3} \tag{10.12}$$

and

$$I_{E3} = (1 + \beta_3)I_{B3} \tag{10.13}$$

then combining Equations (10.11), (10.12), and (10.13) produces

$$I_{\text{REF}} = I_{C1} + \frac{I_{E3}}{(1 + \beta_3)} = I_{C1} + \frac{2I_{B2}}{(1 + \beta_3)} \tag{10.14}$$

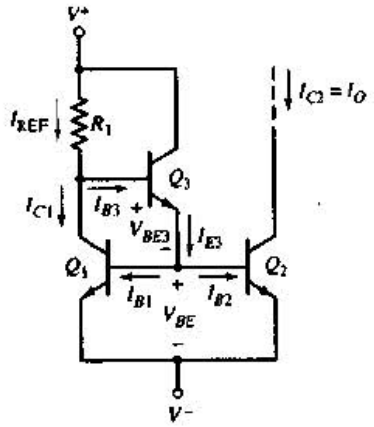

Figure 10.5 Basic three-transistor current source

Replacing I_{C1} by I_{C2} and noting that $I_{B2} = I_{C2}/\beta$, we can rewrite Equation (10.14) as

$$I_{\text{REF}} = I_{C2} + \frac{2I_{C2}}{\beta(1 + \beta_3)} = I_{C2}\left[1 + \frac{2}{\beta(1 + \beta_3)}\right] \tag{10.15}$$

The output or bias current is then

$$I_{C2} = I_O = \frac{I_{\text{REF}}}{\left[1 + \dfrac{2}{\beta(1 + \beta_3)}\right]} \tag{10.16}$$

The reference current is given by

$$I_{REF} = \frac{V^+ - V_{BE3} - V_{BE} - V^-}{R_1} \cong \frac{V^+ - 2V_{BE} - V^-}{R_1} \tag{10.17}$$

As a first approximation, we usually assume that the B–E voltage of Q_3 and Q_1 are equal, as indicated in Equation (10.17).

A comparison of Equation (10.16) for the three-transistor current source and Equation (10.4) for the two-transistor current source shows that the approximation of $I_O \cong I_{REF}$ is better for the three-transistor circuit. In addition, as we will see in the following example, the change in load current with a change in β is much smaller in the three-transistor current source.

Example 10.3 **Objective:** Compare the variation in bias current between the two- and three-transistor current-source circuits as a result of variations in β. A PSpice analysis is used.

Figure 10.6(a) shows the two-transistor PSpice circuit schematic and Figure 10.6(b) shows the three-transistor PSpice circuit schematic used in this analysis.

Solution: In both circuits, the current gain β of all transistors was assumed to be equal, but the actual value was varied between 20 and 200. Since the change in β is very large, we cannot use derivatives to determine the changes in bias currents. Standard 2N3904 transistors were used, which means that the Early voltage is 74 V, and not infinite as in the ideal circuit. The Early voltage will influence the actual value of bias current, but has very little effect in terms of the change in bias current with a change in current gain.

Figure 10.6(c) shows the bias current versus current gain for both the two-transistor and three-transistor current-source circuits.

Comment: There is a significant decrease in the variation in bias current for the three-transistor circuit compared to that of the two-transistor circuit. For values of β greater than approximately 50, there is no perceptible change in bias current for the three-transistor current mirror

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The output resistance looking into the collector of the output transistor Q_2 of the basic three-transistor current source shown in Figure 10.5 is the same as that of the two-transistor current source; that is,

$$\frac{dI_O}{dV_{CE2}} = \frac{1}{r_{o2}} \tag{10.18}$$

This means that, in the three-transistor current source, the change in bias current I_O with a change in V_{CE2} is the same as that in the two-transistor current-source circuit. In addition, any mismatch between Q_1 and Q_2 produces a deviation in the bias current from the ideal, as given by Equation (10.10).

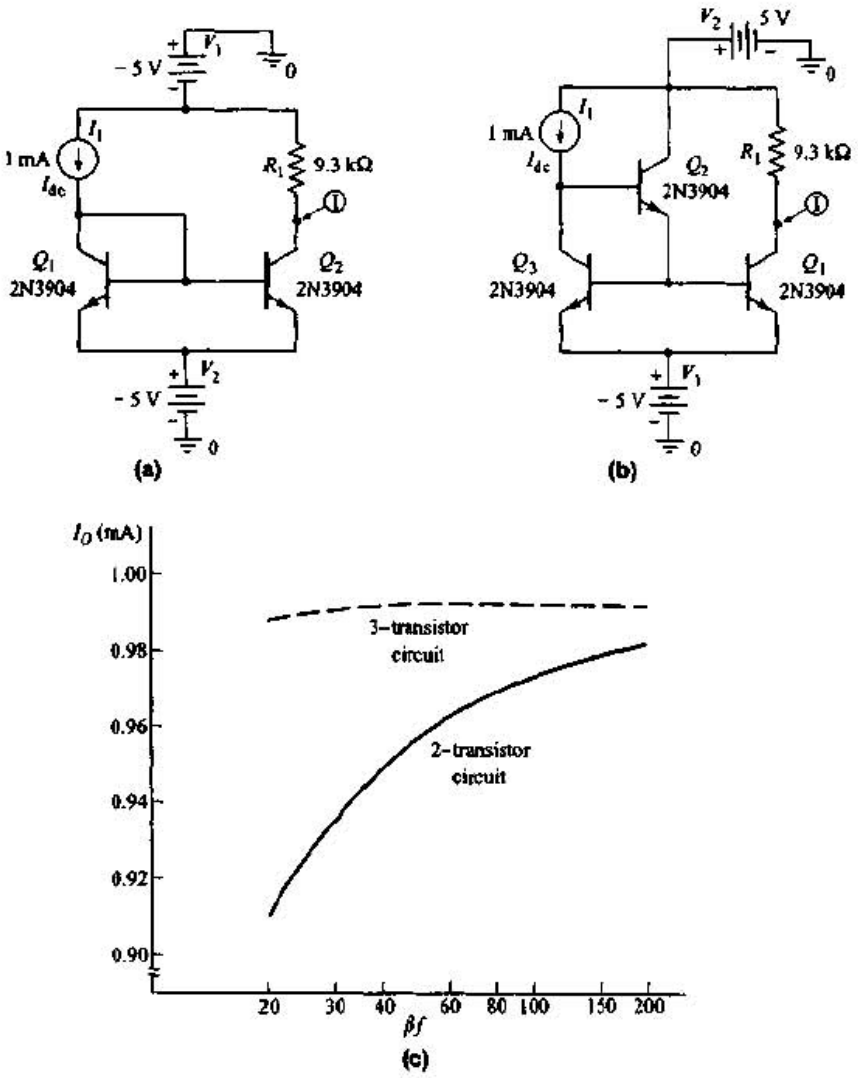

Figure 10.6 (a) Two-transistor current mirror; (b) three-transistor current mirror; (c) variation in bias currents with a change in β

Test Your Understanding

10.4 The parameters for the circuit shown in Figure 10.5 are: $V^+ = 9\,\text{V}$, $V^- = 0$, and $R_1 = 12\,\text{k}\Omega$. The transistor parameters, for all transistors, are: $V_{BE}(\text{on}) = 0.7\,\text{V}$, $\beta = 75$, and $V_A = \infty$. Calculate the value of each current shown in the figure. (Ans. $I_{\text{REF}} = 0.6333\,\text{mA}$, $I_O = 0.6331\,\text{mA} = I_{C1}$, $I_{B1} = I_{B2} = 8.44\,\mu\text{A}$, $I_{E3} = 16.88\,\mu\text{A}$, $I_{B3} = 0.222\,\mu\text{A}$)

10.5 The current source shown in Figure 10.5 utilizes BJTs, with parameters $\beta = 100$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, and $V_A = 100\,\text{V}$. The circuit parameters are: $V^+ = 10\,\text{V}$, $V^- = 0$, and $R_1 = 12\,\text{k}\Omega$. Determine the output resistance and the change in load current if the collector voltage at Q_2 changes from 1 V to 5 V. (Ans. $r_o = 139\,\text{k}\Omega$, $\Delta I_O = 0.0288\,\text{mA}$)

Cascode Current Source

Current-source circuits can be designed such that the output resistance is much greater than that of the two-transistor circuit. One example is the cascode circuit shown in Figure 10.7(a). In this case, if the transistors are matched, then the load and reference currents are essentially equal.

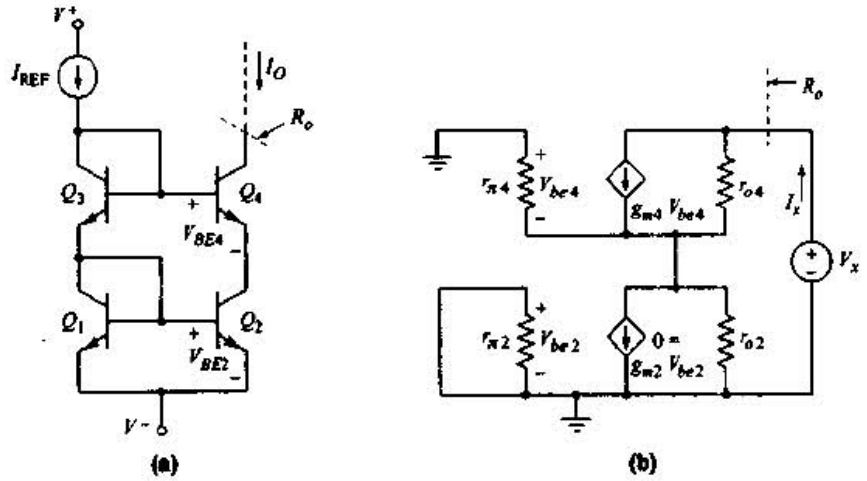

Figure 10.7 (a) Bipolar cascode current mirror; (b) small-signal equivalent circuit

We may calculate the output resistance R_o by considering the small-signal equivalent transistor circuits. For a constant reference current, the base voltages of Q_2 and Q_4 are constant, which implies these terminals are at signal ground. The equivalent circuit is then shown in Figure 10.7(b). Since $g_{m2}V_{be2} = 0$, then $V_{be4} = -I_x(r_{o2} \| r_{\pi 4})$. Summing currents at the output node yields

$$\begin{aligned} I_x &= g_{m4}V_{be4} + \left(\frac{V_x - I_x(r_{o2} \| r_{\pi 4})}{r_{o4}}\right) \\ &= -g_{m4}I_x(r_{o2} \| r_{\pi 4}) + \left(\frac{V_x - I_x(r_{o2} \| r_{\pi 4})}{r_{o4}}\right) \end{aligned} \tag{10.19}$$

Combining terms, we find

$$R_o = \frac{V_x}{I_x} = r_{o4}(1 + \beta) + r_{\pi 4} \cong \beta r_{o4} \tag{10.20}$$

The output resistance has increased by a factor of β compared to the two-transistor current source, which increases the stability of the current source with changes in output voltage.

Wilson Current Source

Another configuration of a three-transistor current source, called a **Wilson current source**, is shown in Figure 10.8. This circuit also has a large output resistance. Our analysis again assumes identical transistors, with $I_{B1} = I_{B2}$ and $I_{C1} = I_{C2}$. The current levels in all three transistors are nearly the same;

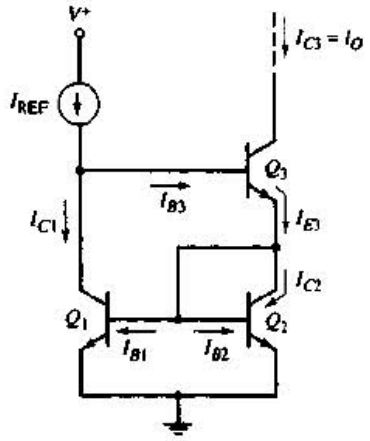

Figure 10.8 Wilson current source

therefore, we can assume that the current gains of the three transistors are equal. Nodal equations at the collector of Q_1 and the emitter of Q_3 yield

$$I_{REF} = I_{C1} + I_{B3} \tag{10.21}$$

and

$$I_{E3} = I_{C2} + 2I_{B2} = I_{C2}\left(1 + \frac{2}{\beta}\right) \tag{10.22}$$

Using the relationships between the base, collector, and emitter currents in Q_3, we can write the collector current I_{C2}, from Equation (10.22), as follows:

$$I_{C2} = \frac{I_{E3}}{\left(1 + \frac{2}{\beta}\right)} = \frac{1}{\left(1 + \frac{2}{\beta}\right)} \times \left(\frac{1+\beta}{\beta}\right) I_{C3} = \left(\frac{1+\beta}{2+\beta}\right) I_{C3} \tag{10.23}$$

If we replace I_{C1} by I_{C2} in Equation (10.21), the reference current becomes

$$I_{REF} = I_{C2} + I_{B3} = \left(\frac{1+\beta}{2+\beta}\right) I_{C3} + \frac{I_{C3}}{\beta} \tag{10.24}$$

Rearranging terms, we can solve for the output current,

$$I_{C3} = I_O = I_{REF} \times \frac{1}{1 + \frac{2}{\beta(2+\beta)}} \tag{10.25}$$

This current relationship is essentially the same as that of the previous three-transistor current source.

The difference between the two three-transistor current-source circuits is the output resistance. In the Wilson current source, the output resistance looking into the collector of Q_3 is $R_o \cong \beta r_{o3}/2$, which is approximately a factor $\beta/2$ larger than that of either the two-transistor source or the basic three-transistor source. This means that, in the Wilson current source, the change in bias current I_O with a change in output collector voltage is much smaller.

Output Voltage Swing

If we consider the equivalent circuit in Figure 10.3, we see that the maximum possible swing in the output voltage is a function of the minimum possible collector–emitter voltage of Q_2. For the two-transistor current source in this figure, the minimum value of $V_{CE2} = V_{CE}(\text{sat})$, which may be on the order of 0.1 to 0.3 V.

For the cascode and Wilson current sources, the minimum output voltage is $V_{BE} + V_{CE}(\text{sat})$ above the negative power supply voltage, which may be on the order of 0.7 to 0.9 V. For circuits biased at ±5 V, for example, this increased minimum voltage may not be a serious problem. However, as the voltages decrease in low-power circuits, this minimum voltage effect may become more serious.

Problem-Solving Technique: BJT Current Source Circuits

1. Sum currents at the various nodes in the circuit to find the relation between the reference current and the bias currrent.
2. To find the output resistance of the current source circuit, place a test voltage at the output node and analyze the small-signal equivalent circuit. Keep in mind that the reference current is a constant, which may make some of the base voltages constant or at ac ground.

Test Your Understanding

10.6 For the Wilson current source in Figure 10.8, the transistor parameters are: $V_{BE}(\text{on}) = 0.7\,\text{V}$, $\beta = 50$, and $V_A = \infty$. For $I_{REF} = 0.50\,\text{mA}$, determine all currents shown in the figure. (Ans. $I_O = 0.4996\,\text{mA}$, $I_{B3} = 9.99\,\mu\text{A}$, $I_{E3} = 0.5096\,\text{mA}$, $I_{C2} = 0.490\,\text{mA} = I_{C1}$, $I_{B1} = I_{B2} = 9.80\,\mu\text{A}$)

10.1.3 Widlar Current Source

In the current-source circuits considered thus far, the load and reference currents have been nearly equal. For a two-transistor current source, such as that shown in Figure 10.2(a), if we require a load current of $I_O = 10\,\mu\text{A}$, then, for $V^+ = 5\,\text{V}$ and $V^- = -5\,\text{V}$, the required resistance value is

$$R_1 = \frac{V^+ - V_{BE} - V^-}{I_{REF}} \cong \frac{5 - 0.7 - (-5)}{10 \times 10^{-6}} = 930\,\text{k}\Omega$$

In ICs, resistors on the order of 1 MΩ require large areas and are difficult to fabricate accurately. We therefore need to limit IC resistor values to the low kilohm range.

The transistor circuit in Figure 10.9, called a **Widlar current source**, meets this objective. A voltage difference is produced across resistor R_E, so that the B–E voltage of Q_2 is less than the B–E voltage of Q_1. A smaller B–E voltage

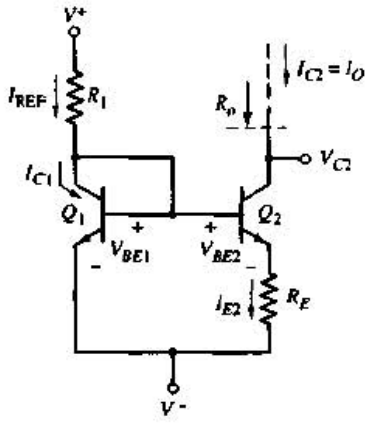

Figure 10.9 Widlar current source

produces a smaller collector current, which in turn means that the load current I_O is less than the reference current I_{REF}.

Current Relationship

If $\beta \gg 1$ for Q_1 and Q_2, and if the two transistors are identical, then

$$I_{REF} \cong I_{C1} = I_S e^{V_{BE1}/V_T} \tag{10.26(a)}$$

and

$$I_O = I_{C2} = I_S e^{V_{BE2}/V_T} \tag{10.26(b)}$$

Solving for the B–E voltages, we have

$$V_{BE1} = V_T \ln\left(\frac{I_{REF}}{I_S}\right) \tag{10.27(a)}$$

and

$$V_{BE2} = V_T \ln\left(\frac{I_O}{I_S}\right) \tag{10.27(b)}$$

Combining Equations (10.27(a)) and (10.27(b)) yields

$$V_{BE1} - V_{BE2} = V_T \ln\left(\frac{I_{REF}}{I_O}\right) \tag{10.28}$$

From the circuit, we see that

$$V_{BE1} - V_{BE2} = I_{E2} R_E \cong I_O R_E \tag{10.29}$$

When we combine Equations (10.28) and (10.29), we obtain:

$$I_O R_E = V_T \ln\left(\frac{I_{REF}}{I_O}\right) \tag{10.30}$$

This equation gives the relationship between the reference and bias currents.

Design Example 10.4 Objective: Design a Widlar current source to achieve specified reference and load currents.

Design the Widlar current source to produce $I_{REF} = 1\,\text{mA}$ and $I_O = 12\,\mu\text{A}$. Let $V^+ = 5\,\text{V}$ and $V^- = -5\,\text{V}$. Assume $V_{BE1} = 0.7\,\text{V}$ at the reference current of 1 mA.

Solution: Resistance R_1 is

$$R_1 = \frac{V^+ - V_{BE1} - V^-}{I_{REF}} = \frac{5 - 0.7 - (-5)}{1} = 9.3\,\text{k}\Omega$$

Resistance R_E is, from Equation (10.30),

$$R_E = \frac{V_T}{I_O} \ln\left(\frac{I_{REF}}{I_O}\right) = \frac{0.026}{0.012} \ln\left(\frac{1}{0.012}\right) = 9.58\,\text{k}\Omega$$

From Equation (10.29), we can determine the difference between the two B–E voltages, as follows:

$$V_{BE1} - V_{BE2} = I_O R_E = (12 \times 10^{-6})(9.58 \times 10^3) = 0.115\,\text{V}$$

Comment: A difference of 115 mV in the B-E voltages of Q_1 and Q_2 produces approximately two orders of magnitude difference between the reference and load currents. Therefore, we can produce a very low bias current using resistors in the low kilohm range. These resistors can easily be fabricated in an IC. Including the resistor R_E gives the designer additional versatility in adjusting the load to reference current ratio.

In our analysis of constant-current source circuits, we have assumed a piecewise linear approximation for the B–E voltage, $V_{BE}(\text{on})$. However, in the Widlar current source and other current-source circuits, the piecewise linear approximation is not adequate, since the B–E voltages are not all equal. With the exponential relationship between collector current and base–emitter voltage, as shown in Equations (10.26(a)) and (10.26(b)), a small change in B–E voltage produces a large change in collector current. To take this variation into account, either the reverse-biased saturation current I_S or the B–E voltage at a particular collector current must be known.

Also in our analysis, we have assumed that the temperatures of all transistors are equal. Maintaining equal temperatures is important for proper circuit operation.

Test Your Understanding

RD10.7 Consider the Widlar current source in Figure 10.9. The bias voltages are $V^+ = 5\,\text{V}$ and $V^- = 0$. Redesign the circuit such that $I_O = 25\,\mu\text{A}$ and $I_{REF} = 0.75\,\text{mA}$. Assume $V_{BE1} = 0.7\,\text{V}$, and neglect the base currents. What is the difference between the two B-E voltages? (Ans. $R_E = 3.54\,\text{k}\Omega$, $R_1 = 5.73\,\text{k}\Omega$, $V_{BE1} - V_{BE2} = 88.5\,\text{mV}$)

10.8 The Widlar current source in Figure 10.9 is biased at $V^+ = 5\,\text{V}$ and $V^- = -5\,\text{V}$. The resistor values are $R_1 = 12\,\text{k}\Omega$ and $R_E = 6\,\text{k}\Omega$. Neglect the base currents and assume the B–E voltage of Q_1 is 0.7 V. Determine I_{REF} and I_O. (Hint: You may need to use trial and error to find I_O.) (Ans. $I_{REF} = 0.775\,\text{mA}$, $I_O \cong 16.6\,\mu\text{A}$)

Output Resistance

The change in load current with a change in voltage V_{C2} of the Widlar current source in Figure 10.9 can be expressed as

$$\frac{dI_O}{dV_{C2}} = \frac{1}{R_o} \tag{10.31}$$

where R_o is the output resistance looking into the collector of Q_2. This output resistance can be determined by using the small-signal equivalent circuit in Figure 10.10(a). (Again, we use the phasor notation in small-signal analyses.) The base, collector, and emitter terminals of each transistor are indicated on the figure.

First, we calculate the resistance R_{o1} looking into the base of Q_1. Writing a KCL equation at the base of Q_1, we obtain

$$I_{x1} = \frac{V_{x1}}{r_{\pi 1}} + g_{m1}V_{x1} + \frac{V_{x1}}{r_{o1} \| R_1} \tag{10.32}$$

Noting that $V_{\pi 1} = V_{x1}$, we have

$$\frac{1}{R_{o1}} = \frac{I_{x1}}{V_{x1}} = \frac{1}{r_{\pi 1}} + g_{m1} + \frac{1}{r_{o1} \| R_1} \tag{10.33(a)}$$

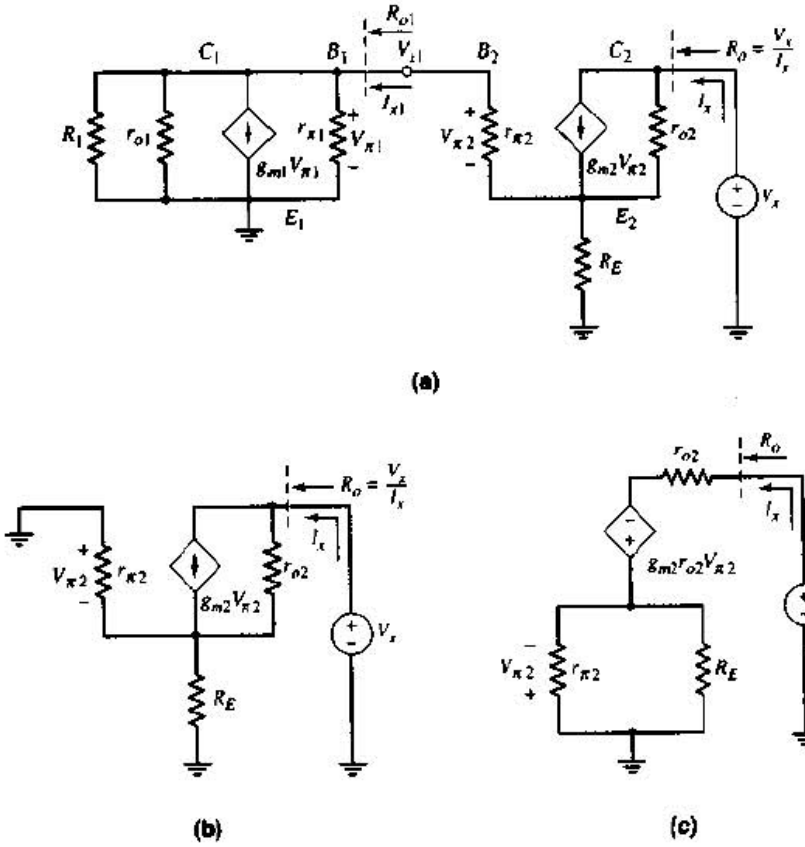

Figure 10.10 (a) Small-signal equivalent circuit for determining output resistance of Widlar current source, (b) simplified equivalent circuit for determining output resistance, and (c) equivalent circuit after a Norton transformation

or

$$R_{o1} = r_{\pi 1} \left\| \frac{1}{g_{m1}} \right\| r_{o1} \| R_1 \qquad \textbf{(10.33(b))}$$

Next, we calculate the approximate value for R_{o1}. If $I_{REF} = 1\,\text{mA}$, then for $\beta = 100$, $r_{\pi 1} = 2.6\,\text{k}\Omega$ and $g_{m1} = 38.5\,\text{mA/V}$. Assume that $R_1 = 9.3\,\text{k}\Omega$ and $r_{o1} = \infty$. For these conditions, $R_{o1} \cong 0.026\,\text{k}\Omega = 26\,\Omega$. For a load current of $I_O = 12\,\mu\text{A}$, we find $r_{\pi 2} = 217\,\text{k}\Omega$. Resistance R_{o1} is in series with $r_{\pi 2}$, and since $R_{o1} \ll r_{\pi 2}$, we can neglect the effect of R_{o1}, which means that the base of Q_2 is essentially at signal ground.

Now we determine the output resistance at the collector of Q_2, using the simplified equivalent circuit in Figure 10.10(b). The Norton equivalent of the current source $g_{m2}V_{\pi 2}$ and resistance r_{o2} can be transformed into a Thevenin equivalent circuit, as shown in Figure 10.10(c). Resistances $r_{\pi 2}$ and R_E are in parallel; therefore, we define $R_E' = R_E \| r_{\pi 2}$. Since the current through the parallel combination of R_E and $r_{\pi 2}$ is I_x, we have

$$V_{\pi 2} = -I_x R_E' \qquad \textbf{(10.34)}$$

Writing a KVL equation, we obtain

$$V_x = I_x r_{o2} - g_{m2} r_{o2} V_{\pi 2} + I_x R_E' \qquad \textbf{(10.35)}$$

Substituting Equation (10.34) into (10.35) yields

$$\frac{V_x}{I_x} = R_o = r_{o2}\left[1 + R_E'\left(g_{m2} + \frac{1}{r_{o2}}\right)\right] \qquad \textbf{(10.36)}$$

Normally, $(1/r_{o2}) \ll g_{m2}$; therefore,

$$R_o \cong r_{o2}(1 + g_{m2} R_E') \qquad \textbf{(10.37)}$$

The output resistance of the Widlar current source is a factor $(1 + g_{m2}R_E')$ larger than that of the simple two-transistor current source.

Example 10.5 **Objective:** Determine the change in load current with a change in collector voltage in a Widlar current source.

Consider the circuit in Figure 10.9. The parameters are: $V^+ = 5\,\text{V}$, $V^- = -5\,\text{V}$, $R_1 = 9.3\,\text{k}\Omega$, and $R_E = 9.58\,\text{k}\Omega$. Let $V_A = 80\,\text{V}$ and $\beta = 100$. Determine the change in I_O as V_{C2} changes by 4 V.

Solution: From Example 10.4, we have $I_O = 12\,\mu\text{A}$. The small-signal collector resistance is

$$r_{o2} = \frac{V_A}{I_O} = \frac{80}{0.012} \Rightarrow 6.67\,\text{M}\Omega$$

We can determine that

$$g_{m2} = \frac{I_O}{V_T} = \frac{0.012}{0.026} = 0.462\,\text{mA/V}$$

and

$$r_{\pi 2} = \frac{\beta V_T}{I_O} = \frac{(100)(0.026)}{0.012} = 217\,\text{k}\Omega$$

The output resistance of the circuit is

$$R_o = r_{o2}[1 + g_{m2}(R_E \| r_{\pi 2})] = (6.67) \cdot [1 + (0.462)(9.58 \| 217)] = 34.9\,\text{M}\Omega$$

From Equation (10.31), the change in load current is

$$dI_O = \frac{1}{R_o} dV_{C2} = \frac{1}{34.9 \times 10^6} \times 4 \Rightarrow 0.115\,\mu\text{A}$$

The percentage change in output current is then

$$\frac{dI_O}{I_O} = \frac{0.115}{12} = 0.0096 \Rightarrow 0.96\%$$

Comment: The stability of the load current, as a function of a change in output voltage, is improved in the Widlar current source, compared to the simple two-transistor current source.

Computer Verification: The output resistance and the change in bias current with a change in output voltage were determined by a PSpice analysis for both the two-transistor and Widlar current-source circuits. Figure 10.11(a) shows the PSpice circuit schematic of the two-transistor current source and Figure 10.11(b) shows the PSpice

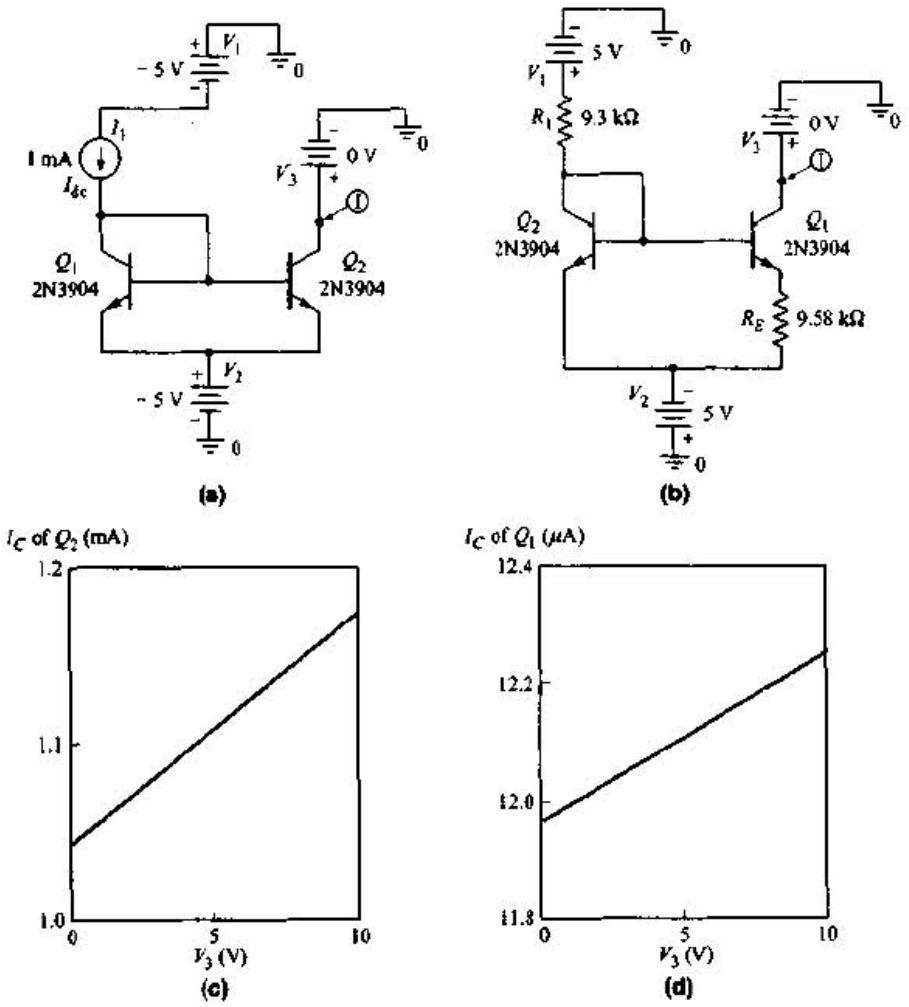

Figure 10.11 (a) The two-transistor current mirror; (b) the Widlar current source; (c) the variation in bias current with output voltage for the two-transistor circuit; (d) the variation in bias current with output voltage for the Widlar circuit

circuit schematic of the Widlar current source used in this analysis. The voltage source V_3 was varied in each circuit from 0 to 10 V.

Figure 10.11(c) shows the change in bias current for the two-transistor current source and Figure 10.11(d) shows the change in bias current for the Widlar current source. The output resistance is 75.8 kΩ for the two-transistor source and is 36.6 MΩ for the Widlar source. The change in bias current for the two-transistor circuit is 13.2 percent and for the Widlar circuit is only 2.28 percent. We, therefore, see the advantage of a large output resistance of a current-source circuit.

Test Your Understanding

***10.9** A Widlar current source is shown in Figure 10.9. The parameters are: $V^+ = 5\,V$, $V^- = 0$, $I_{REF} = 0.70\,mA$, and $I_O = 25\,\mu A$ at $V_{C2} = 1\,V$. The transistor parameters are: $\beta = 150$, $V_{BE1}(on) = 0.7\,V$, and $V_A = 100\,V$. Determine the change in I_O when V_{C2} changes from 1 V to 4 V. (Ans. $dI_O = 0.176\,\mu A$)

10.1.4 Multitransistor Current Mirrors

In the previous current sources, we established a reference current and one load current. In the two-transistor current source in Figure 10.2(a), the B–E junction of the diode-connected transistor Q_1 is forward biased when the bias voltages V^+ and V^- are applied. Once V_{BE} is established, the voltage is applied to the B–E junction of Q_2, which turns Q_2 on and produces the load current I_O.

The B–E voltage of Q_1 can also be applied to additional transistors, to generate multiple load currents. Consider the circuit in Figure 10.12. Transistor Q_R, which is the reference transistor, is connected as a diode. The resulting B–E voltage of Q_R, established by I_{REF}, is applied to N output transistors, creating N load currents. The relationship between each load current and the reference current, assuming all transistors are matched and $V_A = \infty$, is

$$I_{O1} = I_{O2} = \cdots = I_{ON} = \frac{I_{REF}}{1 + \dfrac{(1+N)}{\beta}} \tag{10.38}$$

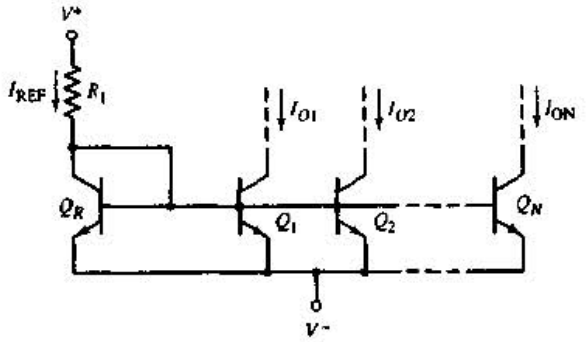

Figure 10.12 Multitransistor current mirror

The collectors of multiple output transistors can be connected together, changing the load current versus reference current relationship. As an example, the circuit in Figure 10.13 has three output transistors with common collectors and a load current I_O. We assume that transistors Q_R, Q_1, Q_2, and Q_3 are all matched. If the current gain β is very large, the base currents can be neglected, $I_1 = I_2 = I_3 = I_{REF}$, and the load current is $I_O = 3I_{REF}$. [Note: This process is not recommended for discrete devices, since a mismatch between devices will generally cause one device to carry more current than the other devices.]

Connecting transistors in parallel increases the effective B–E area of the device. In actual IC fabrication, the B–E area would be doubled or tripled to provide a load current twice or three times the value of I_{REF}.

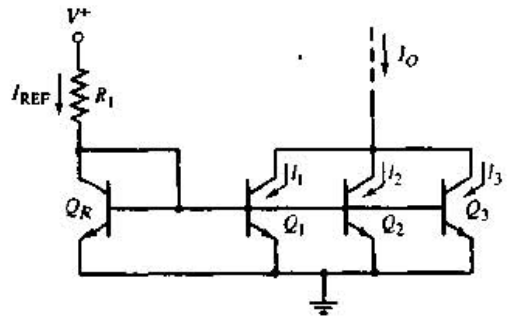

Figure 10.13 Multioutput transistor current source

Rather than drawing each set of parallel output transistors, we can use the circuit symbols in Figure 10.14. Figure 10.14(a) is the equivalent symbol for two transistors connected in parallel, Figure 10.14(b) is for three transistors in parallel, and Figure 10.14(c) is for N transistors in parallel. Although the transistors appear to be multiemitter devices, we are simply indicating devices with different B–E junction areas.

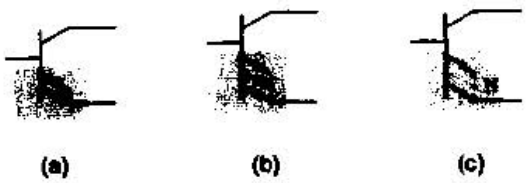

Figure 10.14 Equivalent circuit symbols (a) two transistors in parallel, (b) three transistors in parallel, and (c) N transistors in parallel

A generalized current mirror is shown in Figure 10.15. We can use pnp transistors to establish the load currents, as shown in the figure. Transistors Q_{R1} and Q_{R2} are connected as diodes. The reference current is established in the branch of the circuit that has the diode-connected transistors, resistor R_1, and bias voltages, and is given by

$$I_{REF} = \frac{V^+ - V_{EB}(Q_{R1}) - V_{BE}(Q_{R2}) - V^-}{R_1} \tag{10.39}$$

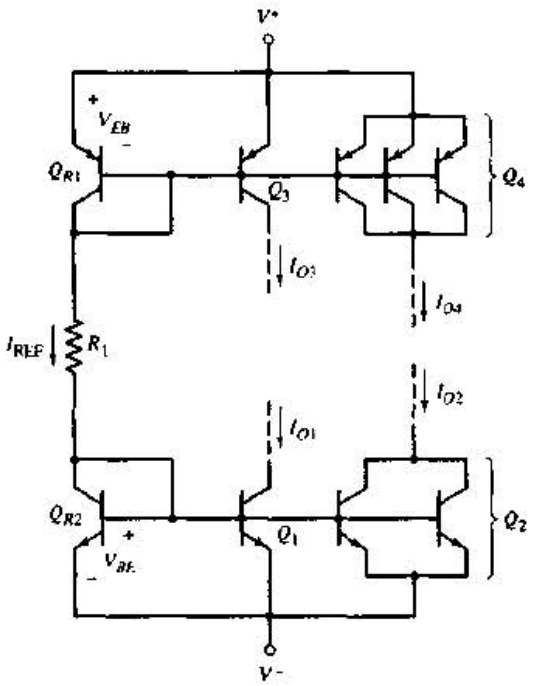

Figure 10.15 Generalized current mirror

If β for each transistor is very large, the base current effects can be neglected. Then the load current I_{O1} generated by output transistor Q_1 is equal to I_{REF}. Likewise, Q_3 generates a load current I_{O3} equal to I_{REF}. Implicitly, all transistors are identical, all load transistors are biased in their forward-active region, and all transistor Early voltages are infinite. Transistor Q_2 is effectively two transistors in parallel; then, since all transistors are identical, $I_{O2} = 2I_{REF}$. Similarly, Q_4 is effectively three transistors connected in parallel, which means that the load current is $I_{O4} = 3I_{REF}$.

In the above discussion, we neglected the effect of base currents. However, a finite β causes the collector currents in each load transistor to be smaller than I_{REF} since the reference current supplies all base currents. This effect becomes more severe as more load transistors are added.

Design Example 10.6 **Objective:** Design a generalized current mirror.

Consider the current mirror shown in Figure 10.15, with parameters $V^+ = 5\,\text{V}$ and $V^- = -5\,\text{V}$. Neglect base currents and assume $V_{BE} = V_{EB} = 0.6\,\text{V}$. Design the circuit such that $I_{O2} = 400\,\mu\text{A}$. Determine I_{REF}, I_{O1}, I_{O3}, I_{O4}, and R_1.

Solution: For $I_{O2} = 400\,\mu\text{A}$, we have

$$I_{REF} = I_{O1} = I_{O3} = 200\,\mu\text{A} \qquad \text{and} \qquad I_{O4} = 600\,\mu\text{A}$$

Resistor R_1 is

$$R_1 = \frac{V^+ - V_{EB}(Q_{R1}) - V_{BE}(Q_{R2}) - V^-}{I_{REF}} = \frac{5 - 0.6 - 0.6 - (-5)}{0.2}$$

or

$$R_1 = 44\,\text{k}\Omega$$

Comment: If the load and reference currents are to be within a factor of approximately four of each other, it is more efficient, from an IC point of view, to adjust the B–E areas of the transistors to achieve the specified currents rather than use the Widlar current source with its additional resistors.

Design Pointer: This example demonstrates that multiple bias currents can be generated by a single reference current that biases various stages of a complex circuit. We will see specific examples of this technique in Chapter 13 when we consider actual operational amplifier circuits.

Test Your Understanding

***10.10** Figure 10.12 shows the N-output current mirror. Assuming all transistors are matched, with a finite gain and $V_A = \infty$, derive Equation (10.38). If each load current must be within 10 percent of I_{REF}, and if $\beta = 50$, determine the maximum number of load transistors that can be connected. (Ans. $N = 4$)

10.2 FET CURRENT SOURCES

Field-effect transistor integrated circuits are biased with current sources in much the same way as bipolar circuits. We will examine the relationship between the reference and load currents, and will determine the output impedance of the basic two-transistor MOSFET current source. We will then analyze multi-MOSFET current-source circuits to determine reference and load current relationships and output impedance. Finally, we will discuss JFET constant-current source circuits.

10.2.1 Basic Two-Transistor MOSFET Current Source

Current Relationship

Figure 10.16 shows a basic two-transistor NMOS current source. The drain and source terminals of the enhancement-mode transistor M_1 are connected, which means that M_1 is always biased in the saturation region. Assuming $\lambda = 0$, we can write the reference current as

$$I_{REF} = K_{n1}(V_{GS} - V_{TN1})^2 \tag{10.40}$$

Solving for V_{GS} yields

$$V_{GS} = V_{TN1} + \sqrt{\frac{I_{REF}}{K_{n1}}} \tag{10.41}$$

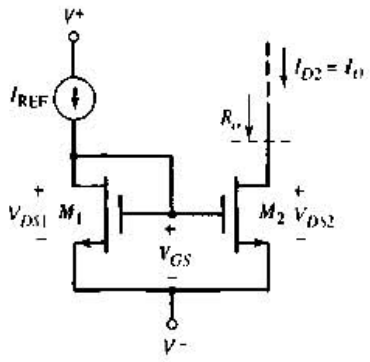

Figure 10.16 Basic two-transistor MOSFET current source

For the drain current to be independent of the drain-to-source voltage (for $\lambda = 0$), transistor M_2 should always be biased in the saturation region. The load current is then

$$I_O = K_{n2}(V_{GS} - V_{TN2})^2 \tag{10.42}$$

Substituting Equation (10.41) into (10.42), we have

$$I_O = K_{n2}\left[\sqrt{\frac{I_{REF}}{K_{n1}}} + V_{TN1} - V_{TN2}\right]^2 \tag{10.43}$$

If M_1 and M_2 are identical transistors, then $V_{TN1} = V_{TN2}$ and $K_{n1} = K_{n2}$, and Equation (10.43) becomes

$$I_O = I_{REF} \tag{10.44}$$

Since there are no gate currents in MOSFETs, the induced load current is identical to the reference current, provided the two transistors are matched. The relationship between the load current and the reference current changes if the width-to-length ratios, or **aspect ratios**, of the two transistors change.

If the transistors are matched except for the aspect ratios, we find

$$I_O = \frac{(W/L)_2}{(W/L)_1} \cdot I_{REF} \tag{10.45}$$

The ratio between the load and reference currents is directly proportional to the aspect ratios and gives designers versatility in their circuit designs.

Output Resistance

The stability of the load current as a function of the drain-to-source voltage is an important consideration in many applications. The drain current versus drain-to-source voltage is similar to the bipolar characteristic shown in Figure 10.4. Taking into account the finite output resistance of the transistors, we can write the load and reference currents as follows:

$$I_O = K_{n2}(V_{GS} - V_{TN2})^2(1 + \lambda_2 V_{DS2}) \tag{10.46(a)}$$

and

$$I_{REF} = K_{n1}(V_{GS} - V_{TN1})^2(1 + \lambda_1 V_{DS1}) \tag{10.46(b)}$$

Since transistors in the current mirror are processed on the same integrated circuit, all physical parameters, such as V_{TN}, μ_n, C_{ox}, and λ, are essentially identical for both devices. Therefore, taking the ratio of I_O to I_{REF}, we have

$$\frac{I_O}{I_{REF}} = \frac{(W/L)_2}{(W/L)_1} \cdot \frac{(1 + \lambda V_{DS2})}{(1 + \lambda V_{DS1})} \tag{10.47}$$

Equation (10.47) again shows that the ratio I_O/I_{REF} is a function of the aspect ratios, which is controlled by the designer, and it is also a function of λ and V_{DS2}.

As before, the stability of the load current can be described in terms of the output resistance. Note from the circuit in Figure 10.16 that $V_{DS1} = V_{GS1} =$ constant for a given reference current. Normally, $\lambda V_{DS1} = \lambda V_{GS1} \ll 1$, and if $(W/L)_2 = (W/L)_1$, then the change in bias current with respect to a change in V_{DS2} is

$$\frac{1}{R_o} \equiv \frac{dI_O}{dV_{DS2}} \cong \lambda I_{REF} = \frac{1}{r_o} \tag{10.48}$$

where r_o is the output resistance of the transistor. As we found with bipolar current-source cicuits, MOSFET current sources require a large output resistance for excellent stability.

Reference Current

The reference current in bipolar current-source circuits is generally established by the bias voltages and a resistor. Since MOSFETs can be configured to act like a resistor, the reference current in MOSFET current mirrors is usually established by using additional transistors.

Consider the current mirror shown in Figure 10.17. Transistors M_1 and M_3 are in series; assuming $\lambda = 0$, we can write,

$$K_{n3}(V_{GS1} - V_{TN1})^2 = K_{n3}(V_{GS3} - V_{TN3})^2 \tag{10.49}$$

If we again assume that V_{TN}, μ_n, and C_{ox} are identical in all transistors, then Equation (10.49) can be rewritten

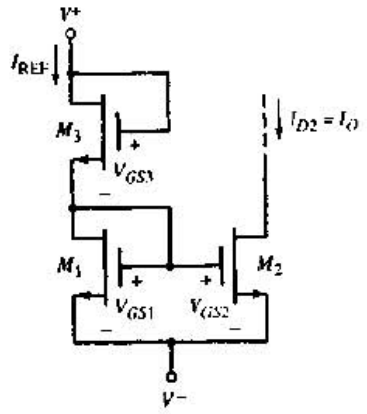

Figure 10.17 MOSFET current source