$$V_{GS1} = \sqrt{\frac{(W/L)_3}{(W/L)_1}} \cdot V_{GS3} + \left(1 - \sqrt{\frac{(W/L)_3}{(W/L)_1}}\right) \cdot V_{TN} \tag{10.50}$$

where V_{TN} is the threshold voltage of both transistors.

From the circuit, we see that

$$V_{GS1} + V_{GS3} = V^+ - V^- \tag{10.51}$$

Therefore,

$$V_{GS1} = \frac{\sqrt{\frac{(W/L)_3}{(W/L)_1}}}{1 + \sqrt{\frac{(W/L)_3}{(W/L)_1}}} \cdot (V^+ - V^-) + \frac{\left(1 - \sqrt{\frac{(W/L)_3}{(W/L)_1}}\right)}{\left(1 + \sqrt{\frac{(W/L)_3}{(W/L)_1}}\right)} \cdot V_{TN} = V_{GS2} \tag{10.52}$$

Finally, the load current, for $\lambda = 0$, is given by

$$I_O = \left(\frac{W}{L}\right)_2 \left(\frac{1}{2}\mu_n C_{ox}\right)(V_{GS2} - V_{TN})^2 \tag{10.53}$$

Since the designer has control over the width-to-length ratios of the transistors, there is considerable flexibility in the design of MOSFET current sources.

Design Example 10.7 **Objective:** Design a MOSFET current source to meet specified current values.

Consider the current source in Figure 10.17, with transistor parameters $\frac{1}{2}\mu_n C_{ox} = 20\,\mu A/V^2$, $V_{TN} = 1\,V$, and $\lambda = 0$. Let $V^+ = 5\,V$ and $V^- = 0$. Design the circuit such that $I_{REF} = 0.25\,mA$ and $I_O = 0.10\,mA$.

Solution: If we choose V_{GS2} to be fairly small, yet greater than V_{TN}, then M_2 will remain biased in the saturation region over a fairly large range of V_{DS2} values. Let $V_{GS2} = 1.85\,V$. Then, from Equation (10.53), we can write

$$\left(\frac{W}{L}\right)_2 = \frac{I_O}{\left(\frac{1}{2}\mu_n C_{ox}\right)(V_{GS2} - V_{TN})^2} = \frac{0.10}{(0.02)(1.85 - 1)^2} = 6.92$$

The reference current is

$$I_{REF} = \left(\frac{W}{L}\right)_1 \left(\frac{1}{2}\mu_n C_{ox}\right)(V_{GS1} - V_{TN})^2$$

Since $V_{GS1} = V_{GS2}$, we have

$$\left(\frac{W}{L}\right)_1 = \frac{I_{REF}}{\left(\frac{1}{2}\mu_n C_{ox}\right)(V_{GS2} - V_{TN})^2} = \frac{0.25}{(0.02)(1.85 - 1)^2} = 17.3$$

The value of V_{GS3} is

$$V_{GS3} = (V^+ - V^-) - V_{GS1} = 5 - 1.85 = 3.15\,\text{V}$$

Then, since $I_{REF} = K_{n3}(V_{GS3} - V_{TN})^2$, we have

$$\left(\frac{W}{L}\right)_3 = \frac{I_{REF}}{\left(\frac{1}{2}\mu_n C_{ox}\right)(V_{GS3} - V_{TN})^2} = \frac{0.25}{(0.02)(3.15 - 1)^2} = 2.70$$

Comment: In this design, the output transistor remains biased in the saturation region for

$$V_{DS} > V_{DS}(\text{sat}) = V_{GS} - V_{TN} = 1.85 - 1 = 0.85\,\text{V}$$

Design Pointer: As with most design problems, there is not a unique solution. The general design criterion was that M_2 was biased in the saturation region over a wide range of V_{DS2} values. Letting $V_{GS2} = 1.85\,\text{V}$ was somewhat arbitrary. If V_{GS2} were smaller, the width-to-length ratios of M_1 and M_2 would need to be larger. Larger values of V_{GS2} would result in smaller width-to-length ratios.

The value of V_{GS3} is the difference between the bias voltage and V_{GS1}. If V_{GS3} becomes too large, the ratio $(W/L)_3$ will become unreasonably small (much less than 1). Two or more transistors in series can be used in place of M_3 to divide the voltage in order to provide reasonable W/L ratios (see Problem 10.49).

Problem-Solving Technique: MOSFET Current-Source Circuit

1. Analyze the reference side of the circuit to determine gate-to-source voltages. Using these gate-to-source voltages, determine the bias current in terms of the reference current.
2. To find the output resistance of the current source circuit, place a test voltage at the output node and analyze the small-signal equivalent circuit. Keep in mind that the reference current is a constant, which may make some of the gate voltages constant or at ac ground.

Test Your Understanding

10.11 Consider the MOSFET current source in Figure 10.17, with $V^+ = 10\,\text{V}$ and $V^- = 0$. The transistor parameters are: $V_{TN} = 1.8\,\text{V}$, $\frac{1}{2}\mu_n C_{ox} = 20\,\mu\text{A/V}^2$, and $\lambda = 0.01\,\text{V}^{-1}$. The transistor width-to-length ratios are: $(W/L)_3 = 3$, $(W/L)_1 = 12$, and $(W/L)_2 = 6$. Determine: (a) I_{REF}, (b) I_O at $V_{DS2} = 2\,\text{V}$, and (c) I_O at $V_{DS2} = 6\,\text{V}$. (Ans. (a) $I_{REF} = 1.13\,\text{mA}$ (b) $I_O = 0.555\,\text{mA}$ (c) $I_O = 0.576\,\text{mA}$)

10.12 Consider the circuit shown in Figure 10.18. The transistor parameters are: $V_{TN} = 2\,\text{V}$, $K_{n1} = K_{n2} = 0.25\,\text{mA/V}^2$, $K_{n3} = 0.10\,\text{mA/V}^2$, and $\lambda = 0$. Determine I_{REF} and I_O. (Note: All transistors labeled M_2 are identical.) (Ans. $I_{REF} = 1.35\,\text{mA}$, $I_O = 4.04\,\text{mA}$)

D10.13 For the circuit shown in Figure 10.17, $V^+ = 10\,\text{V}$ and $V^- = 0$, and the transistor parameters are: $V_{TN} = 2\,\text{V}$, $\frac{1}{2}\mu_n C_{ox} = 20\,\mu\text{A/V}^2$, and $\lambda = 0$. Design the circuit such that $I_{REF} = 0.5\,\text{mA}$ and $I_O = 0.2\,\text{mA}$, and M_2 remains biased in the saturation region for $V_{DS2} \geq 1\,\text{V}$. (Ans. $(W/L)_2 = 10$, $(W/L)_1 = 25$, $(W/L)_3 = 1$)

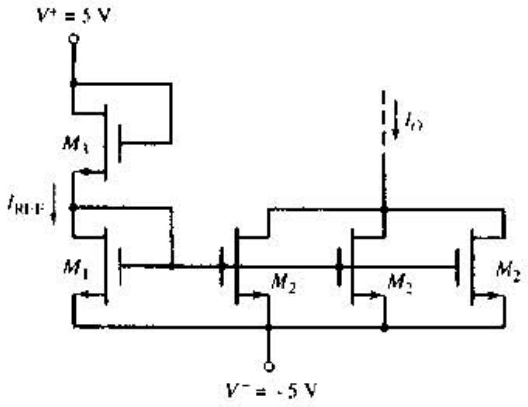

Figure 10.18 Figure for Exercise 10.12

10.2.2 Multi-MOSFET Current-Source Circuits

Cascode Current Mirror

In MOSFET current-source circuits, the output resistance is a measure of the stability with respect to changes in the output voltage. This output resistance can be increased by modifying the circuit, as shown in Figure 10.19, which is a **cascode current mirror**. The reference current is established by including another MOSFET in the reference branch of the circuit as was done in the basic two-transistor current mirror. Assuming all transistors are identical, then $I_O = I_{REF}$.

To determine the output resistance at the drain of M_4, we use the small-signal equivalent circuit. Since I_{REF} is a constant, the gate voltages to M_1 and M_3, and hence to M_2 and M_4, are constant. This is equivalent to an ac short circuit. The ac equivalent circuit for calculating the output resistance is shown

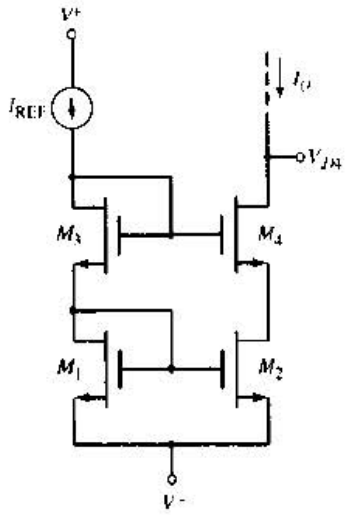

Figure 10.19 MOSFET cascode current mirror

in Figure 10.20(a). The small-signal equivalent circuit is given in Figure 10.20(b). The small-signal resistance looking into the drain of M_2 is r_{O2}.

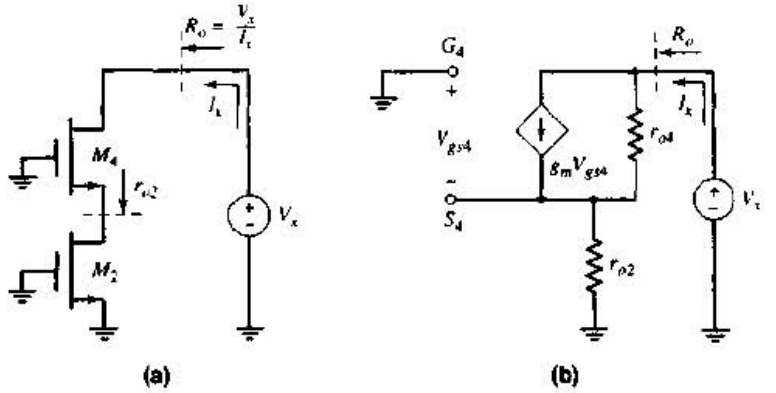

Figure 10.20 Equivalent circuits of the MOSFET cascode current mirror for determining output resistance

Writing a KCL equation, in phasor form, at the output node, we have

$$I_x = g_m V_{gs4} + \frac{V_x - (-V_{gs4})}{r_{o4}} \tag{10.54}$$

Also,

$$V_{gs4} = -I_x r_{o2} \tag{10.55}$$

Substituting Equation (10.55) into (10.54), we obtain

$$I_x + \frac{r_{o2}}{r_{o4}} I_x + g_m r_{o2} I_x = \frac{V_x}{r_{o4}} \tag{10.56}$$

The output resistance is then

$$R_o = \frac{V_x}{I_x} = r_{o4} + r_{o2}(1 + g_m r_{o4}) \tag{10.57}$$

Normally, $g_m r_{o4} \gg 1$, which implies that the output resistance of this cascode configuration is much larger than that of the basic two-transistor current source.

Example 10.8 **Objective:** Compare the output resistance of the cascode MOSFET current source to that of the two-transistor current source.

Consider the two-transistor current source in Figure 10.17 and the cascode current source in Figure 10.19. Assume $I_{REF} = I_O = 100\,\mu A$ in both circuits, $\lambda = 0.01\ V^{-1}$ for all transistors, and $g_m = 0.5\,mA/V$.

Solution: The output resistance of the two-transistor current source is, from Equation (10.48)

$$r_o = \frac{1}{\lambda I_{REF}} = \frac{1}{(0.01)(0.10)} \Rightarrow 1\,M\Omega$$

For the cascode circuit, we have $r_{o2} = r_{o4} = 1\,\text{M}\Omega$. Therefore, the output resistance of the cascode circuit is, from Equation (10.57),

$$R_o = r_{o4} + r_{o2}(1 + g_m r_{o4}) = 1 + (1)[1 + (0.5 \times 10^{-3})(10^6)]$$

or

$$R_o = 502\,\text{M}\Omega$$

Comment: The output resistance of the cascode current source is substantially larger than that of the basic two-transistor circuit. Since $dI_O \propto 1/R_o$, the load current in the cascode circuit is more stable against variations in output voltage.

Design Pointer: Achieving the output resistance of 502 MΩ assumes the transistors are ideal. In fact, small leakage currents will begin to be a factor in actual output resistance values, so a value of 502 MΩ may not be achieved in reality.

Test Your Understanding

10.14 In the MOSFET cascode current source shown in Figure 10.19, all transistors are identical, with parameters: $V_{TN} = 1\,\text{V}$, $K_n = 80\,\mu\text{A/V}^2$, and $\lambda = 0.02\,\text{V}^{-1}$. Let $I_{REF} = 20\,\mu\text{A}$. The circuit is biased at $V^+ = 5\,\text{V}$ and $V^- = -5\,\text{V}$. Determine: (a) V_{GS} of each transistor, (b) the lowest possible voltage value V_{D4}, and (c) the output resistance R_o. (Ans. (a) $V_{GS} = 1.5\,\text{V}$ (b) $V_{D4}(\text{min}) = -3.0\,\text{V}$ (c) $R_o = 505\,\text{M}\Omega$)

Wilson Current Mirror

Two additional multi-MOSFET current sources are shown in Figures 10.21(a) and 10.21(b). The circuit in Figure 10.21(a) is the **Wilson current source**. Note

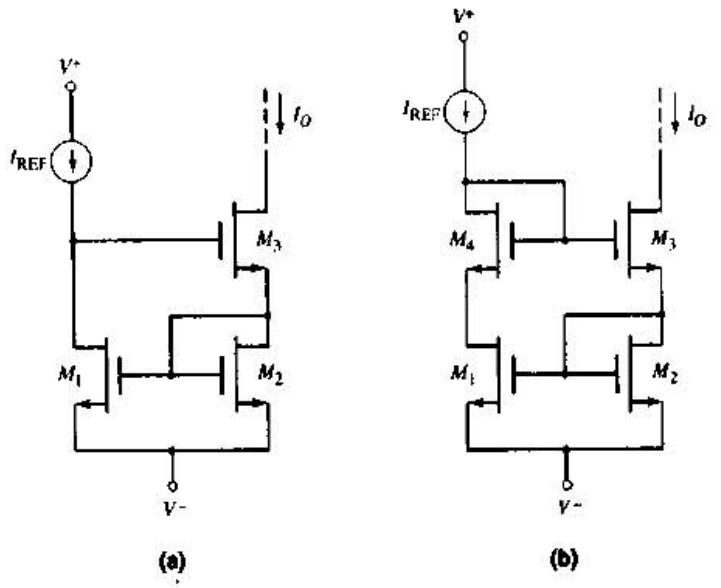

Figure 10.21 (a) MOSFET Wilson current source and (b) modified MOSFET Wilson current source

that the V_{DS} values of M_1 and M_2 are not equal. Since λ is not zero, the ratio I_O/I_{REF} is slightly different from the aspect ratios. This problem is solved in the **modified Wilson current source**, shown in Figure 10.21(b), which includes transistor M_4. For a constant reference current, the drain-to-source voltages of M_1, M_2, and M_4 are held constant. The primary advantage of these circuits is the increase in output resistance, which further stabilizes the load current.

Test Your Understanding

10.15 For the transistors in the MOSFET Wilson current source in Figure 10.21(a), the parameters are: $V_{TN} = 1\,V$, $\lambda = 0$, and $K_{n1} = 2K_{n2} = K_{n3} = 0.15\,mA/V^2$. If $I_{REF} = 200\,\mu A$, determine I_O and V_{GS} for each transistor. (Ans. $V_{GS1} = V_{GS2} = 2.15\,V$, $I_O = 0.10\,mA$, $V_{GS3} = 1.82\,V$)

10.16 All transistors in the MOSFET modified Wilson current source in Figure 10.21(b) are identical. The parameters are: $V_{TN} = 1\,V$, $K_n = 0.2\,mA/V^2$, and $\lambda = 0$. If $I_{REF} = 250\,\mu A$, determine I_O and V_{GS} for each transistor. (Ans. $I_O = I_{REF} = 250\,\mu A$, $V_{GS} = 2.12\,V$)

Wide-Swing Current Mirror

If we consider the cascode current mirror in Figure 10.17, we can determine the minimum value of V_{D4}, which will influence the maximum symmetrical swing of the voltage in the load circuit being biased. The gate voltage of M_4 is

$$V_{G4} = V^- + V_{GS1} + V_{GS2} \tag{10.58}$$

The minimum V_{D4} is then

$$V_{D4}(\text{min}) = V_{G4} - V_{GS4} + V_{DS4}(\text{sat}) \tag{10.59}$$

Assuming matched transistors, $V_{GS1} = V_{GS2} = V_{GS4} \equiv V_{GS}$. We then find

$$V_{D4}(\text{min}) = V^- + \left(V_{GS} + V_{DS4}(\text{sat})\right) \tag{10.60}$$

In considering the simple two-transistor current mirror, the minimum output voltage is

$$V_O(\text{min}) = V^- + V_{DS}(\text{sat}) \tag{10.61}$$

If, for example, $V_{GS} = 0.75\,V$ and $V_{TN} = 0.50\,V$, then from Equation (10.60), $V_{D4}(\text{min}) = 1.0\,V$ above V^-, and from Equation (10.61), $V_O(\text{min})$ is only $0.25\,V$ above V^-. For bias voltages in the range of $\pm 3.5\,V$, this additional required voltage across the output of the cascode current mirror can have a significant effect on the output of the load circuit.

One current mirror circuit that does not limit the output voltage swing as severely as the cascode circuit, but retains the high output resistance, is shown in Figure 10.22. Width-to-length ratios of the transistors are shown. Otherwise, the transistors are assumed to be identical.

The transistor pair M_3 and M_4 acts like a single diode-connected transistor in creating the gate voltage for M_3. By including M_4, the drain-to-source voltage of M_3 is reduced and is matched to the drain-to-source voltage of

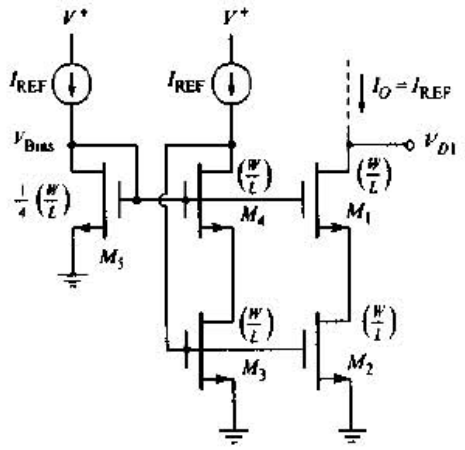

Figure 10.22 A wide-swing MOSFET cascode current mirror

M_2. Since M_5 is one-fourth the size of $M_1 - M_4$ and since all drain currents are equal, we have

$$(V_{GS5} - V_{TN}) = 2(V_{GSi} - V_{TN}) \tag{10.62}$$

where V_{GSi} corresponds to the gate-to-source voltage of $M_1 - M_4$.

The voltage at the gate of M_1 is

$$V_{G1} = V_{GS5} = (V_{GS5} - V_{TN}) + V_{TN} \tag{10.63}$$

The minimum output voltage at the drain of M_1 is

$$\begin{aligned} V_{D1}(\text{min}) &= V_{G1} - V_{GS1} + V_{DS1}(\text{sat}) \\ &= [(V_{GS5} - V_{TN}) + V_{TN}] - V_{GS1} + (V_{GS1} - V_{TN}) \end{aligned} \tag{10.64}$$

or

$$V_{D1}(\text{min}) = V_{GS5} - V_{TN} = 2(V_{GSi} - V_{TN}) = 2V_{DSi}(\text{sat}) \tag{10.65}$$

If we have $V_{GSi} = 0.75\,\text{V}$ and $V_{TN} = 0.5\,\text{V}$, then $V_{D1}(\text{min}) = 0.50\,\text{V}$, which is one-half the value for the cascode circuit. At the same time, the high output resistance is maintained.

Discussion: In the ideal circuit design in Figure 10.22, the transistors M_3 and M_4 are biased exactly at the transition point between the saturation and non-saturation regions. The analysis has neglected the body effect, so threshold voltages will not be exactly equal. In an actual circuit design, therefore, the size of M_5 will be made slightly smaller to ensure transistors are biased in the saturation region. This design change then means that the minimum output voltage increases by perhaps 0.1 to 0.15 V.

10.2.3 Bias-Independent Current Source

In all of the current mirror circuits considered up to this point (both BJT and MOSFET), the reference current is a function of the applied supply voltages. This implies that the load current is also a function of the supply voltages. In most cases, the supply voltage dependence is undesirable. Circuit designs exist

in which the load currents are essentially independent of the bias. One such MOSFET circuit is shown in Figure 10.23. The width-to-length ratios are given.

Since the PMOS devices are matched, the currents I_{D1} and I_{D2} must be equal. Equating the currents in M_1 and M_2, we find

$$I_{D1} = \frac{k_n'}{2}\left(\frac{W}{L}\right)_1 (V_{GS1} - V_{TN})^2 = I_{D2} = \frac{k_n'}{2}\left(\frac{W}{L}\right)_2 (V_{GS2} - V_{TN})^2 \qquad (10.66)$$

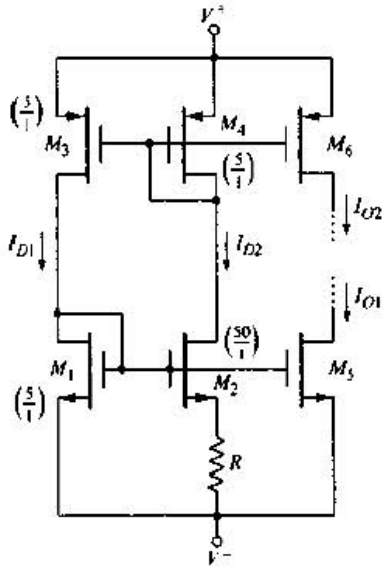

Figure 10.23 Bias-independent MOSFET current mirror

Also

$$V_{GS2} = V_{GS1} - I_{D2}R \qquad (10.67)$$

Substituting Equation (10.67) into Equation (10.66) and solving for R, we obtain

$$R = \frac{1}{\sqrt{K_{n1}I_{D1}}}\left(1 - \sqrt{\frac{(W/L)_1}{(W/L)_2}}\right) \qquad (10.68)$$

This value of resistance R will establish the drain currents $I_{D1} = I_{D2}$. These currents establish the gate-to-source voltage across M_1 and source-to-gate voltage across M_3. These voltages, in turn, can be applied to M_5 and M_6 to establish load currents I_{O1} and I_{O2}.

The currents I_{D1} and I_{D2} are independent of the supply voltages V^+ and V^- as long as M_2 and M_3 are biased in the saturation region. As the difference, $V^+ - V^-$, increases, the values of V_{DS2} and V_{SD3} increase but the currents remain essentially constant.

Similar bipolar bias-independent current mirror designs exist, but will not be covered here.

10.2.4 JFET Current Sources

Current sources are also fundamental elements in JFET integrated circuits. The simplest method of forming a current source is to connect the gate and source terminals of a depletion-mode JFET, as shown in Figure 10.24 for an n-channel device. The device will remain biased in the saturation region as long as

$$v_{DS} \geq v_{DS}(\text{sat}) = v_{GS} - V_P = |V_P| \tag{10.69}$$

In the saturation region, the current is

$$i_D = I_{DSS}\left(1 - \frac{v_{GS}}{V_P}\right)^2 (1 + \lambda v_{DS}) = I_{DSS}(1 + \lambda v_{DS}) \tag{10.70}$$

The output resistance looking into the drain is, from Equation (10.70),

$$\frac{1}{r_o} = \frac{di_D}{dv_{DS}} = \lambda I_{DSS} \tag{10.71}$$

This expression for the output resistance of a JFET current source is the same as that of the MOSFET current source.

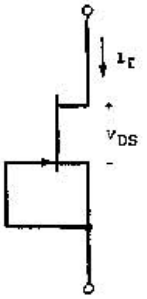

Figure 10.24 Depletion-mode JFET connected as a current source

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Example 10.9 **Objective:** Determine the currents and voltages in a simple JFET circuit biased with a constant-current source.

Consider the circuit shown in Figure 10.25. The transistor parameters are: $I_{DSS1} = 2\,\text{mA}$, $I_{DSS2} = 1\,\text{mA}$, $V_{P1} = V_{P2} = -1.5\,\text{V}$, and $\lambda_1 = \lambda_2 = 0.05\,\text{V}^{-1}$. Determine the minimum values of V_S and V_I such that Q_2 is biased in the saturation region. What is the value of I_O?

Solution: In order for Q_2 to remain biased in the saturation region, we must have $v_{DS} \geq |V_P| = 1.5\,\text{V}$, from Equation (10.69). The minimum value of V_S is then

$$V_S(\text{min}) - V^- = v_{DS}(\text{min}) = 1.5\,\text{V}$$

or

$$V_S(\text{min}) = 1.5 + V^- = 1.5 + (-5) = -3.5\,\text{V}$$

From Equation (10.70), the output current is

$$i_D = I_O = I_{DSS2}(1 + \lambda v_{DS}) = (1)[1 + (0.05)(1.5)] = 1.08\,\text{mA}$$

As a first approximation in calculating the minimum value of V_I, we neglect the effect of λ in transistor Q_1. Then, assuming Q_1 is biased in the saturation region, we have

$$i_D = I_{DSS1}\left(1 - \frac{v_{GS1}}{V_{P1}}\right)^2$$

or

$$1.08 = 2\left(1 - \frac{v_{GS1}}{(-1.5)}\right)^2$$

which yields

$$v_{GS1} = -0.40\,\text{V}$$

We see that

$$v_{GS1} = -0.40\,\text{V} = V_I - V_S = V_I - (-3.5)$$

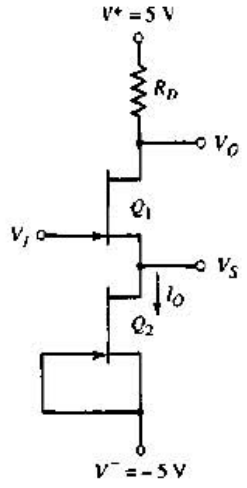


Figure 10.25 The dc equivalent circuit of simple JFET amplifier biased with JFET current source

or

$$V_t = -3.90\,\text{V}$$

Comment: Since Q_1 is an n-channel device, the voltage at the gate is negative with respect to the source.

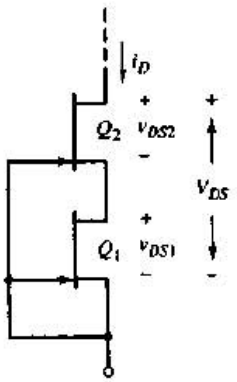


Figure 10.26 JFET cascode current source

The output resistance of a JFET current source can be increased by using a cascode configuration. A simple JFET cascode current source with two n-channel depletion-mode devices is shown in Figure 10.26. The current–voltage relationship, assuming Q_1 and Q_2 are identical, is given by

$$i_D = I_{DSS}(1 + \lambda v_{DS1}) = I_{DSS}\left(1 - \frac{v_{GS2}}{V_P}\right)^2 (1 + \lambda v_{DS2}) \tag{10.72}$$

From the circuit, we see that $v_{GS2} = -v_{DS1}$. We define

$$V_{DS} = v_{DS1} + v_{DS2} \tag{10.73(a)}$$

so that

$$v_{DS2} = V_{DS} - v_{DS1} \tag{10.73(b)}$$

From Equation (10.72), we obtain

$$(1 + \lambda v_{DS1}) = \left(1 + \frac{v_{DS1}}{V_P}\right)^2 [1 + \lambda(V_{DS} - v_{DS1})] \tag{10.74}$$

For a given application, the value of V_{DS} will usually be known, and the value of v_{DS1} can then be determined. The load current i_D can then be calculated by using Equation (10.72).

We can determine the output resistance by using the small-signal equivalent circuit of the composite two-transistor configuration, as shown in Figure 10.27(a), which includes the phasor variables. Since the gate and source of Q_1 are connected together, the small-signal voltage V_{gs1} is zero, which means that

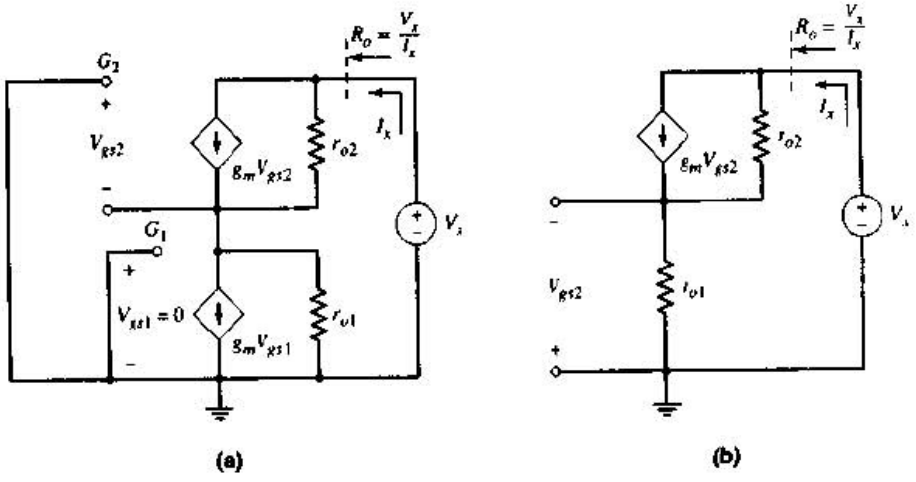


Figure 10.27 (a) Equivalent circuit, using phasor notation, of the JFET cascode current source for determining output resistance and (b) final configuration

the dependent current source $g_m V_{gs1}$ is zero. This corresponds to an open circuit. Figure 10.27(b) shows the final configuration.

The analysis is the same as for the MOSFET cascode circuit in Figure 10.17. Writing a KCL equation at the output node, we have

$$I_x = g_m V_{gs2} + \frac{V_x - (-V_{gs2})}{r_{o2}} \tag{10.75}$$

Noting that

$$V_{gs2} = -I_x r_{o1} \tag{10.76}$$

Equation (10.75) becomes

$$I_x = -(g_m r_{o1}) I_x + \frac{V_x}{r_{o2}} - \left(\frac{r_{o1}}{r_{o2}}\right) I_x \tag{10.77}$$

The output resistance is then

$$R_o = \frac{V_x}{I_x} = r_{o2} + r_{o1} + g_m r_{o1} r_{o2} = r_{o2} + r_{o1}(1 + g_m r_{o2}) \tag{10.78}$$

From Equation (10.78), we see that the output resistance relationship for the JFET cascode current source has the same form as that of the MOSFET cascode current source.

Test Your Understanding

***10.17** Consider the JFET circuit in Figure 10.25. The transistor parameters are: $I_{DSS2} = 0.5\,\text{mA}$, $I_{DSS1} = 0.8\,\text{mA}$, $V_{P1} = V_{P2} = -2\,\text{V}$, and $\lambda_1 = \lambda_2 = 0.15\,\text{V}^{-1}$. Determine the minimum values of V_S and V_I such that Q_2 is biased in the saturation region. What is the value of I_O? What is the output impedance looking into the drain of Q_2? (Ans. $V_S(\text{min}) = -3\,\text{V}$, $I_O = 0.65\,\text{mA}$, $V_I(\text{min}) = -3.2\,\text{V}$, $r_o = 1.09\,\text{k}\Omega$)

***10.18** The JFET cascode circuit in Figure 10.26 has identical transistors, with parameters $I_{DSS} = 2\,\text{mA}$, $V_P = -2\,\text{V}$, and $\lambda = 0.1\,\text{V}^{-1}$. If $V_{DS} = v_{DS1} + v_{DS2} = 3\,\text{V}$, determine: (a) v_{DS1}, v_{GS2}, v_{DS2}, and i_D, and (b) the output impedance R_o. (Ans. (a) $v_{DS1} = 0.212\,\text{V}$, $v_{GS2} = -0.212\,\text{V}$, $v_{DS2} = 2.79\,\text{V}$, $i_D = 2.04\,\text{mA}$ (b) $R_o = 54.8\,\text{k}\Omega$)

10.3 CIRCUITS WITH ACTIVE LOADS

In bipolar amplifiers, such as that shown in Figure 10.28, the small-signal voltage gain is directly proportional to the collector resistor R_C. To increase the gain, we need to increase the value of R_C. Typically, circuit parameters are $I_C = 0.5\,\text{mA}$, $V_{CC} = 10\,\text{V}$, and $R_C = 10\,\text{k}\Omega$. However, if we increase R_C, we would also have to increase the supply voltage V_{CC} if we want to maintain the same collector current and collector–emitter voltage. In practice, there is a limited range of values of R_C and V_{CC} that are reasonable.

To get around this limitation, we need a load device that will pass a current of 0.5 mA at a voltage of 5 V, but which will resist a change in current better than a 10 kΩ resistor. This load device can be a transistor, which will also occupy less area in an integrated circuit, another advantage in using transistors

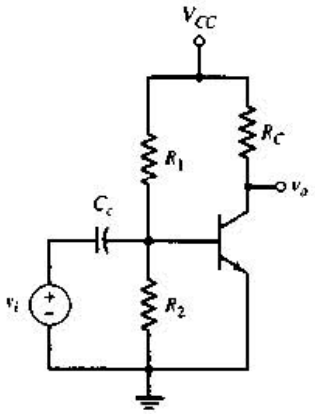


Figure 10.28 Bipolar common-emitter circuit

in place of resistors. In addition, active loads produce a much larger small-signal gain than discrete resistors, as discussed in Chapter 4.

In Chapter 6, we introduced NMOS enhancement load and depletion load devices in MOSFET amplifiers. This was an introduction to active load devices. In this section, we consider the dc analysis of a bipolar active load in a simple BJT circuit and then the dc analysis of a MOSFET active load. Our discussion will include the voltage gains of these active load circuits. The small-signal analysis of active load circuits is covered in the next section.

The discussion of active loads here can be considered an introduction. The use of active loads with differential amplifiers is considered in detail in the next chapter.

10.3.1 DC Analysis: BJT Active Load Circuit

Consider the circuit shown in Figure 10.29. The elements R_1, Q_1, and Q_2 form the active load circuit, and Q_2 is referred to as the **active load device** for driver transistor Q_0. The combination of R_1, Q_1, and Q_2 forms the pnp version of the two-transistor current mirror. For the dc analysis of this circuit, we will use the dc symbols for the currents and voltages. The objective of this analysis is to

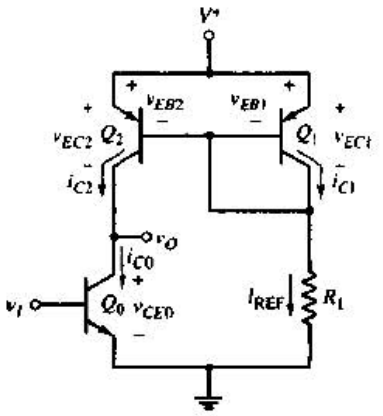


Figure 10.29 Simple BJT amplifier with active load, showing currents and voltages

obtain the voltage transfer function V_O versus V_I.

The B–E voltage of Q_0 is the dc input voltage V_I; therefore, the collector current in Q_0 is

$$I_{C0} = I_{S0}\left[e^{V_I/V_T}\right]\left(1 + \frac{V_{CE0}}{V_{AN}}\right) \tag{10.79}$$

where I_{S0} is the reverse-saturation current, V_T is the thermal voltage, and V_{AN} is the Early voltage of the npn transistor. Similarly, the collector current in Q_2 is

$$I_{C2} = I_{S2}\left[e^{V_{EB2}/V_T}\right]\left(1 + \frac{V_{EC2}}{V_{AP}}\right) \tag{10.80}$$

where V_{AP} is the Early voltage of the pnp transistors.

If we neglect base currents, then

$$I_{REF} = I_{C1} = I_{S1}\left[e^{V_{EB1}/V_T}\right]\left(1 + \frac{V_{EC1}}{V_{AP}}\right) \tag{10.81}$$

Assuming Q_1 and Q_2 are identical, then $I_{S1} = I_{S2}$ and the Early voltages of the pnp transistors are equal. Also note that $V_{EC1} = V_{EB1} = V_{EB2}$. We can also assume that $V_{CE} \ll V_{AN}$ and $V_{EC} \ll V_{AP}$. Combining equations, we find the output voltage is given as

$$V_O = \frac{V_{AN}V_{AP}}{V_{AN} + V_{AP}}\left[1 - \frac{I_{S0}e^{V_I/V_T}}{I_{REF}}\right] + \frac{V_{AN}}{V_{AN} + V_{AP}}(V^+ - V_{EB2}) \tag{10.82}$$

Equation (10.82) is valid as long as Q_0 and Q_2 remain biased in the forward-active region, which means that the output voltage must remain in the range

$$V_{CE0}(\text{sat}) < V_O < (V^+ - V_{EC2}(\text{sat})) \tag{10.83}$$

A sketch of V_O versus V_I is shown in Figure 10.30. If the circuit is to be used as a small-signal amplifier, a Q-point must be established, as indicated in the figure, for maximum symmetrical swing. Because of the exponential input voltage function, as given in Equation (10.82), the input voltage range over which both Q_0 and Q_2 remain in their active regions is very small. A sinusoidal variation in the input voltage produces a sinusoidal variation in the output voltage as shown in the figure.

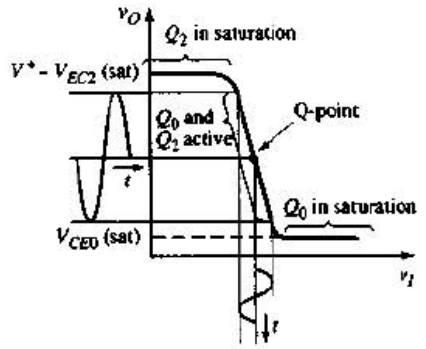


Figure 10.30 Voltage transfer characteristics of bipolar circuit with active load

In addition to the voltage transfer function, we can also consider the load curve. Figure 10.31 shows the transistor characteristics of the driver transistor Q_0 for several values of B–E or V_I voltages. Superimposed on these curves is the load curve, which essentially is the I_C versus V_{EC} characteristic of the active load Q_2 at a constant V_{EB} voltage.

The Q-point shown corresponds to a quiescent input voltage V_{IQ}. From the curve, we see that as the input changes between V_{IH} and V_{IL}, the Q-point moves up and down the load curve producing a change in output voltage. Also, as V_I increases to V_{I2}, the driver transistor Q_0 is driven into saturation; as V_I decreases to V_{I1}, the load transistor Q_2 is driven into saturation.

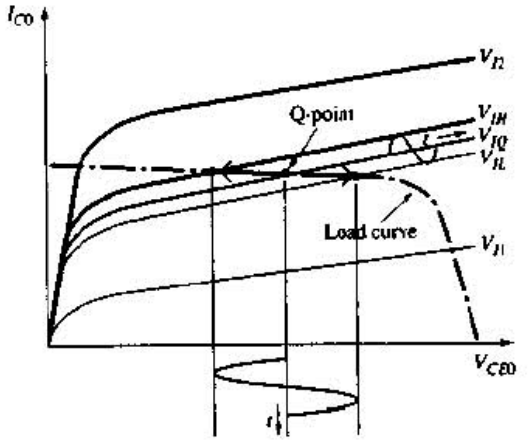


Figure 10.31 Driver transistor characteristics and load curve for BJT circuit with active load

10.3.2 Voltage Gain: BJT Active Load Circuit

The small-signal voltage gain of a circuit is the slope of the voltage transfer function curve at the Q-point. For the bipolar circuit with an active load, the voltage gain can be found by taking the derivative of Equation (10.82) with respect to V_I, as follows:

$$A_v = \frac{dV_O}{dV_I} = -\left(\frac{V_{AN}V_{AP}}{V_{AN}+V_{AP}}\right)\left(\frac{I_{S0}}{I_{REF}}\right)\left(\frac{1}{V_T}\right)e^{V_I/V_T} \tag{10.84}$$

As a good approximation, we can write that

$$I_{REF} \cong I_{S0}e^{V_I/V_T} \tag{10.85}$$

Equation (10.84) then becomes

$$A_v = \frac{dV_O}{dV_I} = -\left(\frac{V_{AN}V_{AP}}{V_{AN}+V_{AP}}\right)\left(\frac{1}{V_T}\right) = \frac{-\left(\frac{1}{V_T}\right)}{\frac{1}{V_{AN}}+\frac{1}{V_{AP}}} \tag{10.86}$$

The small-signal voltage gain is a function of the Early voltages and the thermal voltage. The voltage gain, given by Equation (10.86), relates to the open-circuit condition. When a load is connected to the output, the voltage gain is degraded, as we will see in the next section.

Example 10.10 **Objective:** Calculate the open-circuit voltage gain of a simple BJT amplifier with an active load.

Consider the circuit shown in Figure 10.29. The transistor parameters are $V_{AN} = 120\,\text{V}$ and $V_{AP} = 80\,\text{V}$. Let $V_T = 0.026\,\text{V}$.

Solution: From Equation (10.86), the small-signal, open-circuit voltage gain is

$$A_v = \frac{-\left(\frac{1}{V_T}\right)}{\frac{1}{V_{AN}} + \frac{1}{V_{AP}}} = \frac{-\left(\frac{1}{0.026}\right)}{\frac{1}{120} + \frac{1}{80}} = \frac{-38.46}{0.00833 + 0.0125} = -1846$$

Comment: For a circuit with an active load, the magnitude of the small-signal, open-circuit voltage gain is substantially larger than the resulting gain when a discrete resistor load is used.

Computer Verification: The voltage transfer characteristics of the active load circuit in Figure 10.29 were determined for a standard 2N3904 transistor as the npn device and standard 2N3906 transistors as the pnp devices. The circuit was biased at 5 V and the resistor was set at $R = 1\,\text{k}\Omega$. The transfer curve is shown in Figure 10.32.

The input transition region, during which both Q_0 and Q_2 remain biased in the forward-active mode, is indeed very narrow. The slope of the curve, which is the voltage gain, is found to be -572. The reason for the smaller value compared to the hand calculation is that the Early voltages of these standard transistors are smaller than assumed in the previous calculation. The Early voltage of the npn device is 74 V and that of the npn devices is only 18.7 V.

Design Pointer: From the transfer characteristics in Figure 10.32, we can see that, for this circuit, it would be very difficult to apply the required input voltage to bias both Q_0 and Q_2 in the active region. This particular circuit, therefore, is not practical as an amplifier. However, the circuit does demonstrate the basic properties of an active load. In Chapters 11 and 13, we will see how an active load is applied to actual circuits.

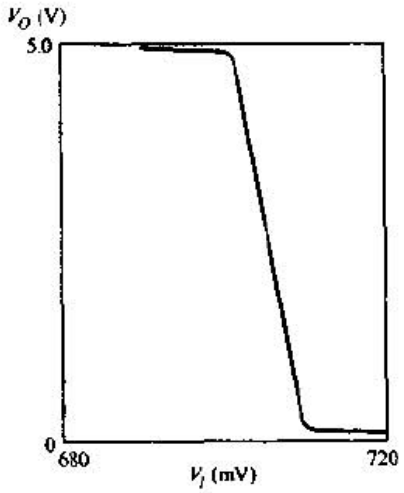


Figure 10.32 Graphical output from a PSpice analysis, showing voltage transfer characteristics of bipolar active load circuit

Test Your Understanding

***10.19** A simple BJT amplifier with active load is shown in Figure 10.29. The transistor parameters are: $I_{S0} = I_{S1} = I_{S2} = 10^{-12}$ A and $V_{AN} = V_{AP} = 100$ V. Let $V^+ = 5$ V. (a) Determine the value of V_{EB2} such that $I_{REF} = 0.5$ mA. (b) Find the value of R_1. (c) What value of V_I will produce $V_{CE0} = V_{EC2}$? (d) Determine the open-circuit, small-signal voltage gain. (Ans. (a) $V_{EB2} = 0.521$ V (b) $R_1 = 8.96\,\text{k}\Omega$ (c) $V_I = 0.521$ V (d) $A_V = -1923$)

***10.20** Repeat Exercise 10.19 if the transistor parameters are $I_{S0} = I_{S1} = I_{S2} = 5 \times 10^{-14}$ A, and if I_{REF} is 0.1 mA. Verify the results with a PSpice analysis. (Ans. (a) $V_{EB2} = 0.557$ V (b) $R_1 = 44.4\,\text{k}\Omega$ (c) $V_I = 0.557$ V (d) $A_V = -1923$)

10.3.3 DC Analysis: MOSFET Active Load Circuit

Consider the circuit in Figure 10.33. Transistors M_1 and M_2 form a PMOS active load circuit, and M_2 is the active load device. We will consider the voltage transfer function of V_O versus V_I for this circuit.

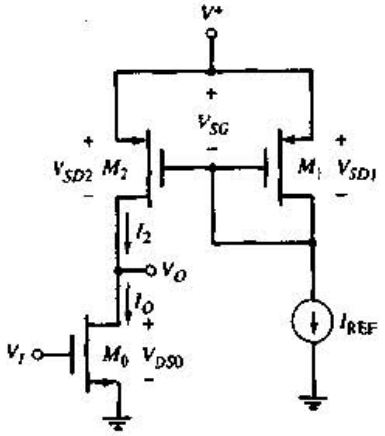


Figure 10.33 Simple MOSFET amplifier with active load, showing currents and voltages

The reference current may be written in the form

$$I_{REF} = K_{p1}(V_{SG} + V_{TP1})^2(1 + \lambda_1 V_{SD1}) \tag{10.87}$$

The drain current I_2 is

$$I_2 = K_{p2}(V_{SG} + V_{TP2})^2(1 + \lambda_2 V_{SD2}) \tag{10.88}$$

If we assume that M_1 and M_2 are identical, then $\lambda_1 = \lambda_2 \equiv \lambda_p$, $V_{TP1} = V_{TP2} \cong V_{TP}$, and $K_{p1} = K_{p2} \cong K_p$. Combining equations, we find the output voltage as

$$V_O = \frac{[1 + \lambda_p(V^+ - V_{SG})]}{\lambda_n + \lambda_p} - \frac{K_n(V_I - V_{TN})^2}{I_{REF}(\lambda_n + \lambda_p)} \tag{10.89}$$

Equation (10.89) describes the V_O versus V_I characteristic of the circuit, provided that both M_0 and M_2 remain biased in their saturation regions. Figure 10.34 shows a sketch of the voltage transfer characteristics. If the circuit is to be used as a small-signal amplifier, then a Q-point must be established, as indicated on the figure, for maximum symmetrical swing. As before, the input transition region in which both M_0 and M_2 are biased in the saturation region is quite narrow. A sinusoidal variation in the input voltage produces a sinusoidal variation in the output voltage as shown in the figure.

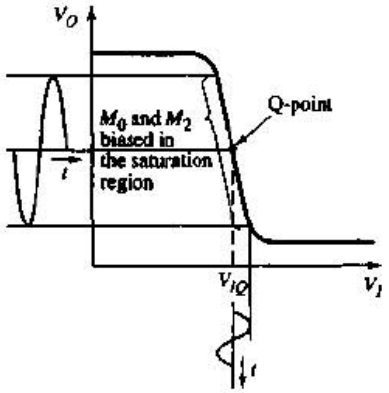


Figure 10.34 Voltage transfer characteristic of MOSFET circuit with active load

We can also consider the load curve for this device. Figure 10.35 shows the transistor characteristics of the driver transistor M_0 for several values of gate-to-source or V_I voltages. Superimposed on these curves is the load curve, which essentially is the I_D versus V_{SD} characteristic of the active load M_2 at a constant V_{SG} voltage.

The Q-point shown corresponds to a quiescent input voltage V_{IQ}. From the curve, we see that as the input changes between V_{IH} and V_{IL}, the Q-point moves up and down the load curve producing a change in output voltage. Also, as V_I increases to V_{I2}, the driver transistor M_0 is driven into the nonsaturation

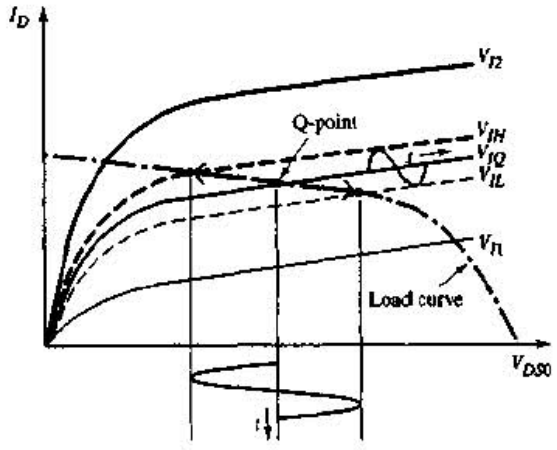


Figure 10.35 Driver transistor characteristics and load curve for MOSFET circuit with active load

region; as V_I decreases to V_{I1}, the load transistor M_2 is driven into the non-saturation region.

10.3.4 Voltage Gain: MOSFET Active Load Circuit

The small-signal voltage gain of a MOSFET circuit with an active load is also the slope of the voltage transfer function curve at the Q-point. Taking the derivative of Equation (10.89) with respect to V_I, we obtain

$$A_v = \frac{dV_O}{dV_I} = \frac{-2K_n(V_I - V_{TN})}{I_{REF}(\lambda_n + \lambda_p)} \tag{10.90}$$

The transconductance of the driver transistor is $g_m = 2K_n(V_I - V_{TN})$. Since M_1 and M_2 are assumed to be identical, then $I_O = I_{REF}$, and the small-signal transistor resistances are $r_{on} = 1/\lambda_n I_{REF}$ and $r_{op} = 1/\lambda_p I_{REF}$. From Equation (10.90), the small-signal, open-circuit voltage gain can now be written

$$A_v = \frac{-g_m}{\left(\dfrac{1}{r_{on}} + \dfrac{1}{r_{op}}\right)} = -g_m(r_{on} \| r_{op}) \tag{10.91}$$

In general, the transconductance g_m of a MOSFET is less than that of a BJT; therefore, the voltage gain of a MOSFET amplifier with an active load is less than that of a BJT amplifier with an active load. However, the active load still produces a significant increase in the voltage gain.

10.3.5 Discussion

In considering the BJT circuit with active load (Figure 10.29) and MOSFET circuit with active load (Figure 10.33), we could have directly considered the small-signal analysis without the dc analysis. However, it is important to understand how narrow the input transition width is (Figure 10.32) such that the transistors are biased correctly. For this reason, the use of active loads in discrete circuits is almost impossible. The biasing of the circuit with an active load depends to a large extent on the use of matched transistors. Matched transistors can be achieved on an integrated circuit. So in considering the small-signal analysis in the next section, we must keep in mind the very narrow range in which the transistors are biased in the active region.

Test Your Understanding

10.21 Consider the simple MOSFET amplifier with active load in Figure 10.33. The transistor parameters are: $V_{TN} = 1\,\text{V}$, $V_{TP} = -1\,\text{V}$, $K_p = K_n = 0.2\,\text{mA/V}^2$, and $\lambda_p = \lambda_n = 0.015\,\text{V}^{-1}$. Let $V^+ = 10\,\text{V}$ and $I_{REF} = 0.25\,\text{mA}$. (a) Find V_{SG}. (b) What value of V_I will produce $V_{DSO} = V_{SD2}$? (c) Determine the open-circuit, small-signal voltage gain. (Ans. (a) $V_{SG} = 2.12\,\text{V}$ (b) $V_I = 2.10\,\text{V}$ (c) $A_v = -58.7$)

10.22 Repeat Exercise 10.21 if the transistor parameters are $K_p = K_n = 50\,\mu\text{A/V}^2$, and if I_{REF} is $80\,\mu\text{A}$. Verify the results with a PSpice analysis (Ans. (a) $V_{SG} = 2.26\,\text{V}$ (b) $V_I = 2.24\,\text{V}$ (c) $A_v = -51.7$)

10.4 SMALL-SIGNAL ANALYSIS: ACTIVE LOAD CIRCUITS

The small-signal voltage gain of a circuit with an active load can be determined from the small-signal equivalent circuit. This is probably the easiest and most direct method of obtaining the gain of such circuits. Again, the dc analysis of these circuits, as shown in the previous section, clearly demonstrates the narrow range of input voltages over which the transistors will remain biased in the active region. The load curves in Figure 10.31 for the BJT circuit and in Figure 10.35 for the MOSFET circuit also help in visualizing the operation of these circuits. Even though a small-signal analysis is extremely useful for determining the voltage gain, we must not lose sight of the physical operation of these circuits, which is described through the dc analysis. If the BJTs are not biased in the active region or the MOSFETs are not biased in the saturation region, the small-signal analysis is not valid.

10.4.1 Small-Signal Analysis: BJT Active Load Circuit

To find the small-signal voltage gain of the BJT circuit with an active load, we must determine the resistance looking into the collector of the active load device. Figure 10.36 is the small-signal equivalent circuit of the entire active load circuit in Figure 10.29, which uses pnp transistors. The base, collector, and emitter terminals of the two transistors are indicated on the figure.

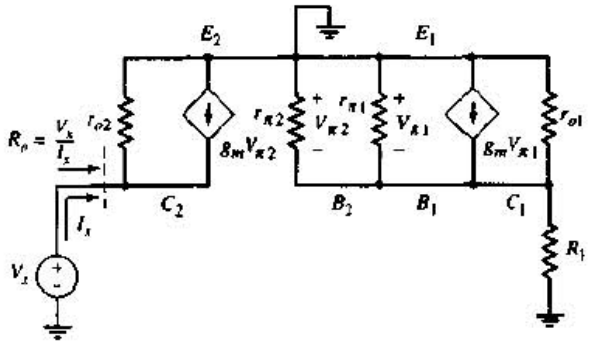


Figure 10.36 Small-signal equivalent circuit of BJT active load circuit

In the Q_1 portion of the equivalent circuit, there are no independent ac sources to excite any currents or voltages. Therefore, $V_{\pi 1} = V_{\pi 2} = 0$, which means that the dependent source $g_m V_{\pi 2}$ is zero and is equivalent to an open circuit. The resistance looking into the collector of Q_2 is just

$$R_o = r_{o2} \tag{10.92}$$

We will use this equivalent resistance to calculate the small-signal voltage gain of the amplifier.

Figure 10.37(a) shows a simple amplifier with an active load and the output voltage capacitively coupled to passive load R_L. The small-signal equivalent circuit, shown in Figure 10.37(b), includes the load resistance R_L, the resistance r_{o2} of the active load, and the output resistance r_o of the amplifying transistor Q_0.

(a) (b)

Figure 10.37 (a) Simple BJT amplifier with active load and load resistance and (b) small-signal equivalent circuit

The output voltage is

$$V_o = -(g_m V_{\pi 1})(r_o \| R_L \| r_{o2}) \tag{10.93}$$

Since $V_{\pi 1} = V_i$, where V_i is the ac input voltage, the small-signal voltage gain is

$$A_v = \frac{V_o}{V_i} = -g_m(r_o \| R_L \| r_{o2}) = \frac{-g_m}{\left(\frac{1}{r_o} + \frac{1}{R_L} + \frac{1}{r_{o2}}\right)} \tag{10.94}$$

The small-signal voltage gain can also be written

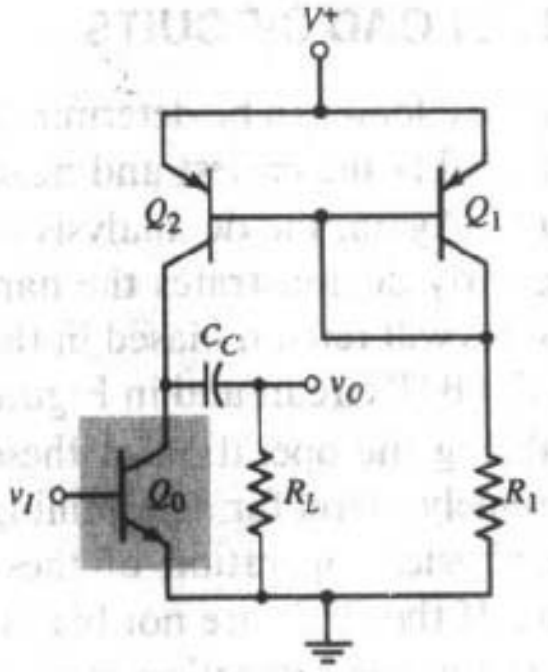
$$A_v = \frac{-g_m}{g_o + g_L + g_{o2}} \tag{10.95}$$

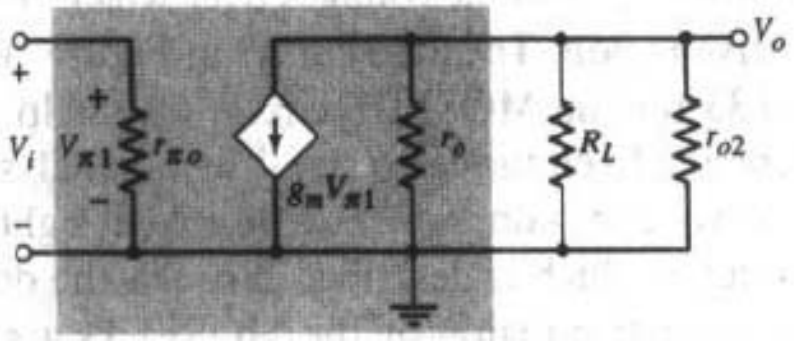
where g_o and g_{o2} are the output conductances of Q_0 and Q_2, and g_L is the load conductance. The transconductance is $g_m = I_{Co}/V_T$, the small-signal conductances are $g_o = I_{Co}/V_{AN}$ and $g_{o2} = I_{Co}/V_{AP}$, and the load conductance is $g_L = 1/R_L$. Therefore, Equation (10.95) becomes

$$A_v = \frac{-\left(\frac{I_{Co}}{V_T}\right)}{\left(\frac{I_{Co}}{V_{AN}} + \frac{1}{R_L} + \frac{I_{Co}}{V_{AP}}\right)} \tag{10.96}$$

If the passive load is an open circuit ($R_L \to \infty$), the small-signal voltage gain is identical to that determined from the dc analysis as given by Equation (10.86). If the load resistance R_L is not an open circuit, then the magnitude of the small-signal voltage gain is reduced.

Example 10.11 **Objective:** Calculate the small-signal voltage gain of an amplifier with an active load and a load resistance R_L.


V+
Q2
Q1
CC
vO
vI
Q0
RL
R1


+
Vi
−
+
Vπ1
−
rπo
gmVπ1
ro
RL
ro2
Vo

For the circuit in Figure 10.37(a), the transistor parameters are $V_{AN} = 120\,\text{V}$ and $V_{AP} = 80\,\text{V}$. Let $V_T = 0.026\,\text{V}$ and $I_{Co} = 1\,\text{mA}$. Determine the small-signal voltage gain for load resistances of $R_L = \infty$, $100\,\text{k}\Omega$, and $10\,\text{k}\Omega$.

Solution: For $R_L = \infty$, Equation (10.96) reduces to

$$A_v = \frac{-\left(\frac{1}{V_T}\right)}{\left(\frac{1}{V_{AN}} + \frac{1}{V_{AP}}\right)} = \frac{-\left(\frac{1}{0.026}\right)}{\left(\frac{1}{120} + \frac{1}{80}\right)} = -1846$$

which is the same as that determined for the open-circuit configuration in Example 10.10.

For $R_L = 100\,\text{k}\Omega$, the small-signal voltage gain is

$$A_v = \frac{-\left(\frac{1}{0.026}\right)}{\left(\frac{1}{120} + \frac{1}{100} + \frac{1}{80}\right)} = \frac{-38.46}{0.00833 + 0.010 + 0.0125} = -1247$$

and for $R_L = 10\,\text{k}\Omega$, the voltage gain is

$$A_v = \frac{-\left(\frac{1}{0.026}\right)}{\left(\frac{1}{120} + \frac{1}{10} + \frac{1}{80}\right)} = \frac{-38.46}{0.00833 + 0.10 + 0.0125} = -318$$

Comment: The small-signal voltage gain is a strong function of the load resistance R_L. As the value of R_L decreases, the loading effect becomes more severe.

Design Pointer: If an amplifier with an active load is to drive another amplifier stage, the loading effect must be taken into account when the small-signal voltage gain is determined. Also, the input resistance of the next stage must be large in order to minimize the loading effect.

Problem-Solving Technique: Active Loads

1. Ensure that the active load devices are biased in the forward-active mode.
2. The small-signal analysis of the circuit with an active load then simply involves considering the output resistance looking into the output of the active load device as well as the equivalent circuit of the amplifying transistor.

Test Your Understanding

10.23 For the circuit in Figure 10.37(a), the transistor parameters are $V_{AN} = V_{AP} = 80\,\text{V}$. Let $I_{Co} = 0.8\,\text{mA}$. (a) Determine the open-circuit small-signal voltage gain. (b) Find the value of R_L that results in a voltage gain of one-half the open-circuit value. (Ans. (a) $A_v = -1540$ (b) $R_L = 50\,\text{k}\Omega$)

10.24 In the circuit shown in Figure 10.37(a), the transistor parameters are $V_{AN} = 120\,\text{V}$ and $V_{AP} = 80\,\text{V}$. Let $I_{Co} = 0.5\,\text{mA}$ and $R_L = 50\,\text{k}\Omega$. (a) Determine the small-

signal parameters g_m, r_o, and r_{o2}. (b) Find the small-signal voltage gain. (Ans. (a) $g_m = 19.2\,\text{mA/V}$, $r_o = 240\,\text{k}\Omega$, $r_{o2} = 160\,\text{k}\Omega$ (b) $A_v = -631$)

10.4.2 Small-Signal Analysis: MOSFET Active Load Circuit

The small-signal voltage gain of a MOSFET amplifier with an active load can also be determined from the small-signal equivalent circuit. Figure 10.38 is the small-signal equivalent circuit of the entire MOSFET active load in Figure 10.33. The signal voltages V_{sg1} and V_{sg2} are zero, since there is no ac excitation in this part of the circuit. This means that $g_m V_{sg2} = 0$ and

$$R_o = r_{o2} \tag{10.97}$$

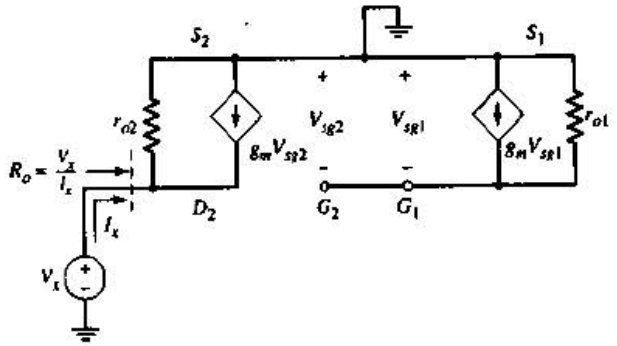
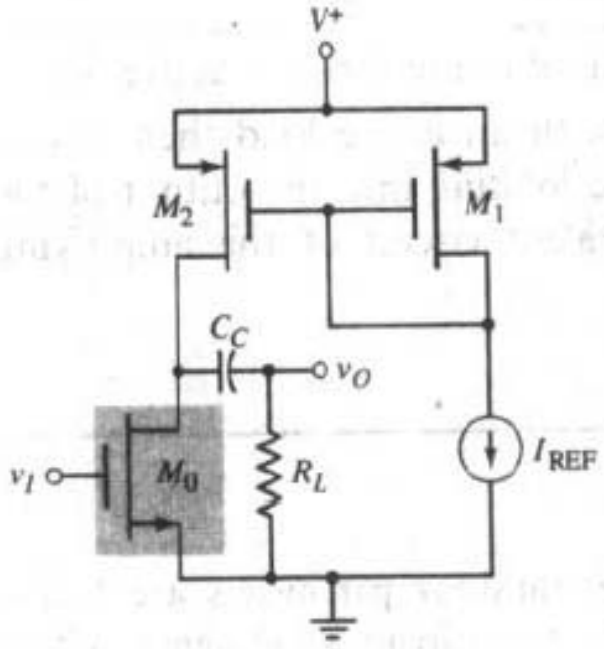


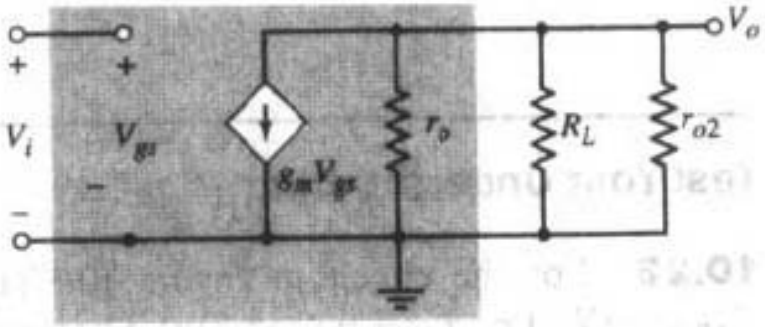
Figure 10.38 Small-signal equivalent circuit of the MOSFET active load circuit

A simple MOSFET amplifier with an active load, and a load resistor R_L capacitively coupled to the output, is shown in Figure 10.39(a). Figure 10.39(b) shows the small-signal equivalent circuit, in which the load R_L, the active load resistance r_{o2}, and the output resistance r_o of transistor M_0 are included.

(a) (b)

Figure 10.39 (a) Simple MOSFET amplifier with active load and load resistance and (b) small-signal equivalent circuit


V+
M2
M1
CC
vO
vI
M0
RL
IREF


Vo
+
Vi
Vgs
−
gmVgs
ro
RL
ro2

The output voltage is

$$V_o = -g_m V_{gs}(r_o \| R_L \| r_{o2}) \tag{10.98}$$

and since $V_{gs} = V_i$, where V_i is the ac voltage, the small-signal voltage gain is

$$A_v = \frac{V_o}{V_i} = -g_m(r_o \| R_L \| r_{o2}) = \frac{-g_m}{g_o + g_L + g_{o2}} \tag{10.99}$$

The parameters g_o and g_{o2} are the output conductances of M_0 and M_2, and g_L is the load conductance. This expression for the small-signal voltage gain of a MOSFET amplifier with active load is the same as that of the BJT amplifier.

A load resistance R_L tends to degrade the gain and to cause a loading effect, as it did in the bipolar circuit with an active load. However, in MOSFET amplifiers, the output may be connected to the gate of another MOSFET amplifier in which the effective R_L is very large.

Example 10.12 **Objective:** Calculate the small-signal voltage gain of an NMOS amplifier with an active load.

For the amplifier shown in Figure 10.39(a) the transistor parameters are: $\lambda_n = \lambda_p = 0.01\ \text{V}^{-1}$, $V_{TN} = 1\ \text{V}$, and $K_n = 1\ \text{mA/V}^2$. Assume M_1 and M_2 are matched and $I_{REF} = 0.5\ \text{mA}$. Calculate the small-signal voltage gain for load resistances of $R_L = \infty$ and $100\ \text{k}\Omega$.

Solution: Since M_1 and M_2 are matched, then $I_O = I_{REF}$, and the transconductance is

$$g_m = 2\sqrt{K_n I_{REF}} = 2\sqrt{(1)(0.5)} = 1.41\ \text{mA/V}$$

The small-signal transistor conductances are

$$g_o = g_{o2} = \lambda I_{REF} = (0.01)(0.5) = 0.005\ \text{mA/V}$$

For $R_L = \infty$, Equation (10.99) reduces to

$$A_v = \frac{-g_m}{g_o + g_{o2}} = \frac{-1.41}{0.005 + 0.005} = -141$$

For $R_L = 100\ \text{k}\Omega$ ($g_L = 0.01\ \text{mA/V}$), the voltage gain is

$$A_v = \frac{-g_m}{g_o + g_L + g_{o2}} = \frac{-1.41}{0.005 + 0.01 + 0.005} = -70.5$$

Comment: The magnitude of the small-signal voltage gain of MOSFET amplifiers with active loads is substantially larger than for those with resistive loads, but it is still smaller than equivalent bipolar circuits, because of the smaller transconductance for the MOSFET.

10.4.3 Small-Signal Analysis: Advanced MOSFET Active Load

The active loads considered in the BJT (Figure 10.37) and MOSFET (Figure 10.39(a)), circuits correspond to the simple two-transistor current mirrors. We may use a more advanced current mirror with a high output resistance as an active load to increase the amplifier gain. Figure 10.40(a) shows a MOSFET cascode amplifying stage with a cascode active load. The small-signal

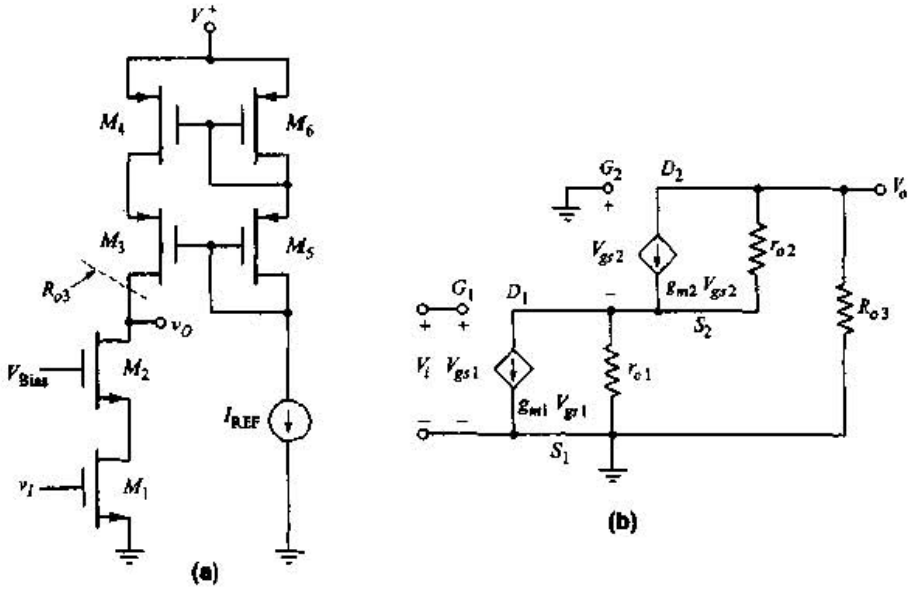


Figure 10.40 (a) MOSFET cascode amplifying stage with cascode active load; (b) small-signal equivalent circuit

equivalent circuit is shown in Figure 10.40(b), where R_{o3} is the effective resistance looking into the drain of M_3. From our discussion of the cascode current mirror, we found $R_{o3} = r_{o3} + r_{o4}(1 + g_m r_{o3})$ (Equation (10.57)).

We can assume all transistors are matched so that the currents in all transistors are equal. Summing currents at D_1, we have

$$g_m V_{gs1} + \frac{(-V_{gs2})}{r_{o1}} = g_m V_{gs2} + \frac{V_o - (-V_{gs2})}{r_{o2}} \tag{10.100}$$

Summing currents at the output node, we find

$$\frac{V_o}{R_{o3}} + \frac{V_o - (-V_{gs2})}{r_{o2}} + g_m V_{gs2} = 0 \tag{10.101}$$

Eliminating V_{gs2} from the two equations, noting that $V_{gs1} = V_i$, and assuming $g_m \gg 1/r_o$, we find the small-signal voltage gain is

$$A_v = \frac{V_o}{V_i} = \frac{-g_m^2}{\dfrac{g_m}{R_{o3}} + \dfrac{1}{r_{o1} r_{o2}}} \tag{10.102}$$

The resistance R_{o3} is approximately $R_{o3} \cong g_m r_{o3} r_{o4}$, so the gain can be written as

$$A_v = \frac{-g_m^2}{\dfrac{1}{r_{o3} r_{o4}} + \dfrac{1}{r_{o1} r_{o2}}} \tag{10.103}$$

For the same transistor parameters given in Example 10.12, the small-signal voltage gain of this circuit would be 39,762! However, a word of warning is in order. As we mentioned previously, output resistances in the hundreds of megohm range are ideal and will, in reality, be limited by leakage currents. For

this reason, a voltage gain of 39,000 in a one-stage amplifier will probably not be achieved. However, the voltage gain of this amplifier should be substantially larger than the amplifier using a simple active load.

Test Your Understanding

10.25 For the circuit in Figure 10.39(a), the transistor parameters are: $\lambda_n = \lambda_p = 0.02\,\text{V}^{-1}$, $K_n = K_p = 0.25\,\text{mA/V}^2$, $V_{TN} = 1\,\text{V}$, and $V_{TP} = -1\,\text{V}$. Let $V^+ = 10\,\text{V}$ and $I_{REF} = 0.40\,\text{mA}$. (a) Determine V_{IQ}. (b) Find the open-circuit small-signal voltage gain. (c) Find the value of R_L that results in a voltage gain of one-half the open-circuit value. (Ans. (a) $V_{IQ} = 2.26\,\text{V}$ (b) $A_v = -39.4$ (c) $R_L = 62.5\,\text{k}\Omega$)

10.26 In the circuit in Figure 10.39(a), the transistor parameters are: $K_p = 0.1\,\text{mA/V}^2$, $K_n = 0.2\,\text{mA/V}^2$, $V_{TN} = 1\,\text{V}$, $V_{TP} = -1\,\text{V}$, $\lambda_n = 0.01\,\text{V}^{-1}$, and $\lambda_p = 0.02\,\text{V}^{-1}$. Let $V^+ = 10\,\text{V}$, $I_{REF} = 0.25\,\text{mA}$, and $R_L = 100\,\text{k}\Omega$. (a) Determine the small-signal parameters g_m (for M_0), r_{on}, and r_{op}. (b) Find the small-signal voltage gain. (Ans. (a) $g_m = 0.448\,\text{mA/V}$, $r_{on} = 400\,\text{k}\Omega$, $r_{op} = 200\,\text{k}\Omega$ (b) $A_v = -25.6$)

10.5 SUMMARY

- This chapter addressed the biasing of bipolar and FET circuits with constant-current sources. The basic bipolar current source is the simple two-transistor circuit with a resistor to establish the reference current. The basic FET current source is also a simple two-transistor circuit but includes additional transistors in the reference portion of the circuit.
- One parameter of interest in the current source circuit is the output resistance, which determines the stability of the bias current. More sophisticated current-source circuits, such as the Widlar and Wilson circuits in the BJT configuration and the Wilson and cascode in the FET configuration, have larger output resistance parameters and increased bias-current stability.
- Multitransistor output stages, in both bipolar and FET circuits, are used to bias multiple amplifier stages using a single reference current. These circuits, called current mirrors, reduce the number of elements required to bias amplifier stages throughout an IC.
- Both bipolar and MOSFET active load circuits were analyzed. Active loads are essentially constant current source circuits and replace the discrete collector resistor and drain resistor. The active loads produce a much larger small-signal voltage gain compared to discrete resistor circuits.

CHECKPOINT

After studying this chapter, the reader should have the ability to:

✔ Analyze and design a simple two-transistor BJT current-source circuit to produce a given bias current. (Section 10.1)

✔ Analyze and design more sophisticated BJT current-source circuits, such as the three-transistor circuit, cascode circuit, Wilson circuit, and Widlar circuit. (Section 10.1)

✔ Analyze the output resistance of the various BJT current-source circuits and design a BJT current-source circuit to yield a specified output resistance. (Section 10.1)

- ✔ Analyze and design a basic two-transistor MOSFET current-source circuit with additional MOSFET devices in the reference portion of the circuit to yield a given bias current. (Section 10.2)
- ✔ Analyze and design more sophisticated MOSFET current-source circuits, such as the cascode circuit, Wilson circuit, and wide-swing cascode circuit. (Section 10.2)
- ✔ Analyze the output resistance of the various MOSFET current-source circuits and design a MOSFET current-source circuit to yield a specified output resistance. (Section 10.2)
- ✔ Describe the operation and characteristics of a BJT and MOSFET active load circuit. (Section 10.3)
- ✔ Discuss the reason for the increased small-signal voltage gain when an active load is used. (Section 10.3)

REVIEW QUESTIONS

1. Sketch the basic BJT two-transistor current source and explain the operation.
2. Explain the significance of the output resistance of the current-source circuit.
3. Discuss the effect of mismatched transistors on the characteristics of the BJT two-transistor current source.
4. Discuss the advantage of the BJT three-transistor current source.
5. What is the primary advantage of a BJT cascode current source?
6. Sketch a Widlar current source and explain the operation.
7. Can a piecewise linear model of the transistor be used in the analysis of the Widlar current source? Why or why not?
8. Discuss the operation and significance of a multiple-output transistor current mirror.
9. Sketch the basic MOSFET two-transistor current-source circuit and discuss its operation.
10. Discuss the effect of mismatched transistors on the characteristics of the MOSFET two-transistor current source.
11. Discuss how the reference portion of the circuit can be designed with MOSFETs only.
12. Sketch a MOSFET cascode current source circuit and discuss the advantages of this design.
13. Discuss the operation of an active load.
14. What is the primary advantage of using an active load?
15. Sketch the voltage transfer characteristics of a simple amplifier with an active load. Where should the Q-point be placed?
16. What is the impedance seen looking into a simple active load?
17. What is the advantage of using a cascode active load?

PROBLEMS

Section 10.1 Bipolar Transistor Current Sources

10.1 Figure P10.1 shows another form of a bipolar current source. (a) Neglecting base currents, derive the expression for I_C in terms of the circuit, transistor, and diode parameters. (b) If the transistor B–E and diode voltages are equal, show that, for $R_1 = R_2$, the expression for I_C reduces to

$$I_C = \frac{(-V^-)}{2R_3}$$

(c) For $V^- = -10\,\text{V}$ and $V_{BE}(\text{on}) = V_\gamma = 0.7\,\text{V}$, design the circuit such that $I_C = I_1 = I_2 = 2\,\text{mA}$.

10.2 The transistor parameters for the circuit in Figure 10.2(b) are: $V_{BE}(\text{on}) = 0.7\,\text{V}$, $\beta = 50$, and $V_A = \infty$. Let $V^+ = 5\,\text{V}$ and $V^- = 0$. For $I_{\text{REF}} = 1\,\text{mA}$, determine I_{C1}, I_{B1}, I_{B2}, and I_{C2}.

10.3 (a) For the circuit in Figure 10.2(b), the bias voltages are $V^+ = +15\,\text{V}$ and $V^- = -15\,\text{V}$. Assume Q_1 and Q_2 are matched, and assume $V_{BE}(\text{on}) = 0.7\,\text{V}$. Neglecting base currents, find R_1 such that $I_{\text{REF}} = I_O = 0.5\,\text{mA}$. (b) The upper terminal of R_1 may instead be connected to ground potential. Find R_1 such that $I_{\text{REF}} = I_O = 0.5\,\text{mA}$ for this case. Discuss any advantage of connecting R_1 to ground rather than to the V^+ power supply. (c) Determine the change in I_O if R_1 varies by ±5 percent from the design values of parts (a) and (b).

D10.4 For the basic two-transistor current source in Figure 10.2(b), the transistor parameters are: $\beta = 100$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, and $V_A = 80\,\text{V}$. Let $V^+ = 15\,\text{V}$ and $V^- = 0$. (a) Design the circuit such that $I_O = 2\,\text{mA}$ when $V_{C2} = 0.7\,\text{V}$. (b) What is the percent change in I_O as V_{C2} varies between 0.7 V and 10 V?

D10.5 Figure P10.5 shows a basic two-transistor pnp current source. The transistor parameters are: $\beta = 25$, $V_{EB}(\text{on}) = 0.7\,\text{V}$, and $V_A = \infty$. Design the circuit such that $I_O = 0.5\,\text{mA}$. What is the value of I_{REF}?

10.6 In the circuit in Figure P10.5, the transistor parameters are $\beta = 50$, $V_{EB}(\text{on}) = 0.7\,\text{V}$, and $V_A = 50\,\text{V}$. Let $R_1 = 18\,\text{k}\Omega$. Determine I_O for: (a) $V_{EC2} = 0.7\,\text{V}$, (b) $V_{EC2} = 2\,\text{V}$, and (c) $V_{EC2} = 4\,\text{V}$.

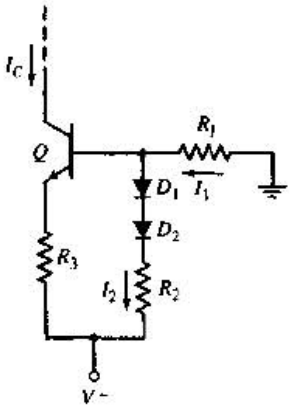


Figure P10.1

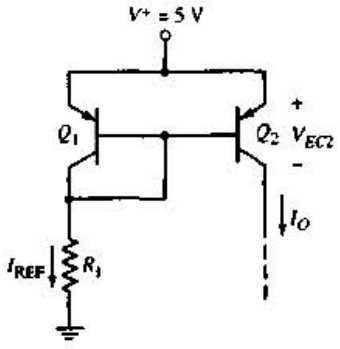


Figure P10.5

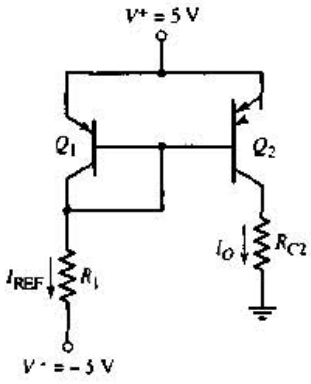


Figure P10.7

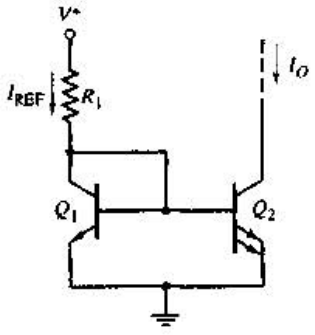


Figure P10.9

D10.7 Consider the pnp current source in Figure P10.7, with transistor parameters $\beta = \infty$, $V_A = \infty$, and $V_{EB}(\text{on}) = 0.7\,\text{V}$. (a) Design the circuit such that $I_{\text{REF}} = 1\,\text{mA}$. (b) What is the value of I_O? (c) What is the maximum value of R_{C2} such that Q_2 remains biased in the forward-active mode?

10.8 The transistors in the basic current mirror in Figure 10.2(b) have a finite β and an infinite Early voltage. The B–E area of Q_2 is n times that of Q_1. Derive the expression for I_O in terms of I_{REF}, β, and n.

D10.9 The transistor Q_2 shown in Figure P10.9 is equivalent to two transistors in parallel, each of which is matched to Q_1. Assume the transistor parameters are: $V_{BE}(\text{on}) = 0.7\,\text{V}$, $\beta = 50$, and $V_A = \infty$. For $V^+ = 5\,\text{V}$, design the circuit such that $I_O = 2\,\text{mA}$. What is the value of I_{REF}?

10.10 Using the basic two-transistor topology biased at $V^+ = +5\,\text{V}$ and $V^- = -5\,\text{V}$ with npn transistors that have $v_{BE} = 0.7\,\text{V}$ at 1 mA, design a current source that provides a bias current of 1.5 mA and a reference current of 0.5 mA. Neglect base currents.

10.11 The values of β for the transistors in Figure P10.11 are very large. (a) If Q_1 is diode-connected with $I_1 = 0.5\,\text{mA}$, determine the collector currents in the other two transistors. (b) Repeat part (a) if Q_2 is diode-connected with $I_2 = 0.5\,\text{mA}$. (c) Repeat part (a) if Q_3 is diode-connected with $I_3 = 0.5\,\text{mA}$.

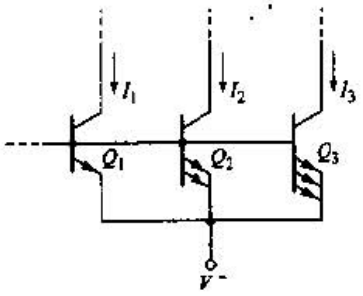


Figure P10.11

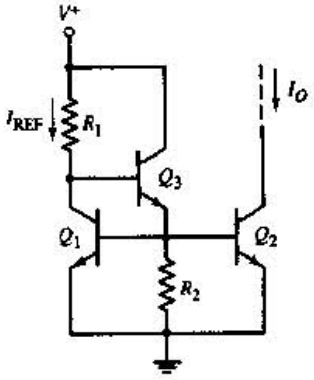


Figure P10.12

10.12 Consider the circuit in Figure P10.12. The transistor parameters are: $\beta = 80$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, and $V_A = \infty$. (a) Derive the expression for I_O in terms of I_{REF}, β, and R_2. (b) For $R_2 = 10\,\text{k}\Omega$ and $V^+ = 10\,\text{V}$, design the circuit such that $I_O = 0.70\,\text{mA}$. What is the value of I_{REF}?

10.13 All transistors in the N output current mirror in Figure P10.13 are matched, with a finite β and $V_A = \infty$. (a) Derive the expression for each load current in terms of I_{REF} and β. (b) If the circuit parameters are $V^+ = 5\,\text{V}$ and $V^- = -5\,\text{V}$, and the transistor parameter is $\beta = 50$, determine R_1 such that each load current is 0.5 mA for $N = 5$. Assume that $V_{EB}(Q_R) = V_{BE}(Q_S) = 0.7\,\text{V}$.

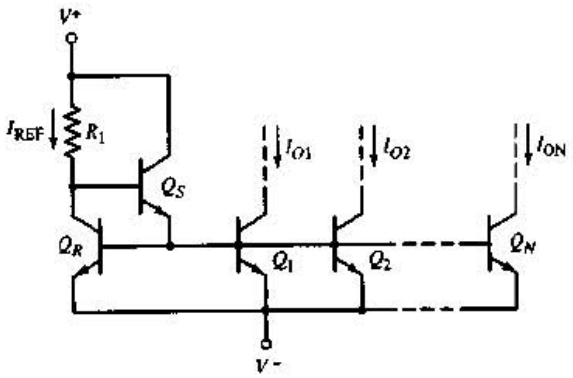


Figure P10.13

D10.14 Design a pnp version of the basic three-transistor current source, using a resistor to establish I_{REF}. The circuit parameters are $V^+ = 5\,\text{V}$ and $V^- = -5\,\text{V}$, and the transistors parameters are: $V_{EB}(\text{on}) = 0.7\,\text{V}$, $\beta = 50$, and $V_A = \infty$. For a load current of 0.5 mA, what is I_{REF}?

D10.15 Design a pnp version of the Wilson current source, using a resistor to establish I_{REF}. The circuit parameters are $V^+ = 9\,V$ and $V^- = -9\,V$, and the transistor parameters are: $V_{EB}(on) = 0.7\,V$, $\beta = 25$, and $V_A = \infty$. If the load current is 0.8 mA, what is I_{REF}?

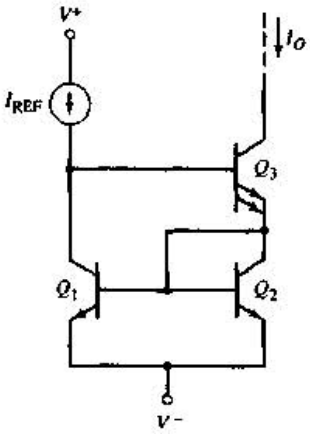


Figure P10.16

***10.16** Consider the Wilson current source in Figure P10.16. The transistors have a finite β and an infinite Early voltage. Derive the expression for I_O in terms of I_{REF} and β.

D10.17 For the transistors in the circuit in Figure P10.17, the parameters are: $V_{BE}(on) = 0.7\,V$, $\beta = 75$, and $V_A = \infty$. Design the circuit such that $I_O = 2\,mA$. What is the value of I_{REF}?

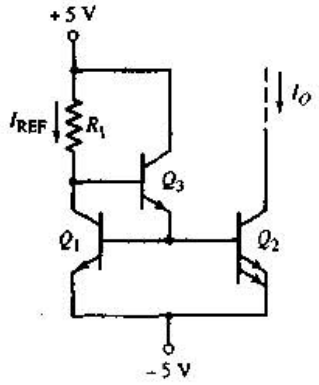


Figure P10.17

10.18 Consider the Wilson current source in Figure 10.8. The reference current is 0.5 mA, and the transistor parameters are: $V_{BE}(on) = 0.7\,V$, $\beta = 80$, and $V_A = 80\,V$. (a) Determine the output resistance looking into the collector of Q_3. (b) What is the change in I_O as the output voltage changes by 5 V?

D10.19 Design the Widlar current source shown in Figure 10.9 such that $I_{REF} = 2\,mA$ and $I_O = 50\,\mu A$. Let $V^+ = 15\,V$ and $V^- = 0$. The transistors are matched, and $V_{BE} = 0.7\,V$ at 1 mA.

10.20 The circuit parameters of the Widlar current source in Figure 10.9 are $V^+ = 10\,V$, $V^- = 0$, and $R_1 = 20\,k\Omega$. The B–E voltage is $V_{BE} = 0.7\,V$ at 1 mA. (a) Determine I_{REF}. (b) Determine R_E such that $I_O = 100\,\mu A$.

10.21 (a) For the Widlar current source in Figure 10.9, find I_{REF}, I_O, and R_o if $R_1 = 100\,k\Omega$, $R_E = 10\,k\Omega$, $V^+ = +5\,V$, and $V^- = -5\,V$. The transistor parameters are $V_{BE}(on) = 0.7\,V$ and $V_A = 30\,V$. (b) Determine the voltage difference $V_{BE1} - V_{BE2}$.

***10.22** Consider the Widlar current source in Problem 10.21. For $\beta = 80$ and $V_A = 80\,V$, determine the change in I_O corresponding to a 5 V change in the output voltage.

***10.23** For the Widlar current source in Figure 10.9, the parameters are: $V^+ = 5\,V$, $V^- = 0$, $I_{REF} = 0.75\,mA$, and $I_O = 25\,\mu A$. Assume $V_{BE1} = 0.7\,V$. If $\beta = 80$ and $V_A = 75\,V$, determine the output resistance looking into the collector of Q_2. What is the percent change in I_O if V_{C2} changes by 3 V?

D10.24 Design a Widlar current source to provide a bias current of $I_O = 100\,\mu A$. The power supplies are $V^+ = 12\,V$ and $V^- = -12\,V$. The maximum resistor value is to be limited to $5\,k\Omega$.

10.25 Consider the Widlar current source in Figure 10.9. The circuit parameters are: $V^+ = 10\,\text{V}$, $V^- = -10\,\text{V}$, $R_1 = 40\,\text{k}\Omega$, and $R_E = 12\,\text{k}\Omega$. Neglect base currents and assume $V_{BE1} = 0.7\,\text{V}$ at 1 mA. Determine I_{REF}, I_O, V_{BE1}, and V_{BE2}.

10.26 Consider the circuit in Figure P10.26. The transistors are matched. Assume that base currents are negligible and that $V_A = \infty$. Using the current-voltage relationships given by Equations (10.26(a)) and (10.26(b)), show that

$$I_O R_{E2} - I_{\text{REF}} R_{E1} = V_T \ln\left(\frac{I_{\text{REF}}}{I_O}\right)$$

If $R_{E1} = R_{E2} \neq 0$ and $V_A \neq \infty$, explain the advantage of this circuit over the basic two-transistor current source in Figure 10.2(b).

***10.27** Consider the circuit in Figure P10.26, with parameters $V^+ = 5\,\text{V}$, $V^- = -5\,\text{V}$, $R_1 = 13.6\,\text{k}\Omega$, and $R_{E1} = R_{E2} = 5\,\text{k}\Omega$. The transistor parameters are: $\beta = 50$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, and $V_A = 75\,\text{V}$. (a) Determine the output resistance $R_0 = dV_{C2}/dI_O$. (b) Compare this output resistance value to that obtained when $R_{E1} = R_{E2} = 0$ and $R_1 = 18.6\,\text{k}\Omega$.

***10.28** Consider the circuit in Figure P10.28. Neglect base currents and assume $V_A = \infty$. (a) Derive the expression for I_O in terms of I_{REF} and R_E. (b) Determine the value of R_E such that $I_O = I_{\text{REF}} = 100\,\mu\text{A}$. Assume $V_{BE} = 0.7\,\text{V}$ at a collector current of 1 mA.

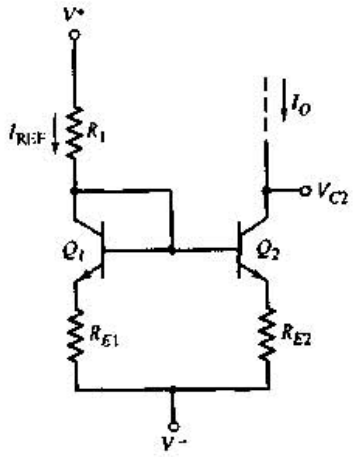


Figure P10.26

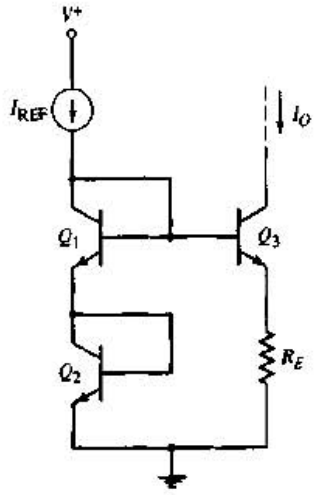


Figure P10.28

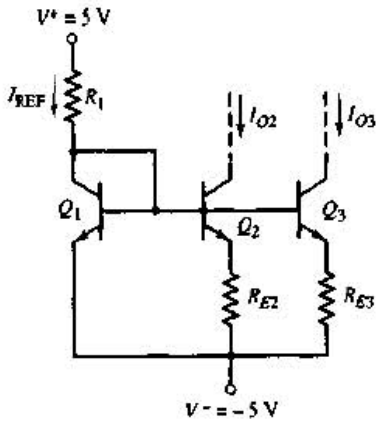


Figure P10.29

D10.29 Consider the Widlar current source with multiple output transistors, as shown in Figure P10.29. Assuming $V_{BE1}(\text{on}) = 0.7\,\text{V}$, design the circuit such that $I_{\text{REF}} = 0.5\,\text{mA}$, $I_{O2} = 10\,\mu\text{A}$, and $I_{O3} = 30\,\mu\text{A}$. What are the values of V_{BE2} and V_{BE3}?

10.30 Assume that all transistors in the circuit in Figure P10.30 are matched and that $\beta = \infty$ (neglect base currents). (a) Derive an expression for I_O in terms of bias voltages and resistor values. (b) Show that if $R_1 = R_2$ and $I_O = I_{\text{REF}}$, then $I_O = (V^+ - V^-)/2R_E$, which means that the currents are independent of V_{BE}. (c) For $V^+ = +5\,\text{V}$ and $V^- = -5\,\text{V}$, design the circuit such that $I_O = 0.5\,\text{mA}$.

10.31 In the circuit in Figure P10.31, the transistor parameters are: $\beta = \infty$, $V_A = \infty$, and $V_{BE} = V_{EB} = 0.7\,\text{V}$ at 1 mA. Let $R_{C1} = 2\,\text{k}\Omega$, $R_{C2} = 3\,\text{k}\Omega$, $R_{C3} = 1\,\text{k}\Omega$, and $R_1 = 12\,\text{k}\Omega$. (a) Determine I_{O1}, I_{O2}, and I_{O3}. (b) Calculate V_{CE1}, V_{EC2}, and V_{EC3}.

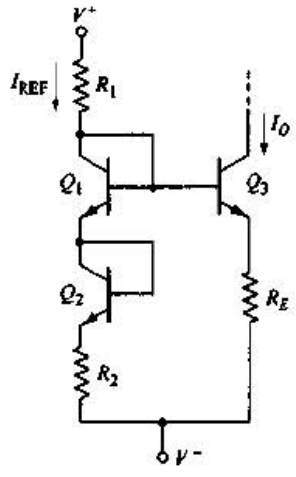


Figure P10.30

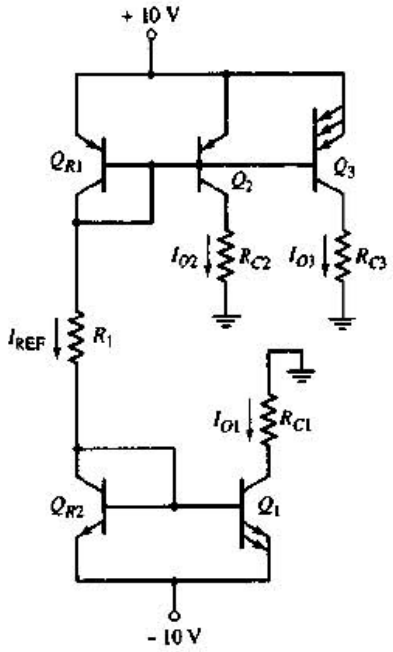


Figure P10.31

10.32 Consider the circuit in Figure P10.31, with transistor parameters: $\beta = \infty$, $V_A = \infty$, and $V_{BE} = V_{EB} = 0.7\,\text{V}$ at 1 mA. Let $R_1 = 8\,\text{k}\Omega$. (a) Find I_{O1}, I_{O2}, and I_{O3}. (b) Determine the maximum values of R_{C1}, R_{C2}, and R_{C3} such that Q_1, Q_2, and Q_3 remain biased in the forward-active region.

***D10.33** Consider the circuit in Figure P10.33. The transistor parameters are: $\beta = \infty$, $V_A = \infty$, and $V_{BE} = 0.7\,\text{V}$ at 1 mA. Design the circuit such that the B–E voltages of Q_1, Q_2, and Q_3 are identical to that of Q_R. What are the values of I_{O1}, I_{O2}, and I_{O3}?

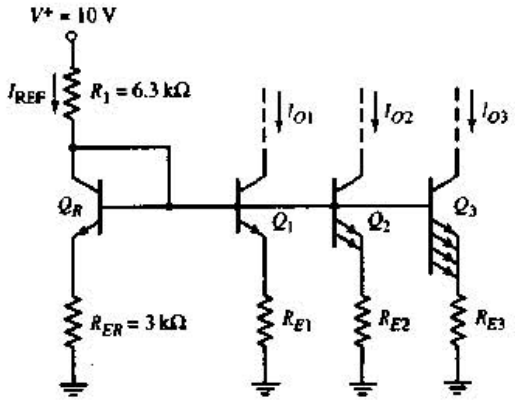


Figure P10.33

Section 10.2 FET Current Sources

10.34 Consider the basic two-transistor NMOS current source in Figure 10.16 with matched transistors. The circuit parameters are: $V^+ = 5\,\text{V}$, $V^- = -5\,\text{V}$, and $I_{REF} = 200\,\mu\text{A}$, and the transistor parameters are: $V_{TN} = 1\,\text{V}$, $K_n = 250\,\mu\text{A/V}^2$, and $\lambda = 0.02\,\text{V}^{-1}$. Find I_O for: (a) $V_{DS2} = 2\,\text{V}$, (b) $V_{DS2} = 4\,\text{V}$, and (c) $V_{DS2} = 6\,\text{V}$.

10.35 In the two-transistor NMOS current source shown in Figure 10.16, the parameters are: $V^+ = 5\,V$, $V^- = -5\,V$, and $I_{REF} = 0.5\,mA$. The transistor parameters are: $V_{TN1} = 1\,V$, $K_{n1} = 0.5\,mA/V^2$, and $\lambda_1 = \lambda_2 = 0$. (a) If $V_{TN2} = 1\,V$ and $K_{n2} = (0.5 \pm 5\%)\,mA/V^2$, determine the range in values of I_O. (b) If $K_{n2} = 0.5\,mA/V^2$ and $V_{TN2} = (1 \pm 5\%)\,V$, determine the range in values of I_O.

10.36 Consider the two-transistor diode-connected circuit in Figure P10.36. Assume that both transistors are biased in the saturation region, and that $g_{m1} = g_{m2} \equiv g_m$ and $r_{o1} = r_{o2} \equiv r_o$. Neglect the body effect. Derive the expression for the output resistance R_o.

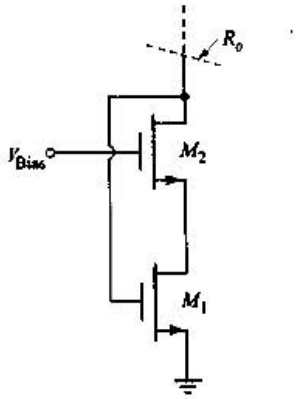


Figure P10.36

10.37 Consider the circuit in Figure 10.22 in the text. Assume $I_{REF} = 50\,\mu A$ and assume transistor parameters of $V_{TN} = 0.8\,V$, $(\frac{1}{2})\mu_n C_{ox} = 48\,\mu A/V^2$, $\lambda = 0$, and $\gamma = 0$. (a) Find W/L such that $V_{DS3}(sat) = 0.2\,V$. (b) What is V_{GS5}? (c) What is the minimum voltage at the drain of M_1 such that all transistors remain biased in the saturation region?

D10.38 For the circuit in Figure 10.17, $V^+ = 5\,V$ and $V^- = -5\,V$, and the transistor parameters are: $V_{TN} = 1.5\,V$, $(\frac{1}{2})\mu_n C_{ox} = 20\,\mu A/V^2$, and $\lambda = 0$. Design the circuit such that $I_O = 0.25\,mA$, $I_{REF} = 0.10\,mA$, and M_2 remains biased in the saturation region for $V_{DS2} \geq 2\,V$.

10.39 The parameters for the circuit in Figure 10.17 are $V^+ = 5\,V$ and $V^- = 0$, and the transistor parameters are: $V_{TN} = 0.5\,V$, $(\frac{1}{2})\mu_n C_{ox} = 18\,\mu A/V^2$, and $\lambda = 0.02\,V^{-1}$. The transistor width-to-length ratios are $(W/L)_3 = 5$, $(W/L)_1 = 25$, and $(W/L)_2 = 15$. Determine: (a) I_{REF}, (b) I_O at $V_{DS2} = 2\,V$, and (c) I_O at $V_{DS2} = 4\,V$.

10.40 The circuit in Figure P10.40 is a PMOS version of a two-transistor MOS current mirror. Assume transistor parameters of $V_{TP} = -0.4\,V$, $(\frac{1}{2})\mu_p C_{ox} = 20\,\mu A/V^2$, and $\lambda = 0$. The transistor width-to-length ratios are $(W/L)_1 = 25$, $(W/L)_2 = 15$, and $(W/L)_3 = 5$. (a) Determine I_O, I_{REF}, V_{SG1}, and V_{SG3}. (b) What is the largest value of R such that M_2 remains biased in the saturation region?

D10.41 The transistors in Figure P10.40 have the same parameters as in Problem 10.40 except for the (W/L) ratios. Design the circuit such that $I_O = 25\,\mu A$, $I_{REF} = 75\,\mu A$, and $V_{SD2}(sat) = 0.25\,V$.

***10.42** For the NMOS cascode current source in Figure 10.19, the parameters are $V^+ = 10\,V$, $V^- = -10\,V$, and $I_{REF} = 100\,\mu A$. All transistors are matched, with parameters $V_{TN} = 2\,V$, $K_n = 100\,\mu A/V^2$, and $\lambda = 0.02\,V^{-1}$. (a) Determine I_O for $V_{D4} = -3\,V$. (b) Determine the change in I_O as V_{D4} changes from $-3\,V$ to $+3\,V$.

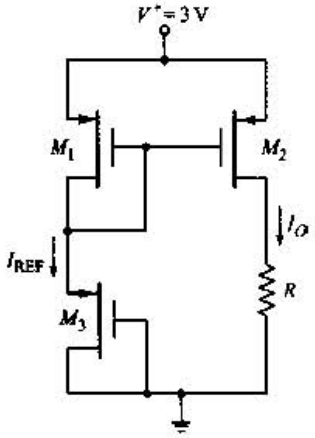


Figure P10.40

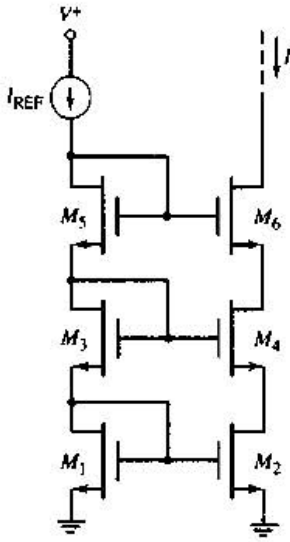


Figure P10.43

***10.43** Consider the NMOS current source in Figure P10.43. Let $I_{REF} = 0.2\,\text{mA}$, $K_n = 0.2\,\text{mA/V}^2$, $V_{TN} = 1\,\text{V}$, and $\lambda = 0.02\,\text{V}^{-1}$. (All transistors are matched.) Determine the output resistance looking into the drain of M_6.

10.44 The transistors in the circuit in Figure P10.44 have parameters $V_{TN} = +0.5\,\text{V}$, $V_{TP} = -0.5\,\text{V}$, $(\frac{1}{2})\mu_n C_{ox} = 50\,\mu\text{A/V}^2$, $(\frac{1}{2})\mu_p C_{ox} = 20\,\mu\text{A/V}^2$, and $\lambda_n = \lambda_p = 0$. The transistor width-to-length ratios are $(W/L)_1 = (W/L)_2 = 20$, $(W/L)_3 = 5$, and $(W/L)_4 = 10$. Determine I_O, I_{REF}, and $V_{DS2}(\text{sat})$.

***D10.45** The transistors in the circuit in Figure P10.44 have the same parameters as in Problem 10.44 except for the (W/L) ratios. Design the circuit such that $I_O = 50\,\mu\text{A}$, $I_{REF} = 150\,\mu\text{A}$, $V_{DS2}(\text{sat}) = 0.5\,\text{V}$, and $V_{GS3} = V_{SG4}$.

***10.46** A Wilson current mirror is shown in Figure 10.21(a). The parameters are: $V^+ = 5\,\text{V}$, $V^- = -5\,\text{V}$, and $I_{REF} = 80\,\mu\text{A}$. The transistor parameters are: $V_{TN} = 1\,\text{V}$, $K_n = 80\,\mu\text{A/V}^2$, and $\lambda = 0.02\,\text{V}^{-1}$. Determine I_O at: (a) $V_{D3} = -1\,\text{V}$, and (b) $V_{D3} = +3\,\text{V}$.

***10.47** Repeat Problem 10.46 for the modified Wilson current mirror in Figure 10.21(b).

10.48 Consider the bias-independent current source in Figure 10.23. Assume transistor parameters of $V_{TN} = +0.5\,\text{V}$, $V_{TP} = -0.5\,\text{V}$, $(\frac{1}{2})\mu_n C_{ox} = 50\,\mu\text{A/V}^2$, $(\frac{1}{2})\mu_p C_{ox} = 20\,\mu\text{A/V}^2$, and $\lambda_n = \lambda_p = 0$. The W/L ratios are given for the M_1–M_4 transistors. (a) Determine R such that $I_{D1} = I_{D2} = 50\,\mu\text{A}$. (b) What is the minimum bias voltage difference $(V^+ - V^-)$ that must be applied? (c) Determine $(W/L)_5$ and $(W/L)_6$ such that $I_{O1} = 25\,\mu\text{A}$ and $I_{O2} = 75\,\mu\text{A}$.

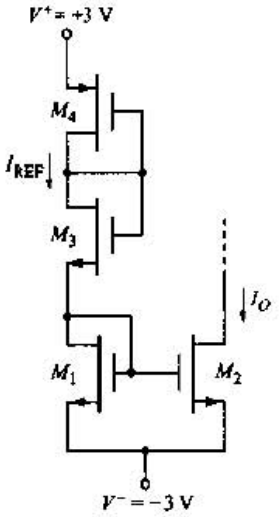


Figure P10.44

D10.49 Consider the multitransistor current source in Figure P10.49. The transistor parameters are: $V_{TN} = 1\,\text{V}$, $(\frac{1}{2})\mu_n C_{ox} = 20\,\mu\text{A/V}^2$, and $\lambda = 0$. Assume M_3, M_4, and M_5 are identical. Design the circuit such that $I_{REF} = 0.1\,\text{mA}$, $I_{O1} = 0.2\,\text{mA}$, and $I_{O2} = 0.3\,\text{mA}$.

10.50 The parameters of the transistors in the circuit in Figure P10.50 are $V_{TN} = 1.2\,\text{V}$, $V_{TP} = -1.2\,\text{V}$, $(\frac{1}{2})\mu_n C_{ox} = 40\,\mu\text{A/V}^2$, $(\frac{1}{2})\mu_p C_{ox} = 18\,\mu\text{A/V}^2$, and $\lambda_n = \lambda_p = 0$. The W/L ratios are given in the figure. For $R = 200\,\text{k}\Omega$, determine I_{REF}, I_1, I_2, I_3, and I_4.

10.51 Repeat Problem 10.50 if the bias voltages are reduced to $V^+ = 5\,\text{V}$ and $V^- = -5\,\text{V}$.

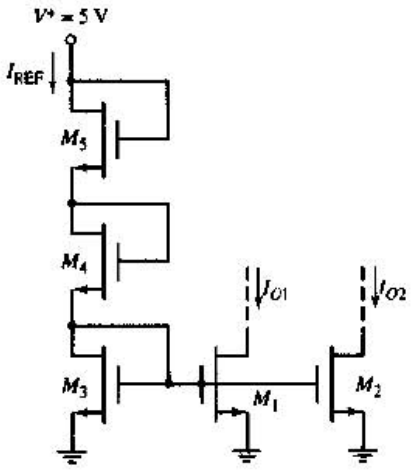


Figure P10.49

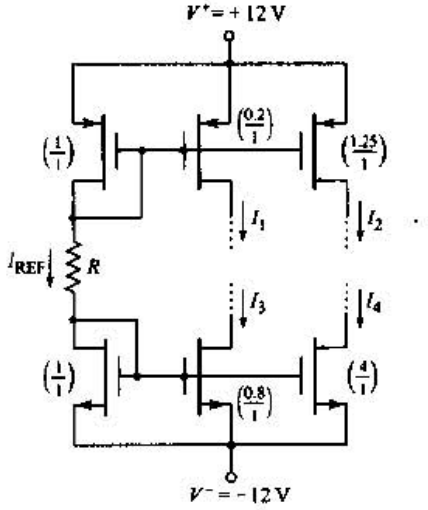


Figure P10.50

10.52 For the JFET in Figure P10.52, the parameters are: $I_{DSS} = 2\,\text{mA}$, $V_P = -2\,\text{V}$, and $\lambda = 0.05\,\text{V}^{-1}$. Determine I_O for: (a) $V_D = -5\,\text{V}$, (b) $V_D = 0\,\text{V}$, and (c) $V_D = +5\,\text{V}$.

***10.53** A JFET cascode current source is shown in Figure P10.53. The transistor parameters are: $I_{DSS} = 1\,\text{mA}$, $V_P = -2\,\text{V}$, and $\lambda = 0.05\,\text{V}^{-1}$. Determine I_O, V_{DS1}, and V_{DS2} at: (a) $V_D = -5\,\text{V}$, (b) $V_D = 0\,\text{V}$, and (c) $V_D = +5\,\text{V}$.

D10.54 A JFET circuit is biased with the current source in Figure P10.54. The transistor parameters are: $I_{DSS} = 4\,\text{mA}$, $V_P = -4\,\text{V}$, and $\lambda = 0$. Design the circuit such that $I_O = 2\,\text{mA}$. What is the minimum value of V_D such that the transistor is biased in the saturation region?

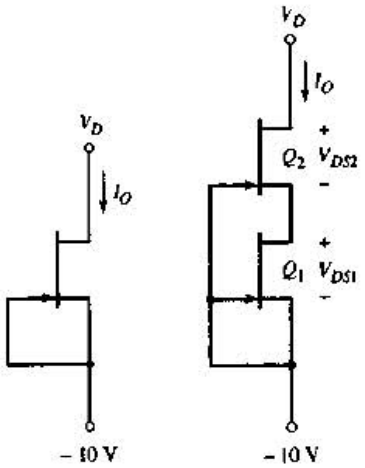


Figure P10.52

Figure P10.53

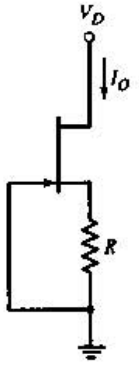


Figure P10.54

Section 10.3 Active Load Circuits

10.55 Consider the simple BJT active load amplifier in Figure 10.29, with transistor parameters: $I_{SO} = 10^{-12}\,\text{A}$, $I_{S1} = I_{S2} = 5 \times 10^{-13}\,\text{A}$, $V_{AN} = 120\,\text{V}$, and $V_{AP} = 80\,\text{V}$. Let $V^+ = 5\,\text{V}$, and neglect base currents. (a) Find the value of V_{EB} that will produce

$I_{REF} = 1\,mA$. (b) Determine the value of R_1. (c) What value of V_I will produce $V_{CEO} = V_{EC2}$? (d) Determine the open-circuit small-signal voltage gain

10.56 The amplifier shown in Figure P10.56 uses a pnp driver and an npn active load circuit. The transistor parameters are: $I_{S0} = 5 \times 10^{-13}\,A$, $I_{S1} = I_{S2} = 10^{-12}\,A$, $V_{AN} = 120\,V$, and $V_{AP} = 80\,V$. Let $V^+ = 5\,V$, and neglect base currents. (a) Find the value of V_{BE} that will produce $I_{REF} = 0.5\,mA$. (b) Determine the value of R_1. (c) What value of V_I will produce $V_{EC0} = V_{CE2}$? (d) Determine the open-circuit small-signal voltage gain.

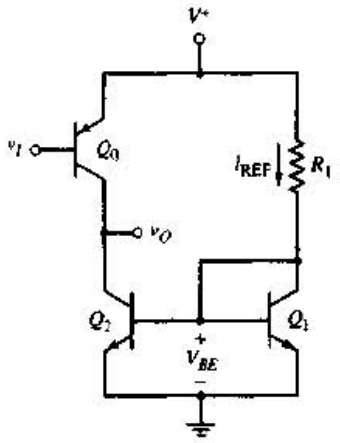


Figure P10.56

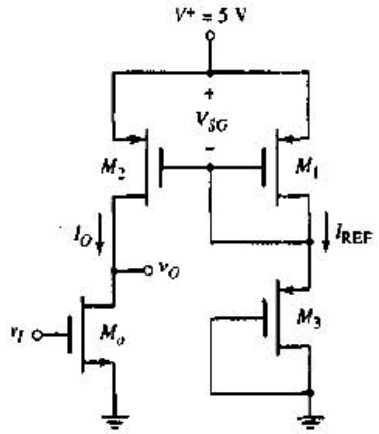


Figure P10.57

D10.57 Consider the basic MOSFET amplifier with active load in Figure P10.57. The transistor parameters are: $V_{TN} = 1\,V$, $V_{TP} = -1\,V$, $(\frac{1}{2})\mu_n C_{ox} = 20\,\mu A/V^2$, $(\frac{1}{2})\mu_p C_{ox} = 10\,\mu A/V^2$, and $\lambda_n = \lambda_p = 0.02\,V^{-1}$. (a) Design the circuit such that $I_{REF} = I_O = 0.1\,mA$. Assume M_1 and M_2 are matched, $(W/L)_3 = 5$, and the quiescent input voltage is $V_{IQ} = 2\,V$. The quiescent output voltage is to be $V_{OQ} = 2.5\,V$. (b) Determine the open-circuit small-signal voltage gain.

10.58 For the simple MOSFET amplifier with active load shown in Figure 10.33, the transistor parameters are: $V_{TN} = 1\,V$, $V_{TP1} = V_{TP2} = -1\,V$, $K_{p1} = K_{p2} = K_n = 100\,\mu A/V^2$, and $\lambda_1 = \lambda_2 = \lambda_n = 0.02\,V^{-1}$. Let $V^+ = 10\,V$ and $I_{REF} = 100\,\mu A$. (a) Find V_{SG}. (b) What value of V_I will produce $V_{DS0} = V_{SD2}$? (c) Determine the open-circuit small-signal voltage gain.

Section 10.4 Small-Signal Analysis: Active Load Circuits

10.59 A BJT amplifier with active load is shown in Figure P10.59. The circuit contains emitter resistors R_E and a load resistor R_L. (a) Derive the expression for the output resistance looking into the collector of Q_2. (b) Using the small-signal equivalent circuit, derive the equation for the small-signal voltage gain. Express the relationship in a form similar to Equation (10.94).

10.60 In the circuit in Figure P10.60, the active load circuit is replaced by a Wilson current source. Assume that $\beta = 80$ for all transistors, and that $V_{AN} = 120\,V$, $V_{AP} = 80\,V$, and $I_{REF} = 0.2\,mA$. Determine the open-circuit small-signal voltage gain.

10.61 For the circuit in Figure 10.39(a) the transistor parameters are: $K_p = 0.2\,mA/V^2$, $K_n = 0.25\,mA/V^2$, $V_{TN} = 1\,V$, $V_{TP} = -1\,V$, $\lambda_n = 0.02\,V^{-1}$, and $\lambda_p =$

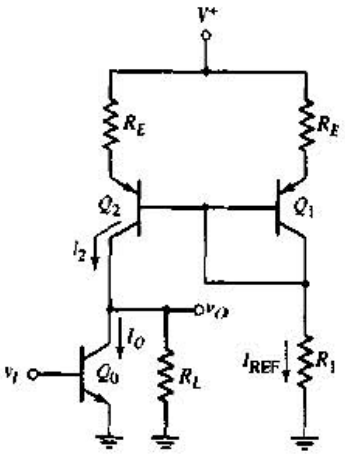


Figure P10.59

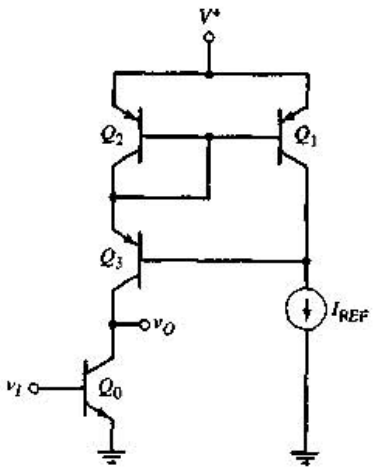


Figure P10.60

$0.03\,V^{-1}$. Let $V^+ = 10\,V$ and $I_{REF} = 0.2\,mA$. (a) Determine the small-signal parameters $g_m(M_0)$, r_{on}, and r_{op}. (b) Determine the open-circuit small-signal voltage gain. (c) Determine the value of R_L that results in a voltage gain of one-half the open-circuit value.

10.62 The parameters of the transistors in Figure P10.62 are $V_{TN} = +0.8\,V$, $V_{TP} = -0.8\,V$, $(\frac{1}{2})\mu_n C_{ox} = 50\,\mu A/V^2$, $(\frac{1}{2})\mu_p C_{ox} = 20\,\mu A/V^2$, and $\lambda_n = \lambda_p = 0.02\,V^{-1}$. The width-to-length ratios are shown in the figure. The value of V_{GSQ} is such that $I_{D1} = 100\,\mu A$, and M_1 and M_2 are biased in the saturation region. Find the small-signal voltage gain $A_v = v_o/v_i$.

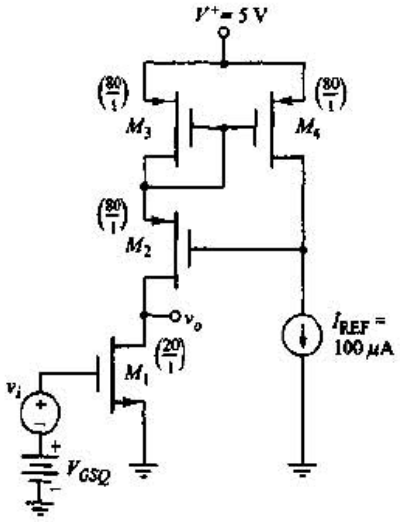


Figure P10.62

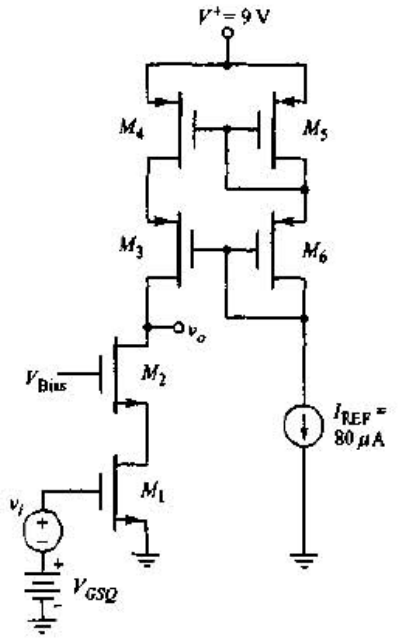


Figure P10.63

10.63 The parameters of the transistors in Figure P10.63 are $V_{TN} = +0.8\,V$, $V_{TP} = -0.8\,V$, $(\frac{1}{2})\mu_n C_{ox} = 50\,\mu A/V^2$, $(\frac{1}{2})\mu_p C_{ox} = 20\,\mu A/V^2$, and $\lambda_n = \lambda_p = 0.02\,V^{-1}$. The width-to-length ratios of M_1 and M_2 are 20, and those of M_3–M_6 are 40. The value

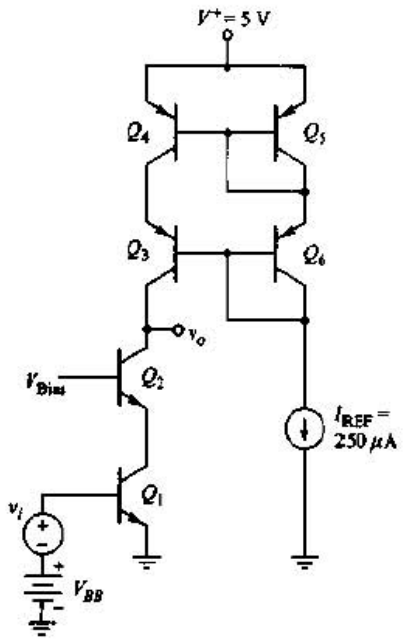


Figure P10.64

of V_{GSQ} is such that $I_{D1} = 80\,\mu A$, and all transistors are biased in the saturation region. Determine the small-signal voltage gain $A_v = v_o/v_i$.

10.64 A BJT cascode amplifier with a cascode active load is shown in Figure P10.64. Assume transistor parameters of $\beta = 120$ and $V_A = 80$ V. The V_{BB} voltage is such that all transistors are biased in the active region. Determine the small-signal voltage gain $A_v = v_o/v_i$.

D10.65 Design a bipolar cascode amplifier with a cascode active load similar to that in Figure P10.64 except the amplifying transistors are to be pnp and the load transistors are to be npn. Bias the circuit at $V^+ = 10$ V and incorporate a reference current of $I_{REF} = 200\,\mu A$. If all transistors are matched with $\beta = 100$ and $V_A = 60$ V, determine the small-signal voltage gain.

D10.66 Design a MOSFET cascode amplifier with a cascode active load similar to that shown in Figure P10.63 except that the amplifying transistors are to be PMOS and the load transistors are to be NMOS. Assume transistor parameters similar to those in Problem 10.63. Determine the small-signal voltage gain.

COMPUTER SIMULATION PROBLEMS

10.67 Consider the Widlar current source in Figure 10.9, with parameters given in Problem 10.25. Choose appropriate transistor parameters. Connect a 40 kΩ resistor between V^+ and the collector of Q_2 as a load. Using a PSpice analysis, determine I_{REF}, I_O, V_{BE1}, and V_{BE2}.

10.68 For the circuit in Figure 10.19, the transistor and circuit parameters are given in Problem 10.42. Connect a separate dc voltage source at the drain of M_4. Change the value of the voltage source such that V_{D4} varies between −3 V and +3 V. From a computer analysis, determine the change in I_O as V_{D4} varies between the two limits.

10.69 In the circuit in Figure P10.59, the parameters are: $V^+ = 10\,V$, $R_1 = 9\,k\Omega$, and $R_E = 4\,k\Omega$. The transistor parameters are: $\beta = 100$ and $V_{AN} = V_{AP} = 100\,V$. (a) Using a computer simulation, plot the voltage transfer characteristics of v_O versus v_I, similar to those in Figure 10.30, for $R_L = \infty$. What is the voltage gain? (b) Repeat part (a) if $R_L = 100\,k\Omega$.

10.70 Consider the circuit in Figure P10.60, with parameters $V^+ = 5\,V$ and $I_{REF} = 0.5\,mA$. Assume all transistors are identical, with parameters $\beta = 100$ and $V_A = 100\,V$. Using a computer analysis, plot the voltage transfer characteristics v_O versus v_I over an appropriate voltage range, and determine the voltage gain.

10.71 A MOSFET active load circuit is shown in Figure P10.57. The circuit and transistor parameters are as described in Problem 10.57. In addition, assume width-to-length ratios of $(W/L)_1 = (W/L)_2 = 5$ and $(W/L)_O = 15$. Using a computer simulation, plot the voltage transfer characteristics of v_O versus v_I, similar to those shown in Figure 10.34. What is the voltage gain?

DESIGN PROBLEMS

[Note: Each design should be verified with a computer analysis.]

***D10.72** Design a generalized Widlar current source (Figure P10.26) to provide a bias current $I_O = 200\,\mu A$. Assume the output impedance is $R_o = 5\,M\Omega$, and the circuit is biased at $V^+ = 9\,V$ and $V^- = -9\,V$. The transistor parameters are: $I_S = 10^{-14}\,A$ and $V_A = 120\,V$.

***D10.73** Consider a MOSFET current source similar to the one shown in Figure 10.17, biased at $V^+ = 10\,V$ and $V^- = -10\,V$. The transistor parameters are: $(\frac{1}{2})\mu_n C_{ox} = 20\,\mu A/V^2$, $V_{TN} = 2\,V$, and $\lambda = 0$. Design the circuit such that $I_O = 150\,\mu A$ and $V_{DS}(sat) = 0.25\,V$ for M_2.

***D10.74** Using MOSFETs, design a circuit similar to that shown in Figure 10.15, to provide $I_{O1} = 100\,\mu A$, $I_{O2} = 150\,\mu A$, $I_{O3} = 200\,\mu A$, and $I_{O4} = 250\,\mu A$. Assume the transistor parameters are: $(\frac{1}{2})\mu_n C_{ox} = 20\,\mu A/V^2$, $(\frac{1}{2})\mu_p C_{ox} = 10\,\mu A/V^2$, $V_{TN} = |V_{TP}| = 2\,V$, and $\lambda = 0$. Let $V^+ = 10\,V$ and $V^- = -10\,V$.

CHAPTER

11

Differential and Multistage Amplifiers

11.0 PREVIEW

In this chapter, we introduce a special multitransistor circuit configuration called the differential amplifier, or diff-amp. We have encountered a diff-amp previously in our discussion of op-amp circuits. However, the diff-amp, in the context of this chapter, is at the basic transistor level.

The diff-amp is a fundamental building block of analog circuits. It is the input stage of virtually every op-amp, and is the basis of a high-speed digital logic circuit family, called emitter-coupled logic, which will be addressed in Chapter 17.

Matched or identical transistor characteristics are critical to the design of the IC diff-amp, as they were in the design of current-source circuits. The design of electronic circuits in this chapter, then, is based on integrated circuit fabrication. The design of IC diff-amps, in general, incorporates current-source biasing and active loads that were analyzed in the last chapter. We consider both BJT and MOSFET differential amplifier designs. At the end of this chapter, the reader should be able to design both BJT and MOSFET diff-amps to meet particular specifications.

Basic BiCMOS analog circuits are considered. BiCMOS circuits combine bipolar and MOS transistors on the same semiconductor chip. The advantages of the MOSFET high input impedance and the bipolar high gain can be utilized in the same circuit.

Up to this point, we have concentrated primarily on the analysis and design of single-stage amplifiers. However, these circuits have limited gain, input resistance, and output resistance. Multistage or cascaded-stage amplifiers can be designed to produce high gain and specified input and output resistance values. In this chapter, we begin to consider these multistage amplifiers.

11.1 THE DIFFERENTIAL AMPLIFIER

In Chapter 4, we discussed the reasons linear amplifiers are necessary in analog electronic systems. In Chapters 4 and 6, we analyzed and designed several configurations of bipolar and MOS transistor amplifiers. In these circuits, there was one input terminal and one output terminal.

In this chapter, we introduce another basic transistor circuit configuration called the differential amplifier. This amplifier, also called a diff-amp, is the

input stage to virtually all op-amps and is probably the most widely used amplifier building block in analog integrated circuits. Figure 11.1 is a block diagram of the diff-amp. There are two input terminals and one output terminal. Ideally, the output signal is proportional to only the difference between the two input signals.

11.2 BASIC BJT DIFFERENTIAL PAIR

In this section, we consider the basic bipolar **difference amplifier** or **diff-amp**. We introduce the terminology, qualitatively describe the operation of the circuit, and analyze the dc and small-signal characteristics of the diff-amp.

11.2.1 Terminology and Qualitative Description

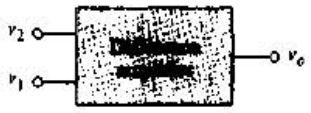


Figure 11.1 Difference amplifier block diagram

As mentioned, Figure 11.1 is a block diagram of a difference amplifier. Ideally, the output is proportional only to the difference between the two input signals, or

$$v_o = A_d(v_1 - v_2) \tag{11.1}$$

In the ideal case, if $v_1 = v_2$, the output voltage is zero. We only obtain a nonzero output voltage if v_1 and v_2 are not equal.

We define the **differential-mode input voltage** as

$$v_d = v_1 - v_2 \tag{11.2}$$

and the **common-mode input voltage** as

$$v_{cm} = \frac{v_1 + v_2}{2} \tag{11.3}$$

These equations show that if $v_1 = v_2$, the differential-mode input signal is zero and the common-mode input signal is $v_{cm} = v_1 = v_2$.

If, for example, $v_1 = +10\,\mu V$ and $v_2 = -10\,\mu V$, then the differential-mode voltage is $v_d = 20\,\mu V$ and the common-mode voltage is $v_{cm} = 0$. However, if $v_1 = 110\,\mu V$ and $v_2 = 90\,\mu V$, then the differential-mode input signal is still $v_d = 20\,\mu V$, but the common-mode input signal is $v_{cm} = 100\,\mu V$. If each pair of input voltages were applied to the ideal difference amplifier, the output voltage in each case would be exactly the same. However, amplifiers are not ideal, and the common-mode input signal does affect the output. One goal of the design of differential amplifiers is to minimize the effect of the common-mode input signal.

Figure 11.2 shows the basic BJT differential-pair configuration. Two identical transistors, Q_1 and Q_2, whose emitters are connected together, are biased by a constant-current source I_Q, which is connected to a negative supply voltage V^-. The collectors of Q_1 and Q_2 are connected through resistors R_C to a positive supply voltage V^+. By design, transistors Q_1 and Q_2 are to remain biased in the forward-active region. We assume that the two collector resistors R_C are equal, and that v_{B1} and v_{B2} are ideal sources, meaning that the output resistances of these sources are negligibly small.

Since both positive and negative bias voltages are used in the circuit, the need for coupling capacitors and voltage divider biasing resistors at the inputs of Q_1 and Q_2 has been eliminated. If the input signal voltages v_{B1} and v_{B2} in the

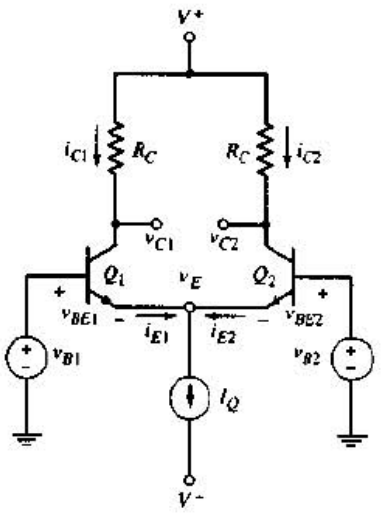


Figure 11.2 Basic BJT differential-pair configuration

circuit shown in Figure 11.2 are both zero, Q_1 and Q_2 are still biased in the active region by the current source I_Q. The common-emitter voltage v_E would be on the order of -0.7 V. This circuit, then, is referred to as a dc-coupled differential amplifier, so differences in dc input voltages can be amplified. Although the diff-amp contains two transistors, it is considered a single-stage amplifier. The analysis will show that it has characteristics similar to those of the common-emitter amplifier.

First, we consider the circuit in which the two base terminals are connected together and a common-mode voltage v_{cm} is applied as shown in Figure 11.3(a). The transistors are biased "on" by the constant-current source, and

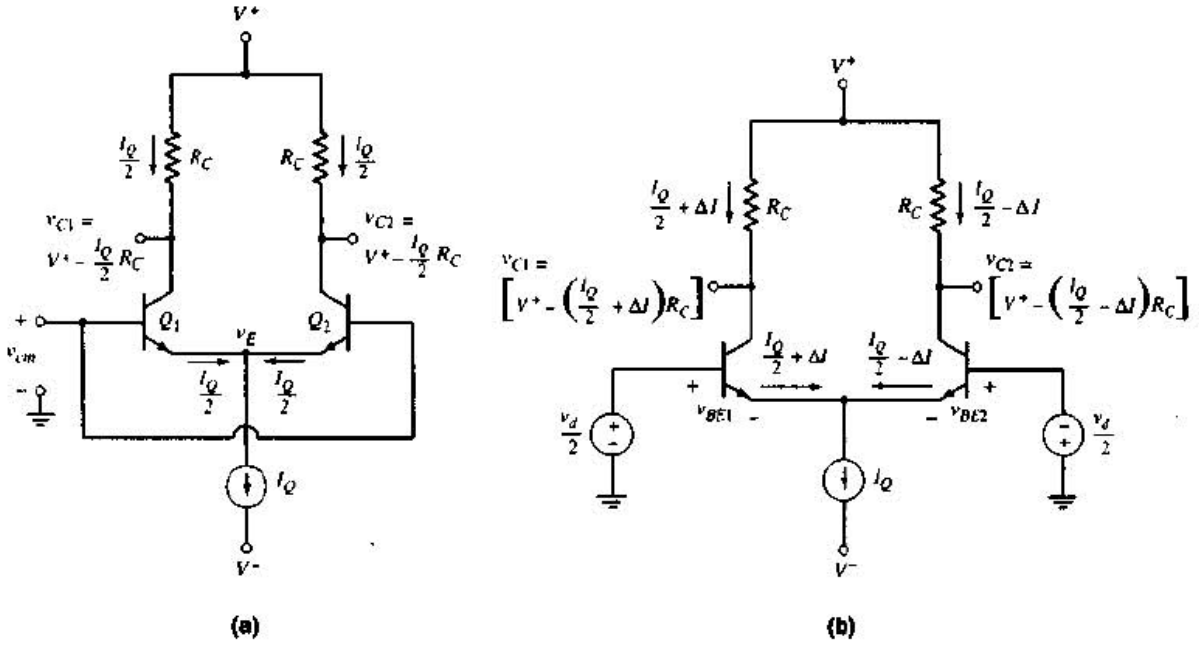


Figure 11.3 Basic diff-amp with applied common-mode voltage and (b) basic diff-amp with applied differential-mode voltage

the voltage at the common emitters is $v_E = v_{cm} - V_{BE}(\text{on})$. Since Q_1 and Q_2 are matched or identical, current I_Q splits evenly between the two transistors, and

$$i_{E1} = i_{E2} = \frac{I_Q}{2} \tag{11.4}$$

If base currents are negligible, then $i_{C1} \cong i_{E1}$ and $I_{C2} \cong i_{E2}$, and

$$v_{C1} = V^+ - \frac{I_Q}{2} R_C = v_{C2} \tag{11.5}$$

We see from Equation (11.5) that, for an applied common-mode voltage, I_Q splits evenly between Q_1 and Q_2 and the difference between v_{C1} and v_{C2} is zero.

Now, if v_{B1} increases by a few millivolts and v_{B2} decreases by the same amount, or $v_{B1} = v_d/2$ and $v_{B2} = -v_d/2$, the voltages at the bases of Q_1 and Q_2 are no longer equal. Since the emitters are common, this means that the B–E voltages on Q_1 and Q_2 are no longer equal. Since v_{B1} increases and v_{B2} decreases, then $v_{BE1} > v_{BE2}$, which means that i_{C1} increases by ΔI above its quiescent value and i_{C2} decreases by ΔI below its quiescent value. This is shown in Figure 11.3(b). A potential difference now exits between the two collector terminals. We can write

$$v_{C2} - v_{C1} = \left[V^+ - \left(\frac{I_{CQ}}{2} - \Delta I\right) R_C\right] - \left[V^+ - \left(\frac{I_{CQ}}{2} + \Delta I\right) R_C\right] = 2\Delta I R_C \tag{11.6}$$

A voltage difference is created between v_{C2} and v_{C1} when a differential-mode input voltage is applied.

Example 11.1 **Objective:** Determine the quiescent collector current and collector-emitter voltage in a difference amplifier.

Consider the diff-amp in Figure 11.2, with circuit parameters: $V^+ = 10\,\text{V}$, $V^- = -10\,\text{V}$, $I_Q = 1\,\text{mA}$, and $R_C = 10\,\text{k}\Omega$. The transistor parameters are: $\beta = \infty$ (neglect base currents), $V_A = \infty$, and $V_{BE}(\text{on}) = 0.7\,\text{V}$. Determine i_{C1} and v_{CE1} for common-mode voltages $v_{B1} = v_{B2} = v_{CM} = 0$, $-5\,\text{V}$, and $+5\,\text{V}$.

Solution: We know that

$$i_{C1} = i_{C2} = \frac{I_Q}{2} = 0.5\,\text{mA}$$

therefore,

$$v_{C1} = v_{C2} = V^+ - i_{C1} R_C = 10 - (0.5)(10) = 5\,V$$

From $v_{CM} = 0$, $v_E = -0.7\,\text{V}$ and

$$v_{CE1} = v_{C1} - v_E = 5 - (-0.7) = 5.7\,\text{V}$$

For $v_{CM} = -5\,\text{V}$, $v_E = -5.7\,\text{V}$ and

$$v_{CE1} = v_{C1} - v_E = 5 - (-5.7) = 10.7\,\text{V}$$

For $v_{CM} = +5\,\text{V}$, $v_E = 4.3\,\text{V}$ and

$$v_{CE1} = v_{C1} - v_E = 5 - 4.3 = 0.7\,\text{V}$$

Comment As the common-mode voltage varies, the ideal constant current I_Q still splits evenly between Q_1 and Q_2, but the collector–emitter voltage varies, which means that the Q-point changes. In this example, if v_{CM} were to increase above +5 V, then Q_1 and Q_2 would be driven into saturation. This demonstrates that there is a limited range of applied common-mode voltage over which Q_1 and Q_2 will remain biased in the forward-active mode.

Test Your Understanding

11.1 Input voltages $v_1 = 2 + 0.005 \sin \omega t$ V and $v_2 = 0.5 - 0.005 \sin \omega t$ V are applied to a differential amplifier. Find the differential- and common-mode components of the input signal. (Ans. $V_d = 1.5 + 0.010 \sin \omega t$ V, $V_{cm} = 1.25$ V)

11.2 For the differential amplifier in Figure 11.2, the parameters are: $V^+ = 10$ V, $V^- = -10$ V, $I_Q = 1$ mA, and $R_C = 10\,\text{k}\Omega$. The transistor parameters are: $\beta = 200$, $V_{BE}(\text{on}) = 0.7$ V, and $V_A = \infty$. Find the voltages v_E, v_{C1}, and v_{C2}, for $v_1 = v_2 = 0$. (Ans. $v_E = -0.7$ V, $v_{C1} = v_{C2} = 5$ V)

RD11.3 Consider the diff-amp in Figure 11.2, with parameters: $V^+ = 10$ V, $V^- = -10$ V, and $I_Q = 2$ mA. Redesign the circuit such that the common-mode input voltage is in the range $-4 \le v_{cm} \le +4$ V, while Q_1 and Q_2 remain biased in the forward-active region. (Ans. $R_C = 6\,\text{k}\Omega$)

11.2.2 DC Transfer Characteristics

We can perform a general analysis of the differential-pair configuration by using the exponential relationship between collector current and B–E voltage. To begin, we know that

$$i_{C1} = I_S e^{v_{BE1}/V_T} \tag{11.7(a)}$$

and

$$i_{C2} = I_S e^{v_{BE2}/V_T} \tag{11.7(b)}$$

We assume Q_1 and Q_2 are matched and are operating at the same temperature, so the coefficient I_S is the same in each expression.

Neglecting base currents and assuming I_Q is an ideal constant-current source, we have

$$I_Q = i_{C1} + I_{C2} \tag{11.8}$$

where i_{C1} and i_{C2} are the total instantaneous currents, which may include the signal currents. We then have

$$I_Q = I_S\left[e^{v_{BE1}/V_T} + e^{v_{BE2}/V_T}\right] \tag{11.9}$$

Taking the ratios of i_{C1} to I_Q and i_{C2} to I_Q, we obtain

$$\frac{i_{C1}}{I_Q} = \frac{1}{1 + e^{(v_{BE2} - v_{BE1})/V_T}} \tag{11.10(a)}$$

and

$$\frac{i_{C2}}{I_Q} = \frac{1}{1 + e^{-(v_{BE2} - v_{BE1})/V_T}} \tag{11.10(b)}$$

From Figure 11.3(b) we see that

$$v_{BE1} - v_{BE2} \cong v_d \tag{11.11}$$

where v_d is the differential-mode input voltage. Equations (11.10(a)) and (11.10(b)) can then be written in terms of v_d, as follows:

$$i_{C1} = \frac{I_Q}{1 + e^{-v_d/V_T}} \tag{11.12(a)}$$

and

$$i_{C2} = \frac{I_Q}{1 + e^{+v_d/V_T}} \tag{11.12(b)}$$

Equations (11.12(a)) and (11.12(b)) describe the basic current–voltage characteristics of the differential amplifier. If the differential-mode input voltage is zero, then the current I_Q splits evenly between i_{C1} and I_{C2}, as we discussed. However, when a differential-mode signal v_d is applied, a difference occurs between i_{C1} and i_{C2} which in turn causes a change in the collector terminal voltage. This is the fundamental operation of the diff-amp. If a common-mode signal $v_{CM} = v_{B1} = v_{B2}$ is applied, the bias current I_Q still splits evenly between the two transistors.

Figure 11.4 is the normalized plot of the **dc transfer characteristics** for the differential amplifier. We can make two basic observations. First, the gain of the differential amplifier is proportional to the slopes of the transfer curves about the point $v_d = 0$. In order to maintain a linear amplifier, the excursion of v_d about zero must be kept small.

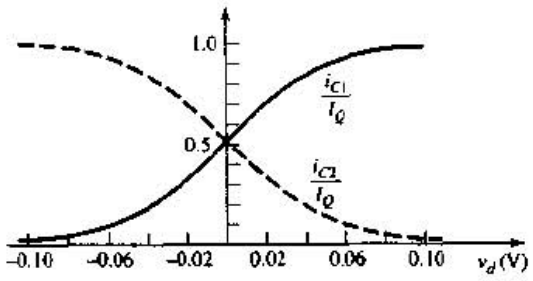


Figure 11.4 Normalized dc transfer characteristics for BJT differential amplifier

Second, as the magnitude of v_d becomes sufficiently large, essentially all of current I_Q goes to one transistor, and the second transistor effectively turns off. This particular characteristic is used in the emitter-coupled logic (ECL) family of digital logic circuits, which is discussed in Chapter 17.

Example 11.2 **Objective:** Determine the maximum differential-mode input signal that can be applied and still maintain linearity in the differential amplifier.

Figure 11.5 shows an expanded view of the normalized i_{C1} versus v_d characteristic. A linear approximation that corresponds to the slope at $v_d = 0$ is superimposed on the curve. Determine $v_d(\max)$ such that the difference between the linear approximation and the actual curve is 1 percent.

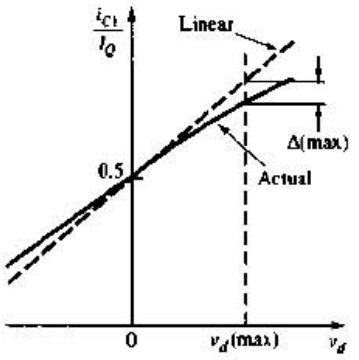


Figure 11.5 Expanded view, normalized i_{C1} versus v_d transfer characteristic

Solution: The actual expression for i_{C1} versus v_d is, from Equation (11.12(a)),

$$i_{C1}(\text{actual}) = \frac{I_Q}{1 + e^{-v_d/V_T}}$$

The slope at $v_d = 0$ is found to be

$$g_f = \left.\frac{di_{C1}}{dv_d}\right|_{v_d=0} = I_Q(-1)\left[1 + e^{-v_d/V_T}\right]^{-2}\left(\frac{-1}{V_T}\right)\left[e^{-v_d/V_T}\right]\Big|_{v_d=0}$$

or

$$g_f = \frac{I_Q}{4V_T} \tag{11.13}$$

where g_f is the **forward transconductance**. The linear approximation for i_{C1} versus v_d can be written

$$i_{C1}(\text{linear}) = 0.5I_Q + g_f v_d = 0.5I_Q + \left(\frac{I_Q}{4V_T}\right)v_d \tag{11.14}$$

The differential-mode input voltage $v_d(\max)$ that results in a 1 percent difference between the ideal linear curve and the actual curve is found from

$$\frac{i_{C1}(\text{linear}) - i_{C1}(\text{actual})}{i_{C1}(\text{linear})} = 0.01$$

or

$$\frac{\left[0.5I_Q + \left(\frac{I_Q}{4V_T}\right)v_d(\max)\right] - \frac{I_Q}{1 + e^{-v_d(\max)/V_T}}}{\left[0.5I_Q + \left(\frac{I_Q}{4V_T}\right)v_d(\max)\right]} = 0.01$$

If we rearrange terms, this expression becomes

$$0.99\left[0.5 + \left(\frac{1}{4V_T}\right)v_d(\max)\right] = \frac{1}{1 + e^{-v_d(\max)/V_T}}$$

Assuming $V_T = 26\,\text{mV}$, and using trial and error, we find that

$$v_d(\text{max}) \cong 18\,\text{mV}$$

Comment: The differential-mode input voltage must be held to within $\pm 18\,\text{mV}$ in order for the output signal of this diff-amp to be within 1 percent of a linear response.

Test Your Understanding

11.4 Considering the dc transfer characteristics in Figure 11.4, determine the value of the differential-mode input signal such that $i_{C2} = 0.99I_Q$. (Ans. $v_d = -119.5\,\text{mV} \cong -120\,\text{mV}$)

11.5 Plot the dc transfer characteristics in Figure 11.4 using a computer simulation.

We can now begin to consider the operation of the diff-amp in terms of the small-signal parameters. Figure 11.6 shows the differential-pair configuration with an applied differential-mode input signal. Note that the polarity of the input voltage at Q_1 is opposite to that at Q_2. The forward-transconductance g_f can be written in terms of the individual transistor transconductances g_m. From Equation (11.13), we have

$$g_f = \frac{I_Q}{4V_T} = \frac{1}{2}\frac{I_Q/2}{V_T} = \frac{1}{2}g_m \tag{11.15}$$

where $(I_Q/2)$ is the quiescent collector current in Q_1 and Q_2. The magnitude of the small-signal collector current in each transistor is then $(g_m v_d)/2$.

Figure 11.6 also shows the linear approximations for the collector currents in terms of the transistor transconductances g_m. The slope of i_{C1} versus v_d is the same magnitude as that of i_{C2} versus v_d, but it has the opposite sign. This is the reason for the negative sign in the expression for i_{C2} versus v_d.

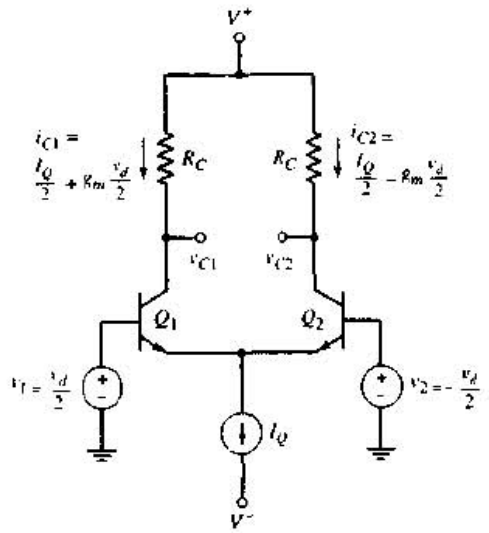


Figure 11.6 BJT differential amplifier with differential-mode input signal

We can define the output signal voltage as

$$v_o = v_{C2} - v_{C1} \tag{11.16}$$

When the output is defined as the difference between the two collector voltages, we have a **two-sided output**. From Figure 11.6, we can write the output voltage as

$$v_o = [V^+ - i_{C2}R_C] - [V^+ - i_{C1}R_C] = (i_{C1} - i_{C2})R_C \tag{11.17(a)}$$

or

$$v_o = \left[\left(\frac{I_Q}{2} + \frac{g_m v_d}{2}\right) - \left(\frac{I_Q}{2} - \frac{g_m v_d}{2}\right)\right] R_C = g_m R_C v_d \tag{11.17(b)}$$

Figure 11.7 shows the ac equivalent circuit of the diff-amp configuration, as well as the signal voltages and currents as functions of the transistor transconductances g_m. Since we are assuming an ideal current source, the output resistance looking into the current source is infinite (represented by the dashed line). Using the equivalent circuit in Figure 11.7(a), we find the signal output voltage to be

$$v_o = v_{c2} - v_{c1} = \left(\frac{g_m v_d}{2}\right) R_C - \left(\frac{-g_m v_d}{2}\right) R_C = g_m R_c v_d \tag{11.18}$$

which is the same as Equation (11.17(b)).

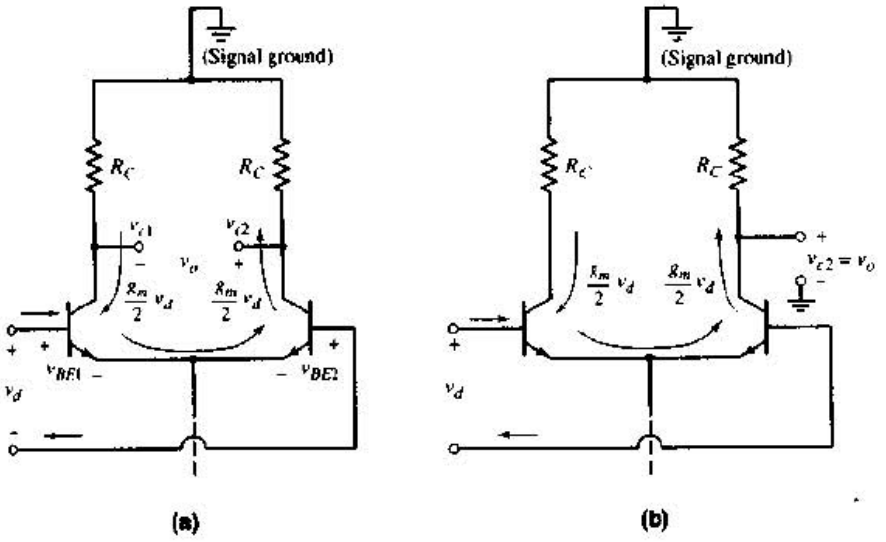


Figure 11.7 (a) Equivalent ac circuit, diff-amp with differential-mode input signal and two-sided output voltage and (b) ac equivalent circuit with one-sided output

The ratio of the output signal voltage to the differential-mode input signal is called the **differential-mode gain**, A_d, which is

$$A_d = \frac{v_o}{v_d} = g_m R_C = \frac{I_Q R_C}{2V_T} \tag{11.19}$$

If the output voltage is the difference between the two collector terminal voltages, then neither side of the output voltage is at ground potential. In many

cases, the output voltage is taken at one collector terminal with respect to ground. The resulting voltage output is called a **one-sided output**. If we define the output to be v_{c2}, then from Figure 11.7(b), the signal output voltage is

$$v_o = \left(\frac{g_m v_d}{2}\right) R_C \tag{11.20}$$

The differential gain for the one-sided output is then given by

$$A_d = \frac{v_o}{v_d} = \frac{g_m R_C}{2} = \frac{I_Q R_C}{4V_T} \tag{11.21}$$

The differential gain for the one-sided output is one-half that of the two-sided output. However, as we will see in our discussion on active loads, only a one-sided output is available.

11.2.3 Small-Signal Equivalent Circuit Analysis

The dc transfer characteristics derived in the last section provide insight into the operation of the differential amplifier. Assuming we are operating in the linear range, we can also derive the gain and other characteristics of the diff-amp, using the small-signal equivalent circuit.

Figure 11.8 shows the small-signal equivalent circuit of the bipolar differential-pair configuration. We assume that the Early voltage is infinite for the two emitter-pair transistors, and that the constant-current source is not ideal but can be represented by a finite output impedance R_o. Resistances R_B are also included. These represent the output resistance of the signal voltage sources. All voltages are represented by their phasor components. Since the two transistors are biased at the same quiescent current, we have

$$r_{\pi 1} = r_{\pi 2} \equiv r_\pi \qquad \text{and} \qquad g_{m1} = g_{m2} \equiv g_m$$

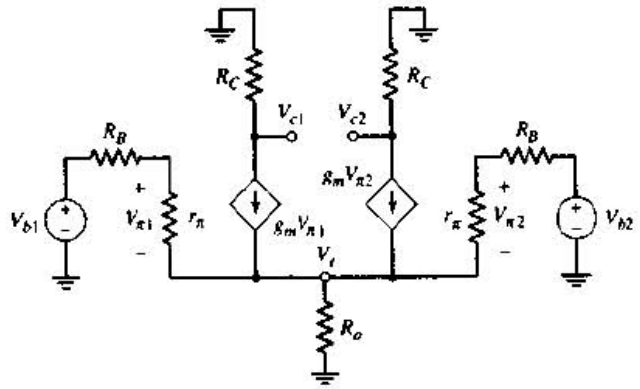


Figure 11.8 Small-signal equivalent circuit, bipolar differential amplifier

Writing a KCL equation at node V_e, using phasor notation, we have

$$\frac{V_{\pi 1}}{r_\pi} + g_m V_{\pi 1} + g_m V_{\pi 2} + \frac{V_{\pi 2}}{r_\pi} = \frac{V_e}{R_o} \tag{11.22(a)}$$

or

$$V_{\pi 1}\left(\frac{1+\beta}{r_\pi}\right)+V_{\pi 2}\left(\frac{1+\beta}{r_\pi}\right)=\frac{V_e}{R_o} \qquad \textbf{(11.22(b))}$$

where $g_m r_\pi = \beta$. From the circuit, we see that

$$\frac{V_{\pi 1}}{r_\pi}=\frac{V_{b1}-V_e}{r_\pi+R_B} \quad \text{and} \quad \frac{V_{\pi 2}}{r_\pi}=\frac{V_{b2}-V_e}{r_\pi+R_B}$$

Solving for $V_{\pi 1}$ and $V_{\pi 2}$ and substituting into Equation (11.22(b)), we find

$$(V_{b1}+V_{b2}-2V_e)\left(\frac{1+\beta}{r_\pi+R_B}\right)=\frac{V_e}{R_o} \qquad \textbf{(11.23)}$$

Solving for V_e, we obtain

$$V_e=\frac{V_{b1}+V_{b2}}{2+\dfrac{r_\pi+R_B}{(1+\beta)R_o}} \qquad \textbf{(11.24)}$$

If we consider a one-sided output at the collector of Q_2, then

$$V_o=V_{c2}=-(g_m V_{\pi 2})R_C=-\frac{\beta R_C(V_{b2}-V_e)}{r_\pi+R_B} \qquad \textbf{(11.25)}$$

Substituting Equation (11.24) into (11.25) and rearranging terms yields

$$V_o=-g_m R_C\left\{\frac{V_{b2}\left[1+\dfrac{r_\pi+R_B}{(1+\beta)R_o}\right]-V_{b1}}{2+\dfrac{r_\pi+R_B}{(1+\beta)R_o}}\right\} \qquad \textbf{(11.26)}$$

In an ideal constant-current source, the output resistance is $R_o = \infty$, and Equation (11.26) reduces to

$$V_o=-\frac{\beta R_C(V_{b2}-V_{b1})}{2(r_\pi+R_B)} \qquad \textbf{(11.27)}$$

The differential-mode input is

$$V_d = V_{b1} - V_{b2}$$

and the differential-mode gain is

$$A_d=\frac{V_o}{V_d}=\frac{\beta R_C}{2(r_\pi+R_B)} \qquad \textbf{(11.28)}$$

which for $R_B = 0$ is identical to Equation (11.21), which was developed from the voltage transfer characteristics.

Equation (11.26) includes a finite output resistance for the current source. We can see that when a common-mode signal $V_{cm} = V_{b1} = V_{b2}$ is applied, the output voltage is no longer zero.

Differential- and common-mode voltages are defined in Equations (11.2) and (11.3). Using phasor notation, we can solve these equations for V_{b1} and V_{b2} in terms of V_d and V_{cm}. We obtain

$$V_{b1}=V_{cm}+\frac{V_d}{2} \qquad \textbf{(11.29(a))}$$

and

$$V_{b2} = V_{cm} - \frac{V_d}{2} \tag{11.29(b)}$$

Since we are dealing with a linear amplifier, superposition applies. Equations (11.29(a)) and (11.29(b)) then simply state that the two input signals can be written as the sum of a differential-mode input signal component and a common-mode input signal component.

Substituting Equations (11.29(a)) and (11.29(b)) into Equation (11.26) and rearranging terms results in the following:

$$V_o = \frac{\beta R_C}{2(r_\pi + R_B)} \cdot V_d - \frac{g_m R_C}{1 + \dfrac{2(1+\beta)R_o}{r_\pi + R_B}} \cdot V_{cm} \tag{11.30}$$

We can write the output voltage in the general form

$$V_o = A_d V_d + A_{cm} V_{cm} \tag{11.31}$$

where A_d is the differential-mode gain and A_{cm} is the common-mode gain. Comparing Equations (11.30) and (11.31), we see that the differential-mode gain is

$$A_d = \frac{\beta R_C}{2(r_\pi + R_B)} \tag{11.32(a)}$$

and the common-mode gain is

$$A_{cm} = \frac{-g_m R_C}{1 + \dfrac{2(1+\beta)R_o}{r_\pi + R_B}} \tag{11.32(b)}$$

We again observe that the common-mode gain goes to zero for an ideal current source in which $R_o = \infty$. For a nonideal current source, R_o is finite and the common-mode gain is not zero for this case of a one-sided output. A nonzero common-mode gain implies that the diff-amp is not ideal. We will see implications of the nonideal effects in later discussions.

Example 11.3 **Objective:** Determine the differential- and common-mode gains of a diff-amp.

Consider the circuit in Figure 11.2, with parameters: $V^+ = 10\,\text{V}$, $V^- = -10\,\text{V}$, $I_Q = 0.8\,\text{mA}$, and $R_C = 12\,\text{k}\Omega$. The transistor parameters are $\beta = 100$ and $V_A = \infty$. Assume the output resistance looking into the constant-current source is $R_o = 25\,\text{k}\Omega$. Assume the source resistors R_B are zero. Use a one-sided output at v_{C2}.

Solution: From Equation (11.32(a)), the differential-mode gain is

$$A_d = \frac{g_m R_C}{2} = \frac{I_{CQ} R_C}{2V_T} = \frac{I_Q R_C}{4V_T} = \frac{(0.8)(12)}{4(0.026)} = 92.3$$

From Equation (11.32(b)), the common-mode gain is

$$A_{cm} = \frac{-\left(\dfrac{I_Q R_C}{2V_T}\right)}{1 + \dfrac{(1+\beta)I_Q R_o}{V_T \beta}} = \frac{-\left[\dfrac{(0.8)(12)}{(2)(0.026)}\right]}{1 + \dfrac{(101)(0.8)(25)}{(0.026)(100)}} = -0.237$$

Comment: The common-mode gain is significantly less than the differential-mode gain, but it is not zero as determined for the ideal diff-amp with an ideal current source.

Design Example 11.4 Objective: Design a differential amplifier to meet the specifications of the following experimental system.

Figure 11.9 shows a Hall-effect experiment to measure semiconductor material parameters. A Hall voltage V_H, which is perpendicular to both a current I_X and a magnetic field B_Z, is to be measured by using a diff-amp. The range of V_H is $-8 \le V_H \le +8\,\text{mV}$ and the desired range of the diff-amp output signal is to be $-0.8 \le V_O \le +0.8\,\text{V}$. The probes that make contact to the semiconductor have an effective resistance of 500 Ω, and each probe has an induced 60 Hz signal with a magnitude of 100 mV. The diff-amp output 60 Hz signal is to be no larger than 10 mV. Typically, $V_X = 5\,\text{V}$, so that the quiescent or common-mode voltage of the Hall probes is 2.5 V.

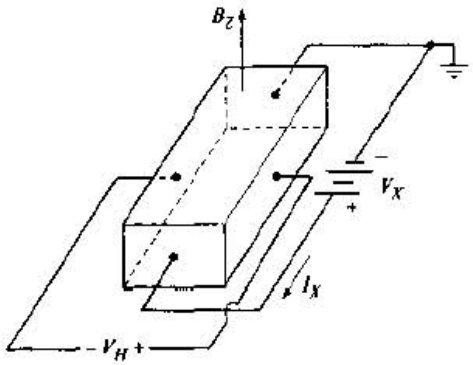


Figure 11.9 Experimental arrangement for measuring Hall voltage

Design Approach: For this example, we will use a bipolar diff-amp with the configuration shown in Figure 11.6. Assume that transistors are available with $\beta = 100$. Assume bias voltages of ±10 V and choose a bias current of $I_Q = 0.5\,\text{mA}$.

Solution: Differential-Mode Gain: The differential-mode voltage gain requirement is

$$A_d = \frac{V_o}{V_d} = \frac{0.8}{0.008} = 100$$

The small-signal parameters are then

$$r_\pi = \frac{\beta V_T}{I_{CQ}} = \frac{(100)(0.026)}{0.25} = 10.4\,\text{k}\Omega$$

and

$$g_m = \frac{I_{CQ}}{V_T} = \frac{0.25}{0.026} = 9.62\,\text{mA/V}$$

The differential gain is

$$A_d = \frac{\beta R_C}{2(r_\pi + R_B)}$$

or

$$100 = \frac{(100)R_C}{2(10.4 + 0.5)}$$

which means that $R_C = 21.8\,\text{k}\Omega$. We may note that the voltage drop across R_C under quiescent conditions is 5.45 V. With a 2.5 V common-mode input voltage, the quiescent collector-emitter voltages of Q_1 and Q_2 are approximately 3.65 V. The two input transistors will then remain in the active region.

Solution: Common-Mode Gain: The common-mode voltage gain requirement is

$$A_{cm} = \frac{V_o}{V_{cm}} = \frac{10\,\text{mV}}{100\,\text{mV}} = 0.10$$

The common-mode gain is given by

$$|A_{cm}| = \frac{g_m R_C}{1 + \dfrac{2(1+\beta)R_o}{r_x + R_B}}$$

or

$$0.10 = \frac{(9.62)(21.8)}{1 + \dfrac{2(101)R_o}{10.4 + 0.5}}$$

which means that $R_o = 113\,\text{k}\Omega$. If we consider a simple two-transistor current source as discussed in the last chapter, the output resistance is $R_o = r_o = V_A/I_Q$, where V_A is the Early voltage. With $I_Q = 0.5$ mA, then $V_A = 56.5$ V is the Early voltage requirement. This specification is not difficult to achieve for most bipolar transistors.

Computer Simulation Verification: Figure 11.10 shows the circuit used in the computer simulation for this example. The bias current I_Q supplied by the Q_3 current source transistor is 0.568 mA. A 2.5 V common-mode input voltage is applied, a 500 Ω source (probe) resistance is included, and an 8 mV differential-mode input signal is applied. The differential output signal voltage measured at the collector of Q_2 is 0.84 V, which is just slightly larger than the designed value. The current gains of the standard 2N3904 transistors used in the computer simulation are larger than the values of 100 used in the hand analysis and design. A common-mode signal voltage of 100 mV replaced the differential-mode signals. The common-mode output signal is 7.11 mV, which is within the design specification.

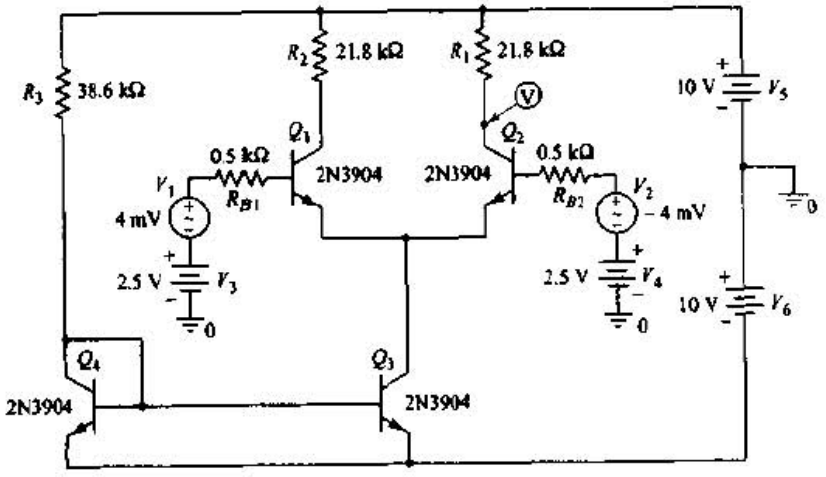


Figure 11.10 Circuit used in the computer simulation of Design Example 11.4

Test Your Understanding

11.6 In the differential amplifier in Figure 11.11, neglect base currents and assume $V_{EB}(\text{on}) = 0.7\,\text{V}$. Determine v_E and v_{EC1} for common-mode input voltages $v_1 = v_2 = v_{cm}$ of: (a) 0 V, (b) +2.5 V, and (c) −2.5 V. (Ans. (a) $v_E = +0.7\,\text{V}$, $v_{EC1} = 3.7\,\text{V}$ (b) $v_E = 3.2\,\text{V}$, $v_{EC1} = 6.2\,\text{V}$ (c) $v_E = -1.8\,\text{V}$, $v_{EC1} = 1.2\,\text{V}$)

D11.7 Using the diff-amp configuration in Figure 11.2, design the circuit such that the differential-mode voltage gain at v_{c2} is +150 and the differential-mode voltage gain at v_{C1} is −100. (Ans. For example, if $I_Q = 1\,\text{mA}$, then $R_C = 15.6\,\text{k}\Omega$ at collector of Q_2 and $R_C = 10.4\,\text{k}\Omega$ at collector of Q_1)

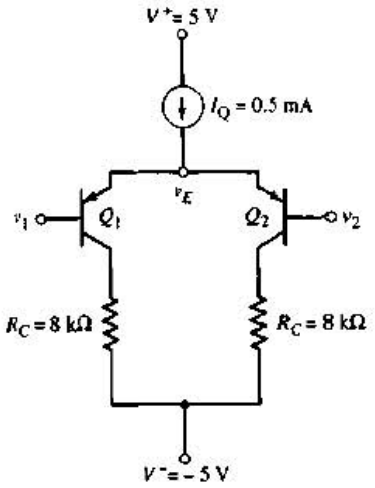


Figure 11.11 Figure for Exercise 11.6

11.2.4 Differential- and Common-Mode Gains

For greater insight into the mechanism that causes differential- and common-mode gains, we reconsider the diff-amp as pure differential- and common-mode signals are applied.

Figure 11.12(a) shows the ac equivalent circuit of the diff-amp with two sinusoidal input signals. The two input voltages are 180 degrees out of phase, so a pure differential-mode signal is being applied to the diff-amp. We see that $v_{b1} + v_{b2} = 0$. From Equation (11.24), the common emitters of Q_1 and Q_2 remain at signal ground. In essence, the circuit behaves like a balanced seesaw. As the base voltage of Q_1 goes into its positive-half cycle, the base voltage of Q_2 is in its negative half-cycle. Then, as the base voltage of Q_1 goes into its negative half-cycle, the base voltage of Q_2 is in its positive half-cycle. The signal current directions shown in the figure are valid for v_{b1} in its positive half-cycle.

Since v_e is always at ground potential, we can treat each half of the diff-amp as a common-emitter circuit. Figure 11.12(b) shows the differential half-circuits, clearly depicting the common-emitter configuration. The differential-

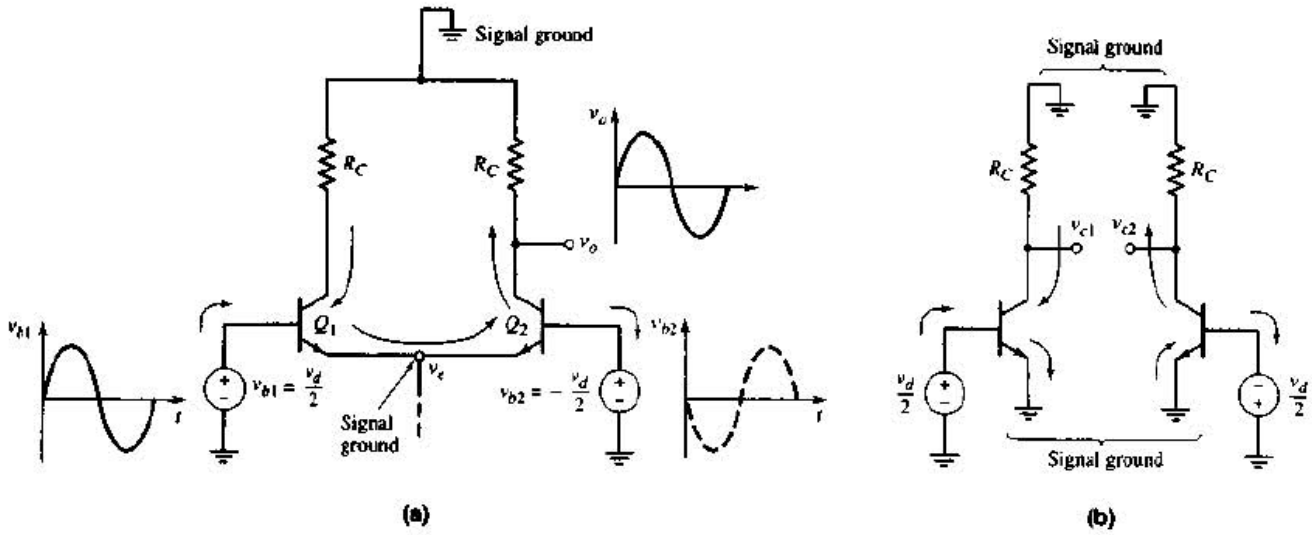


Figure 11.12 (a) Equivalent ac circuit, diff-amp with applied sinusoidal differential-mode input signal, and resulting signal current directions and (b) differential-mode half-circuits

mode characteristics of the diff-amp can be determined by analyzing the half-circuit. In evaluating the small-signal hybrid-π parameters, we must keep in mind that the half-circuit is biased at $I_Q/2$.

Figure 11.13(a) shows the ac equivalent circuit of the diff-amp with a pure common-mode sinusoidal input signal. In this case, the two input voltages are in phase. The current source is represented as an ideal source I_Q in parallel with its output resistance R_O. Current i_q is the time-varying component of the source current. As the two input signals increase, voltage v_e increases and current i_q increases. Since this current splits evenly between Q_1 and Q_2, each collector current also increases. The output voltage v_o then decreases below its quiescent value.

As the two input voltages go through the negative half-cycle, all signal currents shown in the figure reverse direction, and v_o increases above its quiescent value. Consequently, a common-mode sinusoidal input signal produces a sinusoidal output voltage, which means that the diff-amp has a nonzero common-mode voltage gain. If the value of R_o increases, the magnitude of i_q decreases for a given common-mode input signal, producing a smaller output voltage and hence a smaller common-mode gain.

With an applied common-mode voltage, the circuit shown in Figure 11.13(a) is perfectly symmetrical. The circuit can therefore be split into the identical common-mode half-circuits shown in Figure 11.13(b). The common-mode characteristics of the diff-amp can then be determined by analyzing the half-circuit, which is a common-emitter configuration with an emitter resistor. Each half-circuit is biased at $I_Q/2$.

The following examples further illustrate the effect of a nonzero common-mode gain on circuit performance.

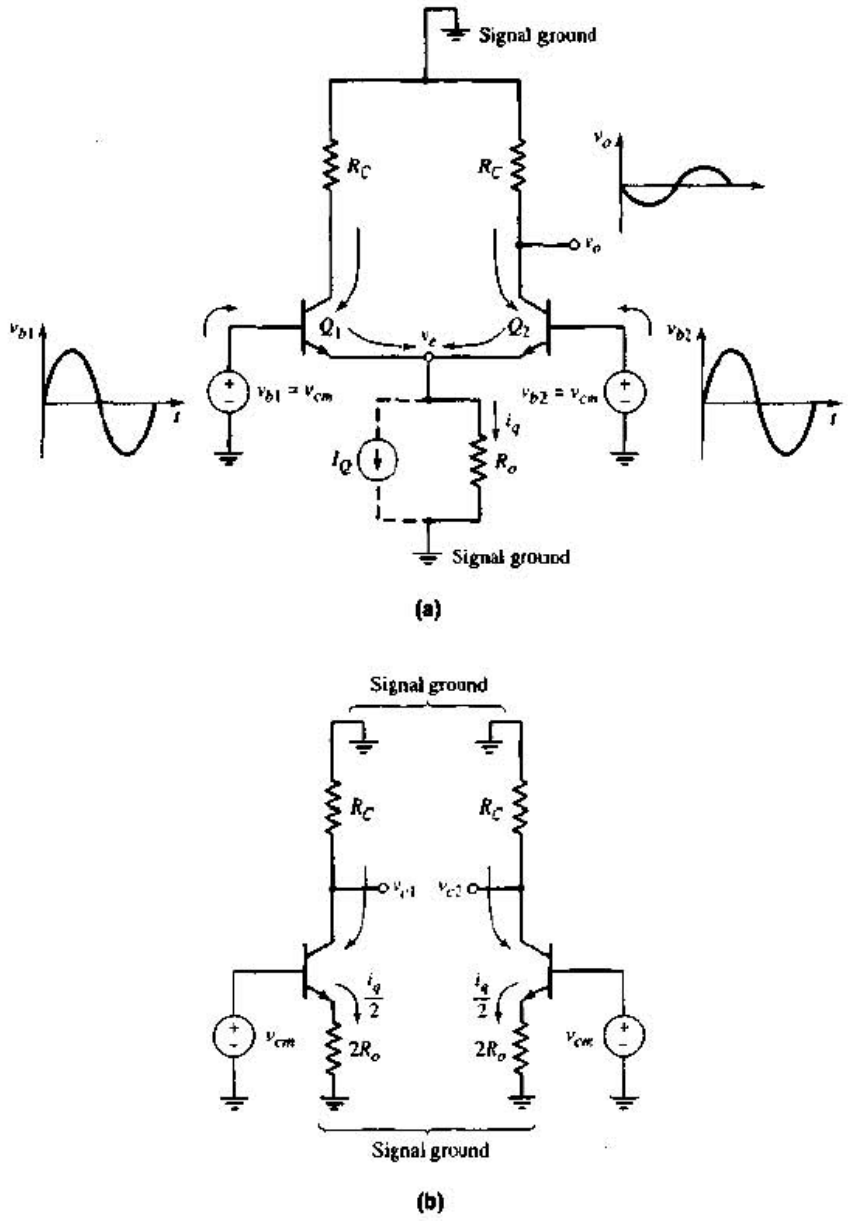


Figure 11.13 (a) Equivalent ac circuit of diff-amp with common-mode input signal, and resulting signal current directions and (b) common-mode half-circuits

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Example 11.5 **Objective:** Determine the output voltage of a diff-amp when only a common-mode signal is applied.

Consider the circuit in Figure 11.2. Use the transistor and circuit parameters described in Example 11.3. Assume the common-mode input signal is $v_1 = v_2 = v_{cm} = 200 \sin \omega t\ \mu V$.

Solution: From Example 11.3, the common-mode gain is $A_{cm} = -0.237$. Since the differential-mode input signal is zero, the output signal voltage is

$$v_o = A_{cm} v_{cm} = -(0.237)(200 \sin \omega t)\ \mu V = -47.4 \sin \omega t\ \mu V$$

Comment: When the magnitude of the common-mode gain is less than unity, the common-mode output voltage is less than the common-mode input voltage; yet it is not zero, which would occur in an ideal diff-amp.

Example 11.6 **Objective:** Determine the output of a diff-amp when both differential- and common-mode signals are applied.

Consider the circuit shown in Figure 11.2. Use the transistor and circuit parameters described in Example 11.3. Assume that four sets of inputs are applied, as described in the following table, which also includes the differential- and common-mode voltages.

	Input signal (μV)	Differential- and common-mode input signals (μV)
Case 1	$v_1 = 10\sin\omega t$	$v_d = 20\sin\omega t$
	$v_2 = -10\sin\omega t$	$v_{cm} = 0$
Case 2	$v_1 = 20\sin\omega t$	$v_d = 40\sin\omega t$
	$v_2 = -20\sin\omega t$	$v_{cm} = 0$
Case 3	$v_1 = 210\sin\omega t$	$v_d = 20\sin\omega t$
	$v_2 = 190\sin\omega t$	$v_{cm} = 200\sin\omega t$
Case 4	$v_1 = 220\sin\omega t$	$v_d = 40\sin\omega t$
	$v_2 = 180\sin\omega t$	$v_{cm} = 200\sin\omega t$

Solution: The output voltage is given by Equation (11.31), as follows:

$$v_o = A_d v_d + A_{cm} v_{cm}$$

From Example 11.3, the differential- and common-mode gains are $A_d = 92.3$ and $A_{cm} = -0.237$. The output voltages for the four sets of inputs are:

	Output signal (mV)
Case 1	$v_o = 1.846\sin\omega t$
Case 2	$v_o = 3.692\sin\omega t$
Case 3	$v_o = 1.799\sin\omega t$
Case 4	$v_o = 3.645\sin\omega t$

Comment: In cases 1 and 2, the common-mode input is zero, and the output is directly proportional to the differential input signal. Comparing cases 1 and 3 and cases 2 and 4, we see that the output voltages are not equal, even though the differential input signals are the same. This shows that the common-mode signal affects the output. Also, even though the differential signal is doubled, in cases 4 and 3, the ratio of the output signals is not 2.0. If a common-mode signal is present, the output is not exactly linear with respect to the differential input signal.

Analysis Technique: Diff-Amps with Resistive Loads

1. To determine the differential-mode voltage gain, apply a pure differential-mode input voltage and use the differential-mode half-circuit in the analysis.
2. To determine the common-mode voltage gain, apply a pure common-mode input voltage and use the common-mode half-circuit in the analysis.

11.2.5 Common-Mode Rejection Ratio

The ability of a differential amplifier to reject a common-mode signal is described in terms of the common-mode rejection ratio (CMRR). The CMRR is a figure-of-merit for the diff-amp and is defined as

$$\text{CMRR} = \left|\frac{A_d}{A_{cm}}\right| \tag{11.33}$$

For an ideal diff-amp, $A_{cm} = 0$ and CMRR $= \infty$. Usually, the CMRR is expressed in decibels, as follows:

$$\text{CMMR}_{\text{dB}} = 20\log_{10}\left|\frac{A_d}{A_{cm}}\right| \tag{11.34}$$

For the diff-amp in Figure 11.2, the one-sided differential- and common-mode gains are given by Equations (11.32(a)) and (11.32(b)). Using these equations, we can express the CMRR as

$$\text{CMRR} = \left|\frac{A_d}{A_{cm}}\right| = \frac{1}{2}\left[1 + \frac{(1+\beta)I_Q R_o}{V_T \beta}\right] \tag{11.35}$$

The common-mode gain decreases as R_o increases. Therefore, we see that the CMRR increases as R_o increases.

Example 11.7 **Objective:** Determine the CMRR of a differential amplifier.

Consider the circuit shown in Figure 11.2, with circuit and transistor parameters as given in Example 11.3.

Solution: From the results of Example 11.3, we have $A_d = 92.3$ and $A_{cm} = -0.237$. The CMRR is then

$$\text{CMRR} = \left|\frac{A_d}{A_{cm}}\right| = \frac{92.3}{0.237} = 389$$

or, expressed in decibels,

$$\text{CMRR}_{\text{dB}} = 20\log_{10}(389) = 51.8\,\text{dB}$$

Comment: For "good" diff-amps, typical values of CMRR are in the range of 80–100 dB. The CMRR of the diff-amp in Figure 11.2 can be improved by increasing the current-source output resistance.

Design Example 11.8 Objective: Design a bipolar current source with the required output resistance parameter to meet a specified CMRR.

Consider the diff-amp in Figure 11.2. Use the circuit and transistor parameters given in Example 11.3. Determine the required value of R_o for $\text{CMRR}_{\text{dB}} = 90\,\text{dB}$.

Solution: If $\text{CMRR}_{\text{dB}} = 90\,\text{dB}$, then $\text{CMRR} = 3.16 \times 10^4$. From Equation (11.35), we have

$$\text{CMRR} = \left|\frac{A_d}{A_{cm}}\right| = \frac{1}{2}\left[1 + \frac{(1+\beta)I_Q R_o}{V_T \beta}\right]$$

or

$$3.16 \times 10^4 = \frac{1}{2}\left[1 + \frac{(101)(0.8)R_o}{(0.026)(100)}\right]$$

which yields

$$R_o = 2.03 \times 10^3\,\text{k}\Omega = 2.03\,\text{M}\Omega$$

Comment: This output resistance level can be achieved with a Widlar or Wilson current source.

Computer Simulation Verification: A standard two-transistor current source (Figure 10.2) was designed with 2N3904 bipolar transistors. With a bias current of 0.8 mA, the output resistance of the current source is 93.8 kΩ which is far below the design requirement. Using a modified Widlar current source (Figure P10.26) with 1 kΩ emitter resistors, the output resistance of the current source is 2.22 MΩ, which is within the design specification.

Test Your Understanding

***RD11.8** For the diff-amp shown in Figure 11.2, the parameters are $V^+ = 15\,\text{V}$ and $V^- = -15\,\text{V}$. Assume $\beta = 200$. The range for the common-mode input voltage is to be $-5 \le v_{cm} \le +5\,\text{V}$. (a) Redesign the circuit to produce the maximum one-sided differential-mode gain at v_{C2}. (b) If $R_o = 100\,\text{k}\Omega$ for the current source, determine the resulting common-mode gain and CMRR_{dB}. (Ans. (a) $I_Q R_C = 20\,\text{V}$, $A_d(\text{max}) = 192$ (b) For $I_Q = 0.5\,\text{mA}$ and $R_C = 40\,\text{k}\Omega$, $A_{cm} = -0.199$; $\text{CMRR}_{\text{dB}} = 59.7\,\text{dB}$)

***D11.9** Consider a differential amplifier with the configuration in Figure 11.14, biased with a modified Widlar current source. Assume transistor parameters of $\beta = 200$, $V_A = 125\,\text{V}$ for Q_3 and Q_4, and $V_A = \infty$ for Q_1 and Q_2. Design the circuit such that the common-mode input voltage is in the range $-5 \le v_{cm} \le +5\,\text{V}$, the common-mode rejection ratio is $\text{CMRR}_{\text{dB}} = 95\,\text{dB}$, and the maximum differential-mode voltage gain is achieved. (Ans. For example, let $I_Q = 0.5\,\text{mA}$ and $I_1 = 1\,\text{mA}$. Then $R_1 = 18.7\,\text{k}\Omega$, $R_2 = 1.31\,\text{k}\Omega$, $R_3 = 0.637\,\text{k}\Omega$, and $R_C = 20\,\text{k}\Omega$.)

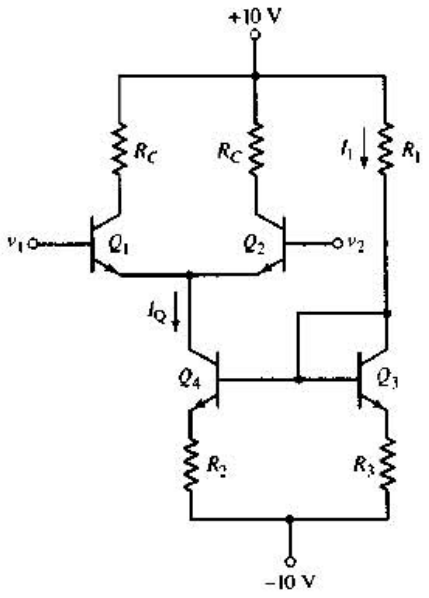


Figure 11.14 Figure for Exercise 11.9

11.2.6 Differential- and Common-Mode Input Impedances

The input impedance, or resistance, of an amplifier is as important a property as the voltage gain. The input resistance determines the loading effect of the circuit on the signal source. We will look at two input resistances for the difference amplifier: the **differential-mode input resistance**, which is the resistance seen by a differential-mode signal source; and the **common-mode input resistance**, which is the resistance seen by a common-mode input signal source.

Differential-Mode Input Resistance

The differential-mode input resistance is the effective resistance between the two input base terminals when a differential-mode signal is applied. A diff-amp with a pure differential input signal is shown in Figure 11.15. The applicable differential-mode half-circuits are shown in Figure 11.12(b). For this circuit, we have

$$\frac{v_d/2}{i_b} = r_\pi \tag{11.36}$$

The differential-mode input resistance is therefore

$$R_{id} = \frac{v_d}{i_b} = 2r_\pi \tag{11.37}$$

Another common diff-amp configuration uses emitter resistors, as shown in Figure 11.16. With a pure applied differential-mode voltage, similar differential-mode half-circuits are applicable to this configuration. We can then use the resistance reflection rule to find the differential-mode input resistance. We have

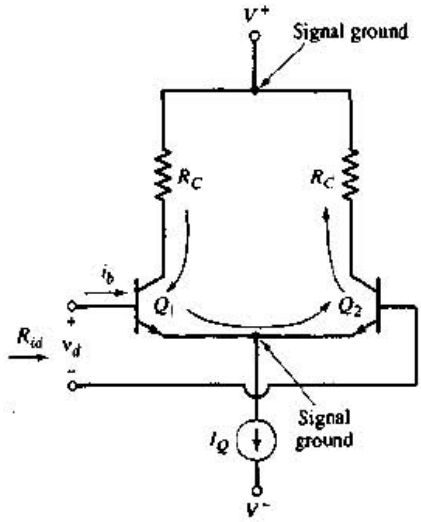


Figure 11.15 BJT differential amplifier with differential-mode input signal, showing differential input resistance

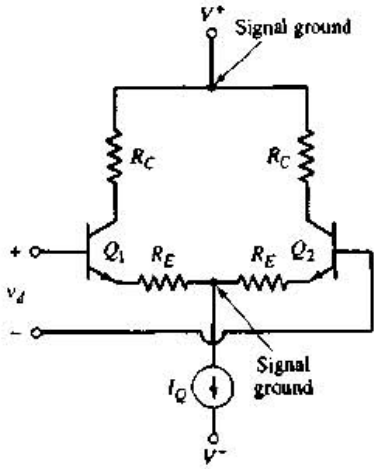


Figure 11.16 BJT differential amplifier with emitter resistors

$$\frac{v_d/2}{i_b} = r_\pi + (1 + \beta)R_E \tag{11.38}$$

Therefore,

$$R_{id} = \frac{v_d}{i_b} = 2[r_\pi + (1 + \beta)R_E] \tag{11.39}$$

Equation (11.39) implies that differential-mode input resistance increases significantly when emitter resistors are included. Although the differential-mode gain decreases when emitter resistors are included, a larger differential-mode voltage (greater than 18 mV) may be applied and the amplifier remains linear.

Common-Mode Input Resistance

Figure 11.17(a) shows a diff-amp with an applied common-mode voltage. The small-signal output resistance R_o of the constant-current source is also shown. The equivalent common-mode half-circuits are given in Figure 11.13(b). Since the half-circuits are in parallel, we can write

$$2R_{icm} = r_\pi + (1+\beta)(2R_o) \cong (1+\beta)(2R_o) \tag{11.40}$$

Equation (11.40) is a first approximation for determining the common-mode input resistance.

(a) (b)

Figure 11.17 (a) BJT differential amplifier with common-mode input signal, including finite current source resistance and (b) equivalent common-mode half-circuit

Normally, R_o is large, and R_{icm} is typically in the megohm range. Therefore, the transistor output resistance r_o and the base–collector resistance r_μ may need to be included in the calculation. Figure 11.17(b) shows the more complete equivalent half-circuit model. For this model, we have

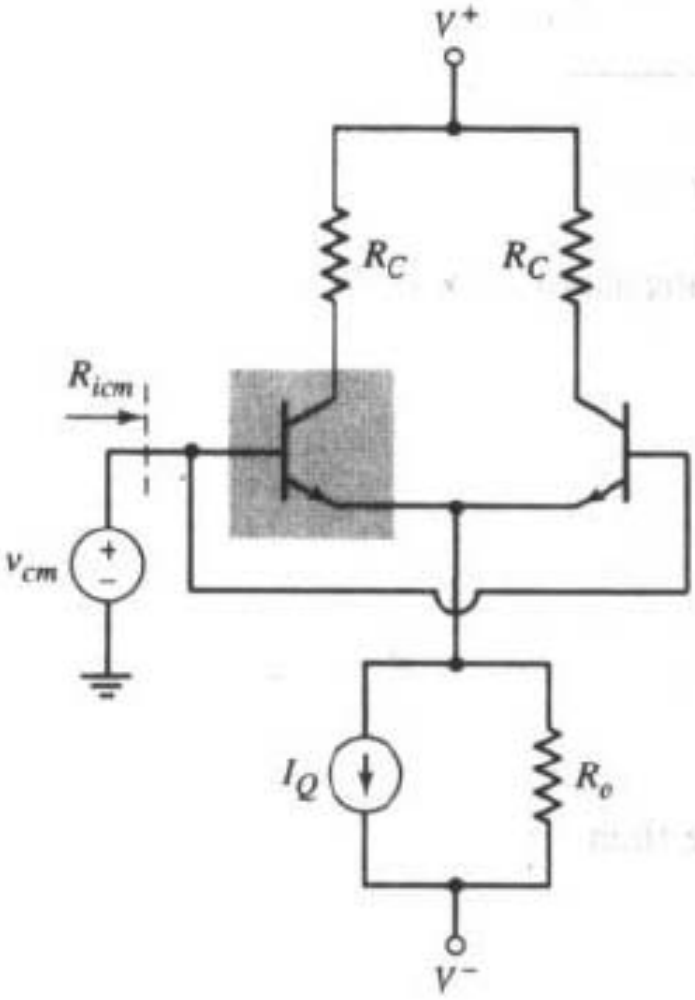
$$2R_{icm} = r_\mu \| [(1+\beta)(2R_o)] \| [(1+\beta)r_o] \tag{11.41(a)}$$

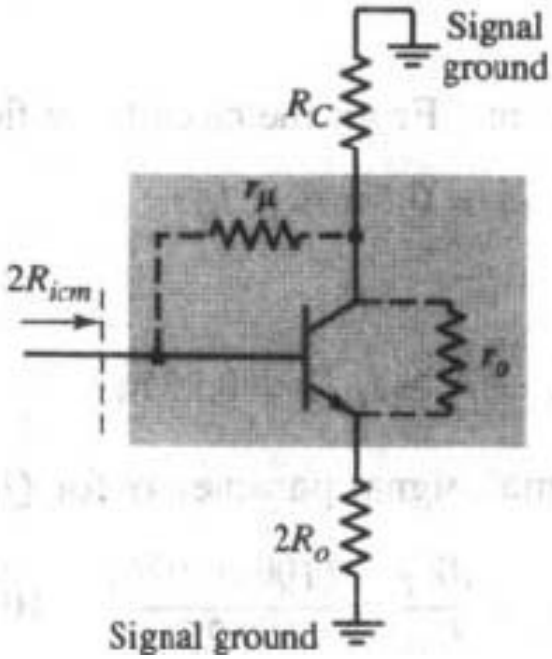
Therefore,

$$R_{icm} = \left(\frac{r_\mu}{2}\right) \left\| [(1+\beta)(R_o)] \right\| \left[(1+\beta)\left(\frac{r_o}{2}\right)\right] \tag{11.41(b)}$$

Example 11.9 **Objective:** Determine the differential- and common-mode input resistances of a differential amplifier.

Consider the circuit in Figure 11.18, with transistor parameters $\beta = 100$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, and $V_A = 100\,\text{V}$. Determine R_{id} and R_{icm}.


V^+
R_C
R_C
R_{icm}
v_{cm}
I_Q
R_o
V^-


Signal ground
R_C
r_μ
$2R_{icm}$
r_o
$2R_o$
Signal ground

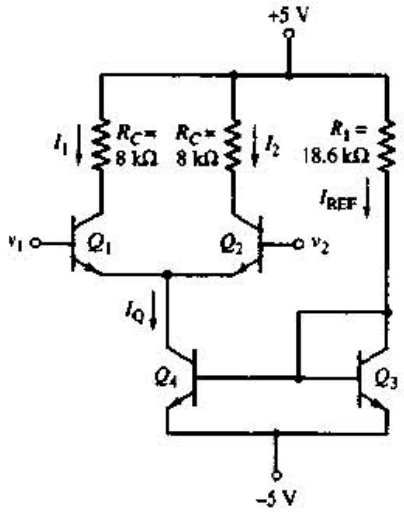


Figure 11.18 BJT differential amplifier for Example 11.9

Solution: From the circuit, we find

$$I_{REF} = 0.5\,\text{mA} \cong I_Q$$

and

$$I_1 = I_2 \cong I_Q/2 = 0.25\,\text{mA}$$

The small-signal parameters for Q_1 and Q_2 are then

$$r_\pi = \frac{\beta V_T}{I_{CQ}} = \frac{(100)(0.026)}{0.25} = 10.4\,\text{k}\Omega$$

and

$$r_o = \frac{V_A}{I_{CQ}} = \frac{100}{0.25} = 400\,\text{k}\Omega$$

and the output resistance of Q_4 is

$$R_o = \frac{V_A}{I_Q} = \frac{100}{0.5} = 200\,\text{k}\Omega$$

From Equation (11.37), the differential-mode input resistance is

$$R_{id} = 2r_\pi = 2(10.4) = 20.8\,\text{k}\Omega$$

From Equation (11.41(b)), neglecting the effect of r_μ, the common-mode input resistance is

$$R_{icm} = (1+\beta)\left[(R_o)\left\|\left(\frac{r_o}{2}\right)\right.\right] = (101)\left\{200\left\|\left(\frac{400}{2}\right)\right.\right\}\text{k}\Omega \rightarrow 10.1\,\text{M}\Omega$$

Comment: If a differential-mode input voltage with a peak value of 15 mV is applied, the source must be capable of supplying a current of $15 \times 10^{-3}/20.8 \times 10^{+3} = 0.72\,\mu A$ without any severe loading effect. However, the input current from a 15 mV common-mode signal would only be approximately 1.5 nA.

Test Your Understanding

11.10 If the differential-mode gain of a diff-amp is $A_d = 60$ and the common-mode gain is $A_{cm} = 0.5$, determine the output voltage for input signals of: (a) $v_1 = 0.505 \sin \omega t$ V, $v_2 = 0.495 \sin \omega t$ V, and (b) $v_1 = 0.5 + 0.005 \sin \omega t$ V, $v_2 = 0.5 - 0.005 \sin \omega t$ V. (Ans. (a) $v_o = 0.85 \sin \omega t$ V (b) $v_o = 0.25 + 0.6 \sin \omega t$ V)

11.11 A differential amplifier is shown in Figure 11.2. The parameters are: $V^+ = 10$ V, $V^- = -10$ V, $I_Q = 2$ mA, and $R_C = 5$ kΩ. The output resistance of the constant-current source is $R_o = 50$ kΩ, and the transistor parameters are: $\beta = 150$, $V_{BE}(\text{on}) = 0.7$ V, and $V_A = \infty$. (a) Determine the dc input base currents. (b) Determine the differential signal input currents if a differential mode input voltage $v_d = 10 \sin \omega t$ mV is applied. (c) If a common-mode input voltage $v_{cm} = 3 \sin \omega t$ V is applied, determine the common-mode signal input currents. (Ans. (a) $I_{B1} = I_{B2} = 6.62\,\mu$A (b) $I_b = 1.28 \sin \omega t\,\mu$A (c) $I_b = 0.199 \sin \omega t\,\mu$A)

11.3 BASIC FET DIFFERENTIAL PAIR

In this section, we will evaluate the basic FET differential amplifier, concentrating on the MOSFET diff-amp. As we did for the bipolar diff-amp, we will develop the dc transfer characteristics, and determine the differential- and common-mode gains. The MOSFET with an active load is then considered.

Differential amplifiers using JFETs are also available. Since the analysis is almost identical to that for the MOSFET diff-amp, we will only briefly consider the JFET differential pair. A few of the problems at the end of this chapter are based on these circuits.

11.3.1 DC Transfer Characteristics

Figure 11.19 shows the basic MOSFET differential pair, with matched transistors M_1 and M_2 biased with a constant current I_Q. We assume that M_1 and

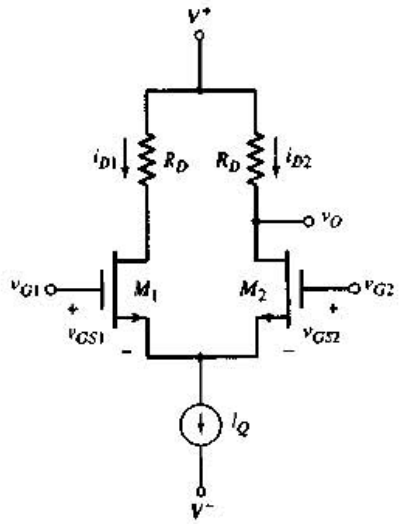


Figure 11.19 Basic MOSFET differential pair configuration

M_2 are always biased in the saturation region. MOSFET current-source circuits were discussed in Chapter 10 in Section 10.2.

Like the basic bipolar configuration, the basic MOSFET diff-amp uses both positive and negative bias voltages, thereby eliminating the need for coupling capacitors and voltage divider biasing resistors at the gate terminals. Even with $v_{G1} = v_{G2} = 0$, the transistors M_1 and M_2 can be biased in the saturation region by the current source I_Q. This circuit, then, is also a **dc-coupled** diff-amp.

Example 11.10 **Objective:** Calculate the dc characteristics of a MOSFET diff-amp.

Consider the differential amplifier shown in Figure 11.20. The transistor parameters are: $K_{n1} = K_{n2} = 0.1\,\text{mA/V}^2$, $K_{n3} = K_{n4} = 0.3\,\text{mA/V}^2$, and for all transistors, $\lambda = 0$ and $V_{TN} = 1\,\text{V}$. Determine the maximum range of common-mode input voltage.

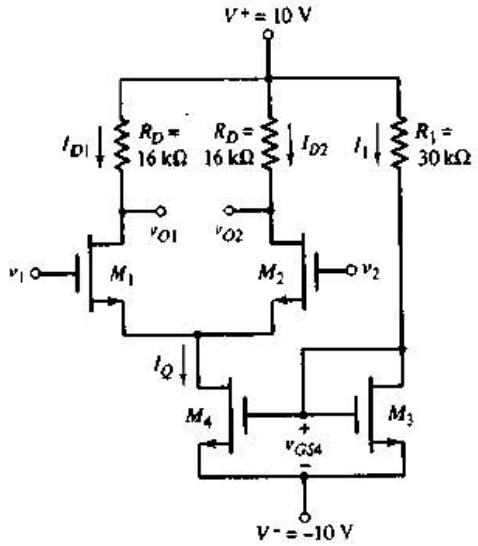


Figure 11.20 MOSFET differential amplifier for Example 11.10

Solution: The reference current can be determined from

$$I_1 = \frac{20 - V_{GS4}}{R_1}$$

and from

$$I_1 = K_{n3}(V_{GS4} - V_{TN})^2$$

Combining these two equations and substituting the parameter values, we obtain

$$9V_{GS4}^2 - 17V_{GS4} - 11 = 0$$

which yields

$$V_{GS4} = 2.40\,\text{V} \quad \text{and} \quad I_1 = 0.587\,\text{mA}$$

Since M_3 and M_4 are identical, we also find

$I_Q = 0.587\,\text{mA}$

The quiescent drain currents in M_1 and M_2 are

$I_{D1} = I_{D2} = I_Q/2 \cong 0.293\,\text{mA}$

The gate-to-source voltages are then

$$V_{GS1} = V_{GS2} = \sqrt{\frac{I_{D1}}{K_{n1}}} + V_{TN} = \sqrt{\frac{0.293}{0.1}} + 1 = 2.71\,\text{V}$$

The quiescent values of v_{O1} and v_{O2} are

$v_{O1} = v_{O2} = 10 - I_{D1}R_D = 10 - (0.293)(16) = 5.31\,\text{V}$

The maximum common-mode input voltage is the value when M_1 and M_2 reach the transition point, or

$V_{DS1} = V_{DS2} = V_{DS1}(\text{sat}) = V_{GS1} - V_{TN} = 2.71 - 1 = 1.71\,\text{V}$

Therefore,

$v_{CM}(\text{max}) = v_{O1} - V_{DS1}(\text{sat}) + V_{GS1} = 5.31 - 1.71 + 2.71$

or

$v_{CM}(\text{max}) = 6.31\,\text{V}$

The minimum common-mode input voltage is the value when M_4 reaches the transition point, or

$V_{DS4} = V_{DS4}(\text{sat}) = V_{GS4} - V_{TN} = 2.4 - 1 = 1.4\,\text{V}$

Therefore,

$v_{CM}(\text{min}) = V_{GS1} + V_{DS4}(\text{sat}) - 10 = 2.71 + 1.4 - 10$

or

$v_{CM}(\text{min}) = -5.89\,\text{V}$

Comment: For this circuit the maximum range for the common-mode input voltage is $-5.89 \le v_{CM} \le 6.31\,\text{V}$.

The dc transfer characteristics of the MOSFET differential pair can be determined from the circuit in Figure 11.19. Neglecting the output resistances of M_1 and M_2, and assuming the two transistors are matched, we can write

$$i_{D1} = K_n(v_{GS1} - V_{TN})^2 \qquad \textbf{(11.42(a))}$$

and

$$i_{D2} = K_n(v_{GS2} - V_{TN})^2 \qquad \textbf{(11.42(b))}$$

Taking the square roots of Equations (11.42(a)) and (11.42(b)), and subtracting the two equations, we obtain

$$\sqrt{i_{D1}} - \sqrt{i_{D2}} = \sqrt{K_n}\,(v_{GS1} - v_{GS2}) = \sqrt{K_n} \cdot v_d \qquad \textbf{(11.43)}$$

where $v_d = v_{G1} - v_{G2} = v_{GS1} - v_{GS2}$ is the differential-mode input voltage. If $v_d > 0$, then $v_{G1} > v_{G2}$ and $v_{GS1} > v_{GS2}$, which implies that $i_{D1} > i_{D2}$. Since

$$i_{D1} + i_{D2} = I_Q \qquad \textbf{(11.44)}$$

then Equation (11.43) becomes

$$\left(\sqrt{i_{D1}} - \sqrt{I_Q - i_{D1}}\right)^2 = \left(\sqrt{K_n} \cdot v_d\right)^2 = K_n v_d^2 \tag{11.45}$$

when both sides of the equation are squared. After the terms are rearranged, Equation (11.45) becomes

$$\sqrt{i_{D1}(I_Q - i_{D1})} = \frac{1}{2}(I_Q - K_n v_d^2) \tag{11.46}$$

If we square both sides of this equation, we develop the quadratic equation

$$i_{D1}^2 - I_Q i_{D1} + \frac{1}{4}(I_Q - K_n v_d^2)^2 = 0 \tag{11.47}$$

Applying the quadratic formula, rearranging terms, and noting that $i_{D1} > I_Q/2$ and $v_d > 0$, we obtain

$$i_{D1} = \frac{I_Q}{2} + \sqrt{\frac{K_n I_Q}{2}} \cdot v_d \sqrt{1 - \left(\frac{K_n}{2I_Q}\right) v_d^2} \tag{11.48}$$

Using Equation (11.44), we find that

$$i_{D2} = \frac{I_Q}{2} - \sqrt{\frac{K_n I_Q}{2}} \cdot v_d \sqrt{1 - \left(\frac{K_n}{2I_Q}\right) v_d^2} \tag{11.49}$$

The normalized drain currents are

$$\frac{i_{D1}}{I_Q} = \frac{1}{2} + \sqrt{\frac{K_n}{2I_Q}} \cdot v_d \sqrt{1 - \left(\frac{K_n}{2I_Q}\right) v_d^2} \tag{11.50}$$

and

$$\frac{i_{D2}}{I_Q} = \frac{1}{2} - \sqrt{\frac{K_n}{2I_Q}} \cdot v_d \sqrt{1 - \left(\frac{K_n}{2I_Q}\right) v_d^2} \tag{11.51}$$

These equations describe the dc transfer characteristics for this circuit. They are plotted in Figure 11.21 as a function of a normalized differential input voltage $v_d/\sqrt{(2I_Q/K_n)}$.

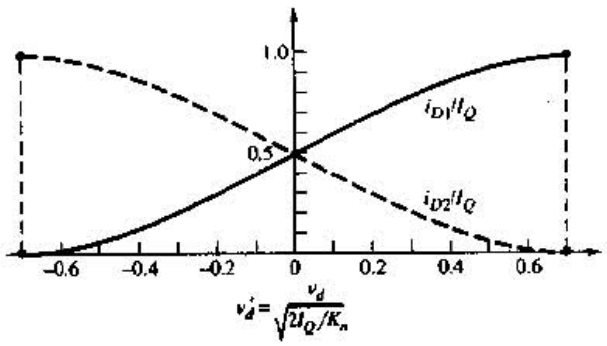


Figure 11.21 Normalized dc transfer characteristics, MOSFET differential amplifier

We can see from Equations (11.50) and (11.51) that, at a specific differential input voltage, bias current I_Q is switched entirely to one transistor or the other. This occurs when

$$|v_d|_{max} = \sqrt{\frac{I_Q}{K_n}} \tag{11.52}$$

The forward transconductance is defined as the slope of the dc transfer characteristic for the i_{D1} curve. From Figure 11.21, we see that the maximum slope, or maximum forward transconductance, occurs at $v_d = 0$, so that

$$g_f(\max) = \left.\frac{di_{D1}}{dv_d}\right|_{v_d = 0} \tag{11.53}$$

Using Equation (11.48), we find that

$$g_f(\max) = \sqrt{\frac{K_n I_Q}{2}} = \frac{g_m}{2} \tag{11.54}$$

where g_m is the transconductance of each transistor. The slope of the i_{D2} characteristic curve at $v_d = 0$ is the same, except it is negative.

We can perform an analysis similar to that in Example 11.2 to determine the maximum differential-mode input signal that can be applied and still maintain linearity. If we let $I_Q = 1\,\text{mA}$ and $K_n = 1\,\text{mA/V}^2$, then for differential input voltages less than 0.34 V, the difference between the linear approximation and the actual curve is less than 1 percent. The maximum differential input signal for the MOSFET diff-amp is much larger than for the bipolar diff-amp. The principal reason is that the gain of the MOSFET diff-amp, as we will see, is much smaller than the gain of the bipolar diff-amp.

Figure 11.22 is the ac equivalent circuit of the diff-amp configuration, showing only the differential voltage and signal currents as a function of the transistor transconductance g_m. We assume that the output resistance looking into the current source is infinite. Using this equivalent circuit, we find the one-sided output voltage at v_{o2}, as follows:

$$v_{o2} \equiv v_o = +\left(\frac{g_m v_d}{2}\right) R_D \tag{11.55}$$

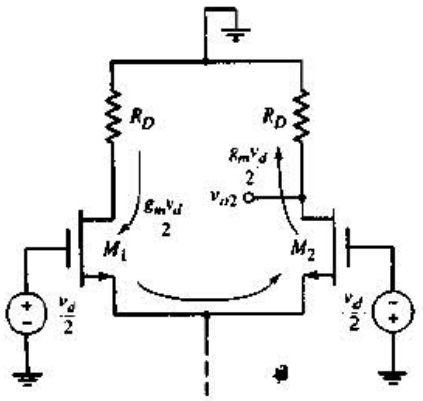


Figure 11.22 AC equivalent circuit, MOSFET differential amplifier

The differential voltage gain is then

$$A_d = \frac{v_o}{v_d} = \frac{g_m R_D}{2} = \sqrt{\frac{K_n I_Q}{2}} \cdot R_D \tag{11.56}$$

Example 11.11 **Objective:** Compare the forward transconductance of a MOSFET differential pair to that of a bipolar differential pair.

For the MOSFET differential pair, assume $K_n = 0.5\,\text{mA/V}^2$ and $I_Q = 1\,\text{mA}$. For the bipolar differential pair, assume $I_Q = 1\,\text{mA}$.

Solution: From Equation (11.54), the transconductance of the MOSFET in the differential pair is

$$g_m = 2\sqrt{\frac{K_n I_Q}{2}} = 2\sqrt{\frac{(0.5)(1)}{2}} = 1.0\,\text{mA/V}$$

From Equation (11.15), the transconductance of the bipolar transistor in the differential pair is

$$g_m = \frac{I_Q}{2V_T} = \frac{1}{2(0.026)} = 19.2\,\text{mA/V}$$

Comment: The transconductance of the bipolar pair is more than an order of magnitude larger than that of the MOSFET pair. Since the differential-mode voltage gain is directly proportional to the transconductance, the bipolar diff-amp gain is normally larger than the MOSFET diff-amp gain. We observed this same effect in Chapters 4 and 6, when we discussed the single-stage common-emitter and common-source circuits.

Test Your Understanding

11.12 Considering the dc transfer characteristics in Figure 11.21, determine the value of differential-mode input signal such that $i_{D1} = 0.90 I_Q$.

***11.13** For the differential amplifier in Figure 11.20, the parameters are: $V^+ = 5\,\text{V}$, $V^- = -5\,\text{V}$, $R_1 = 80\,\text{k}\Omega$, and $R_D = 40\,\text{k}$. The transistor parameters are $\lambda = 0$ and $V_{TN} = 0.8\,\text{V}$ for all transistors, and $K_{n3} = K_{n4} = 100\,\mu\text{A/V}^2$ and $K_{n1} = K_{n2} = 50\,\mu\text{A/V}^2$. Determine the range of the common-mode input voltage. (Ans. $-2.18 \le v_{cm} \le 3.76\,\text{V}$)

11.14 In the diff-amp in Figure 11.19, the transistor parameters are: $K_{n1} = 1\,\text{mA/V}^2$, $V_{TN} = 1\,\text{V}$, and $\lambda = 0$. The circuit is biased at $I_Q = 2\,\text{mA}$, and the drain resistors are $R_D = 5\,\text{k}\Omega$. Determine the maximum forward transconductance $g_f(\text{max})$ and the one-sided differential-mode voltage gain A_d. (Ans. $g_f(\text{max}) = 1\,\text{mA/V}$, $A_d = 5$)

11.3.2 Differential- and Common-Mode Input Impedances

At low frequencies, the input impedance of a MOSFET is essentially infinite, which means that both the differential- and common-mode input resistances of a MOSFET diff-amp are infinite. Also, we know that the differential input resistance of a bipolar pair can be in the low kilohm range. A design trade-off,

then, would be to use a MOSFET diff-amp with infinite input resistance, and sacrifice the differential-mode voltage gain.

11.3.3 Small-Signal Equivalent Circuit Analysis

We can determine the basic relationships for the differential-mode gain, common-mode gain, and common-mode rejection ratio from an analysis of the small-signal equivalent circuit.

Figure 11.23 shows the small-signal equivalent circuit of the MOSFET differential pair configuration. We assume the transistors are matched, with $\lambda = 0$ for each transistor, and that the constant-current source is represented by a finite output resistance R_o. All voltages are represented by their phasor components. The two transistors are biased at the same quiescent current, and $g_{m1} = g_{m2} \equiv g_m$.

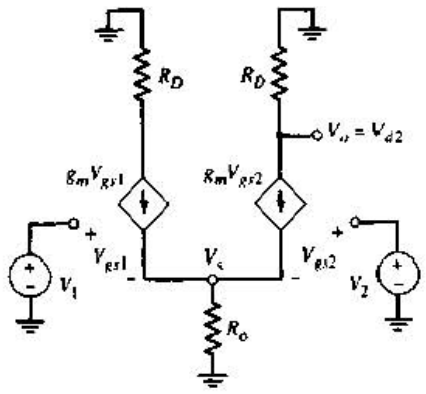


Figure 11.23 Small-signal equivalent circuit, MOSFET differential amplifier

Writing a KCL equation at node V_s, we have

$$g_m V_{gs1} + g_m V_{gs2} = \frac{V_s}{R_o} \tag{11.57}$$

From the circuit, we see that $V_{gs1} = V_1 - V_s$ and $V_{gs2} = V_2 - V_s$. Equation (11.57) then becomes

$$g_m(V_1 + V_2 - 2V_s) = \frac{V_s}{R_o} \tag{11.58}$$

Solving for V_s we obtain

$$V_s = \frac{V_1 + V_2}{2 + \dfrac{1}{g_m R_o}} \tag{11.59}$$

For a one-sided output at the drain of M_2, we have

$$V_o = V_{d2} = -(g_m V_{gs2})R_D = -(g_m R_D)(V_2 - V_s) \tag{11.60}$$

Substituting Equation (11.59) into (11.60) and rearranging terms yields

$$V_o = -g_m R_D \left[\frac{V_2\left(1 + \frac{1}{g_m R_o}\right) - V_1}{2 + \frac{1}{g_m R_o}} \right] \tag{11.61}$$

Based on the relationships between the input voltages V_1 and V_2 and the differential- and common-mode voltages, as given by Equation (11.29), Equation (11.61) can be written

$$V_o = \frac{g_m R_D}{2} V_d - \frac{g_m R_D}{1 + 2 g_m R_o} V_{cm} \tag{11.62}$$

The output voltage, in general form, is

$$V_o = A_d V_d + A_{cm} V_{cm} \tag{11.63}$$

The transconductance g_m of the MOSFET is

$$g_m = 2\sqrt{K_n I_{DQ}} = \sqrt{2 K_n I_Q}$$

Comparing Equations (11.62) and (11.63), we develop the relationships for the differential-mode gain,

$$A_d = \frac{g_m R_D}{2} = \sqrt{2 K_n I_Q}\left(\frac{R_D}{2}\right) = \sqrt{\frac{K_n I_Q}{2}} \cdot R_D \tag{11.64(a)}$$

and the common-mode gain

$$A_{cm} = \frac{-g_m R_D}{1 + 2 g_m R_o} = \frac{-\sqrt{2 K_n I_Q} \cdot R_D}{1 + 2\sqrt{2 K_n I_Q} \cdot R_o} \tag{11.64(b)}$$

We again, see that for an ideal current source, the common-mode gain is zero since $R_o = \infty$.

From Equations (11.64(a)) and (11.64(b)), the common-mode rejection ratio, CMRR $= |A_d / A_{cm}|$, is found to be

$$\text{CMRR} = \frac{1}{2}\left[1 + 2\sqrt{2 K_n I_Q} \cdot R_o\right] \tag{11.65}$$

This demonstrates that the CMRR for the MOSFET diff-amp is also a strong function of the output resistance of the constant-current source.

Example 11.12 **Objective:** Determine the differential-mode voltage gain, common-mode voltage gain, and CMRR for a MOSFET diff-amp.

Consider a MOSFET diff-amp with the configuration in Figure 11.20. Assume the same transistor parameters as given in Example 11.10 except assume $\lambda = 0.01\ \text{V}^{-1}$ for M_4.

Solution: From Example 11.10, we found the bias current to be $I_Q = 0.587\,\text{mA}$. The output resistance of the current source is then

$$R_o = \frac{1}{\lambda I_Q} = \frac{1}{(0.01)(0.587)} = 170\,\text{k}\Omega$$

The differential-mode voltage gain is

$$A_d = \sqrt{\frac{K_n I_Q}{2}} \cdot R_D = \sqrt{\frac{(1)(0.587)}{2}} \cdot (16) = 8.67$$

and the common-mode voltage gain is

$$A_{cm} = -\frac{\sqrt{2K_n I_Q} \cdot R_D}{1 + 2\sqrt{2K_n I_Q} \cdot R_o} = -\frac{\sqrt{2(1)(0.587)} \cdot (16)}{1 + 2\sqrt{2(1)(0.587)} \cdot (170)} = -0.0469$$

The common-mode rejection ratio is then

$$\text{CMRR}_{\text{dB}} = 20\log_{10}\left(\frac{8.67}{0.0469}\right) = 45.3\,\text{dB}$$

Comment: As mentioned earlier, the differential-mode voltage gain of the MOSFET diff-amp is considerably less than that of the bipolar diff-amp, since the value of the MOSFET transconductance is, in general, much smaller than that of the BJT.

The value of the common-mode rejection ratio can be increased by increasing the output resistance of the current source. An increase in the output resistance can be accomplished by using a more sophisticated current source circuit. Figure 11.24 shows a MOSFET cascode current mirror that was discussed in the last chapter. The output resistance, as given by Equation (10.57), is $R_o = r_{o4} + r_{o2}(1 + g_m r_{o4})$. For the parameters of Example 11.12, $r_{o2} = r_{o4} = 170\,\text{k}\Omega$ and $g_m = 2\sqrt{K_n I_Q} = 1.53\,\text{mA/V}$. Then

$$R_o = 170 + 170[1 + (1.53)(170)] \Rightarrow 44.6\,\text{M}\Omega$$

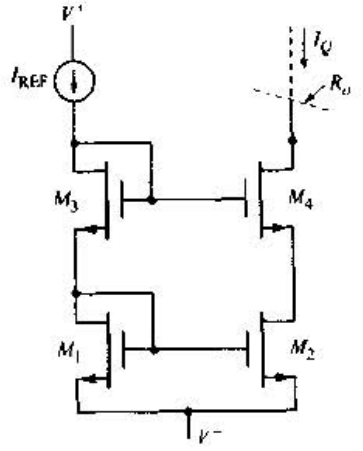


Figure 11.24 MOSFET cascode current source

Again, using the parameters of Example 11.12, the common-mode voltage gain of the diff-amp with a cascode current mirror would be

$$A_{cm} = -\frac{\sqrt{2K_n I_Q} \cdot R_D}{1 + 2\sqrt{2K_n I_Q} \cdot R_o} = -\frac{\sqrt{2(1)(0.587)} \cdot (16)}{1 + 2\sqrt{2(1)(0.587)} \cdot (44600)} = -0.000179$$

so that the CMRR would be

$$\text{CMRR}_{\text{dB}} = 20\log_{10}\left(\frac{8.67}{0.000179}\right) = 93.7\,\text{dB}$$

We increased the common-mode rejection ratio dramatically by using the cascode current mirror instead of the single two-transistor current source. Note, however, that the differential-mode voltage gain is unchanged.

To gain an appreciation of the difference in CMRR between 45.3 dB and 93.7 dB, we can reconsider the linear scale. For a $\text{CMRR}_{\text{dB}} = 45.3\,\text{dB}$, the differential gain is a factor of 185 times larger than the common-mode gain, while for a $\text{CMRR}_{\text{dB}} = 93.7\,\text{dB}$, the differential gain is a factor of 48,436 times larger than the common-mode gain.

Test Your Understanding

11.15 The diff-amp in Figure 11.19 has a differential gain of $A_d = 8$. The maximum current source available is $I_Q = 4\,\text{mA}$, and the maximum drain resistance is $R_D = 4\,\text{k}\Omega$. Determine the required $g_f(\text{max})$ and the transistor conductance K_n. (Ans. $g_f(\text{max}) = 2\,\text{mA/V}$, $K_n = 2\,\text{mA/V}^2$)

11.16 Consider the differential amplifier in Figure 11.20. The transistor parameters are given in Example 11.10, except that $\lambda = 0.02\,\text{V}^{-1}$ for M_3 and M_4. Determine the differential voltage gain $A_d = v_{o2}/v_d$, the common-mode gain $A_{cm} = v_{o2}/v_{cm}$, and the CMRR_{dB}. (Ans. $A_d = 2.74$, $A_{cm} = -0.0925$, $\text{CMRR}_{\text{dB}} = 29.4\,\text{dB}$)

11.17 The diff-amp in Figure 11.19 is biased at $I_Q = 0.2\,\text{mA}$ and the transistor conduction parameter for all transistors is $K_n = 100\,\mu\text{A/V}^2$. Determine the minimum output resistance of the current source such that $\text{CMRR}_{\text{dB}} = 60\,\text{dB}$. (Ans. $R_o \cong 5\,\text{M}\Omega$)

***RD11.18** The differential amplifier in Figure 11.20 is to be redesigned. The current-source biasing is to be replaced with the cascode current source in Figure 11.24. The reference current is $I_{\text{REF}} = 100\,\mu\text{A}$ and λ for transistors in the current source circuit is $0.01\,\text{V}^{-1}$. The parameters of the differential pair M_1 and M_2 are the same as described in Example 11.10. The range of the common-mode input voltage is to be $-4 \leq v_{cm} \leq +4\,\text{V}$. Redesign the diff-amp to achieve the highest possible differential-mode voltage gain. Determine the values of A_d, A_{cm}, and CMRR_{dB}.

11.3.4 JFET Differential Amplifier

Figure 11.25 shows a basic JFET differential pair biased with a constant-current source. If a pure differential-mode input signal is applied such that $v_{G1} = +v_d/2$ and $v_{G2} = -v_d/2$, then drain currents I_{D1} and I_{D2} increase and decrease, respectively, in exactly the same way as in the MOSFET diff-amp.

We can determine the differential-mode voltage gain by analyzing the small-signal equivalent circuit. Figure 11.26 shows the equivalent circuit, with the output resistance of the constant-current source and the small-signal resistances of Q_1 and Q_2 assumed to be infinite. The small-signal equivalent circuit of the JFET diff-amp is identical to that of the MOSFET diff-amp in Figure 11.23 for the case when the current-source output resistance is infinite. A KCL equation at the common-source node, in phasor notation, is

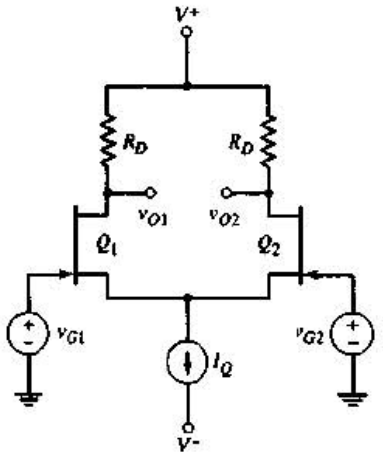


Figure 11.25 Basic JFET differential pair configuration

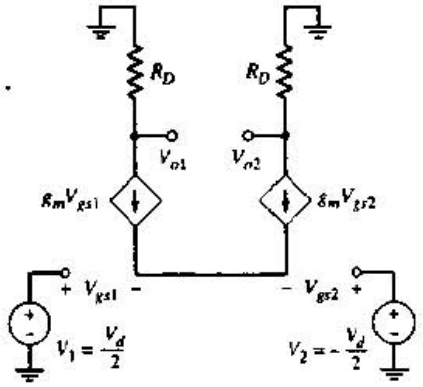


Figure 11.26 Small-signal equivalent circuit, JFET differential amplifier

$$g_m V_{gs1} + g_m V_{gs2} = 0 \tag{11.66(a)}$$

or

$$V_{gs1} = -V_{gs2} \tag{11.66(b)}$$

The differential-mode input voltage is

$$V_d \equiv V_1 - V_2 = V_{gs1} - V_{gs2} = -2V_{gs2} \tag{11.67}$$

A one-sided output at V_{o2} is given by

$$V_{o2} = -g_m V_{gs2} R_D = -g_m \left(\frac{-V_d}{2}\right) R_D \tag{11.68}$$

and the differential-mode voltage gain is

$$A_d = \frac{V_{o2}}{V_d} = +\frac{g_m R_D}{2} \tag{11.69}$$

The expression for the differential-mode voltage gain for the JFET diff-amp (Equation (11.69)) is exactly the same as that of the MOSFET diff-amp

(Equation 11.64(a)). If the constant-current source output resistance is finite, then the JFET diff-amp will also have a nonzero common-mode voltage gain.

11.4 DIFFERENTIAL AMPLIFIER WITH ACTIVE LOAD

In Chapter 10, we considered an active load in conjunction with a simple transistor amplifier. Active loads can also be used in diff-amp circuits to increase the differential-mode gain.

Active loads are essentially transistor current sources used in place of resistive loads. The transistors in the active load circuit are biased at a Q-point in the forward-active mode as shown in Figure 11.27. A change in collector current is induced by the differential-pair, which, in turn, produces a change in the emitter–collector voltage as shown in the figure. The relation between the change in current and change in voltage is proportional to the small-signal output resistance r_o of the transistor. The value of r_o is, in general, much larger than that of a discrete resistive load, so the small-signal voltage gain will be larger with the active load.

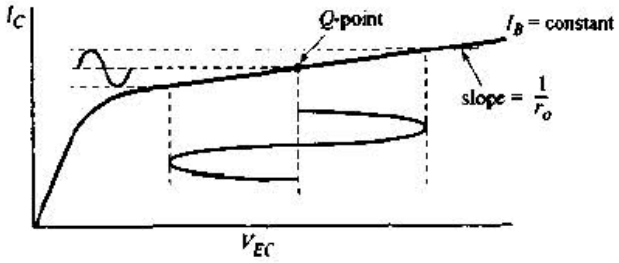


Figure 11.27 Current–voltage characteristic of active load device

11.4.1 BJT Diff-Amp with Active Load

Figure 11.28 shows a differential amplifier with an active load. Transistors Q_1 and Q_2 are the differential pair biased with a constant current I_Q, and transistors Q_3 and Q_4 form the load circuit. From the collectors of Q_2 and Q_4, we obtain a one-sided output.

If we assume all transistors are matched, then a pure applied common-mode voltage means that $v_{B1} = v_{B2} = v_{CM}$, and current I_Q splits evenly between Q_1 and Q_2. Neglecting base currents, $I_4 = I_3$ through the current-source circuit and $I_1 = I_2 = I_3 = I_4 = I_Q/2$ with no load connected at the output.

In actual diff-amp circuits, base currents are not zero. In addition, a second amplifier stage is connected at the diff-amp output. Figure 11.29 shows a diff-amp with an active load circuit, corresponding to a three-transistor current source, as well as a second amplifying stage. In general, the common–emitter current gain β is a function of collector current, as was shown in Figure 4.21(c). However, for simplicity, we assume all transistor current gains are equal, even though the current level in Q_5 is much smaller than in the other transistors. Current I_O is the dc bias current from the gain stage. Assuming all transistors are matched and $v_{B1} = v_{B2} = v_{CM}$, current I_Q splits evenly and $I_1 = I_2$. To

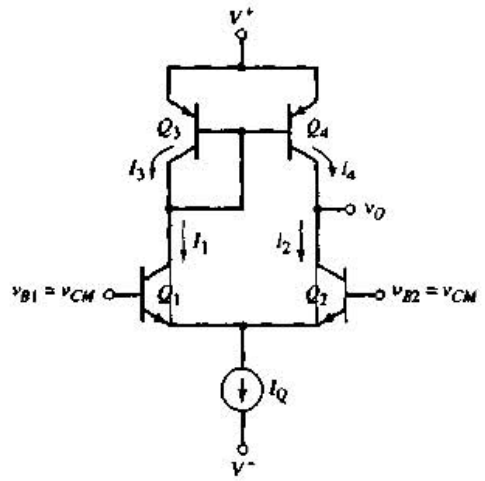


Figure 11.28 BJT differential amplifier with active load

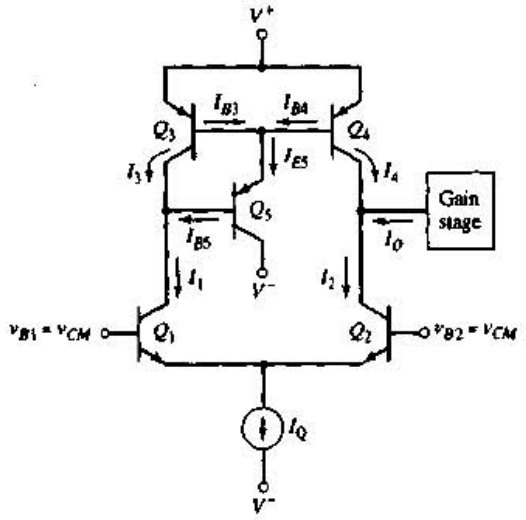


Figure 11.29 BJT differential amplifier with three-transistor active load and second gain stage

ensure that Q_2 and Q_4 are biased in the forward-active mode, the dc currents must be balanced, or $I_3 = I_4$. We see that

$$I_{E5} = I_{B3} + I_{B4} = \frac{I_3}{\beta} + \frac{I_4}{\beta} \tag{11.70}$$

Then

$$I_{B5} = \frac{I_{E5}}{1+\beta} = \frac{I_3 + I_4}{\beta(1+\beta)} \tag{11.71}$$

If the base currents and I_O are small, then

$$I_3 + I_4 \cong I_Q \tag{11.72}$$

Therefore,

$$I_{B5} \cong \frac{I_Q}{\beta(1+\beta)} \tag{11.73}$$

For the circuit to be balanced, that is, for $I_1 = I_2$ and $I_3 = I_4$, we must have

$$I_O = I_{B5} = \frac{I_O}{\beta(1+\beta)} \tag{11.74}$$

Equation (11.74) implies that the second amplifying stage must be designed and biased such that the direction of the dc bias current is as shown and is equal to the result of Equation (11.74). To illustrate this condition, we will analyze a second amplifying stage using a Darlington pair, later in this chapter.

11.4.2 Small-Signal Analysis of BJT Active Load

Figure 11.30 shows a diff-amp with a three-transistor active load circuit. The resistance R_L represents the small-signal input resistance of the gain stage. A pure differential-mode input voltage is applied as indicated. The signal voltage at the base of Q_1 produces a signal collector current $i_1 = (g_m v_d)/2$, where g_m is the transistor transconductance for both Q_1 and Q_2. Assuming the base currents are negligible, a signal current $i_3 = i_1$ is induced in Q_3, and the current mirror produces a signal current i_4 equal to i_3. The signal voltage at the base of Q_2 produces a signal collector current $i_2 = (g_m v_d)/2$, with the direction shown. The two signal currents, i_2 and i_4, add to produce a signal current in the load resistance R_L. The discussion is a first-order evaluation of the circuit operation.

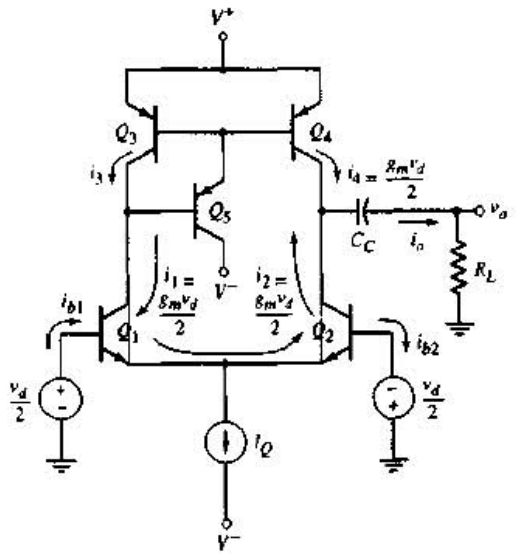


Figure 11.30 BJT differential amplifier with three-transistor active load, showing the signal currents

From the above discussion, we know the induced currents in Q_2 and Q_4. To more accurately determine the output voltage, we need to consider the equivalent small-signal collector–emitter output circuit of the two transistors.

Figure 11.31(a) shows the small-signal equivalent circuit at the collector nodes of Q_2 and Q_4. The circuit can be rearranged to combine the signal grounds at a common point, as in Figure 11.31(b). From this figure, we determine that

$$v_o = 2\left(\frac{g_m v_d}{2}\right)(r_{o2} \| r_{o4} \| R_L) \tag{11.75}$$

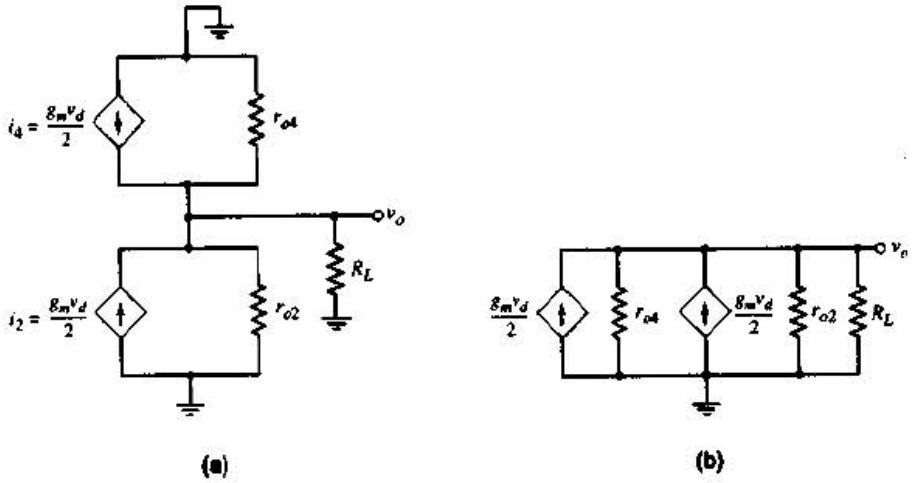


Figure 11.31 (a) Small-signal equivalent circuit BJT differential amplifier with active load and (b) rearrangement of small-signal equivalent circuit

and the small-signal differential-mode voltage gain is

$$A_d = \frac{v_o}{v_d} = g_m(r_{o2} \| r_{o4} \| R_L) \tag{11.76}$$

Equation (11.76) can be rewritten in the form

$$A_d = \frac{g_m}{\dfrac{1}{r_{o2}} + \dfrac{1}{r_{o4}} + \dfrac{1}{R_L}} = \frac{g_m}{g_{o2} + g_{o4} + G_L} \tag{11.77}$$

We recall that $g_m = I_Q/2V_T$, $r_{o2} = V_{A2}/I_2$, and $r_{o4} = V_{A4}/I_4$. The parameters g_{o2}, g_{o4}, and G_L are the corresponding conductances. Assuming $I_2 = I_4 = I_Q/2$, we can write Equation (11.77) in the form

$$A_d = \frac{\dfrac{I_Q}{2V_T}}{\dfrac{I_Q}{2V_{A2}} + \dfrac{I_Q}{2V_{A4}} + \dfrac{1}{R_L}} \tag{11.78}$$

This expression of the differential-mode voltage gain of the diff-amp with an active load is very similar to that obtained in the last chapter for a simple amplifier with an active load.

Example 11.13 **Objective:** Determine the differential-mode gain of a diff-amp with an active load, taking loading effects into account.

Consider the diff-amp in Figure 11.30, biased with $I_Q = 0.20\,\text{mA}$. Assume an Early voltage of $V_A = 100\,\text{V}$ for all transistors. Determine the open-circuit ($R_L = \infty$) differential-mode voltage gain, as well as the differential-mode voltage gain when $R_L = 100\,\text{k}\Omega$.

Solution: From Equation (11.78), the open-circuit voltage gain becomes

$$A_d = \frac{\dfrac{1}{V_T}}{\dfrac{1}{V_{A2}} + \dfrac{1}{V_{A4}}} = \frac{\dfrac{1}{0.026}}{\dfrac{1}{100} + \dfrac{1}{100}} = 1923$$

When $R_L = 100\,\text{k}\Omega$, the voltage gain is

$$A_d = \frac{\dfrac{0.02 \times 10^{-3}}{2(0.026)}}{\dfrac{0.20 \times 10^{-3}}{2(100)} + \dfrac{0.20 \times 10^{-3}}{2(100)} + \dfrac{1}{100 \times 10^3}}$$

which can be written

$$A_d = \frac{\dfrac{0.20}{2(0.026)}}{\dfrac{0.20}{2(100)} + \dfrac{0.20}{2(100)} + \dfrac{1}{100}} = \frac{3.85}{0.001 + 0.001 + 0.01} = 321$$

An inspection of this last equation shows that the external load factor, $1/R_L$, dominates the denominator term and thus has a tremendous influence on the gain.

Comment: The open-circuit differential-mode voltage gain, for a diff-amp with an active load, is large. However, a finite load resistance R_L causes severe loading effects, as shown in this example. A $100\,\text{k}\Omega$ load caused almost an order of magnitude decrease in the gain.

The output resistance looking back into the common collector node is $R_o = r_{o2} \| r_{o4}$. To minimize loading effects, we need $R_L > R_o$. However, since R_o is generally large for active loads, we may not be able to satisfy this condition. We can determine the severity of the loading effect by comparing R_L and R_o.

Test Your Understanding

11.19 Consider the diff-amp in Figure 11.29, with parameters: $V^+ = 10\,\text{V}$, $V^- = -10\,\text{V}$, and $I_Q = 0.5\,\text{mA}$. The transistor parameters are: $\beta = 180$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, and $V_A = 100\,\text{V}$. (a) Find I_O such that the circuit is balanced. (b) For the balanced condition, what are the values of V_{EC4} and V_{CE2}, for $v_1 = v_2 = 0$? (Ans. (a) $I_O = 15.3\,\text{nA}$ (b) $V_{EC4} = 0.7\,\text{V}$, $V_{CE2} = 10\,\text{V}$)

11.20 The diff-amp circuit in Figure 11.30 is biased at $I_Q = 0.5\,\text{mA}$. The transistor parameters are: $\beta = 150$, $V_{A1} = V_{A2} = 125\,\text{V}$, and $V_{A3} = V_{A4} = 85\,\text{V}$. (a) Determine the open-circuit ($R_L = \infty$) differential-mode voltage gain. (b) Find the differential-mode voltage gain when $R_L = 100\,\text{k}\Omega$. (c) Find the differential-mode input resistance. (d) Find

the output resistance looking back from the load R_L. (Ans. (a) $A_d = 1947$ (b) $A_d = 644$ (c) $R_{id} = 31.2\,\text{k}\Omega$ (d) $R_o = 202\,\text{k}\Omega$)

11.21 Consider the diff-amp in Figure 11.28, with parameters: $V^+ = 10\,\text{V}$, $V^- = -10\,\text{V}$, and $I_Q = 0.2\,\text{mA}$. The transistor parameters are: $\beta = 120$, $V_{BE}(\text{on}) = V_{EB}(\text{on}) = 0.6\,\text{V}$, $V_{A1} = V_{A2} = 120\,\text{V}$, and $V_{A3} = V_{A4} = 80\,\text{V}$. Assume the output impedance of the current source is $1\,\text{M}\Omega$. Determine the differential-mode gain. (Ans. $A_d = 1843$)

RD11.22 Redesign the circuit in Figure 11.30 using a Widlar current source and bias voltages of $\pm 5\,\text{V}$. The bias current I_Q is to be no less than $100\,\mu\text{A}$ and the total power dissipated in the circuit (including the current-source circuit) is to be no more than 10 mW. The diff-amp transistor parameters are the same as in Exercise 11.20. The circuit is to provide a minimum loading effect when a second stage with an input resistance of $R = 90\,\text{k}\Omega$ is connected to the diff-amp. Determine the differential-mode voltage gain for this circuit.

11.23 Consider the diff-amp in Figure 11.28, using the parameters described in Exercise 11.21. (a) For a differential-mode input signal, determine the output resistance R_o at the output terminal. (b) Determine the load resistance R_L that would reduce the differential-mode voltage gain to one-half the open-circuit value. (Ans. (a) $R_o = 0.48\,\text{M}\Omega$ (b) $R_L = 0.48\,\text{M}\Omega$)

11.4.3 MOSFET Differential Amplifier with Active Load

We can use an active load in conjunction with a MOSFET differential pair, as we did for the bipolar differential amplifier. Figure 11.32 shows a MOSFET diff-amp with an active load. Transistors M_1 and M_2 are n-channel devices and form the differential pair biased with I_Q. The load circuit consists of transistors M_3 and M_4, both p-channel devices, connected in a current mirror configuration. A one-sided output is taken from the common drains of M_2 and M_4. When a common-mode voltage of $v_1 = v_2 = v_{cm}$ is applied, the current I_Q splits

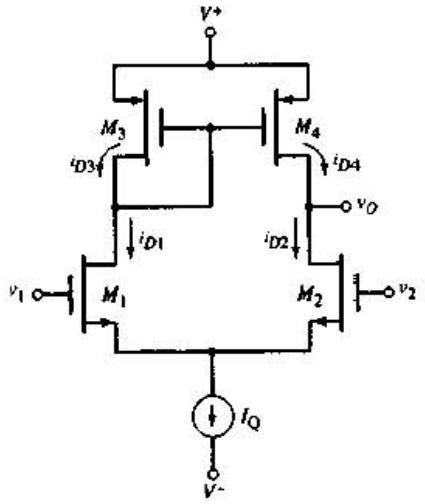


Figure 11.32 MOSFET differential amplifier with active load

evenly between M_1 and M_2, and $i_{D1} = i_{D2} = I_Q/2$. There are no gate currents; therefore, $i_{D3} = i_{D1}$ and $i_{D4} = i_{D2}$.

If a small differential-mode input voltage $v_d = v_1 - v_2$ is applied, then from Equation (11.48) and (11.49), we can write

$$i_{D1} = \frac{I_Q}{2} + i_d \tag{11.79(a)}$$

and

$$i_{D2} = \frac{I_Q}{2} - i_d \tag{11.79(b)}$$

where i_d is the signal current. For small values of v_d, we have $i_d = (g_m v_d)/2$. Since M_1 and M_3 are in series, we see that

$$i_{D3} = i_{D1} = \frac{I_Q}{2} + i_d \tag{11.80}$$

Finally, the current mirror consisting of M_3 and M_4 produces

$$i_{D4} = i_{D3} = \frac{I_Q}{2} + i_d \tag{11.81}$$

Figure 11.33 is the ac equivalent circuit of the diff-amp with active load, showing the signal currents. The negative sign for i_{D2} in Equation (11.79(b)) shows up as a change in current direction in M_2, as indicated in the figure.

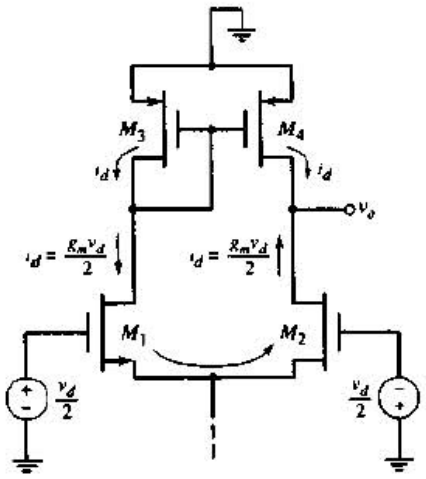


Figure 11.33 The ac equivalent circuit, MOSFET differential amplifier with active load

Figure 11.34(a) shows the small-signal equivalent circuit at the drain node of M_2 and M_4. If the output is connected to the gate of another MOSFET, which is equivalent to an infinite impedance at low frequency, the output terminal is effectively an open circuit. The circuit can be rearranged by combining the signal grounds at a common point, as shown in Figure 11.34(b). Then,

$$v_o = 2\left(\frac{g_m v_d}{2}\right)(r_{o2} \| r_{o4}) \tag{11.82}$$

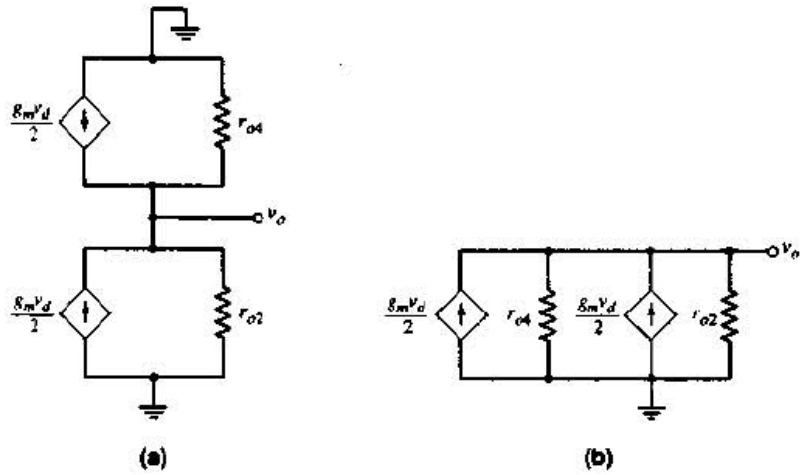


Figure 11.34 (a) Small-signal equivalent circuit, MOSFET differential amplifier with active load and (b) rearranged small-signal equivalent circuit

and the small-signal differential-mode voltage gain is

$$A_d = \frac{v_o}{v_d} = g_m(r_{o2} \| r_{o4}) \tag{11.83}$$

Equation (11.83) can be rewritten in the form

$$A_d = \frac{g_m}{\frac{1}{r_{o2}} + \frac{1}{r_{o4}}} = \frac{g_m}{g_{o2} + g_{o4}} \tag{11.84}$$

If we recall that $g_m = 2\sqrt{K_n I_D} = \sqrt{2K_n I_Q}$, $g_{o2} = \lambda_2 I_{DQ2} = (\lambda_2 I_Q)/2$, and $g_{o4} = \lambda_4 I_{DQ4} = (\lambda_4 I_Q)/2$, then Equation (11.84) becomes

$$A_d = \frac{2\sqrt{2K_n I_Q}}{I_Q(\lambda_2 + \lambda_4)} = 2\sqrt{\frac{2K_n}{I_Q}} \cdot \frac{1}{\lambda_2 + \lambda_4} \tag{11.85}$$

Design Example 11.14 **Objective:** Design a MOSFET diff-amp with the configuration in Figure 11.32 to meet the specifications of the experimental system in Example 11.4.

Design Approach: We need not only to try to obtain the necessary differential-mode gain and minimize the common-mode gain in our design, but we must also be cognizant of the swing in the output voltage. In the circuit in Figure 11.32, if the corresponding PMOS and NMOS transistors are matched, then the quiescent value of V_{SD4} is equal to $V_{SG4} = V_{SG3}$. As the signal output voltage increases, the source-to-drain voltage of M_4 decreases. The minimum value of this voltage such that M_4 remains biased in the saturation region is $V_{SD4}(\text{min}) = V_{SD4}(\text{sat}) = V_{SG} + V_{TP}$. This means that the maximum swing in the output voltage is equal to the magnitude of the threshold voltage of M_4. In this example, the maximum swing in the output voltage is 0.8 V, so that the magnitude of the threshold voltages of the PMOS devices must be greater than 0.8 V. Assume that NMOS devices are available with the following parameters: $V_{TN} = 0.5$ V, $k_n' = 80\,\mu\text{A/V}^2$, and $\lambda_n = 0.02\,\text{V}^{-1}$. Assume that PMOS devices are available with the

following parameters: $V_{TP} = -1.0\,\text{V}$, $k_p' = 40\,\mu\text{A/V}^2$, and $\lambda_p = 0.02\,\text{V}^{-1}$. Choose supply voltages of $\pm 5\,\text{V}$ and choose a bias current of approximately $I_Q = 200\,\mu\text{A}$.

Figure 11.35 is the diff-amp and current-source network used for the design in this example.

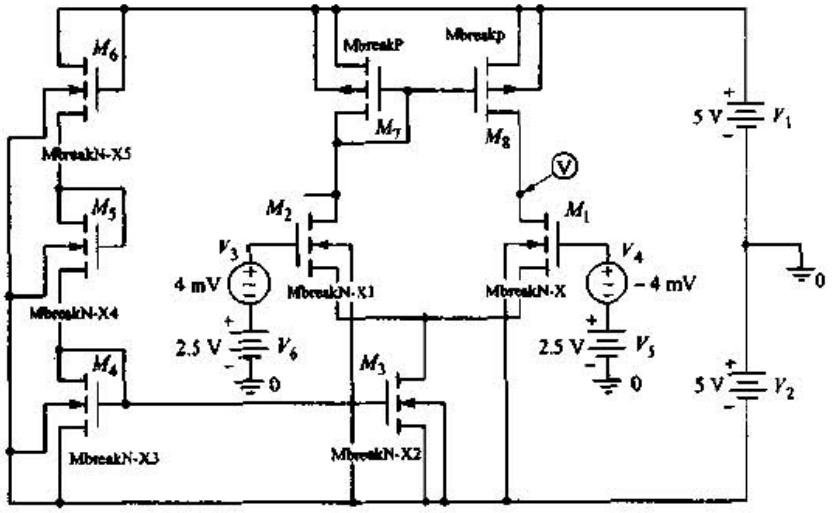


Figure 11.35 CMOS differential amplifier and current source network for Example 11.14

Design, Differential Amplifier: Differential-Mode Gain: From Equation (11.85), the differential-mode gain is

$$A_d = 2\sqrt{2\left(\frac{k_n'}{2}\right)\left(\frac{W}{L}\right)_n \frac{1}{I_Q}} \cdot \frac{1}{\lambda_n + \lambda_p}$$

or

$$100 = 2\sqrt{2\left(\frac{80}{2}\right)\left(\frac{W}{L}\right)\frac{1}{200}} \cdot \frac{1}{0.02 + 0.02}$$

which yields a width-to-length ratio of $(W/L)_n = 20$ for the NMOS differential pair. Since the width-to-length ratios of the other transistors do not directly affect the gain of the diff-amp, we may arbitrarily choose width-to-length ratios of 10 for all other transistors except M_5 and M_6. The W/L ratio of 10 means that the other devices are reasonably small and do not lead to a large circuit area.

Design, Current-Source Network: For the transistor M_3 in the current source, we have

$$I_Q = \frac{k'}{2} \cdot \frac{W}{L} \cdot (V_{GS3} - V_{TN})^2$$

or

$$200 = \frac{80}{2}(10)(V_{GS3} - 0.5)^2$$

which means that the required gate-to-source voltage of M_3 is $V_{GS3} = 1.21\,\text{V}$. We may choose M_4 and M_3 to be identical so that the current in the reference portion of the

circuit is also 200 μA. Assuming that M_5 and M_6 are identical, then each transistor must have a gate-to-source voltage of

$$V_{GS5} = V_{GS6} = (10 - 1.21)/2 \cong 4.4\,\text{V}$$

The width-to-length of these transistors is now found from

$$I_{REF} = I_Q = \frac{k_n'}{2} \cdot \left(\frac{W}{L}\right)_5 (V_{GS5} - V_{TN})^2$$

or

$$200 = \frac{80}{2} \cdot \left(\frac{W}{L}\right)_5 (4.4 - 0.5)^2$$

which yields

$$(W/L)_5 = (W/L)_6 = 0.33$$

Computer Simulation Verification: The circuit in Figure 11.35 was used in the computer simulation verification. In the hand design, the finite output resistance (lambda parameter) was neglected in the dc calculations. These parameters became important in the actual design and in the actual currents developed in the circuit. For $(W/L)_5 = (W/L)_6 = 0.75$, the reference current is $I_{REF} = 231\,\mu\text{A}$ and the bias current is $I_Q = 208\,\mu\text{A}$.

The differential-mode voltage gain is approximately 102 so that the signal output voltage is 0.82 V for a differential-mode input signal voltage of 8 mV. The common-mode output signal is approximately 0.86 mV, which is well within the specified 10 mV maximum value.

Design Pointer: The body effect has been neglected in this design. In actual integrated circuits, the differential pair transistors may actually be fabricated within their own p-type substrate region (for NMOS devices). This p-type substrate region is then directly connected to the source terminals so that the body effect in the NMOS differential pair devices can be neglected.

11.4.4 MOSFET Diff-Amp with Cascode Active Load

The differential-mode voltage gain is proportional to the output resistance looking into the active load transistor. The voltage gain can be increased, therefore, if the output resistance can be increased. An increase in output resistance can be achieved by using, for example, a cascode active load. This configuration is shown in Figure 11.36.

The output resistance R_o was considered in the last section in the discussion of the cascode current source. As applied to Figure 11.36, the output resistance is given by

$$R_o = r_{o4} + r_{o6}(1 + g_m r_{o4}) \cong g_m r_{o4} r_{o6} \qquad (11.86)$$

The small-signal differential-mode voltage gain is then

$$A_d = \frac{v_o}{v_d} = g_m(r_{o2} \| R_o) \tag{11.87}$$

Example 11.15 **Objective:** Calculate the differential-mode voltage gain of a MOSFET diff-amp with a cascode active load.

Consider the diff-amp shown in Figure 11.36. Assume the circuit and transistor parameters are the same as in Example 11.14.

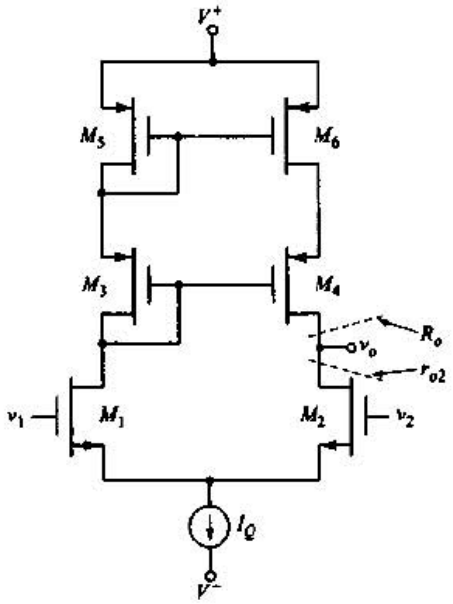


Figure 11.36 MOSFET diff-amp with cascode active load

Solution: The transistor transconductance is

$$g_m = 2\sqrt{K_n I_{DQ}} = 2\sqrt{(0.2)(0.1)} = 0.283\,\text{mA/V}$$

The output resistance of the individual transistors is

$$r_o = \frac{1}{\lambda I_{DQ}} = \frac{1}{(0.01)(0.1)} = 1000\,\text{k}\Omega = 1\,\text{M}\Omega$$

The output resistance of the cascode active load is then

$$R_o = r_{o4} + r_{o6}(1 + g_m r_{o4}) = 1 + (1)[1 + (0.283)(1000)] = 285\,\text{M}\Omega$$

The differential-mode voltage gain is then found as

$$A_d = g_m(r_{o2} \| R_o) = (0.283)(1000 \| 285000) = 282$$

Comment: Since $R_o \gg r_{o2}$, the voltage gain is now essentially equal to $A_d = g_m r_{o2}$ which is twice as large as the gain calculated in Example 11.14.

The differential-mode voltage gain can be further increased by incorporating a cascode configuration in the differential pair as well as in the active load. One such example is shown in Figure 11.37. Transistors M_3 and M_4 are the cascode transistors for the differential pair M_1 and M_2. The differential-mode voltage gain is now

$$A_d = \frac{v_o}{v_d} = g_m(R_{o4} \| R_{o6})$$

where $R_{o4} \cong g_m r_{o2} r_{o4}$ and $R_{o6} \cong g_m r_{o6} r_{o8}$. The small-signal differential-mode voltage gain of this type of amplifier can be on the order of 10,000.

Other types of MOSFET differential amplifiers will be considered in Chapter 13 when operational amplifier circuits are discussed.

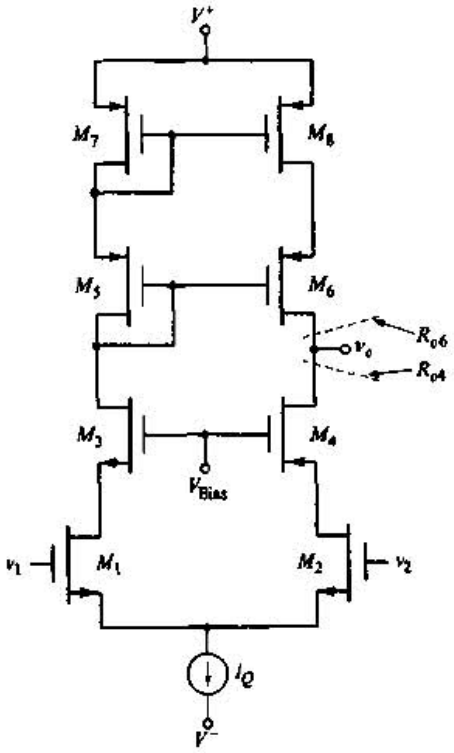


Figure 11.37 A MOSFET cascode diff-amp with a cascode active load

Test Your Understanding

11.24 A differential amplifier is shown in Figure 11.32. The parameters are: $V^+ = 10\,\text{V}$, $V^- = -10\,\text{V}$, and $I_Q = 0.1\,\text{mA}$. The PMOS parameters are: $K_p = 80\,\mu\text{A/V}^2$, $\lambda_p = 0.015\,\text{V}^{-1}$, and $V_{TP} = -1\,\text{V}$. The NMOS parameters are: $K_n = 100\,\mu\text{A/V}^2$, $\lambda_n = 0.01\,\text{V}^{-1}$, and $V_{TN} = 1\,\text{V}$. Determine the differential-mode voltage gain $A_d = v_o/v_d$. (Ans. $A_d = 113$)

11.5 BiCMOS CIRCUITS

Thus far, we have considered two basic amplifier design technologies: the bipolar technology, which uses npn and pnp bipolar junction transistors; and the MOS technology, which uses NMOS and PMOS field-effect transistors. We showed that bipolar transistors have a larger transconductance than MOSFETs biased at the same current levels, and that, in general, bipolar amplifiers have larger voltage gains. We also showed that MOSFET circuits have an essentially infinite imput impedance at low frequencies, which implies a zero input bias current.

These advantages of the two technologies can be exploited by combining bipolar and MOS transistors in the same integrated circuit. The technology is called **BiCMOS**. BiCMOS technology is especially useful in digital circuit design, but also has applications in analog circuits. In this section, we will examine basic BiCMOS analog circuit configurations.

11.5.1 Basic Amplifier Stages

A bipolar multitransistor circuit previously studied is the Darlington pair configuration. Figure 11.38(a) shows a modified Darlington pair configuration, in which the bias current I_{BIAS}, or some equivalent element, is used to control the quiescent current in Q_1. This Darlington pair circuit is used to boost the effective current gain of bipolar transistors. There is no comparable configuration in FET circuits.

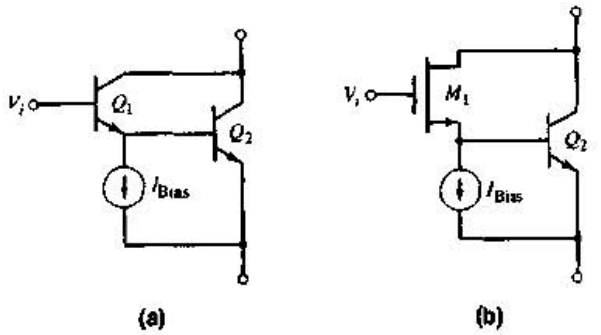


Figure 11.38 (a) Bipolar Darlington pair configuration and (b) BiCMOS Darlington pair configuration

A potentially useful BiCMOS circuit is shown in Figure 11.38(b). Transistor Q_1 in the Darlington pair is replaced with a MOSFET. The advantages of this configuration are an infinite input resistance, and a large transconductance due to the bipolar transistor Q_2.

To analyze the circuit, we consider the small-signal equivalent circuit shown in Figure 11.39. We assume that $r_o = \infty$ in both transistors.

The output signal current is

$$I_o = g_{m1} V_{gs} + g_{m2} V_\pi \tag{11.88}$$

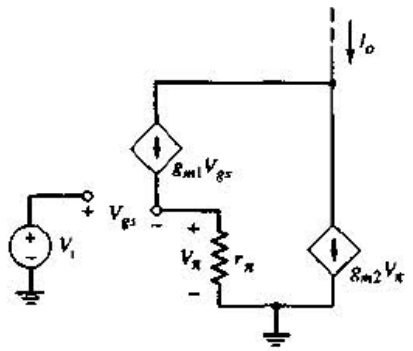


Figure 11.39 Small-signal equivalent circuit, BiCMOS Darlington pair configuration

We see that

$$V_i = V_{gs} + V_\pi \tag{11.89}$$

and

$$V_\pi = g_{m1} V_{gs} r_\pi \tag{11.90}$$

Combining Equations (11.89) and (11.90) produces

$$V_{gs} = \frac{V_i}{1 + g_{m1} r_\pi} \tag{11.91}$$

From Equation (11.88), the output current can now be written

$$I_o = g_{m1} V_{gs} + g_{m2}(g_{m1} r_\pi) V_{gs} = (g_{m1} + g_{m2} g_{m1} r_\pi) V_{gs} \tag{11.92}$$

Substituting Equation (11.91) into (11.92), we obtain

$$I_o = \frac{g_{m1}(1 + g_{m2} r_\pi)}{(1 + g_{m1} r_\pi)} \cdot V_i = g_m^c \cdot V_i \tag{11.93}$$

where g_m^c is the **composite transconductance**. Since g_{m2} of the bipolar transistor is usually at least an order of magnitude greater than g_{m1} of the MOSFET, the composite transconductance is approximately an order of magnitude larger than that of the MOSFET alone. We now have the advantages of a large transconductance and an infinite input resistance.

A bipolar cascode circuit is shown in Figure 11.40(a); a corresponding BiCMOS configuration is shown in Figure 11.40(b). The output resistance of

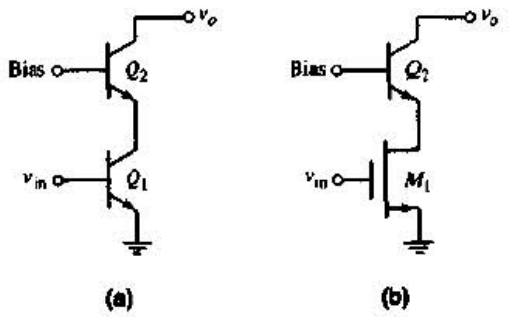


Figure 11.40 (a) Bipolar cascode configuration and (b) BiCMOS cascode configuration

the cascode circuit is very high, as we saw in Chapter 10. Also, the cascode amplifier has a wider frequency bandwidth than the common-emitter circuit, since the input resistance looking into the emitter of Q_2 is very low, thereby minimizing the Miller multiplication effect. This effect was observed in Chapter 7.

Again, the advantage of the BiCMOS circuit is the infinite input resistance of M_1. The equivalent resistance looking into the emitter of a bipolar transistor is much less than the resistance looking into the source of a MOSFET; therefore, the frequency response of a BiCMOS cascode circuit is superior to that of an all-MOSFET cascode circuit.

11.5.2 Current Sources

In our previous discussions of constant-current sources, we mentioned that cascode current sources increase the output resistance, as well as the stability of the bias current. Figure 11.41 shows a bipolar cascode configuration in which the output resistance is $R_o \cong \beta r_{o4}$. The bias current in this circuit is much more stable against variations in output voltage than the basic two-transistor current source.

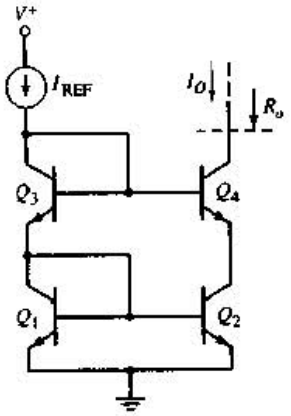


Figure 11.41 Bipolar cascode constant-current source

A BiCMOS double cascode constant-current source is shown in Figure 11.42. The small-signal equivalent circuit for determining output resistance is shown in Figure 11.43(a). The gate voltage to M_6 and the base voltages to Q_2 and Q_4 are constants, equivalent to signal ground. Also, since $V_{\pi 2} = 0$, then $g_{m6}V_{\pi 2} = 0$, and the equivalent circuit can be rearranged as shown in Figure 11.43(b).

The output resistance of this circuit is extremely large. A detailed analysis shows that the output resistance is given approximately by

$$R_o \cong (g_{m6}r_{o6})(\beta r_{o4}) \tag{11.94}$$

The output resistance is increased by a factor $(g_m r_{o6})$ compared to the bipolar cascode circuit in Figure 11.41. If a bipolar transistor were to be used in place of M_6, then a resistance $r_{\pi 6}$ would be connected across the terminals indicated by V_{gs6}. This resistance would effectively eliminate the multiplying constant $(g_{m6}r_{o6})$, and the output resistance would be essentially the same as that of the circuit in Figure 11.41. The BiCMOS circuit, then, increases the output resistance compared to an all-bipolar circuit.

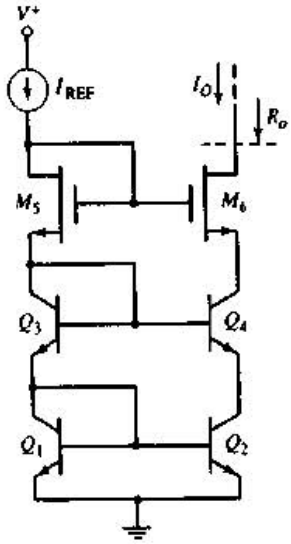


Figure 11.42 BiCMOS double cascode constant-current source

11.5.3 BiCMOS Differential Amplifier

A basic BiCMOS differential amplifier, with a constant-current source bias and a bipolar active load, is shown in Figure 11.44. Again, the primary advantages are the infinite input resistance and the zero input bias current. One disadvantage of a MOSFET input stage is a relatively high offset voltage compared to that of a bipolar input circuit. Offset voltages occur when the differential-pair input transistors are mismatched. In Chapter 14, we will examine the effect of offset voltages, as well as nonzero bias currents, in op-amp circuits.

We will consider additional BiCMOS op-amp circuits in Chapter 13, when we discuss the analysis and design of full op-amp circuits.

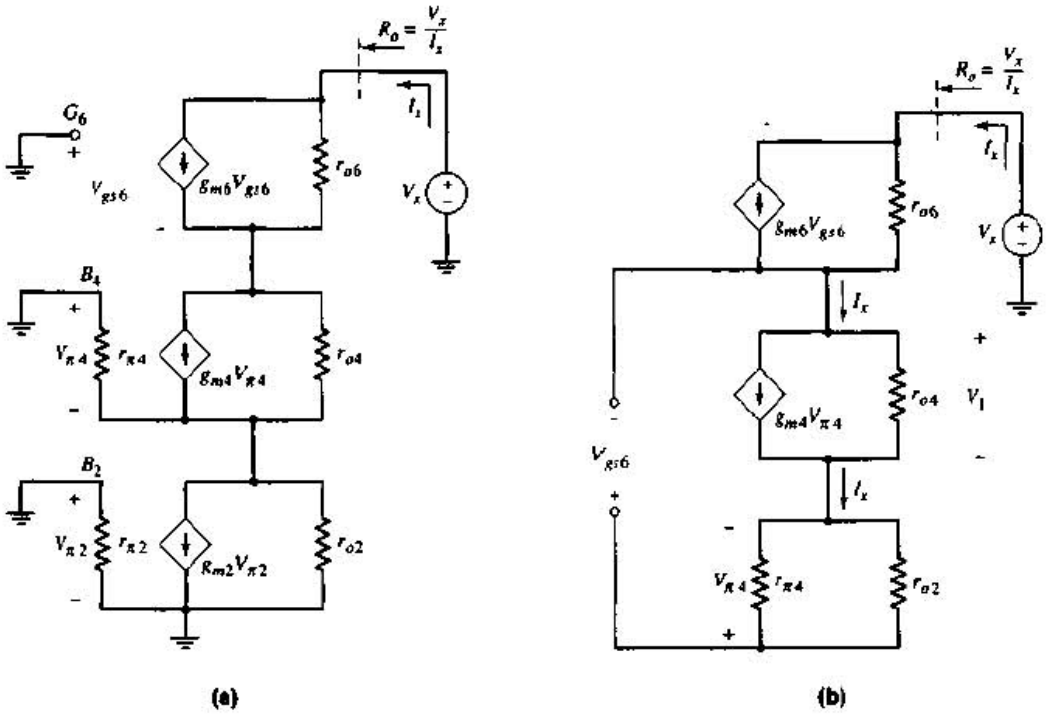


Figure 11.43 (a) Equivalent circuit for determining output impedance of BiCMOS double cascode current source and (b) rearranged equivalent circuit

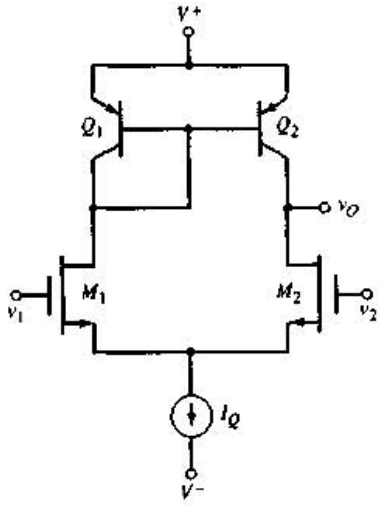


Figure 11.44 Basic BiCMOS differential amplifier

Test Your Understanding

11.25 Consider the BiCMOS Darlington pair in Figure 11.45. The transistor parameters are $K_n = 20\,\mu A/V^2$, $V_{TN} = 1\,V$, and $\lambda = 0$ for M_1 and $\beta = 100$, $V_{BE}(on) = 0.7\,V$, and $V_A = \infty$ for Q_2. Determine the small-signal parameters for each transistor, as well as the composite transconductance. (Ans. $g_{m1} = 44.8\,\mu A/V$, $g_{m2} = 2.88\,mA/V$, $r_{\pi 2} = 34.7\,k\Omega$, $r_{o1} = r_{o2} = \infty$, $g_m^c = 1.77\,mA/V$)

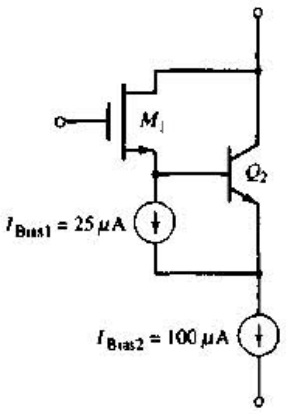


Figure 11.45 Figure for Exercise 11.25

11.26 The reference current in each of the constant-current source circuits shown in Figures 11.41 and 11.42 is $I_{REF} = 0.5\,mA$. All bipolar transistor parameters are $\beta = 150$ and $V_A = 80\,V$, and all MOSFET parameters are: $K_n = 500\,\mu A/V^2$, $V_{TN} = 1\,V$, and $\lambda = 0.0125\,V^{-1}$. Neglecting bipolar base currents, determine the output resistance R_o of each constant-current source. (Ans. For Figure 11.41, $R_o \cong 24\,M\Omega$; for Figure 11.42, $R_o = 3840\,M\Omega$)

11.6 GAIN STAGE AND SIMPLE OUTPUT STAGE

A diff-amp, including those previously discussed, is the input stage of virtually all op-amps. The second op-amp stage, or gain stage, is often a Darlington pair configuration, and the third, or output, stage is normally an emitter follower.

11.6.1 Darlington Pair and Simple Emitter-Follower Output

Figure 11.46 shows a BJT diff-amp with a three-transistor active load, a Darlington pair connected to the diff-amp output, and a simple emitter-follower output stage.

The differential-pair transistors are biased with a Widlar current source at a bias current I_Q. We noted previously that, for the diff-amp dc currents to be balanced, we must have

$$I_O = I_{B5} = \frac{I_Q}{\beta(1+\beta)} \tag{11.95}$$

From the figure, we see that

$$I_O = \frac{I_{E6}}{(1+\beta)} = \frac{I_{C7}}{\beta(1+\beta)} \tag{11.96}$$

In order for $I_O = I_{B5}$, we must require that $I_{C7} = I_Q$. This means that the emitter resistors of Q_{10} and Q_{11} should have the same value. Transistor Q_{11} also acts as an active load for the Darlington pair gain stage.

Transistor Q_8 and resistor R_4 form the simple emitter-follower output stage. The emitter-follower amplifier minimizes loading effects because its output resistance is small.

Ideally, when the diff-amp input is a pure common-mode signal, the output v_o is zero. The combination of Q_7 and Q_{11} allows the dc level to shift. By slightly changing the bias current I_{C7}, we can vary voltages V_{EC7} and V_{CE11} such that $v_o = 0$. The small variation of I_{C7} required to achieve the necessary dc

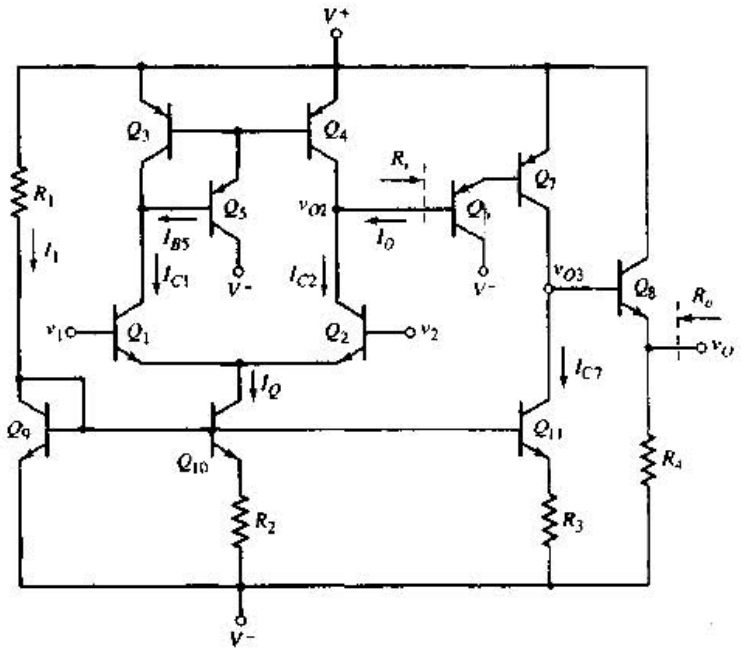


Figure 11.46 BJT diff-amp with three-transistor active load, Darlington pair gain stage, and simple emitter-follower output stage

level shift will not significantly change the balance between I_Q and I_{B5}. As we will see in later chapters, other forms of level shifters could also be used.

11.6.2 Input Impedance, Voltage Gain, and Output Impedance

The input resistance of the Darlington pair determines the loading effect on the basic diff-amp. In addition, the gain of the Darlington pair affects the overall gain of the op-amp circuit, and the output resistance of the emitter follower determines any loading effects on the output signal.

Figure 11.47(a) is the ac equivalent circuit of the Darlington pair, where R_{L7} is the effective resistance connected between the collector of Q_7 and signal

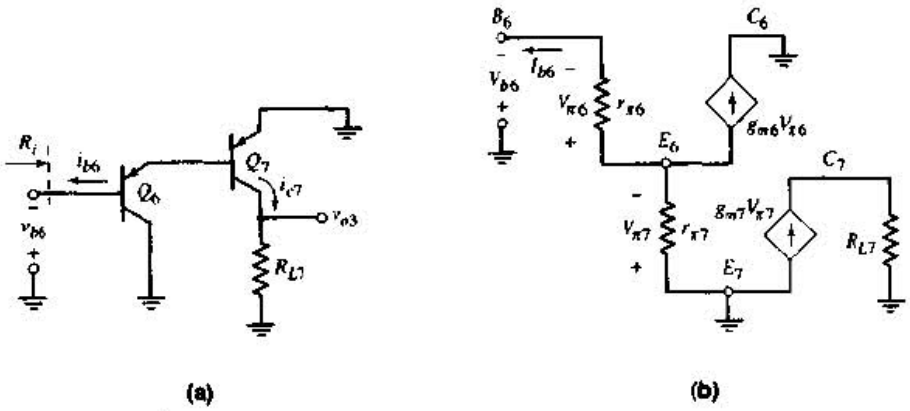


Figure 11.47 (a) The ac equivalent circuit, Darlington pair, and (b) small-signal equivalent circuit, Darlington pair

ground. Figure 11.47(b) shows the simple hybrid-π model of the Darlington pair. We see that the equivalent circuits for Q_6 and Q_7 have been effectively turned upside down compared to the transistors in Figure 11.47(a).

Writing a KVL equation around the B–E loop of Q_6 and Q_7, we have

$$V_{b6} = V_{\pi 6} + V_{\pi 7} \tag{11.97}$$

We can also write that

$$V_{\pi 6} = I_{b6} r_{\pi 6} \tag{11.98}$$

and the KCL equation is

$$\frac{V_{\pi 7}}{r_{\pi 7}} = \frac{V_{\pi 6}}{r_{\pi 6}} + g_{m6} V_{\pi 6} \tag{11.99(a)}$$

or

$$V_{\pi 7} = r_{\pi 7}\left[\frac{(1+\beta)}{r_{\pi 6}}\right] V_{\pi 6} = r_{\pi 7}(1+\beta) I_{b6} \tag{11.99(b)}$$

where $r_{\pi 6} g_{m6} = \beta$. Substituting Equations (11.99(b)) and (11.98) into Equation (11.97), we obtain

$$V_{b6} = I_{b6} r_{\pi 6} + r_{\pi 7}(1+\beta) I_{b6} \tag{11.100}$$

The input resistance is therefore

$$R_i = \frac{V_{b6}}{I_{b6}} = r_{\pi 6} + r_{\pi 7}(1+\beta) \tag{11.101}$$

Assuming $I_{C7} = I_Q$, the hybrid-π parameters are

$$r_{\pi 7} = \frac{\beta V_T}{I_{C7}} = \frac{\beta V_T}{I_Q} \tag{11.102(a)}$$

and

$$r_{\pi 6} = \frac{\beta V_T}{I_{C6}} = \frac{(1+\beta)\beta V_T}{I_Q} \tag{11.102(b)}$$

Combining Equations (11.102(a)), (11.102(b)), and Equation (11.101) yields an expression for the input resistance, as follows:

$$R_i = \frac{(1+\beta)\beta V_T}{I_Q} + \frac{(1+\beta)\beta V_T}{I_Q} = \frac{2(1+\beta)\beta V_T}{I_Q} \tag{11.103}$$

We can determine the small-signal voltage gain of the Darlington pair circuit by using the small-signal equivalent circuit in Figure 11.47(b). We see that

$$v_{o3} = i_{c7} R_{L7} = (\beta i_{b7}) R_{L7} = \beta(1+\beta) i_{b6} R_{L7} \tag{11.104}$$

and

$$i_{b6} = \frac{v_{b6}}{R_i} \tag{11.105}$$

The small-signal voltage gain is therefore

$$A_v = \frac{v_{o3}}{v_{b6}} = \frac{\beta(1+\beta) R_{L7}}{R_i} \tag{11.106}$$

Substituting Equation (11.103) into (11.106), we find that

$$A_v = \frac{\beta(1+\beta)R_{L7}}{\dfrac{2(1+\beta)\beta V_T}{I_Q}} = \left(\frac{I_Q}{2V_T}\right)R_{L7} \tag{11.107}$$

In Figure 11.46, we see that resistance R_{L7} is the parallel combination of the resistance looking into the collector of Q_{11} and the resistance looking into the base of Q_8. From Chapter 10, the resistance looking into the collector of Q_{11} is

$$R_{c11} = r_{o11}(1 + g_{m11}R'_E) \tag{11.108}$$

where $R'_E = r_{\pi 11} \| R_3$. The resistance looking into the base of Q_8 is

$$R_{b8} = r_{\pi 8} + (1+\beta)R_4 \tag{11.109}$$

Equations (11.108) and (11.109) indicate that resistances R_{c11} and R_{b8} are large, which means that the effective resistance R_{L7} is also large.

Example 11.16 **Objective:** Calculate the input resistance and the small-signal voltage gain of a Darlington pair.

Consider the circuit shown in Figure 11.46, with parameters $I_{C7} = I_Q = 0.2\,\text{mA}$, $I_{C8} = 1\,\text{mA}$, $R_4 = 10\,\text{k}\Omega$, and $R_3 = 0.2\,\text{k}\Omega$. Assume $\beta = 100$ for all transistors, and the Early voltage for Q_{11} is 100 V.

Solution: The input resistance, given by Equation (11.103), is

$$R_i = \frac{2(1+\beta)\beta V_T}{I_Q} = \frac{2(101)(100)(0.026)}{0.2} \Rightarrow 2.63\,\text{M}\Omega$$

The small-signal voltage gain is a function of R_{L7}, which in turn is a function of R_{c11} and R_{b8}. We can find that

$$R_{\pi 11} = \beta V_T / I_Q = (100)(0.026)/0.2 = 13\,\text{k}\Omega$$

such that

$$R'_E = 13 \| 0.2 = 0.197\,\text{k}\Omega$$

Also

$$g_{m11} = I_Q / V_T = 0.2/0.026 = 7.69\,\text{mA/V}$$

and

$$r_{o11} = V_A / I_Q = 100/0.2 = 500\,\text{k}\Omega$$

Therefore,

$$R_{c11} = r_{o11}(1 + g_{m11}R'_E) = 500[1 + (7.69)(0.197)] \Rightarrow 1.26\,\text{M}\Omega$$

We can determine that

$$r_{\pi 8} = \beta V_T / I_{C8} = (100)(0.026)/1 = 2.6\,\text{k}\Omega$$

Then

$$R_{b8} = r_{\pi 8} + (1+\beta)R_4 = 2.6 + (101)(10) \Rightarrow 2.02\,\text{M}\Omega$$

Consequently, resistance R_{L7} is

$$R_{L7} = R_{c11} \| R_{b8} = 1.26 \| 2.02 = 0.776\,\text{M}\Omega$$

Finally, from Equation (11.107), the small-signal voltage gain is

$$A_v = \left(\frac{I_Q}{2V_T}\right)R_{L7} = \left[\frac{0.2}{2(0.026)}\right](776) = 2985$$

Comment: The input resistance of the Darlington pair is in the megohm range, which should minimize severe loading effects on the diff-amp. In addition, the small-signal gain is large because of the active load (Q_{11}) and the large input resistance of the emitter-follower output stage.

We can use the results of Chapter 4 to determine the output resistance of the emitter follower. The output resistance is

$$R_o = R_4 \left\| \left(\frac{r_{\pi 8} + Z}{(1+\beta)}\right) \right. \tag{11.110}$$

where Z is the equivalent impedance, or resistance, in the base of Q_8. In this case, $Z = R_{c11} \| R_{c7}$, where R_{c7} is the resistance looking into the collector of Q_7. Because of the factor $(1+\beta)$ in the denominator, the output resistance of the emitter follower is normally small, as previously determined.

Example 11.17 **Objective:** Calculate the output resistance of the circuit in Figure 11.46.

Consider the same circuit and transistor parameters described in Example 11.16. Assume the Early voltage of Q_7 is 100 V.

Solution: From Example 11.16, we have that $R_{c11} = 1.26\,\text{M}\Omega$ and $r_{\pi 8} = 2.6\,\text{k}\Omega$. We can then determine that

$$R_{c7} = \frac{V_A}{I_Q} = \frac{100}{0.2} = 500\,\text{k}\Omega$$

Then,

$$Z = R_{c11} \| R_{c7} = 1260 \| 500 = 358\,\text{k}\Omega$$

Therefore,

$$R_o = R_4 \left\| \left[\frac{r_{\pi 8} + Z}{(1+\beta)}\right] = 10 \right\| \left(\frac{2.6 + 358}{101}\right) = 2.63\,\text{k}\Omega$$

Comment: The output resistance is obviously less than R_4 and is substantially less than the equivalent resistance Z in the base of Q_8. In a later chapter, we will examine a Darlington pair emitter-follower output stage in which the output resistance is on the order of 100 Ω.

A BJT diff-amp with an active load can produce a small-signal differential-mode voltage gain on the order of 10^3, and the Darlington pair can also provide a voltage gain on the order of 10^3. Since the emitter follower has a gain of essentially unity, the overall voltage gain of the op-amp circuit is on the order of 10^6. This value is typical for the low-frequency, open-loop gain of op-amp circuits.

Test Your Understanding

***11.27** Consider the Darlington pair and emitter-follower portions of the circuit in Figure 11.46. The parameters are: $I_{C7} = I_Q = 0.5\,\text{mA}$, $I_{C8} = 2\,\text{mA}$, $R_4 = 5\,\text{k}\Omega$, and $R_3 = 0.1\,\text{k}\Omega$. For all transistors, the current gain is $\beta = 120$, and for Q_{11} and Q_7, the Early voltage is $V_A = 120\,\text{V}$. Calculate the input resistance and small-signal voltage gain of the Darlington pair, and the output resistance of the emitter follower. (Ans. $R_i = 1.51\,\text{M}\Omega$, $A_v = 3115$, $R_o = 1.14\,\text{k}\Omega$)

11.28 In the circuit in Figure 11.46, the Darlington pair and emitter-follower transistor parameters are the same as in Exercise 11.27. Determine the effective resistance R_{L7} (see Figure 11.47(a)) such that the small-signal voltage gain is 10^3. (Ans. $R_{L7} = 104\,\text{k}\Omega$)

11.7 SIMPLIFIED BJT OPERATIONAL AMPLIFIER CIRCUIT

An operational amplifier (op-amp) is a multistage circuit composed of a differential amplifier input stage, a gain stage, and an output stage. In this section, we will consider a simplified BJT op-amp circuit.

Although active load devices increase the gain of an amplifier, in this discussion, we will consider resistive loads, in order to simplify the analysis and design. For the bipolar circuit, all component values are given; we will analyze both the dc and ac circuit characteristics.

Figure 11.48 depicts a simple bipolar operational amplifier. The differential amplifier stage is biased with a Widlar current source, and a one-sided output is connected to the Darlington pair gain stage. An emitter bypass

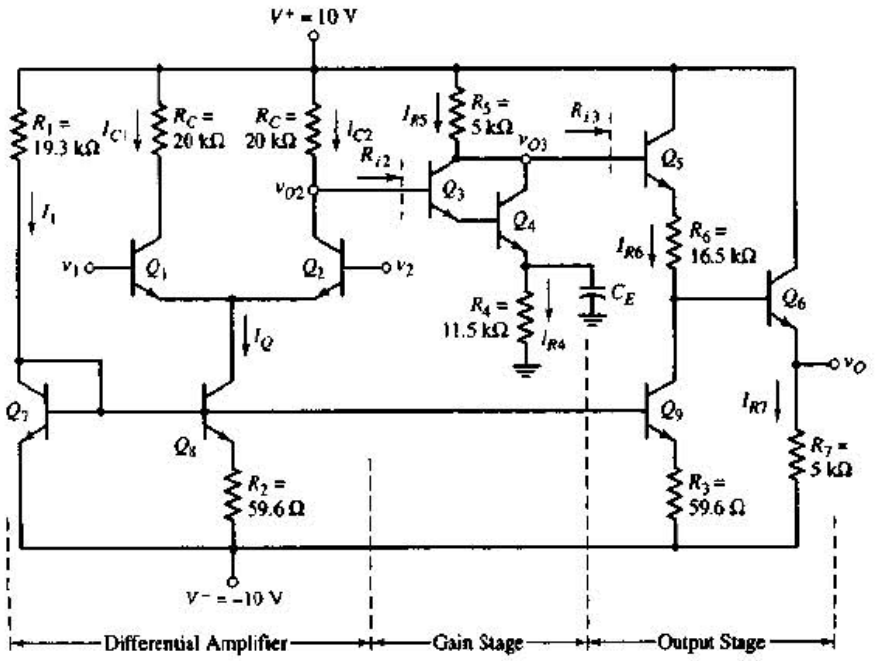


Figure 11.48 Bipolar operational amplifier circuit

capacitor C_E is included to increase the small-signal voltage gain. The output stage is an emitter follower. In general, we want the dc value of the output voltage to be zero when the input voltage is zero. To accomplish this, we need to insert a dc level shifting circuit between the voltage v_{O3} and the output voltage v_O.

Example 11.18 **Objective:** Analyze the dc characteristics of the bipolar op-amp circuit.

Consider the circuit in Figure 11.48. Neglect base currents and, as a simplification, assume $V_{BE}(\text{on}) = 0.7\,\text{V}$ for all transistors except Q_8 and Q_9 in the Widlar circuit.

Solution: The reference current I_1 is

$$I_1 = \frac{10 - 0.7 - (-10)}{19.3} = 1\,\text{mA}$$

The bias current I_Q is determined from

$$I_Q R_2 = V_T \ln\left(\frac{I_1}{I_Q}\right)$$

and is

$$I_Q = 0.4\,\text{mA}$$

The collector currents are then

$$I_{C1} = I_{C2} = 0.2\,\text{mA}$$

The dc voltage at the collector of Q_2 is

$$V_{O2} = 10 - I_{c2}R_C = 10 - (0.2)(20) = 6\,\text{V}$$

With these circuit parameters, the common-mode input voltage is limited to the range $-9.3 \le v_{CM} \le 6\,\text{V}$, which will keep all transistors biased in the forward-active mode.

The current I_{R4} is determined to be

$$I_{R4} = \frac{V_{O2} - 2V_{BE}(\text{on})}{R_4} = \frac{6 - 1.4}{11.5} = 0.4\,\text{mA}$$

Since base currents are assumed negligible, the current I_{R5} is $I_{R5} \cong I_{R4}$.

The dc voltage at the collectors of Q_3 and Q_4 is then

$$V_{O3} = 10 - I_{R5}R_5 = 10 - (0.4)(5) = 8\,\text{V}$$

This shows us that the dc voltage V_{O3} is midway between the 10 V supply voltage and the dc input voltage $V_{O2} = 6\,\text{V}$ to Q_3. This allows a maximum symmetrical swing in the time-varying voltage at v_{o3}.

Transistor Q_5 and resistor R_6 form the dc voltage level shifting function. Since $R_3 = R_2$, we have

$$I_{R6} = I_Q = 0.4\,\text{mA}$$

The dc voltage at the base of Q_6 is found to be

$$V_{B6} = V_{O3} - V_{BE}(\text{on}) - I_{R6}R_6 = 8 - 0.7 - (0.4)(16.5) = 0.7\,\text{V}$$

This relationship produces a zero dc output voltage when a zero differential-mode voltage is applied at the input.

Finally, current I_{R7} is

$$I_{R7} = \frac{v_o - (-10)}{R_7} = \frac{10}{5} = 2\,\text{mA}$$

Comment: The dc analysis of this simplified op-amp circuit proceeds in much the same way as in previous examples. We observe that all transistors are biased in the forward-active mode.

Example 11.19 **Objective:** Determine the small-signal differential-mode voltage gain of the bipolar op-amp circuit.

Consider the circuit in Figure 11.48, with transistor parameters $\beta = 100$ and $V_A = \infty$.

Solution: The overall differential-mode voltage gain can be written

$$A_d = A_{d1} \cdot A_2 \cdot A_3 = \left(\frac{v_{o2}}{v_1 - v_2}\right) \cdot \left(\frac{v_{o3}}{v_{o2}}\right) \cdot \left(\frac{v_o}{v_{o3}}\right)$$

The overall small-signal voltage gain is the product of the individual stage gains *only* if the load resistance of the following stage is taken into account.

We will rely on previous results to determine the individual voltage gains. The input resistances to the Darlington pair R_{i2} and to the output stage R_{i3} are indicated in Figure 11.48. The one-sided differential-mode voltage gain of the diff-amp is given by

$$A_{d1} = \frac{V_{o2}}{v_d} = \frac{g_m}{2}(R_C \| R_{i2})$$

where R_{i2} is the input resistance of the Darlington pair, as follows:

$$R_{i2} = r_{\pi 3} + (1 + \beta) r_{\pi 4}$$

where

$$r_{\pi 4} = \beta V_T / I_{R4} = (100)(0.026)/0.4 = 6.5\,\text{k}\Omega$$

and

$$r_{\pi 3} \cong \beta^2 V_T / I_{R4} = (100)^2(0.026)/0.4 = 650\,\text{k}\Omega$$

Therefore,

$$R_{i2} = 650 + (101)(6.5) = 1307\,\text{k}\Omega$$

The transistor transconductance is

$$g_m = \frac{I_Q}{2V_T} = \frac{0.4}{2(0.026)} = 7.70\,\text{mA/V}$$

The gain of the differential amplifier stage is therefore

$$A_{d1} = \frac{g_m}{2}(R_C \| R_{i2}) = \left(\frac{7.70}{2}\right)[20 \| 1307] = 75.8$$

Since the load resistance $R_{i2} \gg R_C$, there is no significant loading effect of the second stage on the diff-amp stage.

From previous results, we know the voltage gain of the Darlington pair is given by

$$A_2 = \left(\frac{I_{R4}}{2V_T}\right)(R_5 \| R_{i3})$$

where

$$R_{i3} = r_{\pi 5} + (1 + \beta)[R_6 + r_{\pi 6} + (1 + \beta)R_7]$$

We find that

$$r_{\pi 5} = \beta V_T / I_{R6} = (100)(0.026)/0.4 = 6.5\,\text{k}\Omega$$

and

$$r_{\pi 6} = \beta V_T / I_{R7} = (100)(0.026)/2 = 1.3\,\text{k}\Omega$$

Therefore

$$R_{i3} = 6.5 + (101)[16.5 + 1.3 + (101)(5)] \Rightarrow 52.8\,\text{M}\Omega$$

Since $R_{i3} \gg R_5$, the output stage does not load down the gain stage, and the small-signal voltage gain is approximately

$$A_2 \cong \left(\frac{I_{R4}}{2V_T}\right)R_5 = \left[\frac{0.4}{2(0.026)}\right](5) = 38.5$$

The combination of Q_5 and Q_6 forms an emitter follower, and the gain of the output stage is

$$A_3 = v_o / v_{o3} \cong 1$$

The overall small-signal voltage gain is therefore

$$A_d = A_{d1} \cdot A_2 \cdot A_3 = (75.8)(38.5)(1) = 2918$$

Comment: From our previous discussion, we know that the overall gain can be increased substantially by using active loads. Yet, the analysis of this simplified circuit provides some insight into the design of multistage circuits, as well as the overall small-signal voltage gain of op-amp circuits.

Computer Correlation: A PSpice analysis was performed on the bipolar op-amp circuit in Figure 11.48. The dc output voltage from this analysis was $V_O = -0.333\,\text{V}$, rather than the desired value of zero. This occurred because the B–E voltages were not exactly 0.7 V, as assumed in the hand analysis. A zero output voltage can be obtained by slightly adjusting R_6. The differential voltage gain was $A_d = 2932$, which agrees very well with the hand analysis.

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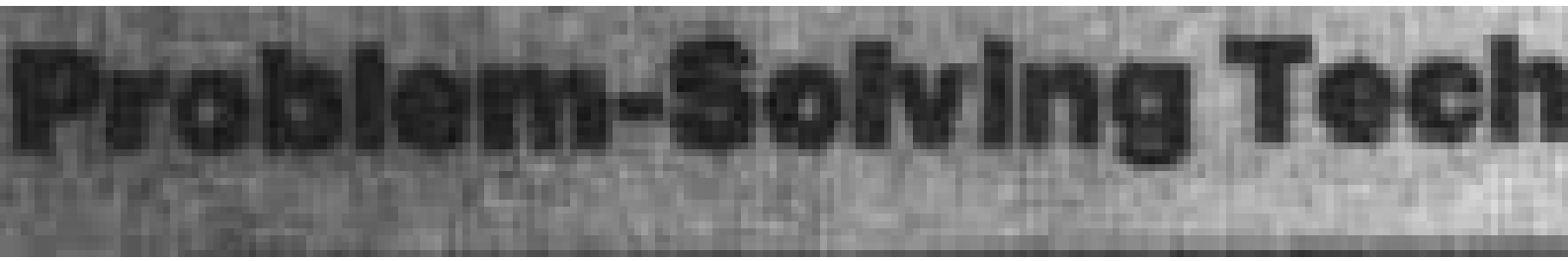
1. Perform the dc analysis of the circuit to determine the small-signal parameters of the transistors. In most cases BJT base currents can be neglected. This assumption will normally provide sufficient accuracy for a hand analysis.
2. Perform the ac analysis on each stage of the circuit, *taking into account the loading effect of the following stage.* (In many cases, previous results of small-signal analyses can be used directly.)
3. The overall small-signal voltage gain or current gain is the product of the gains of the individual stages *as long as the loading effect of each stage is taken into account.*

Test Your Understanding

***RD11.29** Consider the bipolar op-amp circuit in Figure 11.48. The transistor parameters are: $\beta = 100$, $V_{BE}(\text{on}) = 0.7\,\text{V}$ (except for Q_8 and Q_9), and $V_A = \infty$. (a) Redesign the circuit such that $I_{C1} = I_{C2} = 0.1\,\text{mA}$, $I_{R7} = 5\,\text{mA}$, $I_1 = I_{R4} = I_{R6} = 0.6\,\text{mA}$,

Problem-Solving Technique: Multistage Circuits


Problem-Solving Tech

$V_{CE1} = V_{CE2} = 4\,\text{V}$, $V_{CE4} = 3\,\text{V}$, and $v_o = 0$. (b) Determine the input resistances R_{i2} and R_{i3}. (c) Determine the overall differential-mode voltage gain $A_v = v_o/v_d$. (Ans. (a) $R_1 = 32.2\,\text{k}\Omega$, $R_2 = 143\,\text{k}\Omega$, $R_3 = 0$, $R_C = 67\,\text{k}\Omega$, $R_4 = 3.17\,\text{k}\Omega$, $R_5 = 8.5\,\text{k}\Omega$, $R_6 = 5.83\,\text{k}\Omega$, and $R_7 = 2\,\text{k}\Omega$ (b) $R_{i2} = 870\,\text{k}\Omega$, $R_{i3} = 21.0\,\text{M}\Omega$ (c) $A_d = 11{,}674$)

11.8 DIFF-AMP FREQUENCY RESPONSE

In Chapter 7, we considered the frequency responses of the three basic amplifier configurations. In this section, we will analyze the frequency response of the differential amplifier. Since the diff-amp is a linear circuit, we can determine the frequency response due to: (a) a pure differential-mode input signal, (b) a pure common-mode input signal, and (c) the total or net result, using superposition.

11.8.1 Due to Differential-Mode Input Signal

Consider the basic bipolar diff-amp shown in Figure 11.49(a). The input is a pure differential-mode input signal. We know from Equation (11.24) that the small-signal voltage v_e is at signal ground when a differential-mode input signal is applied. To determine the frequency response, we evaluate the equivalent

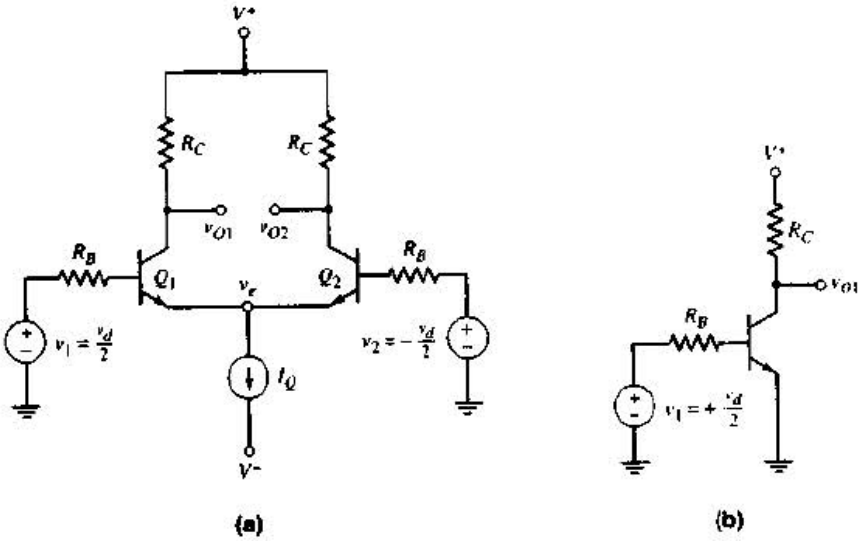


Figure 11.49 (a) BJT differential amplifier with differential-mode input signal and (b) equivalent common-emitter half-circuit of differential amplifier

common-emitter half-circuit in Figure 11.49(b).

Since the diff-amp is a direct-coupled amplifier, the midband voltage gain extends to zero frequency. This one-sided midband gain is

$$A_{v1} = \frac{V_{o1}}{V_d/2} = -g_m R_C \left(\frac{r_\pi}{r_\pi + R_B} \right) \qquad \textbf{(11.111(a))}$$

or

$$A_{v1} = \frac{-\beta R_C}{r_\pi + R_B} \tag{11.111(b)}$$

From the high-frequency common-emitter characteristics determined in Chapter 7 we know that the upper 3 dB frequency is

$$f_H = \frac{1}{2\pi[r_\pi \| R_B](C_\pi + C_M)} \tag{11.112}$$

where C_M is the equivalent Miller capacitance given by

$$C_M = C_\mu(1 + g_m R_C) \tag{11.113}$$

Equation (11.113) implies that, if the value of R_C is fairly large, the Miller capacitance will significantly affect the bandwidth of the differential amplifier.

11.8.2 Due to Common-Mode Input Signal

Figure 11.50(a) shows the basic diff-amp with a pure common-mode input signal. The circuit is symmetrical, which means that resistors R_B, resistors R_C, and the transistors are effectively in parallel. Figure 11.50(b) is the small-signal equivalent circuit, with the constant-current source replaced by its output resistance R_o and capacitance C_o.

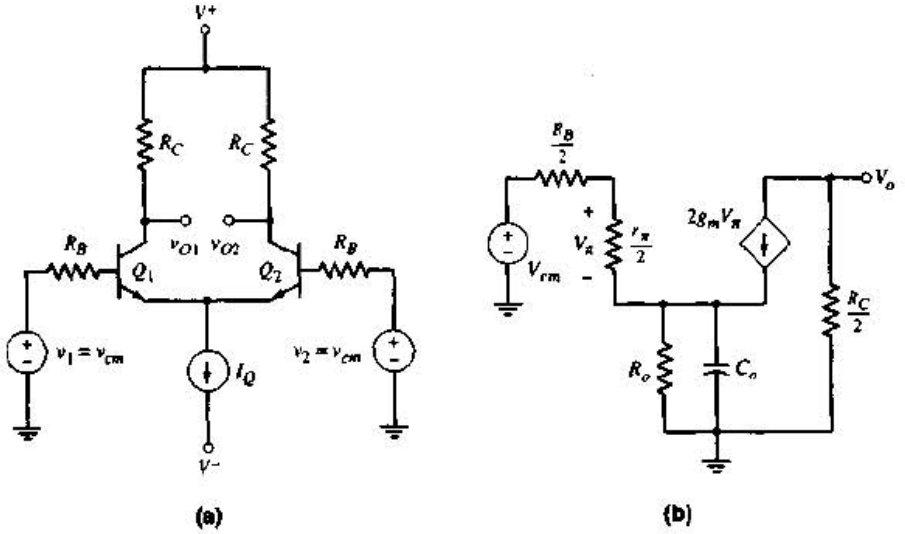


Figure 11.50 (a) BJT differential amplifier with common-mode input signal and (b) small-signal equivalent circuit, common-mode configuration

We will justify neglecting the transistor parameters C_π and C_μ. The output voltage is

$$V_o = -(2g_m V_\pi)\left(\frac{R_C}{2}\right) \tag{11.114}$$