A KVL equation around the B–E loop produces

$$V_{cm} = \left(\frac{V_\pi}{r_\pi/2}\right)\left(\frac{R_B}{2}\right) + V_\pi + \left(\frac{V_\pi}{r_\pi/2} + 2g_m V_\pi\right)\left[R_o \left\| \left(\frac{1}{sC_o}\right)\right.\right] \qquad \textbf{(11.115(a))}$$

or

$$V_{cm} = V_\pi\left\{\frac{R_B}{r_\pi} + 1 + 2\left(\frac{1+\beta}{r_\pi}\right)\left(\frac{R_o}{1+sR_oC_o}\right)\right\} \qquad \textbf{(11.115(b))}$$

Solving for V_π and substituting the result into Equation (11.114) yields the common-mode gain, which is

$$A_{cm} = \frac{V_o}{V_{cm}} = \frac{-g_m R_C}{\dfrac{R_B}{r_\pi} + 1 + \dfrac{2(1+\beta)}{r_\pi}\left(\dfrac{R_o}{1+sR_oC_o}\right)} \qquad \textbf{(11.116(a))}$$

or

$$A_{cm} = \frac{-g_m R_C(1+sR_oC_o)}{\left(1+\dfrac{R_B}{r_\pi}\right)(1+sR_oC_o) + \dfrac{2(1+\beta)R_o}{r_\pi}} \qquad \textbf{(11.116(b))}$$

Equation (11.116(b)) shows that there is a zero in the common-mode gain. To explain, capacitor C_o is in parallel with R_o, and it acts as a bypass capacitor. At very low frequency, C_o is effectively an open circuit and the common-mode signal "sees" R_o. As the frequency increases, the impedance of the capacitor decreases and R_o is effectively bypassed; hence, the zero in Equation (11.116(b)). The frequency analysis of an emitter bypass capacitor also showed the presence of a zero in the voltage gain expression.

The common-mode gain frequency response is shown in Figure 11.51. The frequency of the zero is

$$f_z = \frac{1}{2\pi R_oC_o} \qquad \textbf{(11.117)}$$

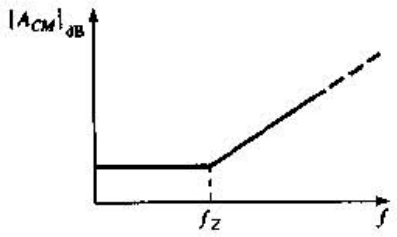

Figure 11.51 Frequency response of common-mode gain

Since the output resistance R_o of a constant-current source is normally large, a small capacitance C_o can result in a small f_z. For frequencies greater than f_z, the common-mode gain increases at the rate of 6 dB/octave.

Equation (11.116(b)) also shows that there is a pole associated with the common-mode gain. Rearranging the terms in that equation, we see that the frequency of the pole is

$$f_p = \frac{1}{2\pi R_{eq} C_o} \tag{11.118}$$

where

$$R_{eq} = \frac{R_o\left(1 + \dfrac{R_B}{r_\pi}\right)}{1 + \dfrac{R_B}{r_\pi} + \dfrac{2(1+\beta)R_o}{r_\pi}} \tag{11.119}$$

The denominator of Equation (11.119) is very large, because of the term $(1 + \beta)R_o$. This implies that R_{eq} is small, which means that the frequency f_p of the pole is very large.

The differential-mode gain is shown in Figure 11.52. The frequency response of the common-mode rejection ratio is found by combining Figures 11.51 and 11.52, and is shown in Figure 11.53.

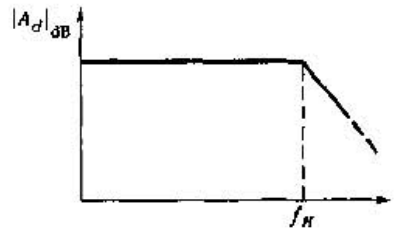

Figure 11.52 Frequency response of differential-mode gain

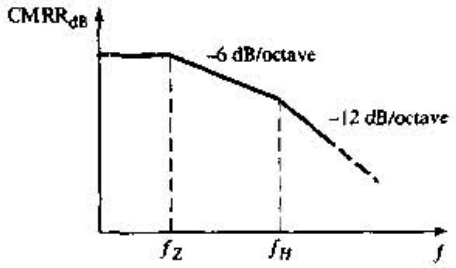

Figure 11.53 Frequency response of common-mode rejection ratio

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Example 11.20 **Objective:** Determine the zero and pole frequencies in the common-mode gain.

Consider a diff-amp biased with a constant-current source. The output resistance is $R_o = 10\,\text{M}\Omega$ and the output capacitance is $C_o = 1\,\text{pF}$. Assume the circuit and transistor parameters are $R_B = 0.5\,\text{k}\Omega$, $r_\pi = 10\,\text{k}\Omega$, and $\beta = 100$.

Solution: In the common-mode gain, the frequency of the zero is

$$f_z = \frac{1}{2\pi R_o C_o} = \frac{1}{2\pi(10 \times 10^6)(1 \times 10^{-12})} \Rightarrow 15.9\,\text{kHz}$$

Also in the common-mode gain, the frequency of the pole is

$$f_P = 1/(2\pi R_{eq} C_o)$$

where

$$R_{eq} = \frac{R_o\left(1 + \dfrac{R_B}{r_\pi}\right)}{1 + \dfrac{R_B}{r_\pi} + \dfrac{2(1+\beta)R_o}{r_\pi}} = \frac{(10 \times 10^6)\left(1 + \dfrac{0.5}{10}\right)}{1 + \dfrac{0.5}{10} + \dfrac{2(101)(10 \times 10^6)}{10 \times 10^3}}$$

or

$$R_{eq} = 51.98\,\Omega$$

The frequency of the pole is therefore

$$f_P = \frac{1}{2\pi(51.98)(1 \times 10^{-12})} \Rightarrow 3.06\,\text{GHz}$$

Comment: The frequency of the zero in the common-mode gain is fairly low, while the frequency of the pole is extremely large. The relatively low frequency of the zero justifies neglecting the effect of C_π and C_μ. The CMRR frequency response is shown in Figure 11.53, where f_z is the zero frequency of the common-mode gain and f_H is the upper 3 dB frequency of the differential-mode gain.

11.8.3 With Emitter-Degeneration Resistors

Figure 11.54 shows a bipolar diff-amp with two resistances R_E connected in the emitter portion of the circuit. One effect of including an emitter resistor is to reduce the voltage gain, so the presence of these resistors is termed **emitter degeneration**.

In Chapter 7, we found that an emitter-follower circuit, which includes an emitter resistance, is a wide-bandwidth amplifier. Therefore, one effect of

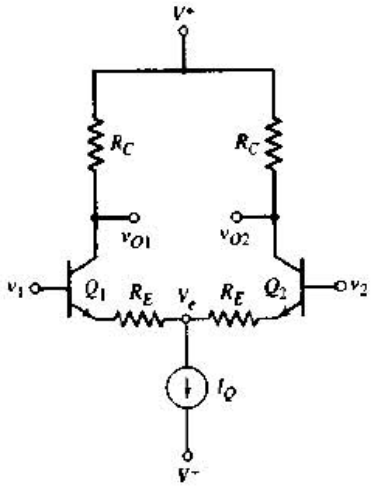


Figure 11.54 BJT differential amplifier with emitter-degeneration resistors

resistors R_E is an increase in the bandwidth of the differential amplifier. We rely on a computer simulation to evaluate emitter degeneration effects.

Figure 11.55 shows the frequency response of a one-sided differential-mode gain, obtained from a PSpice analysis for four R_E resistance values. The diff-amp is biased at $I_Q = 0.5\,\text{mA}$ and the R_C resistors are $R_C = 30\,\text{k}\Omega$. The transistor capacitances are $C_\pi = 34.6\,\text{pF}$ and $C_\mu = 4.3\,\text{pF}$. As the emitter degeneration increases, the differential-mode voltage gain decreases, but the bandwidth increases, as previously indicated. The figure-of-merit for amplifiers, the gain-bandwidth product, is approximately a constant for the results shown in Figure 11.55.

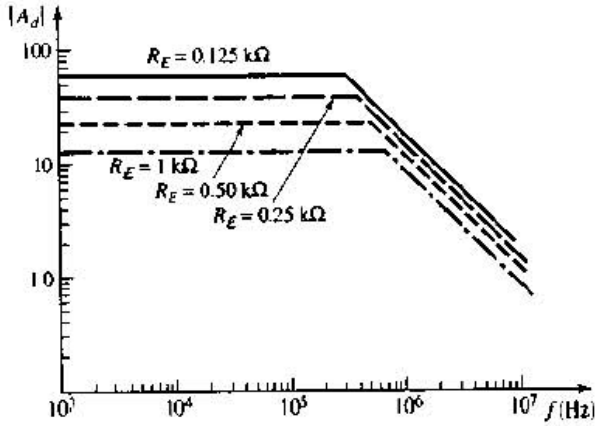


Figure 11.55 PSpice results for frequency response of diff-amp with emitter-degeneration

11.8.4 With Active Load

Figure 11.56 shows a bipolar diff-amp with an active load and a single input at v_1. The base and collector junctions of Q_3 are connected together, and a one-sided output is taken at v_{O2}.

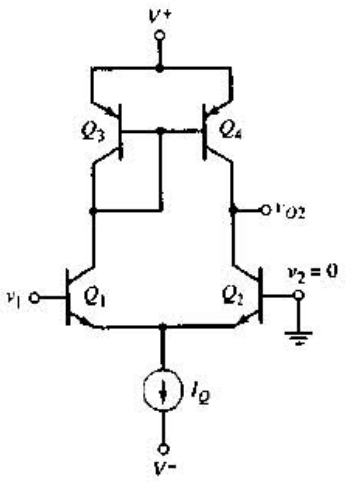


Figure 11.56 BJT diff-amp with active load and single-sided input signal

With the connection of Q_3, the equivalent load resistance in the collector of Q_1 is on the order of $r_\pi/(1+\beta)$. This small resistance minimizes the Miller multiplication factor in Q_1. Also, with the base of Q_2 at ground potential, one side of $C_{\mu 2}$ is grounded, and the Miller multiplication in Q_2 is zero. Therefore, we expect the bandwidth of the diff-amp with an active load to be relatively wide. At high frequencies, however, the effective impedance in the collector of Q_1 also includes the input capacitances of Q_3 and Q_4. These additional capacitances also affect the frequency response of the diff-amp, potentially narrowing the bandwidth.

Again, we rely on a computer analysis to determine the frequency characteristics of the diff-amp with an active load. Figure 11.57 shows the results of the computer simulation. The diff-amp is biased at $I_Q = 0.5\,\text{mA}$, and the Early voltage of each transistor is assumed to be 80 V. The transistor capacitances are $C_\pi = 34.6\,\text{pF}$ for each transistor, $C_\mu = 3.8\,\text{pF}$ in Q_1 and Q_2, and $C_\mu = 7\,\text{pF}$ and 5.5 pF in Q_3 and Q_4, respectively.

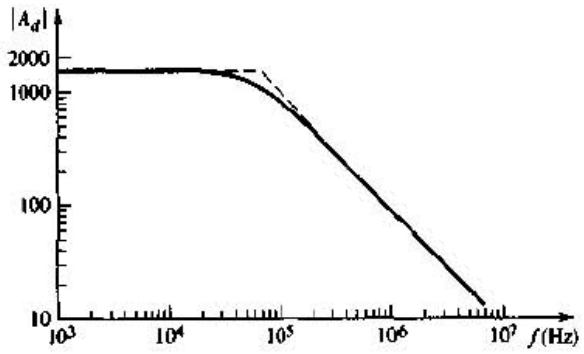


Figure 11.57 PSpice results for frequency response of diff-amp with active load and single-sided input signal

The low-frequency voltage gain is 1560 and the upper 3 dB frequency is 64 kHz. The large gain is as expected for an active load amplifier, but the 3 dB frequency is lower than expected. However, the gain–bandwidth product for the active load diff-amp is approximately four times that of the diff-amp shown in Figure 11.54. The increased gain–bandwidth product implies a reduced Miller multiplication factor in the active load diff-amp, as predicted.

11.9 SUMMARY

- The ideal differential amplifier amplifies only the difference between two input signals.
- The differential-mode input voltage is defined as the difference between the two input signals and the common-mode input voltage is defined as the average of the two input signals.
- When a differential input voltage is applied, one transistor of the differential pair turns on more than the second transistor of the differential pair so that the currents become unbalanced, producing a signal output voltage.

- A common-mode output signal is generated because of a finite output resistance of the current source.
- The common-mode rejection ratio, CMRR, is defined in terms of decibels as $CMRR_{dB} = 20 \log_{10} |A_d/A_{cm}|$, where A_d and A_{cm} are the differential-mode voltage gain and common-mode voltage gain, respectively.
- Differential amplifiers are usually designed with active loads to increase the differential-mode voltage gain.
- BiCMOS circuits may be designed to incorporate the best parameters and characteristics of BJTs and MOSFETs in the same circuit.
- A BJT Darlington pair is typically used as a second stage to a BJT diff-amp. The input impedance is large, which tends to minimize loading effects on the diff-amp, and the effective current gain of the pair is the product of the individual gains.

CHECKPOINT

After studying this chapter, the reader should have the ability to:

✔ Describe the mechanism by which a differential-mode signal and common-mode signal are produced in a BJT diff-amp. (Section 11.2)

✔ Describe the dc transfer characteristics of a BJT diff-amp. (Section 11.2)

✔ Define common-mode rejection ratio. (Section 11.2)

✔ Describe the mechanism by which a differential-mode signal and common-mode signal are produced in a MOSFET diff-amp. (Section 11.3)

✔ Describe the dc transfer characteristics of a MOSFET diff-amp. (Section 11.3)

✔ Design a MOSFET diff-amp with an active load to yield a specified differential-mode voltage gain. (Section 11.4)

✔ Analyze BiCMOS circuits. (Section 11.5)

✔ Analyze a simplified BJT operational amplifier circuit. (Section 11.7)

REVIEW QUESTIONS

1. Define differential-mode and common-mode input voltages.
2. Sketch the dc transfer characteristics of a BJT differential amplifier.
3. From the dc transfer characteristics, qualitatively define the linear region of operation for a differential amplifier.
4. What is meant by matched transistors?
5. Explain how a differential-mode output signal is generated.
6. Explain how a common-mode output signal is generated.
7. Define the common-mode rejection ratio, CMRR. What is the ideal value?
8. What design criteria will yield a large value of CMRR in an emitter-coupled pair?
9. Sketch the differential-mode and common-mode half-circuit models for an emitter-coupled diff-amp.
10. Define differential-mode and common-mode input resistances.
11. Sketch the dc transfer characteristics of a MOSFET differential amplifier.
12. Sketch and describe the advantages of a MOSFET cascode current source used with a MOSFET differential amplifier.
13. Sketch a simple MOSFET differential amplifier with an active load.
14. Explain the advantages of an active load.
15. Sketch and describe the advantages of a MOSFET cascode active load with a MOSFET differential pair.

16. Discuss one advantage of a BiCMOS circuit.
17. Describe the effect of connecting a second stage to the output of the diff-amp on the differential-mode voltage gain of the first stage.
18. Explain the frequency response of the differential-mode voltage gain.
19. Sketch a BJT Darlington pair circuit and explain the advantages.
20. Describe the three stages of a simple BJT operational amplifier.

PROBLEMS

Section 11.2 Basic BJT Differential Pair

RD11.1 Consider the differential amplifier shown in Figure P11.1, with transistor parameters: $\beta = 200$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, and $V_A = \infty$. (a) Redesign the circuit such that the Q-point values are $I_{C1} = I_{C2} = 2.0\,\text{mA}$ and $V_{O2} = 8\,\text{V}$ when $v_1 = v_2 = 0$. (b) Draw the dc load line and plot the Q-point for transistor Q_2. (c) What are the maximum and minimum values of the common-mode input voltage?

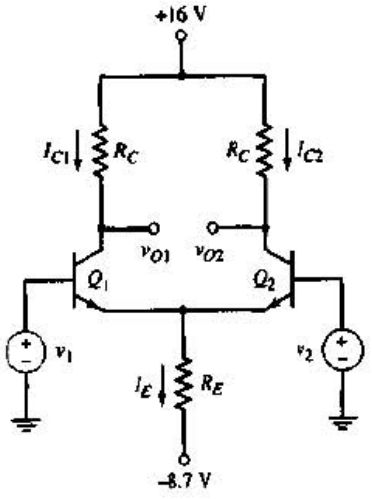


Figure P11.1

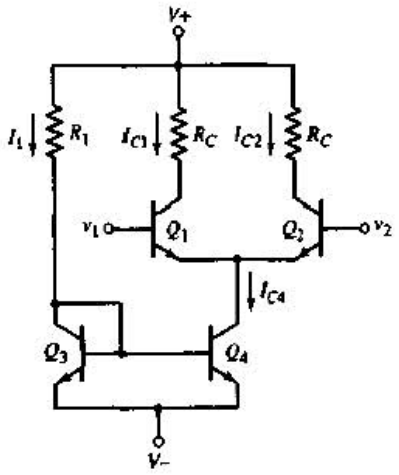


Figure P11.2

D11.2 The diff-amp configuration shown in Figure P11.2 is biased at ±3 V. The maximum power dissipation in the entire circuit is to be no more than 1.2 mW when $v_1 = v_2 = 0$. The available transistors have parameters: $\beta = 120$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, and $V_A = \infty$. Design the circuit to produce the maximum possible differential-mode voltage gain, but such that the common-mode input voltage can be within the range $-1 \le v_{CM} \le 1\,\text{V}$ and the transistors are still biased in the forward-active region. What is the value of A_d? What are the current and resistor values?

11.3 The differential amplifier in Figure P11.3 is biased with a three-transistor current source. The transistor parameters are: $\beta = 100$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, and $V_A = \infty$. (a) Determine I_1, I_{C2}, I_{C4}, V_{CE2}, and V_{CE4}. (b) Determine a new value of R_1 such that $V_{CE4} = 2.5\,\text{V}$. What are the values of I_{C4}, I_{C2}, I_1, and R_1?

11.4 Consider the circuit in Figure P11.4, with transistor parameters: $\beta = 100$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, and $V_A = \infty$. (a) For $v_1 = v_2 = 0$, find I_{C1}, I_{C2}, I_E, V_{CE1}, and V_{CE2}. (b) Determine the maximum and minimum values of the common-mode input voltage. (c) Calculate A_d for a one-sided output at the collector of Q_2.

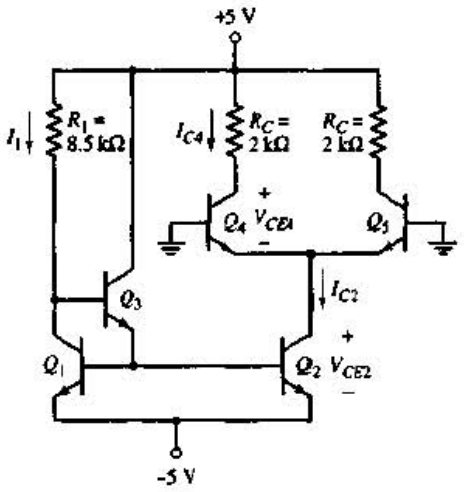


Figure P11.3

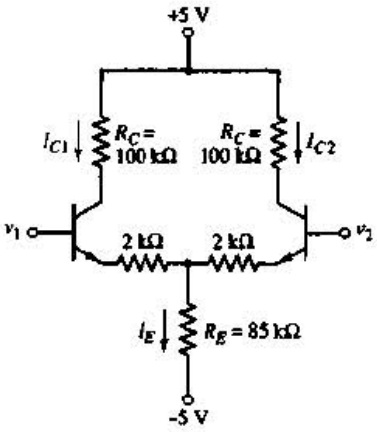


Figure P11.4

11.5 Consider the differential amplifier in Figure P11.5. Neglect base currents, assume $V_A = \infty$ for all transistors, and let $I_Q = 2\,\text{mA}$. The emitter currents can be written as

$$I_{E1} = I_{S1}e^{V_{BE1}/V_T} \quad \text{and} \quad I_{E2} = I_{S2}e^{V_{BE2}/V_T}$$

(a) If $v_1 = v_2 = 0$ and $I_{S1} = I_{S2} = 1 \times 10^{-13}\,\text{A}$, find $(v_{o1} - v_{o2})$ when: (i) $R_{C1} = R_{C2} = 8\,\text{k}\Omega$, and (ii) $R_{C1} = 8\,\text{k}\Omega$, $R_{C2} = 7.9\,\text{k}\Omega$. (b) Repeat part (a) if $I_{S1} = 1 \times 10^{-13}\,\text{A}$ and $I_{S2} = 1.1 \times 10^{-13}\,\text{A}$.

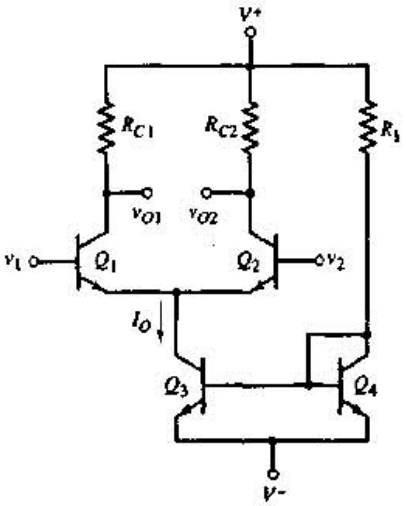


Figure P11.5

11.6 For the diff-amp in Figure 11.2, determine the value of $v_d = v_1 - v_2$ that produces $i_{C2} = 0.90I_Q$.

***RD11.7** The diff-amp for the experimental system described in Example 11.4 needs to be redesigned. The range of the output voltage has increased to $-2 \le V_O \le 2\,\text{V}$ while the differential-mode voltage gain is still $A_d = 100$. The common-mode input voltage has increased to $v_{CM} = 3.5\,\text{V}$. The value of CMRR needs to be increased to 80 dB.

***11.8** The transistor parameters for the circuit in Figure P11.8 are: $\beta = 100$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, and $V_A = \infty$. (a) Determine R_E such that $I_E = 150\,\mu\text{A}$. (b) Find A_d, A_{cm}, and CMRR_{dB} for a one-sided output at v_{O2}. (c) Determine the differential- and common-mode input resistances.

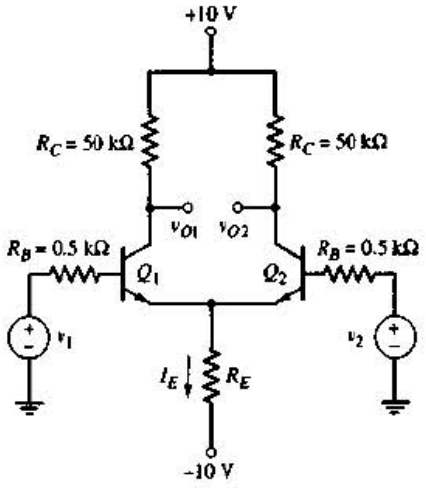


Figure P11.8

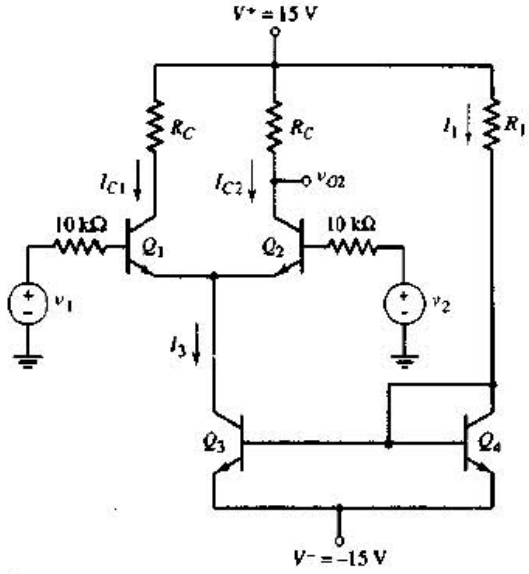


Figure P11.10

***11.9** The transistor parameters for the circuit in Figure P11.8 are: $\beta = 120$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, and $V_A = \infty$. (a) Determine R_E such that $I_E = 0.25\,\text{mA}$. (b) Assume the R_B resistance connected to the base of Q_2 is zero while the R_B resistance connected to the base of Q_1 remains at $0.5\,\text{k}\Omega$. (i) Determine the differential-mode voltage gain for a one-sided output at v_{O2}. (ii) Determine the common-mode voltage gain for a one-sided output at v_{O2}.

***RD11.10** For the transistors in the circuit in Figure P11.10, the parameters are $\beta = 100$ and $V_{BE}(\text{on}) = 0.7\,\text{V}$. The Early voltage is $V_A = \infty$ for Q_1 and Q_2, and is $V_A = 50\,\text{V}$ for Q_3 and Q_4. (a) Redesign resistor values such that $I_3 = 400\,\mu\text{A}$ and $V_{CE1} = V_{CE2} = 10\,\text{V}$. (b) Find A_d, A_{cm}, and CMRR_{dB} for a one-sided output at v_{O2}. (c) Determine the differential- and common-mode input resistances.

D11.11 Consider the diff-amp in Figure 11.2. Base currents are negligible and $V_A = \infty$ for each transistor. The supply voltages are $V^+ = 10\,\text{V}$ and $V^- = -10\,\text{V}$, and the maximum current source available is $I_Q = 2\,\text{mA}$. Design the circuit such that a differential-mode output voltage of $v_o = v_{C2} - v_{C1} = 2\,\text{V}$ is produced when a differential-mode input voltage of $v_d = v_1 - v_2 = 15\,\text{mV}$ is applied. What is the maximum possible common-mode input voltage for this circuit?

***11.12** Consider the circuit in Figure P11.12. Assume the Early voltage of Q_1 and Q_2 is $V_A = \infty$, and assume the current source I_Q is ideal. Derive the expressions for the one-sided differential-mode gain $A_{v1} = v_{o1}/v_d$ and $A_{v2} = v_{o2}/v_d$, and for the two-sided differential-mode gain $A_d = (v_{o2} - v_{o1})/v_d$.

11.13 The Early voltage of transistors Q_1 and Q_2 in the circuit in Figure P11.13 is $V_A = \infty$. Assming an ideal current source I_Q, derive the expression for the differential-mode gain $A_d = v_o/v_d$.

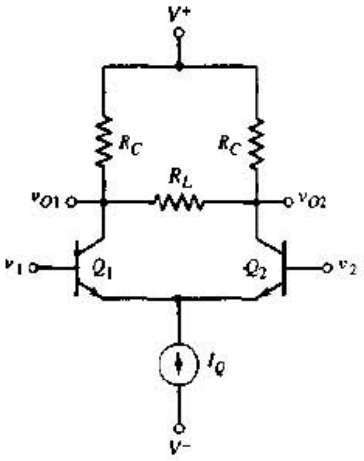


Figure P11.12

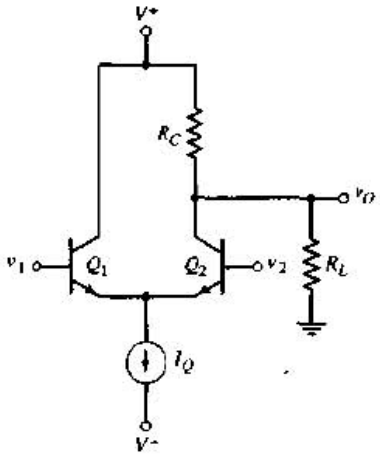


Figure P11.13

***11.14** Consider the small-signal equivalent circuit of the differential-pair configuration shown in Figure 11.8. Derive the expressions for the differential- and common-mode voltage gains if the output is a two-sided output defined as $V_o = V_{c2} - V_{c1}$.

***D11.15** Consider a BJT diff-amp with the configuration in Figure P11.15. The signal sources have nonzero source resistances as shown. The transistor parameters are: $\beta = 150$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, and $V_A = \infty$. The range of the common-mode input voltage is to be $-3 \le v_{CM} \le 3\,\text{V}$ and the CMRR is to be 75 dB. (a) Design the diff-amp to produce the maximum possible differential-mode voltage gain. (b) Design the current source to produce the desired bias current and CMRR.

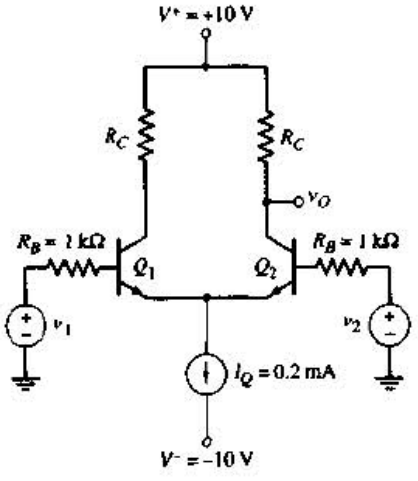


Figure P11.15

11.16 A diff-amp has a differential-mode voltage gain of 180 and a CMRR of 85 dB. A differential-mode input signal of $v_d = 2\sin\omega t\,\text{mV}$ is applied, along with a common-mode voltage of $V_{cm} = 2\sin\omega t\,\text{V}$. Determine the ideal output voltage and the actual output voltage.

***11.17** The bridge circuit in Figure P11.17 is a temperature transducer in which the resistor R_A is a thermistor (a resistor whose resistance varies with temperature). The value of δ varies over the range of $-0.01 \le \delta \le 0.01$ as temperature varies over a particular range. Assume the value of $R = 10\,\text{k}\Omega$. The bridge circuit is to be connected to the diff-amp in Figure 11.2. The transistor parameters are: $\beta = 120$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, and $V_A = \infty$. The circuit parameters are: $I_Q = 0.5\,\text{mA}$, $R_C = 3\,\text{k}\Omega$, and dc bias voltages $= \pm 5\,\text{V}$. Terminal A of the bridge circuit is connected to the base of Q_1 and terminal B is connected to the base of Q_2. Determine the range of output voltage v_{O2} as δ changes. [Hint: Make a Thevenin equivalent circuit at terminals A and B of the bridge circuit.]

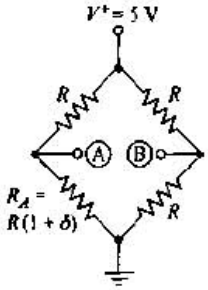


Figure P11.17

11.18 A diff-amp is biased with a constant-current source $I_Q = 0.4\,\text{mA}$, for which the output resistance is $R_o = 1\,\text{M}\Omega$. The bipolar transistor parameters are $\beta = 180$ and $V_A = 125\,\text{V}$. Determine: (a) the differential-mode input resistance, and (b) the common-mode input resistance.

D11.19 The transistor parameters for the circuit shown in Figure P11.19 are: $\beta = 180$, $V_{BE}(\text{on}) = 0.7\,\text{V}$ at 1 mA, and $V_A = 100\,\text{V}$. (a) Determine R_1 and R_2 such that $I_1 = 1\,\text{mA}$ and $I_Q = 100\,\mu\text{A}$. (b) Determine the common-mode input resistance. (c) For $R_C = 50\,\text{k}\Omega$, determine the common-mode voltage gain.

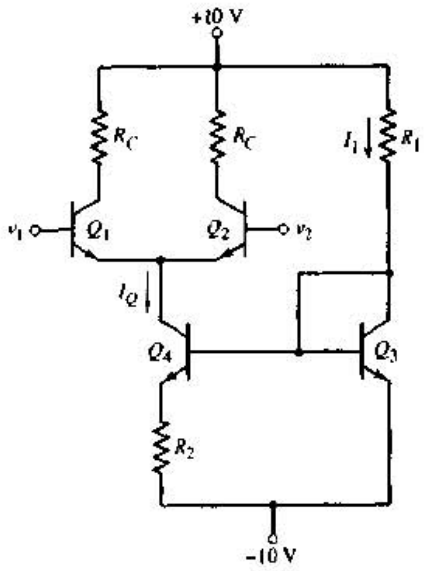


Figure P11.19

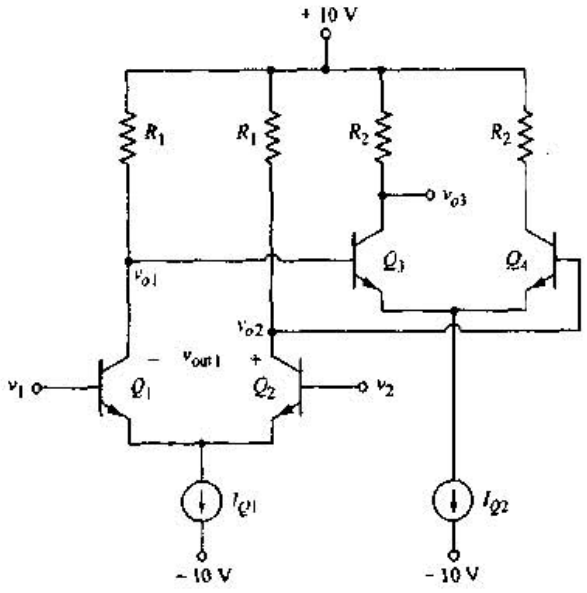


Figure P11.20

D11.20 Figure P11.20 shows a two-stage cascade diff-amp with resistive loads. Power supply voltages of $\pm 10\,\text{V}$ are available. Assume transistor parameters of: $\beta = 100$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, and $V_A = \infty$. Design the circuit such that the two-sided differential-mode voltage gain is $A_{d1} = (v_{o1} - v_{o1})/(v_1 - v_2) = 20$ for the first stage, and that the one-sided differential-mode voltage gain is $A_{d2} = v_{o3}/(v_{o2} - v_{o1}) = 30$ for the second stage. The circuit is to be designed such that the maximum differential-mode voltage swing is obtained in each stage.

Section 11.3 Basic FET Differential Pair

11.21 For the differential amplifier in Figure P11.21 the parameters are $R_1 = 50\,\text{k}\Omega$ and $R_D = 24\,\text{k}\Omega$. The transistor parameters are: $K_n = 0.25\,\text{mA/V}^2$, $\lambda = 0$, and $V_{TN} = 2\,\text{V}$. (a) Determine I_1, I_Q, I_{D1}, V_{DS1}, and V_{DS4} when $v_1 = v_2 = 0$. (b) Draw the dc load line and plot the Q-point for transistor M_2. (c) What are the maximum and minimum values of the common-mode input voltage?

RD11.22 The transistor parameters in the differential amplifier in Figure P11.21 are: $K_{n1} = K_{n2} = 100\,\mu\text{A/V}^2$, $K_{n3} = K_{n4} = 200\,\mu\text{A/V}^2$, $\lambda_1 = \lambda_2 = 0$, $\lambda_3 = \lambda_4 = 0.01\,\text{V}^{-1}$, and $V_{TN} = 1.2\,\text{V}$ (all transistors). (a) Design the circuit such that $V_{DS1} = V_{DS2} = 12\,\text{V}$ and $I_{D1} = I_{D2} = 120\,\mu\text{A}$ when $v_1 = v_2 = -5.4\,\text{V}$. What are the values of I_Q and I_1? (b) Calculate the change in I_Q if $v_1 = v_2 = 0$.

11.23 The transistor parameters for the differential amplifier in Figure P11.23 are: $K_n = 0.4\,\text{mA/V}^2$, $\lambda = 0$, and $V_{TN} = 2\,\text{V}$. (a) Find R_D and I_Q such that $I_{D1} = I_{D2} = 0.5\,\text{mA}$ and $v_{O2} = 7\,\text{V}$ when $v_1 = v_2 = 0$. (b) Draw the dc load line, and plot the Q-point for transistor M_2. (c) What are the maximum and minimum common-mode input voltages?

11.24 Consider the differential amplifier in Figure P11.24. Assume $\lambda = 0$ and $V_{TN} = 0.8\,\text{V}$ for all transistors, and let $I_Q = 1\,\text{mA}$. The drain currents can be written as

$$I_{D1} = K_{n1}(V_{GS1} - V_{TN})^2 \quad \text{and} \quad I_{D2} = K_{n2}(V_{GS2} - V_{TN})^2$$

(a) If $v_1 = v_2 = 0$ and $K_{n1} = K_{n2} = 0.4\,\text{mA/V}^2$, find $(v_{o1} - v_{o2})$ when: (i) $R_{D1} = R_{D2} = 6\,\text{k}\Omega$, and (ii) $R_{D1} = 6\,\text{k}\Omega$, $R_{D2} = 5.9\,\text{k}\Omega$. (b) Repeat part (a) if $K_{n1} = 0.4\,\text{mA/V}^2$ and $K_{n2} = 0.44\,\text{mA/V}^2$.

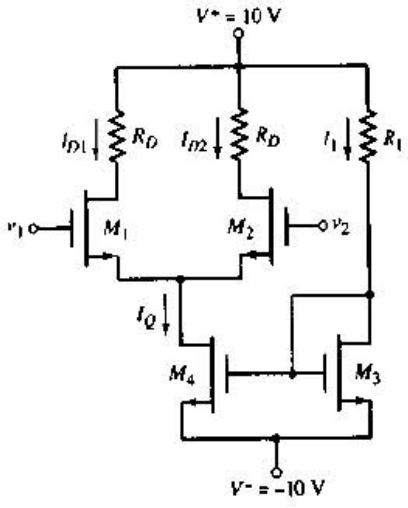


Figure P11.21

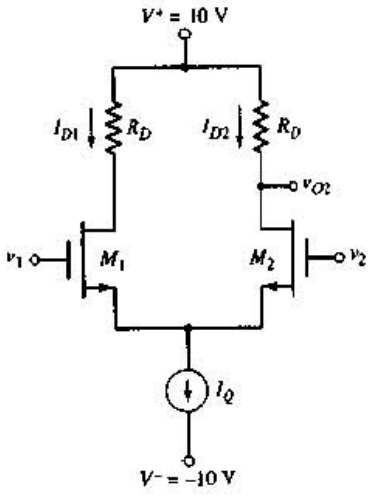


Figure P11.23

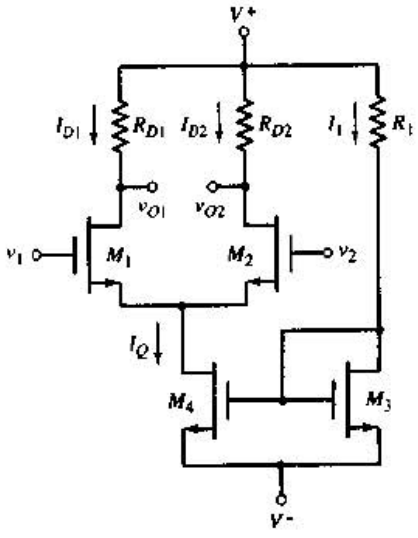


Figure P11.24

11.25 The transistor parameters for the diff-amp shown in Figure 11.19 are: $K_n = 0.1\,\text{mA/V}^2$, $\lambda = 0$, and $V_{TN} = 1\,\text{V}$. The bias current is $I_Q = 0.25\,\text{mA}$. (a) Determine the value of $v_d = v_{G1} - v_{G2}$ that produces $i_{D2} = 0.90\,I_Q$. (b) At what value of v_d does $i_{D1} = I_Q$?

***D11.26** The Hall effect experimental arrangement was described in Example 11.4. The required diff-amp is to be designed in the circuit configuration in Figure P11.24.

The transistor parameters are $V_{TN} = 0.8\,\text{V}$, $k_n' = 80\,\mu\text{A/V}^2$, $\lambda_1 = \lambda_2 = 0$, and $\lambda_3 = \lambda_4 = 0.01\,\text{V}^{-1}$. If the CMRR requirement cannot be met, a more sophisticated current source may have to be designed.

***11.27** Consider the diff-amp in Figure P11.27. The transistor parameters are: $K_{n1} = K_{n2} = 50\,\mu\text{A/V}^2$, $\lambda_1 = \lambda_2 = 0.02\,\text{V}^{-1}$, and $V_{TN1} = V_{TN2} = 1\,\text{V}$. (a) Determine I_S, I_{D1}, I_{D2}, and v_{O2} for $v_1 = v_2 = 0$. (b) Using the small-signal equivalent circuit, determine the differential-mode voltage gain $A_d = v_{o2}/v_d$, the common-mode voltage gain $A_{cm} = v_{o2}/v_{cm}$, and the CMRR_{dB}.

11.28 Consider the circuit shown in Figure P11.28. Assume that $\lambda = 0$ for M_1 and M_2. Also assume an ideal current source I_Q. Derive the expression for the one-sided differential mode gains $A_{d1} = v_{o1}/v_d$ and $A_{d2} = v_{o2}/v_d$, and the two-sided differential-mode gain $A_d = (v_{o2} - v_{o1})/v_d$.

11.29 Assume $\lambda_1 = \lambda_2 = 0$ for the transistors M_1 and M_2 in the circuit in Figure P11.29. Assuming an ideal current source I_Q, derive the expression for the differential-mode gain $A_d = v_o/v_d$.

***RD11.30** Consider the diff-amp in Figure 11.19. Assume $\lambda = 0$ and $V_{TN} = 1\,\text{V}$ for each transistor. The supply voltages are $V^+ = 10\,\text{V}$ and $V^- = -10\,\text{V}$, and the maximum current source available is $I_Q = 0.5\,\text{mA}$. Redesign the circuit such that a differential-mode output voltage of $v_o = 2\,\text{V}$ is produced when a differential-mode input voltage of $v_d = v_1 - v_2 = 200\,\text{mV}$ is applied. What is the maximum possible common-mode input voltage that can be applied to this circuit?

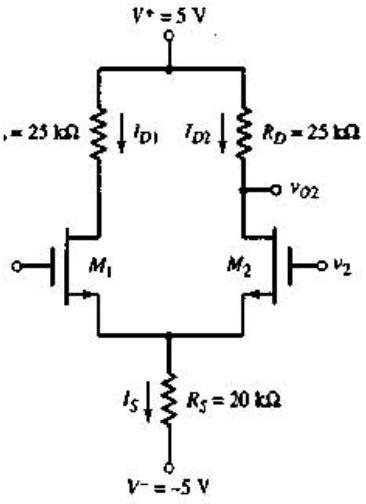


Figure P11.27

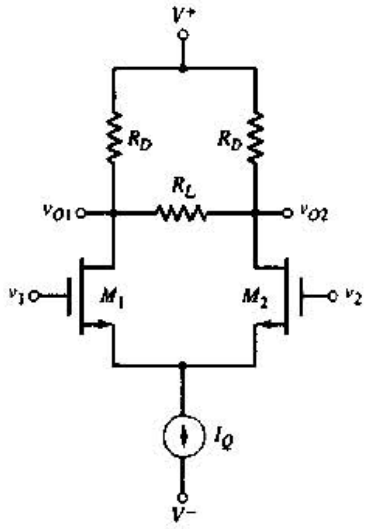


Figure P11.28

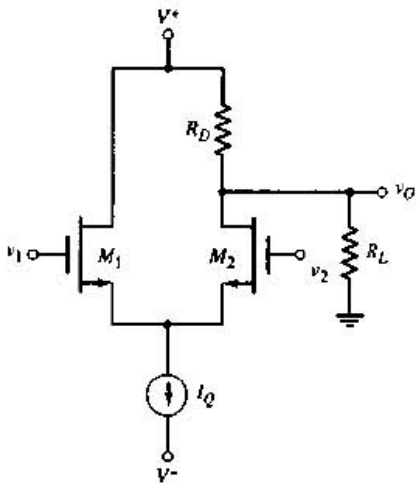


Figure P11.29

11.31 Consider the small-signal equivalent circuit in Figure 11.23. Assume the output is a two-sided output defined as $V_o = V_{d2} - V_{d1}$, where V_{d2} and V_{d1} are the signal voltages at the drains of M_2 and M_1, respectively. Derive expressions for the differential- and common-mode voltage gains.

***D11.32** Consider a MOSFET diff-amp with the configuration in Figure P11.23. The transistor parameters are $V_{TN} = 1\,\text{V}$, $k_n' = 80\,\mu\text{A/V}^2$, $(W/L)_1 = (W/L)_2 = 10$, and $\lambda = 0$. Let $I_Q = 0.2\,\text{mA}$. The range of the common-mode input voltage is $-3 \le v_{CM} \le 3\,\text{V}$ and the CMRR is to be 45 dB. (a) Design the diff-amp to produce the maximum possible differential-mode voltage gain. (b) Design an all-MOSFET current

source to produce the desired bias current and CMRR. (The minimum W/L ratio of any transistor is to be 0.8.)

11.33 Consider the bridge circuit and diff-amp described in Problem 11.17. The BJT pair is to be replaced with a MOSFET pair whose parameters are $V_{TN} = 0.5\,\text{V}$, $K_n = 0.25\,\text{mA/V}^2$, and $\lambda = 0$. Determine the range of output voltage v_{O2} as δ changes. Explain the advantages and disadvantages of this circuit configuration compared to that in Problem 11.17.

***D11.34** Figure P11.34 shows a two-stage cascade diff-amp with resistive loads. Power supply voltages of $\pm 10\,\text{V}$ are available. Assume transistor parameters of $V_{TN} = 1\,\text{V}$, $k_n' = 60\,\mu\text{A/V}^2$, and $\lambda = 0$. Design the circuit such that the two-sided differential-mode voltage gain is $A_{d1} = (v_{o2} - v_{o1})/(v_1 - v_2) = 20$ for the first stage, and that the one-sided differential-mode voltage gain is $A_{d2} = v_{o3}/(v_{o2} - v_{o1}) = 30$ for the second stage. The circuit is to be designed such that the maximum differential-mode voltage swing is obtained in each stage.

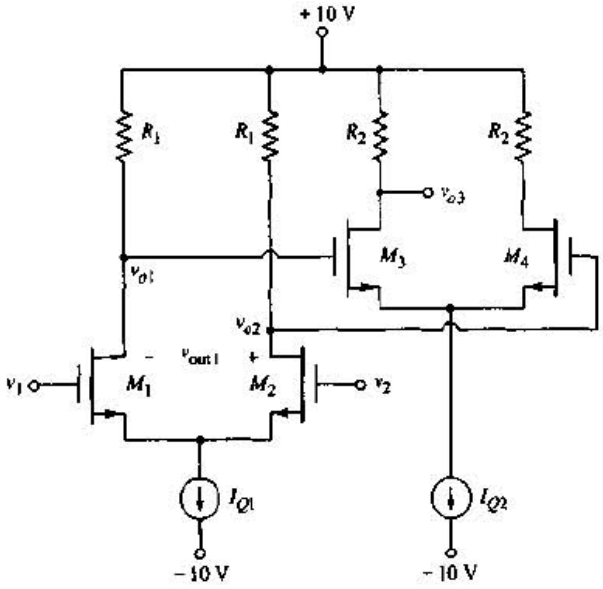


Figure P11.34

***11.35** Figure P11.35 shows a matched JFET differential pair biased with a current source I_Q. (a) Starting with

$$i_D = I_{DSS}\left(1 - \frac{v_{GS}}{V_p}\right)^2$$

show that

$$\frac{i_{D1}}{I_Q} = \frac{1}{2} + \left(\frac{1}{-2V_p}\right)v_d\sqrt{2\left(\frac{I_{DSS}}{I_Q}\right) - \left(\frac{I_{DSS}}{I_Q}\right)^2\left(\frac{v_d}{V_p}\right)^2}$$

and

$$\frac{i_{D2}}{I_Q} = \frac{1}{2} - \left(\frac{1}{-2V_p}\right)v_d\sqrt{2\left(\frac{I_{DSS}}{I_Q}\right) - \left(\frac{I_{DSS}}{I_Q}\right)^2\left(\frac{v_d}{V_p}\right)^2}$$

(b) Show that the I_Q bias current is switched entirely to one transistor or the other when

$$|v_d| = |V_P|\sqrt{\frac{I_Q}{I_{DSS}}}$$

(c) Show that the maximum forward transconductance is given by

$$g_f(\max) = \left.\frac{di_{D1}}{dv_d}\right|_{v_d=0} = \left(\frac{1}{-V_P}\right)\sqrt{\frac{I_Q \cdot I_{DSS}}{2}}$$

11.36 A JFET differential amplifier is shown in Figure P11.36. The transistor parameters are: $V_P = -4\,\text{V}$, $I_{DSS} = 2\,\text{mA}$, and $\lambda = 0$. (a) Find R_D and I_Q such that $I_{D1} = I_{D2} = 0.5\,\text{mA}$ and $v_{o2} = 7\,\text{V}$ when $v_1 = v_2 = 0$. (b) Calculate the maximum forward transconductance. (c) Determine the one-sided differential-mode voltage gain $A_d = v_o/v_d$.

***11.37** Consider the JFET diff-amp shown in Figure P11.37. The transistor parameters are: $I_{DSS} = 0.8\,\text{mA}$, $\lambda = 0.02\,\text{V}^{-1}$, and $V_P = -2\,\text{V}$. (a) Determine I_S, I_{D1}, I_{D2}, and v_{o2} for $v_1 = v_2 = 0$. (b) Using the small-signal equivalent circuit, determine the differential-mode voltage gain $A_d = v_{o2}/v_d$, the common-mode voltage gain $A_{cm} = v_o/v_{cm}$, and the CMRR_{dB}.

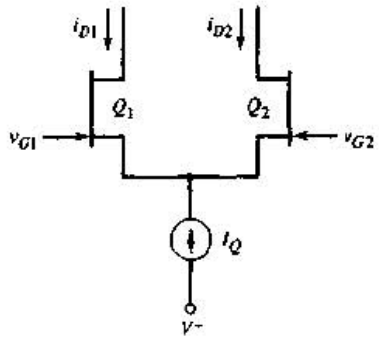


Figure P11.35

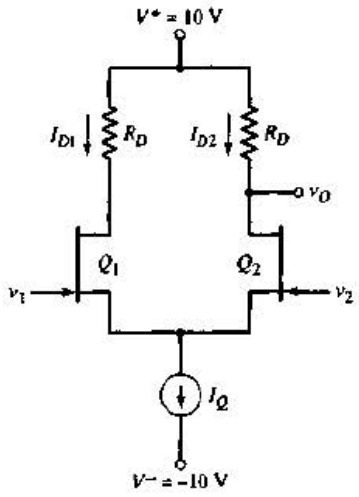


Figure P11.36

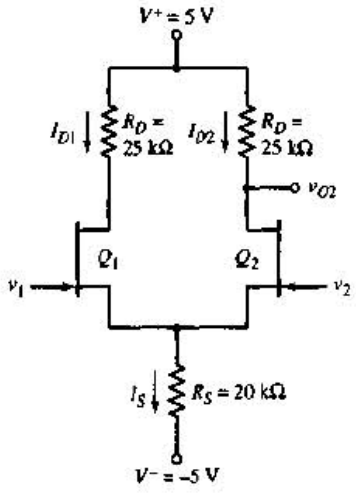


Figure P11.37

***11.38** Consider the circuit in Figure P11.38. Assume that $\lambda = 0$ for the transistors, and assume an ideal current source I_Q. Derive the expressions for the one-sided differential-mode gains $A_{d1} = v_{o1}/v_d$ and $A_{d2} = v_{o2}/v_d$, and for the two-sided differential-mode gain $A_d = (v_{o2} - v_{o1})/v_d$.

Section 11.4 Differential Amplifier with Active Load

***11.39** Consider the diff-amp with active load in Figure P11.39. The Early voltages are $V_{AN} = 120\,\text{V}$ for Q_1 and Q_2 and $V_{AP} = 80\,\text{V}$ for Q_3 and Q_4. (a) Determine the open-circuit differential-mode voltage gain. (b) Compare this value to the gain obtained when $R = 0$. (c) Determine the output resistance R_o for parts (a) and (b).

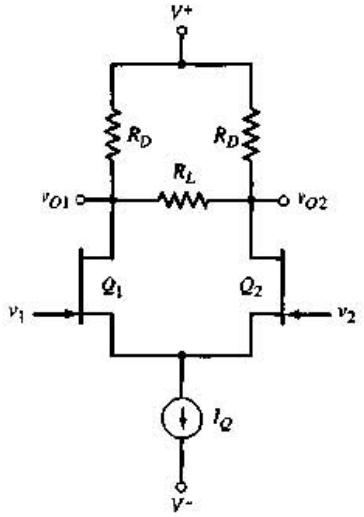


Figure P11.38

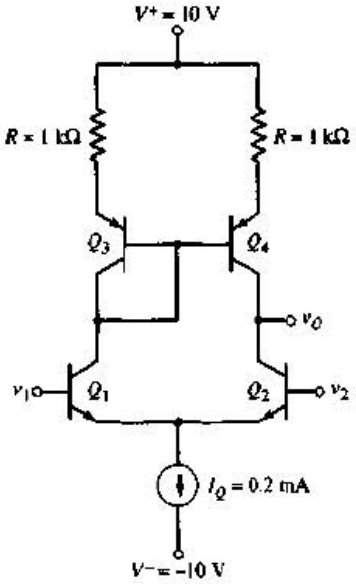


Figure P11.39

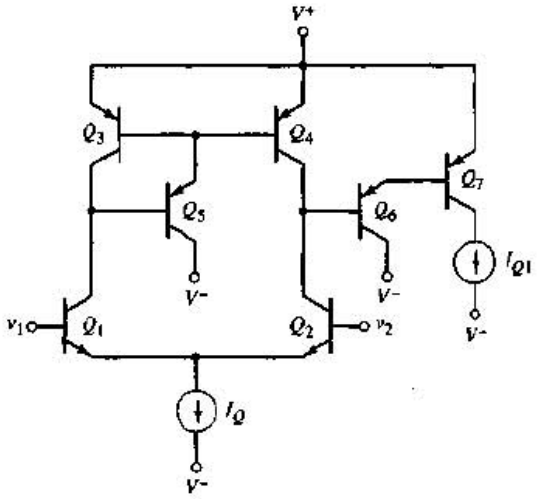


Figure P11.40

11.40 The diff-amp in Figure P11.40 has a three-transistor active load circuit and a Darlington pair configuration connected to the output. Determine the bias current I_{Q1} in terms of I_Q such that the diff-amp dc currents are balanced.

11.41 For the diff-amp in Figure 11.30, the parameters are: $V^+ = 10\,\text{V}$, $V^- = -10\,\text{V}$, and $I_Q = 0.8\,\text{mA}$. The transistor parameters are: $\beta = 150$, $V_{A1} = V_{A2} = 150\,\text{V}$, and $V_{A3} = V_{A4} = 100\,\text{V}$. (a) Determine the open-circuit differential-mode voltage gain. (b) Find the load resistance R_L that will reduce the differential-mode voltage gain to one-half the open-circuit value.

***11.42** Consider the circuit in Figure P11.42, in which the input transistors to the diff-amp are Darlington pairs. Assume transistor parameters of β(npn) = 120, β(pnp) = 80, V_A(npn) = 100 V, and V_A(pnp) = 80V. Let the power supply voltages be ±10 V and let

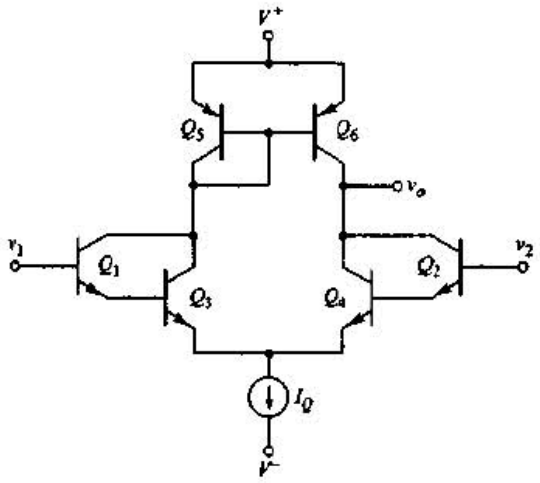


Figure P11.42

$I_Q = 1\,\text{mA}$. (a) Determine the output resistance R_o. (b) Calculate the differential-mode voltage gain. (c) Find the differential-mode input resistance R_{id}.

***D11.43** Design a differential amplifier as shown in Figure 11.28 incorporating a basic two-transistor current source to establish I_Q. The bias voltages are $V^+ = 15\,\text{V}$ and $V^- = -15\,\text{V}$, the transistor parameters are $\beta = 180$ and $V_A = 100\,\text{V}$, and the maximum forward transconductance is to be $8\,\text{mA/V}$. (a) Show the complete circuit, with all component values. (b) What are the values of open-circuit differential-mode voltage gain, differential-mode input resistance, and output resistance? (c) Determine the common-mode input voltage range and the common-mode input resistance.

11.44 The differential amplifier shown in Figure P11.44 has a pair of pnp bipolars as input devices and a pair of npn bipolars connected as an active load. The circuit bias is $I_Q = 0.2\,\text{mA}$, and the transistor parameters are $\beta = 100$ and $V_A = 100\,\text{V}$. (a) Determine I_O such that the dc currents in the diff-amp are balanced. (b) Find the open-circuit differential-mode voltage gain. (c) Determine the differential-mode voltage gain if a load resistance $R_L = 250\,\text{k}\Omega$ is connected to the output.

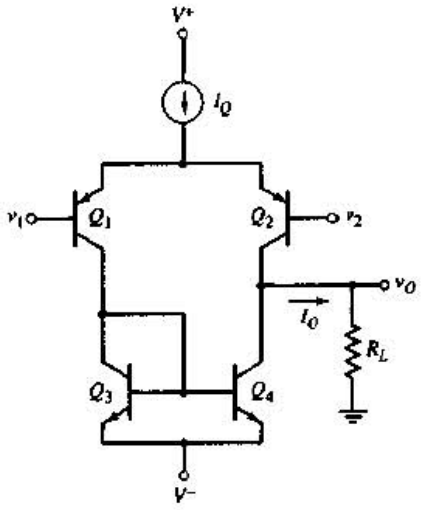


Figure P11.44

***11.45** Reconsider the circuit in Figure P11.44 except that 1 kΩ resistors are inserted at the emitters of the active load transistors Q_3 and Q_4 as in the circuit in Figure P11.39. Assume the same transistor parameters as in Problem 11.44. (a) Determine the output resistance looking into the output of the diff-amp circuit. (b) Find the open-circuit differential-mode voltage gain.

***D11.46** For the transistors in the diff-amp circuit in Figure 11.30 the parameters are: $\beta = 150$, $V_{A1} = V_{A2} = 125\,\text{V}$, and $V_{A3} = V_{A4} = 80\,\text{V}$. The supply voltages are $V^+ = 10\,\text{V}$ and $V^- = -10\,\text{V}$, and the maximum current source available is $I_Q = 2\,\text{mA}$. A load resistance of $R_L = 200\,\text{k}\Omega$ is connected to the output. (a) Design the circuit such that the differential-mode voltage gain is 1000. (b) If $V_{BE}(\text{on}) = 0.6\,\text{V}$, what is the maximum possible common-mode input voltage that can be applied to the circuit?

D11.47 Design a BJT diff-amp with an active load similar to the configuration in Figure P11.42 except that the input devices are to be pnp transistors and the active load will have npn transistors. Using the same parameters as in Problem 11.42, determine the small-signal differential-mode voltage gain.

11.48 The differential amplifier in Figure P11.48 has a pair of PMOS transistors as input devices and a pair of NMOS transistors connected as an active load. The circuit is biased with $I_Q = 0.2\,\text{mA}$, and the transistor parameters are: $K_n = K_p = 0.1\,\text{mA/V}^2$, $\lambda_n = 0.01\,\text{V}^{-1}$, $\lambda_p = 0.015\,\text{V}^{-1}$, $V_{TN} = 1\,\text{V}$, and $V_{TP} = -1\,\text{V}$. (a) Determine the quiescent drain-to-source voltage in each transistor. (b) Find the open-circuit differential-mode voltage gain. (c) What is the output resistance?

11.49 For the differential amplifier in Figure 11.32, the parameters are: $V^+ = 5\,\text{V}$, $V^- = -5\,\text{V}$, and $I_Q = 0.15\,\text{mA}$. The PMOS parameters are: $K_p = 100\,\mu\text{A/V}^2$, $\lambda_p = 0.02\,\text{V}^{-1}$, and $V_{TP} = -0.8\,\text{V}$. The NMOS parameters are: $K_n = 120\,\mu\text{A/V}^2$, $\lambda_n = 0.015\,\text{V}^{-1}$, and $V_{TN} = +0.8\,\text{V}$. Determine the differential-mode voltage gain $A_d = v_o/v_d$.

***11.50** Consider the diff-amp in Figure P11.50. The PMOS parameters are: $K_p = 80\,\mu\text{A/V}^2$, $\lambda_p = 0.02\,\text{V}^{-1}$, $V_{TP} = -2\,\text{V}$. The NMOS parameters are: $K_n = 80\,\mu\text{A/V}^2$, $\lambda_n = 0.015\,\text{V}^{-1}$, $V_{TN} = +2\,\text{V}$. (a) Determine the open-circuit differential-mode voltage

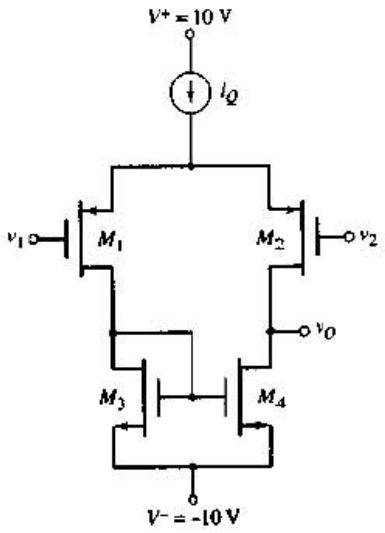


Figure P11.48

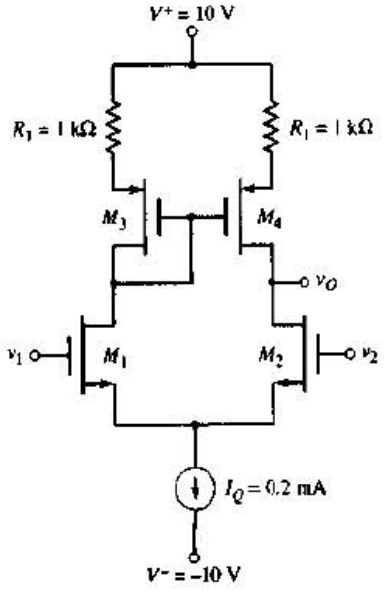


Figure P11.50

gain. (b) Compare this value to the gain obtained when $R_1 = 0$. (c) What is the output resistance of the diff-amp for parts (a) and (b)?

D11.51 Reconsider the diff-amp specifications listed in Problem 11.26. (a) Design an all-CMOS diff-amp with the configuration in Figure 11.32 to meet the specifications. Assume NMOS parameters of $V_{TN} = 0.8\,\text{V}$, $k_n' = 80\,\mu\text{A/V}^2$, and $\lambda_n = 0.02\,\text{V}^{-1}$ and PMOS parameters of $V_{TP} = -0.8\,\text{V}$, $k_p' = 35\,\mu\text{A/V}^2$, and $\lambda_p = 0.025\,\text{V}^{-1}$. (b) Determine the common-mode voltage gain using a computer simulation.

D11.52 Design an all-CMOS diff-amp, including the current source circuit, with the configuration in Figure 11.32 to have a differential-mode voltage gain of $A_d = 80$. The circuit is to be biased at $\pm 3\,\text{V}$ and the total power dissipated in the circuit is to be no more than 0.5 mW. The available transistors have parameters of $V_{TN} = 0.4\,\text{V}$, $k_n' = 80\,\mu\text{A/V}^2$, $\lambda_n = 0.015\,\text{V}^{-1}$, $V_{TP} = -0.4\,\text{V}$, $k_p' = 40\,\mu\text{A/V}^2$, and $\lambda_p = 0.02\,\text{V}^{-1}$. Verify the differential-mode voltage gain of the design with a computer simulation. Also, determine the common-mode gain with a computer simulation.

RD11.53 Redesign the cascode active load CMOS diff-amp in Figure 11.36 to achieve a differential-mode voltage gain of $A_d = 400$. Assume $k_n' = 80\,\mu\text{A/V}^2$ and $k_p' = 40\,\mu\text{A/V}^2$ and use other transistor parameters described in Example 11.15.

***11.54** Consider the fully cascoded diff-amp in Figure 11.37. Assume $I_Q = 80\,\mu\text{A}$ and transistor parameters of: $V_{TN} = 0.8\,\text{V}$, $k_n' = 60\,\mu\text{A/V}^2$, $\lambda_n = 0.015\,\text{V}^{-1}$, $V_{TP} = -0.8\,\text{V}$, $k_p' = 25\,\mu\text{A/V}^2$, and $\lambda_p = 0.02\,\text{V}^{-1}$. The transistor width-to-length ratios are $W/L = 60/4$ for transistors M_1–M_4, $W/L = 40/4$ for transistors M_5–M_6, and $W/L = 4/4$ for transistors M_7–M_8. (a) Determine the output resistance of the diff-amp. (b) Calculate the differential-mode voltage gain of the diff-amp. (c) Find the common-mode voltage gain of the diff-amp using a computer simulation.

Section 11.5 BiCMOS Circuits

11.55 The Darlington pair circuit in Figure 11.45 has new bias current levels of $I_{BIAS1} = 0.25\,\text{mA}$ and $I_{BIAS2} = 1\,\text{mA}$. The transistor parameters are: $K_n = 0.2\,\text{mA/V}^2$, $V_{TN} = 1\,\text{V}$, and $\lambda = 0$ for M_1; and $\beta = 120$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, and $V_A = \infty$ for Q_2. Determine the small-signal parameters for each transistor, and find the composite transconductance.

11.56 Consider the BiCMOS diff-amp in Figure 11.44, biased at $I_Q = 0.4\,\text{mA}$. The transistor parameters for M_1 and M_2 are: $K_n = 0.2\,\text{mA/V}^2$, $V_{TN} = 1\,\text{V}$, and $\lambda = 0.01\,\text{V}^{-1}$. The parameters for Q_1 and Q_2 are: $\beta = 120$, $V_{EB}(\text{on}) = 0.7\,\text{V}$, and $V_A = 80\,\text{V}$. (a) Determine the differential-mode voltage gain. (b) If the output resistance of the current source is $R_o = 500\,\text{k}\Omega$, determine the common-mode voltage gain using a computer simulation analysis.

***11.57** The BiCMOS circuit in Figure P11.57 is equivalent to a pnp bipolar transistor with an infinite input impedance. The bias current is $I_Q = 900\,\mu\text{A}$. The transistor parameters are: $K_p = 1\,\text{mA/V}^2$, $V_{TP} = -1\,\text{V}$, and $\lambda = 0$ for M_1; and $\beta = 100$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, and $V_A = \infty$ for Q_2. (a) Sketch the small-signal equivalent circuit. (b) Determine the small-signal parameters for each transistor. (c) Determine the small-signal voltage gain $A_v = v_o/v_i$.

***11.58** Consider the BiCMOS circuit in Figure P11.57. The bias current is $I_Q = 1.2\,\text{mA}$, and the transistor parameters are the same as described in Problem 11.57. (a) Determine the small-signal transistor parameters. (b) Find the output impedance R_o.

***11.59** The bias current I_Q is $25\,\mu\text{A}$ in each circuit in Figure P11.59. The BJT parameters are $\beta = 100$ and $V_A = 50\,\text{V}$, and the MOSFET parameters are $V_{TN} = 0.8\,\text{V}$, $K_n = 0.25\,\text{mA/V}^2$, and $\lambda = 0.02\,\text{V}^{-1}$. Assume the two amplifying transistors M_1 and

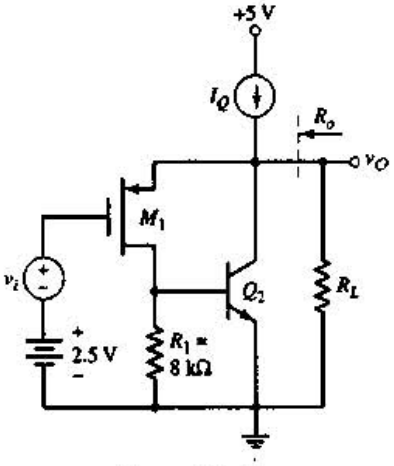


Figure P11.57

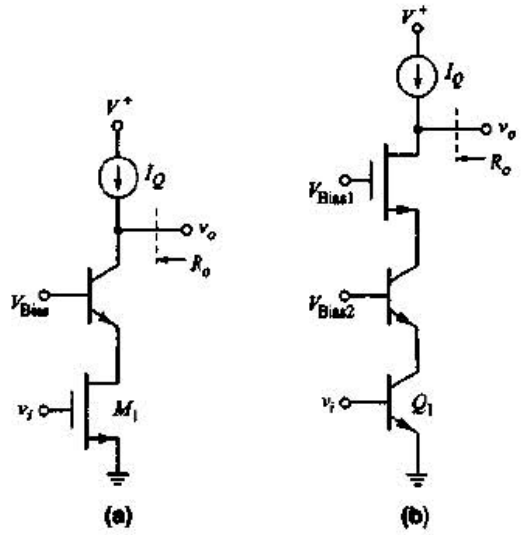


Figure P11.59

Q_1 are biased in the saturation region and forward-active region, respectively. Determine the small-signal voltage gain $A_v = v_o/v_i$ and the output resistance R_o for each circuit.

11.60 For the circuit shown in Figure P11.60, determine the small-signal voltage gain, $A_v = v_o/v_i$. Assume transistor parameters of $V_{TN} = 1\,\text{V}$, $K_n = 0.2\,\text{mA/V}^2$, and $\lambda = 0$ for M_1 and $\beta = 80$ and $V_A = \infty$ for Q_1.

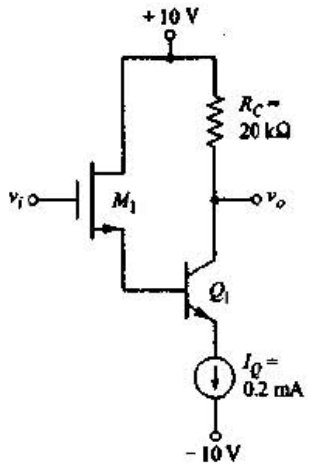


Figure P11.60

Section 11.6 Gain Stage and Simple Output Stage

11.61 Consider the circuit in Figure P11.61. The output stage is a Darlington pair emitter-follower configuration. Assume $\beta = 100$ for all transistors, and let $V_A = 100\,\text{V}$ for Q_7 and Q_{11}. Determine the output resistance R_o.

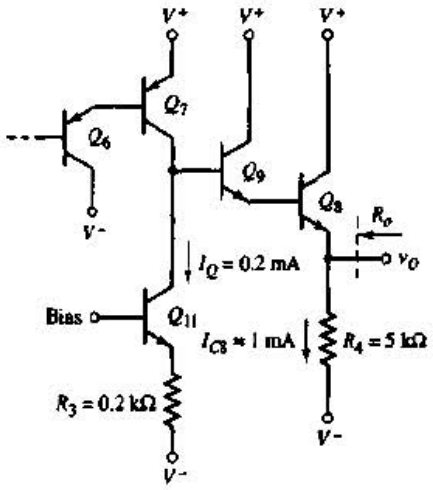


Figure P11.61

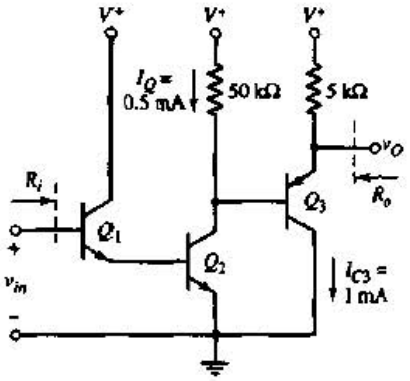


Figure P11.62

***11.62** For the circuit in Figure P11.62, the transistor parameters are $\beta = 100$ and $V_A = \infty$. The bias currents in the transistors are indicated on the figure. Determine the input resistance R_i, the output resistance R_o, and the small-signal voltage gain $A_v = v_o/v_{in}$.

11.63 Consider the circuit in Figure P11.63. The bias currents I_1 and I_2 are such that a zero dc output voltage is established. The transistor parameters are: $K_p = 0.2\,\text{mA/V}^2$, $K_n = 0.5\,\text{mA/V}^2$, $V_{TP} = -0.8\,\text{V}$, $V_{TN} = +0.8\,\text{V}$, and $\lambda_n = \lambda_p = 0.01\,\text{V}^{-1}$. Determine the small-signal voltage gain $A_v = v_o/v_{in}$ and the output resistance R_o.

11.64 The circuit shown in Figure P11.64 has bias currents $I_1 = 0.1\,\text{mA}$ and $I_2 = 0.5\,\text{mA}$. The transistor parameters are: $K_n = 100\,\mu\text{A/V}^2$, $K_p = 250\,\mu\text{A/V}^2$, $V_{TN} = 1\,\text{V}$, $V_{TP} = -1\,\text{V}$, and $\lambda_n = \lambda_p = 0.01\,\text{V}^{-1}$. (a) Determine the resistor values R_1 and R_2 such that the dc value of the output voltage is zero. (b) Find the small-signal voltage gain $A_v = v_o/v_{in}$ and the output resistance R_o.

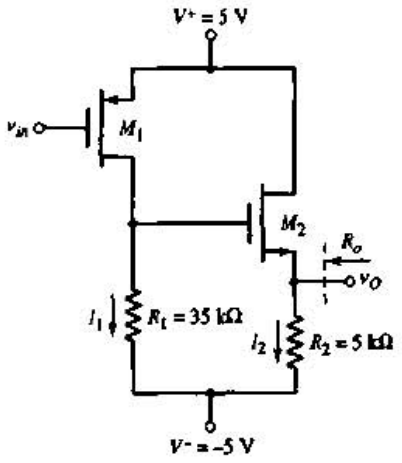


Figure P11.63

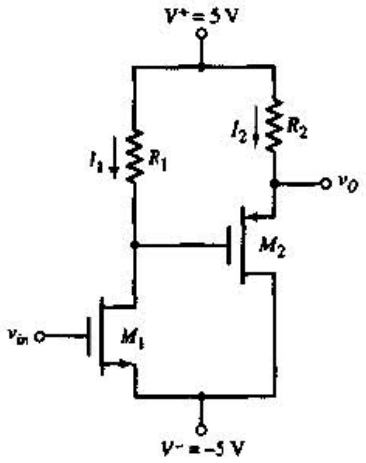


Figure P11.64

Section 11.7 Simplified Op-Amp Circuits

***11.65** Consider the multistage bipolar circuit in Figure P11.65, in which base currents are negligible. Assume the transistor parameters are: $\beta = 100$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, and $V_A = \infty$. The output resistance of the constant-current source is $R_o = 100\,\text{k}\Omega$. (a) For $v_1 = v_2 = 0$, design the circuit such that: $v_{o2} = 2\,\text{V}$, $v_{o3} = 3\,\text{V}$, $v_o = 0$, $I_{CQ3} = 0.5\,\text{mA}$, and $I_{CQ4} = 3\,\text{mA}$. (b) Determine the differential-mode voltage gains $A_{d1} = v_{o2}/v_d$ and $A_d = v_o/v_d$. (c) Determine the common-mode voltage gains $A_{cm1} = v_{o2}/v_{cm}$ and $A_{cm} = v_o/v_{cm}$, and the overall CMRR_{dB}.

***D11.66** The circuit in Figure P11.66 has two bipolar differential amplifiers in cascade, biased with ideal current sources I_{Q1} and I_{Q2}. Assume the transistor parameters are $\beta = 180$ and $V_A = \infty$. (a) Design the circuit such that $v_{o1} = v_{o2} = 2\,\text{V}$ and $v_{O4} = 6\,\text{V}$ when $v_1 = v_2 = 0$. (b) Determine the differential-mode voltage gains $A_{d1} = (v_{o1} - v_{o2})/v_d$ and $A_d = v_{o4}/v_d$.

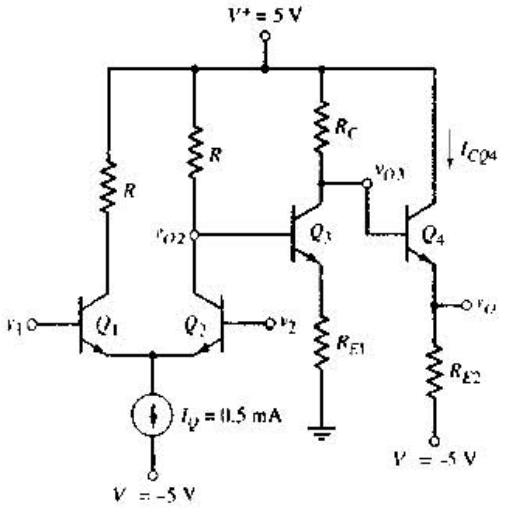


Figure P11.65

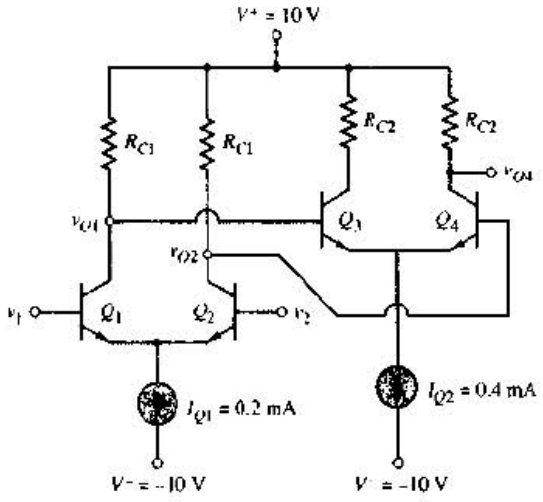


Figure P11.66

***11.67** The transistor parameters for the circuit in Figure P11.67 are: $\beta = 200$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, and $V_A = 80\,\text{V}$. (a) Determine the differential-mode voltage gain $A_d = v_{o3}/v_d$ and the common-mode voltage gain $A_{cm} = v_{o3}/v_{cm}$. (b) Determine the output voltage v_{o3} if $v_1 = 2.015\sin\omega t\,\text{V}$ and $v_2 = 1.985\sin\omega t\,\text{V}$. Compare this output to the ideal output that would be obtained if $A_{cm} = 0$. (c) Find the differential-mode and common-mode input resistances.

***11.68** For the transistors in the circuit in Figure P11.68, the parameters are: $K_n = 0.2\,\text{mA/V}^2$, $V_{TN} = 2\,\text{V}$, and $\lambda = 0.02\,\text{V}^{-1}$. (a) Determine the differential-mode voltage gain $A_d = v_{o3}/v_d$ and the common-mode voltage gain $A_{cm} = v_{o3}/v_{cm}$. (b) Determine the output voltage v_{o3} if $v_1 = 2.15\sin\omega t\,\text{V}$ and $v_2 = 1.85\sin\omega t\,\text{V}$. Compare this output to the ideal output that would be obtained if $A_{cm} = 0$.

Section 11.8 Diff-Amp Frequency Response

11.69 Consider the differential amplifier in Figure 11.49(a), with parameters: $I_Q = 1\,\text{mA}$, $R_C = 10\,\text{k}\Omega$, and $R_B = 0.5\,\text{k}\Omega$. The transistor parameters are: $\beta = 100$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, $V_A = \infty$, $C_\pi = 8\,\text{pF}$, and $C_\mu = 2\,\text{pF}$. Determine the low-frequency

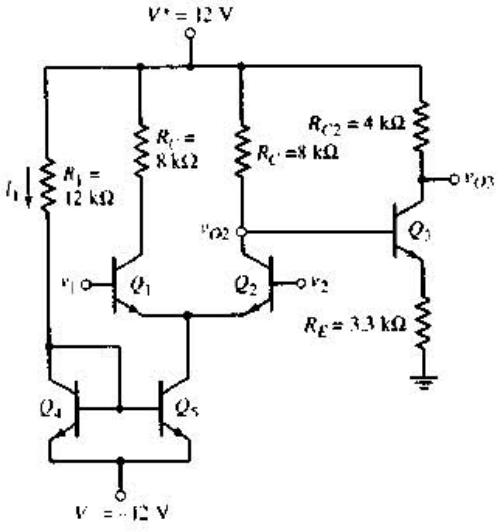


Figure P11.67

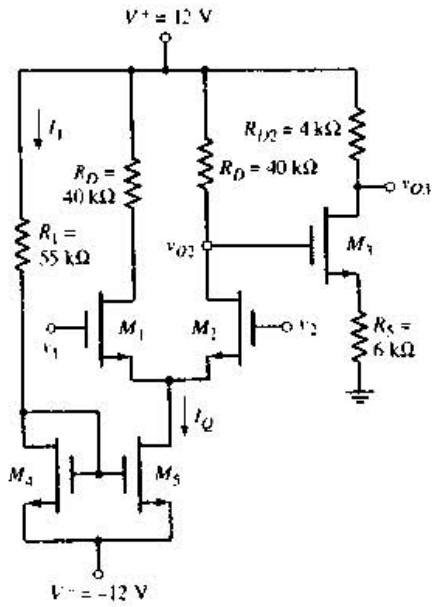


Figure P11.68

differential-mode gain and the upper 3 dB frequency. What is the equivalent Miller capacitance of each transistor?

11.70 The differential amplifier in Figure 11.50(a) has the same circuit and transistor parameters as in Problem 11.69. The equivalent impedance parameters of the current source are $R_o = 5\,\text{M}\Omega$ and $C_o = 0.8\,\text{pF}$. (a) Determine the frequency of the zero in the common-mode gain. (b) Plot CMRR_{dB} versus frequency, showing the frequencies f_z and f_H.

11.71 A BJT diff-amp is biased with a current source $I_Q = 2\,\text{mA}$, and the circuit parameters are $R_C = 10\,\text{k}\Omega$ and $R_B = 1\,\text{k}\Omega$. The transistor paramaters are: $\beta = 120$, $f_T = 800\,\text{MHz}$, and $C_\mu = 1\,\text{pF}$. (a) Determine the upper 3dB frequency of the differential-mode gain. (b) If the current source impedance parameters are $R_o = 10\,\text{M}\Omega$ and $C_o = 1\,\text{pF}$, find the frequency of the zero in the common-mode gain.

11.72 Consider the diff-amp in Figure 11.54. The circuit and transistor parameters are the same as in Problem 11.69. For a one-sided output at v_{o2}, determine the differential-mode gain for: (a) $R_E = 100\,\Omega$, and (b) $R_E = 250\,\Omega$.

COMPUTER SIMULATION PROBLEMS

11.73 For the transistors in the circuit in Figure P11.73, the parameters are: $\beta = 100$, $I_S = 2 \times 10^{-15}\,\text{A}$, and $V_A = 100\,\text{V}$. From a PSpice analysis, determine: (a) the quiescent currents I_1, I_Q, I_{C1}, and I_{C2}, and (b) the differential- and common-mode gains for (i) $R_L = 10\,\text{M}\Omega$, and (ii) $R_L = 200\,\text{k}\Omega$.

11.74 Consider the circuit in Figure P11.74. The transistor parameters are: $V_{TN} = 2\,\text{V}$ (all NMOS devices), $V_{TP} = -2\,\text{V}$ (all PMOS devices), $K_{n5} = K_{n6} = 50\,\mu\text{A/V}^2$, $K_{n7} = K_{n8} = 200\,\mu\text{A/V}^2$, $K_{n1} = K_{n2} = K_{p3} = K_{p4} = 100\,\mu\text{A/V}^2$, and $\lambda = 0.01\,\text{V}^{-1}$ (all devices). From a computer analysis, determine: (a) the quiescent currents I_1 and I_Q, and (b) the differential- and common-mode gains for (i) $R_L = 10\,\text{M}\Omega$ and (ii) $R_L = 400\,\text{k}\Omega$.

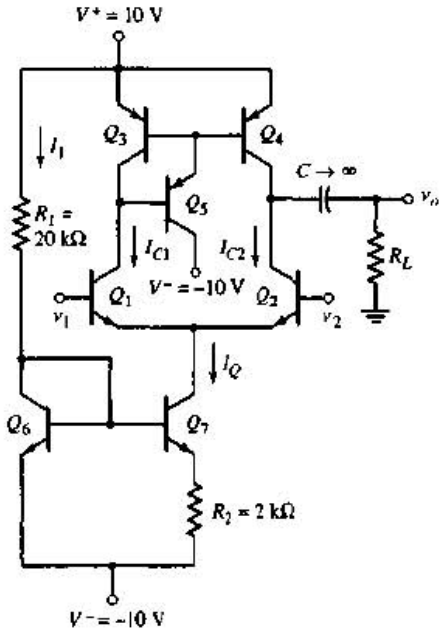


Figure P11.73

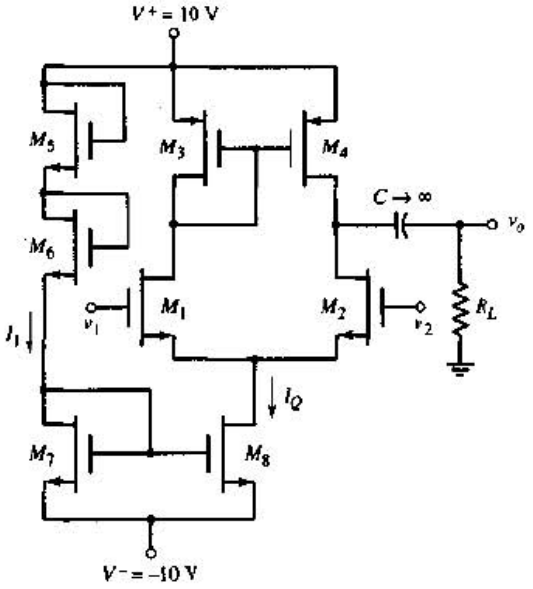


Figure P11.74

11.75 For the circuit in Figure 11.46 the parameters are: $V^+ = 10\,\text{V}$, $V^- = -10\,\text{V}$, $R_1 = 19\,\text{k}\Omega$, $R_2 = R_3 = 0.2\,\text{k}\Omega$, and $R_4 = 10\,\text{k}\Omega$. The transistor parameters are: $\beta = 100$, $I_S = 2 \times 10^{-15}\,\text{A}$, and $V_A = 100\,\text{V}$. (a) From a computer analysis, determine the quiescent currents I_1, I_Q, I_{C1}, I_{C2}, I_{B5}, I_O, and I_{C7}. (b) Also from a computer analysis, determine the input resistance R_i, output resistance R_o, and voltage gain $A_v = v_o/v_{o2}$. (c) Compare these results to those obtained in Examples 11.16 and 11.17.

11.76 Consider the circuit in Figure P11.67, with circuit and transistor parameters described in Problem 11.67. Let $I_S = 2 \times 10^{-15}\,\text{A}$. From a computer analysis, determine: (a) the differential-mode voltage gain, (b) the common-mode voltage gain, (c) the input differential-mode resistance, and (d) the input common-mode resistance.

11.77 Consider the diff-amp described in Problems 11.69 and 11.70. Using a computer analysis, determine the CMRR_{dB} versus frequency characteristic.

DESIGN PROBLEMS

[Note: Each design is to be correlated with a computer simulation analysis.]

***D11.78** Design a basic BJT diff-amp with an active load, to provide an open-circuit differential-mode gain of $|A_d| = 2000$ and a common-mode rejection ratio of $\text{CMRR}_{\text{dB}} = 80\,\text{dB}$. Specify the bias currents, minimum Early voltage, and minimum output impedance of the current source. Design the current source to achieve the specified output impedance.

***D11.79** Design a basic MOSFET diff-amp with an active load, to provide an open-circuit differential-mode gain of $|A_d| = 200$ and a common-mode rejection ratio of $\text{CMRR}_{\text{dB}} = 70\,\text{dB}$. Specify the bias currents, conduction parameter values, minimum λ values, and minimum output impedance of the current source. Design the current source to achieve the specified output impedance specification.

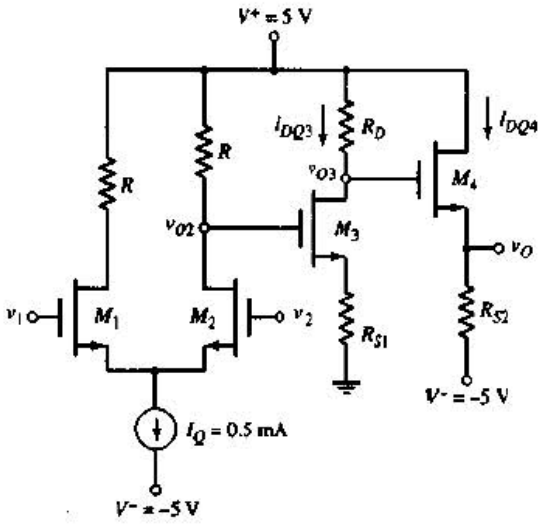


Figure P11.82

***D11.80** Consider the BiCMOS diff-amp in Figure 11.44. Design the circuit to provide a differential-mode gain of $|A_d| = 500$ and a common-mode rejection ratio of $\text{CMRR}_{\text{dB}} = 70\,\text{dB}$. Specify the bias currents, MOSFET conduction parameter values, minimum bipolar Early voltage, MOSFET λ values, and minimum output resistance of the current source. Design the current source to achieve this specified output resistance.

***D11.81** Consider the bipolar op-amp configuration in Figure 11.48. The bias voltages are $\pm 10\,\text{V}$, as shown, the current I_{R7} is to be $I_{R7} = 3\,\text{mA}$, and the maximum dc power dissipation in the circuit is to be 120 mW. The output voltage is to be $v_o = 0$ for $v_1 = v_2 = 0$. Design the circuit, using reasonable resistance and current values. What is the overall differential-mode voltage gain?

***D11.82** The transistor parameters for the circuit in Figure P11.82 are: $K_n = 0.2\,\text{mA/V}^2$, $V_{TN} = 0.8\,\text{V}$, and $\lambda = 0$. The output resistance of the constant-current source is $R_o = 100\,\text{k}\Omega$. (a) For $v_1 = v_2 = 0$, design the circuit such that: $v_{o2} = 2\,\text{V}$, $v_{o3} = 3\,\text{V}$, $v_o = 0$, $I_{DQ3} = 0.25\,\text{mA}$, and $I_{DQ} = 2\,\text{mA}$. (b) Determine the differential-mode gains $A_{d1} = v_{o2}/v_d$ and $A_d = v_o/v_d$. (c) Determine the common-mode voltage gains $A_{cm1} = v_{o2}/v_{cm}$ and $A_{cm} = v_o/v_{cm}$, and the overall CMRR_{dB}.

CHAPTER

12

Feedback and Stability

12.0 PREVIEW

Previously, we found that the small-signal voltage gain and other characteristics of discrete BJT and MOSFET transistor circuit amplifiers are functions of the bipolar current gain and the MOSFET conduction parameter. In general, these transistor parameters vary with temperature and they have a range of values for a given type of transistor group, because of processing and material property tolerances. This means that the Q-point, voltage gain, and other circuit properties can vary from one circuit to another, and can be functions of temperature.

Transistor circuit characteristics can be made essentially independent of the individual transistor parameters by using feedback. The feedback process takes a portion of the output signal and returns it to the input to become part of the input excitation. We previously encountered feedback in our study of ideal op-amps and op-amp circuits. For example, resistors are connected between the output and input terminals of an ideal op-amp to form a feedback network. The voltage gain of these ideal circuits is a function only of the ratio of resistors and not of any individual transistor parameters. In this chapter, we formally study feedback and feedback circuits.

We begin the chapter by presenting general feedback theory and determining general properties of feedback circuits. We then analyze the four basic ideal feedback configurations. For each type of feedback topology, the output-to-input signal transfer function is determined and the expressions for input and output resistances are derived. We analyze various op-amp and discrete transistor circuits representing each of the four basic feedback configurations, and compare the transfer functions, input resistance, and output resistances to the ideal theory. Principal goals of this chapter are to understand the characteristics of the various types of feedback configurations to be able to determine the type of feedback circuit required for a specific design application and to design a stable feedback amplifier.

12.1 INTRODUCTION TO FEEDBACK

Feedback is used in virtually all amplifier systems. Harold Black, an electronics engineer with the Western Electric Company, invented the feedback amplifier

in 1928 while searching for methods to stabilize the gain of amplifiers for use in telephone repeaters. In a feedback system, a signal that is proportional to the output is fed back to the input and combined with the input signal to produce a desired system response. As we will see, external feedback is used deliberately to achieve particular system benefits. However, feedback may be unintentional and an undesired system response may be produced.

We have already seen examples of feedback in previous chapters, although the term feedback may not have been used. For example, in Chapters 3 and 5 we introduced resistors at the emitter of BJT common-emitter circuits and at the source of MOSFET common-source circuits to stabilize the Q-point against variations in transistor parameters. This technique introduces *negative feedback* in the circuit. An increase in collector or drain current produces an increase in the voltage across these resistors which produces a decrease in the base-emitter or gate-source voltage. The decrease in these device voltages tends to reduce or oppose the change in collector or drain current. Opposition to change is suggested by use of the term negative feedback.

Feedback can be either negative or positive. In **negative feedback**, a portion of the output signal is subtracted from the input signal; in **positive feedback**, a portion of the output signal is added to the input signal. Negative feedback, for example, tends to maintain a constant value of amplifier voltage gain against variations in transistor parameters, supply voltages, and temperature. Positive feedback is used in the design of oscillators and in a number of other applications. In this chapter, we will concentrate on negative feedback.

12.1.1 Advantages and Disadvantages of Negative Feedback

Before we actually get into the analysis and design of feedback circuits, we will list some of the advantages and disadvantages of negative feedback. Although these characteristics and properties of negative feedback are not obvious at this point, they are listed here so that the reader can anticipate these results during the derivations and analysis.

Advantages

1. *Gain sensitivity.* Variations in the circuit transfer function (gain) as a result of changes in transistor parameters are reduced by feedback. This reduction in sensitivity is one of the most attractive features of negative feedback.
2. *Bandwidth extension.* The bandwidth of a circuit that incorporates negative feedback is larger than that of the basic amplifier.
3. *Noise sensitivity.* Negative feedback may increase the signal-to-noise ratio if noise is generated within the feedback loop.
4. *Reduction of nonlinear distortion.* Since transistors have nonlinear characteristics, distortion may appear in the output signals, especially at large signal levels. Negative feedback reduces this distortion.
5. *Control of impedance levels.* The input and output impedances can be increased or decreased with the proper type of negative feedback circuit.

Disadvantages

1. *Circuit gain.* The overall amplifier gain, with negative feedback, is reduced compared to the basic amplifier used in the circuit.
2. *Stability.* There is a possibility that the feedback circuit may become unstable (oscillate) at high frequencies.

These advantages and disadvantages will be further discussed as we develop the feedback theory.

In the course of our discussion, we will analyze several feedback circuits, in both discrete and op-amp circuit configurations. First, however, we will consider the ideal feedback theory and derive the general characteristics of feedback amplifiers. In this section, we discuss the ideal signal gain, gain sensitivity, bandwidth extension, noise sensitivity, and reduction of nonlinear distortion of a generalized feedback amplifier.

12.1.2 Use of Computer Simulation

Conventional methods of analysis that have been used in the previous chapters apply directly to feedback circuits. That is, the same dc analysis techniques and the same small-signal transistor equivalent circuits apply directly to feedback circuits in this chapter. However, in the analysis of feedback circuits, several simultaneous equations can be obtained, the time involved may be quite long and the probability of introducing errors may become almost certain.

Therefore, computer simulation of feedback circuits may prove to be very useful and is used fairly often throughout this chapter. As always, a word of warning is in order concerning computer simulation. Computer simulation does not replace basic understanding. It is important for the reader to understand the concepts and characteristics of the basic types of feedback circuits. Computer simulation is used only as a tool for obtaining specific results.

12.2 BASIC FEEDBACK CONCEPTS

Figure 12.1 shows the basic configuration of a feedback amplifier. In the diagram, the various signals S can be either currents or voltages. The circuit contains a basic amplifier with an open-loop gain A and a feedback circuit that samples the output signal and produces a feedback signal S_{fb}. The feedback signal is subtracted from the input source signal, which produces an error signal S_e. The error signal is the input to the basic amplifier and is the signal that is amplified to produce the output signal. The subtraction property produces the negative feedback.

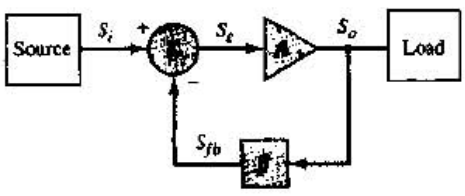


Figure 12.1 Basic configuration of a feedback amplifier

Implicit in the diagram in Figure 12.1 is the assumption that the input signal is transmitted through the amplifier only, none through the feedback network, and that the output signal is transmitted back through the feedback network only, none through the amplifier. Also, there are no loading effects in the ideal feedback system. The feedback network does not load down the output of the basic amplifier, and the basic amplifier and feedback network do not produce a loading effect on the input signal source. In actual feedback circuits, these assumptions and conditions are not entirely accurate. We will see later how nonideal conditions change the characteristics of actual feedback circuits with respect to those of the ideal feedback network.

12.2.1 Ideal Closed-Loop Signal Gain

From Figure 12.1, the output signal is

$$S_o = AS_\varepsilon \tag{12.1}$$

where A is the **amplification factor**, and the feedback signal is

$$S_{fb} = \beta S_o \tag{12.2}$$

where β in this case is the **feedback transfer function.**[1] At the summing node, we have

$$S_\varepsilon = S_i - S_{fb} \tag{12.3}$$

where S_i is the input signal. Equation (12.1) then becomes

$$S_o = A(S_i - \beta S_o) = AS_i - \beta A S_o \tag{12.4}$$

Equation (12.4) can be rearranged to yield the **closed-loop transfer function**, or gain, which is

$$A_f = \frac{S_o}{S_i} = \frac{A}{(1 + \beta A)} \tag{12.5}$$

As mentioned, signals S_i, S_o, S_{fb}, and S_ε can be either currents or voltages; however, they do not need to be all voltages or all currents in a given feedback amplifier. In other words, there may be a combination of current and voltage signals in the same circuit.

Equation (12.5) can be written

$$A_f = \frac{A}{(1 + \beta A)} = \frac{A}{1 + T} \tag{12.6}$$

where $T = \beta A$ is the **loop gain**. For negative feedback, we assume T to be a positive real factor. We will see later that the loop gain can become a complex function of frequency, but for the moment, we will assume that T is positive for negative feedback. We will also see that in some cases the gain will be negative (180 degree phase difference between input and output signals) which means

[1] In this chapter, β is the feedback transfer function, rather than the transistor current gain. The parameter h_{FE} will be used as the transistor current gain. Normally, h_{FE} indicates the dc current gain and h_{fe} indicates the ac current gain. However, as usual, we neglect any difference between the two parameters and assume $h_{FE} = h_{fe}$.

that the feedback transfer function β will also be a negative quantity for a negative feedback circuit.

Combining Equations (12.1) and (12.2), we obtain the loop gain relationship

$$T = A\beta = \frac{S_{fb}}{S_\epsilon} \tag{12.7}$$

Normally, the error signal is small, so the expected loop gain is large. If the loop gain is large so that $\beta A \gg 1$, then, from Equation (12.6), we have

$$A_f \cong \frac{A}{\beta A} = \frac{1}{\beta} \tag{12.8}$$

and the gain or transfer function of the feedback amplifier essentially becomes a function of the feedback network only.

The feedback circuit is usually composed of passive elements, which means that the feedback amplifier gain is almost completely independent of the basic amplifier properties, including individual transistor parameters. Since the feedback amplifier gain is a function of the feedback elements only, the closed-loop gain can be designed to be a given value. This property was demonstrated in Chapter 9, where we showed that the closed-loop gain of ideal op-amp circuits is a function of the feedback elements only. The individual transistor parameters may vary widely, and may depend on temperature and frequency, but the feedback amplifier gain is constant. The net results of negative feedback is stability in the amplifier characteristics.

In general, the magnitude and phase of the loop gain are functions of frequency, and they become important when we discuss the stability of feedback circuits.

Example 12.1 **Objective:** Calculate the feedback transfer function β, given A and A_f.

Case A:
Assume that the open-loop gain of a system is $A = 10^5$ and the closed-loop gain is $A_f = 50$.

Solution: From Equation (12.5), the closed-loop gain is

$$A_f = \frac{A}{(1 + \beta A)}$$

Therefore,

$$50 = \frac{10^5}{1 + \beta(10^5)}$$

which yields $\beta = 0.01999$ or $1/\beta = 50.025$.

Case B:
Now assume that the open-loop gain is $A = -10^5$ and the closed-loop gain is $A_f = -50$.

Solution: Again, from Equation (12.5), the closed-loop gain is

$$A_f = \frac{A}{(1 + \beta A)}$$

so that

$$-50 = \frac{-10^5}{1 + \beta(-10^5)}$$

which yields $\beta = -0.01999$ or $1/\beta = -50.025$.

Comment From these typical parameter values, we see that $A_f \cong 1/\beta$, as Equation (12.8) predicts. We also see that if the open-loop gain A is negative, then the closed-loop gain A_f and feedback transfer function β will also be negative for a negative feedback network.

Assuming a large loop gain, the output signal, from Equation (12.5), becomes

$$S_o = \left(\frac{A}{1 + \beta A}\right) S_i \cong \frac{1}{\beta} \cdot S_i \tag{12.9}$$

Substituting Equation (12.9) into (12.3), we obtain the error signal,

$$S_\epsilon = S_i - \beta S_o \cong S_i - \beta\left(\frac{S_i}{\beta}\right) = 0 \tag{12.10}$$

With a large loop gain, the error signal decreases to almost zero. We will see this result again as we consider specific feedback circuits throughout the chapter.

Test Your Understanding

12.1 The open-loop gain of an amplifier is $A = 10^4$, and the closed-loop gain is $A_f = 20$. (a) What is the feedback transfer function β? (b) What is the ratio of A_f to $(1/\beta)$? (Ans. (a) $\beta = 0.0499$ (b) 0.998)

12.2 The closed-loop gain of a feedback amplifier is $A_f = 80$, and the feedback transfer function is $\beta = 0.0120$. What is the value of the open-loop gain A? (Ans. $A = 2000$)

12.2.2 Gain Sensitivity

As previously stated, if the loop gain $T = \beta A$ is very large, the overall gain of the feedback amplifier is essentially a function of the feedback network only. We can quantify this characteristic.

If the feedback transfer function β is a constant, then taking the derivative of A_f with respect to A, from Equation (12.5), produces

$$\frac{dA_f}{dA} = \frac{1}{(1 + \beta A)} - \frac{A}{(1 + \beta A)^2} \cdot \beta = \frac{1}{(1 + \beta A)^2} \tag{12.11(a)}$$

or

$$dA_f = \frac{dA}{(1+\beta A)^2} \qquad \textbf{(12.11(b))}$$

Dividing both sides of Equation (12.11(b)) by the closed-loop gain yields

$$\frac{dA_f}{A_f} = \frac{\dfrac{dA}{(1+\beta A)^2}}{\dfrac{A}{1+\beta A}} = \frac{1}{(1+\beta A)} \cdot \frac{dA}{A} = \left(\frac{A_f}{A}\right)\frac{dA}{A} \qquad \textbf{(12.12)}$$

Equation (12.12) shows that the percent change in the closed-loop gain A_f is less than the corresponding percent change in the open-loop gain A by the factor $(1 + \beta A)$. The change in open-loop gain may result from variations in individual transistor parameters in the basic amplifier.

Example 12.2 **Objective:** Calculate the percent change in the closed-loop gain A_f, given a change in the open-loop gain A.

Using The same parameter values as in Example 12.1, we have $A = 10^5$, $A_f = 50$, and $\beta = 0.01999$. Assume that the change in the open-loop gain is $dA = 10^4$ (a 10 percent change).

Solution: From Equation (12.12), we have

$$dA_f = \frac{A_f}{(1+\beta A)} \cdot \frac{dA}{A} = \frac{50}{[1+(0.01999)(10^5)]} \cdot \frac{10^4}{10^5} = 2.5 \times 10^{-3}$$

The percent change is then

$$\frac{dA_f}{A_f} = \frac{2.5 \times 10^{-3}}{50} = 5 \times 10^{-5} \Rightarrow 0.005\%$$

compared to the 10 percent change assumed in the open-loop gain.

Comment: From this example, we see that the resulting percent change in the closed-loop gain is substantially less than the percent change in the open-loop gain. This is one of the principal advantages of negative feedback.

From Equation (12.12), the change in A_f is reduced by the factor $(1 + \beta A)$ compared to the change in A. The term $(1 + \beta A)$ is called the **desensitivity factor**.

Test Your Understanding

12.3 Consider a general feedback system with parameters $A = 10^6$ and $A_f = 100$. If the magnitude of A decreases by 20 percent, what is the corresponding percent change in A_f? (Ans. 0.002%)

12.4 The gain factors in a feedback system are $A = 5 \times 10^5$ and $A_f = 100$. Parameter A_f must not change more than ±0.001 percent because of a change in A. What is the maximum allowable variation in A? (Ans. ±5%)

12.2.3 Bandwidth Extension

The amplifier bandwidth is a function of feedback. Assume the frequency response of the basic amplifier can be characterized by a single pole. We can then write

$$A(s) = \frac{A_o}{1 + \dfrac{s}{\omega_H}} \tag{12.13}$$

where A_o is the low-frequency or midband gain, and ω_H is the upper 3 dB or corner frequency.

The closed-loop gain of the feedback amplifier can be expressed as

$$A_f(s) = \frac{A(s)}{(1 + \beta A(s))} \tag{12.14}$$

where we assume that the feedback transfer function β is independent of frequency. Substituting Equation (12.13) into Equation (12.14), we can write the closed-loop gain in the form

$$A_f(s) = \frac{A_o}{(1 + \beta A_o)} \cdot \frac{1}{1 + \dfrac{s}{\omega_H(1 + \beta A_o)}} \tag{12.15}$$

From Equation (12.15), we see that the low-frequency closed-loop gain is smaller than the open-loop gain by a factor of $(1 + \beta A_o)$, but the closed-loop 3 dB frequency is larger than the open-loop value by a factor of $(1 + \beta A_o)$.

If we multiply the low-frequency open-loop gain A_o by the bandwidth (3 dB frequency) ω_H, we obtain $A_o\omega_H$, which is the gain–bandwidth product. The product of the low-frequency closed-loop gain and the closed-loop bandwidth is

$$\frac{A_o}{(1 + \beta A_o)}[\omega_H(1 + \beta A_o)] = A_o\omega_H \tag{12.16}$$

Equation (12.16) states that the gain-bandwidth product of a feedback amplifier is a constant. That is, for a given circuit, we can increase the gain at the expense of a reduced bandwidth, or we can increase the bandwidth at the expense of a reduced gain. This property is illustrated in Figure 12.2.

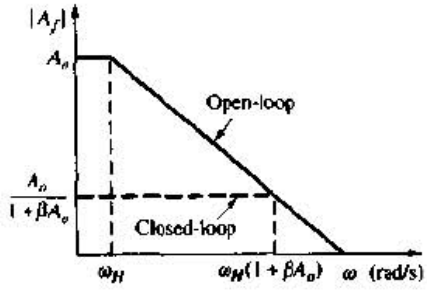


Figure 12.2 Open-loop and closed-loop gain versus frequency, illustrating bandwidth extension

Example 12.3 **Objective:** Determine the bandwidth of a feedback amplifier.

Consider a feedback amplifier with an open-loop low-frequency gain of $A_o = 10^4$, an open-loop bandwidth of $\omega_H = (2\pi)(100)$ rad/s, and a closed-loop low-frequency gain of $A_f(0) = 50$.

Solution: From Equation (12.15), the low-frequency closed-loop gain is

$$A_f(0) = \frac{A_o}{(1 + \beta A_o)}$$

or

$$50 = \frac{10^4}{(1 + \beta A_o)}$$

which yields

$$(1 + \beta A_o) = \frac{10^4}{50} = 200$$

From Equation (12.15), the closed-loop bandwidth is

$$\omega_{fH} = \omega_H(1 + \beta A_o) = (2\pi)(100)(200) = (2\pi)(20 \times 10^3)$$

Comment: The bandwidth increases from 100 Hz to 20 kHz as the gain decreases from 10^4 to 50.

Test Your Understanding

12.5 A feedback amplifier has an open-loop low-frequency gain of $A_o = 10^5$, an open-loop bandwidth of $\omega_H = (2\pi)(10)$ rad/s, and a closed-loop low-frequency gain of $A_f(0) = 100$. Determine the bandwidth of the closed-loop system. (Ans. $\omega = (2\pi)(10^4)$ rad/s)

12.6 In a feedback amplifier, the open-loop low-frequency gain is $A_o = 10^6$ and the open-loop 3 dB frequency is 8 Hz. If the bandwidth of the closed-loop system is 250 kHz, what is the maximum allowable value of the closed-loop low-frequency gain? (Ans. $A_f(0) = 32$)

12.2.4 Noise Sensitivity

In any electronic system, unwanted random and extraneous signals may be present in addition to the desired signal. These random signals are called **noise**. Electronic noise can be generated within an amplifier, or may enter the amplifier along with the input signal. Negative feedback may reduce the noise level in amplifiers; more accurately, it may increase the **signal-to-noise ratio**. More precisely, feedback can help reduce the effect of noise generated in an amplifier, but it cannot reduce the effect when the noise is part of the input signal.

The input signal-to-noise ratio is defined as

$$(\text{SNR})_i = \frac{S_i}{N_i} = \frac{v_i}{v_n} \tag{12.17}$$

where $S_i = v_i$ is the input source signal and $N_i = v_n$ is the input noise signal. The output signal-to-noise ratio is

$$(\text{SNR})_o = \frac{S_o}{N_o} = \frac{A_{Ti}S_i}{A_{Tn}N_i} \tag{12.18}$$

where the desired output signal is $S_o = A_{Ti}S_i$ and the output noise signal is $N_o = A_{Tn}N_i$. The parameter A_{Ti} is the amplification factor that multiplies the source signal, and the parameter A_{Tn} is the amplification factor that multiplies the noise signal. A large signal-to-noise ratio allows the signal to be detected without any loss of information. This is a desirable characteristic.

The following example compares the signal and noise amplification factors, which may or may not be equal.

Example 12.4 **Objective:** Determine the effect of feedback on the source signal and noise signal levels.

Consider the four possible amplifier configurations shown in Figure 12.3. The amplifiers are designed to provide the same output signal voltage. Determine the effect of the noise signal v_n.

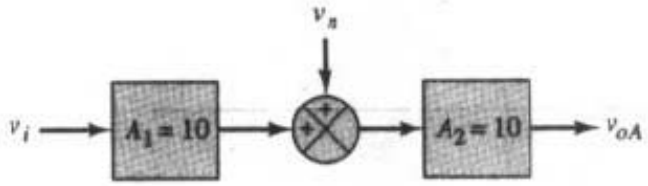
Figure 12.3 Four amplifier configurations with different input noise sources

Solution: Figure 12.3(a): Two open-loop amplifiers are in a cascade configuration, and the noise signal is generated between the two amplifiers. The output voltage is

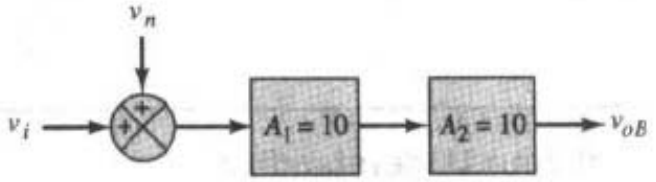
$$v_{oa} = A_1A_2v_i + A_2v_n = 100v_i = 10v_n$$

Therefore, the output signal-to-noise ratio is

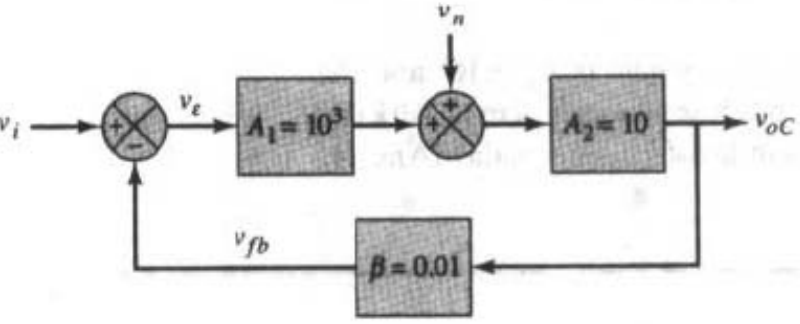
$$\frac{S_o}{N_o} = \frac{100v_i}{10v_n} = 10\frac{S_i}{N_i}$$


v_n
v_i
$A_1 = 10$
$A_2 = 10$
v_{oA}

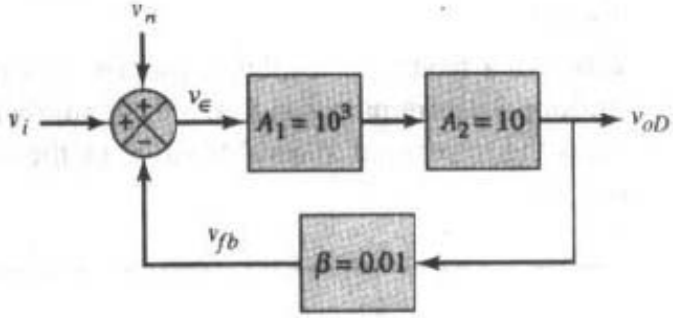
(a)


v_n
v_i
$A_1 = 10$
$A_2 = 10$
v_{oB}

(b)


v_n
v_i
v_ϵ
$A_1 = 10^3$
$A_2 = 10$
v_{oC}
v_{fb}
$\beta = 0.01$

(c)


v_n
v_i
v_ϵ
$A_1 = 10^3$
$A_2 = 10$
v_{oD}
v_{fb}
$\beta = 0.01$

(d)

Solution: Figure 12.3(b): Two open-loop amplifiers are in a cascade configuration, and the noise is part of the input signal. The output voltage is

$$v_{ob} = A_1A_2v_i + A_1A_2v_n = 100v_i + 100v_n$$

Therefore, the output signal-to-noise ratio is

$$\frac{S_o}{N_o} = \frac{100v_i}{100v_n} = \frac{S_i}{N_i}$$

Solution: Figure 12.3(c): Two amplifiers are in a feedback configuration, and the noise signal is generated between the two amplifiers. The output voltage is

$$v_{oc} = A_1A_2v_\epsilon + A_2v_n$$

and the feedback signal is

$$v_{fb} = \beta v_{oc}$$

Then,

$$v_\epsilon = v_i - v_{fb} = v_i - \beta v_{oc}$$

therefore,

$$v_{oc} = A_1A_2(v_i - \beta v_{oc}) + A_2v_n$$

or

$$v_{oc} = \frac{A_1A_2}{(1 + \beta A_1A_2)} \cdot v_i + \frac{A_2}{(1 + \beta A_1A_2)} \cdot v_n \cong 100v_i + 0.1v_n$$

The output signal-to-noise ratio is

$$\frac{S_o}{N_o} = \frac{100v_i}{0.1v_n} = 1000\frac{S_i}{N_i}$$

Solution: Figure 12.3(d): A basic feedback configuration, and the noise is part of the input signal. The output voltage is

$$v_{od} = \frac{A_1A_2}{(1 + \beta A_1A_2)}(v_i + v_n) \cong 100v_i + 100v_n$$

Therefore, the output signal-to-noise ratio is

$$\frac{S_o}{N_o} = \frac{100v_i}{100v_n} = \frac{S_i}{N_i}$$

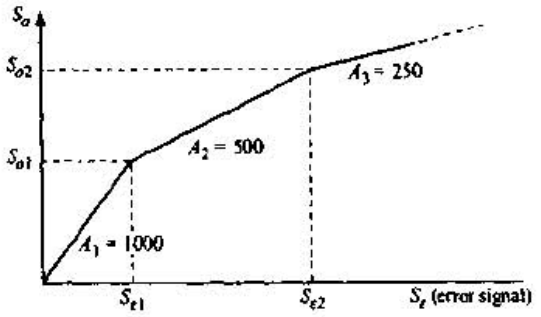
Comment: Comparing the four configurations, we see that Figure 12.3(c) produces the largest output signal-to-noise ratio. This configuration may occur when amplifier A_2 is an audio power-amplifier stage, in which large currents can produce excessive noise, and when amplifier A_1 corresponds to a low-noise preamplifier, which provides most of the voltage gain.

We must emphasize that the increased signal-to-noise ratio due to feedback occurs only in specific situations. As indicated in Figure 12.3(d), when noise is effectively part of the amplifier input signal, the feedback mechanism does not improve the ratio.

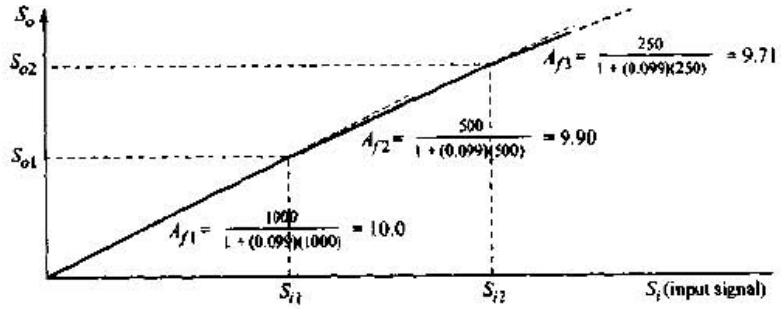
12.2.5 Reduction of Nonlinear Distortion

Distortion in an output signal is caused by a change in the basic amplifier gain or a change in the slope of the basic amplifier transfer function. The change in gain is a function of the nonlinear properties of bipolar and MOS transistors used in the basic amplifier.

Assume the basic amplifier, or open-loop, transfer function is as shown in Figure 12.4(a), which shows changes in gain as the input signal changes. The gain values are shown on the figure. When this amplifier is incorporated in a feedback circuit with a feedback transfer function of $\beta = 0.099$, the resulting closed-loop transfer characteristics are shown in Figure 12.4(b). This transfer function also has changes in gain but, whereas the open-loop gain changes by a factor of 2, the closed-loop gain changes by only 1 percent and 2 percent, respectively. A smaller change in gain means less distortion in the output signal of the negative feedback amplifier.



(a)



(b)

Figure 12.4 (a) Basic amplifier (open-loop) transfer characteristics; (b) closed-loop transfer characteristics

12.3 IDEAL FEEDBACK TOPOLOGIES

There are four basic feedback topologies, based on the parameter to be amplified (voltage or current) and the output parameter (voltage or current). The four feedback circuit categories can be described by the types of connections at the input and output of circuit. The four types of connections are shown in Figure 12.5. The four connections are referred to as: series–shunt (voltage amplifier), shunt–series (current amplifier), series–series (transconductance

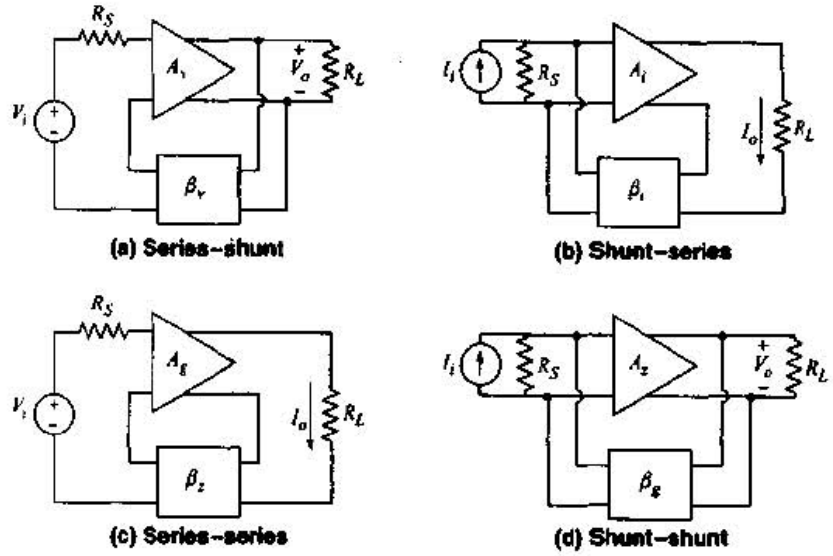


Figure 12.5 Basic feedback connections

amplifier), and shunt–shunt (transresistance amplifier). The first term refers to the connection at the amplifier input, and the second term refers to the connection at the output. Also, the type of connection determines which parameter (voltage or current) is sampled at the output and which parameter is amplified. The connections also determine the feedback amplifier characteristics—in particular, the input and output resistances. The resistance parameters become an important circuit property, when, for example, we consider voltage amplifiers versus current amplifiers.

In this section, we will determine the ideal transfer functions and the ideal input and output resistances of each of the four feedback topologies. In later sections, we will compare actual versus ideal feedback circuit characteristics.

As a note, the ideal topologies are small-signal equivalent circuits; therefore, phasor notation is used throughout this analysis.

12.3.1 Series–Shunt Configuration

The configuration of an ideal **series–shunt** feedback amplifier is shown in Figure 12.6. The circuit consists of a basic voltage amplifier with an input resistance R_i and an open-loop voltage gain A_v. The feedback circuit samples the output voltage and produces a feedback voltage V_{fb}, which is in series with the input signal voltage V_i. In this ideal configuration, the input resistance to the feedback circuit is infinite; therefore, there is no loading effect on the output of the basic amplifier due to the feedback circuit.

Voltage V_ϵ is the difference between the input signal voltage and the feedback voltage and is called an error signal. The error signal is amplified in the basic voltage amplifier. We can recognize the series connection on the input and the shunt connection of the output for this configuration.

The circuit is a voltage-controlled voltage source and is an ideal voltage amplifier. The feedback circuit samples the output voltage and provides a feedback voltage in series with the source voltage. For example, an increase

Figure 12.6 Ideal series–shunt feedback topology

in the output voltage produces an increase in the feedback voltage, which in turn decreases the error voltage due to the negative feedback. Then, the smaller error voltage is amplified producing a smaller output voltage, which means that the output signal tends to be stabilized.

If the output of the feedback network is an open circuit, then the output voltage is

$$V_o = A_v V_\varepsilon \tag{12.19}$$

and the feedback voltage is

$$V_{fb} = \beta V_o = \beta_v V_o \tag{12.20}$$

Parameter β_v is the voltage feedback transfer function, which is the ratio of the feedback voltage to the output voltage. The notation is similar to the voltage gain A_v, which is also the ratio of two voltages.

The error voltage, assuming the source resistance R_S is negligible, is

$$V_\varepsilon = V_i - V_{fb} \tag{12.21}$$

Combining Equations (12.19), (12.20), and (12.21), we find the closed-loop voltage transfer function is

$$A_{vf} = \frac{V_o}{V_i} = \frac{A_v}{(1 + \beta_v A_v)} \tag{12.22}$$

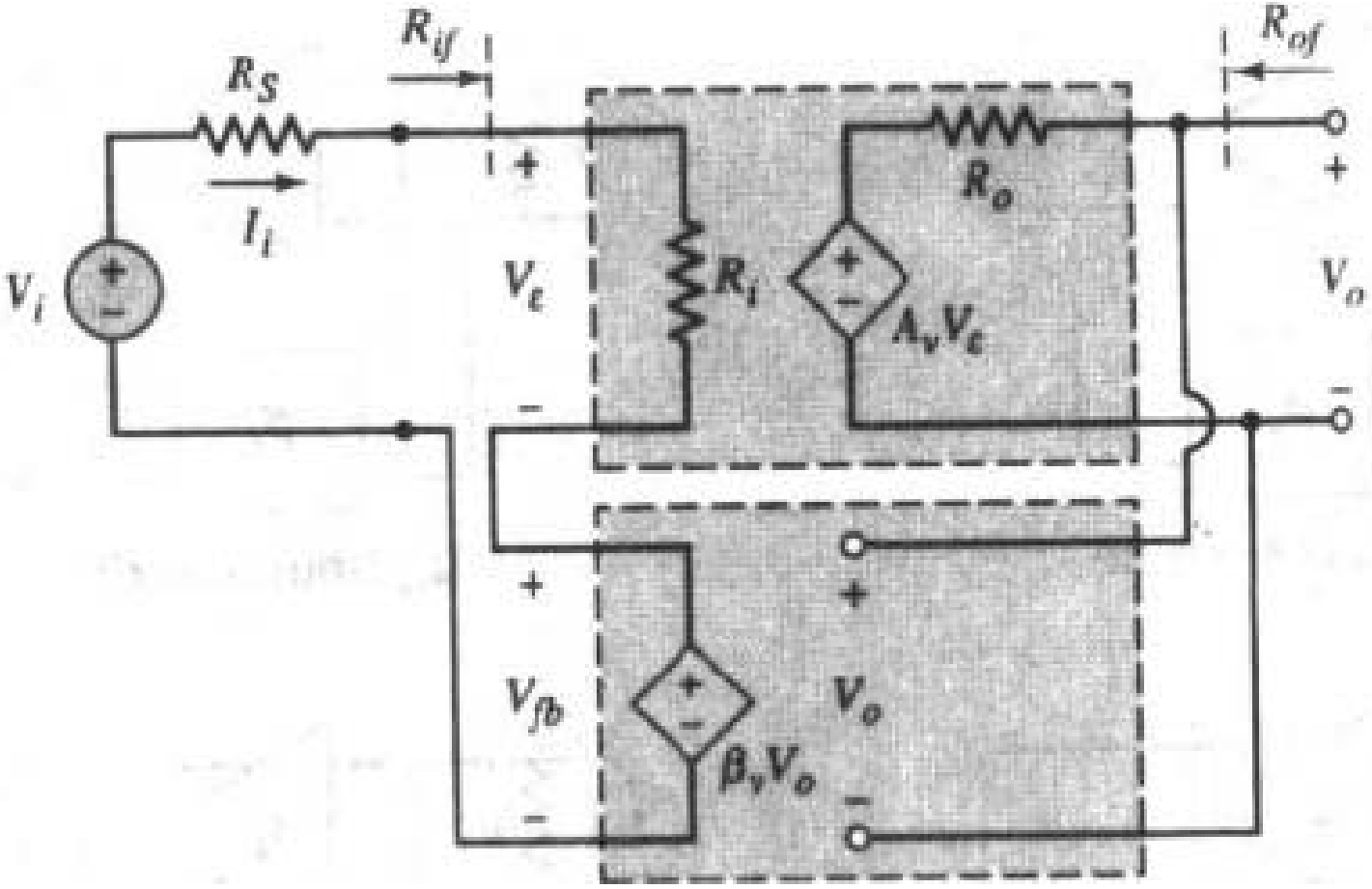
Equation (12.22) is the **closed-loop voltage gain** of the feedback amplifier, and it has the same form as the ideal feedback transfer function given by Equation (12.5). Although the magnitude of the closed-loop voltage gain is less than that of the open-loop amplifier, the advantage is that the closed-loop voltage gain becomes essentially independent of the individual transistor parameters. We will examine this characteristic later in this chapter.

The input resistance including feedback is denoted by R_{if}. Starting with Equation (12.21), using Equations (12.19) and (12.20), we find that

$$V_i = V_\varepsilon + V_{fb} = V_\varepsilon + \beta_v V_o = V_\varepsilon + \beta_v (A_v V_\varepsilon) \tag{12.23(a)}$$

or

$$V_\varepsilon = \frac{V_i}{(1 + \beta_v A_v)} \tag{12.23(b)}$$


R_{if}
R_{of}
R_S
I_i
V_i
V_i
R_i
$A_v V_i$
R_o
V_o
V_{fb}
$\beta_v V_o$
V_o

The input current is

$$I_i = \frac{V_\varepsilon}{R_i} = \frac{V_i}{R_i(1 + \beta_v A_v)} \tag{12.24}$$

and the input resistance with feedback is then

$$R_{if} = \frac{V_i}{I_i} = R_i(1 + \beta_v A_v) \tag{12.25}$$

Equation (12.25) shows that a series input connection results in an increased input resistance compared to that of the basic voltage amplifier. A large input resistance is a desirable property of a voltage amplifier. This eliminates loading effects on the input signal source due to the amplifier.

The output resistance of the feedback circuit can be determined from the equivalent circuit in Figure 12.7. The input signal voltage source is set equal to zero (a short circuit), and a test voltage is applied to the output terminals.

Figure 12.7 Ideal series–shunt feedback configuration for determining output resistance

From the circuit, we see that

$$V_\varepsilon + V_{fb} = V_\varepsilon + \beta_v V_x = 0 \tag{12.26(a)}$$

or

$$V_\varepsilon = -\beta_v V_x \tag{12.26(b)}$$

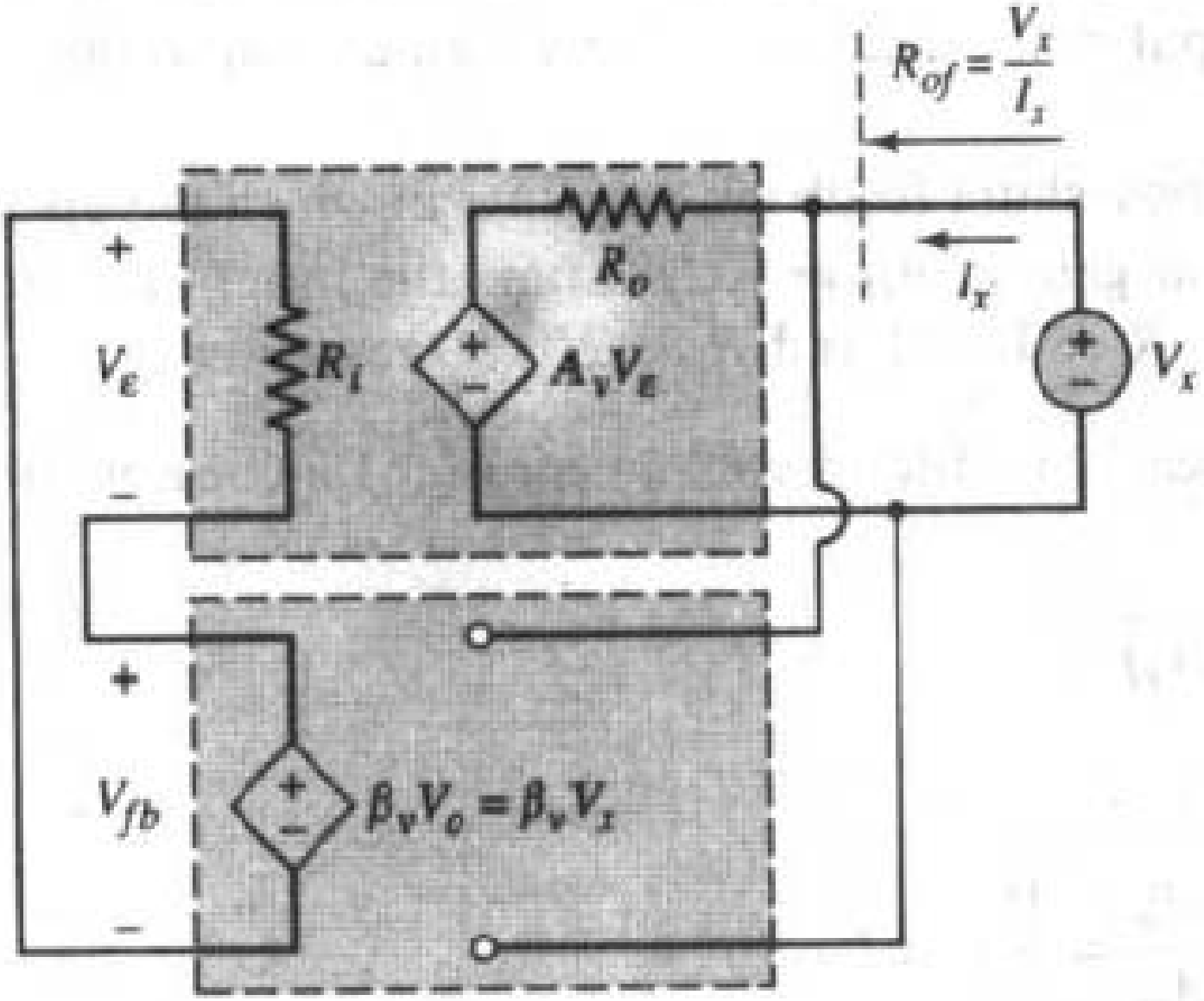
The output current is

$$I_x = \frac{V_x - A_v V_\varepsilon}{R_o} = \frac{V_x - A_v(-\beta_v V_x)}{R_o} = \frac{V_x(1 + \beta_v A_v)}{R_o} \tag{12.27}$$

and the output resistance, including feedback, is

$$R_{of} = \frac{V_x}{I_x} = \frac{R_o}{(1 + \beta_v A_v)} \tag{12.28}$$

Equation (12.28) shows that a shunt output connection results in a decreased output resistance compared to that of the basic voltage amplifier. A small output resistance is a desirable property of a voltage amplifier. This


$R_{of} = \frac{V_x}{I_x}$
R_o
I_x
V_ϵ
R_i
$A_v V_\epsilon$
V_x
V_{fb}
$\beta_v V_o = \beta_v V_x$

eliminates loading effects on the output signal when an output load is connected.

The equivalent circuit of this feedback voltage amplifier is shown in Figure 12.8.

Figure 12.8 Equivalent circuit of the series–shunt feedback circuit or voltage amplifier

Example 12.5 **Objective:** Determine the input resistance of a series input connection and the output resistance of a shunt output connection for an ideal feedback voltage amplifier.

Consider a series–shunt feedback amplifier in which the open-loop gain is $A_v = 10^5$ and the closed-loop gain is $A_{vf} = 50$. Assume the input and output resistances of the basic amplifier are $R_i = 10\,\text{k}\Omega$ and $R_o = 20\,\text{k}\Omega$, respectively.

Solution: The ideal closed-loop voltage transfer function is, from Equation (12.22),

$$A_{vf} = \frac{A_v}{(1 + \beta_v A_v)}$$

or

$$(1 + \beta_v A_v) = \frac{A_v}{A_{vf}} = \frac{10^5}{50} = 2 \times 10^3$$

From Equation (12.25), the input resistance is

$$R_{if} = R_i(1 + \beta_v A_v) = (10)(2 \times 10^3)\,\text{k}\Omega \Rightarrow 20\,\text{M}\Omega$$

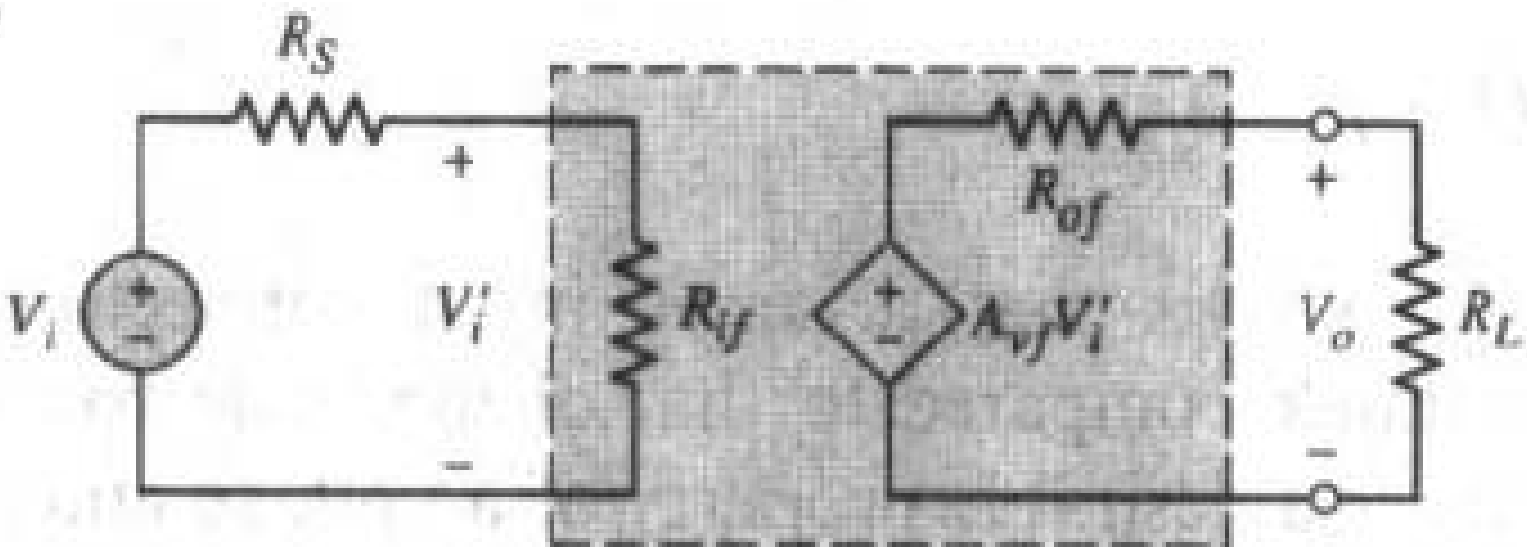
and, from Equation (12.28), the output resistance is

$$R_{of} = \frac{R_o}{(1 + \beta_v A_v)} = \frac{20}{2 \times 10^3}\,\text{k}\Omega \Rightarrow 10\,\Omega$$

Comment: With a series input connection, the input resistance increases drastically, and with a shunt output connection, the output resistance decreases substantially, with negative feedback. These are the desired characteristics of a voltage amplifier.

Test Your Understanding

12.7 An ideal series–shunt feedback amplifier is shown in Figure 12.6. Assume R_S is negligibly small. (a) If $V_i = 100\,\text{mV}$, $V_{fb} = 99\,\text{mV}$, and $V_o = 5\,\text{V}$, determine A_v, β_v, and A_{vf}, including units. (b) Using the results of part (a), determine R_{if} and R_{of}, for $R_l = 5\,\text{k}\Omega$ and $R_o = 4\,\text{k}\Omega$. (Ans. (a) $A_v = 5000\,\text{V/V}$, $\beta_v = 0.0198\,\text{V/V}$, $A_{vf} = 50\,\text{V/V}$ (b) $R_{if} = 500\,\text{k}\Omega$, $R_{of} = 40\,\Omega$)


R_S
V_i
+
V_i'
−
R_{if}
R_{of}
$A_{vf}V_i'$
+
V_o
−
R_L

12.3.2 Shunt–Series Configuration

The configuration of an ideal **shunt–series** feedback amplifier is shown in Figure 12.9. The circuit consists of a basic current amplifier with an input resistance R_i and an open-loop current gain A_i. The feedback circuit samples the output current and produces a feedback current I_{fb}, which is in shunt with an input signal current I_i. In this ideal configuration, the feedback circuit does not load down the basic amplifier output; therefore, the load current I_o is not affected.

Figure 12.9 Ideal shunt–series feedback topology

Current I_ϵ is the difference between the input signal current and the feedback current and is the error signal. The error signal is amplified in the basic current amplifier. We can recognize the shunt connection on the input and the series connection on the output for this configuration.

This circuit is a current-controlled current source and is an ideal current amplifier. The feedback circuit samples the output current and provides a feedback signal in shunt with the signal current. An increase in output current produces an increase in feedback current, which in turn decreases the error current. The smaller error current is then amplified, producing a smaller output current and stabilizing the output signal.

The input source shown is a Norton equivalent circuit; it could be converted to a Thevenin equivalent circuit.

If the output is essentially a short circuit, then the output current is

$$I_o = A_i I_\epsilon \tag{12.29}$$

and the feedback current is

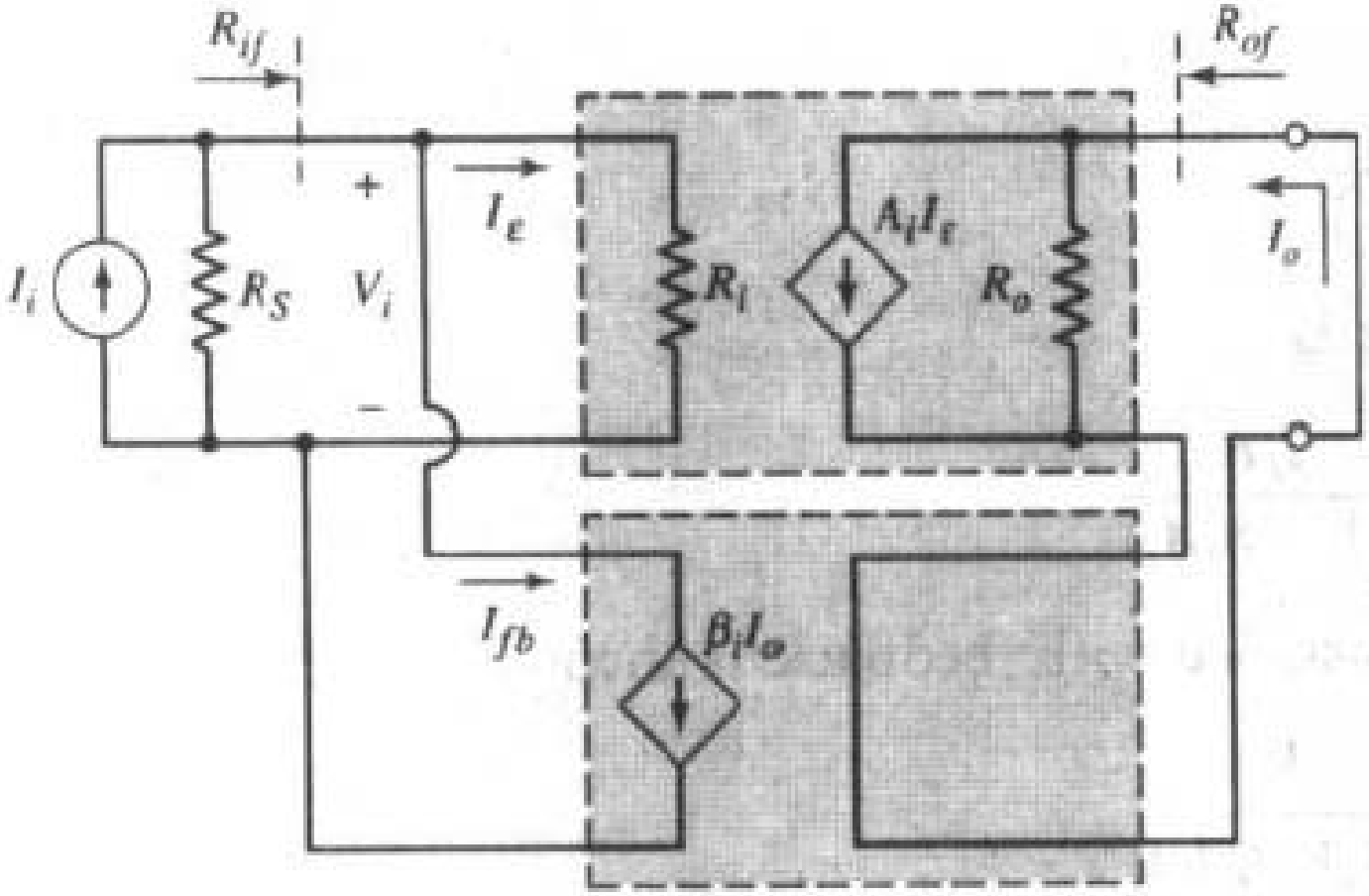
$$I_{fb} = \beta I_o = \beta_i I_o \tag{12.30}$$

The parameter β_i is the feedback current transfer function. The input signal current, assuming R_S is large, is

$$I_i = I_\epsilon + I_{fb} \tag{12.31}$$

Combining Equations (12.29), (12.30), and (12.31) yields the closed-loop current transfer function

$$A_{if} = \frac{I_o}{I_i} = \frac{A_i}{(1 + \beta_i A_i)} \tag{12.32}$$


R_{if}
R_{of}
I_i
R_S
V_i
+
−
I_ε
R_i
$A_f I_\varepsilon$
R_o
I_o
I_{fb}
$\beta_f I_o$

Equation (12.32) is the **closed-loop current gain** of the feedback amplifier.

The form of the equation for the current transfer function of the current amplifier (shunt–series connection) is the same as that for the voltage transfer function of the voltage amplifier (series–shunt connection). We will show that this will be the same for the two feedback connections yet to be discussed.

The input resistance of the shunt–series configuration is R_{if}. Starting with Equation (12.31), using Equations (12.29) and (12.30), we find that

$$I_i = I_\varepsilon + I_{fb} = I_\varepsilon + \beta_i I_o = I_\varepsilon + \beta_i(A_i I_\varepsilon) \tag{12.33(a)}$$

or

$$I_\varepsilon = \frac{I_i}{(1 + \beta_i A_i)} \tag{12.33(b)}$$

The input voltage is

$$V_i = I_\varepsilon R_i = \frac{I_i R_i}{(1 + \beta_i A_i)} \tag{12.34}$$

The input resistance with feedback is then

$$R_{if} = \frac{V_i}{I_i} = \frac{R_i}{(1 + \beta_i A_i)} \tag{12.35}$$

Equation (12.35) shows that a shunt input connection decreases the input resistance compared to that of the basic amplifier. A small input resistance is a desirable property of a current amplifier, to avoid loading effects on the input signal current source due to the amplifier.

The output resistance of the feedback circuit can be determined from the equivalent circuit in Figure 12.10. The input signal current is set equal to zero (an open circuit) and a test current is applied to the output terminals. Since the input signal current source is assumed to be ideal we have $R_S = \infty$.

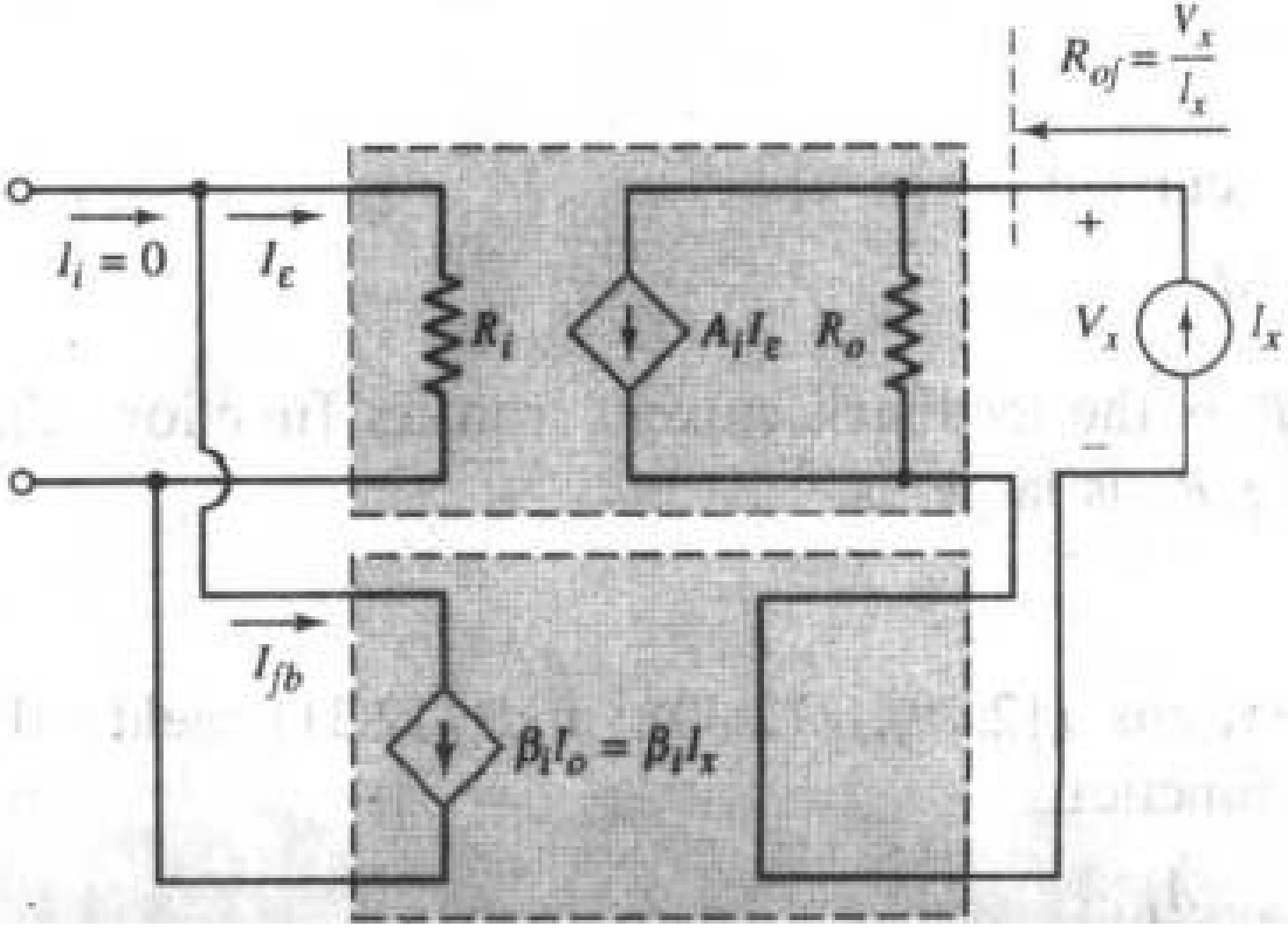
From the circuit, we see that

$$I_\varepsilon + I_{fb} = I_\varepsilon + \beta_i I_x = 0 \tag{12.36(a)}$$

or

$$I_\varepsilon = -\beta_i I_x \tag{12.36(b)}$$

Figure 12.10 Ideal shunt–series feedback configuration for determining output resistance


$R_{of} = \frac{V_x}{I_x}$
$I_i = 0$
I_ε
R_i
$A_i I_\varepsilon$
R_o
+
V_x
I_x
−
I_{fb}
$\beta_i I_o = \beta_i I_x$

The output voltage can be written as

$$\begin{aligned} V_x &= (I_x - A_i I_\varepsilon)R_o = [I_x - A_i(-\beta_i I_x)]R_o \\ &= I_x(1 + \beta_i A_i)R_o \end{aligned} \tag{12.37}$$

Therefore,

$$R_{of} = \frac{V_x}{I_x} = (1 + \beta_i A_i)R_o \tag{12.38}$$

Equation (12.38) shows that a series output connection increases the output resistance compared to that of the basic amplifier. A large output resistance is a desirable property of a current amplifier, to avoid loading effects on the output signal due to a load connected to the amplifier output.

The equivalent circuit of this feedback current amplifier is shown in Figure 12.11.

Figure 12.11 Equivalent circuit of shunt–series feedback circuit, or current amplifier

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Example 12.6 **Objective:** Determine the input resistance of a shunt input connection and the output resistance of a series output connection, for a feedback current amplifier.

Consider a shunt–series feedback amplifier in which the open-loop gain is $A_i = 10^5$ and the closed-loop gain is $A_{if} = 50$. Assume the input and output resistances of the basic amplifier are $R_i = 10\,\text{k}\Omega$ and $R_o = 20\,\text{k}\Omega$, respectively.

Solution: The ideal closed-loop current transfer function, from Equation (12.32), is

$$A_{if} = \frac{A_i}{(1 + \beta_i A_i)}$$

or

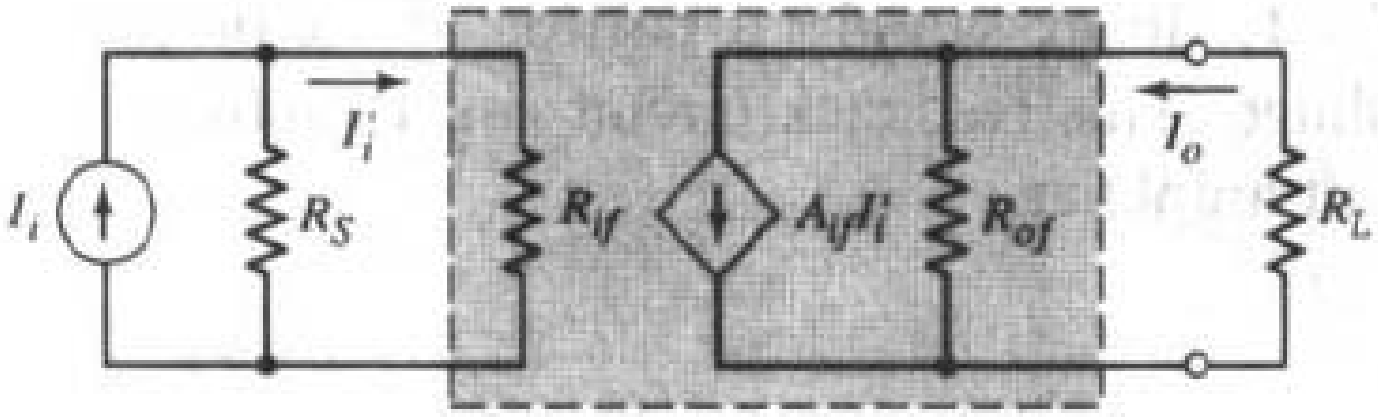
$$(1 + \beta_i A_i) = \frac{A_i}{A_{if}} = \frac{10^5}{50} = 2 \times 10^3$$

From Equation (12.35), the input resistance is

$$R_{if} = \frac{R_i}{(1 + \beta_i A_i)} = \frac{10}{2 \times 10^3}\,\text{k}\Omega \Rightarrow 5\,\Omega$$

and from Equation (12.38), the output resistance is

$$R_{of} = (1 + \beta_i A_i)R_o = (2 \times 10^3)(20)\,\text{k}\Omega \Rightarrow 40\,\text{M}\Omega$$


I_i
R_S
I_i'
R_{if}
$A_{if}I_i$
R_{of}
I_o
R_L

Comment: With a shunt input connection, the input resistance decreases drastically, and with a series output connection, the output resistance increases substantially, assuming negative feedback. These are the desired characteristics of a current amplifier.

Test Your Understanding

12.8 Consider the ideal shunt–series feedback amplifier in Figure 12.9. Assume that the source resistance is $R_S = \infty$. (a) If $I_i = 100\,\mu A$, $I_{fb} = 99\,\mu A$, and $I_o = 5\,mA$, determine A_i, β_i, and A_{if}, including units. (b) Using the results of part (a), determine R_{if} and R_{of}, for $R_i = 5\,k\Omega$ and $R_o = 4\,k\Omega$. (Ans. (a) $A_i = 5000\,A/A$, $\beta_i = 0.0198\,A/A$, $A_{if} = 50\,A/A$ (b) $R_{if} = 50\,\Omega$, $R_{of} = 400\,k\Omega$)

12.3.3 Series–Series Configuration

The configuration of an ideal **series–series** feedback amplifier is shown in Figure 12.12. The feedback samples a portion of the output current and converts it to a voltage. This feedback circuit can therefore be thought of as a voltage-to-current amplifier.

Figure 12.12 Ideal series–series feedback topology

The circuit consists of a basic amplifier that converts the error voltage to an output current with a gain factor A_g and that has an input resistance R_i. The feedback circuit samples the output current and produces a feedback voltage V_{fb}, which is in series with the input signal voltage V_i.

Assuming the output is essentially a short circuit, the output current is

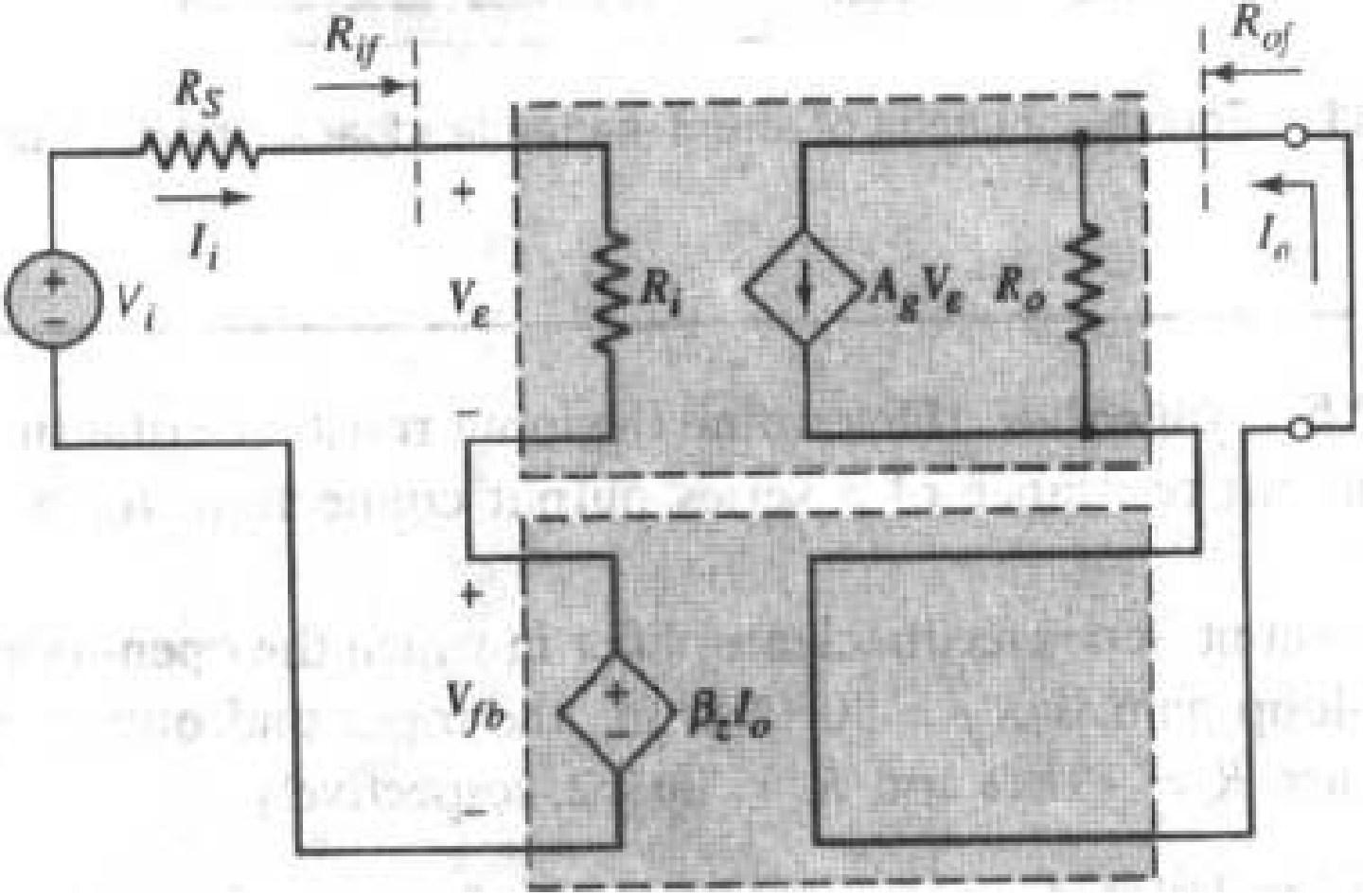
$$I_o = A_g V_\varepsilon$$

and the feedback voltage is

$$V_{fb} = \beta_z I_o$$

where β_z is called a resistance feedback transfer function, with units of *resistance*. The input signal voltage, neglecting the effect of R_S, is

$$V_i = V_\varepsilon + V_{fb}$$


R_{if}
R_{of}
R_S
I_i
V_i
+
V_ε
−
R_i
$A_g V_\varepsilon$
R_o
I_o
+
V_{fb}
−
$\beta_\varepsilon I_o$

Combining these equations, as we have in previous analyses, yields the closed-loop current-to-voltage transfer function,

$$A_{gf} = \frac{I_o}{V_i} = \frac{A_g}{(1 + \beta_z A_g)} \tag{12.39}$$

The units of the transfer function given by Equation (12.39) are amperes/volt, or conductance. We may note that the term $\beta_z A_g$ is dimensionless. This particular feedback circuit is therefore called a **transconductance amplifier**.

The input and output resistances are a function of the specific types of input and output connections, respectively. The input resistance for the series connection is given by Equation (12.25), which shows that with this configuration, the input resistance increases compared to that of the basic amplifier. The output resistance for the series connection is given by Equation (12.38), which shows that with this configuration, the output resistance increases compared to that of the basic amplifier. The equivalent circuit for the series–series feedback amplifier is shown in Figure 12.13.

Figure 12.13 Equivalent circuit of series–series feedback circuit, or transconductance amplifier

Test Your Understanding

12.9 An ideal series–series feedback amplifier is shown in Figure 12.12. Assume R_S is negligibly small. If $V_i = 100\,\text{mV}$, $V_{fb} = 99\,\text{mV}$, and $I_o = 5\,\text{mA}$, determine A_g, β_z, and A_{gf}, including units. (Ans. $A_g = 5\,\text{A/V}$, $\beta_z = 19.8\,\text{V/A}$, $A_{gf} = 50\,\text{mA/V}$)

12.3.4 Shunt–Shunt Configuration

The configuration of the ideal **shunt–shunt** feedback amplifier is shown in Figure 12.14. The feedback samples a portion of the output voltage and converts it to a current. This feedback circuit can therefore be thought of as a current-to-voltage amplifier.

The circuit consists of a basic amplifier that converts the error current to an output voltage with a gain factor A_z and that has an input resistance R_i. The feedback circuit samples the output voltage and produces a feedback current I_{fb}, which is in shunt with the input signal current I_i.

Assuming the output is essentially an open circuit, the output voltage is

$$V_o = A_z I_\varepsilon$$

and the feedback current is

$$I_{fb} = \beta_g V_o$$

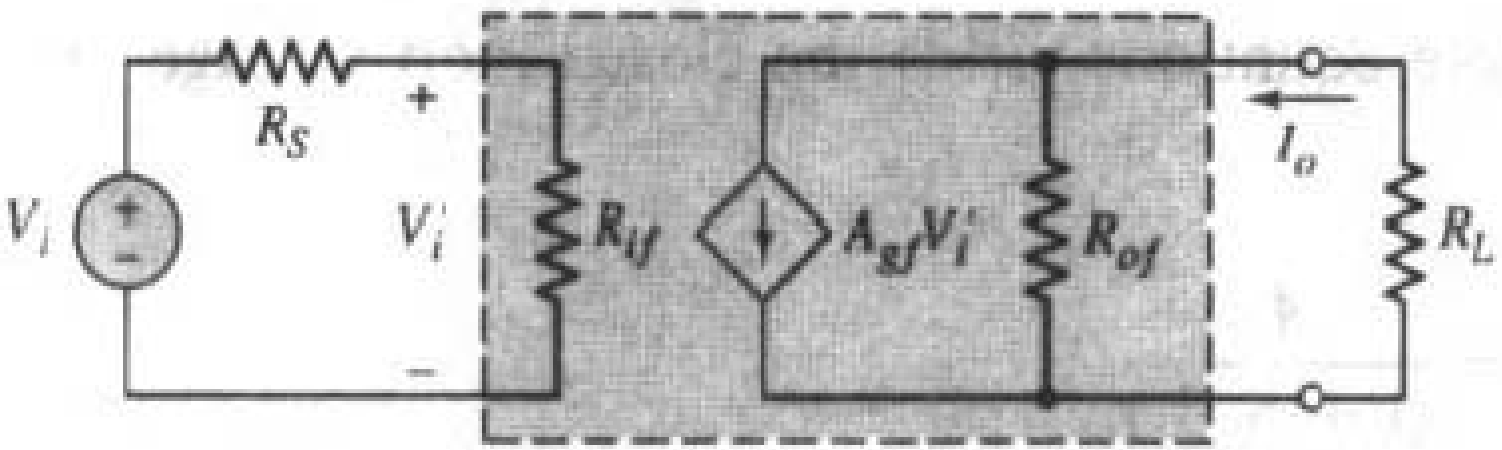

R_S
+
V_i
V_i'
−
R_{if}
$A_{sf}V_i'$
R_{of}
I_o
R_L

Figure 12.14 Ideal shunt–shunt feedback topology

where β_g is the conductance feedback transfer function, with units of conductance. The input signal current, assuming R_S is very large, is

$$I_i = I_\epsilon + I_{fb}$$

Combining these equations yields the closed-loop voltage-to-current transfer function,

$$A_{zf} = \frac{V_o}{I_i} = \frac{A_z}{(1 + \beta_g A_z)} \tag{12.40}$$

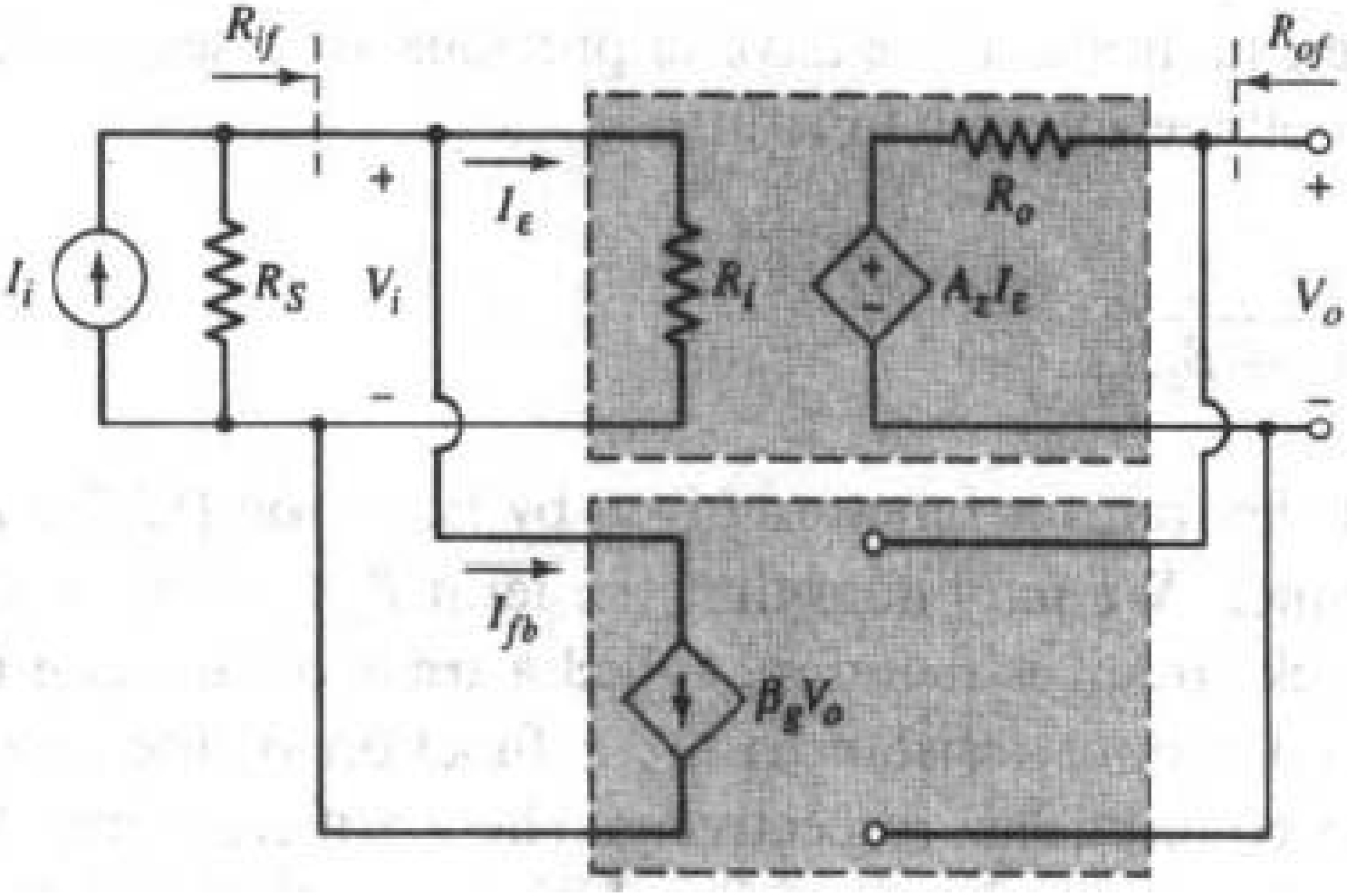
The units of the transfer function given by Equation (12.40) are volts/ampere, or resistance. We may note that the term $\beta_g A_z$ is dimensionless. This particular feedback circuit is therefore referred to as a **transresistance amplifier**.

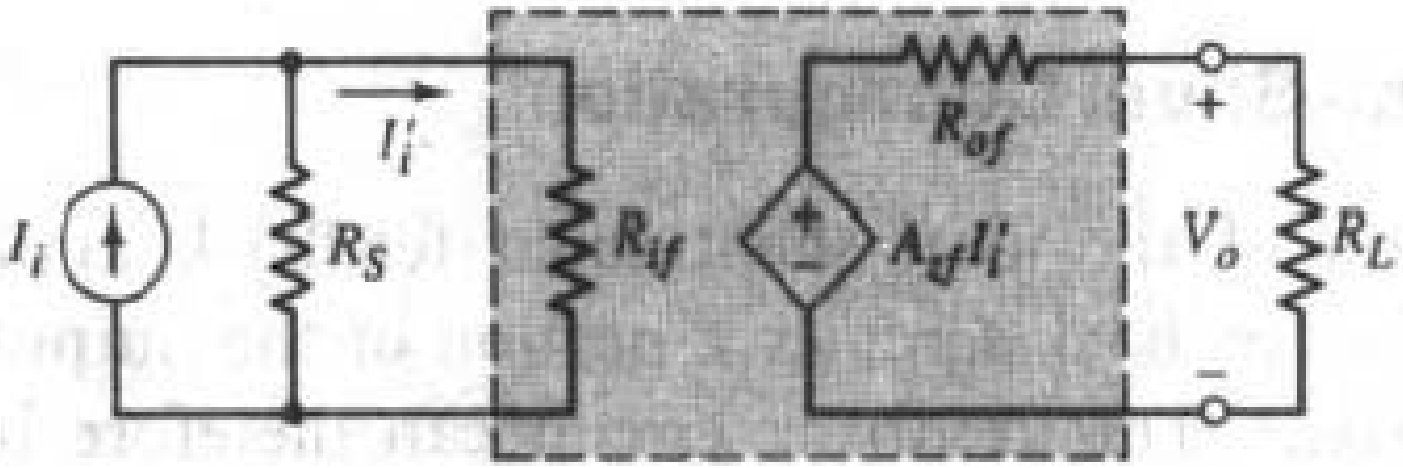
The input and output resistances are again a function of only the types of input and output connections, respectively. The input resistance is given by Equation (12.35) and the output resistance is given by Equation (12.28). The equivalent circuit for the shunt–shunt feedback amplifier is shown in Figure 12.15.

Figure 12.15 Equivalent circuit of shunt–shunt feedback circuit or, transresistance amplifier

Test Your Understanding

12.10 Consider the ideal shunt–shunt feedback amplifier in Figure 12.14. Assume that the source resistance is $R_S = \infty$. If $I_i = 100\,\mu A$, $I_{fb} = 99\,\mu A$, and $V_o = 5\,V$, determine A_z, β_g, and A_{zf}, including units. (Ans. $A_z = 5 \times 10^6\,V/A$, $\beta_g = 1.98 \times 10^{-5}\,A/V$, $A_{zf} = 50\,V/mA$)


R_{if}
R_{of}
I_i
R_S
V_i
+
−
I_ϵ
R_i
$A_I I_\epsilon$
R_o
+
V_o
−
I_{fb}
$B_g V_o$


I_i
R_S
I_i'
R_{if}
R_{of}
$A_{if}I_i'$
+
V_o
−
R_L

12.3.5 Summary of Results

Table 12.1 summarizes the ideal relationships, including the transfer functions, input resistances, and output resistances, obtained in the analysis of the four types of feedback amplifiers.

Having analyzed the characteristics of the four ideal feedback topologies, we will next derive the transfer functions and resistance characteristics of op-amp and discrete transistor representations of each type of feedback configuration. We will compare actual results with the ideal results, discussing any deviations from the ideal.

Table 12.1 Summary results of feedback amplifier functions for the ideal feedback circuit

Feedback amplifier	Source signal	Output signal	Transfer function	Input resistance	Output resistance
Series–shunt (voltage amplifier)	Voltage	Voltage	$A_{vf} = \frac{V_o}{V_i} = \frac{A_v}{(1 + \beta_v A_v)}$	$R_i(1 + \beta_v A_v)$	$\frac{R_o}{(1 + \beta_v A_v)}$
Shunt–series (current amplifier)	Current	Current	$A_{if} = \frac{I_o}{I_i} = \frac{A_i}{(1 + \beta_i A_i)}$	$\frac{R_i}{(1 + \beta_i A_i)}$	$R_o(1 + \beta_i A_i)$
Series–series (transconductance amplifier)	Voltage	Current	$A_{gf} = \frac{I_o}{V_i} = \frac{A_g}{(1 + \beta_z A_g)}$	$R_i(1 + \beta_z A_g)$	$R_o(1 + \beta_z A_g)$
Shunt–shunt (transresistance amplifier)	Current	Voltage	$A_{zf} = \frac{V_o}{I_i} = \frac{A_z}{(1 + \beta_g A_z)}$	$\frac{R_i}{(1 + \beta_g A_z)}$	$\frac{R_o}{(1 + \beta_g A_z)}$

12.4 VOLTAGE (SERIES–SHUNT) AMPLIFIERS

In this section, we will analyze an op-amp and a discrete circuit representation of the series–shunt feedback configuration. Since the series–shunt circuit is a voltage amplifier, we will derive the transfer function relating the output signal voltage to the input signal voltage. For the ideal configuration, this function is shown in Equation (12.22) and is

$$A_{vf} = \frac{A_v}{(1 + \beta_v A_v)}$$

where A_v is the basic amplifier voltage gain and β_v is the voltage feedback transfer function. We found that this feedback configuration, the input resistance increases and the output resistance decreases compared to the basic amplifier values.

12.4.1 Op-Amp Circuit Representation

Figure 12.16 shows a noninverting op-amp circuit, which is an example of the series–shunt configuration. The input signal is the input voltage V_i, the feedback voltage is V_{fb}, and the error signal is the voltage V_e. Since the shunt output samples the output voltage, the feedback voltage is a function of the output voltage.

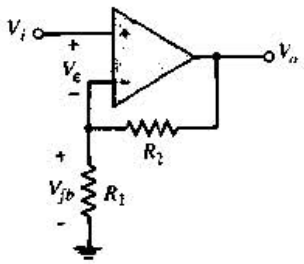


Figure 12.16 Example of an op-amp series–shunt feedback circuit

In the ideal feedback circuit, the amplification factor A_v is very large; from Equation (12.22), the transfer function is then

$$A_{vf} = \frac{V_o}{V_i} \cong \frac{1}{\beta_v} \tag{12.41}$$

For the ideal noninverting op-amp amplifier, we found in Chapter 9 that

$$A_{vf} = \frac{V_o}{V_i} = \left(1 + \frac{R_2}{R_1}\right) \tag{12.42}$$

Therefore, the feedback transfer function β_v is

$$\beta_v = \frac{1}{\left(1 + \frac{R_2}{R_1}\right)} \tag{12.43}$$

We can take a finite amplifier gain into account by considering the equivalent circuit in Figure 12.17. The parameter A_v is the open-loop voltage gain of the basic amplifier. We can write, for $R_o \approx 0$,

$$V_o = A_v V_\varepsilon \tag{12.44}$$

and

$$V_\varepsilon = V_i - V_{fb} \tag{12.45}$$

therefore,

$$V_o = A_v(V_i - V_{fb}) \tag{12.46}$$

Assuming the input resistance R_i is very large, the feedback voltage is given by

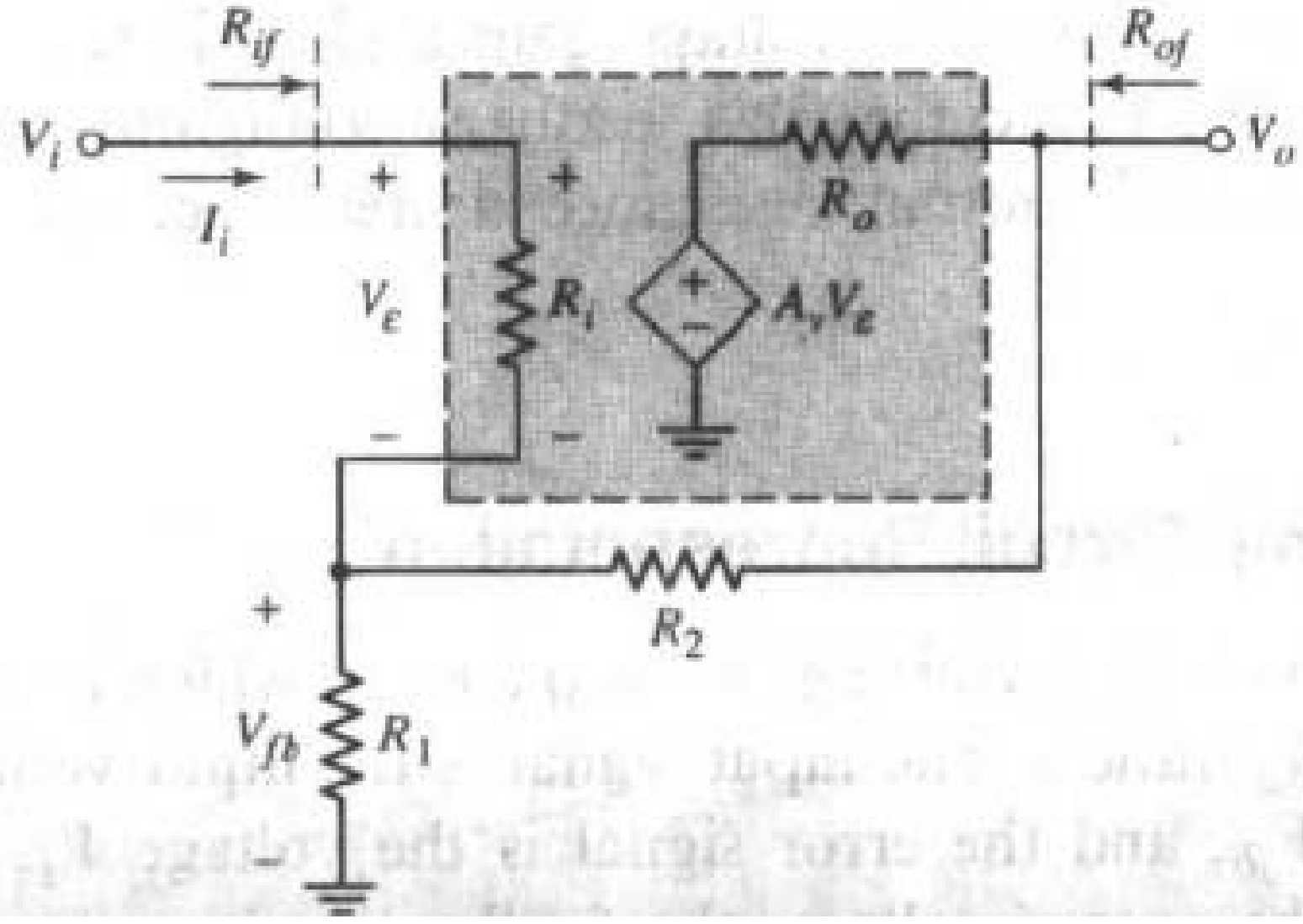
$$V_{fb} \cong \left(\frac{R_1}{R_1 + R_2}\right) V_o \tag{12.47}$$

Substituting Equation (12.47) into (12.46) and rearranging terms, we obtain

$$A_{vf} = \frac{V_o}{V_i} = \frac{A_v}{1 + \frac{A_v}{\left(1 + \frac{R_2}{R_1}\right)}} \tag{12.48}$$

The voltage feedback transfer function β_v is given by Equation (12.43), and the closed-loop voltage transfer function can be written

Figure 12.17 Equivalent circuit, op-amp series–shunt feedback configuration


R_{if}
R_{of}
V_i
V_o
I_i
V_ϵ
R_i
$A_v V_\epsilon$
R_o
R_2
V_{fb}
R_1

$$A_{vf} = \frac{A_v}{(1 + \beta_v A_v)} \tag{12.49}$$

The voltage transfer function for the noninverting op-amp circuit has the same form as that for the ideal series-shunt configuration, assuming the input resistance R_i is very large.

We may note in this case that the voltage gain A_v of the basic amplifier is positive and that the feedback transfer function β_v is also positive, so that the loop gain $T = \beta_v A_v$ is positive for negative feedback.

We can now derive the expression for the input resistance R_{if}. We see from the figure that $V_\varepsilon = I_i R_i$, $V_o = A_v V_\varepsilon$, and $V_i = V_\varepsilon + V_{fb}$. The approximate feedback voltage is given by Equation (12.47). Therefore, the input voltage is

$$\begin{aligned} V_i &= V_\varepsilon + \left(\frac{R_1}{R_1 + R_2}\right) V_o = V_\varepsilon + \frac{A_v V_\varepsilon}{\left(1 + \dfrac{R_2}{R_1}\right)} \\ &= V_\varepsilon \left[1 + \frac{A_v}{(1 + R_2/R_1)}\right] \end{aligned} \tag{12.50}$$

The input resistance is then

$$\begin{aligned} R_{if} &= \frac{V_i}{I_i} = \frac{V_i}{(V_\varepsilon / R_i)} \\ &= R_i \left[1 + \frac{A_v}{(1 + (R_2/R_1))}\right] = R_i (1 + \beta_v A_v) \end{aligned} \tag{12.51}$$

The expression for the input resistance for the op-amp circuit has the same form as that for the ideal series input connection, as given in Equation (12.25). In the ideal case in which the gain is $A_v = \infty$, the input resistance of the noninverting op-amp is also infinite. However, if the gain is finite, the input resistance will also be finite.

Example 12.7 **Objective:** Determine the expected input resistance of the noninverting op-amp circuit.

Consider the noninverting op-amp in Figure 12.16, with parameters $R_i = 50\,\text{k}\Omega$, $R_1 = 10\,\text{k}\Omega$, $R_2 = 90\,\text{k}\Omega$, and $A_v = 10^4$.

Solution: The feedback transfer function β_v is

$$\beta_v = \frac{1}{\left(1 + \dfrac{R_2}{R_1}\right)} = \frac{1}{\left(1 + \dfrac{90}{10}\right)} = 0.10$$

The input resistance is therefore

$$R_{if} = R_i (1 + \beta_v A_v) = (50)[1 + (0.10)(10^4)]$$

or

$$R_{if} \cong 50 \times 10^3\,\text{k}\Omega = 50\,\text{M}\Omega$$

Comment: Even with a moderate differential input resistance R_i to the op-amp, the closed-loop input resistance R_{if} is very large, because of the series input feedback connection.

The analysis results for the noninverting op-amp circuit are consistent with the ideal series–shunt feedback characteristics.

12.4.2 Discrete Circuit Representation

Figures 12.18(a) and (b) show the basic emitter-follower and source-follower circuits, which we examined in previous chapters. These are examples of discrete-circuit series–shunt feedback topologies. The input signal is the voltage v_i, the error signal is the base-emitter voltage in the emitter follower and the gate-source voltage in the source follower, and the feedback voltage is equal to the output voltage, which means that the feedback transfer function is $\beta_v = 1$.

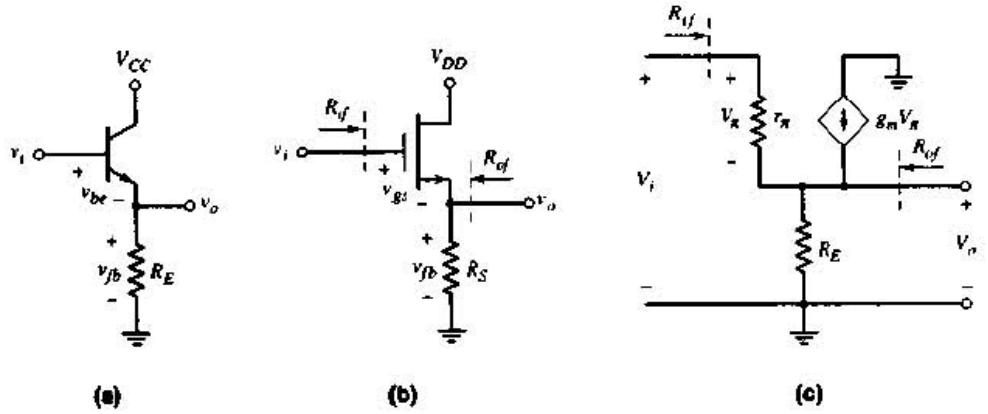


Figure 12.18 Discrete transistor series–shunt feedback circuits: (a) emitter-follower, (b) source-follower, and (c) small-signal equivalent circuit of emitter follower

The small-signal equivalent circuit of the emitter follower is shown in Figure 12.18(c). Since we have already analyzed the emitter-follower circuit, we will simply state the results here. The small-signal voltage gain is

$$A_{vf} = \frac{V_o}{V_i} = \frac{\left(\frac{1}{r_\pi} + g_m\right)R_E}{1 + \left(\frac{1}{r_\pi} + g_m\right)R_E} = \frac{\frac{R_E}{r_e}}{1 + \frac{R_E}{r_e}} \tag{12.52}$$

where

$$r_e = \frac{r_\pi}{(1 + g_m r_\pi)}$$

The voltage gain of the emitter follower can be written as a voltage divider equation. Since the feedback transfer function is unity, the form of the voltage gain expression is the same as that for the ideal series–shunt configuration, as given in Equation (12.22). The open-loop voltage gain corresponds to

$$A_v = \left(\frac{1}{r_\pi} + g_m\right)R_E = \frac{R_E}{r_e} \tag{12.53}$$

The closed-loop input resistance is[2]

$$R_{if} = r_\pi + (1 + h_{FE})R_E = r_\pi\left[1 + \left(\frac{1}{r_\pi} + g_m\right)R_E\right] \tag{12.54}$$

The form of the input resistance is also the same as that of the ideal expression, given by Equation (12.25). The input resistance increases with a series input connection.

The output resistance of the emitter-follower circuit is given by

$$R_{of} = R_E \left\| \frac{r_\pi}{1 + h_{FE}} = R_E \| r_e \right. \tag{12.55}$$

which can be written in the form

$$R_{of} = \frac{R_E}{1 + \left(\frac{1}{r_\pi} + g_m\right)R_E} \tag{12.56}$$

The output resistance decreases with a shunt output connection. For the emitter-follower circuit, the form of the output resistance is also the same as that of the ideal expression, given by Equation (12.28).

Even though the magnitude of the emitter-follower voltage gain is slightly less than unity, this circuit is a classic example of a series–shunt feedback configuration, which represents a voltage amplifier.

Design Example 12.8 Objective: Design a feedback amplifier to amplify the output signal of a microphone.

The output signal from the microphone is 10 mV and the output signal from the feedback amplifier must be 0.5 V to drive a power amplifier that in turn drives the speakers. The nominal output resistance of the microphone is $R_S = 5\,\text{k}\Omega$ and the nominal input resistance of the power amplifier is $R_L = 75\,\Omega$. An op-amp with parameters $R_i = 10\,\text{k}\Omega$, $R_o = 100\,\Omega$, and a low-frequency gain of $A_v = 10^4$ is available. [Note: In this simple design, neglect frequency response.]

Solution: Design Approach: Since the source resistance is fairly large, an amplifier with a large input resistance is required to minimize loading at the input. Also, since the load resistance is low, an amplifier with a low output resistance is required to minimize loading at the output. To satisfy these requirements, a series–shunt feedback configuration, or voltage amplifier, should be used.

The closed-loop voltage gain must be $A_{vf} = 0.5/0.01 = 50$. For the ideal case, $A_{vf} = 1/\beta_v$, so the feedback transfer function is $\beta_v = 1/50 = 0.02$. The loop gain is then

$$T = \beta_v A_v = (0.02)(10^4) = 200$$

Referring to Table 12.1, we expect the input resistance to be

$$R_{if} \cong (10)(200)\,\text{k}\Omega \rightarrow 2\,\text{M}\Omega$$

---

[2]Reminder: In this chapter, the parameter h_{FE} is used as the transistor current gain to avoid confusion with β, which is used as the feedback transfer function. Again, we assume that the dc and ac current gains are equal; therefore, $h_{FE} = h_{fe} = g_m r_\pi$.

and the output resistance to be

$$R_{of} \cong (100/200)\Omega = 0.5\,\Omega$$

These input and output resistance values will minimize any loading effects at the amplifier input and output terminals.

If we use the noninverting amplifier configuration in Figure 12.16, then we have

$$\frac{1}{\beta_v} = 1 + \frac{R_2}{R_1} = 50$$

and

$$\frac{R_2}{R_1} = 49$$

The feedback network loads the output of the amplifier; consequently, we need $R_1 + R_2$ to be much larger than R_o. However, the output resistance of the feedback network is in series with the input terminals, so extremely large values of R_1 and R_2 will reduce the actual signal applied to the op-amp because of voltage divider action. Initially, then, we choose $R_1 = 1\,\text{k}\Omega$ and $R_2 = 49\,\text{k}\Omega$.

Computer Simulation Verification: The circuit in Figure 12.19 was used in a PSpice analysis of the voltage amplifier. A standard 741 op-amp was used in the circuit. For a 10 mV input signal, the output signal was 499.6 mV, for a gain of 49.96. This result is within 0.08 percent of the ideal designed value. The input resistance R_{if} was found to be approximately 580 MΩ and the output resistance R_{of} was determined to be approximately 0.042 Ω. The differences between the measured input and output resistances compared to the predicted values are due to the differences between the actual μA-741 op-amp parameters and the assumed parameters. However, the measured input resistance is larger than predicted and the measured output resistance is smaller than predicted, which is desired and more in line with an ideal op-amp circuit.

Comment: An almost ideal feedback voltage amplifier can be realized if an op-amp is used in the circuit.

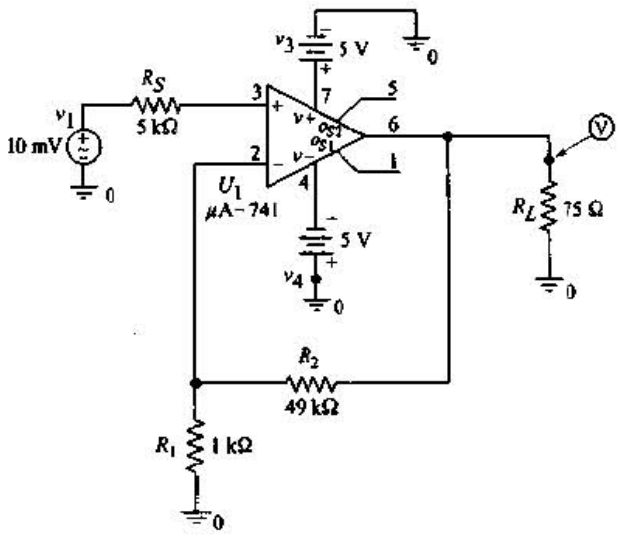


Figure 12.19 Circuit used in the computer simulation analysis in Example 12.8

Test Your Understanding

12.11 Consider the noninverting op-amp circuit in Figure 12.16, with parameters $R_1 = 10\,k\Omega$, $R_2 = 30\,k\Omega$, and $A_v = 10^4$. Assume $R_i = \infty$. Determine the closed-loop voltage gain. If the open-loop gain increases by a factor of 10, what is the percent change in the closed-loop gain? (Ans. $A_{vf} = 3.9984$, 0.036%)

12.12 Assume the transistor in the emitter-follower circuit in Figure 12.18(a) is biased such that $I_{CQ} = 0.5\,mA$. Let $R_E = 2\,k\Omega$. (a) If the transistor current gain is $h_{FE} = 100$, determine A_{vf}, R_{if}, and R_{of}. (b) Determine the percent change in A_{vf}, R_{if}, and R_{of} if the transistor current gain increases to $h_{FE} = 150$. Assume the quiescent collector current remains unchanged. (Ans. (a) $A_{vf} = 0.97490$, $R_{if} = 207\,k\Omega$, $R_{of} = 50.2\,\Omega$ (b) A_{vf}, 0.0082%; R_{if}, 1.25%; R_{of}, 0.397%)

12.13 Assume the transistor in the source-follower circuit shown in Figure 12.18(b) is biased such that $I_{DQ} = 250\,\mu A$. Let $R_S = 5\,k\Omega$. If the transistor parameters are $K = 200\,\mu A/V^2$ and $V_{TN} = 1\,V$, determine A_{vf}, R_{if}, and R_{of}. How do these results agree with the ideal feedback characteristics given in Table 12.1? (Ans. $A_{vf} = 0.691$, $R_{if} = \infty$, $R_{of} = 1.55\,k\Omega$)

***D12.14** Design a feedback voltage amplifier to provide a voltage gain of 15. The nominal voltage source resistance is $R_S = 2\,k\Omega$, and the nominal load is $R_L = 100\,\Omega$. An op-amp with parameters $R_i = 5\,k\Omega$, $R_o = 50\,\Omega$, and a low-frequency open-loop gain of $A_v = 5 \times 10^3$ is available. Correlate the design with a computer simulation analysis to determine the voltage gain, input resistance, and output resistance

12.5 CURRENT (SHUNT–SERIES) AMPLIFIERS

In this section, we will analzye an op-amp and a discrete circuit representation of the shunt-series feedback amplifier. The shunt–series circuit is a current amplifier; therefore, we must derive the output current to input current transfer function. For the ideal configuration, this function is given in Equation (12.32):

$$A_{if} = \frac{A_i}{(1 + \beta_i A_i)}$$

where A_i is the basic amplifier current gain and β_i is the current feedback transfer function. For this amplifier, the input resistance decreases and the output resistance increases compared to the basic amplifier values.

12.5.1 Op-Amp Circuit Representation

Figure 12.20 shows an op-amp current amplifier, which is a shunt–series configuration. The input signal is the current I_i' from the Norton equivalent source of I_i and R_S. The feedback current is I_{fb}, the error signal is the current I_ε, and the output signal is the current I_o. With the shunt input connection, the input resistance R_{if} is small, as previously stated. Resistance R_S is the output resistance of the current source and is normally large. If $R_S \gg R_{if}$, then $I_i' \cong I_i$.

If we assume initially that I_ε is negligible, then, from Figure 12.20, we have

$$I_i \cong I_i' = I_{fb}$$

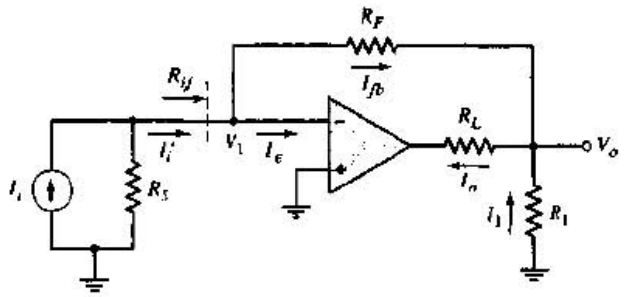


Figure 12.20 Example of an op-amp shunt–series feedback circuit

The output voltage V_o, assuming V_1 is at virtual ground, is

$$V_o = -I_{fb}R_F = -I_iR_F$$

and current I_1 is

$$I_1 = -V_o/R_1$$

The output current can be expressed

$$I_o = I_{fb} + I_1 = I_i + \left(-\frac{1}{R_1}\right)(-I_iR_F) = I_i\left(1 + \frac{R_F}{R_1}\right) \tag{12.57}$$

Therefore, the ideal current gain is

$$\frac{I_o}{I_i} = 1 + \frac{R_F}{R_1} \tag{12.58}$$

In the ideal feedback circuit, the amplification factor A_i is very large; consequently, the current transfer function, from Equation (12.32), becomes

$$A_{if} = \frac{I_o}{I_i} \cong \frac{1}{\beta_i} \tag{12.59}$$

Comparing Equation (12.59) with (12.58), we see that the current feedback transfer function for the ideal op-amp current amplifier is

$$\beta_i = \frac{1}{\left(1 + \frac{R_F}{R_1}\right)} \tag{12.60}$$

We can take the finite amplifier gain into account by considering the equivalent circuit in Figure 12.21. The parameter A_i is the open-loop current gain. We have

$$I_o = A_iI_\epsilon \tag{12.61}$$

and

$$I_\epsilon = I_i' - I_{fb} \cong I_i - I_{fb} \tag{12.62}$$

therefore,

$$I_o = A_i(I_i - I_{fb}) \tag{12.63}$$

If we again assume that V_1 is at virtual ground, voltage V_o is given by

$$V_o = -I_{fb}R_F \tag{12.64}$$

Figure 12.21 Equivalent circuit, op-amp shunt–series feedback configuration

We can then write

$$I_1 = -\frac{V_o}{R_1} = -\left(\frac{1}{R_1}\right)(-I_{fb}R_F) = I_{fb}\left(\frac{R_F}{R_1}\right) \tag{12.65}$$

The output current is also expressed as

$$I_o = I_{fb} + I_1 = I_{fb} + I_{fb}\left(\frac{R_F}{R_1}\right) \tag{12.66}$$

Solving for I_{fb} from Equation (12.66), substituting that into Equation (12.63), and rearranging terms yields the closed-loop current gain

$$A_{if} = \frac{I_o}{I_i} = \frac{A_i}{1 + \dfrac{A_i}{\left(1 + \dfrac{R_F}{R_1}\right)}} \tag{12.67}$$

Since the current feedback transfer function is $\beta_i = 1/[1 + (R_F/R_1)]$, the closed-loop current gain expression for the op-amp current amplifier has the same form as that for the ideal shunt–series configuration.

12.5.2 Simple Discrete Circuit Representation

Figure 12.22(a) shows the ac equivalent circuit of a common-base circuit, which is an example of a simple discrete shunt–series configuration. Figure 12.22(b) is the same circuit rearranged to demonstrate more clearly the input, feedback, and error components of the currents. The output current is

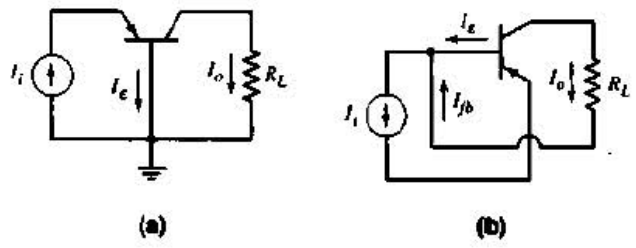
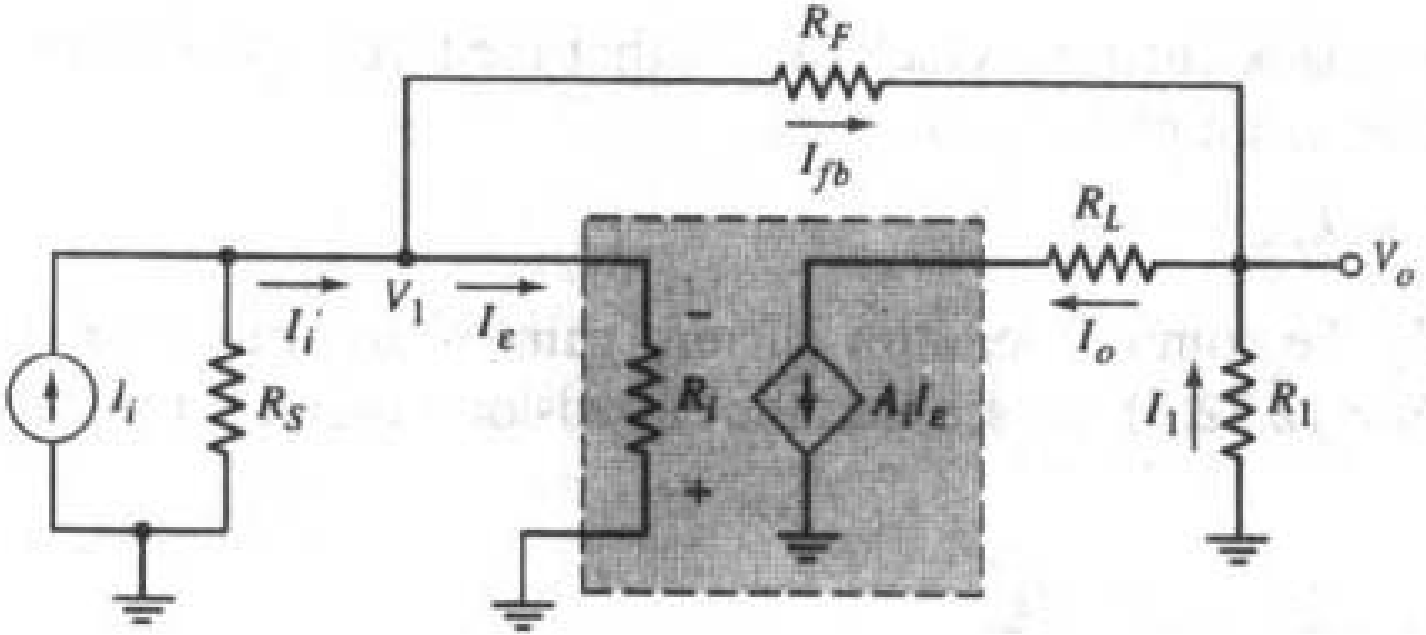


Figure 12.22 (a) Equivalent circuit for simple common-base circuit and (b) reconfigured circuit


R_F
I_{fb}
R_L
V_o
I_i
V_1
I_ϵ
I_o
I_i
R_S
R_I
$A_I I_\epsilon$
I_1
R_1
−
+

equal to the feedback current, which means that the feedback transfer function is $\beta_i = 1$. The basic amplifier gain is

$$I_o/I_\epsilon = A_i = h_{FE}$$

which is simply the common-emitter current gain of the transistor.

From Figure 12.22(b), we see that the closed-loop current transfer function or gain is

$$A_{if} = \frac{I_o}{I_i} = \frac{h_{FE}}{1 + h_{FE}} = \frac{A_i}{1 + A_i} \tag{12.68}$$

Since the current feedback transfer function β_i is unity, Equation (12.68) has the same form as that for the ideal shunt-series transfer function.

Figure 12.23(a) is a more realistic common-base circuit. Resistor R_E and the supply voltages V^+ and V^- bias the transistor in the forward-active mode. The ac equivalent circuit is in Figure 12.23(b). We can show that the current gain is

$$A_{if} = \frac{I_o}{I_i} = \frac{h_{FE}}{\left(1 + \frac{r_\pi}{R_E}\right) + h_{FE}} = \frac{A_i}{\left(1 + \frac{r_\pi}{R_E}\right) + A_i} \tag{12.69}$$

Equation (12.69) does not have the same form as the ideal shunt–series feedback transfer function. This is common in many discrete transistor feedback circuits. The reason is that resistor R_E introduces loading effects that are not present in the ideal configuration. Typically, then, the transfer functions of actual discrete circuits are not the same as for the ideal case.

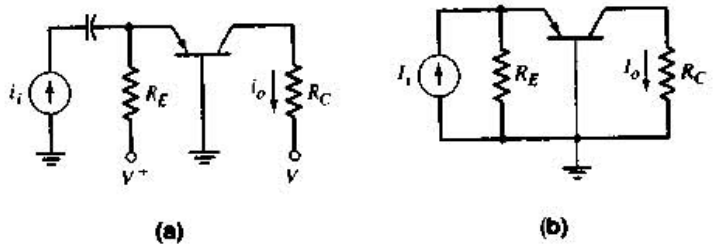


Figure 12.23 (a) Common-base circuit, including biasing and (b) ac equivalent circuit

12.5.3 Discrete Circuit Representation

Figure 12.24(a) shows a two-stage discrete transistor circuit example of a shunt–series feedback configuration. While the large number of capacitors makes this circuit somewhat impractical, it can be used to illustrate the basic concepts of feedback. Figure 12.24(b) shows the ac equivalent circuit, in which all capacitors act as short circuits. With the shunt input connection, the input signal current is essentially I_i (assuming R_S is large), the feedback current is I_{fb}, and the error signal is I_ϵ. The signal emitter current I_e is directly proportional to the load current I_o, and the feedback current is directly proportional to I_e, demonstrating that this series output connection samples the output current I_o.

The small-signal equivalent circuit is shown in Figure 12.25. We assume that the small-signal output resistance r_o of each transistor is infinite. We could

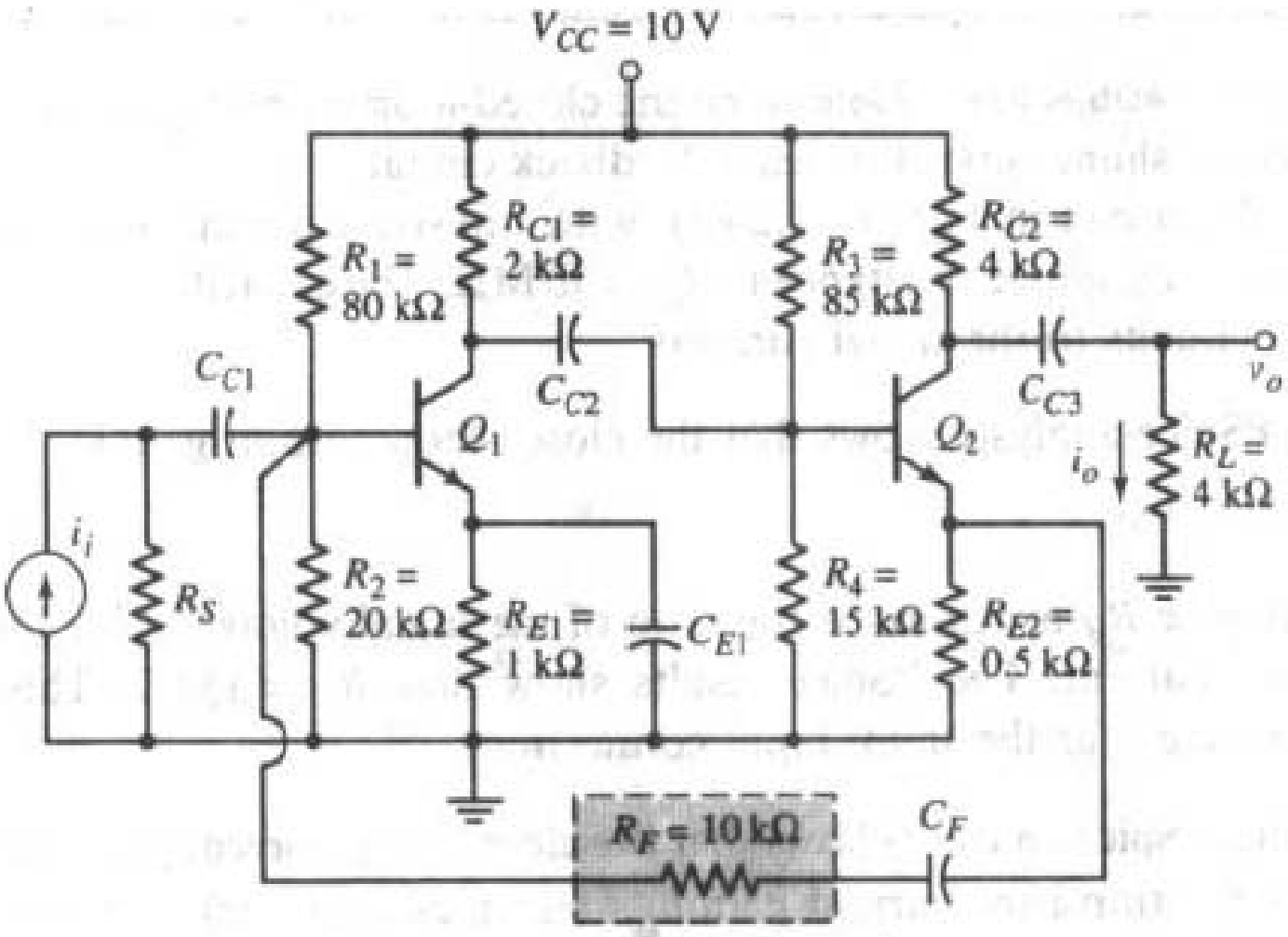
(a)

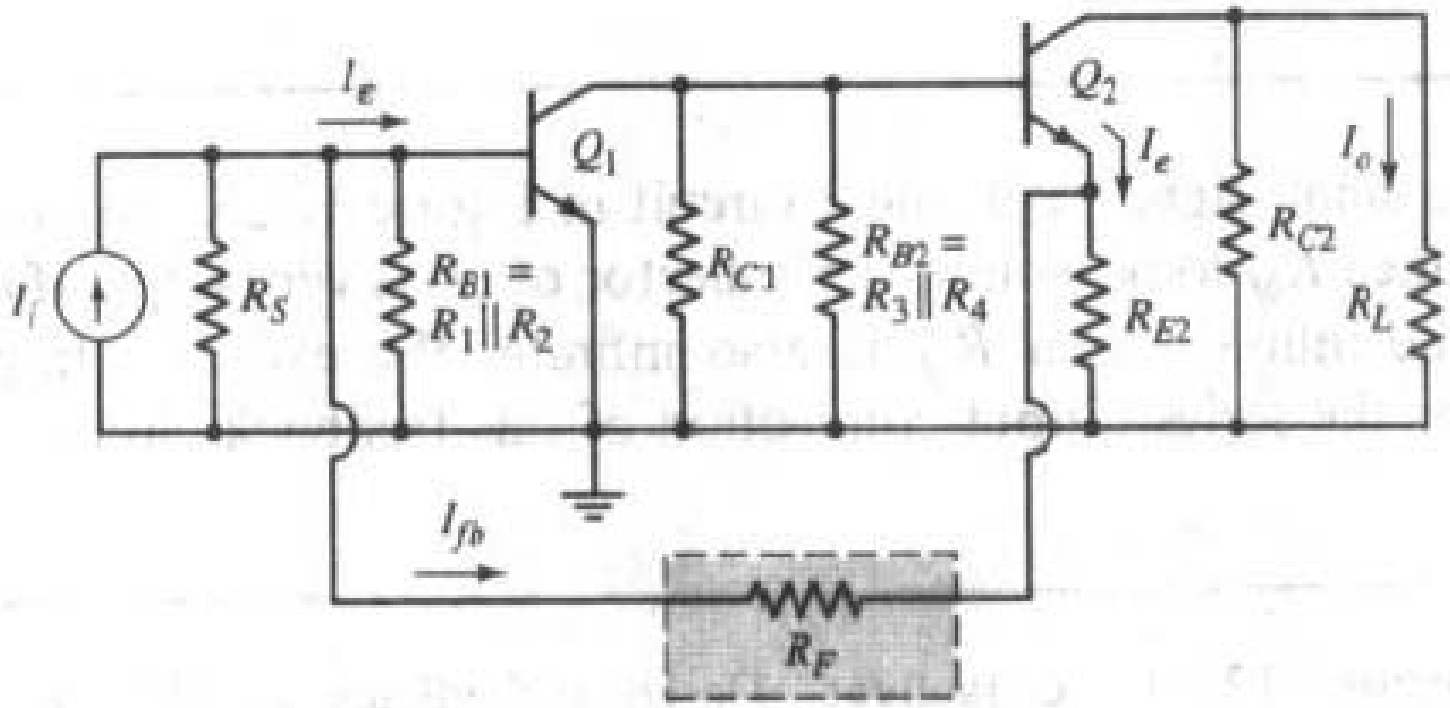
(b)

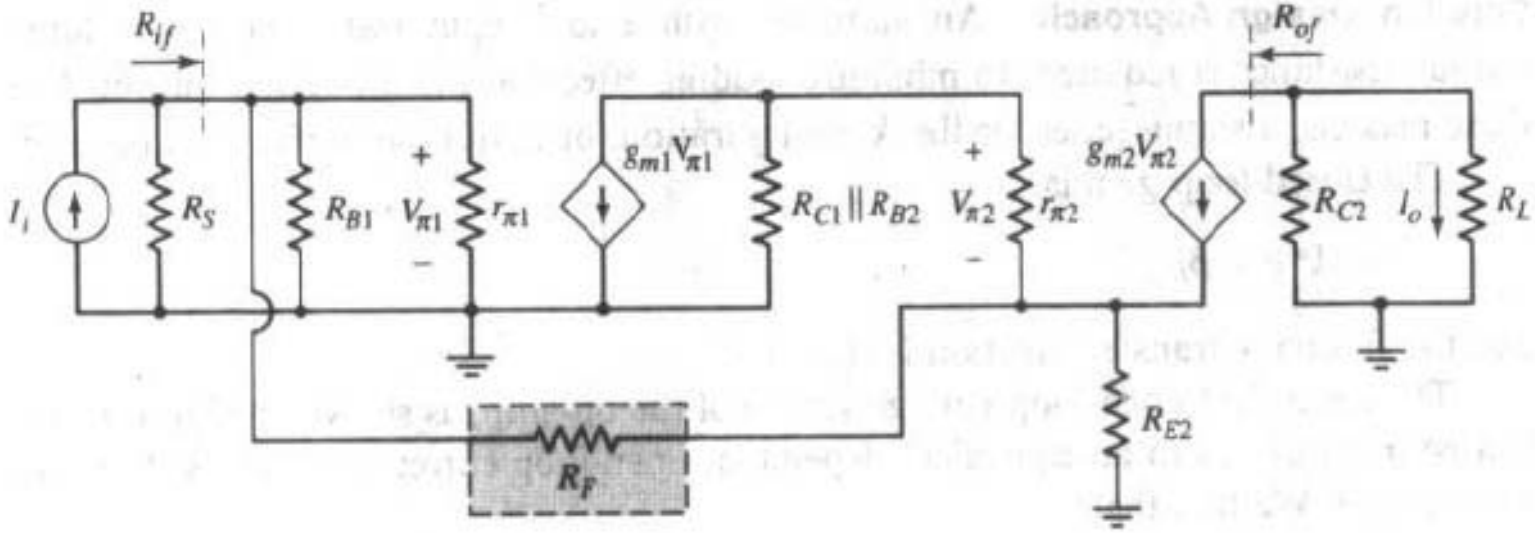
Figure 12.24 (a) Example of a discrete transistor shunt–series feedback circuit and (b) ac equivalent circuit

Figure 12.25 Small-signal equivalent circuit of circuit in Figure 12.24(a)

derive the expression for the closed-loop current gain by writing and solving a set of simultaneous nodal equations. However, as with most discrete transistor feedback circuits, the transfer function cannot be arranged exactly in the ideal form without several approximations. For this circuit, then, we rely on a computer analysis to provide the required results.


V_{CC} = 10 V
R_1 = 80 kΩ
R_{C1} = 2 kΩ
R_3 = 85 kΩ
R_{C2} = 4 kΩ
C_{C1}
C_{C2}
C_{C3}
Q_1
Q_2
v_o
i_o
R_L = 4 kΩ
i_i
R_S
R_2 = 20 kΩ
R_{E1} = 1 kΩ
C_{E1}
R_4 = 15 kΩ
R_{E2} = 0.5 kΩ
R_F = 10 kΩ
C_F


I_i
R_S
I_e
$R_{B1} = R_1 \| R_2$
Q_1
R_{C1}
$R_{B2} = R_3 \| R_4$
Q_2
I_e
R_{E2}
R_{C2}
I_o
R_L
I_{fb}
R_F


R_{if}
R_{of}
I_i
R_S
R_{B1}
$V_{\pi 1}$
$r_{\pi 1}$
$g_{m1}V_{\pi 1}$
$R_{C1} \| R_{B2}$
$V_{\pi 2}$
$r_{\pi 2}$
$g_{m2}V_{\pi 2}$
R_{C2}
i_o
R_L
R_{E2}
R_F

Example 12.9 **Objective:** Determine the closed-loop current gain and input resistance of a discrete shunt–series transistor feedback circuit.

Consider the circuit in Figure 12.24(a), with transistor parameters $h_{FE} = 100$ and $V_A = \infty$. Assume the source resistance is $R_S = 10\,\text{M}\Omega$. The capacitors are large enough to act as short circuits to the signal currents.

Solution: A PSpice analysis shows that the closed-loop current gain is

$$A_{if} = I_o/I_i = 9.58$$

The input resistance R_{if} is defined as the ratio of the signal voltage at the base of Q_1 to the input signal current. The PSpice results show that $R_{if} = 134\,\Omega$. This low input resistance is expected for the shunt input connection.

Comment: The PSpice analysis shows that the closed-loop current gain increases from 9.58 to 10.2 as the transistor current gain h_{FE} increases from 100 to 1000. This result again demonstrates a principal characteristic of feedback circuits, which is that the transfer function is relatively insensitive to changes in the individual transistor parameters.

From the small-signal equivalent circuit in Figure 12.25, we find that the output resistance R_{of} looking into the collector of Q_2 is very large. If r_o of Q_2 is assumed to be infinite, then R_{of} is also infinite. We expect a large output impedance for the series output connection of this feedback circuit.

Design Example 12.10 **Objective:** Design a feedback amplifier to provide a given current gain.

Assume that a signal current source has a nominal output resistance of $R_S = 10\,\text{k}\Omega$ and that the amplifier will drive a nominal load of $R_L = 50\,\Omega$. A current gain of 10 is required. An op-amp with the same characteristics described in Example 12.8 is available.

Solution: Design Approach: An amplifier with a low input resistance and a large output resistance is required, to minimize loading effects at the input and output. For these reasons, a shunt–series feedback configuration, or current amplifier, will be used.

The closed-loop gain is

$$A_{if} = 10 \cong 1/\beta_i$$

and the feedback transfer function is $\beta_i = 0.1$.

The dependent open-loop voltage source of the op-amp, as shown in Figure 12.17, can be transformed to an equivalent dependent open-loop current source, as shown in Figure 12.9. We find that

$$A_i = A_v R_i / R_o$$

Using the parameters specified for the op-amp, we find $A_i = 10^6$. The loop gain for the shunt–series configuration is

$$A_i\beta_i = (10^6)(0.1) = 10^5$$

Referring to Table 12.1, we expect the input resistance to be

$$R_{if} = 10/10^5\,\text{k}\Omega \rightarrow 0.1\,\Omega$$

and the output resistance to be

$$R_{of} = (100)(10^5)\,\Omega \rightarrow 10\,\text{M}\Omega$$

These resistance values will minimize any loading effects at the amplifier input and output.

For the shunt–series configuration in Figure 12.20, we have

$$\frac{1}{\beta_1} = 1 + \frac{R_F}{R_1} = 10$$

or

$$R_F/R_1 = 9$$

For our purposes, R_1 must be fairly small, to avoid a loading effect at the output. However, R_1 must not be too small, to avoid large currents in the amplifier. Therefore, we choose $R_1 = 1\,\text{k}\Omega$ and $R_F = 9\,\text{k}\Omega$.

Computer Simulation Verification: Figure 12.26 shows the circuit used in the computer simulation. A standard μA-741 op-amp was used in the circuit. The current gain was found to be exactly 10.0. The input resistance R_{if} looking into the op-amp with feedback was found to be 0.056 Ω, which compares favorably to the predicted value of 0.1 Ω. The output resistance seen by the load resistor was found to be approximately 200 MΩ. This value is on the order of 20 times larger than the predicted value, but is closer to the ideal value. The differences between predicted and measured values are due to the differences in assumed op-amp parameters and the μA-741 op-amp parameters.

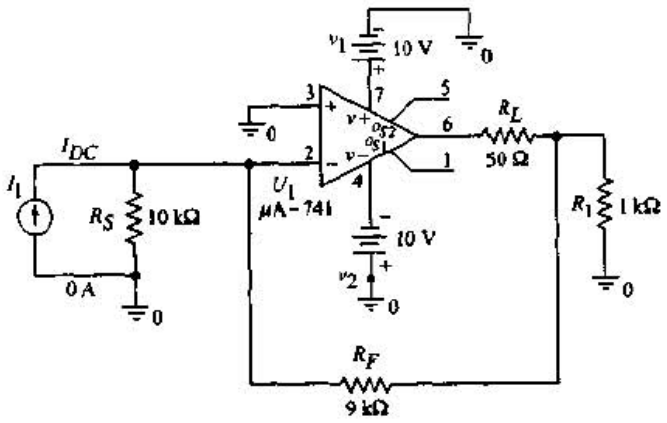


Figure 12.26 Circuit used in the computer simulation analysis in Example 12.10

Comment: This design also produces an almost ideal feedback current amplifier, if reasonable values of feedback resistors are used.

Test Your Understanding

***RD12.15** Consider the common-base circuit in Figure 12.23(a), with transistor parameters $h_{FE} = 80$, $V_{EB}(\text{on}) = 0.7\,\text{V}$, and $V_A = \infty$. Assume the transistor is biased at $I_{CQ} = 0.5\,\text{mA}$. Redesign the circuit such that the closed-loop current gain is greater than 0.95. (Ans. $R_E(\text{min}) = 1.30\,\text{k}\Omega$, and $V^+(\text{min}) = 1.36\,\text{V}$)

***12.16** Consider the shunt–series feedback circuit in Figure 12.24(a). Using a computer simulation analysis, investigate the magnitude of the current gain A_{if} as the emitter resistor R_{E2} is varied between 0.4 kΩ and 1.6 kΩ. What is the relationship between R_F, R_{E2}, and A_{if}?

***12.17** Consider the shunt–series feedback circuit in Figure 12.24(a). Using a computer simulation analysis, investigate the magnitude of the input resistance R_{if} as the feedback resistor R_F is varied between 5 kΩ and 50 kΩ. What is the influence of R_F on the input resistance R_{if}?

***D12.18** Design a feedback current amplifier to provide a current gain of 15. The nominal current source resistance is $R_S = 500\,\Omega$, and the nominal load is $R_L = 200\,\Omega$. An op-amp with parameters $R_i = 5\,\text{k}\Omega$, $R_o = 50\,\Omega$, and a low-frequency open-loop voltage gain of $A_v = 5 \times 10^3$ is available. Correlate the design with a PSpice analysis to determine the current gain, input resistance, and output resistance.

12.6 TRANSCONDUCTANCE (SERIES–SERIES) AMPLIFIERS

In this section, we will analyze an op-amp and a discrete circuit representation of the series–series feedback amplifier. The series–series circuit is a transconductance amplifier; therefore, we must derive the output current to input voltage transfer function. For the ideal configuration, this function is, from Equation (12.39),

$$A_{gf} = \frac{A_g}{(1 + \beta_z A_g)}$$

where A_g is the basic amplifier transconductance gain and β_z is the resistance feedback transfer function. We found that with this feedback configuration, both the input and output resistances increase compared to the basic amplifier values.

12.6.1 Op-Amp Circuit Representation

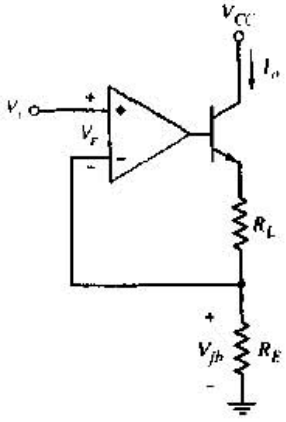


Figure 12.27 Example of an op-amp series–series feedback circuit

The op-amp circuit in Figure 12.27 is an example of the series–series feedback configuration. The input signal is the input voltage V_i, the feedback voltage is V_{fb}, and the error signal is the voltage V_E. The series output connection samples the output current, which means that the feedback voltage is a function of the output current.

In the ideal feedback circuit, the amplification factor A_g is very large; therefore, from Equation (12.39), the transfer function is

$$A_{gf} = \frac{I_o}{V_i} \cong \frac{1}{\beta_z} \tag{12.70}$$

Assuming an ideal op-amp circuit and neglecting the transistor base current, we have

$$V_i = V_{fb} = I_o R_E$$

and

$$A_{gf} = \frac{I_o}{V_i} = \frac{1}{R_E} \tag{12.71}$$

Comparing Equations (12.70) and (12.71), we see that the ideal feedback transfer function is

$$\beta_z = R_E \tag{12.72}$$

We can take a finite amplifier gain into account by considering the equivalent circuit in Figure 12.28. The parameter A_g is the open-loop transconductance gain of the amplifier. Assuming the collector and emitter currents are nearly equal and R_i is very large, we can write that

$$I_o = \frac{V_{fb}}{R_E} = h_{FE} I_b = h_{FE} A_g V_\varepsilon \tag{12.73}$$

Figure 12.28 Equivalent circuit, op-amp series–series feedback configuration

Also,

$$V_\varepsilon = V_i - V_{fb} = V_i - I_o R_E \tag{12.74}$$

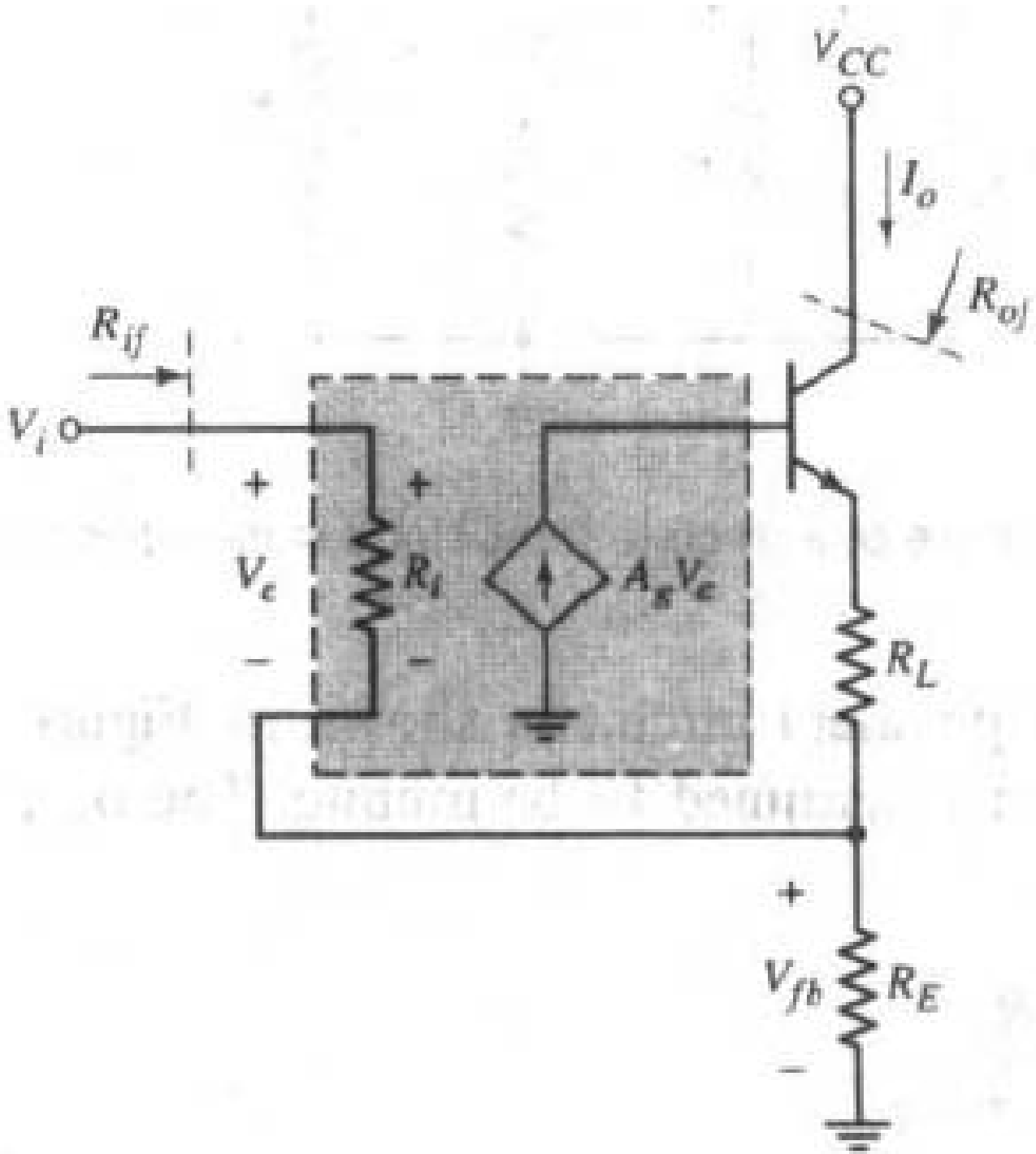
Substituting Equation (12.74) into Equation (12.73) yields

$$I_o = h_{FE} A_g (V_i - I_o R_E) \tag{12.75}$$

which can be rearranged to yield the closed-loop transfer function,

$$A_{gf} = \frac{I_o}{V_i} = \frac{(h_{FE} A_g)}{1 + (h_{FE} A_g) R_E} \tag{12.76}$$

which has the same form as that of the ideal theory. In this example, we see that in this feedback network, the transistor current gain is part of the basic amplifier gain.


V_{CC}
I_o
R_{of}
R_{if}
V_i
+
V_c
−
+
R_i
−
$A_g V_c$
R_L
+
V_{fb}
R_E
−

12.6.2 Discrete Circuit Representation

Figure 12.29 shows a single bipolar transistor circuit that is an example of a series–series feedback configuration. This circuit is similar to those evaluated in Chapters 3 and 4. The input signal is the input voltage v_i, the feedback voltage is v_{fb}, and the error signal is the base–emitter voltage. The series output connection samples the output current; therefore, the feedback voltage is a function of the output current.

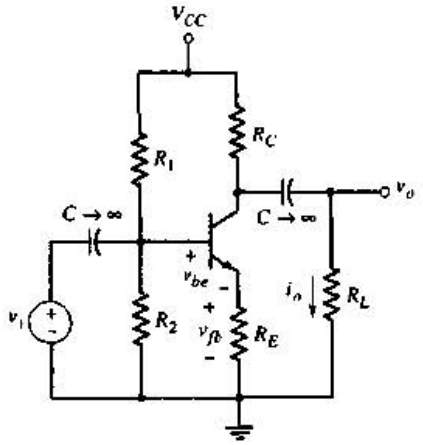


Figure 12.29 Example of a discrete transistor series–series feedback circuit

The small-signal equivalent circuit is shown in Figure 12.30. The Early voltage of the transistor is assumed to be infinite. The output current can be written

$$I_o = -(g_m V_\pi)\left(\frac{R_C}{R_C + R_L}\right) \tag{12.77}$$

and the feedback voltage is

$$V_{fb} = \left(\frac{V_\pi}{r_\pi} + g_m V_\pi\right) R_E \tag{12.78}$$

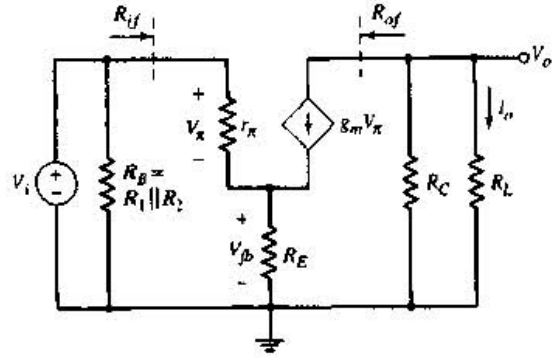


Figure 12.30 Small-signal equivalent circuit, discrete transistor series–series feedback configuration

A KVL equation around the B–E loop yields

$$V_i = V_\pi + V_{fb} = V_\pi\left[1 + \left(\frac{1}{r_\pi} + g_m\right)R_E\right] \tag{12.79}$$

Solving Equation (12.79) for V_π, substituting that into Equation (12.77), and rearranging terms produces the expression for the transconductance transfer function,

$$A_{gf} = \frac{I_o}{V_i} = \frac{-g_m\left(\dfrac{R_C}{R_C + R_L}\right)}{1 + \left(\dfrac{1}{r_\pi} + g_m\right)R_E} \tag{12.80}$$

Again, the closed-loop transfer function of the discrete transistor feedback circuit cannot be put in exactly the same form as that of the ideal series–series feedback network. Resistor R_C introduces loading on the output, and r_π introduces loading on the input. If both R_C and r_π become large, then Equation (12.80) changes to the ideal form, where the feedback transfer function is $\beta_z = -R_E$ and the basic amplifier transconductance is $A_g = -g_m$.

Example 12.11 **Objective:** Determine the transconductance gain of a transistor feedback circuit.

Consider the circuit in Figure 12.29, with transistor parameters $h_{FE} = 100$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, and $V_A = \infty$. The circuit parameters are: $V_{CC} = 10\,\text{V}$, $R_1 = 55\,\text{k}\Omega$, $R_2 = 12\,\text{k}\Omega$, $R_E = 1\,\text{k}\Omega$, $R_C = 4\,\text{k}\Omega$, and $R_L = 4\,\text{k}\Omega$.

Solution: From a dc analysis of the circuit, the quiescent values are $I_{CQ} = 0.983\,\text{mA}$ and $V_{CEQ} = 5.08\,\text{V}$. The transistor small-signal parameters are

$$r_\pi = \frac{h_{FE}V_T}{I_{CQ}} = \frac{(100)(0.026)}{0.983} = 2.64\,\text{k}\Omega$$

and

$$g_m = \frac{I_{CQ}}{V_T} = \frac{0.983}{0.026} = 37.8\,\text{mA/V}$$

From Equation (12.80), the transconductance transfer function is

$$A_{gf} = \frac{-(37.8)\left(\dfrac{4}{4+4}\right)}{1 + \left(\dfrac{1}{2.64} + 37.8\right)(1)} = -0.482\,\text{mA/V}$$

As a first approximation, we have

$$A_{gf} = \frac{1}{\beta_z} \approx \frac{1}{-R_E} = \frac{1}{-1\,\text{k}\Omega} = -1\,\text{mA/V}$$

The term $R_C/(R_C + R_L)$ introduces the largest discrepancy between the actual and ideal transconductance values.

This circuit is often used as a voltage amplifier. The output voltage is directly proportional to the output current. Therefore,

$$A_{vf} = \frac{v_o}{v_i} = \frac{i_o R_L}{v_i} = A_{gf}R_L$$

which yields

$$A_{vf} = (-0.482)(4) = -1.93$$

Comment: The circuit in Figure 12.29 is an example of a series–series feedback topology, even though in many cases we treat this circuit as a voltage amplifier. When an emitter resistor is included, the small-signal voltage gain decreases, because of the feedback effect of R_E. However, the transconductance and voltage gain become insensitive to the transistor parameters, also a result of the feedback effect of R_E. A 100 percent increase in the transistor current gain h_{FE} produces a 0.5 percent change in the closed-loop voltage gain.

The input resistance R_{if} of the series input feedback connection includes R_E multiplied by $(1 + h_{FE})$, where h_{FE} is the transistor current gain. The input resistance increases significantly because of the series connection.

The output resistance of a series output feedback connection is usually very large. However, resistance R_C reduces the output resistance and introduces a loading effect. The reduced output resistance demonstrates that discrete transistor feedback circuits do not conform exactly to ideal feedback circuits. Nevertheless, overall circuit characteristics improve when feedback is used.

Design Example 12.12 **Objective:** Design a driver amplifier to supply current to an LED.

The available voltage source is variable from 0 to 5 V and has an output resistance of 200 Ω. The required diode current is 10 mA when the maximum input voltage is applied. The required closed-loop transconductance gain is then $A_{gf} = I_o/V_i = (10 \times 10^{-3})/5 \rightarrow 2$ mS. An op-amp with the characteristics described in Example 12.8 and a BJT with $h_{FE} = 100$ are available.

Solution: Design Approach: To minimize loading effects on the input, an amplifier with a large input resistance is required; to minimize loading effects on the output, a large output resistance is required. For these reasons, a series–series feedback configuration, or transconductance amplifier, is selected.

The closed-loop gain is

$$A_{gf} = 2 \times 10^{-3} \cong 1/\beta_z$$

and the resistance feedback transfer function is

$$\beta_z = 500\,\Omega$$

The dependent open-loop voltage source of the op-amp, as shown in Figure 12.17, can be transformed to an equivalent dependent op-loop transconductance source for the transconductance amplifier, as shown in Figure 12.12. We find that

$$A_g = A_v/R_o$$

The parameters specified for the op-amp yield

$$A_g = 100\ \text{A/V}$$

The loop gain for the series–series configuration is

$$A_g\beta_z = (100)(500) = 5 \times 10^4$$

Referring to Table 12.1, the expected input resistance is

$$R_{if} = (10)(5 \times 10^4)\,\text{k}\Omega \rightarrow 500\,\text{M}\Omega$$

and the expected output resistance is

$$R_{of} = (100)(5 \times 10^4)\,\Omega \rightarrow 5\,\text{M}\Omega$$

These input and output resistances should minimize any loading effects at the amplifier input and output.

For this example, we may use the amplifier configuration shown in Figure 12.27, in which the load resistor R_L is replaced by an LED. In the ideal case,

$$\beta_z = R_E = 500\,\Omega$$

Computer Simulation Verification: Figure 12.31 shows the circuit used in the computer simulation. Again, a standard μA-741 op-amp was used in the circuit and a standard diode was used in place of an LED. When the input voltage reached 5 V, the current through the diode was 10.0 mA, which was the design value. The input resistance R_{if} was found to be approximately 2400 MΩ and the output resistance R_{of} was found to be approximately 60 MΩ. Both of these values are larger than predicted because of the differences in the assumed op-amp parameters and those of the μA-741 op-amp.

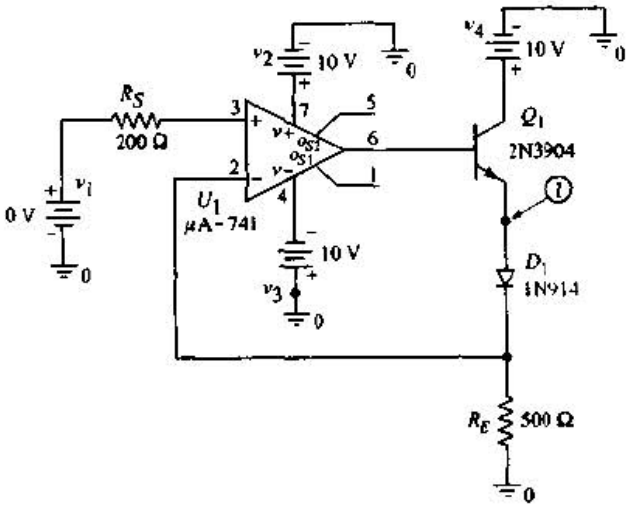


Figure 12.31 Circuit used in the computer simulation analysis for Example 12.12

Comment: Again, an almost ideal feedback circuit can be designed by using an op-amp.

Test Your Understanding

12.19 Consider the op-amp circuit in Figure 12.27, with parameters $R_E = 1\,\text{k}\Omega$ and $A_v = 10^3$ A/V. Assume the transistor current gain is $h_{FE} = 200$. (a) Determine the transfer function $A_{gf} = I_o/V_i$. (b) If the amplifier gain increases by a factor of 10, determine the percent change in the transconductance transfer function. (Ans. (a) $A_{gf} = 1$ mA/V (b) $4.5 \times 10^{-7}\,\% \cong 0\%$)

12.20 For the circuit in Figure 12.32, the transistor parameters are: $K_n = 1.5\,\text{mA/V}^2$, $V_{TN} = 2\,\text{V}$, and $\lambda = 0$. (a) Determine the transconductance transfer function $A_{gf} = i_o/v_i$. (b) Determine the percent change in A_{gf} if the transistor conduction parameter decreases to $K_n = 1\,\text{mA/V}^2$. (Ans. (a) $A_{gf} = -0.732\,\text{mA/V}$ (b) A_{gf}, 12.7% decrease)

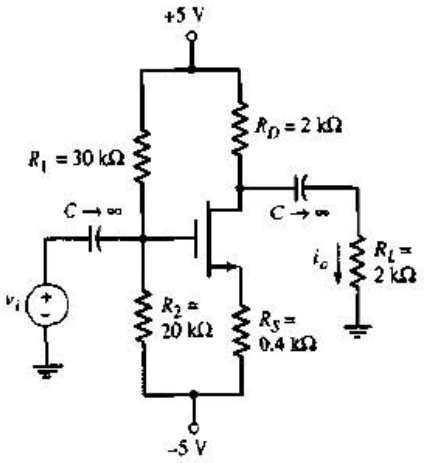


Figure 12.32 Figure for Exercise 12.20

***D12.21** Design a transconductance feedback amplifier with a gain of $A_{gf} = 10\,\text{mS}$. The source resistance is $R_S = 500\,\Omega$, and the load is an LED. State any necessary assumptions. Use an op-amp with the characteristics described in Example 12.8. From a computer simulation analysis, determine the closed-loop transconductance, input resistance, and output resistance of your design.

12.7 TRANSRESISTANCE (SHUNT–SHUNT) AMPLIFIERS

In this section, we will analyze an op-amp and a discrete circuit representation of the shunt–shunt feedback amplifier. The shunt–shunt circuit is a transresistance amplifier; therefore, we must derive the output voltage to input current transfer function. For the ideal configuration, this function is given by Equation (12.40) as

$$A_{zf} = \frac{A_z}{(1 + \beta_g A_z)}$$

where A_z is the basic amplifier transresistance gain, and β_g is the feedback transfer function. With this feedback connection, both the input and output resistance decrease compared to the basic amplifier values.

12.7.1 Op-Amp Circuit Representation

Figure 12.33 shows an inverting op-amp circuit, which is an example of the shunt–shunt configuration. The input signal is the input current I_i, the feedback current is I_{fb}, and the error signal is the current I_e. The shunt output

Figure 12.33 Example of an op-amp shunt–shunt feedback circuit

samples the output voltage; therefore, the feedback current is a function of the output voltage.

In the ideal feedback circuit, the amplification factor A_z is very large, and the transresistance transfer function is, from Equation (12.40),

$$A_{zf} = \frac{V_o}{I_i} \cong \frac{1}{\beta_g} \tag{12.81}$$

For the ideal inverting op-amp circuit, V_1 is at virtual ground, and

$$V_o = -I_{fb}R_2$$

Also for the ideal op-amp, $I_{fb} = I_i$, and the ideal transresistance transfer function is

$$A_{zf} = \frac{V_o}{I_i} = -R_2 \tag{12.82}$$

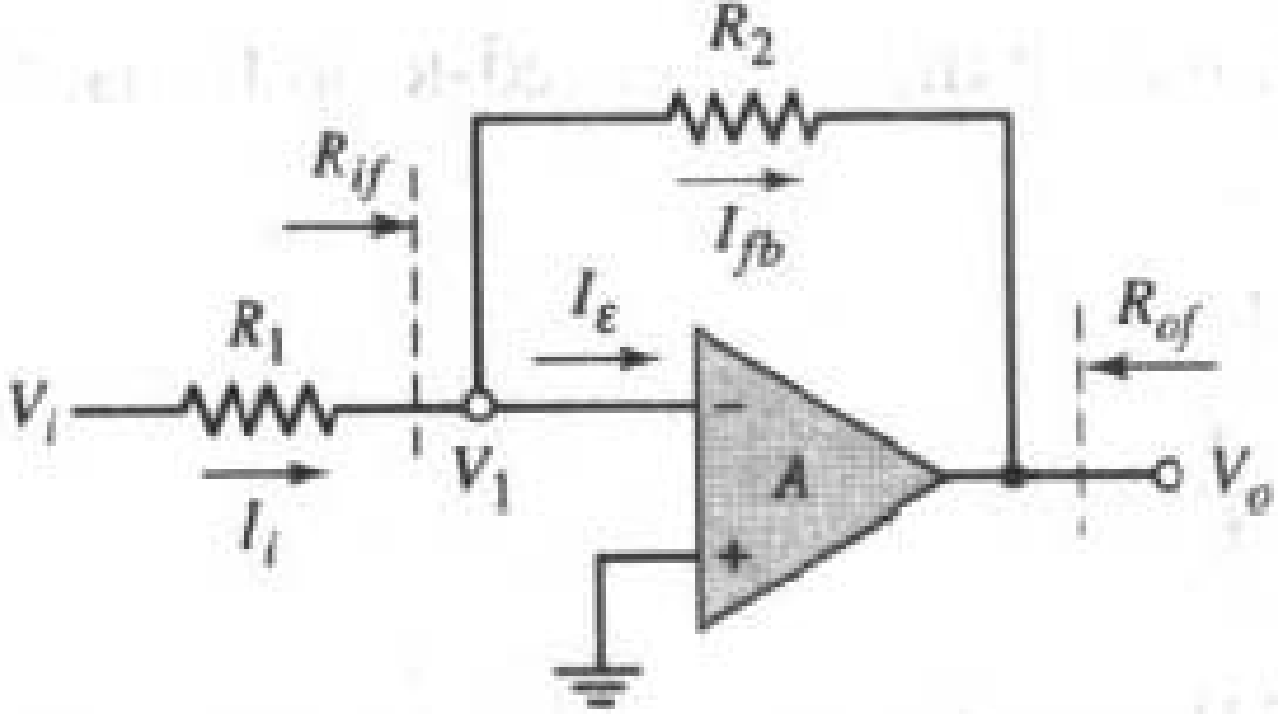
Comparing Equation (12.82) to Equation (12.81), we see that the feedback transfer function for the ideal inverting op-amp circuit is

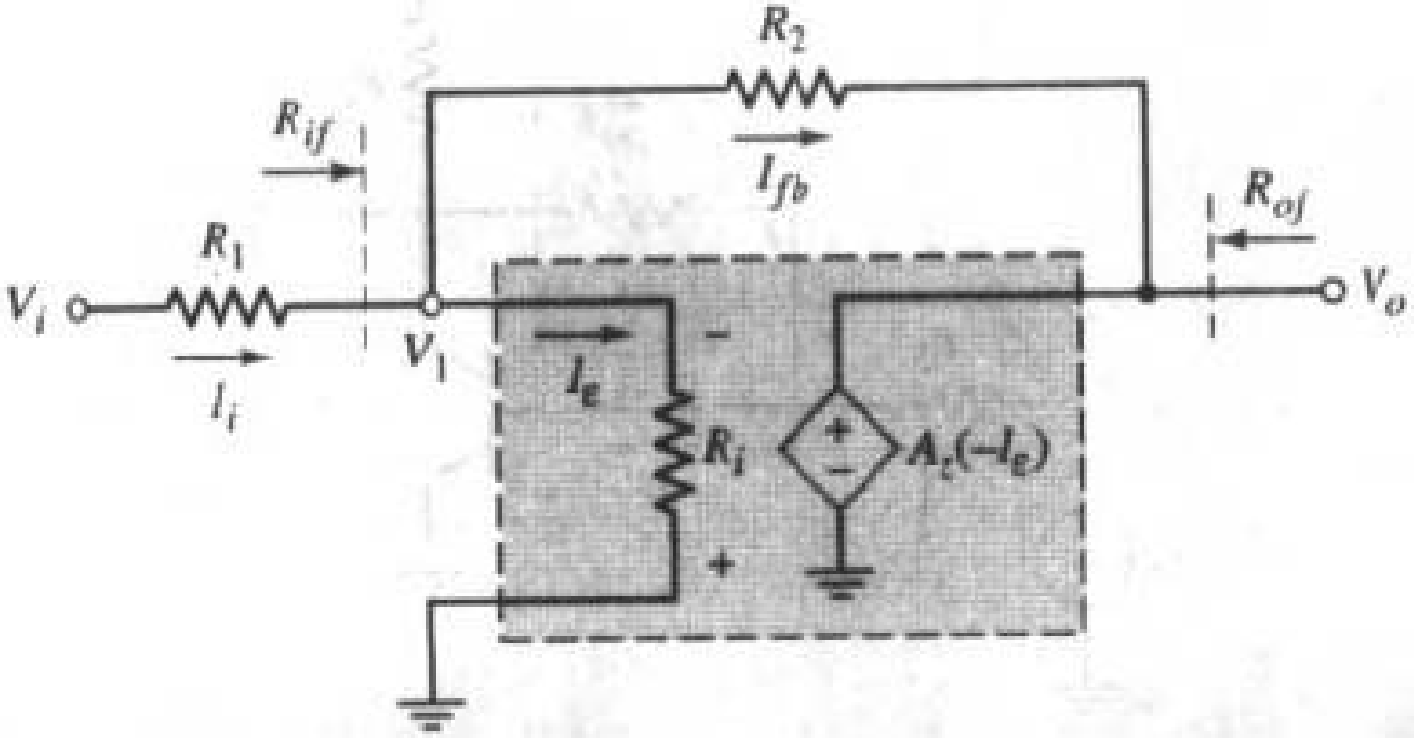
$$\beta_g = -\frac{1}{R_2} \tag{12.83}$$

We can take a finite amplifier gain into account by considering the equivalent circuit in Figure 12.34. The parameter A_z is the open-loop transresistance gain factor, and the minus sign indicates that the error signal current is entering the inverting terminal. Therefore, we can write $V_o = -A_z I_\varepsilon$, $I_\varepsilon = I_i - I_{fb}$, and $V_o = -A_z(I_i - I_{fb})$. If we assume that voltage V_1 is at virtual ground, then

$$I_{fb} = -V_o/R_2$$

Figure 12.34 Equivalent circuit, op-amp shunt-shunt feedback configuration


R_2
R_{if}
I_{fb}
I_ε
R_1
R_{of}
V_i
V_1
A
V_o
I_i


R_2
R_{if}
I_{fb}
R_{of}
R_1
V_i
V_o
V_1
I_i
I_e
R_i
$A_v(-I_e)$

Combining equations, we see that the closed-loop transresistance transfer function is

$$A_{zf} = \frac{V_o}{I_i} = \frac{-A_z}{\left(1 + \frac{A_z}{R_2}\right)} \tag{12.84}$$

From Equation (12.83), the feedback transfer function is $\beta_g = -1/R_2$, and Equation (12.84) becomes

$$A_{zf} = \frac{V_o}{I_i} = \frac{(-A_z)}{1 + (-A_z)\beta_g} \tag{12.85}$$

This feedback circuit is one example in which the gain of the basic amplifier, $A_z = V_o/I_s$, is negative and the feedback transfer function, $\beta_g = -1/R_2$, is also negative, but the loop gain $T = \beta_g A_z$ is positive for a negative feedback circuit.

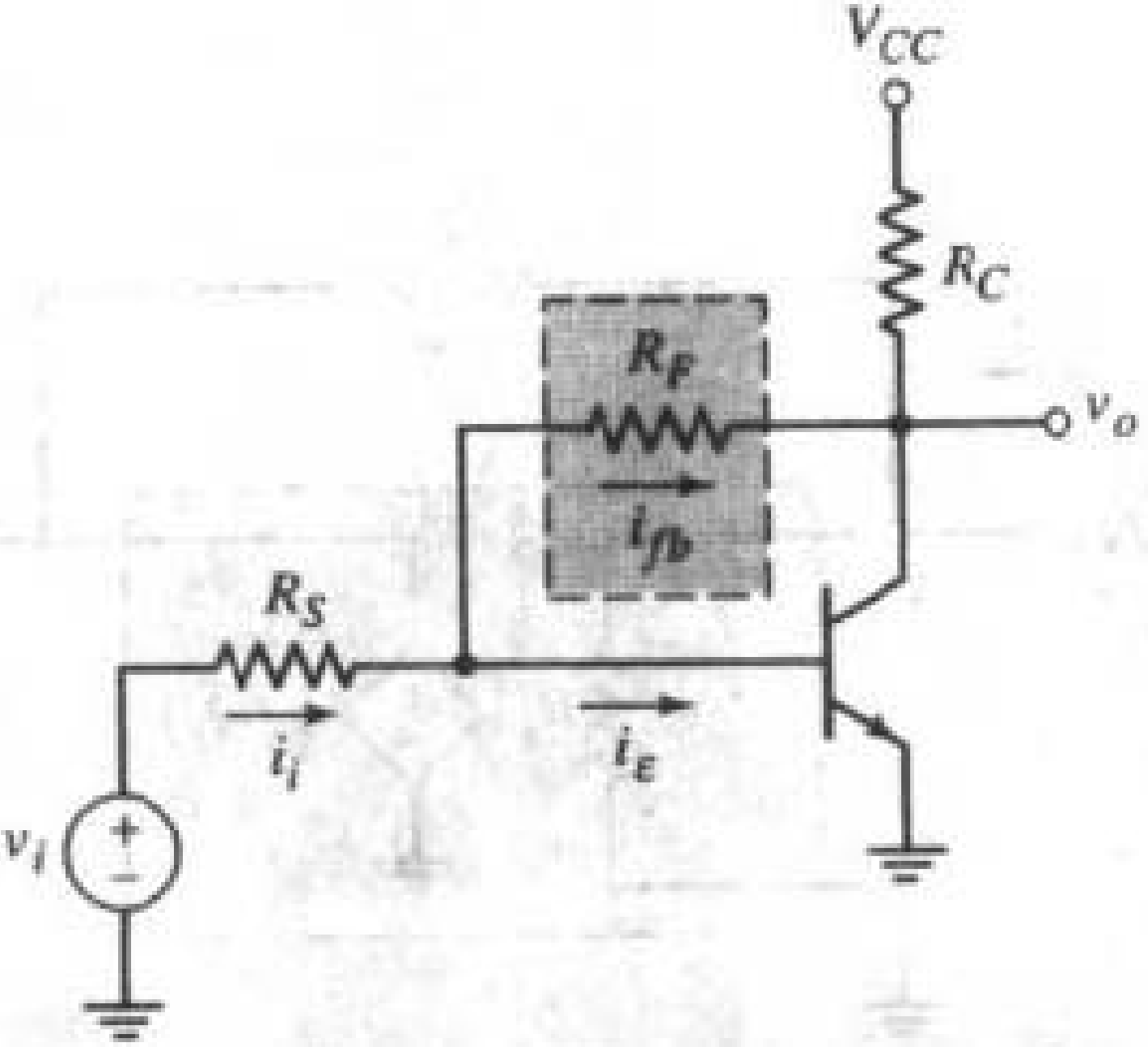
The transresistance transfer function for the inverting op-amp circuit has the same form as that for the ideal shunt–shunt configuration. In addition, since V_1 is at virtual ground, the input resistance including feedback, R_{if}, is essentially zero, and we have shown that the output resistance with feedback, R_{of}, is very small. These small resistance values are a result of the shunt–shunt configuration. Therefore, our analysis of the inverting op-amp circuit produces results consistent with ideal shunt–shunt feedback characteristics.

The inverting amplifier circuit in Figure 12.33 is most often thought of as a voltage amplifier. The input current I_i is directly proportional to the input voltage V_i, which means that the voltage transfer function (gain) and transresistance transfer function have the same characteristics. Even though we are usually concerned with the voltage gain, the inverting amplifier is an example of a shunt–shunt feedback topology which is a transresistance amplifier.

12.7.2 Discrete Circuit Representation

Figure 12.35 shows a single bipolar transistor circuit, which is an example of a shunt–shunt feedback configuration. The input signal current is I_i, the feedback current is i_{f0}, and the error signal current is i_e and is the signal base

Figure 12.35 Example of a discrete transistor shunt–shunt feedback circuit


V_{CC}
R_C
R_F
v_o
i_{fb}
R_S
i_i
i_ε
v_i

current. The shunt output samples the output voltage; therefore, the feedback current is a function of v_o.

The small-signal equivalent circuit is shown in Figure 12.36. The input signal is assumed to be an ideal signal current source. Also the Early voltage of the transistor is assumed to be infinite.

Figure 12.36 Small-signal equivalent circuit, discrete transistor shunt–shunt feedback configuration

Writing a KCL equation at the output node, we find

$$\frac{V_o}{R_C} + g_m V_\pi + \frac{V_o - V_\pi}{R_F} = 0 \tag{12.86}$$

A KCL equation at the input node yields

$$I_i = \frac{V_\pi}{r_\pi} + \frac{V_\pi - V_o}{R_F} \tag{12.87}$$

Solving Equation (12.87) for V_π and substituting that result into Equation (12.86), we obtain

$$V_o\left(\frac{1}{R_C} + \frac{1}{R_F}\right)\left(\frac{1}{r_\pi} + \frac{1}{R_F}\right) + \left(g_m - \frac{1}{R_F}\right)\left(I_i + \frac{V_o}{R_F}\right) = 0 \tag{12.88}$$

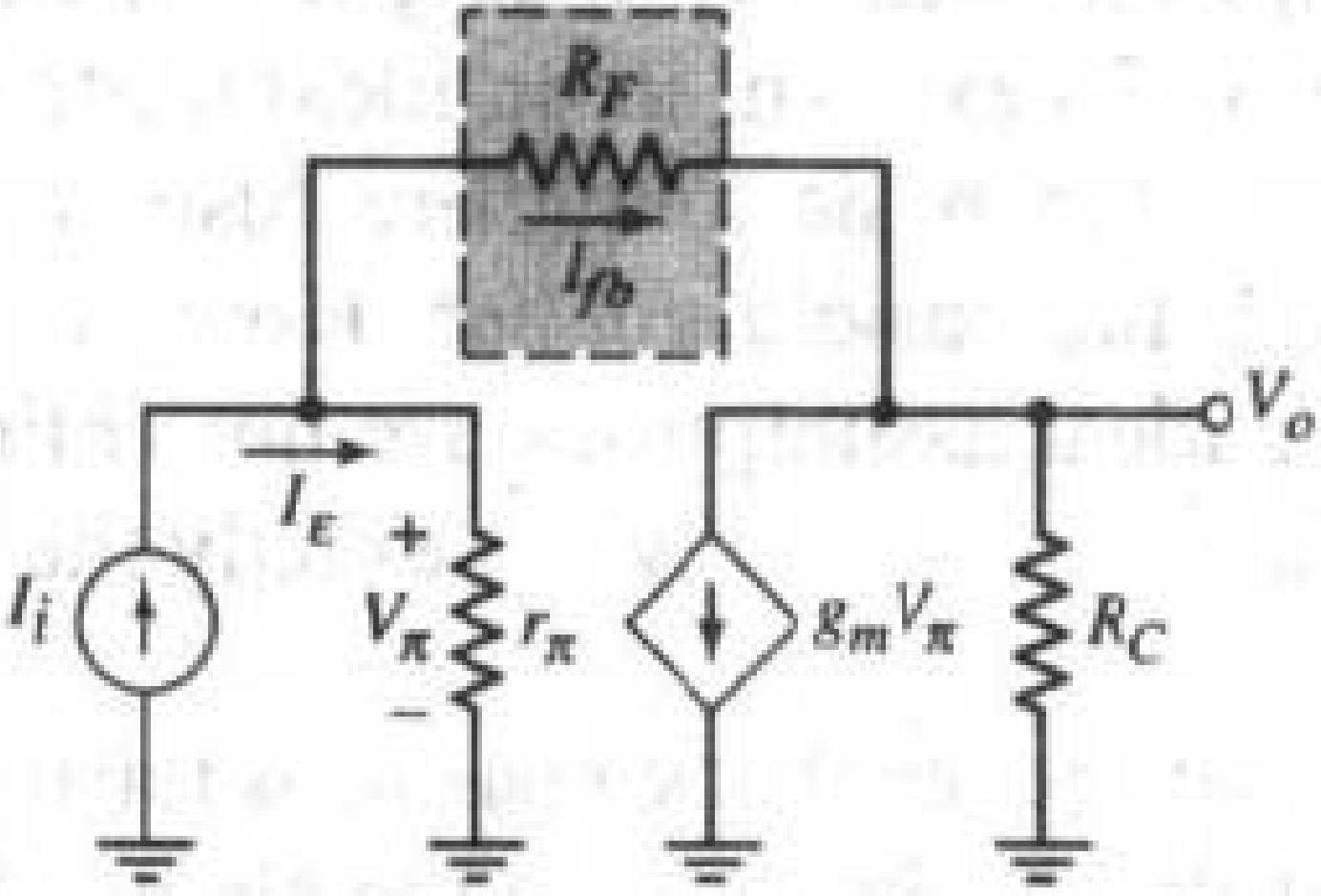
The transresistance transfer function is then

$$A_{zf} = \frac{V_o}{I_i} = \frac{-\left(g_m - \dfrac{1}{R_F}\right)}{\left(\dfrac{1}{R_C} + \dfrac{1}{R_F}\right)\left(\dfrac{1}{r_\pi} + \dfrac{1}{R_F}\right) + \dfrac{1}{R_F}\left(g_m - \dfrac{1}{R_F}\right)} \tag{12.89}$$

The open-loop transresistance gain factor A_z is found by setting $R_F = \infty$. We find

$$A_z = \frac{-g_m}{\left(\dfrac{1}{R_C}\right)\left(\dfrac{1}{r_\pi}\right)} = -g_m r_\pi R_C = -h_{FE} R_C \tag{12.90}$$

where h_{FE} is the common-emitter transistor current gain. Multiplying both numerator and denominator of Equation (12.89) by $(r_\pi R_C)$, we obtain the closed-loop transresistance gain,


R_F
I_{fb}
V_o
I_i
I_ε
+
V_π
−
r_π
$g_m V_\pi$
R_C

$$A_{zf} = \frac{V_o}{I_i} = \frac{+\left(A_z + \dfrac{r_\pi R_C}{R_F}\right)}{\left(1 + \dfrac{R_C}{R_F}\right)\left(1 + \dfrac{r_\pi}{R_F}\right) - \dfrac{1}{R_F}\left(A_z + \dfrac{r_\pi R_C}{R_F}\right)} \tag{12.91}$$

The closed-loop transresistance gain for the single-transistor feedback circuit cannot be put into the ideal form, as given in Equation (12.40), without further approximations. To explain, in an ideal feedback circuit, the feedback network does not load the basic amplifier. Also, the forward transmission occurs entirely through the basic amplifier. However, in a discrete transistor feedback circuit, these ideal assumptions are not entirely valid; therefore, the form of the transfer function is usually not exactly the same as that of the ideal configuration.

We may assume that the feedback resistor is fairly large, which means that the feedback does not drastically perturb the circuit. We may then assume

$$h_{FE} = g_m r_\pi \gg (r_\pi / R_F)$$

If we also assume that $R_C \ll R_F$ and $r_\pi \ll R_F$, then Equation (12.91) reduces to

$$A_{zf} = \frac{V_o}{I_i} \cong \frac{A_z}{1 + (A_z)\left(\dfrac{-1}{R_F}\right)} \tag{12.92}$$

Consequently, the feedback transfer function is approximately

$$\beta_g \cong \frac{-1}{R_F} \tag{12.93}$$

Equation (12.93) demonstrates that the approximate value of the feedback transfer function depends only on a resistance value.

Although the actual closed-loop transfer function does not fit the ideal form, the magnitude of that function depends less on the individual transistor parameters than does the open-loop gain. This characteristic is one of the general properties of feedback circuits.

Also, since the input current is proportional to the input voltage, we can use this circuit as a voltage amplifier.

Example 12.13 **Objective:** Determine the transresistance and voltage gain of a single-transistor shunt–shunt feedback circuit.

Consider the circuit in Figure 12.37(a). The transistor parametes are: $h_{FE} = 100$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, and $V_A = \infty$. Since the input signal current is directly proportional to the input voltage, the voltage gain of this shunt–shunt configuration has the same general properties as the transresistance transfer function.

As with many circuits considered in this chapter, several capacitors are included. In the circuit in Figure 12.37(a), R_1 and C_{C2} may be removed. Resistor R_F can be used for biasing, and the circuit can be redesigned to provide the same feedback properties.

Solution: By including C_{C2} in the circuit, the feedback is a function of the ac signal only, which means that the transistor quiescent values are not affected by feedback. The quiescent parameters are found to be

(b)

Figure 12.37 (a) Circuit for Example 12.13 and (b) small-signal equivalent circuit

$$I_{CQ} = 0.492\,\text{mA} \quad \text{and} \quad V_{CEQ} = 5.08\,\text{V}$$

The small-signal transistor parameters are

$$r_\pi = \frac{h_{FE} V_T}{I_{CQ}} = \frac{(100)(0.026)}{0.492} = 5.28\,\text{k}\Omega$$

and

$$g_m = \frac{I_{CQ}}{V_T} = \frac{0.492}{0.026} = 18.9\,\text{mA/V}$$

In the small-signal equivalent circuit, which is shown in Figure 12.37(b), the Thevenin equivalent input source is converted to a Norton equivalent circuit. Writing a KCL equation at the output, we obtain

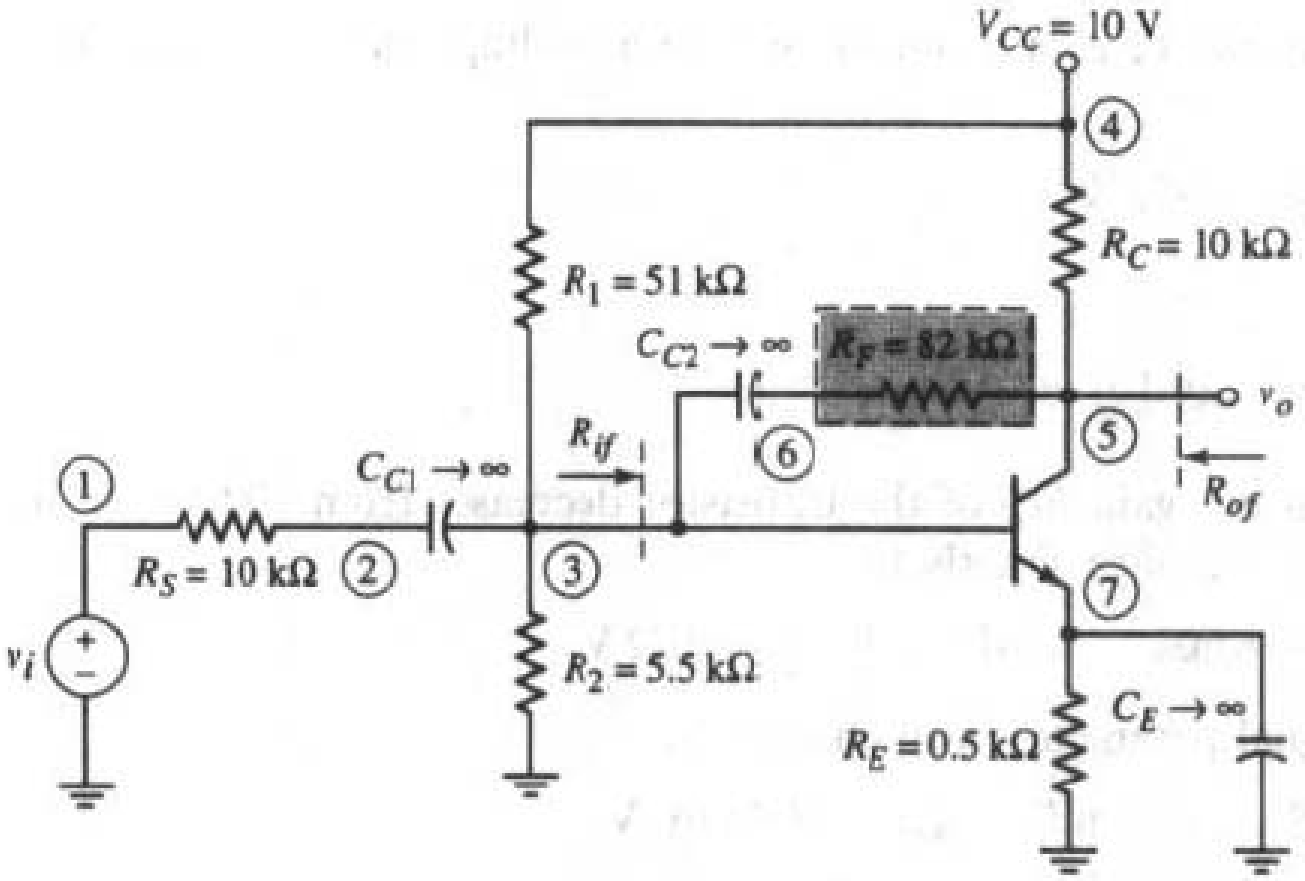
$$\frac{V_o}{10} + (18.9)V_\pi + \frac{V_o - V_\pi}{82} = 0$$

A KCL equation at the input yields

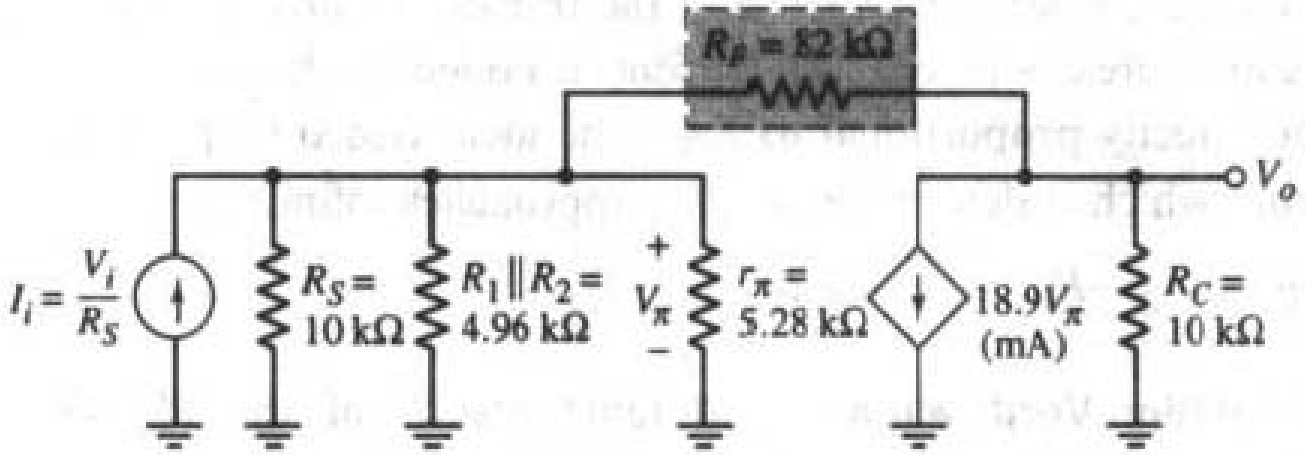
$$I_i = \frac{V_\pi}{10} + \frac{V_\pi}{4.96} + \frac{V_\pi}{5.28} + \frac{V_\pi - V_o}{82}$$

Combining these two equations and eliminating V_π, we find the small-signal transresistance gain, which is

$$A_{sf} = \frac{V_o}{I_i} = -65.8\,\text{k}\Omega$$


$V_{CC} = 10$ V
4
$R_C = 10$ kΩ
$R_1 = 51$ kΩ
$C_{C2} \to \infty$
$R_F = 82$ kΩ
v_o
5
R_{if}
6
$C_{C1} \to \infty$
1
R_{of}
$R_S = 10$ kΩ
2
3
7
v_i
$R_2 = 5.5$ kΩ
$C_E \to \infty$
$R_E = 0.5$ kΩ

(a)


$R_F = 82$ kΩ
V_o
$I_i = \frac{V_i}{R_S}$
$R_S =$ 10 kΩ
$R_1 \| R_2 =$ 4.96 kΩ
+
V_π
−
$r_\pi =$ 5.28 kΩ
$18.9V_\pi$ (mA)
$R_C =$ 10 kΩ

Since this unit of gain is not as familiar as voltage gain, we determine the voltage gain from

$$I_i = V_i/R_S = V_i/10$$

Therefore,

$$\frac{V_o}{V_i} = -(65.8)(0.10) = -6.58$$

If the current gain h_{FE} of the transistor decreases from 100 to 75, the transistor quiescent values change slightly to

$$I_{CQ} = 0.478\,\text{mA} \quad \text{and} \quad V_{CEQ} = 5.22\,\text{V}$$

The small-signal parameters also change, to

$$r_\pi = 4.08\,\text{k}\Omega \quad \text{and} \quad g_m = 18.4\,\text{mA/V}$$

and the closed-loop small-signal voltage gain becomes

$$V_o/V_i = -6.41$$

Comment: With a 25 percent decrease in the transistor current gain h_{FE}, the closed-loop voltage gain decreases by only 2.6 percent. If no feedback were present, the voltage gain would be directly proportional to h_{FE}. The ideal closed-loop voltage gain of the feedback circuit, which is determined as h_{FE} approaches infinity, is

$$A_v(h_{FE} \to \infty) = -R_F/R_S = -7.20$$

Computer Simulation Verification: Additional results of the PSpice analysis are shown in Figure 12.38. The magnitude of the voltage gain is plotted as a function of the transistor current gain h_{FE}, for three values of feedback resistance. The results for $R_F = 82\,\text{k}\Omega$ agree very well with the results from the hand analysis. As R_F increases to 160 kΩ, there is less feedback, and the magnitude of the voltage gain increases. However, the variation in the closed-loop gain is substantially greater as the transistor gain changes. In contrast, when R_F decreases to 47 kΩ, there is increased feedback, and

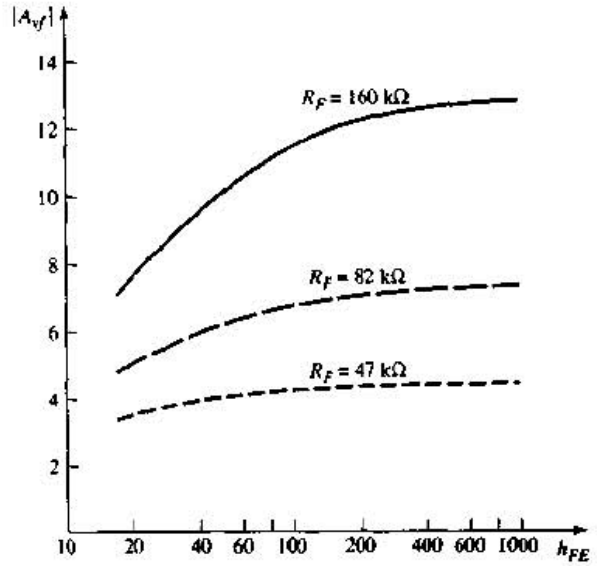


Figure 12.38 Voltage gain magnitude versus transistor current gain, for three values of feedback resistance, from a PSpice analysis of the circuit in Figure 12.37(a)

the magnitude of the voltage gain decreases. However, there is very little variation in closed-loop gain as the transistor gain changes. In all cases, as the gain of the transistor increases, there is less change in closed-loop gain. This result demonstrates the need for a large gain in the basic amplifier in the feedback network.

Expressions for the input and output resistances of the ideal shunt–shunt configuration are given in Equations (12.35) and (12.28), respectively. As with the loop gain function, the input and output resistance expressions for the single-transistor feedback circuit cannot be put in exactly the same form as that for the ideal configuration. However, the same general characteristics are obtained; that is, both input and output resistances decrease, predicted by the ideal case.

Example 12.14 **Objective:** Determine the input and output resistances of a single-transistor shunt–shunt feedback circuit.

Consider the circuit in Figure 12.37(a), with transistor parameters: $h_{FE} = 100$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, and $V_A = \infty$.

Solution: The small-signal equivalent circuit for calculating the input resistance R_{if} is shown in Figure 12.39(a). The small-signal transistor parameters were determined in Example 12.13.

(a) (b)

Figure 12.39 Small-signal equivalent circuits of the circuit in Figure 12.37(a) for calculating (a) input resistance and (b) output resistance

Writing a KCL equation at the input, we have

$$I_x = \frac{V_\pi}{r_\pi} + \frac{V_\pi - V_o}{R_F} = \frac{V_\pi}{5.28} + \frac{V_\pi - V_o}{82}$$

From a KCL equation at the output node, we have

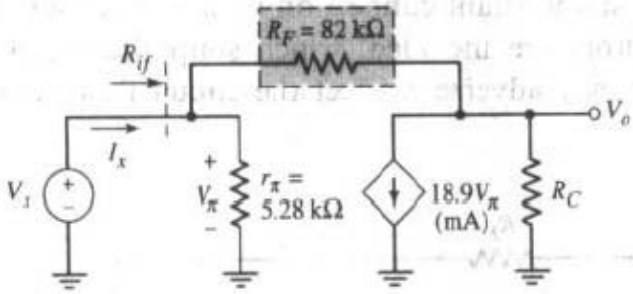
$$\frac{V_o}{R_C} + g_m V_\pi + \frac{V_o - V_\pi}{R_F} = \frac{V_o}{10} + (18.9)V_\pi + \frac{V_o - V_\pi}{82} = 0$$

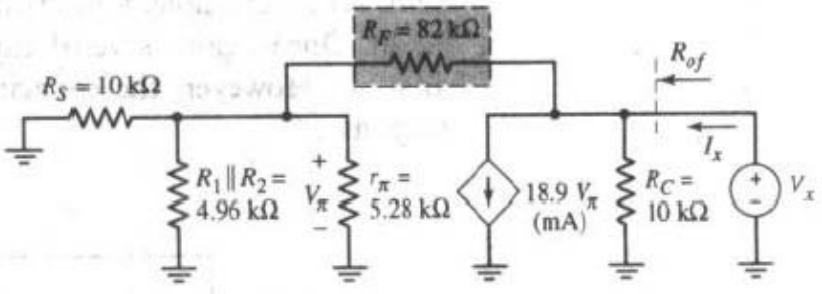
Combining these two equations, eliminating V_o, and noting that $V_\pi = V_x$, we find that

$$R_{if} = \frac{V_x}{I_x} = 0.443\,\text{k}\Omega$$

The small-signal equivalent circuit for calculating the output resistance R_{of} is shown in Figure 12.39(b). If we define

$$R_{eq} = r_\pi \| R_1 \| R_2 \| R_S$$


$R_F = 82\ \text{k}\Omega$
R_{if}
I_x
V_i
V_π
$r_\pi = 5.28\ \text{k}\Omega$
$18.9 V_\pi$ (mA)
R_C
V_o


$R_F = 82\ \text{k}\Omega$
R_{of}
$R_S = 10\ \text{k}\Omega$
$R_1 \| R_2 = 4.96\ \text{k}\Omega$
V_π
$r_\pi = 5.28\ \text{k}\Omega$
$18.9 V_\pi$ (mA)
$R_C = 10\ \text{k}\Omega$
I_x
V_x

then a KCL equation at node V_x yields

$$I_x = \frac{V_x}{R_C} + g_m V_\pi + \frac{V_x}{R_F + R_{eq}}$$

From a voltage divider equation, we find that

$$V_\pi = \left(\frac{R_{eq}}{R_{eq} + R_F}\right) V_x$$

Combining these two equations, we find the output resistance to be

$$R_{of} = \frac{V_x}{I_x} = 1.75\,\text{k}\Omega$$

Comment: The input resistance with no feedback would be $r_\pi = 5.28\,\text{k}\Omega$. The shunt input feedback connection has lowered the input resistance to $R_{if} = 0.443\,\text{k}\Omega$. Similarly, the output resistance with no feedback would be $R_C = 10\,\text{k}\Omega$. The shunt output feedback connection has lowered the output resistance to $R_{of} = 1.75\,\text{k}\Omega$. The decrease in both the input and output resistances agrees with the ideal feedback theory.

The magnitude of the transfer function, input resistance, and output resistance of the discrete transistor feedback circuit all tend to approach the ideal values if additional transistor stages are included to increase the basic amplifier gain. As an example, a multistage shunt–shunt connection is shown in Figure 12.40. Once again, several capacitors are included, which simplifies the dc analysis. However, the capacitors may adversely affect the circuit frequency response.

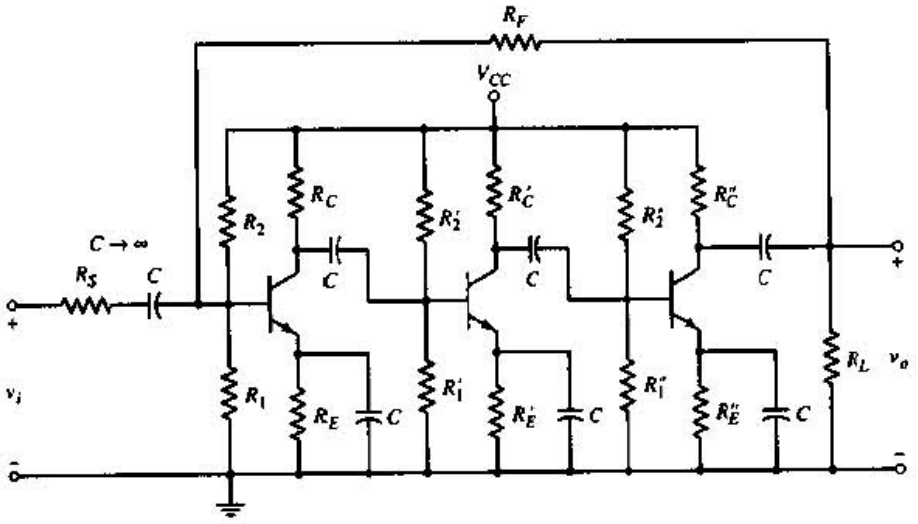


Figure 12.40 Example of multistage shunt–shunt feedback circuit

Since negative feedback is desired, there must be an odd number of negative gain stages. As the number of stages increases, the open-loop gain increases, and the circuit characteristics approach those of the ideal shunt–shunt configuration. The analysis of this circuit is left as a computer simulation problem at the end of the chapter.

Design Example 12.15 **Objective:** Design an amplifier that converts a photodiode current to an output voltage.

Assume the photodiode signal is variable from 0 to 1 mA, the source resistance is $R_S = 100\,\Omega$, and the amplifier is to drive a nominal load of $R_L = 1\,\text{k}\Omega$. The required output voltage is $V_o = \pm 5 \times 10^3 I_i$ (the phase of the output is not important), which means that the amplifier transresistance is to be $A_{zf} = 5 \times 10^3\,\Omega$. An op-amp with the characteristics described in Example 12.8 is available.

Solution: Design Approach: To minimize loading effects on the amplifier input, a small input resistance is required; to minimize loading effects on the amplifier output, a small output resistance is also required. For these reasons, a shunt–shunt feedback, or transresistance, amplifier should be used.

The closed-loop gain is

$$A_{zf} = 5 \times 10^3 \cong 1/\beta_g$$

therefore, the conductance feedback transfer function is

$$\beta_g = 2 \times 10^{-4}\,\text{S}$$

The dependent open-loop voltage source of the op-amp, as shown in Figure 12.17, can be transformed to an equivalent dependent open-loop transresistance source for the transresistance amplifier, as shown in Figure 12.14. We find that

$$A_z = A_v R_i$$

Using the parameters specified for the op-amp, we find

$$A_z = (10^4)(10^4) = 10^8\,\Omega$$

The loop gain for the shunt–shunt configuration is

$$A_z\beta_g = (10^8)(2 \times 10^{-4}) = 2 \times 10^4$$

Referring to Table 12.1, we expect the input resistance to be

$$R_{if} = 10/2 \times 10^4 = 5 \times 10^{-4}\,\text{k}\Omega \rightarrow 0.5\,\Omega$$

and the output resistance to be

$$R_{of} = 100/2 \times 10^4 = 5 \times 10^{-3}\,\Omega$$

These input and output resistances should minimize any loading effects at the amplifier input and output.

For our design we may use the amplifier configuration in Figure 12.41. In the ideal case, we have,

$$\frac{V_o}{I_i} = -R_F = \frac{1}{\beta_g}$$

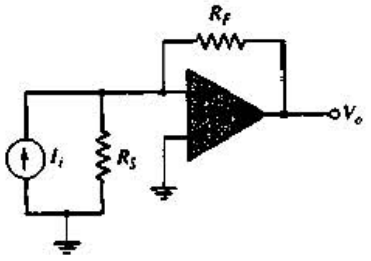


Figure 12.41 Transresistance amplifier for Example 12.15

or

$$R_F = \frac{1}{2 \times 10^{-4}} \rightarrow 5\,\text{k}\Omega$$

Comment: The design produces a transresistance amplifier that is extremely close to the ideal.

Test Your Understanding

12.22 Consider the circuit in Figure 12.42, with transistor parameters $V_{TN} = 1.5\,\text{V}$, $K_n = 1\,\text{mA/V}^2$, and $\lambda = 0$. (a) Determine the closed-loop small-signal voltage gain $A_{vf} = V_o/V_i$. (b) If the transistor conduction parameter K_n increases to $1.5\,\text{mA/V}^2$, determine the new value of voltage gain. By what percentage does the voltage gain change? (Ans. (a) $A_{vf} = -1.48$ (b) $A_{vf} = -1.62$, 9.46% change)

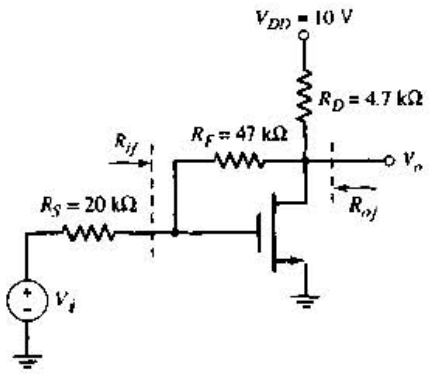


Figure 12.42 Figure for Exercises 12.22 and 12.23

12.23 Consider the feedback circuit in Figure 12.42, with transistor parameters $V_{TN} = 1.5\,\text{V}$, $K_n = 1\,\text{mA/V}^2$, and $\lambda = 0$. (a) Determine the input and output resistances R_{if} and R_{of}. (b) Repeat part (a) if the transistor conduction parameter increases to $K_n = 1.5\,\text{mA/V}^2$. (Ans. (a) $R_{if} = 7.0\,\text{k}\Omega$, $R_{of} = 1.58\,\text{k}\Omega$ (b) $R_{if} = 5.56\,\text{k}\Omega$, $R_{of} = 1.32\,\text{k}\Omega$)

***D12.24** Design a feedback transresistance amplifier to provide a gain of $-10\,\text{k}\Omega$. The nominal current signal source resistance is $50\,\Omega$, and the nominal load is $500\,\Omega$. An op-amp with parameters $R_i = 5\,\text{k}\Omega$, $R_o = 50\,\Omega$, and a low-frequency open-loop gain of $A_v = 5 \times 10^3$ is available. Correlate the design with a computer simulation analysis to determine the gain, input resistance, and output resistance.

12.8 LOOP GAIN

In previous sections, the loop gain T was easily determined for circuits involving ideal op-amps. For discrete transistor circuits, however, the loop gain usually cannot be obtained directly from the closed-loop transfer function. As we will see later in this chapter, loop gain is an important parameter in the stability of a feedback circuit; we will describe a number of techniques for determining the loop gain.

12.8.1 Basic Approach

The general feedback network was shown in Figure 12.1 and is repeated in Figure 12.43(a). To find the loop gain, set the source S_i equal to zero, and break the feedback loop at some point. Figure 12.43(b) shows a feedback network in which the loop is broken at the amplifier input and a test signal S_t is applied at this point. The amplifier output signal is $S_o = AS_t$, and the feedback signal is

$$S_{fb} = \beta S_o = A\beta S_t$$

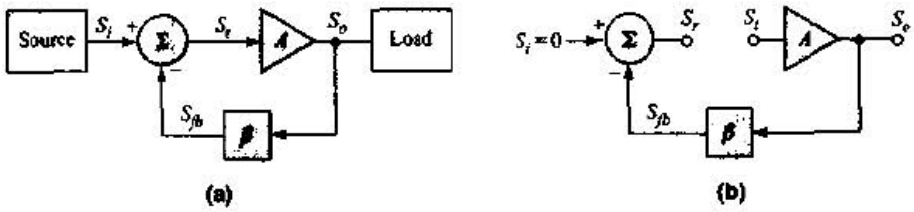


Figure 12.43 (a) Ideal configuration of a feedback amplifier; (b) basic feedback network with loop broken at amplifier input

The return signal S_r, which was previously the error signal, is now $-S_{fb}$ (the minus sign indicates negative feedback). Therefore,

$$\frac{S_r}{S_t} = -A\beta \tag{12.94}$$

The ratio of the return signal S_r to the test signal S_t is the negative of the loop gain factor.

As the feedback loop is broken, the conditions that existed prior to the loop being broken must remain unchanged. These conditions include: maintaining the same transistor biasing and maintaining the same impedance at the return point. An equivalent impedance must therefore be inserted at the point where the loop is broken. This is shown in Figure 12.44. Figure 12.44(a) shows the amplifier input impedance R_{in} prior to the loop being broken. Figure 12.44(b) shows the configuration after the loop is broken. A test voltage V_t is applied, and a load impedance R_{in} is inserted at the output of the broken

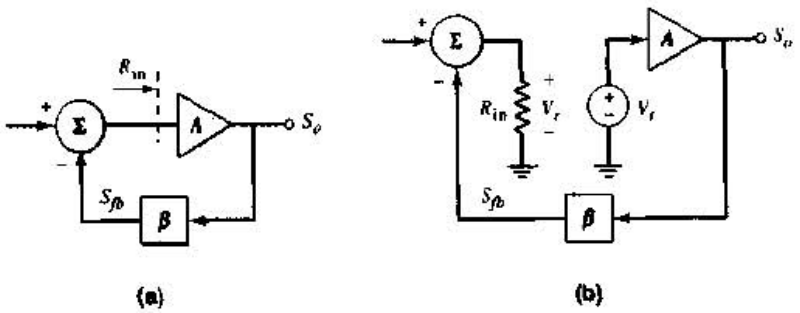


Figure 12.44 (a) Basic feedback network, showing amplifier input resistance and (b) feedback network after the loop is broken, showing test voltage and load resistance.

loop. The return voltage is then measured at this output terminal. The loop gain is found to be

$$T = A\beta = -\frac{V_r}{V_t} \tag{12.95}$$

Also, a test current I_t may be applied and a return current signal I_r measured, to find the loop gain as

$$T = -\frac{I_r}{I_t} \tag{12.96}$$

As an example, consider the circuit shown in Figure 12.45(a). The circuit is similar to the one considered in Examples 12.13 and 12.14. The feedback loop is broken at the input to the transistor, at the point marked X. The small-signal equivalent circuit is shown in Figure 12.45(b). A test voltage is applied to the base of the transistor and the equivalent load resistance r_π is connected at the return point. The input signal current is set equal to zero.

Since $V_\pi = V_t$, if we define $R_{eq} = R_S \| R_1 \| R_2 \| r_\pi$, then the output voltage can be written

$$V_o = -g_m V_t [R_C \| (R_F + R_{eq})] \tag{12.97}$$

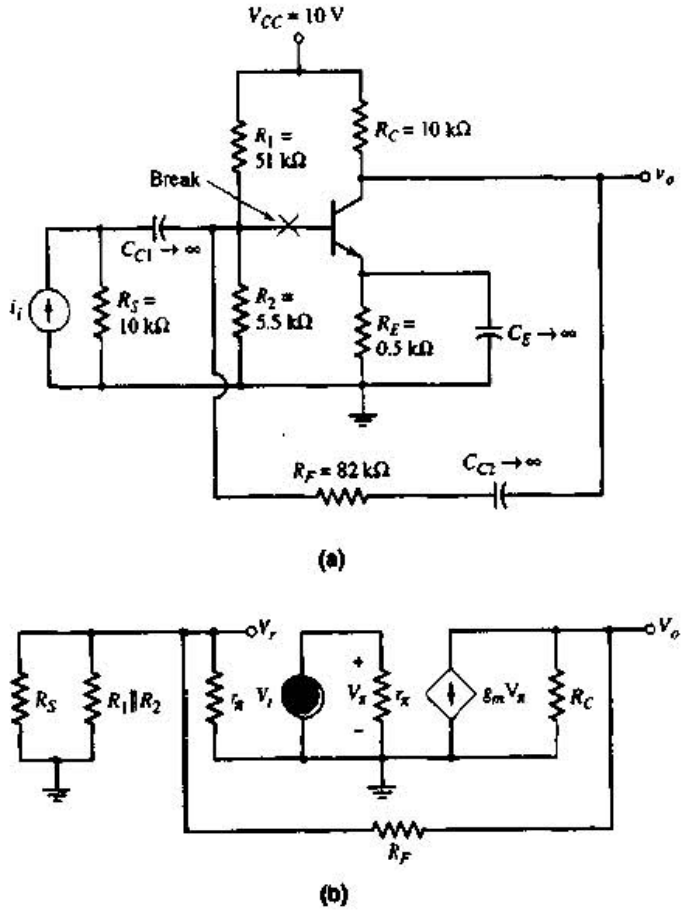


Figure 12.45 (a) Feedback circuit prior to breaking the loop and (b) small-signal equivalent circuit after breaking the loop

From a voltage divider, the return voltage V_r expression is

$$V_r = \left(\frac{R_{eq}}{R_F + R_{eq}}\right)V_o \tag{12.98}$$

Substituting Equation (12.97) into Equation (12.98) yields the loop gain

$$T = -\frac{V_r}{V_i} = +g_m\left(\frac{R_{eq}}{R_F + R_{eq}}\right)[R_C \| (R_F + R_{eq})] \tag{12.99(a)}$$

which can be written as

$$T = (g_m R_c)\left(\frac{R_{eq}}{R_C + R_F + R_{eq}}\right) \tag{12.99(b)}$$

Example 12.16 **Objective:** Determine the loop gain for a feedback circuit.

Consider the circuit shown in Figure 12.45(a), with transistor parameters: $h_{FE} = 100$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, and $V_A = \infty$. From Example 12.13, the quiescent collector current is $I_{CQ} = 0.492\,\text{mA}$, and the resulting small-signal parameters are $r_\pi = 5.28\,\text{k}\Omega$ and $g_m = 18.9\,\text{mA/V}$.

Solution: The equivalent resistance is

$$R_{eq} = R_S \| R_1 \| R_2 \| r_\pi = (10) \| (51) \| (5.5) \| (5.28) = 2.04\,\text{k}\Omega$$

From Equation (12.99(b)), the loop gain is

$$T = (g_m R_C)\left(\frac{R_{eq}}{R_C + R_F + R_{eq}}\right)$$

$$= [(18.9)(10)]\left(\frac{2.04}{10 + 82 + 2.04}\right) = 4.10$$

If the transistor current gain h_{FE} increases to 1000, then $I_{CQ} = 0.547\,\text{mA}$, $r_\pi = 47.5\,\text{k}\Omega$, and $g_m = 21.0\,\text{mA/V}$. The new value of R_{eq} becomes $3.10\,\text{k}\Omega$ and the loop gain is $T = 6.85$.

Comment: Since the loop gain is a function of the basic amplifier gain, we expect this parameter to change as the transistor current gain changes. Also, since no capacitance effects were considered, the loop gain is a positive, real number that corresponds to negative feedback.

12.8.2 Computer Analysis

The loop gain can also be determined from a computer analysis of the feedback circuit. In Example 12.17, we demonstrate a direct approach to determining the loop gain. First, we consider the circuit analyzed in the last example, to correlate the results of a computer analysis to those of a hand analysis. Then, we determine the loop gain of a feedback circuit when taking capacitance effects into account.

Example 12.17 **Objective:** Determine the loop gain factor for a feedback circuit, using a computer simulation analysis.

Consider the circuit in Figure 12.45(a).

Solution: We determine the loop gain factor by using the circuit in Figure 12.46, in which the loop is effectively broken at the base of the transistor. The circuit conditions, however, must remain unchanged from those prior to breaking the loop. This includes maintaining the same bias currents in the transistor and terminating the broken loop with the proper impedance.

A large inductance is inserted in the transistor base connection, to act as a short circuit for dc signals, so that the proper dc bias can be maintained on the transistor, and to act as an open circuit for ac signals, so that the loop appears to be broken for the ac signal. A test voltage V_t is applied to the base of the transistor through a coupling capacitor, and a load resistance R_p is connected through a coupling capacitor at the return point. These coupling capacitors act as short circuits to the ac signals, but as open circuits to dc signals, so that the dc bias is not disturbed by these elements.

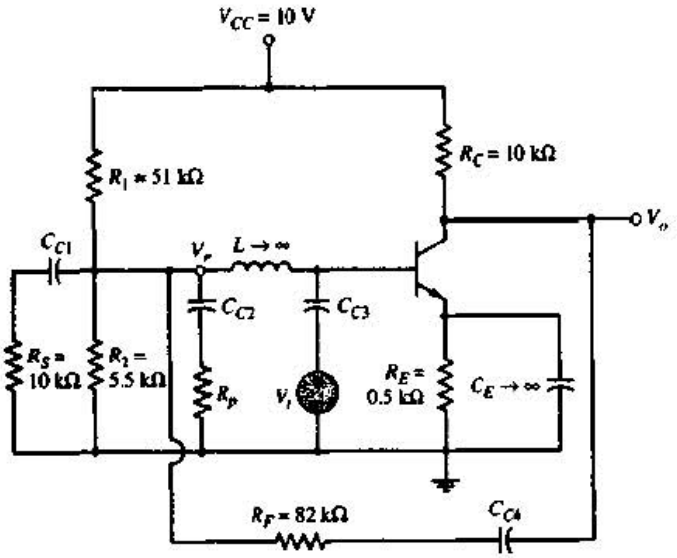


Figure 12.46 Feedback circuit with the loop effectively broken, for determining the loop gain from a computer analysis

From the computer simulation, the loop gain for a transistor current gain of $h_{FE} = 100$ is

$$T = -V_t/V_i = 5.04$$

For a current gain of 1000, the loop gain is $T = 9.37$. These values differ slightly from the hand analysis results in Example 12.16. The slight difference arises because the quiescent collector currents determined in the hand analysis and the computer analysis are not quite the same, leading to different values of g_m and r_π.

Comment: The analysis of this circuit is straightforward. In the next example, we demonstrate another advantage of a computer analysis.

When capacitances are part of the feedback circuit, the phase of the loop gain becomes a factor in determining whether the feedback is negative or positive. Figure 12.47 shows a three-stage amplifier with feedback. Each stage is the same as the circuit given in Figure 12.45(a). For an odd number of stages at low frequency, the loop gain is a positive, real quantity, and negative feedback is applied. The coupling and emitter bypass capacitors are assumed to be very large, and capacitors C_1, C_2, and C_3 between the stages can represent either load capacitances or transistor input capacitances. As the frequency increases, the magnitude of the loop gain decreases, because of decreasing capacitor impedances, and the phase of the loop gain also changes.

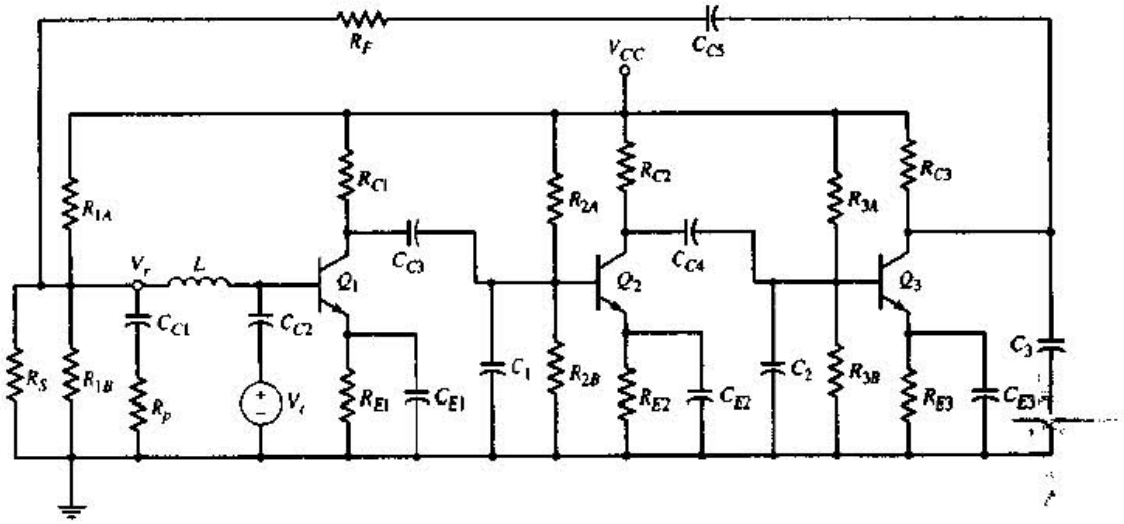


Figure 12.47 The ac equivalent circuit of three-stage feedback amplifier, including load capacitors

Example 12.18 **Objective:** Determine the magnitude and phase of the loop gain of a multistage feedback circuit.

Consider the circuit in Figure 12.47, with parameters: $R_S = 10\,\text{M}\Omega$, $R_A = 51\,\text{k}\Omega$, $R_B = 5.5\,\text{k}\Omega$, $R_F = 82\,\text{k}\Omega$, $R_C = 10\,\text{k}\Omega$, and $C = 100\,\text{pF}$. The transistor current gains are assumed to be $h_{FE} = 15$, which keeps the overall gain fairly small.

Solution: The loop is broken at the base of Q_1, and the ratio of the return signal to the test signal is measured by the same technique shown in Figure 12.46.

The magnitude of V_r/V_t versus frequency is shown in Figure 12.48(a). The magnitude of loop gain drops off with frequency, as expected, and is equal to unity at approximately 5.5 MHz.

The phase of the return signal is shown in Figure 12.48(b). Since the loop gain is given by $T = -V_r/V_t$, then the phase of the loop gain is $\angle T = -180° + \angle V_r - \angle V_t$ where the $-180°$ corresponds to the minus sign. Since the phase of the input signal was set to zero, then the phase of the loop gain is $\angle T = -180° + \angle V_r$. At low frequencies, where the phase of the return signal is approximately $+180°$, the phase of the loop gain is essentially zero, corresponding to negative feedback. At approximately $f = 2.5\,\text{MHz}$, the phase of the return signal is zero so that the phase of the loop gain is $-180°$, which corresponds to positive feedback.

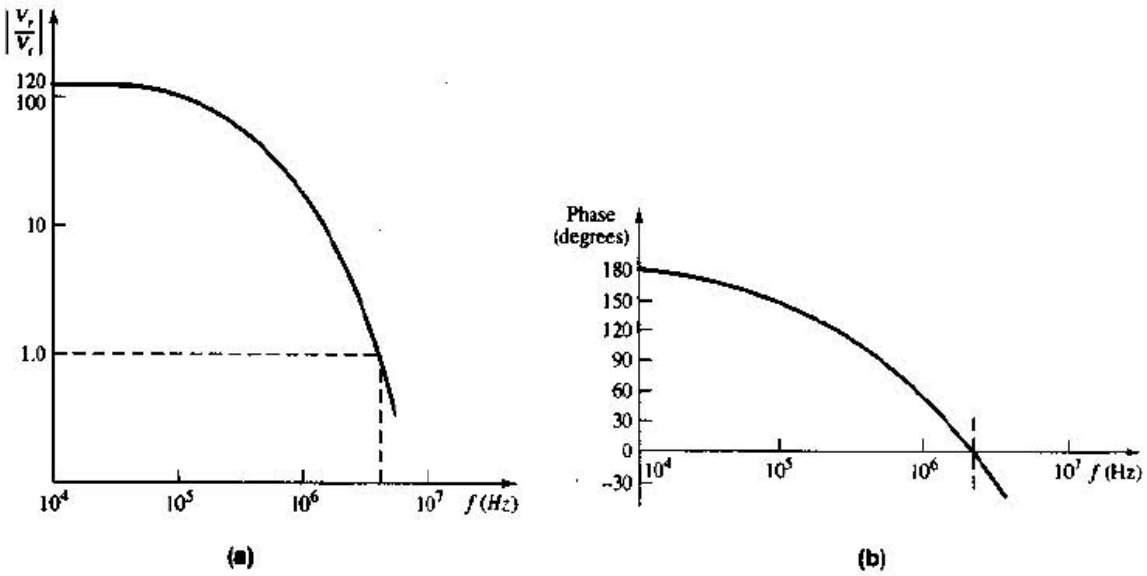


Figure 12.48 (a) Bode plot of loop gain magnitude for three-stage feedback amplifier, from Example 12.17; (b) phase of the return signal for the three-stage amplifier

Comment: For this circuit, the loop gain magnitude is greater than unity at the frequency at which the phase of T is $-180°$. As discussed in the next section, this condition means that the circuit is unstable and will oscillate.

A hand analysis of the three-stage amplifier just considered would be tedious, especially taking the frequency response into account. In this case, a computer analysis is more suitable.

Test Your Understanding

12.25 Consider the circuit in Figure 12.45(a) with a new value of $R_E = 1\,\text{k}\Omega$. The transistor parameters are: $h_{FE} = 120$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, and $V_A = \infty$. Determine the loop gain T. (Ans. $T = 3.68$)

12.26 Consider the feedback circuit in Figure 12.16, with the equivalent circuit given in Figure 12.17. Break the feedback loop at an appropriate point, and derive the expression for the loop gain. (Ans. $T = A_v/[1 + R_2/(R_1 \| R_i)]$)

12.9 STABILITY OF THE FEEDBACK CIRCUIT

In negative feedback, a portion of the output signal is subtracted from the input signal to produce the error signal. However, as we found in the last section, this subtraction property, or the loop gain, may change as a function of frequency. At some frequencies, the subtraction may actually be addition; that is, the negative feedback may become positive, producing an unstable system. In this section, we will examine the stability of feedback circuits.

12.9.1 The Stability Problem

The basic feedback configuration is shown in Figure 12.1, and the ideal closed-loop transfer function is given by Equation (12.5), which is repeated here:

$$A_f = \frac{S_o}{S_i} = \frac{A}{(1 + \beta A)} \tag{12.5}$$

The open-loop gain is a function of the individual transistor parameters and capacitances, and is therefore a function of frequency. The closed-loop gain can then be written as

$$A_f(s) = \frac{A(s)}{(1 + \beta A(s))} = \frac{A(s)}{1 + T(s)} \tag{12.100}$$

where $T(s)$ is the loop gain. For physical frequencies, $s = j\omega$, and the loop gain is $T(j\omega)$, which is a complex function. The loop gain can be represented by its magnitude and phase, as follows:

$$T(j\omega) = |T(j\omega)| \angle \phi \tag{12.101}$$

The closed-loop gain can be written

$$A_f(j\omega) = \frac{A(j\omega)}{1 + T(j\omega)} \tag{12.102}$$

The stability of the feedback circuit is a function of the loop gain $T(j\omega)$. If the loop gain magnitude is unity when the phase is 180 degrees, then $T(j\omega) = -1$ and the closed-loop gain goes to infinity. This implies that an output will exist for a zero input, which means that the circuit will oscillate. If we are trying to build a linear amplifier, an oscillator is considered an unstable circuit. We will show that if $|T(j\omega)| < 1$ when the phase is 180 degrees, the system is stable, whereas if $|T(j\omega)| \geq 1$ when the phase is 180 degrees, the system is unstable. To study the stability of feedback circuits, we must therefore analyze the frequency response of the loop gain factor.

12.9.2 Bode Plots: One-, Two-, and Three-Pole Amplifiers

Figure 12.49(a) shows a simple single-stage common-emitter current amplifier. The high-frequency small-signal equivalent circuit is shown in Figure 12.49(b). The capacitance C_1 includes the forward-biased base-emitter junction capacitance as well as the effective Miller capacitance. The Miller capacitance and Miller effect were discussed in Chapter 7. The equivalent circuit shown in Figure 12.49(b) is identical to that developed in Figure 7.39. The output current in Figure 12.49(b) is given by

$$I_o = \left(\frac{R_C}{R_C + R_L}\right) g_m V_\pi \tag{12.103}$$

and the voltage V_π is

$$V_\pi = I_i \left[R_\pi \left\| \left(\frac{1}{sC_1}\right) \right. \right] \tag{12.104}$$

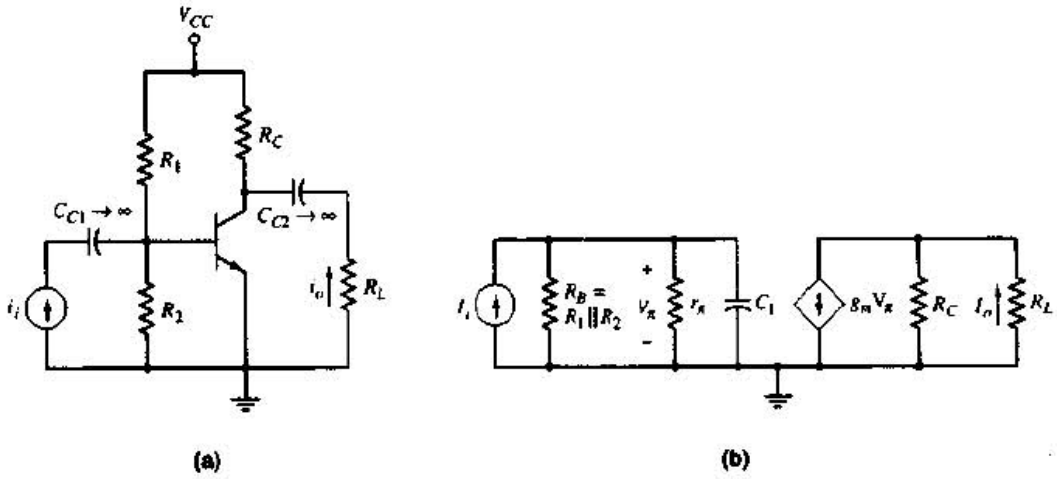


Figure 12.49 (a) Single-stage common-emitter amplifier and (b) small-signal equivalent circuit, including input capacitance

where $R_\pi = r_\pi \| R_B = r_\pi \| R_1 \| R_2$. Equation (12.104) can be expanded to

$$V_\pi = I_i \left[\frac{R_\pi}{1 + sR_\pi C_1} \right] \tag{12.105}$$

Substituting Equation (12.105) into (12.103), we get an expression for the small-signal current gain,

$$A_i = g_m R_\pi \left(\frac{R_C}{R_C + R_L} \right) \left[\frac{1}{1 + sR_\pi C_1} \right] \tag{12.106}$$

When we set $s = j\omega = j(2\pi f)$, Equation (12.106) can be written as

$$A_i = \frac{A_{io}}{1 + j\left(\dfrac{f}{f_1}\right)} \tag{12.107}$$

where A_{io} is the low-frequency or midband gain and f_1 is the upper 3dB frequency. The gain is a complex function that can be written

$$A_i = \frac{A_{io}}{\sqrt{1 + \left(\dfrac{f}{f_1}\right)^2}} \angle -\tan^{-1}\left(\frac{f}{f_1}\right) \tag{12.108}$$

Figure 12.50(a) is a Bode plot of the current gain magnitude, and Figure 12.50(b) is a Bode plot of the current gain phase. Note that, from the definition of the directions of input and output currents, the output current is in phase with the input current at low frequencies. At high frequencies, the output current becomes 90 degrees out of phase with respect to the input current. This single-stage circuit is an example of a one-pole amplifier. As we have previously shown, similar expressions can be obtained for voltage gain, the transresistance transfer function, and the transconductance transfer function.

Figure 12.51 shows the small-signal equivalent circuit of a two-stage amplifier, using the same hybrid-π configuration for the transistors. The capacitance

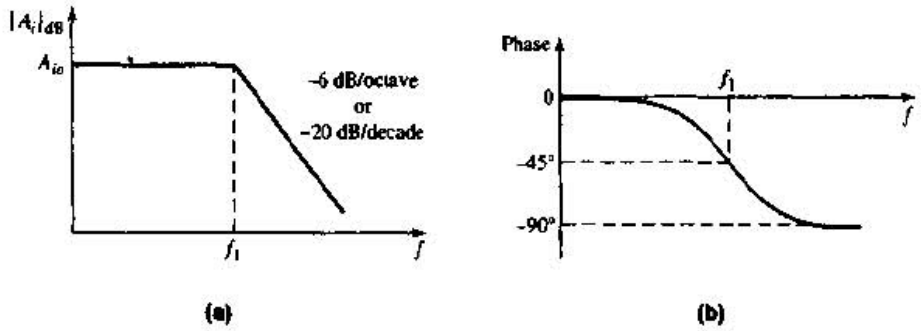


Figure 12.50 Bode plots of current gain for single-stage common-emitter amplifier: (a) magnitude and (b) phase

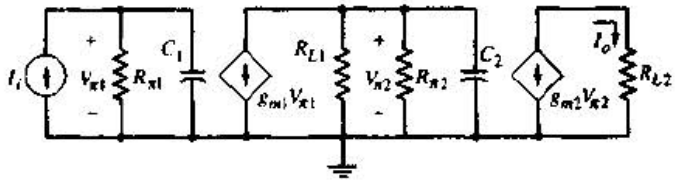


Figure 12.51 Small-signal equivalent circuit, two-stage amplifier including input capacitances

C_2 is the input capacitance of the second transistor, including the effective Miller capacitance. The output current is

$$I_o = -g_{m2}V_{\pi 2} \tag{12.109}$$

and $V_{\pi 2}$ is

$$V_{\pi 2} \approx -g_{m1}V_{\pi 1}\left[R_{L1} \| R_{\pi 2} \| \left(\frac{1}{sC_2}\right)\right] \tag{12.110}$$

The voltage $V_{\pi 1}$ is

$$V_{\pi 1} = I_i\left[R_{\pi 1} \| \left(\frac{1}{sC_1}\right)\right] \tag{12.111}$$

Combining Equations (12.109), (12.110), and (12.111) yields an expression for the small-signal current gain, as follows:

$$A_i = \frac{I_o}{I_i} = (g_{m1}g_{m2})(R_{\pi 1})(R_{L1} \| R_{\pi 2})\left[\frac{1}{1 + sR_{\pi 1}C_1}\right]\left[\frac{1}{1 + s(R_{L1} \| R_{\pi 2})C_2}\right] \tag{12.112}$$

Setting $s = j\omega = j(2\pi f)$, we can write Equation (12.112)

$$A_i = \frac{A_{io}}{\left(1 + j\dfrac{f}{f_1}\right)\left(1 + j\dfrac{f}{f_2}\right)} \tag{12.113}$$

where $f_1 = 1/2\pi R_{\pi 1} C_1$ and $f_2 = 1/2\pi(R_{L1} \| R_{\pi 2})C_2$. Frequency f_1 is the upper 3 dB frequency of the first stage, and f_2 is the upper 3 dB frequency of the second stage. This two-stage circuit is an example of a two-pole amplifier.

Equation (12.113) can be written

$$A_i = \frac{A_{io}}{\sqrt{1 + \left(\frac{f}{f_1}\right)^2}\sqrt{1 + \left(\frac{f}{f_2}\right)^2}} \angle - \left[\tan^{-1}\left(\frac{f}{f_1}\right) + \tan^{-1}\left(\frac{f}{f_2}\right)\right] \qquad \textbf{(12.114)}$$

Figure 12.52(a) is a Bode plot of the current gain magnitude, assuming $f_1 \ll f_2$. This assumption implies that the two poles are far apart. The Bode plot of the current gain phase is shown in Figure 12.52(b). Again the phase of the output current is in phase with the input current at low frequency. This phase relation is a direct result of the way the directions of current were defined. At high frequencies, the output current becomes 180 degrees out of phase with respect to the input current.

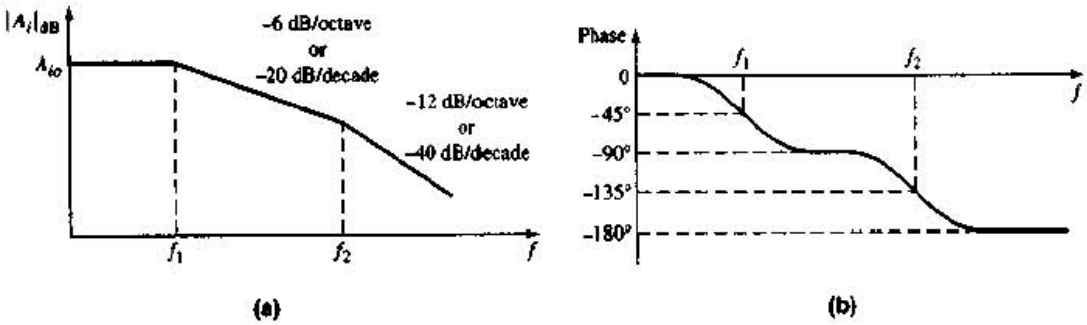


Figure 12.52 Bode plots of current gain for two-stage amplifier: (a) magnitude and (b) phase

An op-amp is a three-stage amplifier, as shown in Figure 12.53. Since each stage has an equivalent input resistance and capacitance, this circuit is an example of a three-pole amplifier. The overall gain can be expressed as

$$A = \frac{A_o}{\left(1 + j\frac{f}{f_1}\right)\left(1 + j\frac{f}{f_2}\right)\left(1 + j\frac{f}{f_3}\right)} \qquad \textbf{(12.115)}$$

where A_o is the low-frequency gain factor. Assuming the poles are far apart (let $f_1 \ll f_2 \ll f_3$), the Bode plots of the gain magnitude and phase are shown in Figure 12.54. At very high frequencies, the phase difference between the output and input signals is -270 degrees.

If we assume an ideal feedback amplifier, the loop gain is

$$T(j\omega) = \beta A(j\omega) \qquad \textbf{(12.116)}$$

Figure 12.53 Three-stage amplifier

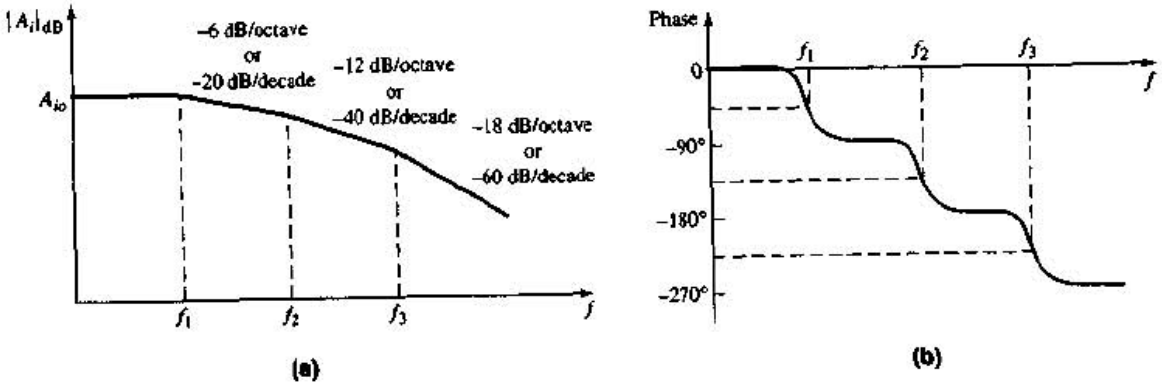


Figure 12.54 Bode plots of three-stage amplifier gain: (a) magnitude and (b) phase

where the feedback transfer function β is assumed to be independent of frequency. For op-amp feedback circuits, we can determine the feedback transfer function β, as previously shown, and the basic amplifier characteristics are assumed to be known. For a three-stage amplifier, the loop gain is therefore

$$T(f) = \frac{\beta A_o}{\left(1 + j\frac{f}{f_1}\right)\left(1 + j\frac{f}{f_2}\right)\left(1 + j\frac{f}{f_3}\right)} \tag{12.117}$$

Both the magnitude and phase of the loop gain are functions of frequency. For the three-stage amplifier, the phase will be −180 degrees at some particular frequency, which means that the amplifier may become unstable.

12.9.3 Nyquist Stability Criterion

In the last section, we saw that a feedback system can become unstable. Several methods can be used to determine whether a system is stable or unstable. The method we will consider is called the **Nyquist stability criterion**. This method not only determines if a system is stable, it also indicates the degree of system stability.

To apply this method, we must plot a **Nyquist diagram**, which is a polar plot of the loop gain factor $T(j\omega)$. The loop gain, which is a complex function, can be written in terms of its magnitude and phase, $T(j\omega) = |T(j\omega)|\angle\phi$, as shown in Equation (12.101). The Nyquist diagram is a plot of the real and imaginary components of $T(j\omega)$ as the frequency ω varies from minus infinity to plus infinity. Although negative frequencies have no physical meaning, they are not mathematically excluded in the loop gain function. The polar plot for negative frequencies, as we will see, is the complex conjugate of the polar plot for positive frequencies.

The loop gain for a two-pole amplifier is, from Equation (12.113),

$$T(j\omega) = \frac{\beta A_{io}}{\left(1 + j\frac{\omega}{\omega_1}\right)\left(1 + j\frac{\omega}{\omega_2}\right)} \tag{12.118}$$

where ω_1 and ω_2 are the upper 3 dB radian frequencies of the first and second stages, respectively. We can also write Equation (12.118) in the form

$$T(j\omega) = \frac{\beta A_{io}}{\sqrt{1+\left(\frac{\omega}{\omega_1}\right)^2}\sqrt{1+\left(\frac{\omega}{\omega_2}\right)^2}} \angle -\left[\tan^{-1}\left(\frac{\omega}{\omega_1}\right)+\tan^{-1}\left(\frac{\omega}{\omega_2}\right)\right] \tag{12.119}$$

The Nyquist plot of Equation (12.119) is shown in Figure 12.55. At $\omega = 0$, the magnitude of $T(j\omega)$ is βA_{io} and the phase is zero. As ω increases, the magnitude decreases and the phase is negative. From Equation (12.119), we see that for negative values of ω, the magnitude also decreases, but the phase becomes positive. This means that the loop gain function for negative frequencies is the complex conjugate of the loop gain function for positive frequencies, and the real axis is the axis of symmetry. As ω approaches $+\infty$, the magnitude approaches zero and the phase approaches -180 degrees.

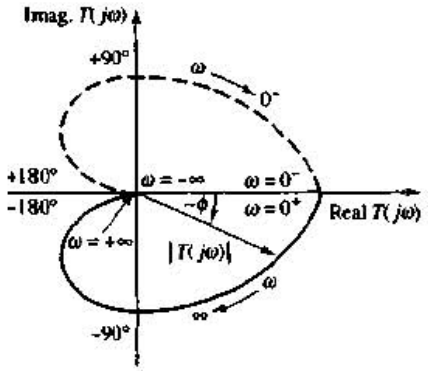


Figure 12.55 Nyquist plot, loop gain for two-stage amplifier

The loop gain for a three-pole amplifier is, from Equation (12.117),

$$T(j\omega) = \frac{\beta A_o}{\left(1+j\frac{\omega}{\omega_1}\right)\left(1+j\frac{\omega}{\omega_2}\right)\left(1+j\frac{\omega}{\omega_3}\right)} \tag{12.120}$$

This loop gain function can also be written in the form

$$T(j\omega) = \frac{\beta A_o}{\sqrt{1+\left(\frac{\omega}{\omega_1}\right)^2}\sqrt{1+\left(\frac{\omega}{\omega_2}\right)^2}\sqrt{1+\left(\frac{\omega}{\omega_3}\right)^2}} \angle \phi \tag{12.121(a)}$$

where ϕ is the phase, given by

$$\phi = -\left[\tan^{-1}\left(\frac{\omega}{\omega_1}\right)+\tan^{-1}\left(\frac{\omega}{\omega_2}\right)+\tan^{-1}\left(\frac{\omega}{\omega_3}\right)\right] \tag{12.121(b)}$$

Figure 12.56(a) shows one possible Nyquist plot. For $\omega = 0$, the magnitude is βA_o and the phase is zero. As ω increases in the positive direction, the magnitude decreases and the phase becomes negative. As the Bode plot in Figure 12.54 shows, the phase goes through -90 degrees, then through -180 degrees, and finally approaches -270 degrees as the magnitude approaches zero. This same effect is shown in the Nyquist diagram. The plot approaches

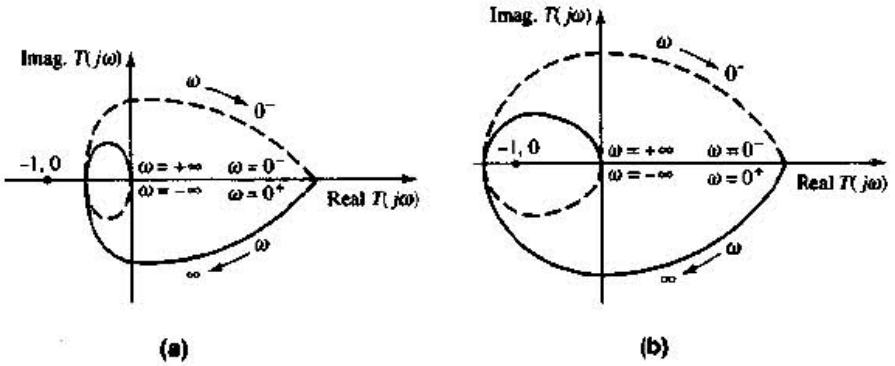


Figure 12.56 Nyquist plot, loop gain for three-stage amplifier, for: (a) stable system and (b) unstable system

the origin and is tangent to the imaginary axis as $\omega \to \infty$. Again, the plot for negative frequencies is the mirror image of the positive frequency plot about the real axis.

Another possible Nyquist plot for the three-pole loop gain function is shown in Figure 12.56(b). The basic plot is the same as that in Figure 12.56(a), except that the position of the point $(-1, 0)$ is different. At the frequency at which the phase is -180 degrees, the curve crosses the negative real axis. In Figure 12.56(a), $|T(j\omega)| < 1$ when the phase is -180 degrees, whereas in Figure 12.56(b), $|T(j\omega)| > 1$ when the phase is -180 degrees. The Nyquist diagram encircles the point $(-1, 0)$ in Figure 12.56(b), and this has particular significance for stability. For this treatment of a three-pole amplifier, the Nyquist criterion for stability of the amplifier can be stated as follows: "If the Nyquist plot encircles or goes through the point $(-1, 0)$, the amplifier is unstable."

Using the criterion, a simpler test for stability can be used in most cases. If $|T(j\omega)| \geq 1$ at the frequency at which the phase is -180 degrees, then the amplifier is unstable. This simpler test allows us to use the Bode plots considered previously, instead of explicitly constructing the Nyquist diagram.

Example 12.19 **Objective:** Determine the stability of an amplifier, given the loop gain function.

Consider a three-pole feedback amplifier with a loop gain given by

$$T(f) = \frac{\beta(100)}{\left(1 + j\dfrac{f}{10^5}\right)^3}$$

In this case, the three poles all occur at the same frequency. Determine the stability of the amplifier for $\beta = 0.20$ and $\beta = 0.02$.

Solution: The loop gain can be written in terms of its magnitude and phase.

$$T(f) = \frac{\beta(100)}{\left[\sqrt{1 + \left(\dfrac{f}{10^5}\right)^2}\right]^3} \angle -3\tan^{-1}\left(\frac{f}{10^5}\right)$$

The frequency f_{180} at which the phase becomes -180 degrees is

$$-3\tan^{-1}\left(\frac{f_{180}}{10^5}\right) = -180^\circ$$

which yields

$$f_{180} = 1.73 \times 10^5 \text{ Hz}$$

The magnitude of the loop gain at this frequency for, $\beta = 0.20$, is then

$$|T(f_{180})| = \frac{(0.20)(100)}{8} = 2.5$$

For $\beta = 0.02$, the magnitude is

$$|T(f_{180})| = \frac{(0.020)(100)}{8} = 0.25$$

Comment: The loop gain magnitude at the frequency at which the phase is -180 degrees is 2.5 when $\beta = 0.20$ and 0.25 when $\beta = 0.02$. The system is therefore unstable for $\beta = 0.20$ and stable for $\beta = 0.02$.

We can also consider the stability of the feedback system in terms of Bode plots. The Bode plot of the loop gain magnitude from the previous example is shown in Figure 12.57(a), for $\beta = 0.20$ and $\beta = 0.02$. The low-frequency loop gain magnitude is dependent on β, but the 3 dB frequency is the same in both cases. Since the three poles all occur at the same frequency, the magnitude of $T(f)$ decreases at the rate of -18 dB/octave at the higher frequencies. The frequencies at which $|T(f)| = 1$ are indicated on the figure.

The phase of the loop gain function is shown in Figure 12.57(b). The two frequencies at which $|T(f)| = 1$, for the two values of β, are also indicated. We see that $|\phi| > 180^\circ$ at $|T(f)| = 1$, when $\beta = 0.20$. This is equivalent to $|T(f)| > 1$ when $\phi = -180^\circ$, which makes the system unstable. However, $|\phi| < 180^\circ$ at

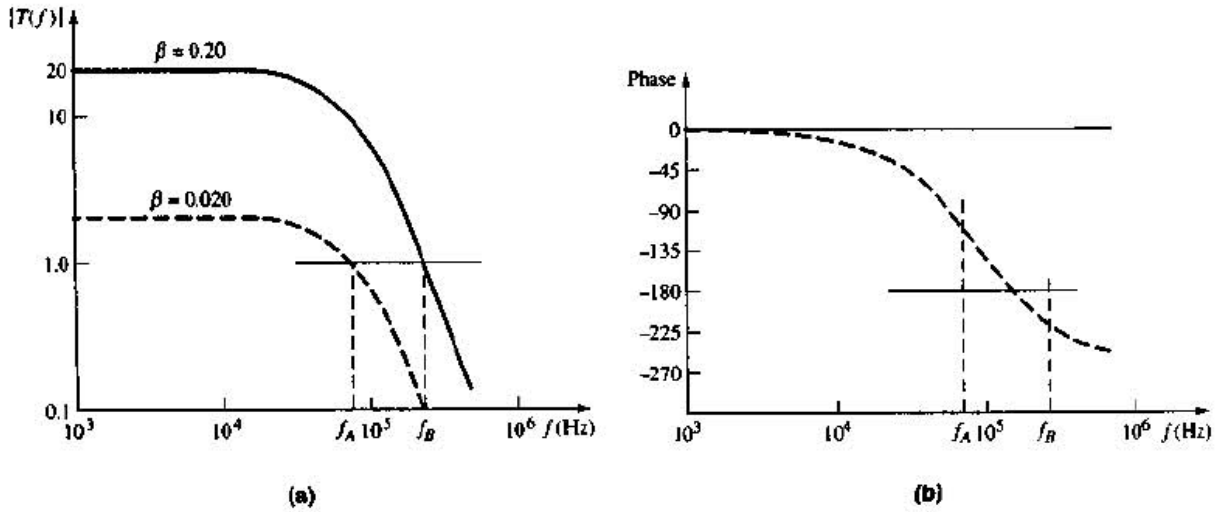


Figure 12.57 Bode plots of loop gain of function described in Example 12.19, for two values of feedback transfer function: (a) magnitude and (b) phase

$|T(f)| = 1$, when $\beta = 0.02$, so the feedback circuit is stable for this feedback transfer factor.

12.9.4 Phase and Gain Margins

From the discussion in the previous section, we can determine whether a feedback amplifier is stable or unstable by examining the loop gain as a function of frequency. This can be done from a Nyquist diagram or from the Bode plots. We can also use this technique to determine the degree of stability of a feedback amplifier.

At the frequency at which the loop gain magnitude is unity, if the magnitude of the phase is less than 180 degrees, the system is stable. This is illustrated in Figure 12.58. The difference (magnitude) between the phase angle at this frequency and 180 degrees is called the **phase margin**. The loop gain can change due, for example, to temperature variations, and the phase margin indicates how much the loop gain can increase and still maintain stability. A typical desired phase margin is in the range of 45 to 60 degrees.

A second term that describes the degree of stability is the **gain margin**, which is also illustrated in Figure 12.58. This function is defined to be $|T(j\omega)|$ in decibels at the frequency where the phase is -180 degrees. This value is usually expressed in dB and also gives an indication of how much the loop gain can increase and still maintain stability.

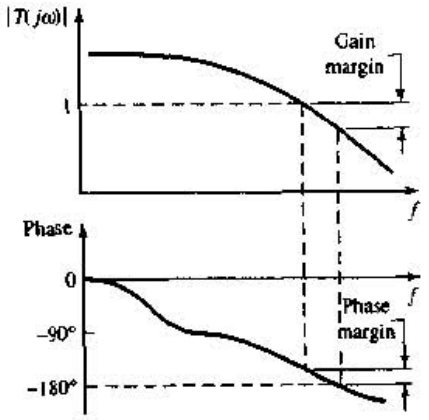


Figure 12.58 Bode plots of loop gain magnitude and phase, indicating phase margin and gain margin

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Example 12.20 **Objective:** Determine the required feedback transfer function β to yield a specific phase margin.

Consider a three-pole feedback amplifier with a loop gain function given by

$$T(f) = \frac{\beta(100)}{\left(1 + j\frac{f}{10^3}\right)\left(1 + j\frac{f}{5 \times 10^4}\right)\left(1 + j\frac{f}{10^6}\right)}$$

Determine the value of β that yields a phase margin of 45 degrees.

Solution: A phase margin of 45 degrees implies that the phase of the loop gain is −135 degrees at the frequency at which the magnitude of the loop gain is unity. The phase of the loop gain is

$$\phi = -\left[\tan^{-1}\left(\frac{f}{10^3}\right) + \tan^{-1}\left(\frac{f}{5 \times 10^4}\right) + \tan^{-1}\left(\frac{f}{10^6}\right)\right]$$

Since the three poles are far apart, the frequency at which the phase is −135 degrees is approximately equal to the frequency of the second pole, as shown in Figure 12.54. In this example, $f_{135} \cong 5 \times 10^4$ Hz, so we have that

$$\phi = -\left[\tan^{-1}\left(\frac{5 \times 10^4}{10^3}\right) + \tan^{-1}\left(\frac{5 \times 10^4}{5 \times 10^4}\right) + \tan^{-1}\left(\frac{5 \times 10^4}{10^6}\right)\right]$$

or

$$\phi = -[88.9° + 45° + 2.86°] \cong -135°$$

Since we want the loop gain magnitude to be unity at this frequency, we have

$$|T(f)| = 1 = \frac{\beta(100)}{\sqrt{1 + \left(\frac{5 \times 10^4}{10^3}\right)^2}\sqrt{1 + \left(\frac{5 \times 10^4}{5 \times 10^4}\right)^2}\sqrt{1 + \left(\frac{5 \times 10^4}{10^6}\right)^2}}$$

or

$$1 \cong \frac{\beta(100)}{(50)(1.41)(1)}$$

which yields $\beta = 0.705$.

Comment: If the frequency is greater than 5×10^4 Hz, the loop gain magnitude is less than unity, and the system remains stable.

Test Your Understanding

12.27 Consider a feedback amplifier with a single pole and an open-loop gain given by Equation (12.107). Assume the parameters are $A_{io} = 10^5$ A/A and $f_1 = 10$ Hz. The basic amplifier is connected to a feedback circuit for which the feedback transfer function is $\beta = 0.01$ A/A. Find the frequency at which $|T(f)| = 1$, and determine the phase margin. (Ans. $f = 10^4$ Hz, 90 degrees)

***12.28** A two-pole feedback amplifier has an open-loop gain given by Equation (12.113), with parameters: $A_{io} = 10^5$ A/A, $f_1 = 10^4$ Hz, and $f_2 = 10^5$ Hz. The basic amplifier is connected to a feedback circuit, for which the feedback transfer ratio is β. Determine the value of β that results in a phase margin of 60 degrees. (Ans. $\beta = 9.73 \times 10^{-5}$ A/A)

12.29 Consider the loop gain function described in Example 12.19. Determine the value of β at which the amplifier becomes unstable. (Ans. $\beta = 0.08$)

12.30 For the loop gain function given in Example 12.19, determine the value of β that produces a phase margin of 60 degrees. (Ans. $\beta = 0.0222$)

12.10 FREQUENCY COMPENSATION

In the previous section, we presented a method for determining whether a feedback system is stable or unstable. In this section, we will discuss a method for modifying the loop gain of a feedback amplifier, to make the system stable. The general technique of making a feedback system stable is called **frequency compensation**.

12.10.1 Basic Theory

One basic method of frequency compensation involves introducing a new pole in the loop gain function, at a sufficiently low frequency that $|T(f)| = 1$ occurs when $|\phi| < 180°$. As an example, consider the Bode plots of a three-pole loop gain magnitude and phase given in Figure 12.59 and shown by the solid lines. In this case, when the magnitude of the loop gain is unity, the phase is nearly -270 degrees and the system is unstable.

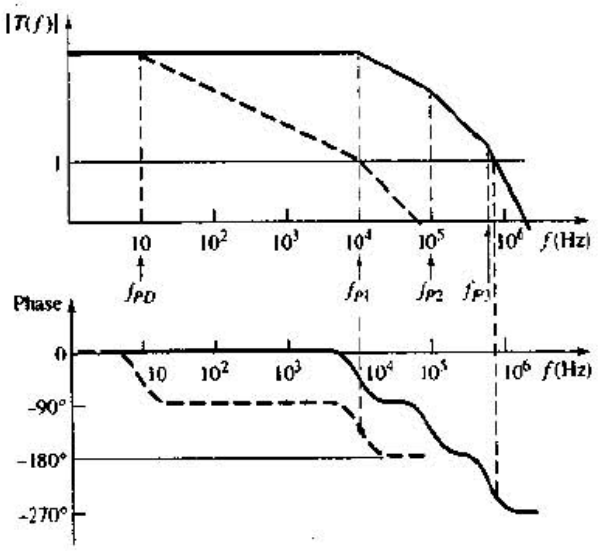

Figure 12.59 Bode plots of loop gain magnitude and phase for three-stage amplifier, before frequency compensation (solid curves), and after frequency compensation (dotted curves)

If we introduce a new pole f_{PD} at a very low frequency, and if we assume that the original three poles do not change, the new Bode plots of the magnitude and phase will be as shown by the dotted lines in Figure 12.59. In this situation, the magnitude of the loop gain becomes unity when the phase is $|\phi| < 180°$, and the system is stable. Since the pole is introduced at a low frequency and since it dominates the frequency response, it is called a **dominant pole**. This fourth pole can be introduced by adding a fourth stage with an extremely large input capacitance. Though not practical, this method demonstrates the basic idea of stabilizing a circuit.

Example 12.21 **Objective:** Determine the dominant pole required to stabilize a feedback system.

Consider a three-pole feedback amplifier with a loop gain given by

$$T(f) = \frac{5 \times 10^5}{\left(1 + j\frac{f}{10^6}\right)\left(1 + j\frac{f}{10^7}\right)\left(1 + j\frac{f}{10^8}\right)}$$

Insert a dominant pole, assuming the original poles do not change, such that the phase margin is at least 45 degrees.

Solution: By inserting a dominant pole, we change the loop gain function to

$$T_{PD}(f) = \frac{5 \times 10^5}{\left(1 + j\frac{f}{f_{PD}}\right)\left(1 + j\frac{f}{10^6}\right)\left(1 + j\frac{f}{10^7}\right)\left(1 + j\frac{f}{10^8}\right)}$$

We assume that $f_{PD} \ll 10^6$ Hz. A phase of -135 degrees, giving a phase margin of 45 degrees, occurs approximately at $f_{135} = 10^6$ Hz.

Since we want the loop gain magnitude to be unity at this frequency, we have

$$|T_{PD}(f_{135})| \simeq 1 = \frac{5 \times 10^5}{\sqrt{1 + \left(\frac{10^6}{f_{PD}}\right)^2}\sqrt{1 + \left(\frac{10^6}{10^6}\right)^2}\sqrt{1 + \left(\frac{10^6}{10^7}\right)^2}\sqrt{1 + \left(\frac{10^6}{10^8}\right)^2}}$$

or

$$1 = \frac{5 \times 10^5}{\sqrt{1 + \left(\frac{10^6}{f_{PD}}\right)^2}(1.414)(1.0)(1.0)}$$

Solving for f_{PD} yields

$$f_{PD} = 2.83 \text{ Hz}$$

Comment: With high-gain amplifiers, the dominant pole must be at a very low frequency to ensure stability of the feedback circuit.

Problem-Solving Technique: Frequency Compensation

1. To stabilize a circuit, insert a dominant pole or move an existing pole to a dominant pole position (see next section). Assume that the dominant pole frequency is small. Determine the frequency of the resulting loop gain function to achieve the required phase margin.
2. Set the magnitude of the loop gain function equal to unity at the frequency determined in step 1 to find the required dominant pole frequency.
3. To actually achieve the required dominant pole frequency in the circuit, a number of techniques are available (for example, see Miller compensation).

One disadvantage of this frequency compensation method is that the loop gain magnitude, and in turn the open-loop gain magnitude, is drastically reduced over a very wide frequency range. This affects the closed-loop response

of the feedback amplifier. However, the advantage of maintaining a stable amplifier greatly outweighs the disadvantage of a reduced gain, demonstrating another trade-off in design criteria.

12.10.2 Closed-Loop Frequency Response

Inserting a dominant pole to obtain the open-loop characteristics (dotted lines, Figure 12.59) is not as extreme or devastating to the circuit as it might first appear. Amplifiers are normally used in a closed-loop configuration, for which we briefly considered the bandwidth extension, in Section 12.2.3.

For the region in which the frequency response is characterized by the dominant pole, the open-loop amplifier gain is

$$A(f) = \frac{A_o}{1 + j\dfrac{f}{f_{PD}}} \tag{12.122}$$

where A_o is the low-frequency gain and f_{PD} is the dominant-pole frequency. The feedback amplifier closed-loop gain can be expressed as

$$A_f(f) = \frac{A(f)}{(1 + \beta A(f))} \tag{12.123}$$

where β is the feedback transfer ratio, which is assumed to be independent of frequency. Substituting Equation (12.122) into (12.123), we can write the closed-loop gain as

$$A_f(f) = \frac{A_o}{(1 + \beta A_o)} \times \frac{1}{1 + j\dfrac{f}{f_{PD}(1 + \beta A_o)}} \tag{12.124}$$

The term $A_o/(1 + \beta A_o)$ is the closed-loop low-frequency gain, and $f_{PD}(1 + \beta A_o) = f_C$ is the 3 dB frequency of the closed-loop system.

Figure 12.60 shows the Bode plot of the gain magnitude for the open-loop parameters $A_o = 10^6$ and $f_{PD} = 10$ Hz, at several feedback transfer ratios. As the closed-loop gain decreases, the bandwidth increases. As previously determined, the gain–bandwidth product is essentially a constant.

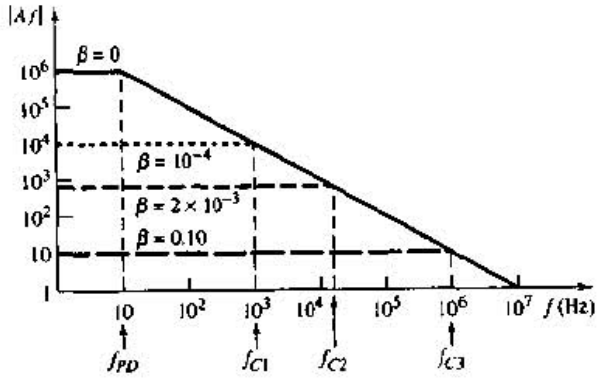

Figure 12.60 Bode plot, gain magnitude for open-loop and three closed-loop conditions

Example 12.22 **Objective:** Determine the shift in the 3 dB frequency when an amplifier is operated in a closed-loop system.

Consider an amplifier with a low-frequency open-loop gain of $A_o = 10^6$ and an open-loop 3 dB frequency of $f_{PD} = 10$ Hz. The feedback transfer ratio is $\beta = 0.01$.

Solution: The low-frequency closed-loop gain is

$$A_f(0) = \frac{A_o}{(1 + \beta A_o)} = \frac{10^6}{1 + (0.01)(10^6)} \cong 100$$

From Equation (12.124), the closed-loop 3 dB frequency is

$$f_C = f_{PD}(1 + \beta A_o) = (10)[1 + (0.01)(10^6)]$$

or

$$f_C \cong 10^5 \text{ Hz} = 100 \text{ kHz}$$

Comment: Even though the open-loop 3 dB frequency is only 10 Hz, the closed-loop bandwidth is extended to 100 kHz. This effect is due to the fact that the gain–bandwidth product is a constant.

12.10.3 Miller Compensation

As previously discussed, an op-amp consists of three stages, with each stage normally responsible for one of the loop gain poles. Assume, for purposes of discussion, that the first pole f_{P1} is created by the capacitance effects in the second gain stage. Instead of adding a fourth dominant pole to achieve a stable system, we can move pole f_{P1} to a low frequency. This can be done by increasing the effective input capacitance to the gain stage.

Previously in Chapter 7, we determined that the effective Miller input capacitance to a transistor amplifier is a feedback capacitance multiplied by the magnitude of the gain of the amplifier stage. We can use this Miller multiplication factor to stabilize a feedback system. The three-stage op-amp circuit is shown in Figure 12.61. The second stage, an inverting amplifier, has a feedback capacitor connected between the output and input. This capacitor C_f is called a **compensation capacitor**.

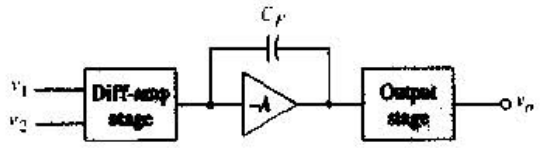

Figure 12.61 Three-stage amplifier, including Miller compensation capacitor

The effective input Miller capacitance is

$$C_M = C_f(1 + A) \tag{12.125}$$

Since the gain of the second stage is large, the equivalent Miller capacitance will normally be very large. The pole introduced by the second stage is approximately

$$f_{P1} = \frac{1}{2\pi R_2 C_M} \tag{12.126}$$

where R_2 is the effective resistance between the amplifier input node and ground. Resistance R_2, then, is the parallel combination of the input resistance to the amplifier and the output resistance of the diff-amp stage.

Example 12.23 **Objective:** Determine the pole of the gain stage that includes a feedback capacitor.

Consider a gain stage with an amplification $A = 10^3$, a feedback capacitor $C_F = 30\,\text{pF}$, and a resistance $R_2 = 5 \times 10^5\,\Omega$.

Solution: The effective input Miller capacitance is

$$C_M = C_F(1 + A) \cong (30)(1000)\,\text{pF} = 3 \times 10^{-8}\,\text{F}$$

The dominant-pole frequency is therefore

$$f_{P1} = \frac{1}{2\pi R_2 C_M} = \frac{1}{2\pi(5 \times 10^5)(3 \times 10^{-8})} = 10.6\,\text{Hz}$$

Comment: The pole of the second stage can be moved to a significantly lower frequency by using the Miller effect.

The effect of moving pole f_{P1}, using the Miller compensation technique, is shown in Figure 12.62. We assume at this point that the other two poles f_{P2} and f_{P3} are not affected. Moving the pole f_{P1} to f'_{P1} means that the frequency at which $|T(f)| = 1$ is lower, and that the phase is $|\phi| < 180°$, which means that the amplifier is stabilized.

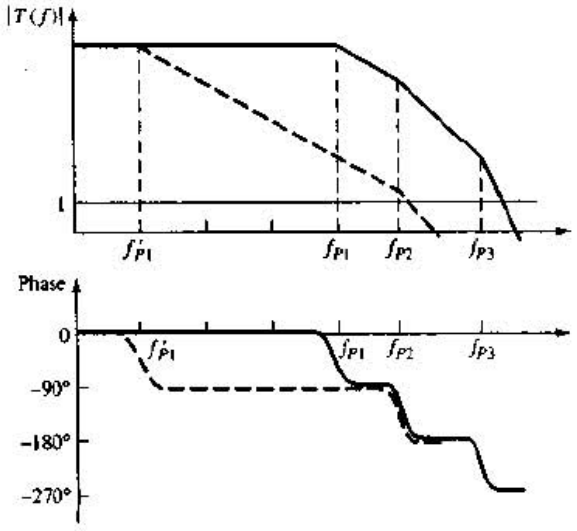

Figure 12.62 Bode plots of loop gain for three-stage amplifier, before (solid curves) and after (dotted curves) incorporating Miller compensation capacitor: (a) magnitude and (b) phase

A detailed analysis of the system using Miller compensation shows that pole f_{P2} does not remain constant; it increases. This phenomenon is called **pole-splitting**. The increase in f_{P2} is actually beneficial, because it increases the phase margin, or the frequency at which a particular phase margin is achieved.

Test Your Understanding

12.31 Consider a three-pole amplifier with a loop gain function given by

$$T(f) = \frac{10^5}{\left(1 + j\frac{f}{5 \times 10^5}\right)\left(1 + j\frac{f}{10^7}\right)\left(1 + j\frac{f}{5 \times 10^8}\right)}$$

Stabilize the circuit by inserting a new dominant pole. Assume the original poles are not altered. At what frequency must the new pole be placed to achieve a phase margin of 45 degrees? (Ans. $f_{PD} = 7.07$ Hz)

12.32 The loop gain function for an amplifier is described in Exercise 12.31. To stabilize the circuit, move the first pole $f_{P1} = 5 \times 10^5$ Hz by introducing a compensation capacitor. Assume the second pole remains fixed. Determine the frequency to which the first pole must be moved to achieve a phase margin of 45 degrees. (Ans. $f_{PD} = 141$ Hz)

12.33 A dc amplifier has a single-pole response with a pole frequency of $f_{PD} = 100$ Hz and a low-frequency gain of $A_o = 2 \times 10^5$. The amplifier is operated in a closed-loop system with $\beta = 0.05$. Find the closed-loop low-frequency gain and bandwidth. (Ans. $A_f(0) \cong 20$, $f_C \cong 1$ MHz)

12.11 SUMMARY

- In a feedback circuit, a portion of the output signal is fed back to the input and combined with the input signal. In negative feedback, a portion of the output signal is subtracted from the input signal. In positive feedback, a portion of the output signal is added to the input signal.
- An important advantage of negative feedback is that the closed-loop amplifier gain is essentially independent of individual transistor parameters and is a function only of the feedback elements.
- Negative feedback increases bandwidth, may increase the signal-to-noise ratio, reduces nonlinear distortion, and controls input and output impedance values at the expense of reduced gain magnitude.
- A series input connection is used when the input signal is a voltage, and a shunt input connection is used when the input signal is a current. A series output connection is used when the output signal is a current, and a shunt output connection is used when the output signal is a voltage.
- The loop gain factor of a feedback amplifier is defined as $T = A\beta$, which is dimensionless and where A is the gain of the basic amplifier and β is the feedback factor. The loop gain is a function of frequency and is complex when the input capacitance of each transistor stage is taken into account.
- A three-stage negative feedback amplifier is guaranteed to be stable if, at the frequency for which the phase of the loop gain is -180 degrees, the magnitude is less than unity.