- A common technique of frequency compensation utilizes the Miller multiplication effect by incorporating a feedback capacitor across, usually, the second stage of the basic amplifier.

CHECKPOINT

After studying this chapter, the reader should have the ability to:

✔ Describe some of the advantages and disadvantages of negative feedback. (Section 12.2)

✔ Discuss the general characteristics of the four basic feedback configurations in terms of input and output signals and input and output resistances. (Section 12.3)

✔ Analyze feedback circuits. (Sections 12.4–12.7)

✔ Design a feedback circuit given the input signal and desired output signal. (Sections 12.4–12.7)

✔ Determine the loop gain of a feedback circuit. (Section 12.8)

✔ Determine whether or not a three-stage feedback amplifier is stable. (Section 12.9)

✔ Stabilize a three-stage amplifier using frequency compensation techniques. (Section 12.10)

REVIEW QUESTIONS

1. What are the two general types of feedback and what are the advantages and disadvantages of each type?
2. Write the ideal form of the general feedback transfer function.
3. Define the loop gain factor.
4. What is the difference between open-loop gain and closed-loop gain?
5. Describe what is meant by the terms (a) gain sensitivity and (b) bandwidth extension.
6. Sketch an ideal series input connection. What is the input signal?
7. Sketch an ideal shunt input connection. What is the input signal?
8. Sketch an ideal series output connection. What is the output signal?
9. Sketch an ideal shunt output connection. What is the output signal?
10. Is the input resistance of a series input connection smaller or larger than that of the basic amplifier? Explain why from the input connection.
11. Is the input resistance of a shunt input connection smaller or larger than that of the basic amplifier? Explain why from the input connection.
12. Is the output resistance of a series output connection smaller or larger than that of the basic amplifier? Explain why from the output connection.
13. Is the output resistance of a shunt output connection smaller or larger than that of the basic amplifier. Explain why from the output connection.
14. Describe the characteristics of a voltage amplifier.
15. Describe the characteristics of a current amplifier.
16. Describe the characteristics of a transconductance amplifier.
17. Describe the characteristics of a transresistance amplifier.
18. Consider a noninverting op-amp circuit. Describe the type of input and output feedback connections.
19. Consider an inverting op-amp circuit. Describe the type of input and output feedback connections.
20. What is the Nyquist stability criterion for a feedback amplifier?

21. Using Bode plots, describe the conditions of stability and instability in a feedback amplifier.
22. What is phase margin?
23. What is meant by frequency compensation?
24. What is a dominant pole?
25. What is a common technique of frequency compensation in a feedback amplifier?

PROBLEMS

Section 12.2 Basic Feedback Concepts

12.1 A negative feedback amplifier has a closed-loop gain of $A_f = 80$ and an open-loop gain of $A = 10^5$. (a) What is the feedback transfer function β? (b) If the open-loop gain decreases by 20 percent, determine the percent change in the closed-loop gain. What is the new value of A_f? (c) Repeat parts (a) and (b) for $A = 10^3$.

12.2 (a) A feedback amplifier is connected as shown in Figure P12.2. Each basic amplifier stage has an open-loop gain of $A = 10$. The closed-loop gain is $A_f = 100$. Determine the required feedback transfer function β. (b) If the gain of each stage increases by 10 percent, determine the percent change in the closed-loop voltage gain.

12.3 Three voltage amplifiers are in cascade as shown in Figure P12.3 with various amplification factors. The 180 degree phase shift for negative feedback actually occurs in the basic amplifier itself. (a) Determine the value of β such that the closed-loop voltage gain is $A_{vf} = V_o/V_s = -120$. (b) Using the results of part (a), determine the percent change in A_{vf} if each individual amplifier gain decreases by 10 percent.

12.4 In a voltage-follower application, the feedback transfer function is $\beta = 1$ and the ideal closed-loop voltage gain is $A_f = 1$. Determine the magnitude of the open-loop voltage gain A such that the closed-loop gain in an actual feedback circuit is within 0.02 percent of the ideal value (see Equation 12.5).

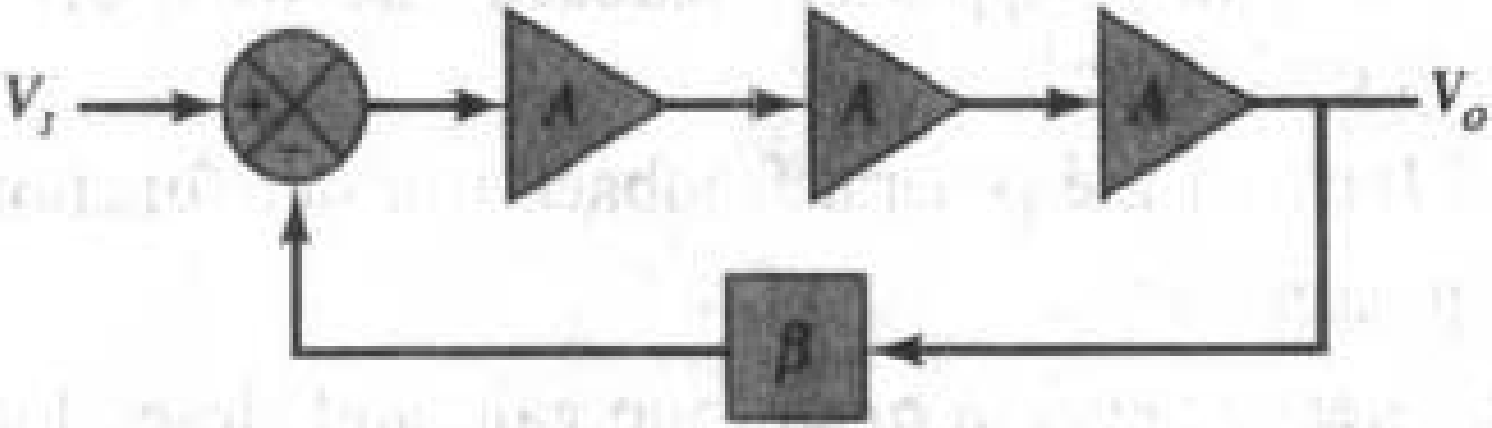


Figure P12.2

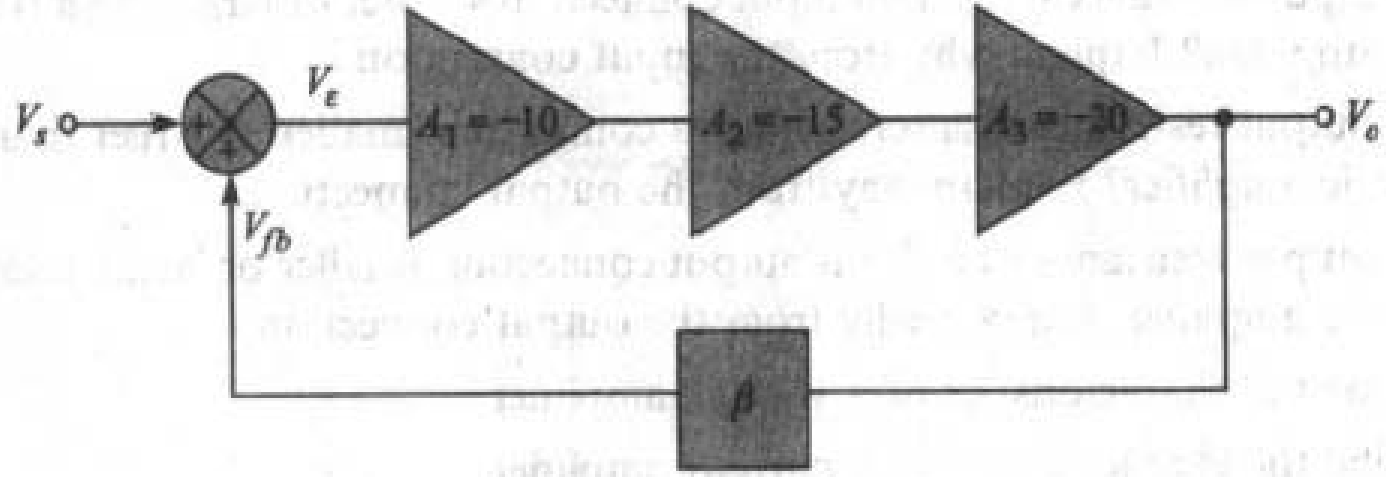


Figure P12.3

12.5 An op-amp has an open-loop low-frequency gain of $A = 10^5$ and an open-loop 3 dB frequency $f_H = 4$ Hz. If an inverting amplifier with a closed-loop low-frequency gain of $|A_{vf}| = 50$ uses this op-amp, determine the closed-loop bandwidth.

12.6 (a) Determine the closed-loop bandwidth of a noninverting amplifier with a gain of 50. The op-amp has the characterisics described in Problem 12.5. (b) If the noninverting amplifier gain is reduced to 10, determine the bandwidth.

12.7 An inverting amplifier uses an op-amp with an open-loop 3 dB frequency of 5 Hz, and has a gain of $|A_{vf}| = 50$ and a bandwidth of 20 kHz. Determine the required open-loop low-frequency op-amp gain.

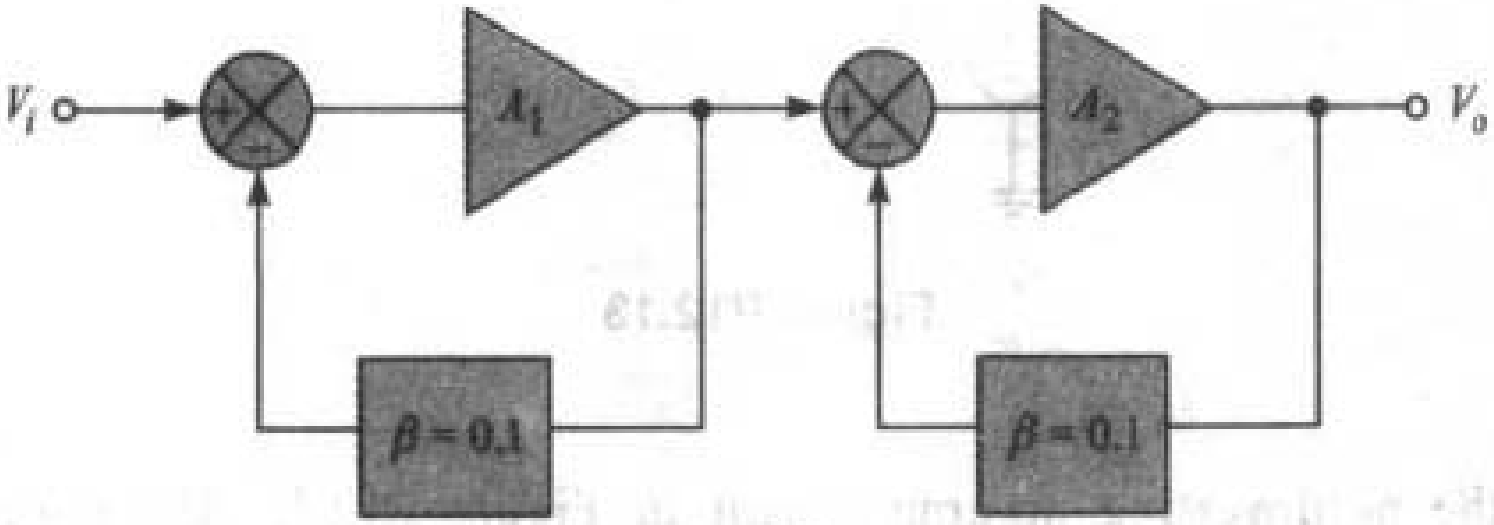
12.8 Consider two open-loop amplifiers in cascade, with a noise signal generated between the two amplifiers as in Figure 12.3(a). Assume the amplification of the first stage is $A_2 = 100$ and that of the second stage is $A_1 = 1$. If $V_{in} = 10$ mV and $V_n = 1$ mV, determine the signal-to-noise ratio at the output.

12.9 Two feedback configurations are shown in Figures P12.9(a) and (b). At low input voltages, the two gains are $A_1 = A_2 = 90$ and at higher input voltages, the gains change to $A_1 = A_2 = 60$. Determine the change in closed-loop gain, $A_f = V_o/V_i$, for the two feedback circuits. (See Figure 12.4.) Which feedback configuration will result in less distortion in the output signal?

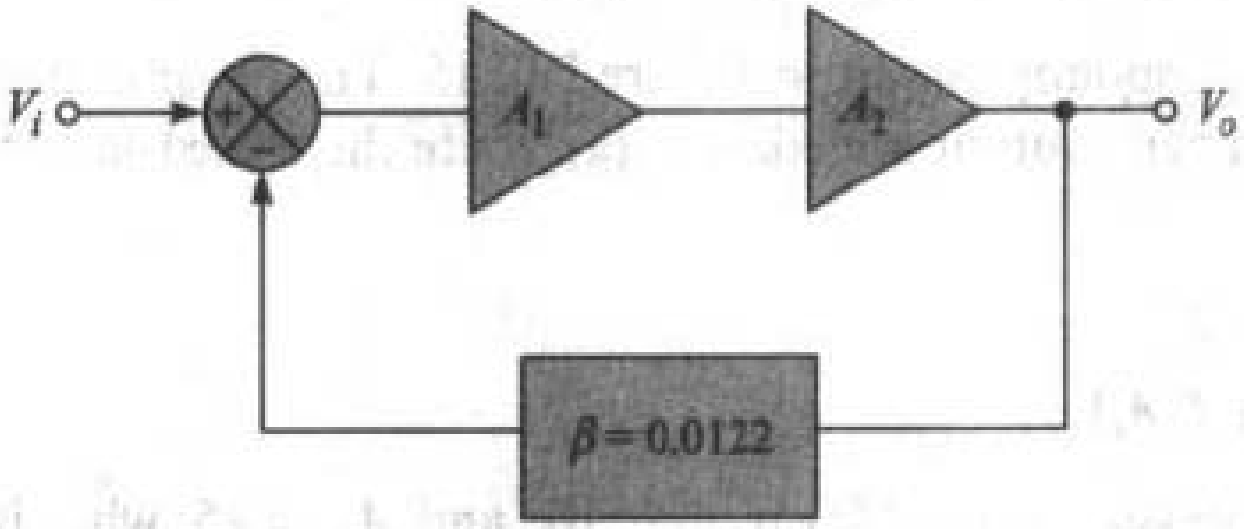
Figure P12.9

D12.10 Determine the type of feedback configuration that should be used in a design to achieve the following objectives: (a) low input resistance and low output resistance, (b) high input resistance and high output resistance, (c) low input resistance and high output resistance, and (d) high input resistance and low output resistance.

12.11 Consider a series of amplifiers and feedback circuits connected in the ideal feedback configurations. In each case the input resistance to the basic amplifier is $R_i = 10\,\text{k}\Omega$, the output resistance of the basic amplifier is $R_o = 1\,\text{k}\Omega$, and the loop gain is $T = 10^4$. (a) Determine the maximum possible input resistance and minimum possible input resistance to the feedback circuit. (b) Determine the maximum possible output resistance and minimum possible output resistance to the feedback circuit.



(a)



(b)

D12.12 A compound transconductance amplifier is to be designed by connecting two basic feedback amplifiers in cascade. What two amplifiers should be connected in cascade to form the compound circuit? Is there more than one possible design?

Section 12.3 Ideal Feedback Topologies

12.13 Consider the noninverting op-amp circuit in Figure P12.13. The input resistance of the op-amp is $R_i = \infty$ and the output resistance is $R_o = 0$, but the op-amp has a finite gain A. (a) Write the closed-loop transfer function in the form

$$A_{vf} = \frac{v_o}{v_s} = \frac{A}{(1 + \beta A)}$$

(b) What is the expression for β? (c) If $A = 10^5$ and $A_{vf} = 20$, what is the required β and R_2/R_1? (d) If A decreases by 10 percent, what is the percent change in A_{vf}?

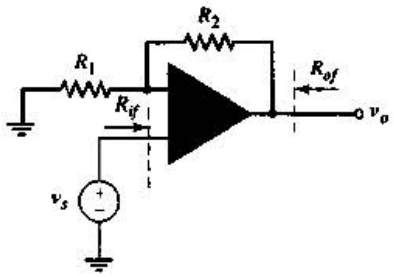


Figure P12.13

12.14 For the noninverting op-amp circuit in Figure P12.13, the parameters are: $A = 10^5$, $A_{vf} = 20$, $R_i = 100\,\text{k}\Omega$, and $R_o = 100\,\Omega$. Determine the closed-loop input and output resistances, R_{if} and R_{of}, respectively.

12.15 Consider the op-amp circuit in Figure P12.15. The op-amp has a finite gain, so that $i_o = Ai_\varepsilon$, and a zero output impedance. (a) Write the closed-loop transfer function in the form

$$A_{if} = \frac{i_o}{i_s} = \frac{A_i}{(1 + \beta_i A_i)}$$

(b) What is the expression for β_i? (c) If $A_i = 10^5$ and $A_{if} = 25$, what is the required β_i and R_F/R_3? (d) If A_i decreases by 15 percent, what is the percent change in A_{if}?

12.16 An op-amp circuit is shown in Figure P12.15. Its parameters are as described in Problem 12.15, except that $R_i = 2\,\text{k}\Omega$ and $R_o = 20\,\text{k}\Omega$. Determine the closed-loop input and output resistances, R_{if} and R_{of}, respectively.

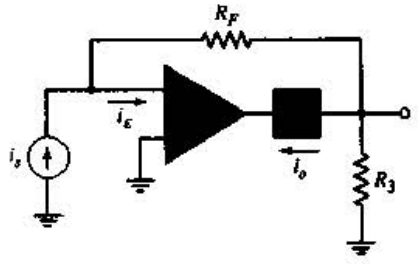


Figure P12.15

Figure P12.17

12.17 Consider the circuit in Figure P12.17. The input resistance of the op-amp is $R_i = \infty$ and the output resistance is $R_o = 0$. The op-amp has a finite gain, so that $i_o' = A_g v_\varepsilon$. The current gain of the transistor is h_{FE}. (a) Write the closed-loop transfer function in the form

$$A_{gf} = \frac{i_o}{v_s} = \frac{A_g}{(1 + \beta_s A_g)}$$

where A_g is the open-loop gain of the system. (b) What is the expression for β_s? (c) If $A_g = 5 \times 10^5$ mS and $A_{gf} = 10$ mS, what is the required β_s and R_E? (d) If A_g increases by 10 percent, what is the corresponding percent change in A_{gf}?

12.18 The circuit shown in Figure P12.17 has the same parameters as described in Problem 12.17, except that $R_i = 20\,\text{k}\Omega$ and $R_o = 50\,\text{k}\Omega$. Determine the closed-loop input and output resistances, R_{if} and R_{of}, respectively.

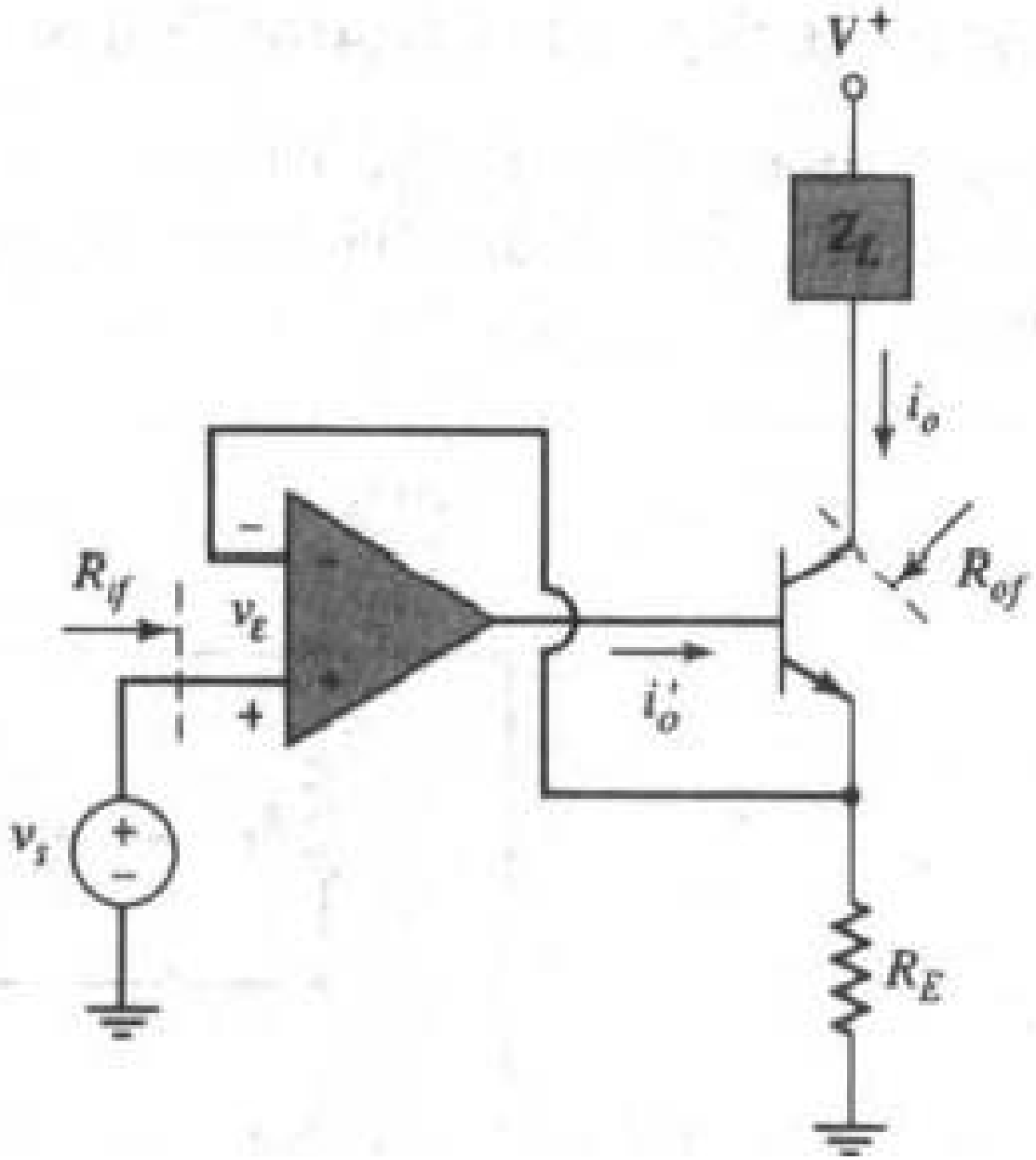
12.19 Consider the current-to-voltage converter circuit shown in Figure P12.19. The input resistance R_{if} is assumed to be small, the output resistance is $R_o = 0$, and the op-amp gain A_z is large. (a) Write the closed-loop transfer function in the form

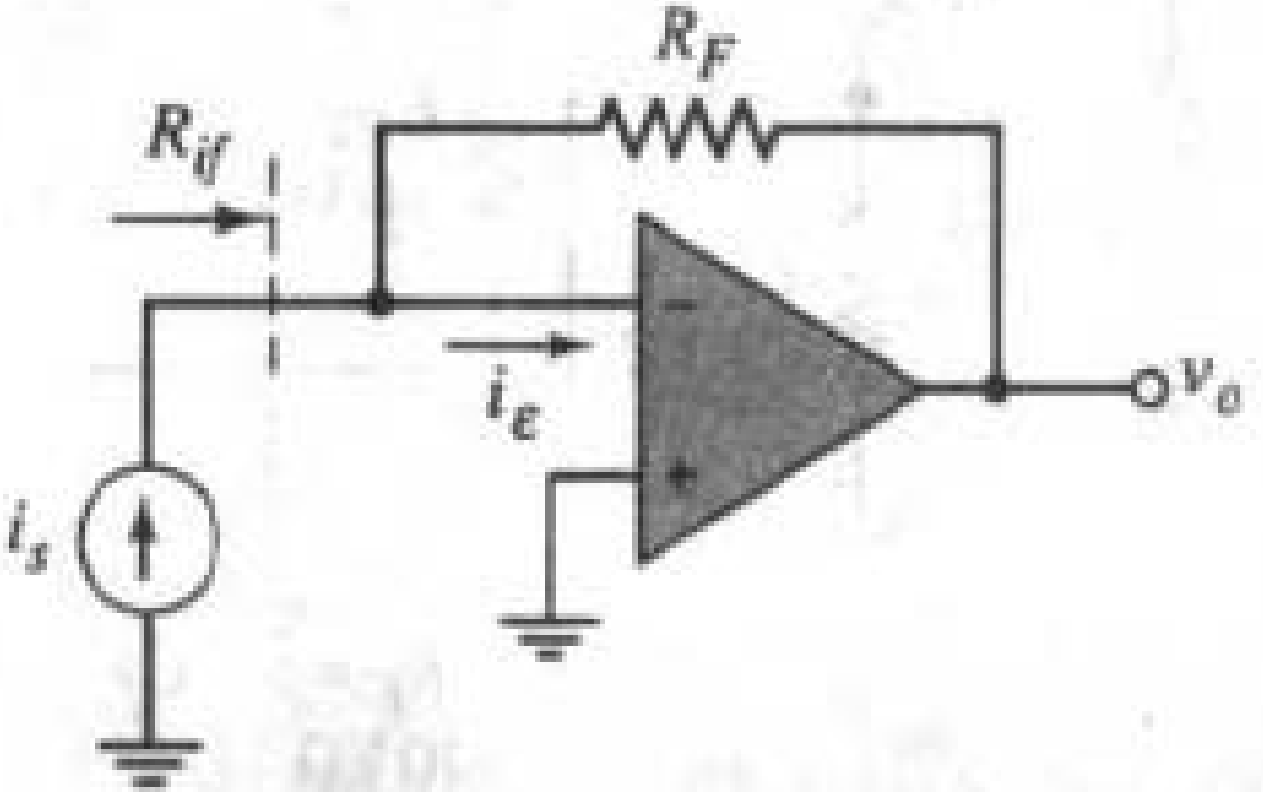
$$A_{zf} = \frac{v_o}{i_s} = \frac{A_z}{(1 + \beta_g A_z)}$$

(b) What is the expression for β_g? (c) If $A_z = 5 \times 10^6\,\Omega$ and $A_{zf} = 5 \times 10^4\,\Omega$, what is the required β_g and R_F? (d) If A_z decreases by 10 percent, what is the percent change in A_{zf}?

12.20 For the current-to-voltage converter circuit in Figure P12.19, the parameters are as described in Problem 12.19. If $R_i = 10\,\text{k}\Omega$, determine the closed-loop input resistance R_{if}.

Figure P12.19


V+
Z_L
i_o
R_{of}
R_{if}
v_ε
i_o'
v_s
R_E


R_F
R_{if}
i_ϵ
v_o
i_s

Section 12.4 Voltage (Series–Shunt) Amplifiers

***12.21** Consider the voltage amplifier in Figure P12.21. The op-amp parameters are $A_v = 5 \times 10^3$, $R_i = 10\,\text{k}\Omega$, and $R_o = 1\,\text{k}\Omega$, and the transistor parameters are $h_{FE} = 100$ and $V_A = 80\,\text{V}$. Determine A_{vf}, R_{if}, and R_{of}.

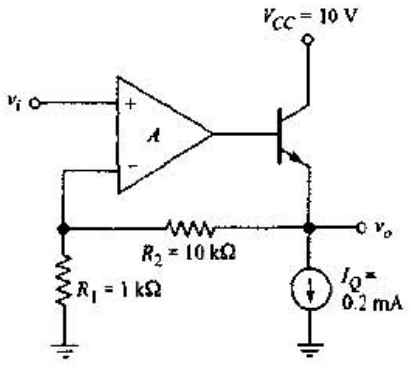


Figure P12.21

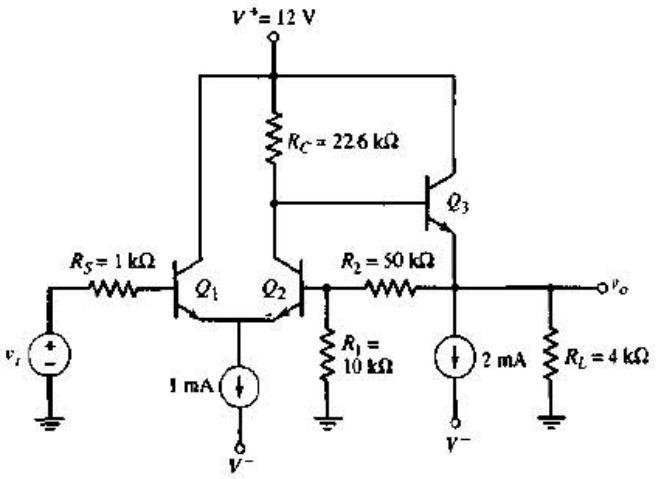


Figure P12.22

12.22 The circuit in Figure P12.22 is an example of a series–shunt feedback circuit. Assume the transistor parameters are: $h_{FE} = 100$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, and $V_A = \infty$. (a) Determine the quiescent collector currents and the dc voltage at the output. (b) Determine the small-signal voltage gain $A_{vf} = v_o/v_i$.

12.23 Consider the series–shunt feedback circuit in Figure P12.23, with transistor parameters: $h_{FE} = 120$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, and $V_A = \infty$. (a) Determine the small-signal parameters for Q_1, Q_2, and Q_3. Using nodal analysis, determine: (b) the small-signal voltage gain $A_{vf} = v_o/v_i$, (c) the input resistance R_{if}, and (d) the output resistance R_{of}.

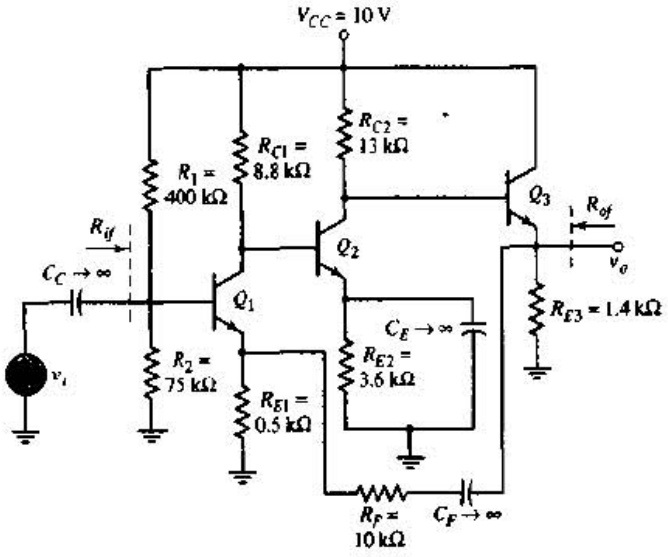


Figure P12.23

12.24 Consider the BiCMOS circuit in Figure P12.24. The transistor parameters are: $K_n = 0.2\,\text{mA/V}^2$, $V_{TN} = 1\,\text{V}$, $\lambda = 0$ for M_1; and $h_{FE} = 100$, $V_{EB}(\text{on}) = 0.7\,\text{V}$, $V_A = \infty$ for Q_2. (a) Determine the small-signal parameters for M_1 and Q_2. (b) Find the small-signal voltage gain $A_{vf} = v_o/v_i$. (c) Determine the output resistance R_{of}.

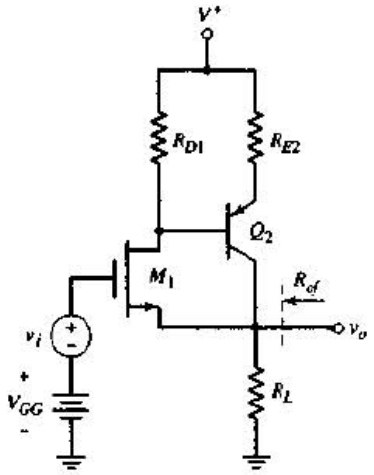


Figure P12.24

12.25 Figure P12.25 shows a basic source-follower circuit. Assume the transistor is biased such that $I_{DQ} = 0.5\,\text{mA}$. Assume the transistor parameters are $V_{TN} = 1\,\text{V}$ and $\lambda = 0$, and let $R_S = 2\,\text{k}\Omega$. (a) If the transistor conduction parameter is $K_n = 0.5\,\text{mA/V}^2$, determine $A_{vf} = v_o/v_i$ and R_{of}. (b) Determine the percent change in A_{vf} and R_{of} if the conduction parameter increases to $K_n = 0.8\,\text{mA/V}^2$.

12.26 The transistor parameters for the circuit in Figure P12.26 are: $h_{FE} = 50$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, and $V_A = \infty$. Using nodal analysis, determine the closed-loop small-signal voltage gain $A_{vf} = v_o/v_s$ at the midband frequency.

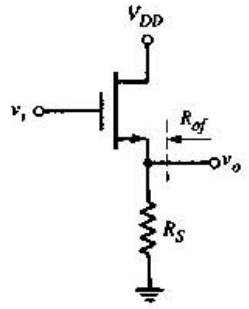


Figure P12.25

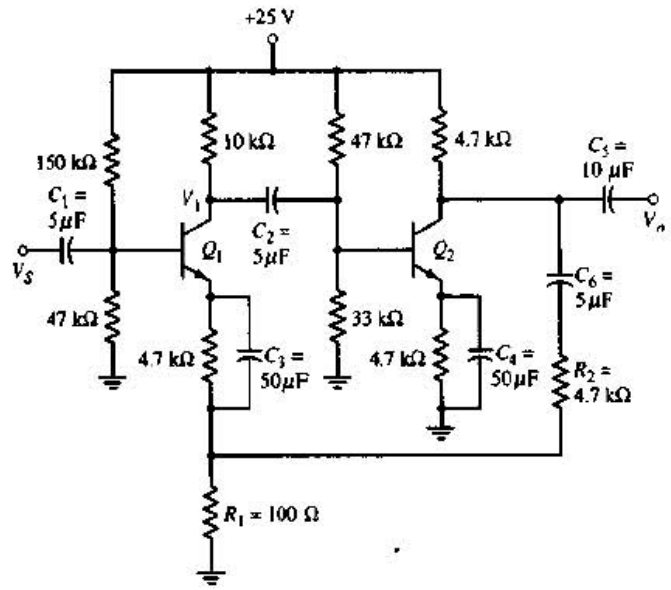


Figure P12.26

***D12.27** Design a discrete transistor feedback voltage amplifier to provide a voltage gain of 50. Assume the available transistors have parameters: $h_{FE} = 120$ and $V_A = \infty$. The signal voltage source has a source resistance of $R_S = 2\,\text{k}\Omega$ and the load is $R_L = 3\,\text{k}\Omega$. Verify the design with a computer simulation. Determine R_{if} and R_{of}.

***RD12.28** Redesign the feedback circuit in Figure P12.22 using MOSFETs to provide a voltage gain of $A_{vf} = 10$. Assume transistor parameters of $V_{TN} = 2\,\text{V}$, $k_n' = 80\,\mu\text{A/V}^2$, and $\lambda = 0$.

Section 12.5 Current (Shunt–Series) Amplifiers

D12.29 An op-amp current gain amplifier (shunt–series configuration) is shown in Figure P12.29. Design the circuit such that the load current is $I_o = 20\,\text{mA}$ when the input current is $I_s = 200\,\mu\text{A}$.

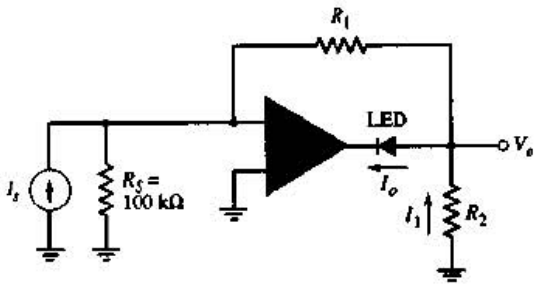


Figure P12.29

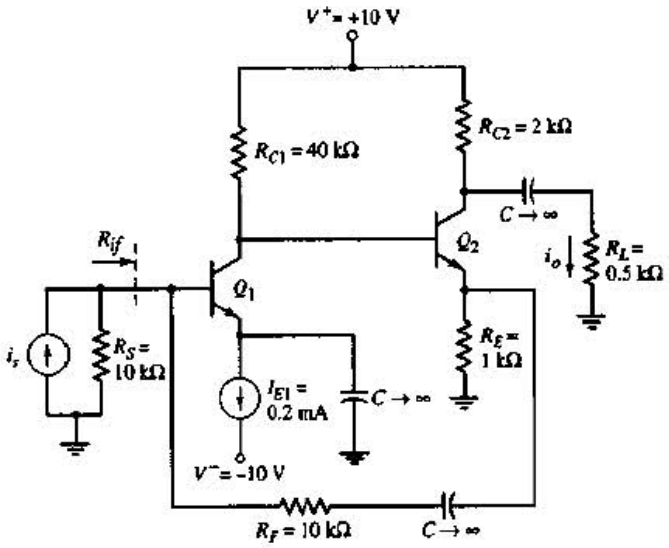


Figure P12.30

12.30 The circuit in Figure P12.30 has transistor parameters: $h_{FE} = 100$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, and $V_A = \infty$. (a) From the quiescent values, determine the small-signal parameters for Q_1 and Q_2. (b) Using nodal analysis, determine the small-signal closed-loop current gain $A_{if} = i_o/i_s$. (c) Using nodal analysis, find the input resistance R_{if}.

12.31 (a) Using the small-signal equivalent circuit in Figure 12.25 for the circuit in Figure 12.24(a), derive the expression for the small-signal current gain $A_{if} = I_o/I_s$. (b) Using the circuit parameters given in Figure 12.24(a) and assuming transistor parameters $h_{FE} = 100$ and $V_A = \infty$, calculate the value of A_{if}. Compare this answer with the results of Example 12.9.

***12.32** The circuit in Figure P12.32 is an example of a shunt–series feedback circuit. A signal proportional to the output current is fed back to the shunt connection at the base of Q_1. However, the circuit may be used as a voltage amplifier. Assume transistor parameters of $h_{FE} = 120$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, and $V_A = \infty$. (a) Determine the small-signal parameters for Q_1 and Q_2. (b) Using nodal analysis, determine the small-signal voltage gain $A_v = v_o/v_s$.

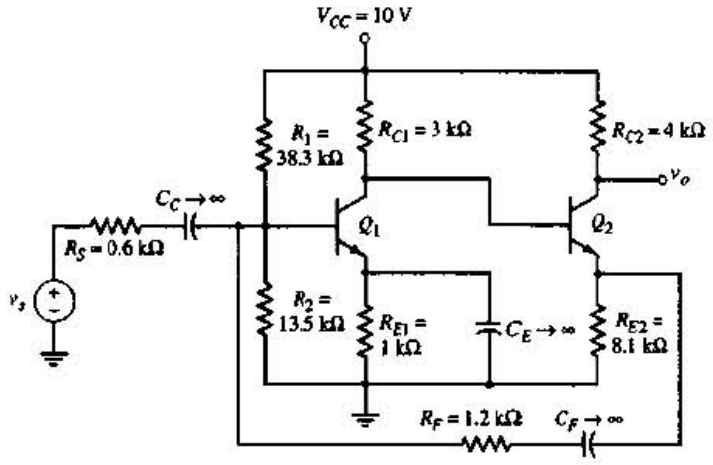


Figure P12.32

12.33 Consider the circuit in Figure P12.32 with transistor parameters, $h_{FE} = 120$, $V_{BE}(\text{on}) = 0.7$ V, and $V_A = \infty$. Using nodal analysis, determine the input resistance R_{if}.

12.34 For the transistors in the circuit in Figure P12.34, the parameters are: $h_{FE} = 50$, $V_{BE}(\text{on}) = 0.7$ V, and $V_A = \infty$. Using nodal analysis, determine the closed-loop current gain $A_{if} = i_o/i_s$.

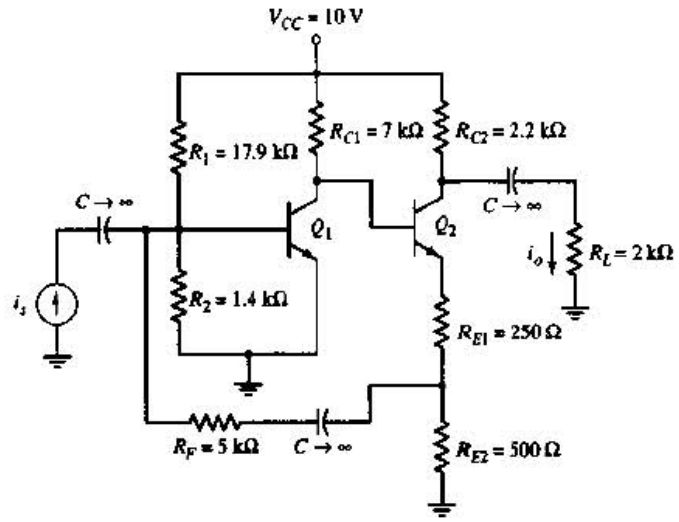


Figure P12.34

***D12.35** Design a discrete transistor feedback current amplifier to provide a current gain of 30. Assume the available transistors have parameters $h_{FE} = 120$ and $V_A = \infty$. The signal current source has a source resistance of $R_S = 25\,\text{k}\Omega$ and the load is $R_L = 500\,\Omega$. Verify the design with a computer simulation. Determine R_{if} and R_{of}.

Section 12.6 Transconductance (Series–Series) Amplifiers

12.36 The circuit in Figure P12.36 is the ac equivalent circuit of a series-series feedback amplifier. Assume that the bias circuit, which is not shown, results in quiescent collector currents of $I_{C1} = 0.5\,\text{mA}$, $I_{C2} = 1\,\text{mA}$, and $I_{C3} = 2\,\text{mA}$. Assume transistor

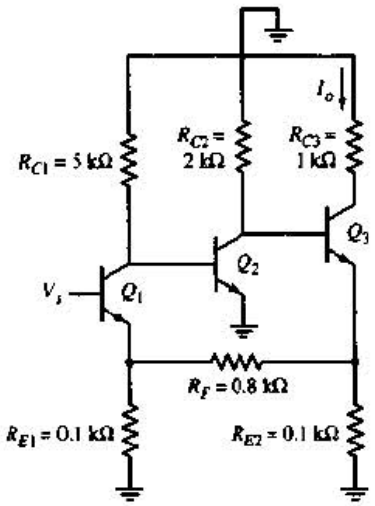


Figure P12.36

parameters of $h_{FE} = 120$ and $r_o = \infty$. Determine the transconductance transfer function $A_{gf} = I_o/V_s$.

RD12.37 Using a computer simulation analysis, redesign the circuit in Figure P12.36 by changing the value of R_F to achieve a transconductance gain of $A_{gf} = I_o/V_s = 120$ mA/V.

12.38 In the circuit in Figure P12.38, the transistor parameters are: $h_{FE} = 100$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, and $V_A = \infty$. Determine the transconductance transfer function $A_{gf} = i_o/v_s$.

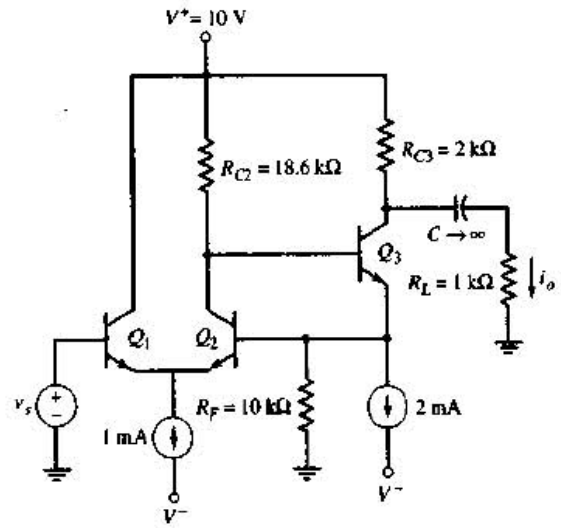


Figure P12.38

D12.39 Design a feedback amplifier to supply a current to an LED. The diode current should be $I_o = 10^{-3} V_i$, where V_i is the amplifier input voltage, which has a range of 0 to 10 V. The voltage source has an output resistance of $R_S = 1\,\text{k}\Omega$. The op-amp parameters are $R_i = 5\,\text{k}\Omega$, $R_o = 50\,\Omega$, and the low-frequency open-loop voltage gain is 5×10^3. Determine the gain, input resistance, and output resistance, from a computer simulation.

Section 12.7 Transresistance (Shunt–Shunt) Amplifiers

12.40 Consider the common-emitter circuit in Figure P12.40, driven by an ideal signal current source. The transistor parameters are: $h_{FE} = 50$, $V_{EB}(\text{on}) = 0.7\,\text{V}$, and $V_A = 100\,\text{V}$. (a) Determine the input and output resistances, R_{if} and R_{of}, respectively. (b) Find the transresistance transfer function $A_{zf} = v_o/i_s$. (c) What happens in the feedback network if the capacitance is finite?

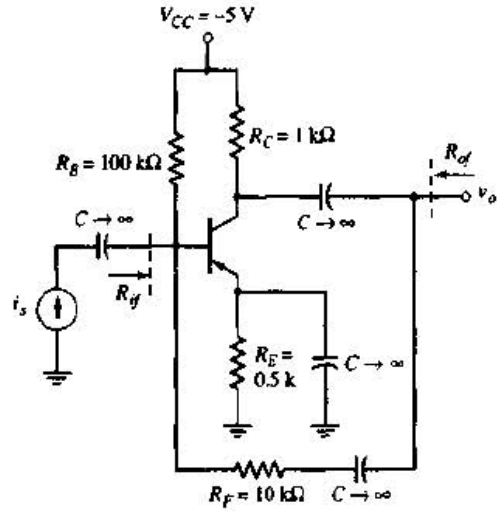


Figure P12.40

12.41 For the circuit shown in Figure P12.41, the transistor parameters are: $V_{TN} = 2\,\text{V}$, $K_n = 0.20\,\text{mA/V}^2$, and $\lambda = 0$. Determine: (a) the voltage gain $A_v = V_o/V_s$, (b) the transresistance transfer function $A_{zf} = V_o/I_s$, (c) the input impedance R_{if}, and (d) the output impedance R_{of}.

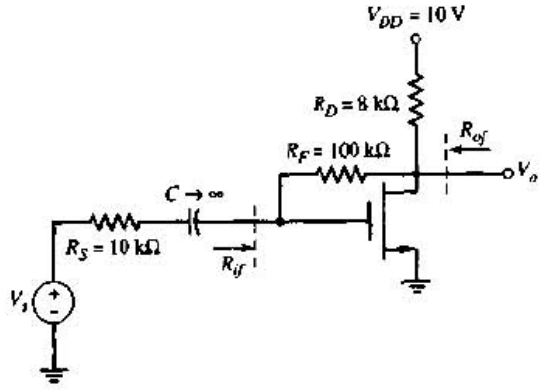


Figure P12.41

12.42 Consider the circuit in Figure P12.41. The transistor parameters are $V_{TN} = 1.5\,\text{V}$ and $\lambda = 0$. Determine the required value of transconductance g_m such that the magnitude of the closed-loop voltage gain is within 10 percent of the ideal value when $g_m \to \infty$.

12.43 For the circuit in Figure P12.43, the transistor parameters are: $h_{FE} = 150$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, and $V_A = \infty$. Determine the value of R_F that will result in a closed-loop voltage gain of $A_v = V_o/V_s = -5.0$.

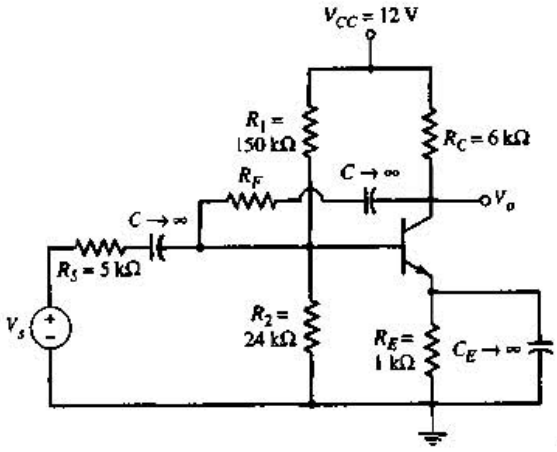


Figure P12.43

12.44 Consider the three-stage cascade feedback circuit in Figure 12.40. Each stage corresponds to the circuit in Figure P12.44, with transistor parameters: $h_{FE} = 180$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, and $V_A = \infty$. The source resistor is $R_S = 10\,\text{k}\Omega$, and the load resistor is $R_L = 4\,\text{k}\Omega$. Determine the value of R_F such that the closed-loop gain is $A_v = v_o/v_i = -80$.

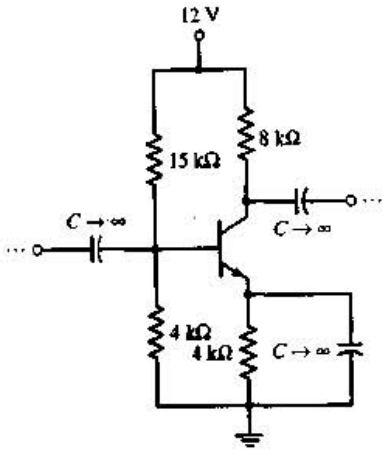


Figure P12.44

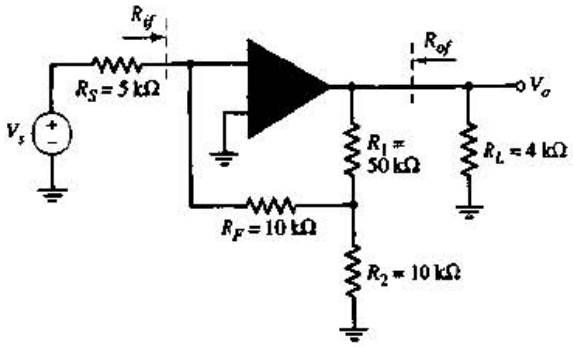


Figure P12.45

12.45 The op-amp in the circuit in Figure P12.45 has an open-loop differential voltage gain of $A_d = 10^4$. Neglect the current into the op-amp, and assume the output resistance looking back into the op-amp is zero. Determine: (a) the closed-loop voltage gain $A_v = V_o/V_s$, (b) the input resistance R_{if}, and (c) the output resistance R_{of}.

D12.46 Design a feedback transresistance amplifier using an op-amp with parameters $R_i = 10\,\text{k}\Omega$, $R_o = 100\,\Omega$, and a low-frequency open-loop gain of $A_v = 10^4$ to produce a

gain of 5 kΩ. The source resistance is $R_S = 500\,\Omega$ and the load resistance is $R_L = 2\,k\Omega$. Determine the actual gain, input resistance, and output resistance using a computer simulation.

Section 12.8 Loop Gain

12.47 The op-amp in Figure 12.20 has an open-loop differential input resistance R_i, an open-loop current gain A_i, and a zero output resistance. Break the feedback loop at an appropriate point, and derive the expression for the loop gain.

12.48 The small-signal parameters of the transistors in the circuit in Figure P12.23 are h_{FE} and $V_A = \infty$. Derive the expression for the loop gain.

12.49 Determine the loop gain T for the circuit in Figure P12.30. The transistor parameters are: $h_{FE} = 100$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, and $V_A = \infty$.

12.50 The transistor parameters for the circuit shown in Figure P12.40 are: $h_{FE} = 50$, $V_{BE}(\text{on}) = 0.7\,\text{V}$, and $V_A = 100\,\text{V}$. Find the loop gain T.

Section 12.9 Stability of the Feedback Circuit

12.51 A three-pole feedback amplifier has a loop gain given by

$$T(f) = \frac{\beta(10^5)}{\left(1 + j\frac{f}{5 \times 10^2}\right)\left(1 + j\frac{f}{10^4}\right)^2}$$

(a) Determine the frequency f_{180} at which the phase is -180 degrees. (b) At the frequency f_{180}, determine the value of β such that $|T(f_{180})| = 1$.

12.52 The open-loop gain of an amplifier is given by

$$A = \frac{5 \times 10^3}{\left(1 + j\frac{f}{10^4}\right)\left(1 + j\frac{f}{10^5}\right)^2}$$

Assuming the feedback function is not a function of frequency, determine the frequency at which the phase is 180 degrees. Determine the value of the feedback transfer function at which the amplifier can break into oscillation.

12.53 A loop gain function is given by

$$T(f) = \frac{\beta(10^3)}{\left(1 + j\frac{f}{10^4}\right)\left(1 + j\frac{f}{5 \times 10^4}\right)\left(1 + j\frac{f}{10^5}\right)}$$

Sketch the Nyquist plot for: (a) $\beta = 0.005$, and (b) $\beta = 0.05$. (c) Is the system stable or unstable in each case?

12.54 A three-pole feedback amplifier has a loop gain function given by

$$T(f) = \frac{\beta(5 \times 10^3)}{\left(1 + j\frac{f}{10^3}\right)^2\left(1 + j\frac{f}{5 \times 10^4}\right)}$$

(a) Sketch the Nyquist diagram for $\beta = 0.20$. (b) Determine the value of β that produces a phase margin of 80 degrees.

12.55 A three-pole feedback amplifier has a loop gain given by

$$T(f) = \frac{\beta(10^4)}{\left(1 + j\frac{f}{10^3}\right)\left(1 + j\frac{f}{10^4}\right)\left(1 + j\frac{f}{10^5}\right)}$$

Sketch Bode plots of the loop gain magnitude and phase for: (a) $\beta = 0.005$, and (b) $\beta = 0.05$. (c) Is the system stable or unstable in each case? If the system is stable, what is the phase margin?

12.56 An amplifier with a low-frequency open-loop gain of 10^5 has poles at 5×10^4 Hz, 10^5 Hz, and 5×10^5 Hz. Determine the feedback transfer function β and the low-frequency closed-loop gain for which the phase margin is 60 degrees.

12.57 A two-pole loop gain function is given by

$$T(f) = \frac{\beta(10^3)}{\left(1 + j\frac{f}{10^3}\right)^2}$$

(a) Determine the value of β that produces a phase margin of 60 degrees. (b) Using the results of part (a), sketch the Bode plots of the loop gain magnitude and phase.

12.58 The open-loop gain of an amplifier has pole frequencies at 10 kHz, 100 kHz, and 1 MHz. The low-frequency open-loop gain is 500 and the feedback transfer function is $\beta = 0.6$. Find the phase margin.

12.59 Sketch the Bode plots of the magnitude and phase of the function

$$T(f) = \frac{K}{\left(1 + j\frac{f}{10^2}\right)^2}$$

for: (a) $K = 1$, and (b) $K = 10^3$.

12.60 Consider a four-pole feedback system with a loop gain given by

$$T(f) = \frac{\beta(10^3)}{\left(1 + j\frac{f}{10^3}\right)\left(1 + j\frac{f}{10^4}\right)\left(1 + j\frac{f}{10^5}\right)\left(1 + j\frac{f}{10^6}\right)}$$

Determine the value of β that produces a phase margin of 45 degrees.

Section 12.10 Frequency Compensation

12.61 A feedback amplifier has a low-frequency loop gain of 5000 and three poles at $f_{P1} = 300$ kHz, $f_{P2} = 2$ MHz, and $f_{P3} = 25$ MHz. A dominant pole is to be added such that the phase margin if 45 degrees. Assuming the original poles remain fixed, determine the dominant pole frequency.

12.62 A feedback amplifier with a compensation capacitor has a low-frequency loop gain of $T(0) = 100$ dB and poles at $f'_{P1} = 10$ Hz, $f_{P2} = 5$ MHz, and $f_{P3} = 10$ MHz. (a) Find the frequency at which $|T(f)| = 1$, and determine the phase margin. (b) If the frequency f'_{P1} is due to a compensation capacitor $C_F = 20$ pF, determine the new dominant pole frequency f'_{P1} and phase margin if the compensation capacitor is increased to $C_F = 75$ pF.

12.63 The equivalent circuit at the interface between the first and second stages of an op-amp is shown in Figure P12.63. The parameters are $R_{o1} = 500\,\text{k}\Omega$, $R_{i2} = 1\,\text{M}\Omega$, and $C_i = 2$ pF. (a) Determine the pole frequency for this part of the circuit. (b) Determine the additional Miller capacitance C_M that would need to be added so that the pole frequency is moved to $f_{PD} = 10$ Hz.

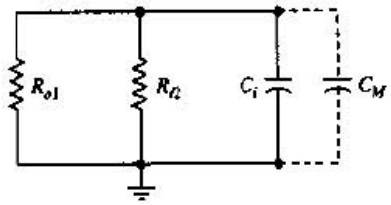


Figure P12.63

12.64 The loop gain function of a feedback amplifier has its first two poles at $f_{p1} = 2\,\text{MHz}$ and $f_{p2} = 12\,\text{MHz}$, and has a low-frequency gain of $|T(0)| = 80\,\text{dB}$. The amplifier is to be stabilized by moving the first pole by using Miller compensation. Assuming that the second pole f_{p2} remains fixed, find the frequency to which f_{p1} must be changed to produce a 45 degree phase margin.

12.65 A three-pole amplifier has its first two poles at $f_{P1} = 1\,\text{MHz}$ and $f_{P2} = 10\,\text{MHz}$, and has a low-frequency open-loop gain of $|A_o| = 80\,\text{dB}$. A dominant pole is to be inserted such that the closed-loop system remains stable when the closed-loop, low-frequency gain is $|A_f(0)| = 5$. Determine the dominant pole frequency assuming the initial poles remain constant.

12.66 The amplifier described in Problem 12.61 is to be stabilized by moving the first pole by using Miller compensation. Assuming f_{P2} remains constant, determine the frequency to which f_{P1} must be moved.

COMPUTER SIMULATION PROBLEMS

12.67 Using a computer analysis, investigate the loop gain factor for the circuit in Figure 12.24(a). Investigate the loop gain as a function of R_F and of h_{FE}.

12.68 Consider the multistage feedback circuit in Figure 12.40. Assume each stage corresponds to the circuit in Figure P12.44. Let $R_F = 200\,\text{k}\Omega$, $R_S = 10\,\text{k}\Omega$, and $R_L = 4\,\text{k}\Omega$. (a) Investigate the open-loop voltage gain $A_v = v_o/v_e$ as a function of the individual transistor current gains h_{FE}. (b) Determine the required value of open-loop gain and transistor current gain needed to achieve a closed-loop gain that is within 2 percent of the ideal value.

12.69 Consider the circuit in Figure P12.32. From a computer analysis, determine the loop gain and the closed-loop transfer gain.

12.70 Consider the circuit in Figure 12.47 with parameters given in Example 12.18. The circuit is biased with $V_{CC} = 10\,\text{V}$, and it includes $0.5\,\text{k}\Omega$ emitter resistors. Insert coupling and emitter bypass capacitors where appropriate. (a) Determine the loop gain versus frequency characteristic. (b) Insert a compensation capacitor, $C_1 = 30\,\text{pF}$, between the collector and base of Q_2. Replot the loop gain versus frequency characteristic and determine whether the system is stable or unstable.

12.71 Consider the circuit in Figure 12.16 with parameters: $A_v = 10^4$, $R_i = 100\,\text{k}\Omega$, $R_o = 50\,\Omega$, $R_2 = 20\,\text{k}\Omega$, and $R_1 = 1\,\text{k}\Omega$. Determine the exact values of voltage gain A_{vf}, input resistance R_{if}, and output resistance R_{of}, from a computer analysis.

DESIGN PROBLEMS

[Note: Each design should be correlated with a computer simulation analysis.]

***D12.72** Redesign the circuit shown in Figure 12.45(a) to provide a loop gain of at least 100. What are the values of I_{CQ} and V_{CEQ}?

***D12.73** An op-amp has a low-frequency open-loop gain of 10^5 and a dominant-pole frequency of 5 Hz. Design a cascade of noninverting amplifiers with an overall minimum gain of 800 and a minimum bandwidth of 12 kHz.

***D12.74** An op-amp has a low-frequency open-loop gain of 5×10^4 and a dominant-pole frequency of 10 Hz. Using this op-amp, design a preamplifier system that can amplify the output of a microphone and produce a 1 V peak signal over a frequency range from 10 Hz to 15 kHz. The equivalent circuit of the microphone is a voltage source in series with an output resistance. The voltage source produces a 5 mV peak signal and the output resistance is 10 kΩ.

***D12.75** The equivalent circuit of a transducer that measures the speed of a motor is a current source in parallel with an output resistance. The current source produces an output of 1 μA per revolution of the motor and the output resistance is 50 kΩ. Design a discrete transistor circuit that produces a full-scale output of 5 V for a maximum motor speed of 60 revolutions per second. The nominal transistor current gain is $h_{FE} = 100$ with tolerances of ±20 percent. The accuracy of the output signal is to remain within ±1 percent.

CHAPTER

13

Operational Amplifier Circuits

13.0 PREVIEW

Thus far, we have considered basic circuit configurations, such as the common emitter, emitter follower, and diff-amp, among others. We have discussed the basic concepts in design and analysis, including biasing techniques, frequency response, and feedback effects. In this chapter, we combine basic circuit configurations to form larger analog circuits that are fabricated as integrated circuits. Operational amplifiers are used extensively in electronic systems, so we concentrate on several forms of the operational amplifier circuit in this chapter.

We introduced the ideal op-amp in Chapter 9. Now, we analyze and design the circuitry of the op-amp, to determine how the various circuit configurations can be combined to form a nearly ideal op-amp.

The LM741 is an example of an all-bipolar general-purpose op-amp. Even though this op-amp is considered a classic, it still provides a good case study in which we perform a detailed analysis to determine both the dc and the small-signal characteristics of the circuit. Since the 741 is an internally compensated op-amp, we determine the dominant-pole frequency and the unity-gain bandwidth.

All-CMOS op-amps can be designed for special on-chip applications. In general, these op-amps are designed to drive other CMOS circuits, which form high capacitive loads. A goal of this chapter is to enable the reader to design CMOS op-amp circuits, including choosing transistor width-to-width ratios, to meet particular specifications, including power and gain parameters.

13.1 GENERAL OP-AMP CIRCUIT DESIGN

An operational amplifier, in general, is a three-stage circuit, as shown in Figure 13.1, and is fabricated as an integrated circuit. The first stage is a differential amplifier, the second stage provides additional voltage gain, and the third stage provides current gain and low output impedance. A feedback capacitor is often included in the second stage to provide frequency compensation as discussed in the last chapter. In some cases, in particular with MOSFET op-amp circuits, only the first two stages are used.

We have on numerous occasions made reference to the op-amp. In Chapter 9, we analyzed and designed op-amp circuits using the ideal op-amp

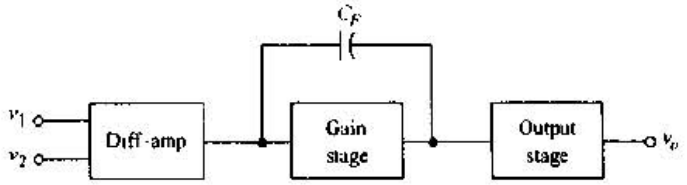


Figure 13.1 General block diagram of an operational amplifier

model. In Chapter 10, we introduced current-source biasing and introduced the active load. The differential amplifier, using current source biasing and active loads was considered in Chapter 11. We also introduced the bipolar Darlington pair in Chapter 11, which is often used as a second gain stage. Previously, in Chapter 8, we considered the class-AB output stage that is often used in operational amplifier circuits. These individual building blocks will now be combined to form the operational amplifier.

In Chapter 9, as mentioned, we analyzed and designed ideal op-amp circuits. Practical operational amplifiers, as we will see in this chapter, exhibit characteristics that deviate from the ideal characteristics. Once we have analyzed these practical op-amp circuits and determined some of their nonideal properties, we will then consider, in the next chapter, the effect of these nonideal characteristics on the op-amp circuits.

13.1.1 General Design Philosophy

All stages of the operational amplifier circuit are direct coupled. There are no coupling capacitors and there are also no bypass capacitors. These types of capacitors would require extremely large areas on the IC chip and hence are impractical. In addition, resistors whose values are over approximately 50 kΩ are avoided in ICs, since they also require large areas and introduce parasitic effects. Op-amp circuits are designed with transistors having matching characteristics.

We may begin to design a simple bipolar operational amplifier by using the knowledge gained in the previous chapters. Figure 13.2 shows the general configuration of the circuit. The first stage will be a differential pair, Q_1 and Q_2, biased with a Widlar current source, Q_3, Q_4, and R_2, and using a three-transistor active load. Assuming matched transistors, we expect the dc voltage at the collector of Q_6 to be two base-emitter voltage drops below the positive bias voltage. Therefore, the Darlington pair, Q_8 and Q_9, that forms the second stage should be properly biased. The bias current for Q_8 is supplied by the Widlar current source, Q_4, Q_{10}, and R_3. The output stage is the complementary push–pull, emitter-follower configuration of Q_{11} and Q_{12}. The crossover distortion is eliminated by including the diodes D_1 and D_2. The emitter-follower configuration provides low output resistance so that the op-amp can drive a load with minimal loading effect. By changing the value of R_3 slightly, the current through Q_{10} and Q_8 can be changed, which will change the collector–emitter voltages across these transistors. This part of the circuit then acts as a dc voltage shifter such that the output voltage, v_O, can be set equal to zero for zero input voltages.

From results that we have derived previously, we expect the differential-mode voltage gain of the first stage to be in the range of 10^2–10^3, depending on

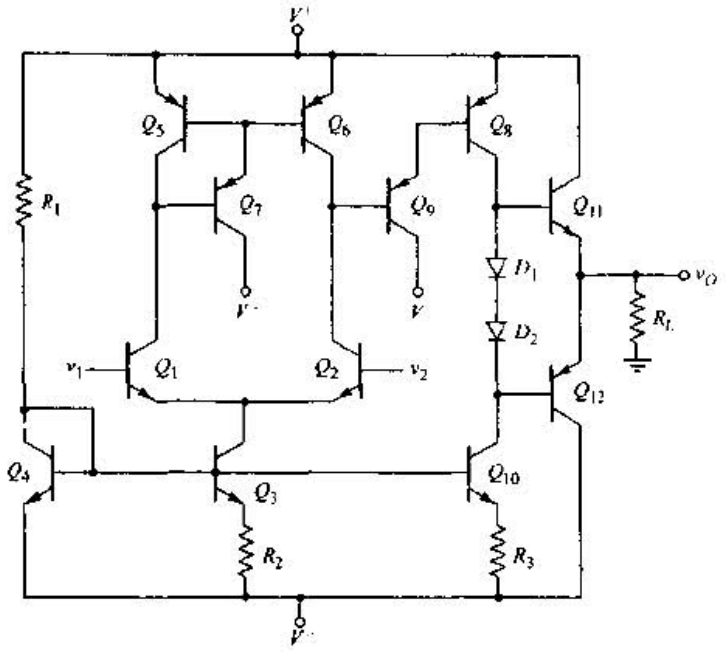


Figure 13.2 A simple bipolar operational amplifier

the specific transistor parameters and the voltage gain of the second stage to also be the range of 10^2–10^3. The voltage gain of the output stage, an emitter follower, is essentially unity. The overall voltage gain of the op-amp circuit is then expected to be in the range of 10^4–10^6. From our study in Chapter 9, this magnitude of voltage gain is required for the circuit to act essentially as an ideal op-amp.

The same op-amp configuration can be designed with MOS transistors. In general, as we have seen, BJT circuits have higher voltage gains, whereas MOSFET circuits have higher input resistances. So, whether a bipolar or MOSFET design is used depends to a large extent on the specific application of the op-amp.

13.1.2 Circuit Element Matching

Integrated circuit design is based directly on the ability to fabricate transistors on a chip that have nearly identical characteristics. In the analysis of current mirrors in Chapter 10 and differential amplifiers in Chapter 11, we assumed that transistors in a given circuit were matched. Transistors are **matched** when they have identical parameters. For bipolar transistors, the parameters are I_S, β, and V_A. Recall that I_S includes the electrical parameters of the semiconductor material as well as the cross-sectional area (geometry) of the base-emitter junction. For NMOS transistors, the parameters are V_{TN}, K_n, and λ_n, and for PMOS transistors, the same corresponding parameters must be identical. Again, recall that the parameter K_n contains semiconductor parameters as well as the width-to-length (geometry) of the transistor.

The absolute parameter values of transistors on an IC chip may vary substantially (on the order of ±25 percent) from one IC chip to the next

because of processing variations. However, the variation in parameter values of adjacent or nearby transistors on a given IC chip are usually within a fraction of a percent. In general, much of an amplifier design is based on the ratio of transistor parameters and on the ratio of resistor values rather than on the absolute values. For this reason, the operational amplifiers described in this chapter can be fabricated as ICs, but are almost impossible to fabricate with discrete circuit elements.

Test Your Understanding

***13.1** Using a computer simulation, determine the dc voltages and currents in the bipolar op-amp circuit in Figure 13.2. Use reasonable resistor values. Adjust the value of R_3 such that the output voltage is nearly zero for zero input voltages.

13.2 Consider the basic diff-amp with active load and current biasing in Figure 13.2. Using a computer simulation, investigate the change in the voltage at the collector of Q_2 as Q_1 and Q_2, and also Q_5 and Q_6, become slightly mismatched.

13.2 A BIPOLAR OPERATIONAL AMPLIFIER CIRCUIT

The **741 op-amp** has been produced since 1966 by many semiconductor device manufacturers. Since then, there have been many advances in op-amp design, but the 741 is still a widely used general-purpose op-amp. Even though the 741 is a fairly old design, it still provides a useful case study to describe the general circuit configuration and to perform a detailed dc and small-signal analysis. From the ac analysis, we determine the voltage gain and the frequency response of this circuit.

13.2.1 Circuit Description

Figure 13.3 shows the equivalent circuit of the 741 op-amp. For easier analysis, we break the overall circuit down into its basic circuits and consider each one individually.

As with most op-amps, this circuit consists of three stages: the input differential amplifier, the gain stage, and the output stage. Figure 13.3 also shows a separate bias circuit, which establishes the bias currents throughout the op-amp. Like most op-amps, the 741 is biased with both positive and negative supply voltages. This eliminates the need for input coupling capacitors, which in turn means that the circuit is also a dc amplifier. The dc output voltage is zero when the applied differential input signal is zero. Typical supply voltages are $V^+ = 15\,\text{V}$ and $V^- = -15\,\text{V}$, although input voltages as low as $\pm 5\,\text{V}$ can be used.

Input Diff-Amp

The input diff-amp stage is more complex than those previously covered. The input stage consists of transistors Q_1 through Q_7, with biasing established by transistors Q_8 through Q_{12}. The two input transistors Q_1 and Q_2 act as emitter

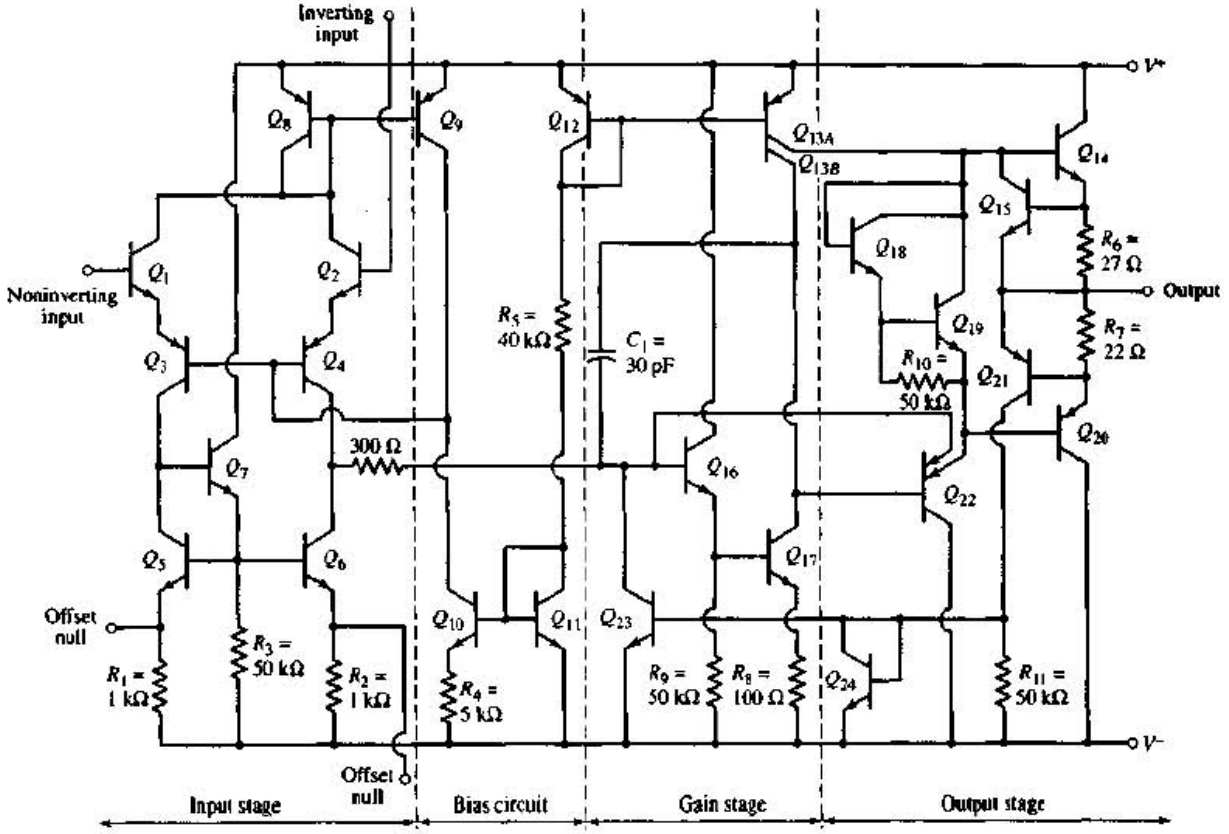


Figure 13.3 Equivalent circuit, 741 op-amp

followers, which results in a high differential input resistance. The differential output currents from Q_1 and Q_2 are the inputs to the common-base amplifier formed by Q_3 and Q_4, which provides a relatively large voltage gain.

Transistors Q_5, Q_6, and Q_7, with associated resistors R_1, R_2, and R_3, form the active load for the diff-amp. A single-sided output at the common collectors of Q_4 and Q_6 is the input signal to the following gain stage.

The dc output voltage at the collector of Q_6 is at a lower potential than the inputs at the bases of Q_1 and Q_2. As the signal passes through the op-amp, the dc voltage level shifts several times. By design, when the signal reaches the output terminal, the dc voltage should be zero if a zero differential input signal is applied. The two null terminals on the input stage are used to make appropriate adjustments to accomplish this design goal. The "null technique" and the corresponding portion of the circuit will be discussed in detail in the next chapter.

The dc current biasing is initiated through the diode-connected transistors Q_{12} and Q_{11} and resistor R_5. Transistors Q_{11} and Q_{10}, with resistor R_4, form a Widlar current source that establishes the bias currents in the common-base transistors Q_3 and Q_4, as well as the current mirror formed by Q_9 and Q_8.

Transistors Q_3 and Q_4 are lateral pnp devices, which refers to the fabrication process and the geometry of the transistors. Lateral pnp transistors provide added protection against voltage breakdown, although the current gain is smaller than in npn devices.

Figure 13.4(a) shows a basic common-emitter differential pair used as the input to a diff-amp. If the input voltage V_1 were to be connected to a supply voltage of 15 V, with V_2 at ground potential, then the B–E junction of Q_2 would be reverse biased by approximately 14.3 V. Since the breakdown voltage of an npn B–E junction is typically in the range of 3–6 V, transistor Q_2 in Figure 13.4(a) would probably enter breakdown and suffer permanent damage.

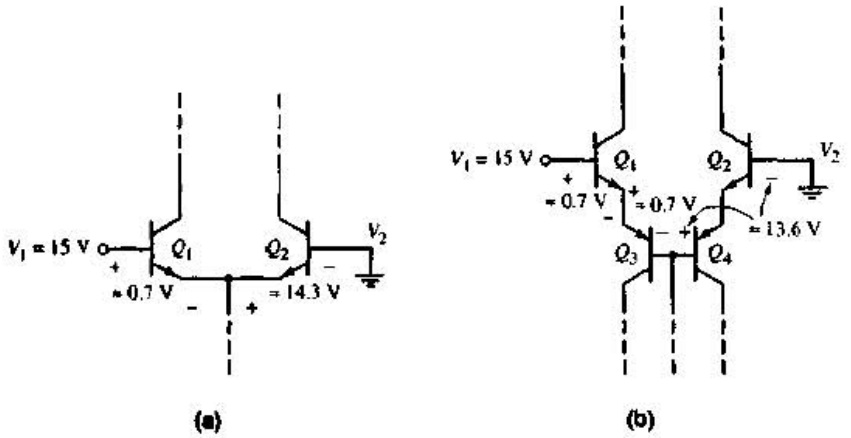


Figure 13.4 (a) Basic common-emitter differential pair, with a large differential voltage and (b) the 741 input stage, with a large differential voltage

By comparison, Figure 13.4(b) shows the input stage of the 741 op-amp with the same input voltages. The B–E junctions of Q_1 and Q_3 are forward biased, which means that the series combination of B–E junctions of Q_2 and Q_4 is reverse biased by approximately 13.6 V. The breakdown voltage of a lateral pnp B–E junction is typically on the order of 50 V, which means that for this input voltage polarity, the B–E junction of Q_4 provides the necessary breakdown protection for the input diff-amp stage.

Gain Stage

The second, or gain, stage consists of transistors Q_{16} and Q_{17}. Transistor Q_{16} operates as an emitter follower; therefore, the input resistance of the gain stage is large. As previously discussed, a large input resistance to the gain stage minimizes loading effects on the diff-amp stage.

Transistor Q_{13} is effectively two transistors connected in parallel, with common base and emitter terminals. The area of Q_{13A} is effectively one-fourth the area of Q_{12}, and the area of Q_{13B} is effectively three-fourths that of Q_{12}. Transistor Q_{13B} provides the bias current for Q_{17} and also acts as an active load to produce a high-voltage gain. Transistor Q_{17} operates in a common-emitter configuration; therefore, the voltage at the collector of Q_{17} is the input signal to the output stage. The signal undergoes another dc level shift as it goes through this gain stage.

The 741 is internally compensated by the feedback capacitor C_f connected between the output and input terminals of the gain stage. This Miller compensation technique assures that the 741 op-amp forms stable feedback circuits.

Output Stage

The output stage of an op-amp should provide a low output resistance, as well as a current gain, if it is to drive relatively large load currents. The output stage is therefore a class-AB circuit consisting of the complementary emitter-follower pair Q_{14} and Q_{20}.

The output of the gain stage is connected to the base of Q_{22}, which operates as an emitter follower and provides a very high input resistance; the gain stage therefore suffers no significant loading effects due to the output stage. Transistor Q_{13A} provides a bias current for Q_{22}, as well as for Q_{18} and Q_{19}, which are used to establish a quiescent bias current in the output transistors Q_{14} and Q_{20}. Transistors Q_{15} and Q_{21} are referred to as short-circuit protection devices. These transistors are normally off; they conduct only if the output is inadvertently connected to ground, resulting in a very large output current. We will consider the characteristics of the output stage in Section 13.2.2.

An abbreviated data sheet for the 741 is shown in Table 13.1. During our discussions in this chapter, we will compare our analysis results to the values in the table. A more complete data sheet for the 741 op-amp is given in Appendix C.

Table 13.1 Data for 741 at $T = 300\,^{\circ}\text{K}$ and supply voltage of $\pm 15\,\text{V}$

Parameter	Minimum	Typical	Maximum	Units
Input bias current		80	500	nA
Differential-mode input resistance	0.3	2.0		MΩ
Input capacitance		1.4		pF
Output short-circuit current		25		mA
Open-loop gain ($R_L \geq 2\,\text{k}\Omega$)	50,000	200,000		V/V
Output resistance		75		Ω
Unity-gain frequency		1		MHz

Test Your Understanding

13.3 The 741 op-amp in Figure 13.3 is biased at $V^+ = 15\,\text{V}$ and $V^- = -15\,\text{V}$. Assume $V_{BE}(\text{npn}) = V_{EB}(\text{pnp}) = 0.6\,\text{V}$. Determine the input common-mode voltage range, neglecting voltage drops across R_1 and R_2. (Ans. $-12.6 < v_{in}(\text{cm}) \leq 14.4\,\text{V}$)

13.4 (a) If the 741 op-amp in Figure 13.3 is biased at $V^+ = 15$ and $V^- = -15\,\text{V}$, estimate the maximum and minimum output voltages such that the op-amp remains biased in its linear region. (b) Repeat part (a) if $V^+ = 5\,\text{V}$ and $V^- = -5\,\text{V}$. (Ans. (a) $-13.2 \leq v_O \leq 13.8\,\text{V}$ (b) $-3.2 \leq v_O \leq 3.8\,\text{V}$)

13.2.2 DC Analysis

In this section, we will analyze the dc characteristics of the 741 op-amp to determine the dc bias currents. We assume that both the noninverting and inverting input terminals are at ground potential, and that the dc supply

voltages are $V^+ = 15\,\text{V}$ and $V^- = -15\,\text{V}$. As an approximation, we assume $V_{BE} = 0.6\,\text{V}$ for npn transistors and $V_{EB} = 0.6\,\text{V}$ for pnp transistors. In most dc calculations, we neglect dc base currents, although we include base current effects in a few specific cases.

Bias Circuit and Input Stage

Figure 13.5 shows the bias circuit and input stage portion of the 741 circuit. The reference current, which is established in the bias circuit branch composed of Q_{12}, Q_{11}, and R_5, is

$$I_{\text{REF}} = \frac{V^+ - V_{EB12} - V_{BE11} - V^-}{R_5} \tag{13.1}$$

Transistors Q_{11} and Q_{10} and resistor R_4 form a Widlar current source. Therefore, I_{C10} is determined from the relationship

$$I_{C10}R_4 = V_T \ln\left(\frac{I_{\text{REF}}}{I_{C10}}\right) \tag{13.2}$$

where V_T is the thermal voltage and Q_{10} and Q_{11} are assumed to be matched transistors.

Neglecting base currents, $I_{C8} = I_{C9} = I_{C10}$. The quiescent collector currents in Q_1 through Q_4 are then

$$I_{C1} = I_{C2} = I_{C3} = I_{C4} = \frac{I_{C10}}{2} \tag{13.3}$$

Assuming the dc currents in the input stage are exactly balanced, the dc voltage at the collector of Q_6, which is the input to the second stage, is the same as the dc voltage at the collector of Q_5. We can write

$$V_{C6} = V_{BE7} + V_{BE6} + I_{C6}R_2 + V^- \tag{13.4}$$

As previously discussed, the dc level shifts through the op-amp.

Example 13.1 **Objective:** Calculate the dc currents in the bias circuit and input stage of the 741 op-amp.

The bias circuit and input stage are shown in Figure 13.5.

Solution: From Equation (13.1), the reference current is

$$I_{\text{REF}} = \frac{V^+ - V_{EB12} - V_{BE11} - V^-}{R_5} = \frac{15 - 0.6 - 0.6 - (-15)}{40} = 0.72\,\text{mA}$$

Current I_{C10} is found from Equation (13.2), as follows:

$$I_{C10}(5) = (0.026)\ln\left(\frac{0.72}{I_{C10}}\right)$$

By trial and error, we find that $I_{C10} = 19\,\mu\text{A}$. The bias currents in the input stage are then

$$I_{C1} = I_{C2} = I_{C3} = I_{C4} = 9.5\,\mu\text{A}$$

From Equation (13.4), the voltage at the collector of Q_6 is

$$V_{C6} = V_{BE7} + V_{BE6} + I_{C6}R_2 + V^- = 0.6 + 0.6 + (0.0095)(1) + (-15)$$

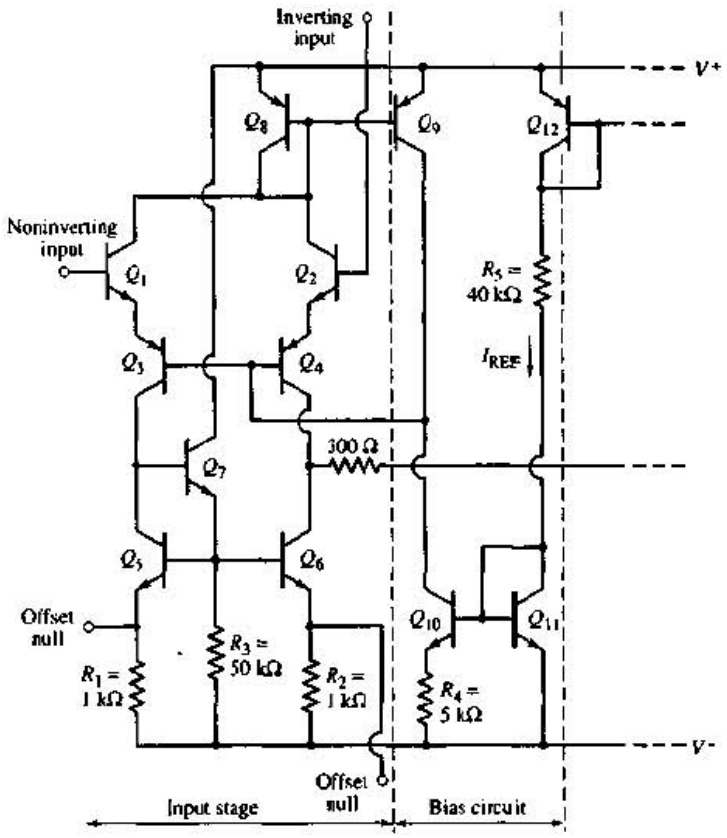


Figure 13.5 Bias circuit and input stage portion of 741 op-amp circuit

or

$$V_{C6} \cong -13.8\,\text{V}$$

Comment: The bias currents in the input stage are quite small; the input base currents at the noninverting and inverting terminals are generally in the nanoampere range. Small bias currents mean that the differential input resistance is large.

The transistor current gain of the lateral pnp transistors Q_3, Q_4, Q_8, and Q_9 may be relatively small, which means that the base currents in these transistors may not be negligible. To determine the effect of the base currents, consider the expanded input stage shown in Figure 13.6. The base currents in the npn transistors are still assumed to be negligible. Current I_{C10} establishes the base currents in Q_3 and Q_4, which then establish the emitter currents designated as I. At the Q_8 collector, we have

$$2I = I_{C8} + \frac{2I_{C9}}{\beta_p} = I_{C9}\left(1 + \frac{2}{\beta_p}\right) \tag{13.5}$$

Since Q_8 and Q_9 are matched, $I_{C8} = I_{C9}$. Then,

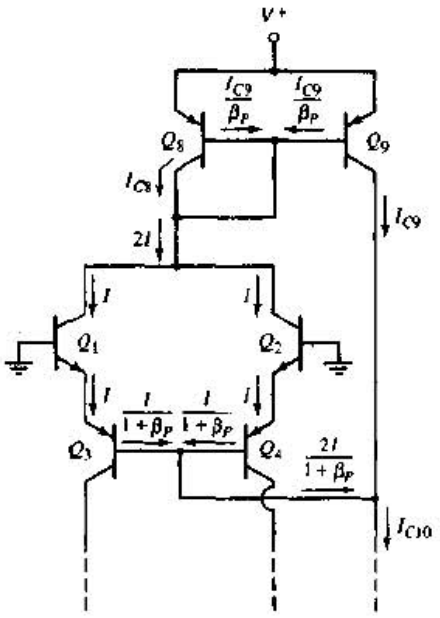


Figure 13.8 Expanded input stage, 741 op-amp, showing base currents

$$I_{C10} = \frac{2I}{1+\beta_p} + I_{C9} = \frac{2I}{1+\beta_p} + \frac{2I}{\left(1+\frac{2}{\beta_p}\right)} = 2I\left[\frac{\beta_p^2+2\beta_p+2}{\beta_p^2+3\beta_p^2+2}\right] \tag{13.6}$$

Even if the pnp transistor base currents are not negligible, the bias currents in Q_1 and Q_2 are, from Equation (13.6), very nearly

$$I = \frac{I_{C10}}{2} \tag{13.7}$$

This bias current is essentially the same as originally assumed in Equation (13.3).

Test Your Understanding

13.5 The current gain β_n of the npn transistors in the 741 op-amp input stage in Figure 13.5 is $\beta_n = 200$. Determine the input base currents to Q_1 and Q_2. (Ans. 47.5 nA)

***13.6** Consider the input stage and bias circuit in Figure 13.5, with $V^+ = 15\,\text{V}$ and $V^- = -15\,\text{V}$. If $I_S = 10^{-14}\,\text{A}$ for each transistor, determine I_{REF}, V_{BE11}, V_{BE10}, and V_{BE6}. (Ans. $I_{\text{REF}} = 0.718\,\text{mA}$, $V_{BE11} = 0.650\,\text{V}$, $V_{BE10} = 0.556\,\text{V}$, $V_{BE6} = 0.537\,\text{V}$)

Gain Stage

Figure 13.7 shows the reference portion of the bias circuit and the gain stage. The reference current is given by Equation (13.1). Transistors Q_{12} and Q_{13}

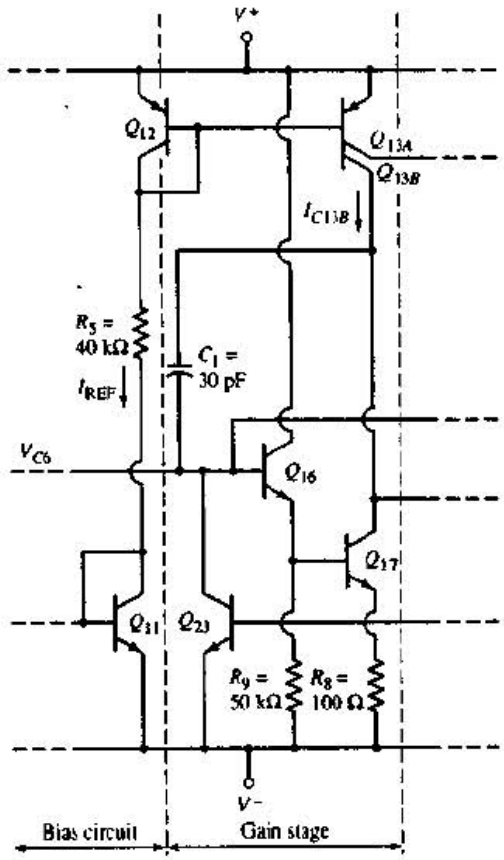


Figure 13.7 Reference circuit and gain stage, 741 op-amp

form a current mirror, and Q_{13B} has a scale factor 0.75 times that of Q_{12}. Neglecting base currents, current I_{C13B} is then

$$I_{C13B} = 0.75 I_{REF} \tag{13.8}$$

The emitter current in Q_{16} is the sum of the base current in Q_{17} and the current in R_9, as follows:

$$I_{C16} \cong I_{E16} = I_{B17} + \frac{I_{E17} R_8 + V_{BE17}}{R_9} \tag{13.9}$$

Example 13.2 **Objective:** Calculate the bias currents in the gain stage of the 741 op-amp in Figure 13.7.

Solution: In Example 13.1, we determined the reference current to be $I_{REF} = 0.72\,\text{mA}$. From Equation (13.8), the collector current in Q_{17} is

$$I_{C17} = I_{C13B} = 0.75 I_{REF} = (0.75)(0.72) = 0.54\,\text{mA}$$

Assuming $\beta = 200$ for the npn transistor, the collector current in Q_{16} is, from Equation (13.9),

$$I_{C16} \cong I_{B17} + \frac{I_{E17}R_8 + V_{BE17}}{R_9} = \frac{0.54}{200} + \frac{(0.54)(0.1) + 0.6}{50}$$

or

$$I_{C16} = 15.8\,\mu\text{A}$$

Comment: The small bias current in Q_{16}, in conjunction with the resistor R_9, ensures that the input resistance to the gain stage is large, which minimizes loading effects on the diff-amp stage. The small bias current in Q_{16} also means that the base current in Q_{16} is negligible, as assumed in the dc analysis of the input stage.

Output Stage

Figure 13.8 shows the basic output stage of the 741 op-amp. This is a class-AB configuration, discussed in Chapter 8. The I_{Bias} is supplied by Q_{13A}, and the input signal is applied to the base of Q_{22}, which operates as an emitter follower. The combination of Q_{18} and Q_{19} establishes two B–E voltage drops between the base terminals of Q_{14} and Q_{20}, causing the output transistors to be biased slightly in the conducting state. This V_{BB} voltage produces quiescent collector currents in Q_{14} and Q_{20}. Biasing both Q_{14} and Q_{20} "on" with no signal present at the input ensures that the output stage will respond linearly when a signal is applied to the op-amp input.

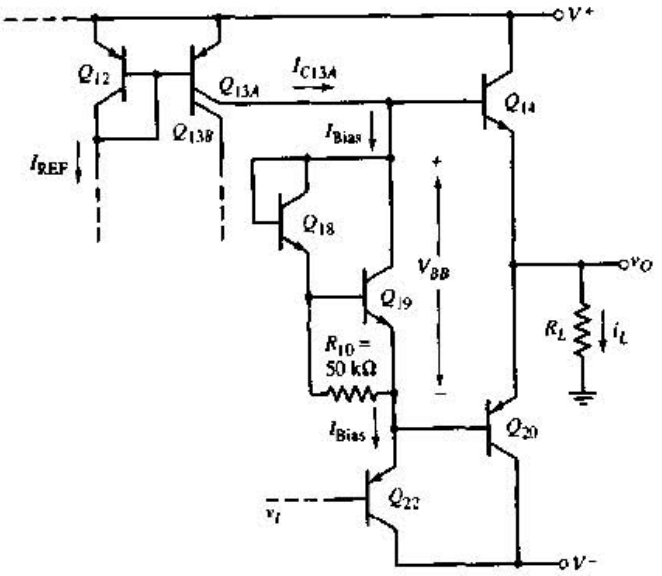


Figure 13.8 Basic output stage, 741 op-amp, showing currents and voltages

The collector of Q_{13A} has a scale factor of 0.25 times that of Q_{12}. Neglecting base currents, current I_{C13A} is

$$I_{C13A} = 0.25I_{\text{REF}} = I_{\text{Bias}} \tag{13.10}$$

where I_{REF} is given by Equation (13.1). Neglecting base currents, the collector current in Q_{22} is also equal to I_{Bias}. The collector current in Q_{18} is

$$I_{C18} \cong \frac{V_{BE19}}{R_{10}} \tag{13.11}$$

Therefore,

$$I_{C19} = I_{Bias} - I_{C18} \tag{13.12}$$

Example 13.3 **Objective:** Calculate the bias currents in the output stage of the 741 op-amp.

Consider the output stage shown in Figure 13.8. Assume the reverse saturation currents of Q_{18} and Q_{19} are $I_S = 10^{-14}$ A, and the reverse saturation currents of Q_{14} and Q_{20} are $I_S = 3 \times 10^{-14}$ A. Neglect base currents.

Solution: The reference current, from Example 13.1, is $I_{REF} = 0.72$ mA. Current I_{C13A} is then

$$I_{C13A} = (0.25)I_{REF} = (0.25)(0.72) = 0.18\,\text{mA} \cong I_{Bias}$$

If we assume $V_{BE19} = 0.6$ V, then the current in R_{10} is

$$I_{R10} = \frac{V_{BE19}}{R_{10}} = \frac{0.6}{50} = 0.012\,\text{mA}$$

The current in Q_{19} is

$$I_{C19} \cong I_{E19} = I_{C13A} - I_{R10} = 0.18 - 0.012 = 0.168\,\text{mA}$$

For this value of collector current, the B–E voltage of Q_{19} is

$$V_{BE19} = V_T \ln\left(\frac{I_{C19}}{I_S}\right) = (0.026)\ln\left(\frac{0.168 \times 10^{-3}}{10^{-14}}\right) = 0.612\,\text{V}$$

which is close to the assumed value of 0.6 V. Assuming $\beta_n = 200$ for the npn devices, the base current in Q_{19} is

$$I_{B19} = \frac{I_{C19}}{\beta_n} = \frac{169\,\mu\text{A}}{200} \cong 0.8\,\mu\text{A}$$

The current in Q_{18} is now

$$I_{C18} \cong I_{E18} = I_{R10} + I_{B19} = 12 + 0.8 = 12.8\,\mu\text{A}$$

The B E voltage of Q_{18} is therefore

$$V_{BE18} = V_T \ln\left(\frac{I_{C18}}{I_S}\right) = (0.026)\ln\left(\frac{12.8 \times 10^{-6}}{10^{-14}}\right) = 0.545\,\text{V}$$

The voltage difference V_{BB} is thus

$$V_{BB} = V_{BE18} + V_{BE19} = 0.545 + 0.612 = 1.157\,\text{V}$$

Since the output transistors Q_{14} and Q_{20} are identical, one-half of V_{BB} is across each B–E junction. The quiescent currents in Q_{14} and Q_{20} are

$$I_{C14} = I_{C20} = I_S e^{(V_{BB}/2)/V_T} = 3 \times 10^{-14} e^{(1.157/2)/0.026}$$

or

$$I_{C14} = I_{C20} = 138\,\mu\text{A}$$

Comment: Using the piecewise linear approximation of 0.6 V for the B–E junction voltage does not allow us to determine the quiescent currents in Q_{14} and Q_{20}. For a more accurate analysis, the exponential relationship must be used, since the base-emitter areas of the output transistors are larger than those of the other transistors, and because the output transistors are biased at a low quiescent current.

Test Your Understanding

13.7 In Figure 13.8, replace the Q_{18}, Q_{19}, and R_{10} combination by two series diodes with $I_S = 10^{-14}$ A. Assume that I_{C13A} is the same as previously determined, and let $I_S = 3 \times 10^{-14}$ A for Q_{14} and Q_{20}. Calculate V_{BB}, I_{C14}, and I_{C20}. (Ans. $V_{BB} = 1.228$ V, $I_{C14} = I_{C20} = 0.541$ mA)

As the input signal v_I increases, the base voltage of Q_{14} increases since the V_{BB} voltage remains almost constant. The output voltage increases at approximately the same rate as the input signal. As v_I decreases, the base voltage of Q_{20} decreases, and the output voltage also decreases, again at approximately the same rate as the input signal. The small-signal voltage gain of the output stage is essentially unity.

Short-Circuit Protection Circuitry

The output stage includes a number of transistors that are off during the normal operation of the amplifier. If the output terminal is at a positive voltage because of an applied input signal, and if the terminal is inadvertently shorted to ground potential, a large current will be induced in output transistor Q_{14}. A large current can produce sufficient heating to cause transistor burnout.

The complete output stage of the 741, including the **short-circuit protection devices**, is shown in Figure 13.9. Resistor R_6 and transistor Q_{15} limit the current in Q_{14} in the event of a short circuit. If the current in Q_{14} reaches 20 mA, the voltage drop across R_6 is 540 mV, which is sufficient to bias Q_{15} in the conducting stage. As Q_{15} turns on, excess base current into Q_{14} is shunted through the collector of Q_{15}. The base current into Q_{14} is then limited to a maximum value, which limits the collector current.

The maximum current in Q_{20} is limited by components R_7, Q_{21}, and Q_{24}, in much the same way as just discussed. A large output current will result in a voltage drop across R_7, which will be sufficient to bias Q_{21} in its conducting state. Transistors Q_{21} and Q_{24} will shunt excessive output current away from Q_{20}, to protect this output transistor.

13.2.3 Small-Signal Analysis

We can analyze the small-signal voltage gain of the 741 op-amp by dividing it into its basic circuits and using results previously obtained.

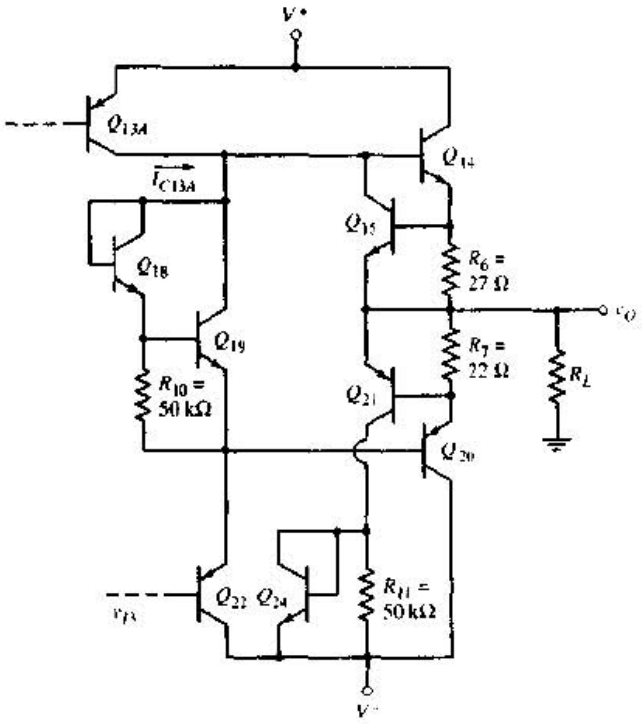


Figure 13.9 Output stage, 741 op-amp with short-circuit protection devices

Input Stage

Figure 13.10 shows the ac equivalent circuit of the input stage with a differential voltage v_d applied between the input terminals. The constant-current biasing at the base of Q_3 and Q_4 means that the effective impedance connected to the base terminal of Q_3 and Q_4 is ideally infinite, or an open circuit. Resistance R_{ac1} is the effective resistance of the active load and R_{i2} is the input resistance of the gain stage.

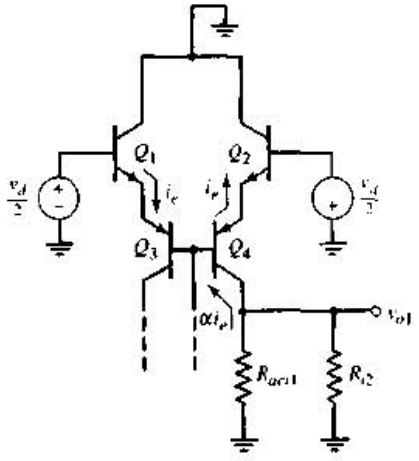


Figure 13.10 The ac equivalent circuit, input stage of 741 op-amp

From the results in Chapter 11, the small-signal differential voltage gain can be written as

$$A_d = \frac{v_{o1}}{v_d} = -g_m(r_{o4} \| R_{act1} \| R_{i2}) = -\left(\frac{I_{CQ}}{V_T}\right)(r_{o4} \| R_{act1} \| R_{i2}) \tag{13.13}$$

where I_{CQ} is the quiescent collector current in each of the transistors Q_1 through Q_4, and r_{o4} is the small-signal output resistance looking into the collector of Q_4. Using r_{o4} as the resistance looking into the collector of Q_4 neglects the effective resistance in the emitter of Q_4. This effective resistance is simply the resistance looking into the emitter of Q_2, which is normally very small. The minus sign in the voltage gain expression results from the applied signal voltage polarity and resulting current directions.

The effective resistance of the active load is given by

$$R_{act1} = r_{o6}[1 + g_{m6}(R_2 \| r_{\pi 6})] \tag{13.14}$$

as determined in Chapter 10 for the output resistance of a Widlar current source. From Figure 13.7, the input resistance of the gain stage is

$$R_{i2} = r_{\pi 16} + (1 + \beta_n)R_E' \tag{13.15}$$

where R_E' is the effective resistance in the emitter of Q_{16}, as given by

$$R_E' = R_9 \| [r_{\pi 17} + (1 + \beta_n)R_8] \tag{13.16}$$

Example 13.4 **Objective:** Determine the small-signal differential voltage gain of the 741 op-amp input stage.

Assume npn transistor gains of $\beta_n = 200$ and Early voltages of $V_A = 50\,\text{V}$.

Solution: The quiescent collector currents were determined previously in this chapter. The input resistance to the gain stage is found from Equations (13.15) and (13.16), as follows:

$$r_{\pi 17} = \frac{\beta_n V_T}{I_{C17}} = \frac{(200)(0.026)}{0.54} = 9.63\,\text{k}\Omega$$

Therefore,

$$R_E' = R_9 \| [r_{\pi 17} + (1 + \beta_n)R_8] = 50 \| [9.63 + (201)(0.1)] = 18.6\,\text{k}\Omega$$

Also,

$$r_{\pi 16} = \frac{\beta_n V_T}{I_{C16}} = \frac{(200)(0.026)}{0.0158} = 329\,\text{k}\Omega$$

Consequently,

$$R_{i2} = r_{\pi 16} + (1 + \beta_n)R_E' = 329 + (201)(18.6) \Rightarrow 4.07\,\text{M}\Omega$$

The resistance of the active load is determined from Equation (13.14). We find

$$r_{\pi 6} = \frac{\beta_n V_T}{I_{C6}} = \frac{(200)(0.026)}{0.0095} = 547\,\text{k}\Omega$$

$$g_{m6} = \frac{I_{C6}}{V_T} = \frac{0.0095}{0.026} = 0.365\,\text{mA/V}$$

and

$$r_{o6} = \frac{V_A}{I_{C6}} = \frac{50}{0.0095} \Rightarrow 5.26\,\text{M}\Omega$$

Then,

$$R_{ac1} = r_{o6}[1 + g_{m6}(R_2 \| r_{\pi 6})] = 5.26[1 + (0.365)(1 \| 547)] = 7.18\,\text{M}\Omega$$

Resistance r_{o4} is

$$r_{o4} = \frac{V_A}{I_{C4}} = \frac{(50)}{(0.0095)} \Rightarrow 5.26\,\text{M}\Omega$$

Finally, from Equation (13.13), the small-signal differential voltage gain is

$$A_d = -\left(\frac{I_{CQ}}{V_T}\right)(r_{o4} \| R_{ac1} \| R_{i2}) = -\left(\frac{9.5}{0.026}\right)(5.26 \| 7.18 \| 4.07)$$

or

$$A_d = -636$$

Comment: The relatively large gain results from the use of an active load and the fact that the gain stage does not drastically load the input stage.

Gain Stage

Figure 13.11 shows the ac equivalent circuit of the gain stage. Resistance R_{ac2} is the effective resistance of the active load and R_{i3} is the input resistance of the output stage.

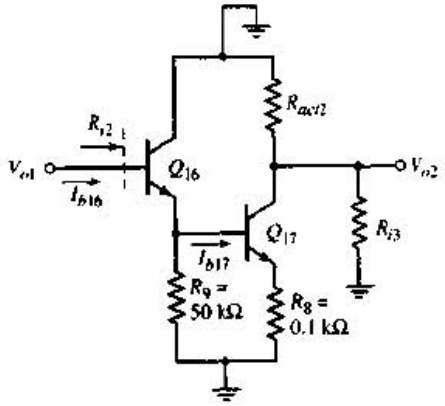


Figure 13.11 The ac equivalent circuit, gain stage of 741 op-amp

We develop the small-signal voltage gain using Figure 13.11 directly. The input base current to Q_{16} is

$$i_{b16} = \frac{v_{o1}}{R_{i2}} \tag{13.17}$$

where R_{i2} is the input resistance to the gain stage. The base current into Q_{17} is

$$i_{b17} = \frac{R_9}{R_9 + [r_{\pi 17} + (1 + \beta_n)R_8]} \times i_{c16} \tag{13.18}$$

where i_{e16} is the emitter current from Q_{16}. The output voltage is

$$v_{o2} = -i_{c17}(R_{ac2} \| R_{i3} \| R_{o17}) \tag{13.19}$$

where i_{c17} is the ac collector current in Q_{17} and R_{o17} is the output impedance looking into the collector of Q_{17}. Combining Equations (13.17), (13.18), and (13.19), we get the following expression for the small-signal voltage gain:

$$A_{v2} = \frac{v_{o2}}{v_{o1}} = \frac{-\beta_n(1+\beta_n)R_9(R_{ac2} \| R_{i3} \| R_{o17})}{R_{i2}[R_9 + [r_{\pi 17} + (1+\beta_n)R_8]]} \tag{13.20}$$

The effective resistance of the active load is the resistance looking into the collector of Q_{13B}, or

$$R_{ac2} = r_{o13B} = \frac{V_A}{I_{C13B}} \tag{13.21}$$

The input resistance of the output stage can be determined from the ac equivalent circuit in Figure 13.12. In this figure, we assume that the pnp output transistor Q_{20} is active and the npn output transistor Q_{14} is cut off. A load resistor R_L is also included. Transistor Q_{22} operates as an emitter follower, which means that the input resistance is

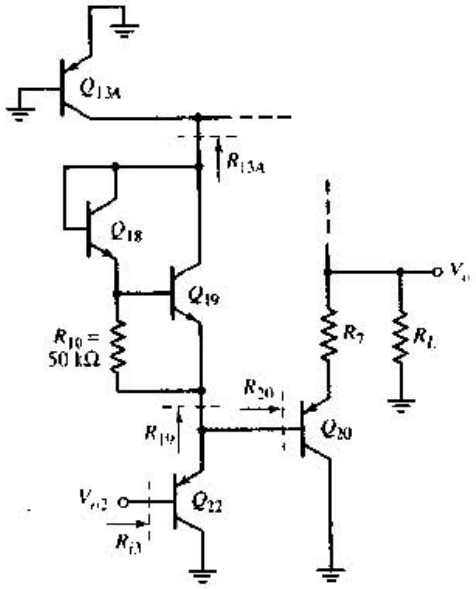


Figure 13.12 The ac equivalent circuit, 741 op-amp output stage, for calculating input resistance

$$R_{i3} = r_{\pi 22} + (1+\beta_f)[R_{19} \| R_{20}] \tag{13.22}$$

Resistance R_{19} is the series combination of the resistance looking into the emitters of Q_{19} and Q_{18}, and the resistance looking into the collector of Q_{13A}. The effective resistance of the combination of Q_{18} and Q_{19} is small compared to R_{13A}; therefore,

$$R_{19} \cong R_{13A} = r_{o13A} = \frac{V_A}{I_{C13A}} \tag{13.23}$$

The output transistor Q_{20} is also an emitter follower; therefore,

$$R_{20} = r_{\pi 20} + (1 + \beta_p)R_L \tag{13.24}$$

where the load resistance R_L is assumed to be much larger than R_7.

Example 13.5 **Objective:** Determine the small-signal voltage gain of the second stage of the 741 op-amp.

Assume the current gains of the pnp transistors are $\beta_p = 50$ and the gains of the npn transistors are $\beta_n = 200$. Also assume the Early voltage is 50 V for all transistors and the load resistance connected to the output is $R_L = 2\,\text{k}\Omega$. The dc quiescent currents were determined previously.

Solution: First, we calculate the various resistances. To begin,

$$r_{\pi 20} = \frac{\beta_p V_T}{I_{C20}} = \frac{(50)(0.026)}{0.138} = 9.42\,\text{k}\Omega$$

which means that

$$R_{20} = r_{\pi 20} + (1 + \beta_p)R_L = 9.42 + (51)(2) \cong 111\,\text{k}\Omega$$

Also,

$$R_{19} = r_{o13A} = \frac{V_A}{I_{C13A}} = \frac{50}{0.18} = 278\,\text{k}\Omega$$

and

$$r_{\pi 22} = \frac{\beta_n V_T}{I_{C13A}} = \frac{(50)(0.026)}{0.18} = 7.22\,\text{k}\Omega$$

The input resistance to the output stage is therefore

$$R_{i3} = r_{\pi 22} + (1 + \beta_p)[R_{19} \| R_{20}] = 7.22 + (51)[278 \| 111] \Rightarrow 4.05\,\text{M}\Omega$$

The effective resistance of the active load is

$$R_{act2} = \frac{V_A}{I_{C13B}} = \frac{50}{0.54} = 92.6\,\text{k}\Omega$$

and the output resistance R_{o17} is

$$R_{o17} \cong \frac{V_A}{I_{C17}} = \frac{50}{0.54} = 92.6\,\text{k}\Omega$$

This calculation neglects the very small value of R_8 in the emitter.

From Equation (13.20), the small-signal voltage gain is as follows (all resistances are given in kilohms):

$$A_{v2} = \frac{-\beta_n(1 + \beta_n)R_9(R_{act2} \| R_{i3} \| R_{o17})}{R_{i2}\{R_9 + [r_{\pi 17} + (1 + \beta_n)R_8]\}} = \frac{-(200)(201)(50)(92.6 \| 4050 \| 92.6)}{4070\{50 + [9.63 + (201)(0.1)]\}}$$

or

$$A_{v2} = -285$$

Comment: The voltage gain of the second stage is fairly large, again because an active load is used and because there is no severe loading effect from the output stage.

Overall Gain

In calculating the voltage gain of each stage, we took the loading effect of the following stage into account. Therefore, the overall voltage gain is the product of the individual gain factors, or

$$A_v = A_d A_{v2} A_{v3} \tag{13.25}$$

where A_{v3} is the voltage gain of the output stage. If we assume that $A_{v3} \approx 1$, as previously discussed, then the overall gain of the 741 op-amp is

$$A_v = A_d A_{v2} A_{v3} = (-636)(-285)(1) = 181{,}260 \tag{13.26}$$

Typical voltage gain values for the 741 op-amp are in the range of 200,000. The value determined in our calculations illustrates the magnitude of voltage gains that can be obtained in op-amp circuits.

Output Resistance

The output resistance can be determined by using the ac equivalent circuit in Figure 13.13. In this case, we assume the output transistor Q_{20} is conducting and Q_{14} is cut off. The same basic result is obtained if Q_{14} is conducting and Q_{20} is cut off. We again rely on results obtained previously for output resistances of basic amplifier stages.

The output resistance is

$$R_o = R_7 + R_{e20} \tag{13.27}$$

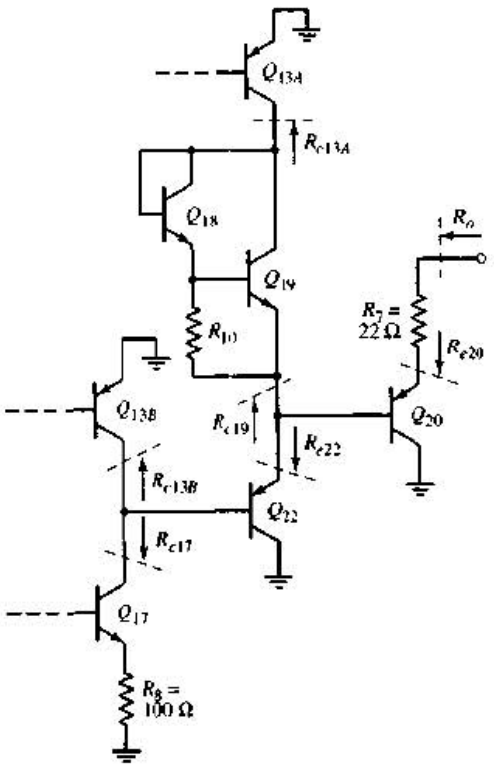


Figure 13.13 The ac equivalent circuit, 741 op-amp output stage, for calculating output resistance

where

$$R_{e20} = \frac{r_{\pi 20} + R_{e22} \| R_{c19}}{(1 + \beta_p)} \tag{13.28}$$

Previously we argued that the series resistance due to Q_{18} and Q_{19} is small compared to R_{c13A}, so that $R_{c19} \cong R_{c13A}$. We also have

$$R_{e22} = \frac{r_{\pi 22} + R_{c17} \| R_{c13B}}{(1 + \beta_p)} \tag{13.29}$$

where

$$R_{c13B} = r_{o13B}$$

and

$$R_{c17} = r_{o17}[1 + g_{m17}(R_8 \| r_{\pi 17})]$$

The output resistance of the op-amp is then found by combining all the resistance terms.

Example 13.6 **Objective:** Calculate the output resistance of the 741 op-amp.

Consider the output stage configuration in Figure 13.13. Assume the output current is $I_{c20} = 2\,\text{mA}$ and all other bias currents are as previously determined.

Solution: Using $\beta_n = 200$, $\beta_p = 50$, and $V_A = 50\,\text{V}$, we find the following:

$$r_{\pi 17} = 9.63\,\text{k}\Omega \qquad r_{\pi 22} = 7.22\,\text{k}\Omega \qquad r_{\pi 20} = 0.26\,\text{k}\Omega$$
$$g_{m17} = 20.8\,\text{mA/V} \qquad r_{o17} = 92.6\,\text{k}\Omega \qquad r_{o13B} = 92.6\,\text{k}\Omega$$

Then,

$$R_{c17} = r_{o17}[1 + g_{m17}(R_8 \| r_{\pi 17})] = 92.6[1 + (20.8)(0.1 \| 9.63)] = 283\,\text{k}\Omega$$

and

$$R_{e22} = \frac{r_{\pi 22} + R_{c17} \| R_{c13B}}{(1 + \beta_p)} = \frac{7.22 + 283 \| 92.6}{51} = 1.51\,\text{k}\Omega$$

Also,

$$R_{c19} \cong R_{c13A} = r_{o13A} = \frac{V_A}{I_{C13A}} = \frac{50}{0.18} = 278\,\text{k}\Omega$$

Therefore

$$R_{e20} = \frac{r_{\pi 20} + R_{e22} \| R_{c19}}{(1 + \beta_p)} = \frac{0.26 + 1.51 \| 278}{51} = 0.0345\,\text{k}\Omega \Rightarrow 34.5\,\Omega$$

Consequently, the output resistance is

$$R_o = R_7 + R_{e20} = 22 + 34.5 = 56.5\,\Omega$$

Comment: We showed previously that the output resistance of an emitter-follower circuit is low. For comparison, typical output resistance values for the 741 op-amp are 75 Ω. This correlates well with our analysis.

13.2.4 Frequency Response

The 741 op-amp is internally compensated by the Miller compensation technique to introduce a dominant low-frequency pole. From Miller's theorem, the effective input capacitance of the second gain stage is

$$C_i = C_1(1 + |A_{v2}|) \tag{13.30}$$

The dominant low-frequency pole is

$$f_{PD} = \frac{1}{2\pi R_{eq} C_i} \tag{13.31}$$

where R_{eq} is the equivalent resistance between the second-stage input node and ground, and is

$$R_{eq} = R_{o1} \| R_{i2} \tag{13.32}$$

Here R_{i2} is the input resistance of the gain stage and R_{o1} is the output resistance of the diff-amp stage. From Figure 13.10, we see that

$$R_{o1} = R_{ac1} \| r_{o4} \tag{13.33}$$

Example 13.7 **Objective:** Determine the dominant-pole frequency of the 741 op-amp.

Use appropriate results from previous calculations.

Solution: Previously, we determined that $|A_{v2}| = 285$, which means that the effective input capacitance is

$$C_i = C_1(1 + |A_{v2}|) = (30)(1 + 285) = 8580\,\text{pF}$$

The gain stage input resistance was found to be $R_{i2} = 4.07\,\text{M}\Omega$. We find

$$R_{o1} = R_{ac1} \| r_{o4} = 7.18 \| 5.26 = 3.04\,\text{M}\Omega$$

The equivalent resistance is then

$$R_{eq} = R_{o1} \| R_{i2} = 3.04 \| 4.07 = 1.74\,\text{M}\Omega$$

Finally, the dominant-pole frequency is

$$f_{PD} = \frac{1}{2\pi R_{eq} C_i} = \frac{1}{2\pi(1.74 \times 10^6)(8580 \times 10^{-12})} = 10.7\,\text{Hz}$$

Comment: The very large equivalent input capacitance C_i justifies neglecting any other capacitance effects at the gain stage input.

If all other poles of the op-amp circuit are at very high frequencies, then the unity-gain bandwidth is

$$f_T = A_o f_{PD} \tag{13.34}$$

Using our results, we find that

$$f_T = (181{,}260)(10.7) \cong 1.9\,\text{MHz} \tag{13.35}$$

A typical unity-gain bandwidth value for the 741 op-amp is 1 MHz. With all the approximations and assumptions, such as the value of reverse saturation

current and Early voltage, used in the calculations, a factor of two between the actual and predicted cutoff frequency is not significant.

If the frequencies of the other poles of the 741 op-amp are greater than 1.9 MHz, the phase margin is 90 degrees. This phase margin ensures that any closed-loop amplifier circuit using the 741 op-amp will be stable for any feedback transfer function.

Problem-Solving Technique: Operational Amplifier Circuits

1. *DC analysis.* The bias portion of the op-amp circuit must be identified. A reference current must be determined and then the bias currents in the individual building blocks of the overall circuit can be determined.
2. *AC analysis.* The small-signal properties of the building blocks of the overall circuit can be analyzed individually, provided that the loading effects of follow-on stages are taken into account.

Test Your Understanding

13.8 The power supply voltages for the 741 op-amp in Figure 13.3 are $V^+ = 10\,\text{V}$ and $V^- = -10\,\text{V}$. Neglect base currents and assume $V_{BE}(\text{npn}) = V_{EB}(\text{pnp}) = 0.6\,\text{V}$. Calculate the bias currents I_{REF}, I_{C10}, I_{C6}, I_{C13B}, and I_{C13A}. (Ans. $I_{\text{REF}} = 0.47\,\text{mA}$, $I_{C10} = 17.2\,\mu\text{A}$, $I_{C6} = 8.6\,\mu\text{A}$, $I_{C13B} = 0.353\,\text{mA}$, $I_{C13A} = 0.118\,\text{mA}$)

***13.9** In the 741 op-amp output stage in Figure 13.3, the combination of Q_{18}, Q_{19}, and R_{10} is replaced by two series diodes with $I_S = 10^{-14}\,\text{A}$. The transistor parameters are: $\beta_n = 200$, $\beta_p = 50$, and $V_A = 50\,\text{V}$. Assume the same dc bias currents calculated previously. Calculate the output resistance, assuming Q_{14} is conducting, producing a load current of 5 mA. (Ans. 41 Ω)

13.3 CMOS OPERATIONAL AMPLIFIER CIRCUITS

The 741 bipolar op-amp is a general-purpose op-amp capable of sourcing and sinking reasonably large load currents. The output stage is an emitter follower capable of supplying the necessary load current, with a low output resistance to minimize loading effects.

In contrast, most CMOS op-amps are designed for specific on-chip applications and are only required to drive capacitive loads of a few picofarads. Most CMOS op-amps therefore do not need a low-resistance output stage, and, if the op-amp inputs are not connected directly to the IC external terminals, they also do not need electrostatic input protection devices.

In this section, we will initially consider a simple CMOS design to begin to understand the basic concepts of a CMOS op-amp. We will then consider a more sophisticated CMOS op-amp design, called a folded cascode op-amp, and then analyze a current-mirror CMOS op-amp circuit. In each case we will do a dc analysis/design and then a small-signal analysis/design.

13.3.1 MC14573 CMOS Operational Amplifier Circuit

Circuit Description

An example of an all-CMOS op-amp is the MC14573, for which a simplified circuit diagram is shown in Figure 13.14. The p-channel transistors M_1 and M_2 form the input differential pair, and the n-channel transistors M_3 and M_4 form the active load. The diff-amp input stage is biased by the current mirror M_5 and M_6, in which the reference current is determined by an external resistor R_{set}.

The second stage, which is also the output stage, consists of the common-source-connected transistor M_7. Transistor M_8 provides the bias current for M_7 and acts as the active load. An internal compensation capacitor C_1 is included to provide stability.

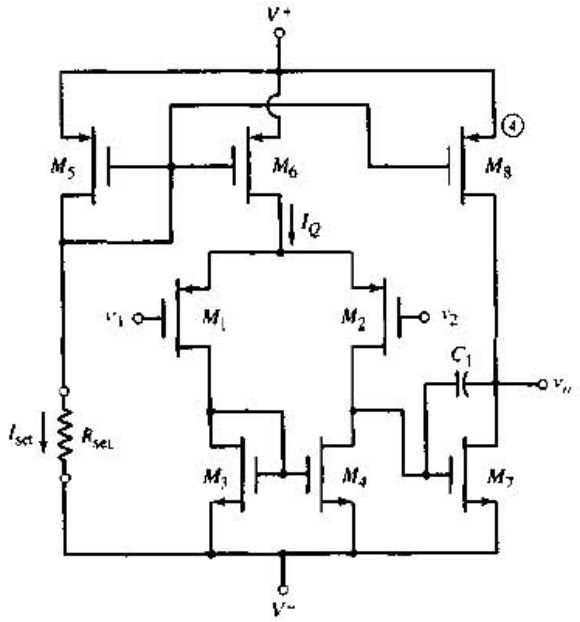


Figure 13.14 MC14573 CMOS op-amp equivalent circuit

DC Analysis

Assuming transistors M_5 and M_6 are matched, the reference and input-stage bias currents are given by

$$I_{set} = I_Q = \frac{V^+ - V^- - V_{SG5}}{R_{set}} \tag{13.36}$$

The reference current and source-to-gate voltage are also related by

$$I_{set} = K_{p5}(V_{SG5} + V_{TP})^2 \tag{13.37}$$

where V_{TP} and K_{p5} are the threshold voltage and conduction parameter of the p-channel transistor M_5.

Example 13.8 **Objective:** Determine the dc bias currents in the MC14573 op-amp.

Assume transistor parameters of $|V_T| = 0.5\,\text{V}$ (all transistors), $(\frac{1}{2})\mu_n C_{ox} = 20\,\mu\text{A/V}^2$, $(\frac{1}{2})\mu_p C_{ox} = 10\,\mu\text{A/V}^2$, and circuit parameters of $V^+ = 5\,\text{V}$, $V^- = -5\,\text{V}$, and $R_{set} = 225\,\text{k}\Omega$. Assume transistor width-to-length ratios of 6.25 for M_3 and M_4, and 12.5 for all other transistors.

Solution: For transistors M_5 and M_6, the conduction parameters are:

$$K_p = \left(\frac{W}{L}\right)\left(\frac{1}{2}\mu_p C_{ox}\right) = (12.5)(10) = 125\,\mu\text{A/V}^2$$

Combining Equations (13.36) and (13.37) yields the source-to-gate voltage of M_5:

$$K_p(V_{SG5} + V_{TP})^2 = \frac{V^+ - V^- - V_{SG5}}{R_{set}}$$

or

$$0.125(V_{SG5} - 0.5)^2 = \frac{5 + 5 - V_{SG5}}{225}$$

which yields

$$V_{SG5} = 1.06\,\text{V}$$

From Equation (13.36), we have

$$I_{REF} = I_Q = \frac{10 - 1.06}{225} \Rightarrow 39.7\,\mu\text{A}$$

The quiescent drain currents in M_7 and M_8 are then also $39.7\,\mu\text{A}$, and the currents in M_1 through M_4 are $19.9\,\mu\text{A}$.

Comment: The quiescent bias currents can be changed easily by changing the external resistor R_{set}. Transistors M_5, M_6, and M_8 are identical, so the currents in these three devices are equal since the source-to-gate voltages are the same. The width-to-length ratio of M_7 is twice that of M_3 and M_4, which means the current in M_7 is twice that in M_3 and M_4. However, this is consistent with the current-source transistor currents.

Test Your Understanding

***13.10** Using the parameters given in Example 13.8, determine the input common-mode voltage range for the MC14573 op-amp. (Ans. $-4.60 \le v_{in}(\text{cm}) \le 3.54\,\text{V}$)

13.11 Using the parameters given in Example 13.8, determine the maximum and minimum output voltage in the MC14573 circuit such that the op-amp remains biased in its linear region. (Ans. $-4.44 \le v_O \le +4.44\,\text{V}$)

Small-Signal Analysis

The small-signal differential voltage gain of the input stage can be written as

$$A_d = \sqrt{2K_{p1}I_Q}\,(r_{o2} \| r_{o4}) \tag{13.38}$$

where r_{o2} and r_{o4} are the output resistances of M_2 and M_4, respectively. The input impedance to the second stage is essentially infinite; therefore, there is no loading effect due to the second stage. If we assume that the parameter λ is the same for all transistors, then

$$r_{o2} = r_{o4} = \frac{1}{\lambda I_D} \tag{13.39}$$

where I_D, which is the quiescent drain current in M_2 and M_4, is $I_D = I_Q/2$.

The gain of the second stage is

$$A_{v2} = g_{m7}(r_{o7} \| r_{o8}) \tag{13.40}$$

where

$$g_{m7} = 2\sqrt{K_{n7} I_{D7}}$$

and

$$r_{o7} = r_{o8} = 1/\lambda I_{D7}$$

Equation (13.40) implies that there is no loading effect due to an external load connected at the output.

Example 13.9 **Objective:** Determine the small-signal voltage gains of the input and second stages, and the overall voltage gain, of the MC14573 op-amp.

Assume the same transistor and circuit parameters as in Example 13.8. Let $\lambda = 0.02\,\text{V}^{-1}$ for all transistors.

Solution: The conduction parameters of M_1 and M_2 are

$$K_{p1} = K_{p2} = \left(\frac{W}{L}\right)\left(\frac{1}{2}\mu_p C_{ox}\right) = (12.5)(10) = 125\,\mu\text{A/V}^2$$

and the output resistances are

$$r_{o2} = r_{o4} = \frac{1}{\lambda I_D} = \frac{1}{(0.02)(0.0199)} \Rightarrow 2.51\,\text{M}\Omega$$

From Equation (13.38), the gain of the input stage is then

$$A_d = \sqrt{2K_{p1} I_Q}\,(r_{o2} \| r_{o4}) = \sqrt{2(0.125)(0.0397)}(2510 \| 2510)$$

or

$$A_d = 125$$

The transconductance of M_7 is

$$g_{m7} = 2\sqrt{K_{n7} I_{D7}} = 2\sqrt{(0.250)(0.0397)} = 0.199\,\text{mA/V}$$

and the output resistances of M_7 and M_8 are

$$r_{o7} = r_{o8} = \frac{1}{\lambda I_{D7}} = \frac{1}{(0.02)(0.0397)} \Rightarrow 1.26\,\text{M}\Omega$$

From Equation (13.40), the gain of the second stage is then

$$A_{v2} = g_{m7}(r_{o7} \| r_{o8}) = (0.199)(1260 \| 1260) = 125$$

Finally, the overall voltage gain of the op-amp is

$$A_v = A_d A_{v2} = (125)(125) = 15{,}625$$

Comment: The calculated overall voltage gain is 84 dB, which correlates fairly well with typical values of 90 dB, as listed in the data sheet for the MC14573 op-amp. The open-loop gain of a CMOS op-amp is generally less than that of a bipolar op-amp, but the use of active loads provides acceptable results.

Test Your Understanding

***13.12** Consider the MC14573 op-amp in Figure 13.14. Assume the same circuit and transistor parameters as given in Examples 13.8 and 13.9, except change R_{set} to 100 kΩ. (a) Calculate all dc bias currents. (b) Determine the overall voltage gain of the op-amp. (Ans. (a) $I_{set} = I_Q = I_{D8} = I_{D7} = 86.7\,\mu A$, $I_{D1} = I_{D2} = I_{D3} = I_{D4} = I_Q/2 = 43.35\,\mu A$ (b) 7189)

13.3.2 Folded Cascode CMOS Operational Amplifier Circuit

As we have mentioned previously, the voltage gain of an amplifier can be increased by using a cascode configuration. In its simplest form, the conventional cascode configuration consists of two transistors in series, as shown in Figure 13.15(a). The transistor M_1 is the common-source amplifying device whose current is determined by the input voltage. This current is the input signal to M_2, which is connected in a common-gate configuration. The output is taken off the drain of the cascode transistor. The circuit in Figure 13.15(b) has a slightly different configuration. The dc current I_1 in M_1 is determined by the input voltage. The dc current in M_2 is the difference between the bias current I_Q and I_1.

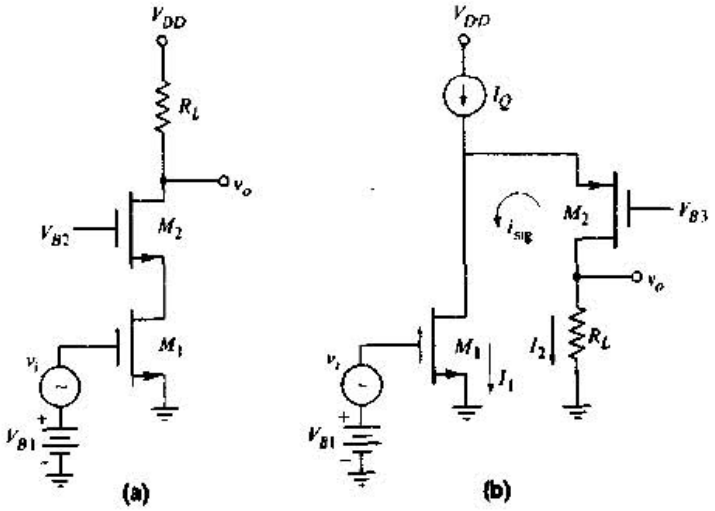


Figure 13.15 (a) Classical cascode stage; (b) folded-cascode stage

The ac current in the conventional cascode circuit of Figure 13.15(a) is through both transistors and the dc power supply. The ac current in the cascode circuit in Figure 13.15(b) is through both transistors and ground as

indicated in the figure. The ac current in M_2 of this circuit is equal in magnitude but in the opposite direction to M_1. Thus the current is said to be folded back and the circuit in Figure 13.15(b) is called a folded cascode circuit.

The folded cascode configuration can be applied to the diff-amp as shown in Figure 13.16. The transistors M_1 and M_2 are the differential pair, as usual, and transistors M_5 and M_6 are the cascode transistors. Transistors M_7–M_{10} form a modified Wilson current mirror acting as an active load. This configuration was discussed in Chapter 10. The biasing V_{B1} and V_{B2} must be provided by a separate network.

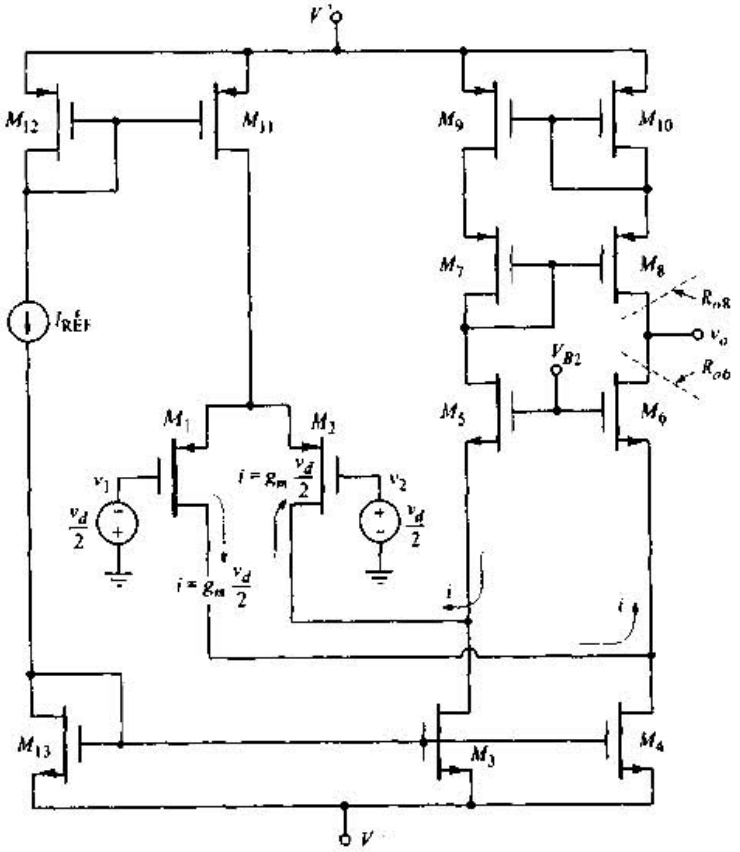


Figure 13.16 CMOS folded cascode amplifier

Assuming that transistors M_3, M_4, and M_{11}–M_{13} are all matched, then the dc currents in M_1 and M_2 are $I_{REF}/2$ and those in M_3 and M_4 are I_{REF}. This means that the dc currents in the cascode transistors M_5 and M_6 are $I_{REF}/2$.

If a differential-mode input voltage is applied, then ac currents are induced in the differential pair as shown in the figure. The ac current in M_1 flows through M_6 to the output. The ac current in M_2 flows through M_5 and is induced in M_8 by the current-mirror action of the active load. From previous work on diff-amps, the differential-mode voltage gain is

$$A_d = g_{m1}(R_{o6} \| R_{o8}) \tag{13.41}$$

where

$$R_{o8} = g_{m8}(r_{o8}r_{o10}) \qquad \textbf{(13.42(a))}$$

and

$$R_{o6} = g_{m6}(r_{o6})(r_{o4}\|r_{o1}) \qquad \textbf{(13.42(b))}$$

We may note that we are neglecting the body effect. Normally the substrates of all NMOS devices are tied to V^- and the substrates of all PMOS devices are tied to V^+.

Example 13.10 **Objective:** Determine the differential-mode voltage gain of the folded cascode diff-amp in Figure 13.16.

Assume circuit and transistor parameters: $I_{REF} = 100\,\mu A$, $k_n' = 80\,\mu A/V^2$, $k_p' = 40\,\mu A/V^2$, $(W/L) = 25$, and $\lambda_n = \lambda_p = 0.02\,V^{-1}$.

Solution: The transconductances are determined to be

$$g_{m1} = g_{m8} = 2\sqrt{\frac{k_p'}{2}\cdot\frac{W}{L}\cdot I_D} = 2\sqrt{\frac{40}{2}\cdot(25)(50)} = 316\,\mu A/V$$

and

$$g_{m6} = 2\sqrt{\frac{k_n'}{2}\cdot\frac{W}{L}\cdot I_D} = 2\sqrt{\frac{80}{2}\cdot(25)(50)} = 447\,\mu A/V$$

The transistor output resistances are found to be

$$r_{o1} = r_{o6} = r_{o8} = r_{o10} = \frac{1}{\lambda I_D} = \frac{1}{(0.02)(50)} = 1\,M\Omega$$

and

$$r_{o4} = \frac{1}{\lambda I_{D4}} = \frac{1}{(0.02)(100)} = 0.5\,M\Omega$$

The composite output resistances can be determined as

$$R_{o8} = g_{m8}(r_{o8}r_{o10}) = (316)(1)(1) = 316\,M\Omega$$

and

$$R_{o6} = g_{m6}(r_{o6})(r_{o4}\|r_{o1}) = (447)(1)(0.5\|1) = 149\,M\Omega$$

The differential-mode voltage gain is then

$$A_d = g_{m1}(R_{o6}\|R_{o8}) = (316)(149\|316) \cong 32{,}000$$

Comment: This example shows that very high differential-mode voltage gains can be achieved in a folded cascode CMOS circuit. In actual circuits, the output resistances may be limited by leakage currents so the very ideal values may not be realizable. However, substantially higher differential-mode voltage gains can be achieved in the folded cascode configuration than in the simpler diff-amp circuits.

Test Your Understanding

13.13 Assume the reference current in the folded cascode circuit shown in Figure 13.16 is $I_{REF} = 50\,\mu A$. Assume the transistor parameters are the same as given in Example 13.10. Determine the differential-mode voltage gain. (Ans. $\cong 64{,}000$)

13.3.3 CMOS Current-Mirror Operational Amplifier Circuit

Another CMOS op-amp circuit is shown in Figure 13.17. The differential pair is formed by M_1 and M_2. The induced ac currents from these transistors drive transistors M_3 and M_4, which are the inputs of two current mirrors with a current multiplication factor B. The current output of M_5 is then induced in M_8 by the current-mirror action of M_7 and M_8. The output signal currents then have a multiplication factor B. The differential-mode voltage gain is then given by

$$A_d = \frac{v_o}{v_d} = Bg_{m1}(r_{o6} \| r_{o8}) \tag{13.43}$$

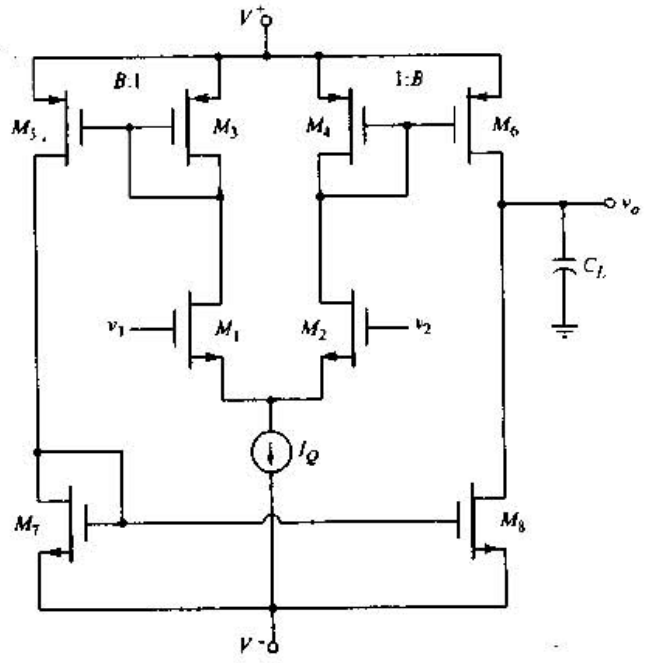


Figure 13.17 CMOS current-mirror op-amp

The factor of B in the gain expression of Equation (13.43) may be slightly misleading. Recall that the individual transistor output resistance is inversely proportional to the drain current. If the current in the output transistors increases by the factor B, then $R_o = r_{o6} \| r_{o8}$ decreases by the factor B so the differential-mode voltage gain remains unchanged.

The advantage of the current-mirror op-amp is an increase in the gain–bandwidth product. The dominant-pole frequency will be determined by the parameters at the output node. The dominant-pole frequency is given by

$$f_{pd} = \frac{1}{2\pi R_o(C_L + C_p)} \tag{13.44}$$

where R_o is the output resistance, C_L is the load capacitance, and C_p is the sum of all other capacitances at the output node. If R_o decreases by the factor B, then the dominant-pole frequency increases by the same factor B. The gain–bandwidth product is

$$\text{GBW} = A_d \cdot f_{pd} \tag{13.45}$$

Since A_d is now independent of B and f_{pd} increases by B, then the gain–bandwidth product increases by B.

Further analysis of this circuit shows that the phase margin decreases with increasing B. As a practical limit, the maximum value of B is limited to approximately 3.

Test Your Understanding

13.14 Consider the CMOS current-gain op-amp in Figure 13.17. Assume the bias current is $I_Q = 100\,\mu\text{A}$ and assume transistor parameters $k_n' = 80\,\mu\text{A/V}^2$, $k_p' = 40\,\mu\text{A/V}^2$, and $\lambda_n = \lambda_p = 0.02\,\text{V}^{-1}$. Assume the basic W/L ratio of the transistors is 20 and let $B = 3$. (a) Determine the small-signal voltage gain. (b) If the effective capacitance at the output node is $C_L + C_p = 2\,\text{pF}$, determine the dominant-pole frequency and the gain–bandwidth product. (Ans. (a) 200, (b) 477 kHz, 95 MHz)

13.3.4 CMOS Cascode Current-Mirror OP-Amp Circuit

As we have already seen, the differential-mode gain can be increased by adding cascode transistors in the output portion of the circuit. Figure 13.18 shows the same current-mirror configuration considered previously but with cascode transistors added to the output. Transistors M_9–M_{12} are the cascode transistors. The differential-mode voltage gain is given by

$$A_d = \frac{v_o}{v_d} = Bg_{m1}(R_{o10} \| R_{o12}) \tag{13.46}$$

where

$$R_{o10} = g_{m10}(r_{o10}r_{o6}) \tag{13.47}$$

and

$$R_{o12} = g_{m12}(r_{o12}r_{o8}) \tag{13.48}$$

The advantage of this circuit is the increased gain at low frequency. The gain–bandwidth product of this circuit is not changed from that of the simple current-mirror op-amp considered previously.

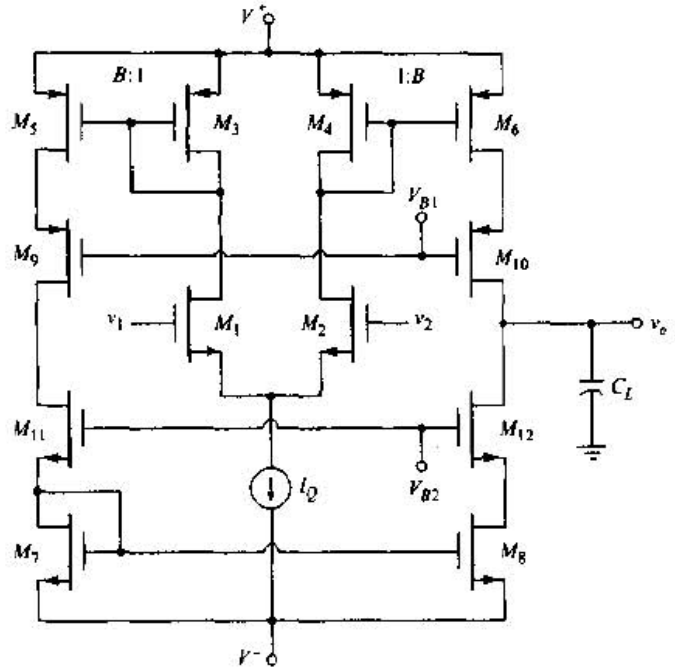


Figure 13.18 CMOS cascode current-mirror op-amp

Test Your Understanding

13.15 Consider the CMOS cascode current-mirror op-amp in Figure 13.18. Assume the bias current and transistor parameters are the same as in Exercise 13.14. Repeat parts (a) and (b) of Exercise 13.14 for this circuit. (Ans. (a) 38,171, (b) 2.50 kHz, 95.4 MHz)

13.4 BICMOS OPERATIONAL AMPLIFIER CIRCUITS

As discussed in Chapter 11, BiCMOS circuits combine the advantages of bipolar and MOSFET devices in the same circuit. One advantage of MOSFETs is the very high input impedance. Therefore, when MOSFETs form the input differential pair of an op-amp, the input bias currents are extremely small. However, the equivalent noise of the input stage may be greater than for an all-BJT op-amp.

In this section, we will examine two BiCMOS op-amp circuits. The first is a variation of the folded cascode configuration analyzed in the last section and the second is the CA3140 BiCMOS op-amp. Since we previously fully analyzed the folded cascode circuit, we will discuss, here, the advantages of using the BiCMOS technology. Many features of the CA3140 BiCMOS op-amp are similar to those of the 741. Therefore, we will not analyze this op-amp in as great a detail as we did the 741. Instead, we will concentrate on some of its unique features.

13.4.1 BiCMOS Folded Cascode Op-Amp

Figure 13.19 shows an example of a BiCMOS folded cascode op-amp. The cascode transistors, Q_5 and Q_6, are now bipolar devices, replacing n-channel MOSFETs. The small-signal voltage gain expression for this circuit is identical to that of the all-CMOS design. We have mentioned that the dominant-pole frequency is determined by the circuit parameters at the output node because of the very large output resistance. Nondominant-pole frequencies are then a function of the parameters at the other circuit nodes. In particular, one node of interest is at the drain of an input transistor and emitter of a cascode transistor. The nondominant-pole frequency can be written as

$$f_{3\text{-dB}} = \frac{g_{m6}}{2\pi C_{p6}} \tag{13.49}$$

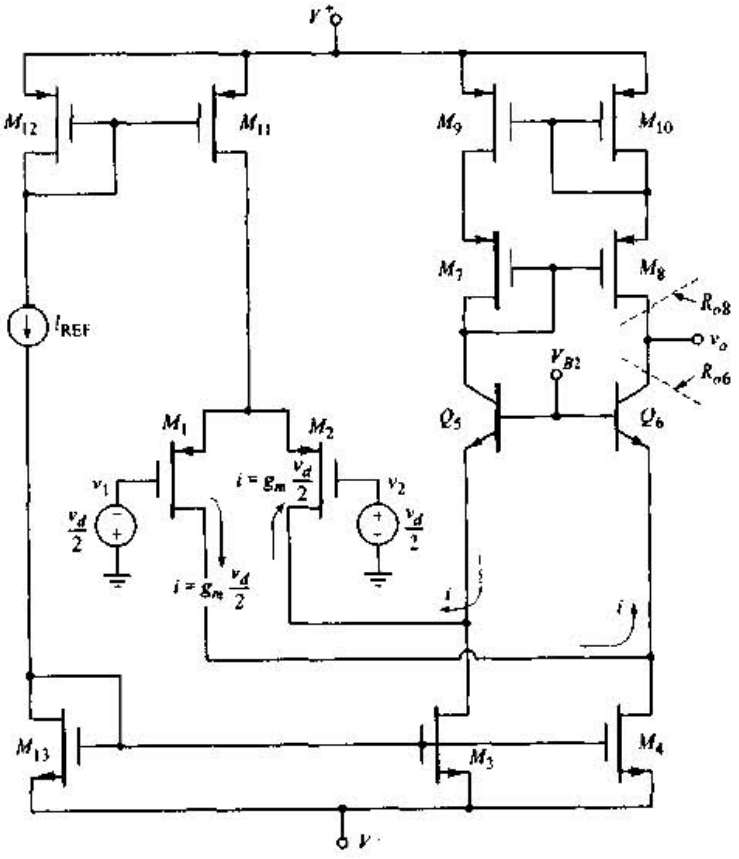


Figure 13.19 BiCMOS folded cascode amplifier

where g_{m6} is the transconductance of the cascode transistor Q_6 and C_{p6} is the effective capacitance at this node. Since the transconductance of a bipolar is usually greater than that of a MOSFET, this 3 dB frequency is larger for the BiCMOS circuit than for the all-CMOS design. This result means that the phase margin of the BiCMOS op-amp circuit is larger than that of the all-CMOS op-amp.

Test Your Understanding

13.16 Consider the BiCMOS folded cascode amplifier in Figure 13.19. Assume the circuit and MOS transistor parameters are the same as in Example 13.10. Assume BJT parameters of $\beta = 120$ and $V_A = 80$ V. (a) Determine the small-signal voltage gain. (b) If the effective capacitance at the output node is 2 pF, determine the dominant-pole frequency and the gain–bandwidth product. (Ans. (a) 76,343, (b) 329 Hz, 25.1 MHz)

13.4.2 CA3140 BiCMOS Circuit Description

Figure 13.20 shows the basic equivalent circuit of the CA3140 op-amp. Like the 741, this op-amp consists of three basic stages: the input differential stage, the gain stage, and the output stage. Also shown in the figure are: the bias circuit, which establishes the dc bias currents in the op-amp; and a section referred to as a dynamic current sink, which will be explained later. Typical supply voltages are $V^+ = 15$ V and $V^- = -15$ V.

Input Diff-Amp

The input differential pair consists of p-channel transistors M_9 and M_{10}, and transistors Q_{11} and Q_{12} form the active load for the diff-amp. A single-sided output at the collector of Q_{12} is the input signal to the following gain stage. Two offset null terminals are also shown, and will be discussed in the next chapter.

MOS transistors are very susceptible to damage from electrostatic charge. For example, electrostatic voltage can be inadvertently induced on the gate of a MOSFET during routine handling. These voltages may be great enough to induce breakdown in the gate oxide, destroying the device. Therefore, input protection against electrostatic damage is provided by the Zener diodes D_3, D_4, and D_5. If the gate voltage becomes large enough, these diodes will provide a discharge path for the electrostatic charge, thus protecting the gate oxide from breakdown.

The dc current biasing is initiated in the bias circuit. The elements labeled D_1 and D_2 are diode-connected transistors. Transistor Q_1 and diode D_1 are matched, which forces the currents in the two branches of the bias circuit to be equal. The current is determined from Q_7, R_1, and M_8. The combination of Q_6 and Q_7 makes the bias current essentially independent of the power supply voltages.

Gain Stage

The second stage consists of Q_{13} connected in a common-emitter configuration. The cascode configuration of transistors Q_3 and Q_4 provides the bias current for Q_{13}, in addition to acting as the active load. Since Q_3 and Q_4 are connected in a cascode configuration, the resistance looking into the collector of Q_4 is very high.

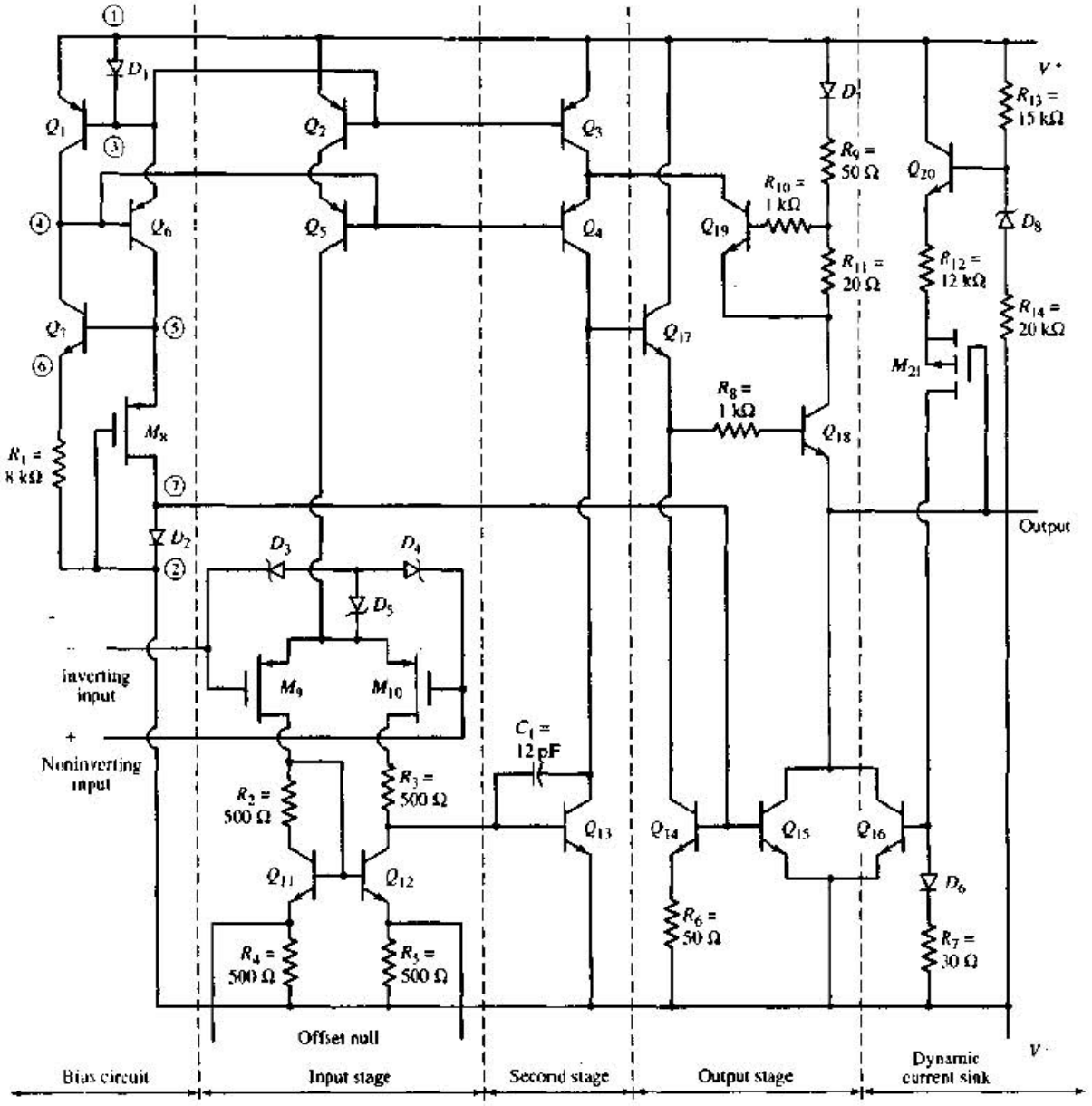


Figure 13.20 CA3140 BiCMOS op-amp equivalent circuit

Output Stage

The basic output stage consists of the npn transistors Q_{17} and Q_{18}. During the positive portion of the output voltage cycle, Q_{18} acts as an emitter follower, supplying a load current. During the negative portion of the output voltage cycle, Q_{16} sinks current from the load. As the output voltage decreases, the source-to-gate voltage on the p-channel M_{21} MOSFET increases, producing a larger current in D_6 and R_7 so that the base voltage on Q_{16} increases. The increase B-E voltage of Q_{16} allows increased load current sinking. Short-circuit protection is provided by the combination of R_{11} and Q_{19}. If a sufficiently large

voltage is developed across R_{11}, Q_{19} turns on and shunts excess base current away from Q_{17}.

An abbreviated data sheet for the CA3140 op-amp is in Table 13.2. As before, we will compare the results of our analysis to the values listed in the table.

Table 13.2 CA3140 BiCMOS data

Parameter	Minimum	Typical	Maximum	Units
Input bias current		10	50	pA
Open-loop gain	20,000	100,000		V/V
Unity-gain frequency		4.5		MHz

13.4.3 CA3140 DC Analysis

In this section, we will determine the dc bias currents in the CA3140 op-amp. As previously stated, we will concentrate on the features that are unique to the CA3140 compared to the 741.

The basic bias circuit is shown in Figure 13.21. The current mirror consisting of Q_1 and D_1 ensures that the two branch currents I_1 and I_2 are equal, since Q_1 and D_1 are matched. The p-channel MOSFET M_8 is to operate in the saturation region, so that we must have

$$V_{SD} > V_{SG} - |V_{TP}| \tag{13.50}$$

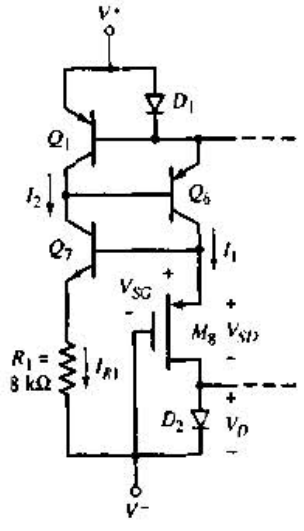


Figure 13.21 Bias circuit, CA3140 BiCMOS op-amp

From the figure, we see that

$$V_{SG} = V_{SD} + V_D \tag{13.51}$$

or

$$V_{SD} = V_{SG} - V_D \tag{13.52}$$

Combining Equations (13.52) and (13.50) yields

$$V_{SG} - V_D > V_{SG} - |V_{TP}| \tag{13.53}$$

which implies that $|V_{TP}| > V_D$. In other words, for M_8 to remain biased in the saturation region, the magnitude of the threshold voltage must be greater than the diode voltage.

From the left branch of the bias circuit, we see that the current can be written

$$I_2 \cong I_{R1} = \frac{V_{SG} - V_{BE7}}{R_1} \tag{13.54}$$

and from the right branch, we have

$$I_1 = K_p(V_{SG} - |V_{TP}|)^2 \tag{13.55}$$

Since $I_1 = I_2$, a simultaneous solution of Equations (13.54) and (13.55) determines the currents and voltages in this bias circuit.

Example 13.11 **Objective:** Determine the currents and voltages in the bias circuit of the CA3140 op-amp.

Consider the bias circuit in Figure 13.21, with parameters: $V^+ = 15\,\text{V}$, $V^- = -15\,\text{V}$, and $R_1 = 8\,\text{k}\Omega$. Assume transistor parameters of $V_{BE}(\text{npn}) = V_{EB}(\text{pnp}) = 0.6\,\text{V}$ for the bipolars, and $K_p = 0.2\,\text{mA/V}^2$ and $|V_{TP}| = 1.4\,\text{V}$ for the MOSFET M_8.

Solution: Set $I_1 = I_2$. Then, from Equations (13.54) and (13.55), we find

$$V_{SG} = 2.49\,\text{V} \quad \text{and} \quad I_1 = I_2 = 0.236\,\text{mA}$$

The voltage at the collector of Q_6 is

$$V_{C6} = V_{SG8} + V^- = 2.49 - 15 = -12.5\,\text{V}$$

and the voltage at the collector of Q_7 is

$$V_{C7} = V^+ - V_{EB1} - V_{EB6} = 15 - 0.6 - 0.6 = 13.8\,\text{V}$$

Therefore, the collector–base junctions of both Q_6 and Q_7 are reverse biased by $13.8 - (-12.5) = 26.3\,\text{V}$, and both Q_6 and Q_7 are biased in the active region.

Comment: The nominal bias current listed in Table 13.2 is $200\,\mu\text{A}$, which correlates well with our calculated value of $236\,\mu\text{A}$. As long as the B–C junctions of Q_6 and Q_7 remain reverse biased, the bias currents remain constant. This means that the bias current is independent of V^+ and V^- over a wide range of voltages.

The PSpice analysis, using $I_S = 2 \times 10^{-15}\,\text{A}$ for the BJTs shows that the currents in the two branches of the current source are essentially $220\,\mu\text{A}$. This compares very favorably with the $236\,\mu\text{A}$ obtained by the hand analysis.

Transistors Q_1 through Q_6 and diode D_1 in Figure 13.20 are all matched, which means that $I_{C5} = I_{C4} \cong 200\,\mu\text{A}$. The current in D_2 establishes the diode voltage that also biases Q_{14} and Q_{15}. The nominal value of I_{C18} is 2 mA.

13.4.4 CA3140 Small-Signal Analysis

We analyze the small-signal voltage gain of the CA3140 op-amp by dividing the configuration into its basic circuits and using results previously obtained.

Input Stage

From the results in Chapter 11, the small-signal differential voltage gain can be written

$$A_d = \sqrt{2K_p I_{Q5}}\,(r_{o10} \| R_{act1} \| R_{i2}) \tag{13.56}$$

where I_{Q5} is the bias current supplied by Q_2 and Q_5. Resistance r_{o10} is the output resistance looking into the drain of M_{10}, R_{act1} is the effective resistance of the active load, and R_{i2} is the input resistance of the gain stage.

Example 13.12 **Objective:** Calculate the small-signal differential voltage gain of the CA3140 op-amp input stage.

Assume a conduction parameter value of $K_p = 0.6\,\text{mA/V}^2$ for M_{10}, an npn bipolar current gain of $\beta_n = 200$, and a bipolar Early voltage of $V_A = 50\,\text{V}$.

Solution: The input resistance to the gain stage is $R_{i2} = r_{\pi 13}$; therefore,

$$R_{i2} = r_{\pi 13} = \frac{\beta_n V_T}{I_{C13}} = \frac{(200)(0.026)}{0.20} = 26\,\text{k}\Omega$$

Resistances r_{o10} and R_{act1} are normally in the hundreds of kilohms or megohm range, so the small value of R_{i2} dominates the parallel resistance value in the gain expression. We then have

$$A_d \cong \sqrt{2K_p I_{Q5}}\,(R_{i2}) = \sqrt{2(0.6)(0.2)}\,(26) = 12.7$$

Comment: The low input resistance of the gain stage severely loads the input stage, which in turn results in a relatively low voltage gain for the input stage.

Gain Stage

The magnitude of the small-signal voltage gain for the second stage is

$$|A_{v2}| = g_{m13}(r_{o13} \| R_{o4} \| R_{i3}) \tag{13.57}$$

where R_{i3} is the input resistance of the output stage and R_{o4} is the output resistance of the cascode configuration of Q_3 and Q_4. Transistor Q_{17}, which is the input transistor of the output stage, is connected as an emitter follower, which means that R_{i3} is typically in the megohm range. Similarly, the output resistance R_{o4} of the cascode configuration is typically in the megohm range.

The voltage gain of the second stage is then approximately

$$|A_{v2}| \cong g_{m13} r_{o13} \tag{13.58}$$

Example 13.13 **Objective:** Calculate the small-signal voltage gain of the second stage of the CA3140 op-amp.

Assume an Early voltage of $V_A = 150\,\text{V}$ for Q_{13}.

Solution: The transconductance is

$$g_{m13} = \frac{I_{C13}}{V_T} = \frac{0.20}{0.026} = 7.69\,\text{mA/V}$$

and the output resistance is

$$r_{o13} = \frac{V_A}{I_{C13}} = \frac{150}{0.20} = 750\,\text{k}\Omega$$

The voltage gain is therefore

$$|A_{v2}| = g_{m13} r_{o13} = (7.69)(750) = 5768$$

Comment: The second stage of the CA3140 operational amplifier provides the majority of the voltage gain.

Overall Gain

Since we have taken the loading effects of each following stage into account, the overall voltage gain is the product of the individual gain factors, or

$$A_v = A_d A_{v2} A_{v3} \tag{13.59}$$

where A_{v3} is the voltage gain of the output stage. If we assume that $A_{v3} \cong 1$ for the emitter-follower output stage, then the overall gain of the CA3140 op-amp is

$$A_v = A_d A_{v2} A_{v3} = (12.7)(5768)(1) = 73{,}254 \tag{13.60}$$

Typical values of the gain of the CA3140 op-amp are in the area of 100,000; thus, our calculations are in reasonable agreement with this value.

Frequency Response

The CA3140 op-amp is internally compensated by the Miller compensation technique to introduce a dominant pole, as was done in the 741 op-amp. The feedback capacitor C_1 is 12 pF and is connected between the collector and the base of Q_{13}, as shown in Figure 13.20. From Miller's theorem, the effective input capacitance of the second stage is

$$C_i = C_1(1 + |A_{v2}|) \tag{13.61}$$

The low-frequency dominant pole is

$$f_{PD} = \frac{1}{2\pi R_{eq} C_i} \tag{13.62}$$

where R_{eq} is the equivalent resistance between the second-stage input node and ground. Since this resistance is dominated by the input resistance to Q_{13}, we have

$$R_{eq} \cong R_{i2} = r_{\pi 13} \tag{13.63}$$

Example 13.14 **Objective:** Determine the dominant-pole frequency and unity-gain bandwidth of the CA3140 op-amp.

Again, we will use results from previous calculations.

Solution: Previously, we determined that $|A_{v2}| = 5768$; therefore, the effective input capacitance is

$$C_i = C_1(1 + |A_{v2}|) = 12(1 + 5768) = 69{,}228 \text{ pF}$$

The gain stage input resistance is

$$R_{i2} = r_{\pi 13} = 26\text{k}\Omega$$

which means that

$$f_{PD} \cong \frac{1}{2\pi R_{i2} C_i} = \frac{1}{2\pi(26 \times 10^3)(69{,}228 \times 10^{-12})} = 88\text{ Hz}$$

Finally, the unity-gain bandwidth is

$$f_T = f_{PD} A_v = (88)(73{,}254) \Rightarrow 6.4\text{ MHz}$$

Comment: This unity-gain bandwidth value compares favorably with typical values of 4.5 MHz listed in the data sheet.

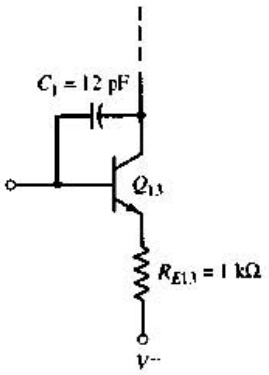


Figure 13.22 Figure for Exercise 13.19

Test Your Understanding

13.17 Using the CA3140 op-amp circuit and the transistor parameters given in Example 13.11, determine the minimum supply voltages that will still mainain Q_6 and Q_7 in the active region. Assume $V^+ = -V^-$. (Ans. $V^+ = -V^- = 1.86$ V)

13.18 Consider the CA3140 op-amp bias circuit in Figure 13.21. Assume that $V_{BE7} = 0.6$ V and $R_1 = 5\text{k}\Omega$. If the p-channel MOSFET parameters are $K_p = 0.3\text{ mA/V}^2$ and $|V_{TP}| = 1.4$ V, determine I_1, I_2, and V_{SG}. (Ans. $V_{SG} = 2.54$ V, $I_1 = I_2 = 0.388$ mA)

***13.19** Assume the gain stage of the CA3140 op-amp is modified to include an emitter resistor, as shown in Figure 13.22. Let $\lambda = 0.02\text{ V}^{-1}$ for M_{10}. Assume all other transistor parameters are the same as those in Example 13.12. If the transistor bias currents in M_{10} and Q_{12} are 100 μA and the current in Q_{13} is 200 μA, determine the new value of the small-signal differential voltage gain of the input stage. (Ans. 69.1)

13.5 JFET OPERATIONAL AMPLIFIER CIRCUITS

The advantage of using MOSFETs as input devices in a BiCMOS op-amp is that extremely small input bias currents can be achieved. However, MOSFET gates connected to outside terminals of an IC must be protected against electrostatic damage. Typically, this is accomplished by using back-biased diodes on the input, as was shown in Figure 13.20. Unfortunately, the input op-amp bias currents are then dominated by the leakage currents in the protection diodes, which means that the small input bias currents cannot be fully realized. JFETs as input devices also offer the advantage of low input currents, and they do not need electrostatic protection devices. Input gate currents in a JFET are

usually well below 1 nA, and are often on the order of 10 pA. In addition, JFETs offer greatly reduced noise properties.

In this section, we will examine two op-amp configurations using JFETs as input devices. Since the analysis is essentially identical to that given in the last two sections, we will limit ourselves to a general discussion of the circuit characteristics.

13.5.1 Hybrid FET Op-Amp, LH002/42/52 Series

Figure 13.23 is a simplified circuit diagram of an LH002/42/52 series op-amp, which uses a pair of JFETs for the input differential pair. Note that the general layout of the circuit is essentially the same as that of the 741 op-amp.

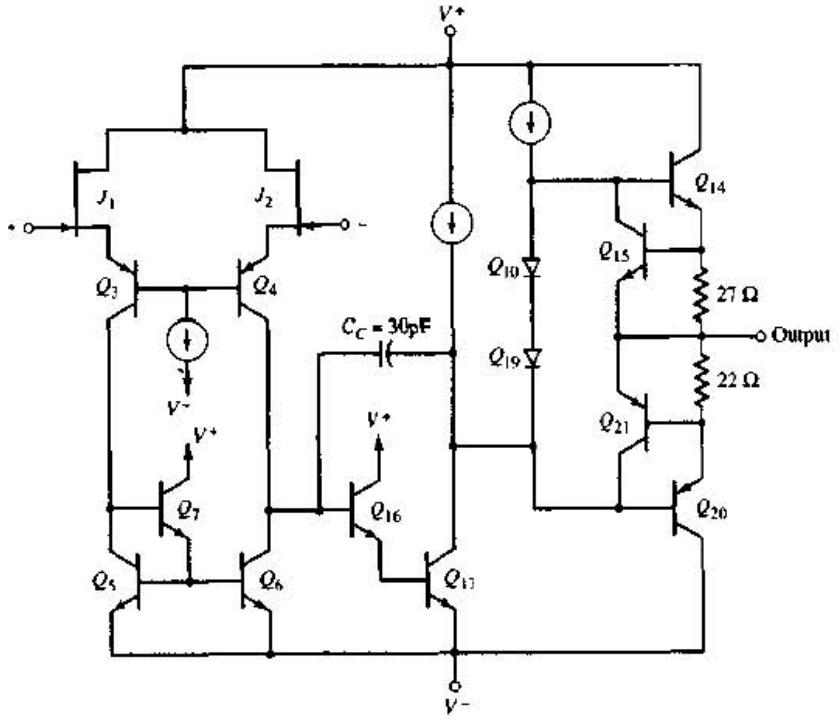


Figure 13.23 Equivalent circuit, LH0022/42/52 series hybrid JFET op-amp

The input diff-amp stage consists of transistors J_1, J_2, Q_3, and Q_4; J_1 and J_2 are n-channel JFETs operating in a source-follower configuration. The differential output signal from J_1 and J_2 is the input to the common-base amplifier formed by Q_3 and Q_4, which provides a large voltage gain. Transistors Q_5, Q_6, and Q_7 form the active load for the input stage.

The gain stage is composed of Q_{16} and Q_{17} connected in a Darlington pair configuration. This stage also includes a 30 pF compensation capacitor. The output stage consists of the complementary push–pull emitter-follower configuration of Q_{14} and Q_{20}. Transistors Q_{14} and Q_{20} are biased slightly "on" by diodes Q_{10} and Q_{19}, to minimize crossover distortion. Transistors Q_{15} and Q_{21} and the associated 27 Ω and 22 Ω resistors provide the short-circuit protection.

An abbreviated data sheet for an LH0042C op-amp is shown in Table 13.3. Note the very large differential-mode input resistance and the low input bias current.

Table 13.3 LH0042C data

Parameter	Minimum	Typical	Maximum	Units
Input bias current		15	50	pA
Differential-mode input resistance		10^{12}		Ω
Input capacitance		4		pF
Open-loop gain (R_L = 1 kΩ)	25,000	100,000		V/V
Unity-gain frequency		1		MHz

13.5.2 Hybrid FET Op-Amp, LF155 Series

Another example of a JFET op-amp is the LF155 BiFET op-amp. A simplified circuit diagram showing the input stage is in Figure 13.24. The input BiFET op-amp stage consists of p-channel JFETs J_1 and J_2 biased by the bipolar transistor Q_8. The active load for the input diff-amp consists of the p-channel JFETs J_3 and J_4, for which $V_{GS} = 0$.

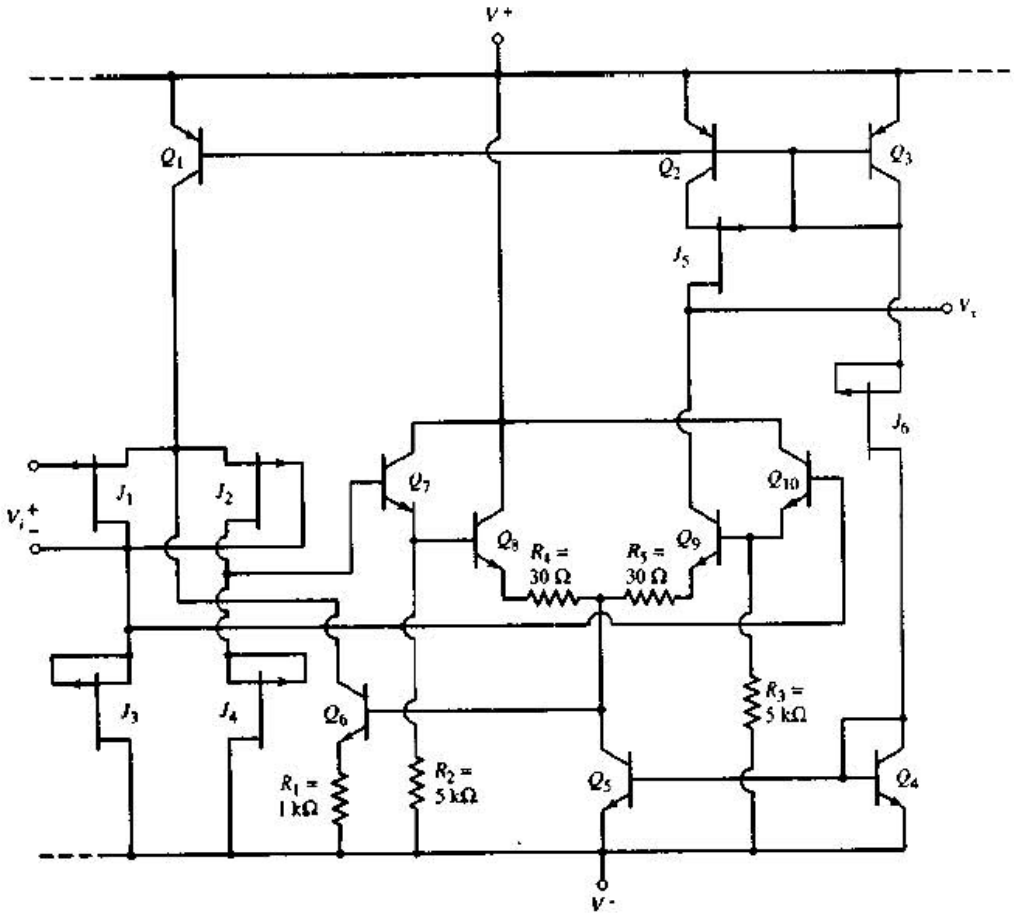


Figure 13.24 Equivalent circuit, LF155 BiFET op-amp input stages

A two-sided output from the input diff-amp stage is connected to a second diff-amp stage consisting of Darlington pairs Q_7 through Q_{10}. The second, or gain, stage is biased by bipolar transistor Q_5. The cascode configuration of J_5 and Q_2 form the active load for the gain stage.

The circuit has a common-mode feedback loop in the bias circuit. The base of Q_6 is connected to the collector of Q_5. If the drain voltages of J_1 and J_2 increase, the Darlington second stage drives the base voltage of Q_6 higher. The current in Q_6 then increases, reducing the drain currents in J_1 and J_2, since I_{C1} is a constant current. Smaller drain currents cause the voltages at the J_1 and J_2 drains to decrease, which then stabilizes the drain voltages.

JFET J_6 is connected as a current source, which establishes a reference current in Q_3, Q_4, and J_6. This reference current then produces the bias currents in the current mirrors Q_4–Q_5 and Q_1–Q_2–Q_3.

In this BiFET op-amp, we see the advantages of incorporating both JFET and bipolars in the same circuit. The JFET input devices provide a very high input impedance, normally in the range of $10^{12}\,\Omega$. The current-connected transistor J_6 allows the reference bias current to be controlled without the use of a resistor. Incorporating bipolar transistors in the second stage takes advantage of their higher transconductance values compared to JFETs, to produce a high second-stage gain.

Test Your Understanding

13.20 Consider the LF155 BiFET input stage in Figure 13.24. The p-channel JFET parameters are $I_{DSS} = 300\,\mu A$, $V_P = 1\,V$, and $\lambda = 0.01\,V^{-1}$. The supply voltages are $V^+ = 5\,V$ and $V^- = -5\,V$. Let $V_{BE}(\text{npn}) = 0.6\,V$ and $V_{EB}(\text{pnp}) = 0.6\,V$. Determine the bias currents I_{C3}, I_{C2}, and I_{C1}. (Ans. $I_{C1} = I_{C2} = I_{C3} = 300\,\mu A$)

13.6 SUMMARY

- In this chapter, we have combined various basic circuit configurations to form larger operational amplifier circuits. In general, an op-amp circuit consists of a diff-amp input stage, a second or gain stage, and an output stage. The design of integrated circuit operational amplifier circuits depends on the use of matched devices.
- The LM741 op-amp is a widely used, general-purpose, bipolar op-amp. This circuit serves as a good case study for a detailed discussion of the circuit design, including a discussion of the input stage design, the Darlington pair gain stage, and the class-AB complementary output stage with the protection circuitry.
- A detailed dc analysis of each stage of the 741 was performed to determine the dc currents and voltages. A detailed small-signal analysis determined the gain of each stage and the overall small-signal voltage gain. The calculated voltage gain of approximately 200,000 agrees well with the typical value given in data sheets. The output resistance is approximately $56\,\Omega$. The 741 is internally compensated, and the dominant pole frequency is on the order of 10 Hz. The unity-gain bandwidth is approximately 1.9 MHz.
- In many cases, all-CMOS operational amplifier circuits require only two stages. These circuits typically drive only low capacitive loads on an IC chip, so the low output impedance of a third output stage is not required. The MC14573 all-CMOS op-amp

circuit was considered. The calculated small-signal voltage gain of this two-stage circuit was approximately 84 dB, which agrees well with data sheets. Even though the gain is smaller than that of typical bipolar op-amps, this circuit is useful in specialized on-chip applications.

- An all-CMOS folded cascode operational amplifier circuit was analyzed. The advantage of this circuit is a very high output resistance that produces a very large differential-mode voltage gain.
- An all-CMOS current-mirror operational amplifier circuit was considered. The advantage of this circuit is an increased gain–bandwidth product. A cascode version of the current mirror op-amp was briefly considered.
- Two BiCMOS operational amplifier circuits were discussed. The first was a modified version of the folded cascode design. The use of bipolar cascode transistors in this circuit produces an increased phase margin. A CA3140 BiCMOS op-amp was analyzed. A unique aspect of this circuit is that the bias current generated from the bias circuitry is independent of bias voltage over a wide range of applied bias voltages.
- Two examples of a hybrid JFET or BiFET op-amp circuit were considered. The input stage is composed of a JFET differential pair, while the remainder of the circuits are designed primarily with bipolar transistors. Using JFETs as the input devices keeps the input bias currents extremely small, usually in the picoampere range.

CHECKPOINT

After studying this chapter, the reader should have the ability to:

✔ Design a basic bipolar or MOSFET operational amplifier circuit. (Section 13.1)

✔ Analyze and understand the operation and characteristics of the LM741 op-amp circuit. (Section 13.2)

✔ Analyze and understand the operation and characteristics of CMOS op-amp circuits, including the folded cascode and the CMOS current-mirror circuits. (Section 13.3)

✔ Analyze and understand the operation and characteristics of BiCMOS operational amplifier circuits. (Section 13.4)

REVIEW QUESTIONS

1. Describe the principal stages of a general-purpose operational amplifier.
2. What is meant by the term matched transistors? What parameters in BJTs and MOSFETs are identical in matched devices?
3. Describe the operation and characteristics of a BJT complementary push–pull output stage. What are the advantages of this circuit?
4. Describe the operation and characteristics of a MOSFET complementary push–pull output stage. What are the advantages of this circuit?
5. Describe the advantages and disadvantages of an all-BJT op-amp circuit.
6. Describe the advantages and disadvantages of an all-CMOS op-amp circuit.
7. Describe the advantages and disadvantages of a BiCMOS op-amp circuit.
8. Describe the advantages and disadvantages of a JFET op-amp circuit.
9. Sketch and describe the characteristics of the 741 input stage.
10. Describe what is meant by output short-circuit protection.
11. Describe the frequency compensation technique in the 741 op-amp circuit.
12. Sketch and describe the general characteristics of a folded cascode circuit.

13. Sketch and describe the general characteristics of a current-mirror op-amp circuit. Why is the gain not increased? What is the principal advantage of this circuit?
14. Sketch and describe the principal advantage of a BiCMOS folded cascode op-amp circuit.
15. Explain why an output resistance on the order of five hundred megohms may not be achieved in practice.
16. What are the principal factors limiting the unity-gain bandwidth of an op-amp circuit?

PROBLEMS

Section 13.1 General Op-Amp Circuit Design

D13.1 Design the circuit in Figure 13.2 such that the maximum power dissipated in the circuit is 15 mW and such that the common-mode input voltage is in the range $-3 \leq v_{CM} \leq 3$ V. Using a computer simulation, adjust the value of R_3 such that the output voltage is zero for zero input signal voltages.

13.2 Using the results of Problem 13.1, determine, from a computer simulation, the differential-mode voltage gain of the diff-amp and the voltage gain of the second stage of the op-amp circuit in Figure 13.2. Use standard transistor models in the circuit.

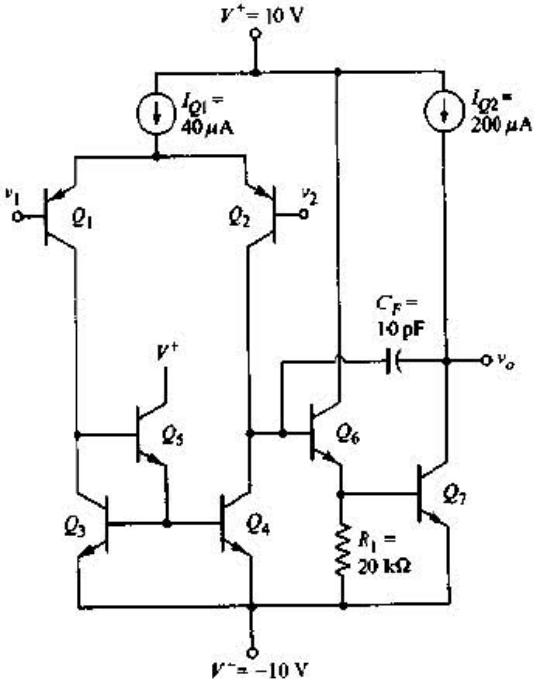


Figure P13.3

***13.3** Consider the BJT op-amp circuit in Figure P13.3. The transistor parameters are: $\beta(\text{npn}) = 120$, $\beta(\text{pnp}) = 80$, $V_A = 80$ V (all transistors), and base–emitter turn-on voltage = 0.6 V (all transistors). (a) Determine the small-signal differential-mode voltage gain. (b) Find the differential-mode input resistance. (c) Determine the unity-gain bandwidth.

Section 13.2 A Bipolar Operational Amplifier Circuit

13.4 Consider the input stage of the 741 op-amp in Figure 13.4(b). (a) Assume the input voltages are $V_1 = 0$ and $V_2 = +15\,\text{V}$. Consider the B–E voltage of each transistor and determine which transistor acts as the protection device. (b) Repeat part (a) for $V_1 = -15\,\text{V}$ and $V_2 = 0$.

13.5 For the input stage of the 741 op-amp, assume B–E breakdown voltages of 5 V for the npn devices and 50 V for the pnp devices. Estimate the differential input voltage at which breakdown will occur.

RD13.6 Consider the bias circuit portion of the 741 op-amp in Figure 13.5. (a) Redesign the resistor values of R_5 and R_4 such that $I_{\text{REF}} = 0.50\,\text{mA}$ and $I_{C10} = 30\,\mu\text{A}$ for bias voltages of $\pm 15\,\text{V}$. Assume base-emitter turn-on voltages of 0.6 V. (b) Using the results of part (a), determine I_{REF} and I_{C10} if the bias voltages change to $\pm 5\,\text{V}$.

13.7 Repeat Problem 13.6 using the exponential relationship between collector current and base–emitter voltage in which $I_S = 10^{-14}\,\text{A}$. What are the actual values of base-emitter voltage in each case?

13.8 The minimum recommended supply voltages for the 741 op-amp are $V^+ = 5\,\text{V}$ and $V^- = -5\,\text{V}$. Using these lower supply voltages, calculate: (a) I_{REF}, I_{C10}, I_{C6}, I_{C17}, and I_{C13A}; and (b) the voltage gains of the input and gain stages for the circuit values in Figure 13.3.

13.9 An expanded circuit diagram of the 741 input stage is shown in Figure 13.6. Assume $I_{C10} = 19\,\mu\text{A}$. If the current gain of the npn transistors is $\beta_n = 200$ and the current gain of the pnp transistors is $\beta_p = 10$, determine I_{C9}, I_{C2}, I_{C4}, I_{B9}, and I_{B4}.

13.10 Consider the 741 op-amp in Figure 13.3, biased with $V^+ = 15\,\text{V}$ and $V^- = -15\,\text{V}$. Assume that no load is connected at the output, and let the input voltages be zero. Calculate the total power dissipated in the op-amp circuit. What are the currents supplied by V^+ and V^-?

13.11 Consider the 741 circuit in Figure 13.3. (a) Determine the maximum range of common-mode input voltage if the bias voltages are $\pm 15\,\text{V}$. (b) Repeat part (a) if the bias voltages are $\pm 5\,\text{V}$.

13.12 For Q_{15} in the output stage of the 741 op-amp, assume $I_S = 10^{-14}\,\text{A}$. If the output is inadvertently connected to $V^- = -15\,\text{V}$ and the inputs are at zero, estimate the currents I_{C14} and I_{C15}.

13.13 Consider the output stage in Figure P13.13, with parameters $V^+ = 10\,\text{V}$, $V^- = -10\,\text{V}$, $R_L = 4\,\text{k}\Omega$, and $I_{\text{Bias}} = 0.25\,\text{mA}$. Assume the diode parameters are $I_S = 2 \times 10^{-14}\,\text{A}$ and the transistor parameters are $I_S = 5 \times 10^{-14}\,\text{A}$. (a) For $v_I = 0$, determine V_{BB}, I_{CN}, and I_{CP}. (b) For $v_I = 5\,\text{V}$, determine v_o, i_L, V_{BB}, I_{CN}, and I_{CP}.

D13.14 Figure P13.14 shows a circuit often used to provide the V_{BB} voltage in the op-amp output stage. Assume $I_S = 10^{-14}\,\text{A}$ for the transistor, $I_{\text{Bias}} = 180\,\mu\text{A}$, and $I_C = 0.9 I_{\text{Bias}}$. Neglect the base current. Design the circuit such that $V_{BB} = 1.157\,\text{V}$.

13.15 Assume bias voltages on the 741 op-amp of $\pm 15\,\text{V}$. (a) Determine the differential-mode voltage gain of the first stage if $R_1 = R_2 = 0$. (b) Determine the voltage gain of the second stage if $R_8 = 0$.

13.16 Recalculate the voltage gain of the 741 op-amp input stage if $I_{C10} = 40\,\mu\text{A}$.

13.17 Calculate the output resistance of the 741 op-amp if Q_{14} is conducting and Q_{20} is cut off. Assume an output current of 2 mA.

13.18 Determine the differential input resistance of the 741 op-amp.

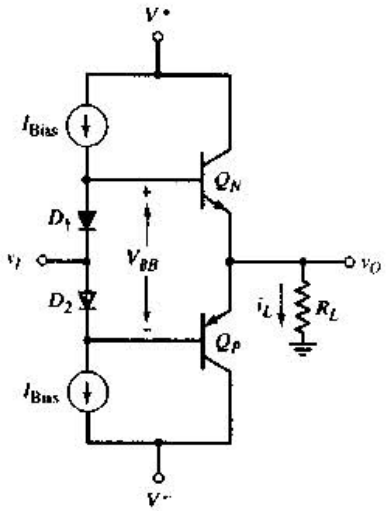


Figure P13.13

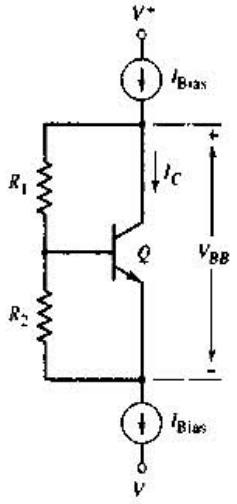


Figure P13.14

13.19 The frequency response of a particular 741 op-amp shows that the op-amp has a phase margin of 70 degrees. If a second single pole exists, in addition to the dominant pole, determine the frequency of the second pole. Use the overall gain and dominant-pole parameters calculated in Section 13.2.

Section 13.3 CMOS Operational Amplifier Circuits

RD13.20 Consider the MC14573 op-amp in Figure 13.14. The dc bias currents and small-signal voltage gains were determined in Examples 13.8 and 13.9. Redesign the circuit such that the width-to-length ratio of M_1 and M_2 is increased from 12.5 to 50. All other circuit and transistor parameters remain the same. (a) Determine the original transconductance of M_1 and M_2, and the new transconductance value. (b) Determine the new values of voltage gain for the input and second stages, and the overall voltage gain.

13.21 Consider the basic diff-amp with active load and current biasing in Figure 13.14. Using a computer simulation, investigate the change in the voltage at the drain of M_2 as M_1 and M_2 and also as M_3 and M_4 become slightly mismatched.

13.22 The CMOS op-amp in Figure 13.14 is biased at $V^+ = 10\,\text{V}$ and $V^- = -10\,\text{V}$. Assume transistor parameters of $|V_T| = 1.5\,\text{V}$ (all transistors), $(\frac{1}{2})\mu_n C_{ox} = 20\,\mu\text{A/V}^2$, $(\frac{1}{2})\mu_p C_{ox} = 10\,\mu\text{A/V}^2$, $\lambda_p = 0.02\,\text{V}^{-1}$, and $\lambda_n = 0.01\,\text{V}^{-1}$. Let $R_{\text{set}} = 200\,\text{k}\Omega$. Assume transistor width-to-length ratios of 10 for M_3 and M_4, and 20 for all other transistors. (a) Determine I_{REF}, I_Q, and I_{D7}. (b) Find the small-signal voltage gain of the input and second stages, and the overall voltage gain.

13.23 For the CMOS op-amp in Figure 13.14, the dc biasing is designed such that $I_{\text{REF}} = I_Q = I_{D8} = 200\,\mu\text{A}$. The transistor parameters are $|V_T| = 1\,\text{V}$ (all transistors), $\lambda_n = 0.005\,\text{V}^{-1}$, $\lambda_p = 0.01\,\text{V}^{-1}$, $(\frac{1}{2})\mu_n C_{ox} = 20\,\mu\text{A/V}^2$, and $(\frac{1}{2})\mu_p C_{ox} = 10\,\mu\text{A/V}^2$. The transistor width-to-length ratios are 5 for M_5, M_6, and M_8; 10 for M_1 and M_2; and 20 for M_3, M_4, and M_7. Determine the small-signal voltage gains of the input and second stages, and the overall voltage gain.

13.24 Consider the MC14573 op-amp in Figure 13.14, with circuit and transistor parameters as given in Examples 13.8 and 13.9. If the compensation capacitor is $C_1 = 12\,\text{pF}$, determine the dominant-pole frequency.

13.25 The CMOS op-amp in Figure 13.14 has circuit and transistor parameters as given in Problem 13.22. Determine the compensation capacitor required such that the dominant-pole frequency is $f_{PD} = 8\,\text{Hz}$.

13.26 Consider the CMOS op-amp in Figure 13.14, with transistor and circuit parameters as given in Examples 13.8 and 13.9. Determine the output resistance R_o of the open-loop circuit.

13.27 A simple output stage for an NMOS op-amp is shown in Figure P13.27. Device M_1 operates as a source follower. Assume that M_1 and M_2 are biased at $I_D = 0.5\,\text{mA}$. (a) Calculate the small-signal open-circuit voltage gain $A_v = v_O/v_I$. (b) If the output resistance of source v_I is $10\,\text{k}\Omega$, determine the output resistance of this output stage.

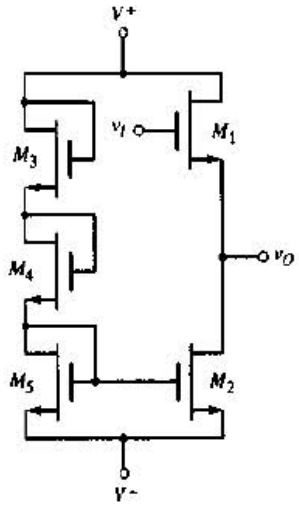


Figure P13.27

***13.28** The CMOS folded cascode circuit in Figure 13.16 is biased at $\pm 5\,\text{V}$ and the reference current is $I_{REF} = 50\,\mu\text{A}$. The transistor parameters are $V_{TN} = 0.5\,\text{V}$, $V_{TP} = -0.5\,\text{V}$, $K_n = K_p = 0.5\,\text{mA/V}^2$, and $\lambda_n = \lambda_p = 0.015\,\text{V}^{-1}$. (a) Determine the small-signal differential voltage gain. (b) Find the output resistance of the circuit. (c) If the capacitance at the output node is $C_L = 5\,\text{pF}$, determine the unity-gain bandwidth of the amplifier.

***RD13.29** The CMOS folded cascode amplifier in Figure 13.16 is to be redesigned to provide a differential voltage gain of 10,000. The biasing is the same as described in Problem 13.28. The transistor parameters are $V_{TN} = 0.5\,\text{V}$, $V_{TP} = -0.5\,\text{V}$, $k_n' = 80\,\mu\text{A/V}^2$, $k_p' = 35\,\mu\text{A/V}^2$, $\lambda_n = 0.015\,\text{V}^{-1}$, and $\lambda_p = 0.02\,\text{V}^{-1}$. Assume $(W/L)_p = 2.2(W/L)_n$ where appropriate so that the electrical parameters of PMOS and NMOS devices are nearly identical.

***D13.30** The CMOS folded cascode amplifier of Figure 13.16 is to be designed to provide a differential voltage gain of 25,000. The maximum power dissipated in the circuit is to be limited to 3 mW. Assume transistor parameters as described in Problem 13.29, except the relation between NMOS and PMOS width-to-length ratios need not be maintained.

13.31 The bias current in the CMOS current-gain op-amp in Figure 13.17 is $I_Q = 60\,\mu\text{A}$. The transistor parameters are $V_{TN} = 0.5\,\text{V}$, $V_{TP} = -0.5\,\text{V}$, $K_n = K_p = 0.5\,\text{mA/V}^2$ (all transistors except M_5 and M_6), and $\lambda_n = \lambda_p = 0.015\,\text{V}^{-1}$. Let $B = 3$. (a) Determine the small-signal differential voltage gain. (b) Find the output resistance of the circuit. (c) If the total capacitance at the output terminal is 5 pF, determine the dominant-pole frequency and the unity-gain bandwidth.

RD13.32 The CMOS current gain op-amp in Figure 13.17 is to be redesigned to provide a differential voltage gain of 400. The transistor parameters are $V_{TN} = 0.5\,\text{V}$, $V_{TP} = -0.5\,\text{V}$, $k_n' = 80\,\mu\text{A/V}^2$, $k_p' = 35\,\mu\text{A/V}^2$, $\lambda_n = 0.015\,\text{V}^{-1}$, and $\lambda_p = 0.02\,\text{V}^{-1}$. The bias current is to be $I_Q = 80\,\mu\text{A}$. Let $B = 2.5$. (a) Design the basic amplifier to provide the specified voltage gain. (b) Design a current source to provide the necessary bias current. (c) Determine the unity-gain bandwidth if the capacitance at the output terminal is 3 pF.

RD13.33 Redesign the CMOS cascode current mirror in Figure 13.18 to provide a differential voltage gain of 20,000. The bias current and transistor parameters are the same as in Problem 13.32. (a) Design the basic amplifier to provide the specified voltage gain. (b) Design a current source to provide the necessary bias current. (c) Determine the unity gain bandwidth if the capacitance at the output terminal is 3 pF.

Section 13.4 BiCMOS Operational Amplifier Circuits

13.34 A BiCMOS amplifier is shown in Figure P13.34. The transistor parameters are $V_{TP} = -0.7\,\text{V}$, $k_p' = 40\,\mu\text{A/V}^2$, $(W/L) = 25$, $\lambda = 0.02\,\text{V}^{-1}$, $\beta = 120$, and $V_A = 120\,\text{V}$. The bias current is $I_Q = 200\,\mu\text{A}$. Determine the small-signal differential voltage gain.

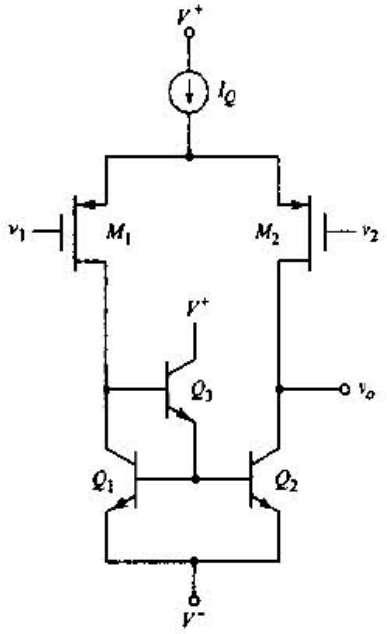


Figure P13.34

D13.35 Design a BiCMOS amplifier that is complementary to the one in Figure P13.34 in that the input devices are NMOS and the load transistors are pnp. Assume transistor parameters of $V_{TN} = 0.5\,\text{V}$, $k_n' = 80\,\mu\text{A/V}^2$, $(W/L) = 25$, $\lambda = 0.015\,\text{V}^{-1}$, $\beta = 80$, and $V_A = 80\,\text{V}$. Assume the bias current is $I_Q = 200\,\mu\text{A}$. Determine the small-signal differential voltage gain.

***13.36** The reference current in the BiCMOS folded cascode amplifier in Figure 13.19 is $I_{REF} = 200\,\mu\text{A}$ and the circuit bias voltages are $\pm 10\,\text{V}$. The MOS transistor parameters are the same as in Problem 13.28. The BJT parameters are $\beta = 120$ and $V_A = 80\,\text{V}$. (a) Determine the small-signal differential voltage gain. (b) Find the output resistance of the circuit. (c) If the capacitance at the output node is 5 pF, determine the unity-gain bandwidth of the amplifier.

***D13.37** The BiCMOS folded cascode amplifier in Figure 13.19 is to be designed to provide a differential voltage gain of 25,000. The maximum power dissipated in the circuit is to be limited to 10 mW. Assume MOS transistor parameters as described in Problem 13.29. The BJT parameters are $\beta = 120$ and $V_A = 80\,\text{V}$.

13.38 If the CA3140 op-amp is biased at $V^+ = 15\,\text{V}$ and $V^- = -15\,\text{V}$, determine the input common-mode voltage range. Assume B-E voltages of 0.6 V for the bipolar transistors and $|V_{TP}| = 1.4\,\text{V}$ for the MOSFETs.

13.39 Consider the bias circuit portion of the CA3140 op-amp in Figure 13.21. If $V_{BE7} = 0.6\,\text{V}$ for Q_7 and $V_{TP} = -1.4\,\text{V}$ for M_8, determine the necessary conduction parameter for M_8 such that $I_1 = I_2 = 300\,\mu\text{A}$.

13.40 In the bias circuit portion of the CA3140 op-amp in Figure 13.21, the bipolar transistor parameters are $V_{BE}(\text{npn}) = 0.6\,\text{V}$ and $V_{EB}(\text{pnp}) = 0.6\,\text{V}$, and the MOSFET parameters are $|V_{TP}| = 1.4\,\text{V}$ and $K_p = 0.25\,\text{mA/V}^2$. If the power supply voltages are $V^+ = -V^- \equiv V_S$, determine the minimum value of V_S such that the bias currents are independent of the supply voltage.

13.41 Consider the CA3140 op-amp in Figure 13.20. If the bias currents change such that $I_{C5} = I_{C4} = 300\,\mu\text{A}$, determine the voltage gains of the input and second stages, and find the overall voltage gain.

13.42 Assume the gain stage of the CA3140 op-amp is modified to include an emitter resistor, as shown in Figure 13.22. Let $\lambda = 0.02\,\text{V}^{-1}$ for M_{10}. If the transistor bias currents in M_{10} and Q_{12} are $150\,\mu\text{A}$ and the current in Q_{13} is $300\,\mu\text{A}$, determine the dominant-pole frequency and unity-gain bandwidth.

Section 13.5 JFET Operational Amplifier Circuits

13.43 In the LF155 BiFET op-amp in Figure 13.24, the combination of Q_3, J_6, and Q_4 establishes the reference bias current. Assume the power supply voltages are $V^+ = 10\,\text{V}$ and $V^- = -10\,\text{V}$. The transistor parameters are $V_{EB}(\text{on}) = 0.6\,\text{V}$, $V_{BE}(\text{on}) = 0.6\,\text{V}$, and $V_P = 4\,\text{V}$ for Q_3, Q_4, and J_6, respectively. Determine the required I_{DSS} value for J_6 to establish a reference current of $I_{\text{REF}} = 0.8\,\text{mA}$.

13.44 Consider the circuit in Figure P13.44. A JFET diff-amp input stage drives a bipolar Darlington second stage. The p-channel differential pair J_1 and J_2 are connected to the bipolar active load transistors Q_3 and Q_4. Assume JFET parameters of $V_P = 3\,\text{V}$, $I_{DSS} = 200\,\mu\text{A}$, and $\lambda = 0.02\,\text{V}^{-1}$. The bipolar transistor parameters are $\beta = 100$ and $V_A = 50\,\text{V}$. (a) Determine the input resistance R_{i2} to the second stage. (b) Calculate the small-signal differential-mode voltage gain of the input stage. Compare this value to the 741 and CA3140 input stage results.

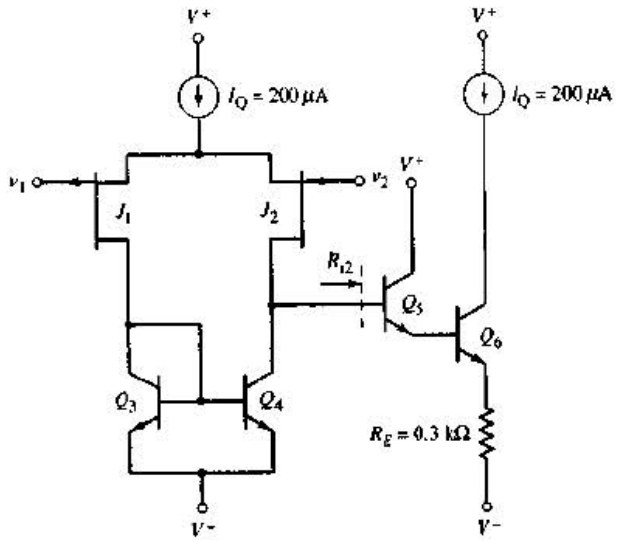


Figure P13.44

D13.45 Consider the BiFET differential input stage in Figure P13.45, biased with power supply voltages V^+ and V^-. Let $V^+ = -V^- \equiv V_S$. (a) Design the bias circuit such that $I_{\text{REF2}} = 100\,\mu\text{A}$ for supply voltages in the range $3 \le V_S \le 12\,\text{V}$. Determine

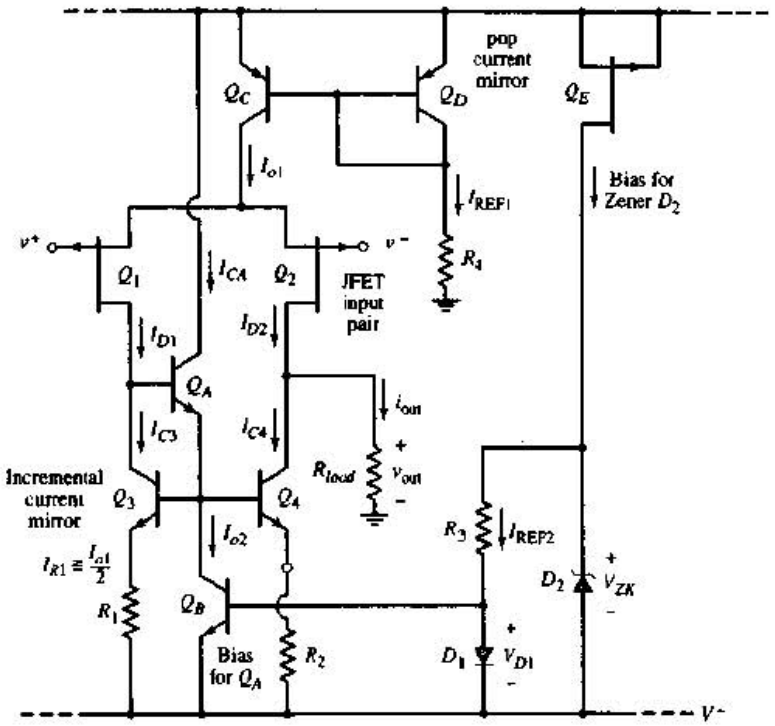


Figure P13.45

V_{ZK}, R_3, and the JFET parameters. (b) Determine the value of R_4 such that $I_{O1} = 500\,\mu A$ when $V^+ = 12\,V$.

13.46 The BiFET diff-amp input stage in Figure P13.45 is biased at $I_{O1} = 1\,mA$. The JFET parameters are $V_P = 4\,V$, $I_{DSS} = 1\,mA$, and $\lambda = 0.02\,V^{-1}$. The bipolar transistor parameters are $\beta = 200$ and $V_A = 100\,V$. (a) For $R_1 = R_2 = 500\,\Omega$, determine the minimum load resistance R_L such that a differential-mode voltage gain of $A_d = 500$ is obtained in the input stage. (b) If $R_L = 500\,k\Omega$, determine the range of resistance values $R_1 = R_2$ such that a differential-mode voltage gain of $A_d = 700$ is obtained in this input stage.

COMPUTER SIMULATION PROBLEMS

13.47 Consider the input stage and bias circuit of the 741 op-amp in Figure 13.5. Transistor Q_{10} may be replaced by a constant-current source equal to $19\,\mu A$. Assume: the npn devices have parameters $\beta = 200$ and $V_A = 150\,V$; the pnp devices have parameters $\beta = 50$ and $V_A = 50\,V$; and all transistors have $I_S = 10^{-14}\,A$. (a) Using an appropriate ac load at the collector of Q_6, determine the differential gain of the input stage. (b) Determine the differential-mode input resistance. (c) Determine the common-mode input resistance.

13.48 The output stage of the 741 op-amp is shown in Figure 13.9. Transistor Q_{13} may be replaced with a constant-current source equal to 0.18 mA. The transistor parameters are as given in Problem 13.47. (a) Plot the voltage transfer function v_O verus v_{I3}. What is the voltage gain? Has the crossover distortion been eliminated? (b) Apply an input voltage v_{I3} that establishes an output voltage of $v_O = 10\,V$, for example, and set $R_L = 0$. Find the output short-circuit current and the transistor currents.

13.49 The bias circuit and gain stage, including the compensation capacitor, of the 741 op-amp is shown in Figure 13.7. Transistor Q_{13} can be simulated by connecting two pnp transistors in parallel, with relative B–E junction areas of 0.25 and 0.75 compared to all other pnp transistors. (a) Determine the low-frequency voltage gain. (b) Plot the magnitude of the voltage gain versus frequency. Compare the 3 dB frequency to the dominant-pole frequency found in Example 13.7.

13.50 Consider the BiCMOS input stage of the CA3140 op-amp in Figure 13.20. Transistor Q_5 can be replaced with a constant-current source of 200 μA. Assume: bipolar transistor parameters of $\beta = 200$, $I_{EO} = 10^{-14}$ A, and $V_A = 50$ V; and MOSFET parameters of $K_p = 0.6\,\text{mA/V}^2$, $|V_{TP}| = 1$ V, and $\lambda = 0.01\,\text{V}^{-1}$. Using an appropriate ac load at the collector of Q_{12}, determine the differential gain of the input stage. Compare the computer analysis results with those in Example 13.12.

13.51 Consider the CMOS op-amp in Figure 13.14. Assume the circuit and transistor parameters are as given in Example 13.8. In addition, let $\lambda = 0.01\,\text{V}^{-1}$ for all transistors. (a) Determine the overall low-frequency differential voltage gain. Compare these results with those in Example 13.9. (b) If the compensation capacitor is $C_1 = 12\,\text{pF}$, plot the magnitude of the voltage gain versus frequency. What is the 3 dB frequency?

DESIGN PROBLEMS

[Note: Each design should be correlated with a computer analysis.]

***D13.52** Redesign the bias circuit of the 741 op-amp such that a current $I_{C10} = 25\,\mu\text{A}$ is established when $V^+ = -V^- = 5$ V. Limit the power dissipated in the input stage and the bias circuit to 2.5 mW.

***D13.53** Consider the bipolar op-amp circuit in Figure P13.53. Design the circuit such that the differential gain is at least 800, and the output voltage is zero when the input

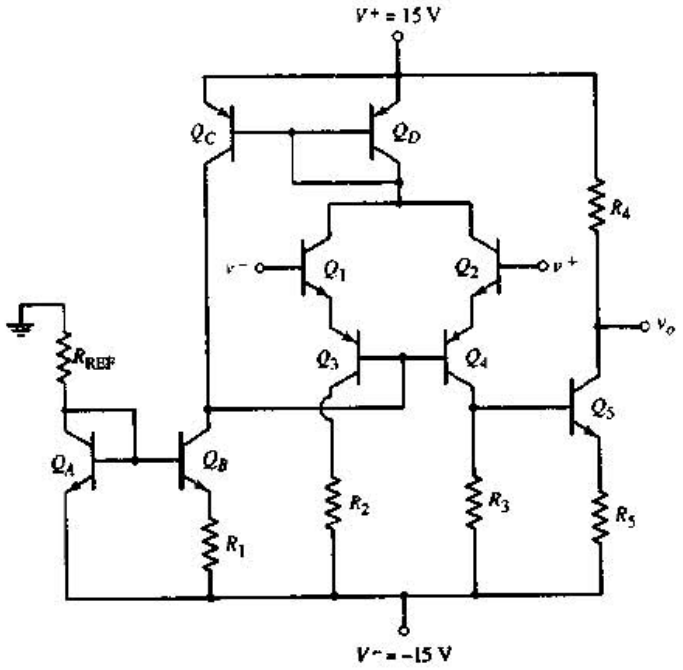


Figure P13.53

voltages are zero. The transistor current gains are 120 for all transistors, and the base–emitter voltages are 0.6 V, where appropriate.

***D13.54** Redesign the CMOS op-amp in Figure 13.14 to provide a minimum overall voltage gain of at least 50,000. The bias voltages are $V^+ = 10\,\text{V}$ and $V^- = -10\,\text{V}$. The threshold voltage is $|V_T| = 1\,\text{V}$ for all transistors, and $\lambda = 0.01\,\text{V}^{-1}$ for all transistors. Design reasonable width-to-length ratios and bias currents.

***D13.55** Consider the CMOS op-amp in Figure 13.14. Design a complementary CMOS circuit in which each element is replaced by its complement. The bias voltages are $\pm 5\,\text{V}$. The threshold voltage is $|V_T| = 0.7\,\text{V}$ for all transistors, and $\lambda = 0.01\,\text{V}^{-1}$ for all transistors. Design reasonable width-to-length ratios and bias currents to provide a minimum overall voltage gain of at least 20,000.

CHAPTER

14

Nonideal Effects in Operational Amplifier Circuits

14.0 PREVIEW

Chapter 9 introduced the ideal operational amplifier and covered a few of its many applications. In the previous chapter, we analyzed actual operational amplifier circuits, including the classic 741 op-amp. From those discussions, we can identify sources of nonideal properties in actual op-amps. Although nonideal effects could have been introduced in Chapter 9, that discussion would have been less meaningful since the source of any nonideal effect would not have been completely understood at that time. In particular, the reason for a very low dominant-pole frequency in the basic amplifier would have been a mystery. Therefore, the discussion of nonideal effects in op-amp circuits has been postponed until now.

This chapter opens by discussing and defining several practical op-amp parameters that will be further analyzed as to the effect they have on the nonideal characteristics of op-amp circuits.

We have seen how matched transistor characteristics are utilized in the design of diff-amp circuits. However, slight mismatches may occur. One part of this chapter is devoted to determining the effect of these slight transistor mismatched characteristics on the op-amp properties.

A general goal of this chapter is for the reader to understand the source of nonideal effects in op-amps and to be able to minimize their effects in the design of op-amp circuits.

14.1 PRACTICAL OP-AMP PARAMETERS

In ideal op-amps, we assume, for example, that the differential voltage gain is infinite, the input resistance is infinite, and the output resistance is zero. In practical op-amp circuits, these ideal parameter values are not realized. In this section, we define some of the practical op-amp parameters that will be considered in detail throughout the chapter. We will discuss and analzye the effect of these nonideal parameters in op-amp circuits.

14.1.1 Practical Op-Amp Parameter Definitions

Input voltage limits. Two input voltage limitations must be considered—a dc input voltage limit and a differential signal input voltage. All transistors in the input diff-amp stage must be properly biased, so there is a limit in the range of common-mode input voltage that can be applied and still maintain the proper transistor biasing. The maximum differential input signal voltage that can be applied and still maintain linear circuit operation is limited primarily by the maximum allowed output signal voltage.

Output voltage limits. The output voltage of the op-amp can never exceed the limits of the dc supply voltages. In practice, the difference between the bias voltage and output voltage must be greater than 1 to 4 V, depending on the design of the output stage. Otherwise, the output voltage saturates and is no longer a function of input voltage.

Output current limitation. The maximum current out of or into the op-amp is determined by the current ratings of the output transistors. Practical op-amp circuits cannot source or sink an infinite amount of current.

Finite open-loop voltage gain. The open-loop gain of the ideal op-amp is assumed to be infinite. In practice, the open-loop gain of any op-amp circuit is always finite. This nonideal parameter value will affect circuit performance.

Input resistance. The input resistance R_i is the small-signal resistance between the inverting and noninverting terminals when a differential voltage is applied. Ideally, this parameter is infinite, but, especially for BJT circuits, this parameter is finite.

Output resistance. The output resistance is the Thevenin equivalent small-signal resistance looking back into the output terminal of the op-amp measured with respect to ground. The ideal output resistance is zero, which means there is no loading effect at the output. In practice, this value is not zero.

Finite bandwidth. In the ideal op-amp, the bandwidth is infinite. In practical op-amps, the bandwidth is finite because of capacitances within the op-amp circuit.

Slew rate. The slew rate is defined as the maximum rate of change in output voltage per unit of time. The maximum rate at which the output voltage can change is also a function of capacitances within the op-amp circuit.

Input offset voltage. In an ideal op-amp, the output voltage is zero for zero differential input signal voltage. However, mismatches between input devices, for example, may create an output voltage with zero input. The input offset voltage is the applied differential input voltage required to induce a zero output voltage.

Input bias currents. In an ideal op-amp, the input current to the op-amp circuit is assumed to be zero. However, in practical op-amps, especially with BJT input devices, the input bias currents are not zero.

The cause of these nonideal op-amp parameters will be discussed in the following sections, as well as the effect these nonideal parameters have on op-amp circuit performance. A few other nonideal parameters will be considered in the last section of the chapter.

Table 14.1 Nonideal parameter values for three op-amp circuits

	741E			CA3140			LH0042C		
	Typ.	Max.	Unit	Typ.	Max.	Unit	Typ.	Max.	Unit
Input offset voltage	0.8	3	mV	5	15	mV	6	20	mV
Average input offset voltage drift		15	μV/°C				10		μV/°C
Input offset current	3.0	30	nA	0.5	30	pA	2		pA
Average input offset current drift		0.5	nA/°C						
Input bias current	30	80	nA	10	50	pA	2	10	pA
Slew rate	0.7		V/μs	9		V/μs	3		V/μs
CMRR	95		dB	90		dB	80		dB

Table 14.1 lists a few of the nonideal parameter values for three of the op-amps considered in the previous chapter. We will refer to this table as we discuss each of the nonideal parameters.

14.1.2 Input and Output Voltage Limitations

For linear circuit operation, all BJTs in an op-amp circuit must be biased in the forward-active region and all MOSFETs must be biased in the saturation region. For these reasons, there are limitations to the range of input and output voltages in op-amp circuits.

Figure 14.1(a) shows the simple all-BJT op-amp circuit discussed at the beginning of Chapter 13 and Figure 14.1(b) shows the all-CMOS folded cascode op-amp circuit discussed in the last chapter. We will use these two circuits to discuss the input and output voltage limitations.

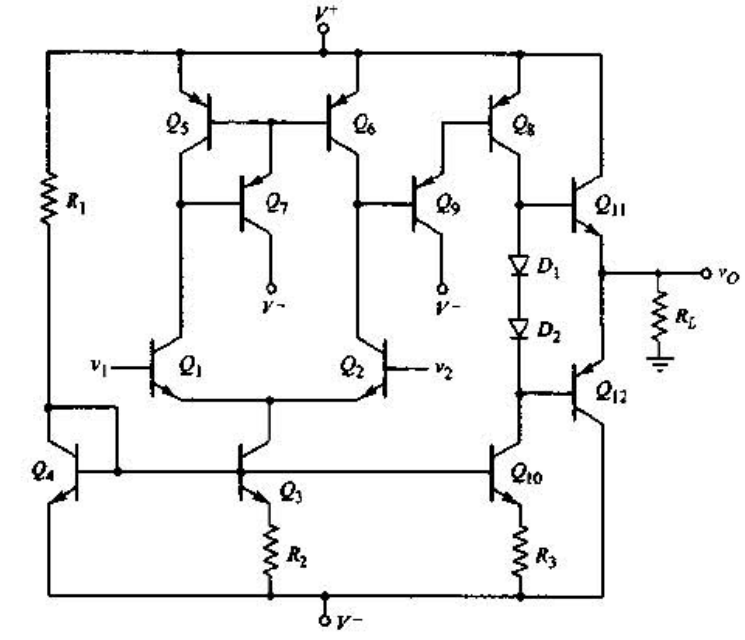
Input Voltage Limitations

Assume that in the BJT circuit of Figure 14.1(a) we apply a common-mode input voltage such that $v_{cm} = v_1 = v_2$. As v_{cm} increases, the base–collector voltages of Q_1 and Q_2 decrease, since the collector voltages are fixed at two base–emitter voltage drops below V^+. If we assume the minimum base–collector voltage is zero so that the transistor is still biased in the active mode, then the maximum value of v_{cm} is $v_{cm}(\text{max}) = V^+ - 2V_{EB}(\text{on})$.

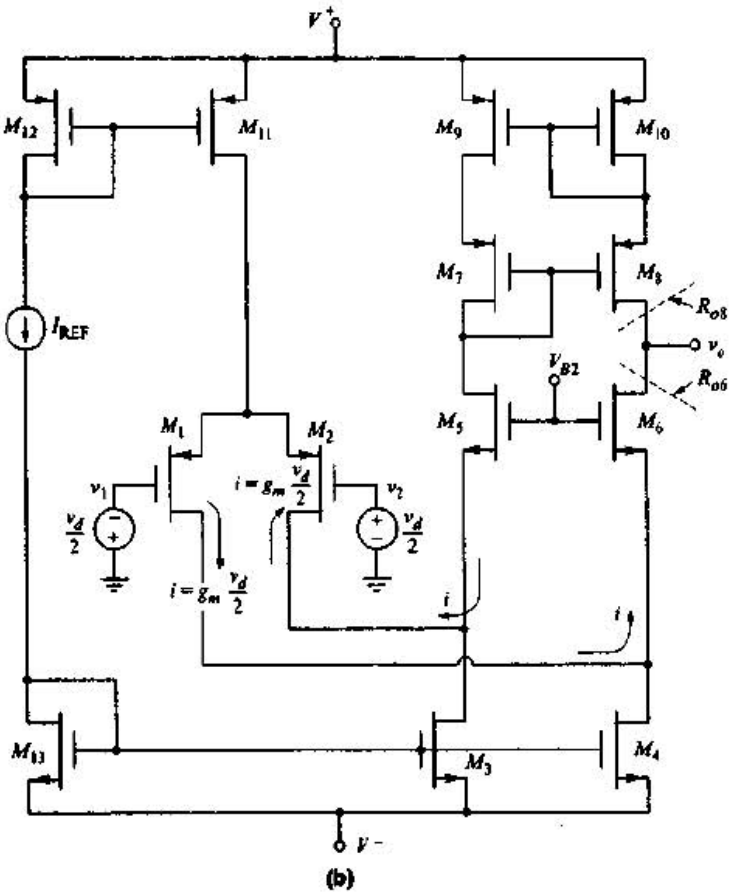
As v_{cm} decreases, the collector–emitter voltage of Q_3 decreases. If we again assume the minimum base–collector voltage is zero, or the minimum collector–emitter voltage is $V_{BE}(\text{on})$, then, taking into account the base–emitter voltage of the input transistors, the minimum value of v_{cm} is $v_{cm}(\text{min}) = V^- + 2V_{BE}(\text{on})$. So the maximum range of v_{cm} is within approximately 1.4 V of each bias voltage.

The same range of common-mode input voltage can be found for the all-MOSFET diff-amp in Figure 14.1(b). In this case, all MOSFETs must be biased in the saturation region. We can again define the common-mode input voltage as $v_{cm} = v_1 = v_2$. Now, as v_{cm} increases, V_{SD} of M_{11} decreases. The minimum value of V_{SD} is $V_{SD11}(\text{sat}) = V_{SG11} + V_{TP11}$. The maximum value of v_{cm} is then $v_{cm}(\text{max}) = V^+ - [V_{SG1} + (V_{SG11} + V_{TP11})]$. The gate-to-source voltages can be determined from the transistor parameters and currents.

As v_{cm} decreases, the source-to-drain voltage of the input transistors decreases. Assuming that M_3 and M_4 are matched to M_{13}, then the drain-to-source voltage of these transistors is equal to V_{GS13}. The minimum common-



(a)



(b)

Figure 14.1 (a) Simple all-bipolar op-amp circuit; (b) all-CMOS folded cascode op-amp circuit

mode input voltage is then $v_{cm}(\text{min}) = V^- + [V_{GS11} + (V_{SG1} + V_{TP1}) - V_{SG1}]$. The V_{SG1} terms cancel, so $v_{cm}(\text{min}) = V^- + [V_{GS11} + V_{TP1}]$.

Output Voltage Limitations

As the output voltage of the BJT circuit in Figure 14.1(a) increases or decreases, the collector–emitter voltages of the output transistors change. Again, assuming the minimum base–collector voltage is zero for a BJT biased in the forward active region, then the maximum output voltage is $v_O(\text{max}) = V^+ - [V_{EB8}(\text{on}) + V_{BE11}(\text{on})]$. The minimum output voltage is similarly found to be $v_O(\text{min}) = V^- + [V_{BE4}(\text{on}) + V_{EB12}(\text{on})]$.

For the all-CMOS circuit in Figure 14.1(b), the maximum output voltage is $v_O(\text{max}) = V^+ - [(V_{SG8} + V_{TP8}) + V_{SG10}]$. The minimum output voltage is $v_O(\text{min}) = V^- + [(V_{GS6} - V_{TN6}) + V_{GS13}]$.

Test Your Understanding

14.1 Using the circuit and transistor parameters of Example 13.10, and assuming threshold voltages of $V_{TN} = 0.5\,\text{V}$ and $V_{TP} = -0.5\,\text{V}$, determine the maximum range of common-mode input voltage for the all-CMOS folded cascode circuit of Figure 14.1(b).

14.2 Using the same circuit and transistor parameters as in Exercise 14.1, calculate the maximum range of output voltage for the all-CMOS folded cascode circuit of Figure 14.1(b).

14.2 FINITE OPEN-LOOP GAIN

In the ideal op-amp, the open-loop gain is infinite, the input differential resistance is infinite, and the output resistance is zero. None of these conditions exists in actual operational amplifiers. In the last chapter, we determined that the open-loop gain and input differential resistance may be large but finite, and the output resistance may be small but nonzero. In this section, we will determine the effect of a finite open-loop gain and input resistance on both the inverting and noninverting amplifier characteristics. We will then calculate the output resistance.

In this section, we limit our discussion of the finite open-loop gain to low frequency. In the next section, we consider the effect of finite gain as well as the frequency response of the amplifier.

14.2.1 Inverting Amplifier Closed-Loop Gain

The equivalent circuit of the inverting amplifier with a finite open-loop gain is shown in Figure 14.2. If the open-loop input resistance is assumed to be infinite, then $i_1 = i_2$, or

$$\frac{v_I - v_1}{R_1} = \frac{v_1 - v_O}{R_2} \qquad \textbf{(14.1(a))}$$

Figure 14.2 Equivalent circuit, inverting amplifier with finite open-loop gain

or

$$\frac{v_I}{R_1} = v_1\left(\frac{1}{R_1} + \frac{1}{R_2}\right) - \frac{v_O}{R_2} \tag{14.1(b)}$$

Since $v_2 = 0$, the output voltage is

$$v_O = -A_{OL}v_1 \tag{14.2}$$

where A_{OL} is the low-frequency open-loop gain. Solving for v_1 from Equation (14.2) and substituting the result into Equation (14.1(b)), we find

$$\frac{v_I}{R_1} = -\left(\frac{v_O}{A_{OL}}\right)\left(\frac{1}{R_1} + \frac{1}{R_2}\right) - \frac{v_O}{R_2} \tag{14.3}$$

The closed-loop voltage gain is then

$$A_{CL} = \frac{v_O}{v_I} = \frac{-\dfrac{R_2}{R_1}}{1 + \dfrac{1}{A_{OL}}\left(1 + \dfrac{R_2}{R_1}\right)} \tag{14.4}$$

Example 14.1 **Objective:** Determine the minimum open-loop voltage gain to achieve a particular accuracy.

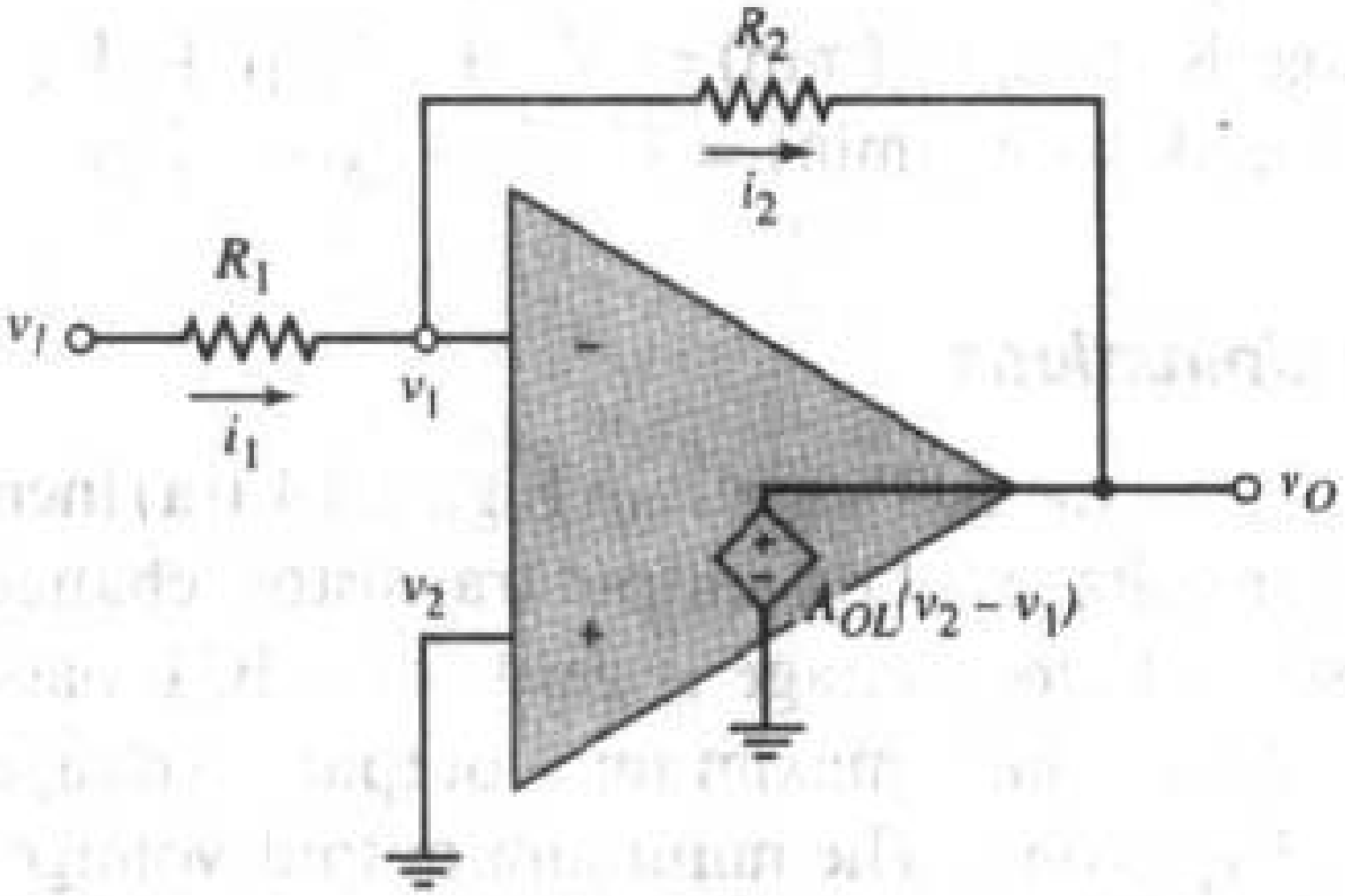
A pressure transducer produces a maximum dc voltage signal of 2 mV and has an output resistance of $R_S = 2\,\text{k}\Omega$. The maximum dc current from the transducer is to be limited to 0.2 μA. An inverting amplifier is to be used in conjunction with the transducer to produce an output voltage of −0.10 V for a 2 mV transducer signal. The error in the output voltage cannot be greater than 0.1 percent. Determine the minimum open-loop gain of the amplifier to meet this specification.

Solution: We must first determine the resistor values to be used in the inverting amplifier. The source resistor is in series with R_1, so let

$$R_1' = R_1 + R_S$$

The minimum input resistance is found from the maximum input current as

$$R_1'(\text{min}) = \frac{v_i}{i_i(\text{max})} = \frac{2 \times 10^{-3}}{0.2 \times 10^{6}} = 10 \times 10^{3}\,\Omega = 10\,\text{k}\Omega$$


R_2
i_2
R_1
v_I
i_1
v_1
v_O
v_2
$A_{OL}(v_2 - v_1)$

The resistor R_1 then needs to be 8 kΩ. The closed-loop voltage gain required is

$$A_{CL} = \frac{v_O}{v_i} = \frac{-0.10}{2 \times 10^{-3}} = -50 = \frac{-R_F}{R_1'}$$

The required value of the feedback resistor is then $R_F = 500\,\text{k}\Omega$.

For the voltage gain to be within 0.1 percent, the minimum gain (magnitude) is 49.95. Using Equation (14.4), we can determine the minimum value of the open-loop gain. We have

$$A_{CL} = \frac{\dfrac{-R_2}{R_1'}}{1 + \dfrac{1}{A_{OL}}\left(1 + \dfrac{R_2}{R_1'}\right)} = -49.95 = \frac{-50}{1 + \dfrac{1}{A_{OL}}(51)}$$

which yields $A_{OL}(\text{min}) = 50{,}949$.

Comment: If the open-loop gain is greater than the value of $A_{OL}(\text{min}) = 50{,}949$, then the error in the voltage gain will be less than 0.1 percent.

In the limit as $A_{OL} \to \infty$, the closed-loop gain is equal to the ideal value, designated $A_{CL}(\infty)$, which for the inverting amplifier is

$$A_{CL}(\infty) = -\frac{R_2}{R_1} \tag{14.5}$$

as previously determined. Equation (14.4) is then

$$A_{CL} = \frac{A_{CL}(\infty)}{1 + \dfrac{1 - A_{CL}(\infty)}{A_{OL}}} \tag{14.6}$$

To determine the variation in closed-loop gain with changes in open-loop gain, we take the derivative of A_{CL} with respect to A_{OL}. We find

$$\frac{dA_{CL}}{dA_{OL}} = \frac{A_{CL}(\infty)(1 - A_{CL}(\infty))}{[A_{OL} + (1 - A_{CL}(\infty))]^2} \tag{14.7}$$

which can be rearranged in the form

$$\frac{dA_{CL}}{A_{CL}} = \frac{dA_{OL}}{A_{OL}} \frac{\dfrac{1 - A_{CL}(\infty)}{A_{OL}}}{1 + \left(\dfrac{1 - A_{CL}(\infty)}{A_{OL}}\right)} \tag{14.8}$$

Normally, $A_{CL}(\infty)| \ll |A_{OL}|$ and Equation (14.8) is approximately

$$\frac{dA_{CL}}{A_{CL}} \cong \frac{dA_{OL}}{A_{OL}} \frac{1 - A_{CL}(\infty)}{A_{OL}} \tag{14.9}$$

Equation (14.9) relates the percent change in the closed-loop gain of the inverting amplifier as the result of a change in open-loop gain. Open-loop gain variations occur when individual transistor parameters change from one circuit to another or with temperature.

From Equation (14.9), we see that changes in closed-loop gain become smaller as the open-loop gain becomes larger.

Test Your Understanding

14.3 Consider an inverting amplifier in which the op-amp open-loop gain is $A_{OL} = 5 \times 10^4$ and the ideal closed-loop amplifier gain is $A_{CL}(\infty) = -50$. (a) Determine the actual closed-loop gain. (b) If the open-loop gain decreases by 10 percent, find the percent change in closed-loop gain and determine the actual closed-loop gain. (Ans. (a) $A_{CL} = -49.949$ (b) 0.0102%, $A_{CL} = -49.943$)

14.4 In an inverting amplifier, the resistors are $R_2 = 500\,\text{k}\Omega$ and $R_1 = 20\,\text{k}\Omega$. If the closed-loop gain must be within 0.1 percent of the ideal value, determine the minimum required open-loop op-amp gain. (Ans. $A_{OL} = 25{,}974$)

14.2.2 Noninverting Amplifier Closed-Loop Gain

Figure 14.3 shows the equivalent circuit of the noninverting amplifier with a finite open-loop gain. Again, the open-loop input differential resistance is assumed to be infinite. The analysis proceeds in much the same way as in the previous section. We have $i_1 = i_2$, and

$$-\frac{v_1}{R_1} = \frac{v_1 - v_O}{R_2} \tag{14.10(a)}$$

or

$$\frac{v_O}{R_2} = v_1\left(\frac{1}{R_1} + \frac{1}{R_2}\right) \tag{14.10(b)}$$

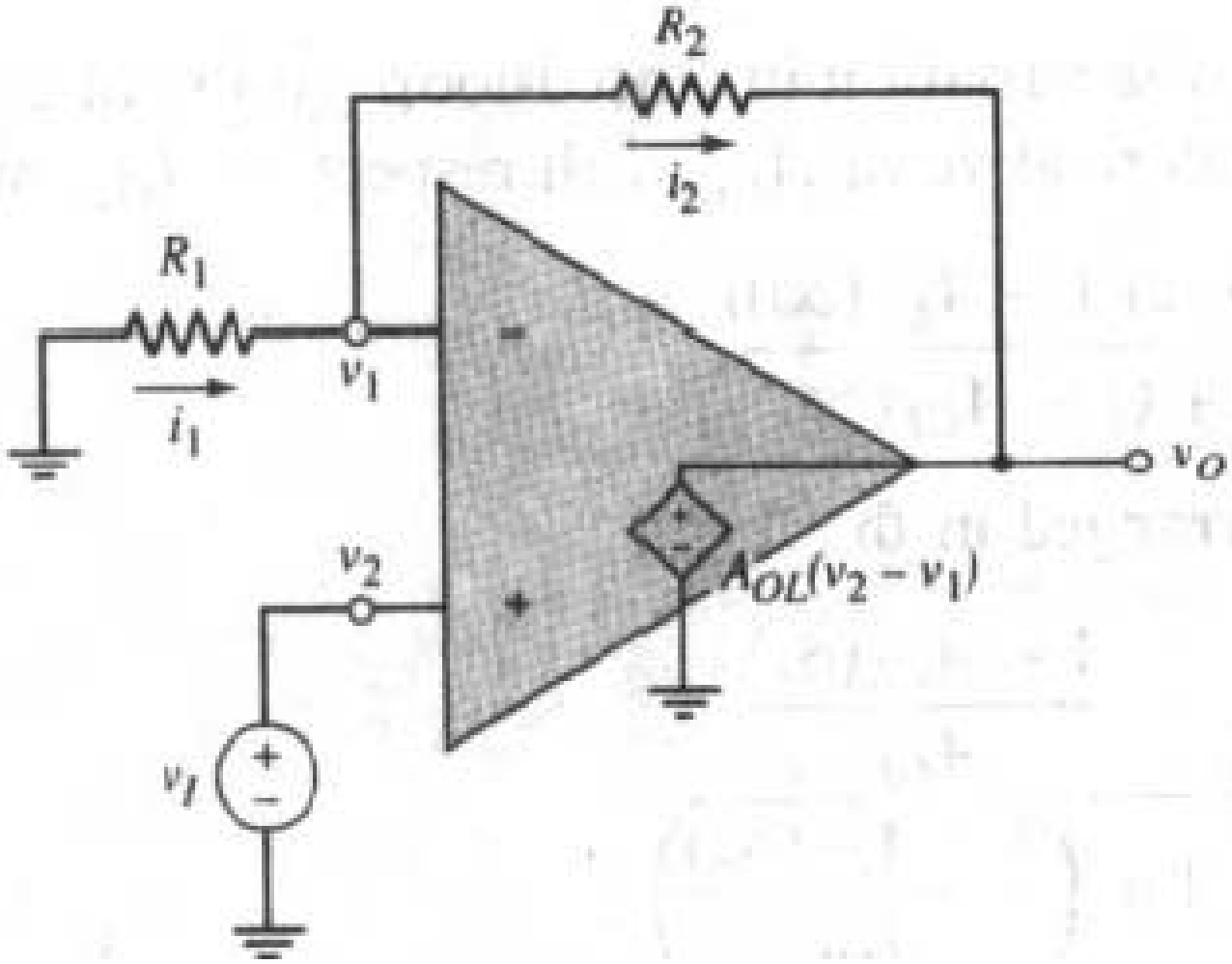
Figure 14.3 Equivalent circuit, noninverting amplifier with finite open-loop gain

The output voltage is

$$v_O = A_{OL}(v_2 - v_1) \tag{14.11}$$

Since $v_2 = v_I$, voltage v_1 can be written

$$v_1 = v_I - \frac{v_O}{A_{OL}} \tag{14.12}$$


R_2
i_2
R_1
i_1
v_1
v_2
v_I
v_O
$A_{OL}(v_2 - v_1)$

Combining Equations (14.12) and (14.10(b)) and rearranging terms, we have an expression for the closed-loop voltage gain:

$$A_{CL} = \frac{v_O}{v_I} = \frac{1 + \dfrac{R_2}{R_1}}{1 + \dfrac{1}{A_{OL}}\left(1 + \dfrac{R_2}{R_1}\right)} \tag{14.13}$$

In the limit as $A_{OL} \to \infty$, the ideal closed-loop gain is

$$A_{CL}(\infty) = 1 + \frac{R_2}{R_1} \tag{14.14}$$

and Equation (14.13) becomes

$$A_{CL} = \frac{A_{CL}(\infty)}{1 + \dfrac{A_{CL}(\infty)}{A_{OL}}} \tag{14.15}$$

Taking the derivative of the closed-loop gain with respect to the open-loop gain and rearranging terms, we obtain

$$\frac{dA_{CL}}{A_{CL}} = \frac{dA_{OL}}{A_{OL}}\left(\frac{A_{CL}}{A_{OL}}\right) \tag{14.16}$$

Equation (14.16) yields the fractional change in the closed-loop gain of the noninverting amplifier as a result of a change in the open-loop gain. The result for the noninverting amplifier is very similar to that for the inverting amplifier.

Test Your Understanding

14.5 An operational amplifier connected in a noninverting configuration has an open-loop gain of $A_{OL} = 10^5$. The resistors are $R_2 = 495\,\text{k}\Omega$ and $R_1 = 5\,\text{k}\Omega$. (a) Determine the actual and ideal closed-loop gains. (b) If the open-loop gain decreases by 10 percent, determine the percent change in closed-loop gain and the actual closed-loop gain. (Ans. (a) $A_{CL} = 99.90$, $A_{CL}(\infty) = 100$ (b) 0.01%, $A_{CL} = 99.89$)

14.6 A noninverting amplifier has an op-amp with an open-loop gain of $A_{OL} = 10^4$. The closed-loop gain must be within 0.1 percent of the ideal value. Determine the maximum closed-loop gain that will still meet the specification. (Ans. $A_{CL} = 10.0$)

14.2.3 Inverting Amplifier Closed-loop Input Resistance

The closed-loop input resistance R_{if} of the inverting amplifier is defined in Figure 14.4(a), and it includes the effect of feedback. The equivalent circuit, including a finite open-loop gain A_{OL}, finite open-loop input differential resistance R_i, and nonzero output resistance R_o, is shown in Figure 14.4(b).

A KCL equation at the output node yields

$$\frac{v_O}{R_L} + \frac{v_O - (-A_{OL}v_I)}{R_o} + \frac{v_o - v_1}{R_2} = 0 \tag{14.17}$$

(a) (b)

Figure 14.4 (a) Inverting amplifier and (b) inverting amplifier equivalent circuit, for calculating closed-loop input resistance

Solving for the output voltage, we have

$$v_O = \frac{-v_1\left(\dfrac{A_{OL}}{R_o} - \dfrac{1}{R_2}\right)}{\dfrac{1}{R_L} + \dfrac{1}{R_o} + \dfrac{1}{R_2}} \tag{14.18}$$

A KCL equation at the input node yields

$$i_1 = \frac{v_1}{R_i} + \frac{v_1 - v_O}{R_2} \tag{14.19}$$

Combining Equations (14.18) and (14.19) and rearranging terms produces

$$\frac{i_1}{v_1} = \frac{1}{R_{if}} = \frac{1}{R_i} + \frac{1}{R_2}\,\frac{1 + A_{OL} + \dfrac{R_o}{R_L}}{1 + \dfrac{R_o}{R_L} + \dfrac{R_o}{R_2}} \tag{14.20}$$

Equation (14.20) describes the closed-loop input resistance of the inverting amplifier, with a finite open-loop gain, finite open-loop input resistance, and nonzero output resistance. In the limit as $A_{OL} \to \infty$, we see that $1/R_{if} \to \infty$, or $R_{if} \to 0$, which means that $v_1 \to 0$, or v_1 is at virtual ground. This is a characteristic of an ideal inverting op-amp.

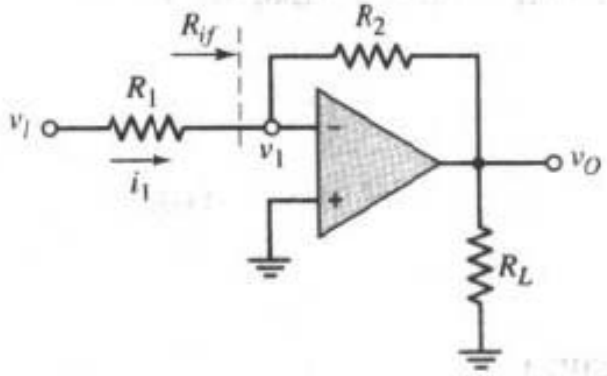
Example 14.2 **Objective:** Determine the closed-loop input resistance at the inverting terminal of an inverting amplifier.

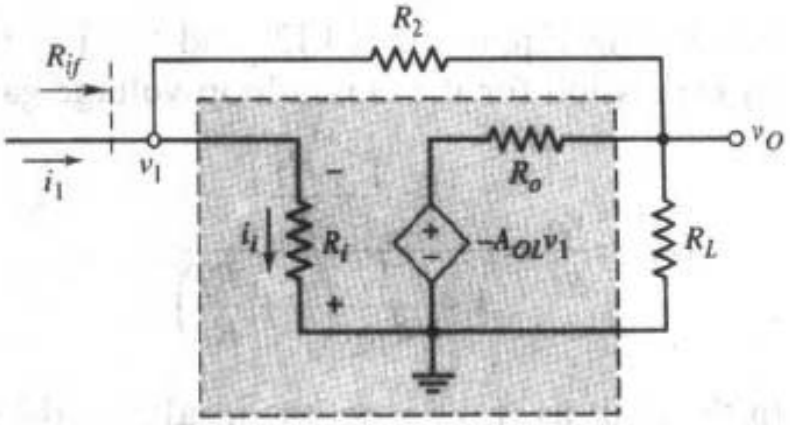
Consider an inverting amplifier with a feedback resistor $R_2 = 10\,\text{k}\Omega$, and an op-amp with parameters $A_{OL} = 10^5$ and $R_i = 10\,\text{k}\Omega$. Assume the output resistance R_o of the op-amp is negligible.

Solution: If $R_o = 0$, then Equation (14.20) becomes

$$\frac{1}{R_{if}} = \frac{1}{R_i} + \frac{1 + A_{OL}}{R_2} = \frac{1}{10^4} + \frac{1 + 10^5}{10^4} \cong 10^{-4} + 10 \tag{14.21}$$

The closed-loop input resistance is then $R_{if} \cong 0.1\,\Omega$.


R_{if}
R_2
R_1
v_I
i_1
v_1
v_O
R_L


R_2
R_{if}
v_O
i_1
v_1
R_o
i_i
R_i
$-A_{OL}v_1$
R_L

Comment: The closed-loop input resistance of the inverting amplifier is a very strong function of the finite open-loop gain. Equation (14.21) shows that the open-loop input resistance R_i essentially does not affect the closed-loop input resistance.

A nonzero closed-loop input resistance R_{if} in conjunction with a finite open-loop input resistance R_i implies that the signal current into the op-amp is not zero, as assumed in the ideal case. From Figure 14.4(b), we see that

$$v_1 = i_1 R_{if} \tag{14.22}$$

Therefore,

$$i_i = \frac{v_1}{R_i} = i_1\left(\frac{R_{if}}{R_i}\right) \tag{14.23}$$

The fraction of input signal current shunted away from R_2 and into the op-amp is (R_{if}/R_i).

Test Your Understanding

14.7 Determine the closed-loop input resistance at the inverting terminal of an inverting amplifier if $A_{OL} = 10^4$, $R_2 = R_i = R_L = 10\,\text{k}\Omega$, and if: (a) $R_o = 0$, and (b) $R_o = 10\,\text{k}\Omega$. (Ans. (a) $R_{if} = 1\,\Omega$ (b) $R_{if} = 3\,\Omega$)

14.8 Consider the equivalent circuit in Figure 14.4(b). If $R_i = 10\,\text{k}\Omega$, determine the percentage of input signal current i_1 shunted from R_2 for: (a) $R_{if} = 0.1\,\Omega$, and (b) $R_{if} = 10\,\Omega$. (Ans. (a) $10^{-3}\%$ (b) 0.1%)

14.2.4 Noninverting Amplifier Closed-Loop Input Resistance

A noninverting amplifier is shown in Figure 14.5(a). The input resistance seen by the signal source is designated R_{if}. The equivalent circuit, including a finite

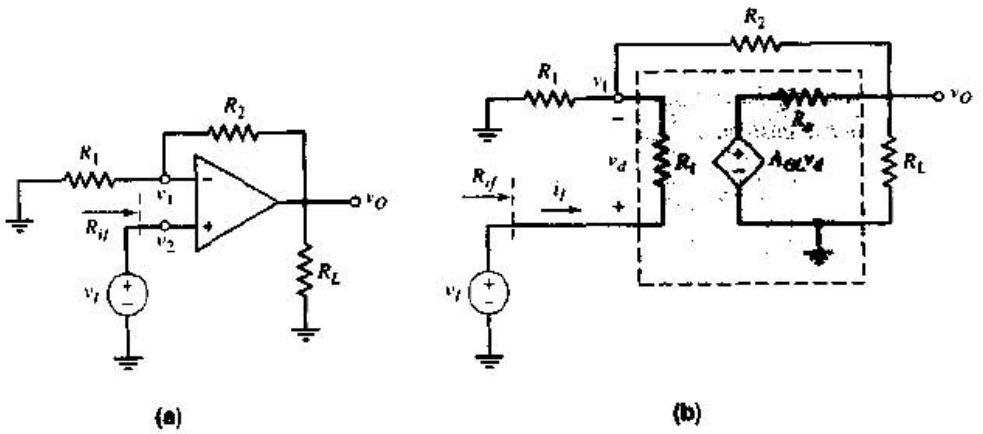


Figure 14.5 (a) Noninverting amplifier and (b) noninverting amplifier equivalent circuit, for calculating closed-loop input resistance

open-loop gain A_{OL}, finite open-loop input differential resistance R_i and nonzero output resistance R_o, is shown in Figure 14.5(b).

Writing a KCL equation at the output node yields

$$\frac{v_O}{R_L} + \frac{v_O - A_{OL}v_d}{R_o} + \frac{v_O - v_1}{R_2} = 0 \tag{14.24}$$

Solving for the output voltage, we have

$$v_O = \frac{\dfrac{v_1}{R_2} + \dfrac{A_{OL}v_d}{R_o}}{\dfrac{1}{R_L} + \dfrac{1}{R_o} + \dfrac{1}{R_2}} \tag{14.25}$$

A KCL equation at the v_1 node yields

$$i_I = \frac{v_1}{R_1} + \frac{v_1 - v_O}{R_2} \tag{14.26}$$

Combining Equations (14.25) and (14.26) and rearranging terms, we obtain

$$i_I\left(1 + \frac{R_o}{R_L} + \frac{R_o}{R_2}\right) = v_1\left\{\left(\frac{1}{R_1} + \frac{1}{R_2}\right)\left(1 + \frac{R_o}{R_L} + \frac{R_o}{R_2}\right) - \frac{R_o}{R_2^2}\right\} - \frac{A_{OL}v_d}{R_2} \tag{14.27}$$

From Figure 14.5(b), we see that

$$v_d = i_i R_i \tag{14.28}$$

and

$$v_1 = v_I - i_I R_i \tag{14.29}$$

Substituting Equations (14.28) and (14.29) into (14.27) we obtain an equation in i_I and v_I so that the input resistance R_{if} can be found as

$$R_{if} = v_I / i_I$$

In order to simplify the algebra, we neglect the effect of R_o, which is normally small. Setting $R_o = 0$ reduces Equation (14.27) to

$$i_I = v_1\left(\frac{1}{R_1} + \frac{1}{R_2}\right) - \frac{A_{OL}v_d}{R_2} \tag{14.30}$$

Substituting Equations (14.28) and (14.29) into (14.30), we find that the input resistance can be written in the form

$$R_{if} = \frac{v_I}{i_I} = \frac{R_i(1 + A_{OL}) + R_2\left(1 + \dfrac{R_i}{R_1}\right)}{1 + \dfrac{R_2}{R_1}} \tag{14.31}$$

Equation (14.31) describes the closed-loop input resistance of the noninverting amplifier with a finite open-loop gain and a finite open-loop input resistance. In the limit as $A_{OL} \to \infty$, or as the open-loop input resistance approaches infinity, we see that $R_{if} \to \infty$, which is a property of the ideal noninverting amplifier.

Example 14.3 **Objective:** Determine the closed-loop input resistance at the noninverting terminal of a noninverting amplifier.

Consider an op-amp with an open-loop gain of $A_{OL} = 10^5$ and an input resistance of $R_i = 10\,\text{k}\Omega$ in a noninverting amplifier configuration with resistor values of $R_1 = R_2 = 10\,\text{k}\Omega$.

Solution: From Equation (14.31), the input resistance is

$$R_{if} = \frac{R_i(1 + A_{OL}) + R_2\left(1 + \dfrac{R_i}{R_1}\right)}{1 + \dfrac{R_2}{R_1}} = \frac{10(1 + 10^5) + 10\left(1 + \dfrac{10}{10}\right)}{1 + \dfrac{10}{10}} \tag{14.32}$$

or

$$R_{if} \cong 5 \times 10^5\,\text{k}\Omega \Rightarrow 500\,\text{M}\Omega$$

Comment: As expected, the closed-loop input resistance of the noninverting amplifier is very large. Equation (14.32) shows that the input resistance is dominated by the term $R_i(1 + A_{OL})$. The combination of a large R_i and large A_{OL} produces an extremely large input resistance, as predicted by ideal feedback theory.

Test Your Understanding

14.9 For a noninverting amplifier, the resistances are $R_2 = 99\,\text{k}\Omega$ and $R_1 = 1\,\text{k}\Omega$. The op-amp properties are: $A_{OL} = 10^4$, $R_i = 40\,\text{k}\Omega$, and $R_o = 0$. Determine the closed-loop input resistance. (Ans. $R_{if} = 4.04\,\text{M}\Omega$)

14.10 Find the closed-loop input resistance of a voltage follower with op-amp characteristics $A_{OL} = 5 \times 10^5$, $R_i = 10\,\text{k}\Omega$, and $R_o = 0$. (Ans. $R_{if} = 5000\,\text{M}\Omega$)

14.2.5 Nonzero Output Resistance

Since the ideal op-amp has a zero output resistance, the output voltage is independent of the load impedance. The op-amp acts as an ideal voltage source and there is no loading effect. An actual op-amp circuit has a nonzero output resistance, which means that the output voltage, and therefore the closed-loop gain, is a function of the load impedance.

Figure 14.6 is the equivalent circuit of both an inverting and noninverting amplifier and is used to find the output resistance. The op-amp has a finite open-loop gain A_{OL}, a nonzero output resistance R_o, and an infinite input resistance R_i. To determine the output resistance, we set the independent input voltages equal to zero. A KCL equation at the output node yields

$$i_o = \frac{v_o - A_{OL}v_d}{R_o} + \frac{v_o}{R_1 + R_2} \tag{14.33}$$

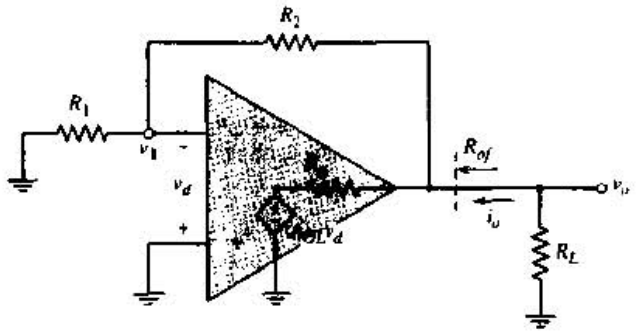


Figure 14.6 Equivalent circuit for calculating closed-loop output resistance

The differential input voltage is $v_d = -v_1$, where

$$v_1 = \left(\frac{R_1}{R_1 + R_2}\right) v_o \tag{14.34}$$

Combining Equations (14.34) and (14.33), we have

$$i_o = \frac{v_o}{R_o} - \frac{A_{OL}}{R_o}\left[-\left(\frac{R_1}{R_1 + R_2}\right) v_o\right] + \frac{v_o}{R_1 + R_2} \tag{14.35(a)}$$

or

$$\frac{i_o}{v_o} = \frac{1}{R_{of}} = \frac{1}{R_o}\left[1 + \frac{A_{OL}}{(1 + R_2/R_1)}\right] + \frac{1}{R_1 + R_2} \tag{14.35(b)}$$

Since R_o is normally small and A_{OL} is normally large, Equation (14.35b), to a good approximation, is as follows:

$$\frac{1}{R_{of}} \cong \frac{1}{R_o}\left[\frac{A_{OL}}{1 + R_2/R_1}\right] \tag{14.36}$$

In most op-amp circuits, the open-loop output resistance R_o is on the order of 100 Ω. Since A_{OL} is normally much larger than $(1 + R_2/R_1)$, the closed-loop output resistance can be very small. Output resistance values in the milliohm range are easily attained.

Example 14.4 **Objective:** Determine the output resistance of an op-amp circuit.

Computer Simulation Solution: Figure 14.7 shows an inverting amplifier circuit with a standard 741 op-amp. One method of determining the output resistance is to measure the output voltage for two different values of load resistance connected to the output. Then, treating the amplifier as a Thevenin equivalent circuit with a fixed source in series with an output resistance, the output resistance can be determined. A 1 mV signal was applied. For a 10 Ω load, the output voltage is 0.999837 mV, and for a 20 Ω load, the output voltage is 0.9999132 mV. This gives an output resistance of 1.53 mΩ.

Comment: As mentioned, the output resistance of a voltage amplifier with negative feedback can be very small. The ideal output resistance is zero, but a practical op-amp circuit can have an output resistance in the milliohm range.

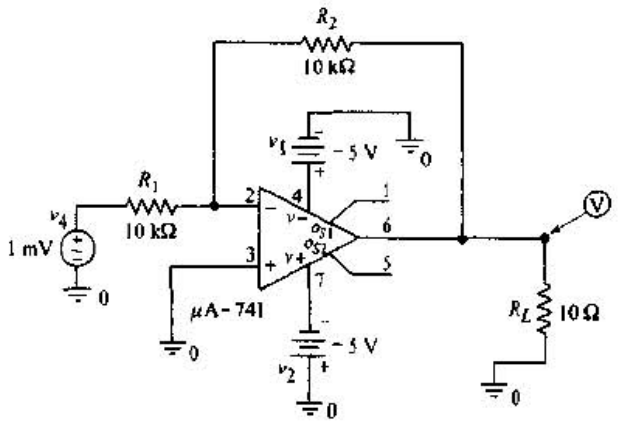


Figure 14.7 Circuit using 741 op-amp to measure output resistance

Test Your Understanding

14.11 An op-amp with an open-loop gain of $A_{OL} = 10^5$ is used in a noninverting amplifier configuration with a closed-loop gain of $A_{CL} = 100$. Determine the closed-loop output resistance R_{of} for: (a) $R_o = 100\,\Omega$, and (b) $R_o = 10\,\text{k}\Omega$. (Ans. (a) $R_{of} = 01.\,\Omega$ (b) $R_{of} = 10\,\Omega$)

14.3 FREQUENCY RESPONSE

In the last chapter, we considered the basic op-amp frequency response. Frequency compensation was included as a means of stabilizing the circuit. In this section, we will consider the bandwidth and the transient response of the closed-loop amplifier.

When a step function is applied at the op-amp input, the output voltage cannot change instantaneously with time because of capacitance effects within the op-amp circuit. The maximum rate at which the output changes with time is called the **slew rate**. We will determine the factors that limit the slew rate.

14.3.1 Open-Loop and Closed-Loop Frequency Response

The frequency response of the open-loop gain can be written as

$$A_{OL}(f) = \frac{A_O}{1 + j\dfrac{f}{f_{PD}}} \tag{14.37}$$

where A_O is the low-frequency open-loop gain and f_{PD} is the dominant-pole frequency. Figure 14.8 shows the Bode plot of the open-loop gain magnitude. The dominant-pole frequency f_{PD} is shown as well as the unity-gain bandwidth f_T. We showed previously that the unity-gain bandwidth is

$$f_T = f_{PD}A_O \tag{14.38}$$

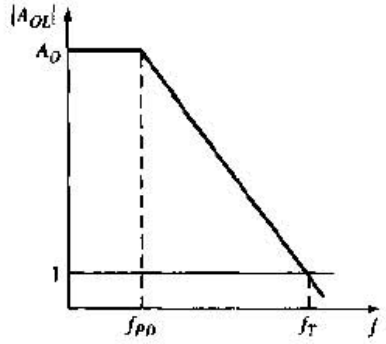


Figure 14.8 Bode plot, open-loop gain magnitude

and is also called the gain–bandwidth product. Equation (14.38) assumes that additional poles of the open-loop frequency response occur at higher frequencies than f_T.

Figure 14.9 shows a noninverting amplifier. In our discussion on feedback theory in Chapter 12, we found that, assuming ideal feedback, the closed-loop gain A_{CL} can be written

$$A_{CL} = \frac{A_{OL}}{(1 + \beta A_{OL})} \tag{14.39}$$

where β is the feedback transfer function. For the noninverting amplifier, this feedback transfer function is

$$\beta = \frac{1}{1 + \dfrac{R_2}{R_1}} \tag{14.40}$$

Combining Equations (14.37), (14.40) and (14.39), we find the expression

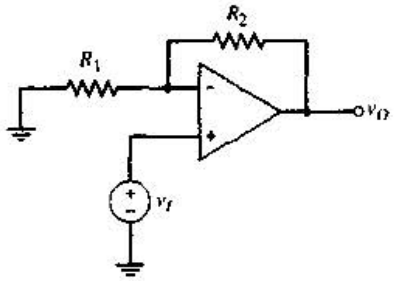


Figure 14.9 Noninverting amplifier

for the closed-loop gain as a function of frequency, as follows:

$$A_{CL}(f) = \frac{A_O}{1 + \dfrac{A_O}{1 + (R_2/R_1)}} \times \frac{1}{1 + j\dfrac{f}{f_{PD}\left[1 + \dfrac{A_O}{1 + (R_2/R_1)}\right]}} \tag{14.41}$$

Normally, $A_O \gg [1 + (R_2/R_1)]$; therefore, the low-frequency closed-loop gain is

$$A_{CLO} = 1 + \frac{R_2}{R_1} \tag{14.42}$$

as previously determined. For $A_O \gg A_{CLO}$, Equation (14.41) is approximately

$$A_{CL}(f) = \frac{A_{CLO}}{1 + j\dfrac{f}{f_{PD}\left(\dfrac{A_O}{A_{CLO}}\right)}} \tag{14.43}$$

The 3 dB frequency, or small-signal bandwidth, is then

$$f_{3\text{dB}} = f_{PD}\left(\frac{A_O}{A_{CLO}}\right) \tag{14.44}$$

Since in most cases $A_O \gg A_{CLO}$, the bandwidth of the closed-loop system is substantially larger than the open-loop dominant-pole frequency f_{PD}. Note also that Equation (14.44) applies to the inverting, as well as the noninverting, amplifier in which A_{CLO} is the magnitude of the closed-loop gain. We have seen this same bandwidth extension for negative feedback several times previously.

14.3.2 Gain–Bandwidth Product

We can also determine the unity-gain bandwidth of the closed-loop system. From Equation (14.43), we can write

$$|A_{CL}(f = f_{\text{unity}})| = 1 = \frac{A_{CLO}}{\sqrt{1 + \left[\dfrac{f_{\text{unity}}}{f_{PD}(A_O/A_{CLO})}\right]^2}} \tag{14.45}$$

where f_{unity} is the unity-gain frequency of the closed-loop system.

If $A_{CLO} \gg 1$, then Equation (14.45) yields

$$\frac{f_{\text{unity}}}{f_{PD}\left(\dfrac{A_O}{A_{CLO}}\right)} \cong A_{CLO} \tag{14.46(a)}$$

which reduces to

$$f_{\text{unity}} = A_{CLO} f_{PD}\left(\frac{A_O}{A_{CLO}}\right) = f_{PD} A_O = f_T \tag{14.46(b)}$$

The unity-gain frequency or bandwidth of the closed-loop system is essentially the same as that of the open-loop amplifier.

The open-loop and closed-loop frequency response curves are shown in Figure 14.10. We observed these same results in Chapter 12 in the discussion on ideal feedback theory.

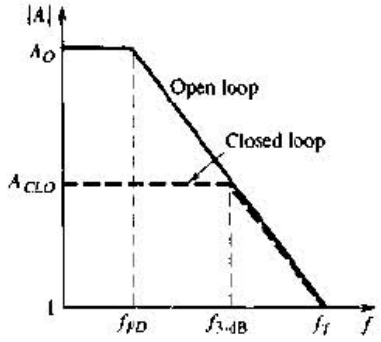


Figure 14.10 Bode plot, open-loop and closed-loop gain magnitude

Example 14.5 **Objective:** Determine the unity-gain bandwidth and the maximum closed-loop gain for a specified closed-loop bandwidth.

An audio amplifier system is to use an op-amp with an open-loop gain of $A_O = 2 \times 10^5$ and a dominant-pole frequency of 5 Hz. The bandwidth of the audio system is to be 20 kHz. Determine the maximum closed-loop gain for the audio amplifier.

Solution: The unity-gain bandwidth is found as

$$f_T = f_{PD}A_O = (5)(2 \times 10^5) = 10^6 \text{ Hz} \Rightarrow 1 \text{ MHz}$$

Since the gain–bandwidth product is a constant, we have

$$f_{3\text{-dB}} \cdot A_{CL} = f_T$$

where $f_{3\text{-dB}}$ is the closed-loop bandwidth and A_{CL} is the closed-loop gain. The maximum closed-loop gain is then

$$A_{CL} = \frac{f_T}{f_{3\text{-dB}}} = \frac{10^6}{20 \times 10^3} = 50$$

Comment: If the closed-loop gain is less than or equal to 50, then the required bandwidth of 20 kHz for the audio amplifier will be realized.

Test Your Understanding

14.12 An op-amp with open-loop parameters of $A_{OL} = 10^4$ and $f_{PD} = 50$ Hz is connected in a noninverting amplifier configuration with a low-frequency closed-loop gain of $A_{CLO} = 25$. If an input voltage of $v_I = 50 \sin(2\pi ft)\,\mu$V is applied, determine the output voltage peak amplitude for: (a) $f = 2$ kHz, (b) $f = 20$ kHz, and (c) $f = 100$ kHz. (Ans. (a) 1.25 mV (b) 0.884 mV (c) 0.245 mV)

14.3.3 Slew Rate

Implicit in the frequency response analysis for the closed-loop amplifier is the assumption that the sinusoidal input signals are small. If a large sinusoidal signal or step function is applied to an op-amp circuit, the input stage can be overdriven and the small-signal model will no longer apply.

Figure 14.11 shows a simplified op-amp circuit. If a large step voltage (greater than 120 mV) is applied at v_2 with v_1 held at ground potential, then Q_2 is effectively cut off, which means $i_{C2} \cong 0$ and $i_{C1} \cong I_Q$. The entire bias current is switched to Q_1. Since $i_{C3} \cong i_{C1}$, then $i_{C3} \cong I_Q$; since Q_3–Q_4 form a current mirror, then we also have $i_{C4} \cong I_Q$.

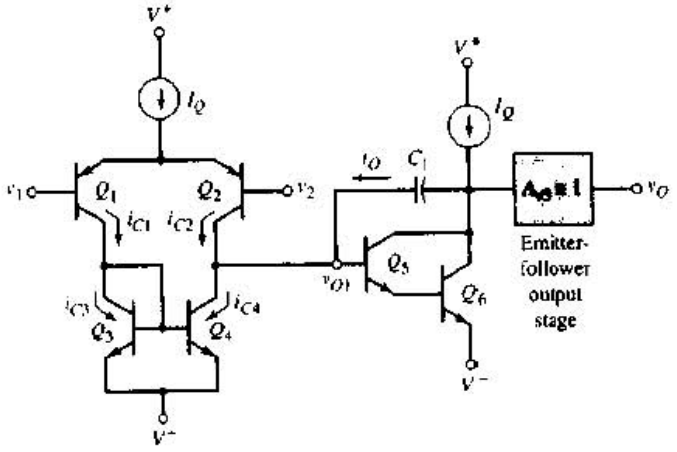


Figure 14.11 Simplified op-amp for calculating slew rate

The base current into Q_5 is very small; therefore, the current through the compensation capacitor C_1 is $i_O \cong i_{C4} = I_Q$. Since the voltage gain of the emitter-follower output stage is essentially unity, the capacitor current can be written as

$$i_O = C_1 \frac{d(v_O - v_{O1})}{dt} \tag{14.47}$$

The gain of the second stage is large, which means that $v_{O1} \ll v_O$. Equation (14.47) then becomes

$$i_O \cong C_1 \frac{dv_O}{dt} = I_Q \tag{14.48}$$

or

$$\frac{dv_O}{dt} = \frac{I_Q}{C_1} \tag{14.49}$$

The maximum current through the compensation capacitor is limited to the bias current I_Q; consequently, the maximum rate at which the output voltage can change is also limited by the bias current I_Q.

The maximum rate of change of the output voltage is the slew rate of the op-amp, the units of which are usually given as volts per microsecond. From Equation (14.49), we have

$$\text{Slew rate (SR)} = \left(\frac{dv_O}{dt}\right)_{\max} = \frac{I_Q}{C_1} \tag{14.50}$$

Although the rate of change in output voltage can be either positive or negative, the slew rate is ***defined*** as a positive quantity.

Figure 14.12 shows the slew-rate limited response of an op-amp voltage follower to a rectangular input voltage pulse. Note the trapezoidal shaped output response. The time needed to reach the full-scale response is approximately $V_O(\text{max})/\text{SR}$.

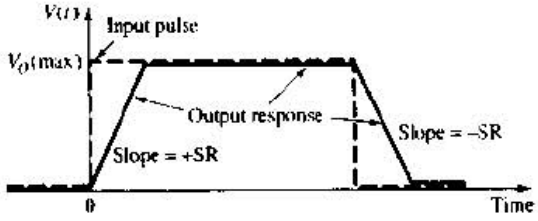


Figure 14.12 Slew-rate-limited response of voltage follower to rectangular input voltage pulse

Example 14.6 **Objective:** Calculate the slew rate of the 741 op-amp.

From the previous chapter, the bias current in the 741 op-amp is $I_Q = 19\,\mu\text{A}$ and the internal frequency compensation capacitor is $C_1 = 30\,\text{pF}$.

Solution: From Equation (14.50), the slew rate is

$$\text{SR} = \frac{I_Q}{C_1} = \frac{19 \times 10^{-6}}{30 \times 10^{-12}} = 0.63 \times 10^6\ \text{V/s} \Rightarrow 0.63\ \text{V/}\mu\text{s}$$

Comment: The partial data sheet in Table 14.1 for the 741 op-amp lists the typical slew rate as 0.7 V/μs, which is in close agreement with our calculated value.

Typical slew-rate values for the CA3140 BiCMOS and LH0042C BiFET op-amps are also given in Table 14.1. The BiCMOS circuit has a typical slew rate of 9 V/μs, and the BiFET op-amp has a typical value of 3 V/μs. The slew rates are larger in the FET op-amps because the bias currents are larger than in the 741 circuit and the gain of the FET input stage is smaller than that of the 741 input stage.

The slew rate is directly related to the unity-gain bandwidth. To explain, the unity-gain bandwidth is directly proportional to the dominant-pole frequency, or $f_T \propto f_{PD}$. In turn, the dominant-pole frequency is inversely proportional to $R_{eq}C_1$, where R_{eq} is the equivalent resistance at the node of the second stage input and C_1 is the compensation capacitance. The equivalent resistance R_{eq} is a function of the second stage input resistance and the diff-amp stage output resistance, both of which are inversely proportional to I_Q. Then,

$$f_T \propto f_{PD} \propto \frac{1}{R_{eq}C_1} \propto \frac{1}{\left(\frac{1}{I_Q}\right)C_1} \propto \frac{I_Q}{C_1} \tag{14.51}$$

where I_Q/C_1 is the slew rate. Equation (14.51) shows that the slew rate is directly proportional to the unity-gain bandwidth.

Now consider what happens when a sinosoidal input signal is applied, for example, to the noninverting amplifier shown in Figure 14.9. If $v_I = V_p \sin \omega t$, then

$$v_O(t) = V_p\left(1 + \frac{R_2}{R_1}\right) \sin \omega t = V_{po} \sin \omega t \tag{14.52}$$

where V_{po} is the ideal peak value of the sinusoidal output voltage.

The rate at which the output voltage changes is

$$\frac{dv_O(t)}{dt} = \omega V_{po} \cos \omega t \tag{14.53}$$

Therefore, the maximum rate of change is ωV_{po}. Figure 14.13 shows two sinusoidal waveforms of the same frequency but different peak amplitudes. The maximum rate of change, or slope, occurs as the curves cross the zero axis. The waveform with the larger peak value has a larger maximum slope. Curve *a* in Figure 14.13 has a maximum slope corresponding to the slew rate; curve *b*, with a smaller peak value, has a maximum slope less than the slew rate. If the maximum slope, ωV_{po}, is greater than the slew rate SR, then the op-amp is slew-rate-limited and the output signal is distorted.

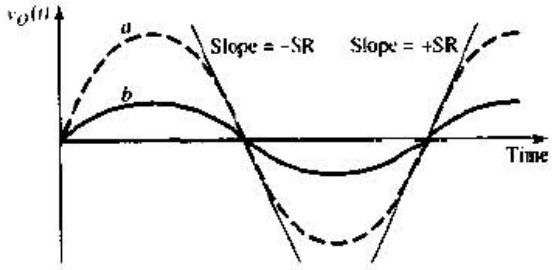


Figure 14.13 Two sinusoidal waveforms of the same frequency with different peak voltages, showing different maximum slopes

Thus, the maximum frequency at which the op-amp can operate without being slew-rate-limited is a function of both the frequency and peak amplitude of the signal. We have that

$$\omega_{max} V_{po} = 2\pi f_{max} V_{po} = \text{SR} \tag{14.54(a)}$$

or

$$f_{max} = \frac{\text{SR}}{2\pi V_{po}} \tag{14.54(b)}$$

As the output voltage peak amplitude increases, the maximum frequency at which slew-rate-limiting occurs decreases. The **full-power bandwidth (FPBW)** is the frequency at which the op-amp output becomes slew-rate-limited. The FPBW is the f_{max} frequency from Equation (14.54(b)), or

$$\text{FPBW} = \frac{\text{SR}}{2\pi V_{po}} \tag{14.55}$$

The full-power bandwidth can be considerably less than the small-signal bandwidth.

Example 14.7 **Objective:** Determine the small-signal bandwidth of an amplifier and the full-power bandwidth that will produce an undistorted output voltage.

Consider an amplifier with a unity-gain bandwidth of $f_T = 1\,\text{MHz}$ and a low-frequency closed-loop gain of $A_{CLO} = 10$. Assume the op-amp slew rate is $\text{SR} = 1\,\text{V}/\mu\text{s}$ and the desired peak output voltage is $V_{po} = 10\,\text{V}$.

Solution: The small-signal closed-loop bandwidth is, from Equation (14.44),

$$f_{3\text{-dB}} = \frac{f_T}{A_{CLO}} = \frac{10^6}{10} \Rightarrow 100\,\text{kHz}$$

The full-power bandwidth, based on slew-rate limitation, from Equations (14.54(b)) and (14.55), is

$$f_{\max} = \text{FPBW} = \frac{\text{SR}}{2\pi V_{po}} = \frac{(1\,\text{V}/\mu\text{s})(10^6\,\mu\text{s/s})}{2\pi(10)} \Rightarrow 15.9\,\text{kHz}$$

Comment: The full-power bandwidth, or the actual maximum frequency at which the system can be operated and still produce a large, undistorted output signal, is considerably smaller than the bandwidth under small-signal nonslew-rate-limiting conditions.

Test Your Understanding

14.13 A 1 V input step function is applied to a noninverting amplifier with a closed-loop gain of 5. The slew rate of the op-amp is $2\,\text{V}/\mu\text{s}$. Determine the time needed for the output voltage to reach its full-scale response. (Ans. $2.5\,\mu\text{s}$)

14.14 For a 741 op-amp with a slew rate of $0.63\,\text{V}/\mu\text{s}$, find the full-power bandwidth for a peak undistorted output voltage of: (a) 1 V, and (b) 10 V. (Ans. (a) 100 kHz (b) 10 kHz)

14.15 An op-amp with a low-frequency open-loop gain of $A_{OL} = 10^5$ and a dominant-pole frequency of $f_{PD} = 10\,\text{Hz}$ is used in a noninverting amplifier configuration with a low-frequency closed-loop gain of $A_{CLO} = 50$. The slew rate of the op-amp is $0.8\,\text{V}/\mu\text{s}$. Determine the maximum undistorted output voltage amplitude such that $f_{\max} = f_{3\text{-dB}}$. (Ans. 6.37 V)

14.4 OFFSET VOLTAGE

In Chapter 11, we analyzed the basic difference amplifier, which is the input stage of the op-amp. In that analysis, we assumed the input differential-pair transistors to be identical, or matched. If the two input devices are mismatched, the currents in the two branches of the diff-amp are unequal and this affects the diff-amp dc output voltage. In fact, the internal circuitry of the entire op-amp usually contains imbalances and asymmetries, all of which can cause a nonzero output voltage for a zero input differential voltage.

The **output dc offset voltage** is the measured open-loop output voltage when the input voltage is zero. This configuration is shown in Figure 14.14. The **input dc offset voltage is defined as the input differential voltage that must be applied to the open-loop op-amp to produce a zero output voltage.** This

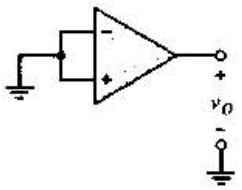


Figure 14.14 Circuit for measuring output offset voltage

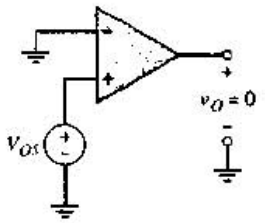


Figure 14.15 Circuit for measuring input offset voltage

configuration is shown in Figure 14.15. The input offset voltage is the parameter most often specified and is usually referred to simply as the offset voltage.

Offset voltage values have a statistical distribution among op-amps of the same type, and the offset voltage polarity may vary from one op-amp to another. The offset voltage specification for an op-amp is the magnitude of the maximum offset voltage for a particular type of op-amp. The offset voltage is a dc value, generally in the range of 1–2 mV for bipolar op-amps, although some op-amps may have offset voltages in the range of 5–10mV. Further, the maximum offset voltage specification for a precision op-amp may be as low as 10 μV.

In this section we will analyze offset voltage effects in the input diff-amp stage and will then consider various techniques used to compensate for offset voltage.

14.4.1 Input Stage Offset Voltage Effects

Several possible mismatches in the input diff-amp stage can produce offset voltages. We will analyze offset voltage effects in two bipolar input stages and in a MOSFET input diff-amp circuit.

Basic Bipolar Diff-Amp Stage

A basic bipolar diff-amp is shown in Figure 14.16. The differential pair is biased with a constant-current source. If Q_1 and Q_2 are matched, then for $v_1 = v_2 = 0$, I_Q splits evenly between the two transistors and $i_{C1} = i_{C2}$. If a two-sided output is defined as the difference in voltage between the two collector terminals, then $v_O = 0$ when the transistors are matched and the collector resistors are matched, which means that the offset voltage is zero.

The collector currents can be written as

$$i_{C1} = I_{S1} e^{v_{BE1}/V_T} \tag{14.56(a)}$$

and

$$i_{C2} = I_{S2} e^{v_{BE2}/V_T} \tag{14.56(b)}$$

where I_{S1} and I_{S2} are related to the reverse-saturation currents in the B–E junctions and are functions of the electrical and geometric transistor properties. If the two transistors are exactly matched, then $I_{S1} = I_{S2}$; if there is any mismatch in the electrical or geometric parameters, then $I_{S1} \neq I_{S2}$.

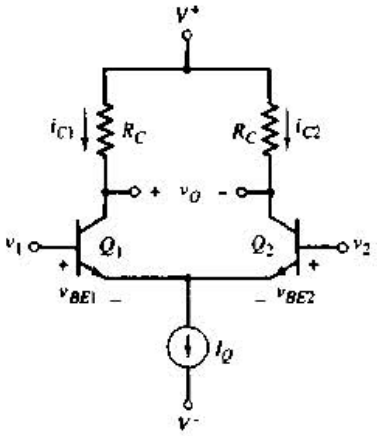


Figure 14.16 Basic bipolar difference amplifier

The input offset voltage is defined as the input differential voltage required to produce a zero output voltage, or in this case to produce $i_{C1} = i_{C2}$. Figure 14.17 shows the i_C versus v_{BE} characteristics of two unmatched transistors. Slightly different B–E voltages must be applied to produce equal collector currents that will result in a zero output voltage in the diff-amp.

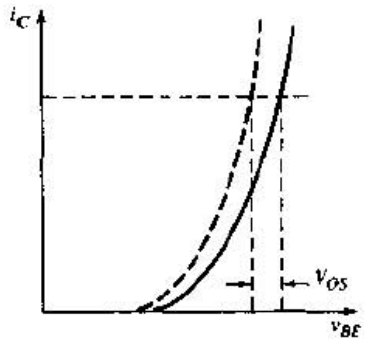


Figure 14.17 The i_C versus v_{BE} characteristics for two unmatched bipolar transistors

For $i_{C1} = i_{C2}$, we have

$$I_{S1}e^{v_{BE1}/V_T} = I_{S2}e^{v_{BE2}/V_T} \tag{14.57}$$

or

$$e^{(v_{BE1}-v_{BE2})/V_T} = \frac{I_{S2}}{I_{S1}} \tag{14.58}$$

We define the offset voltage as

$$v_{BE1} - v_{BE2} \equiv V_{OS}$$

Since $v_1 - v_2 = v_{BE1} - v_{BE2}$, then the offset voltage V_{OS} is the differential input voltage that must be applied to produce $i_{C1} = i_{C2}$.

Equation (14.58) can then be written as

$$e^{V_{OS}/V_T} = \frac{I_{S2}}{I_{S1}} \qquad \textbf{(14.59(a))}$$

or

$$V_{OS} = V_T \ln\left(\frac{I_{S2}}{I_{S1}}\right) \qquad \textbf{(14.59(b))}$$

Example 14.8 **Objective:** Calculate the offset voltage in a bipolar diff-amp for a given mismatch between the input transistors.

Consider the diff-amp in Figure 14.16 with transistor parameters $I_{S1} = 10^{-14}$ A and $I_{S2} = 1.05 \times 10^{-14}$ A.

Solution: From Equation (14.59(b)), the offset voltage is

$$V_{OS} = V_T \ln\left(\frac{I_{S2}}{I_{S1}}\right) = (0.026)\ln\left(\frac{1.05 \times 10^{-14}}{1 \times 10^{-14}}\right) = 0.00127\,\text{V} \Rightarrow 1.27\,\text{mV}$$

Comment: A 5 percent difference in I_S for Q_1 and for Q_2 produces an offset voltage of 1.27 mV. Since the offset voltage is defined as a positive quantity, if in the previous example I_{S1} were 5 percent larger than I_{S2}, the offset voltage would also be 1.27 mV.

It should be cautioned that the offset voltage in this example is one component of the offset voltage for the entire op-amp. For example, if the two collector resistors are not equal, then the two-sided output voltage v_O will not be zero even if the two transistors are identical. Nevertheless, the calculation provides information on one source of offset voltage, as well as the resulting magnitude of V_{OS}.

Test Your Understanding

14.16 Consider the bipolar diff-amp in Figure 14.16 with transistor parameters $I_{S1} = 2 \times 10^{-14}$ A and $I_{S2} = 1.85 \times 10^{-14}$ A. Calculate the offset voltage. (Ans. 2.03 mV)

Bipolar Active Load Diff-Amp Stage

Figure 14.18 shows a bipolar diff-amp with a simple two-transistor active load. As before, this input stage is biased with a constant-current source. If Q_1 and Q_2 are matched and if Q_3 and Q_4 are matched, then I_Q splits evenly between Q_1 and Q_2 for $v_1 = v_2$, and the E–C voltages of Q_3 and Q_4 are equal. The one-sided dc output voltage v_O will therefore be one E-B voltage below V^+.

If, however, Q_3 and Q_4 are not exactly matched, then i_{C1} and i_{C2} may not be equal since the active load influences the split in the bias current, even if Q_1 and Q_2 are matched. This effect is caused by a finite Early voltage. Taking the

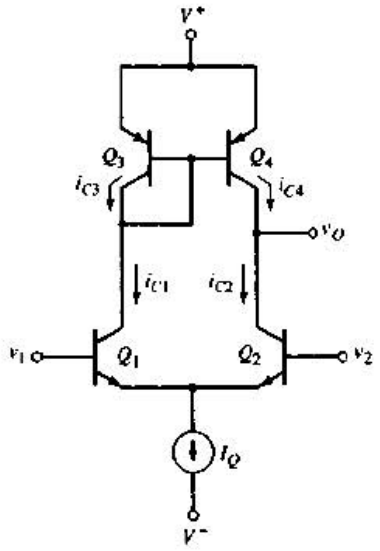


Figure 14.18 Basic bipolar diff-amp with active load

Early voltages into account, but neglecting base currents, we can write the collector currents as

$$\begin{aligned} i_{C1} = i_{C3} &= I_{S1}\left(e^{v_{BE1}/V_T}\right)\left(1+\frac{v_{CE1}}{V_{A1}}\right) \\ &= I_{S3}\left(e^{v_{EB3}/V_T}\right)\left(1+\frac{v_{EC3}}{V_{A3}}\right) \end{aligned} \tag{14.60(a)}$$

and

$$\begin{aligned} i_{C2} = i_{C4} &= I_{S2}\left(e^{v_{BE2}/V_T}\right)\left(1+\frac{v_{CE2}}{V_{A2}}\right) \\ &= I_{S4}\left(e^{v_{EB4}/V_T}\right)\left(1+\frac{v_{EC4}}{V_{A4}}\right) \end{aligned} \tag{14.60(b)}$$

If we assume that Q_1 and Q_2 are matched, then $I_{S1} = I_{S2} \equiv I_S$ and $V_{A1} = V_{A2} \equiv V_{AN}$. Assume that Q_3 and Q_4 are slightly mismatched, so that $I_{S3} \neq I_{S4}$ but still assume that $V_{A3} = V_{A4} \equiv V_{AP}$. For $v_1 = v_2$, we have $v_{BE1} = v_{BE2}$; also, $v_{EB3} = v_{EB4} = v_{EC3} \equiv v_{EB}$. Taking the ratio of Equations (14.60(a)) and (14.60(b)) produces

$$\frac{i_{C1}}{i_{C2}} = \frac{1+\dfrac{v_{CE1}}{V_{AN}}}{1+\dfrac{v_{CE2}}{V_{AN}}} = \frac{I_{S3}}{I_{S4}}\frac{1+\dfrac{v_{EB}}{V_{AP}}}{1+\dfrac{v_{EC4}}{V_{AP}}} \tag{14.61}$$

Equation (14.61) can be rearranged in the form

$$\frac{1+\dfrac{v_{CE1}}{V_{AN}}}{1+\dfrac{v_{EB}}{V_{AP}}} = \frac{I_{S3}}{I_{S4}}\frac{1+\dfrac{v_{CE2}}{V_{AN}}}{1+\dfrac{v_{EC4}}{V_{AP}}} \tag{14.62}$$

Since Q_3 is connected as a diode, v_{CE1} is a constant for a given bias current and supply voltage, which means that the left side of Equation (14.62) is a constant. If $I_{S3} = I_{S4}$, then $v_{CE2} = v_{CE1}$ and $v_{EC4} = v_{EB} = v_{EC3}$. However, if $I_{S3} \neq I_{S4}$, then the collector–emitter voltages on Q_2 and Q_4 must change. If, for example, $I_{S3} > I_{S4}$, then v_{EC4} is larger than v_{CE2}. If, on the other hand, $I_{S4} > I_{S3}$, then v_{EC4} is smaller than v_{CE2}, and Q_4 may be driven into saturation by the mismatch.

Example 14.9 **Objective:** Calculate the change in output voltage for a given mismatch in the active load transistors.

Consider the diff-amp in Figure 14.18 with $V^+ = 10\,\text{V}$. Assume that Q_1 and Q_2 are matched with $v_{BE1} = v_{BE2} = 0.6\,\text{V}$, and assume that $v_{EB3} = v_{EB4} = v_{EC3} = 0.6\,\text{V}$. Let $I_{S3} = 1.05I_{S4}$. Also assume that $V_{AN} = V_{AP} = 50\,\text{V}$.

Solution: Since $v_{EB3} = 0.6\,\text{V} = v_{BE1}$, then for $v_1 = v_2 = 0$,

$$v_{CE1} = V^+ = 10\,\text{V}$$

The left side of Equation (14.62) is therefore

$$\frac{1 + \dfrac{v_{CE1}}{V_{AN}}}{1 + \dfrac{v_{EB}}{V_{AP}}} = \frac{1 + \dfrac{10}{50}}{1 + \dfrac{0.6}{50}} = 1.186$$

We have that

$$v_{EC4} + v_{CE2} = V^+ + v_{BE2} = 10.6\,\text{V}$$

or

$$v_{CE2} = 10.6 - v_{EC4}$$

Equation (14.62) then becomes

$$1.186 = 1.05\frac{1 + \dfrac{10.6 - v_{EC4}}{50}}{1 + \dfrac{v_{EC4}}{50}}$$

which yields

$$v_{EC4} = 1.94\,\text{V}$$

Comment: A 5 percent difference between the properties of Q_3 and Q_4 produces a change from 0.6 to 1.94 V in the E–C voltage of Q_4.

Computer Simulation Verification: A PSpice analysis of the offset voltage effects in the active load diff-amp was performed. The two input terminals are at ground potential.

Using $I_S = 5 \times 10^{-15}\,\text{A}$ for all transistors, the PSpice analysis shows that $v_{EB3} = 0.654\,\text{V}$ rather than the assumed value of 0.6 V. Also, v_{EC4} is 1.19 V rather than equal to v_{EB3}. This occurs because the circuit is slightly unbalanced; that is, i_{C1} includes the base currents of Q_3 and Q_4, and i_{C4} does not. When Q_3 and Q_4 are not matched and $I_{S3} = 1.05I_{S4} = 5.25 \times 10^{-15}\,\text{A}$, then v_{EC4} increases to 2.51 V, compared to 1.94 V from the hand analysis. If, however, $I_{S3} = 0.95I_{S4} = 4.75 \times 10^{-15}\,\text{A}$, then Q_4 goes into saturation.

An offset voltage that will slightly change i_{C1} and i_{C2} will allow the E–C voltage of Q_4 to be adjusted back to its original value.

As shown in actual op-amp circuits, resistors are usually included in the emitters of the active load transistors. By producing a slight imbalance in the two resistor values, we can change the ratio of i_{C1} to i_{C2}, causing a change in the output voltage. This is discussed in the next section when offset voltage null adjustment is discussed.

Test Your Understanding

***14.17** Consider the active load bipolar diff-amp stage in Figure 14.18. Assume the circuit and transistor parameters are as given in Example 14.9. Using Equations (14.60(a)) and (14.60(b)), determine the offset voltage $V_{OS} = |v_{BE2} - v_{BE1}|$ such that $v_{EC3} = v_{EC4}$ and $v_{CE1} = v_{CE2}$. (Ans. 1.27 mV)

MOSFET Diff-Amp Stage

Figure 14.19 shows a basic MOSFET diff-amp in which the differential pair is biased with a constant-current source. If M_1 and M_2 are matched, then for $v_1 = v_2 = 0$, I_Q splits evenly between the two transistors and $i_{D1} = i_{D2}$. Since a two-sided output is the voltage difference between the two drain terminals, then for this symmetrical situation, $v_O = 0$ and the offset voltage is zero.

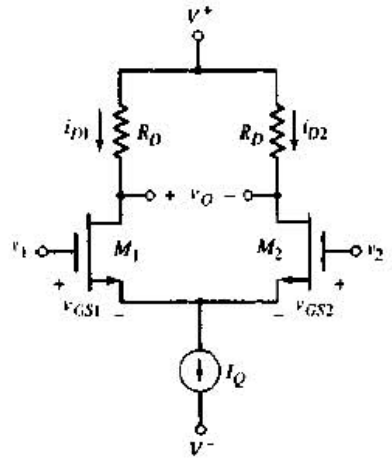


Figure 14.19 Basic MOSFET diff-amp

The drain currents can be written as

$$i_{D1} = K_{n1}(v_{GS1} - V_{TN1})^2 \qquad \textbf{(14.63(a))}$$

and

$$i_{D2} = K_{n2}(v_{GS2} - V_{TN2})^2 \qquad \textbf{(14.63(b))}$$

As previously stated, the conduction parameters K_{n1} and K_{n2} are functions of the electrical and geometric properties of the two transistors, and the threshold voltages V_{TN1} and V_{TN2} are also functions of the transistor electrical properties. If there is a mismatch in electrical or geometric parameters, then we may have $K_{n1} \neq K_{n2}$ and $V_{TN1} \neq V_{TN2}$.

As with the bipolar diff-amp, the input offset voltage is defined as the input differential voltage that must be applied to produce a zero output voltage, or

$$V_{OS} = v_{GS1} - v_{GS2} \tag{14.64}$$

When the offset voltage is applied, $i_{D1} = i_{D2} = I_Q/2$; when the two drain resistors are equal, then $v_O = 0$. Solving Equations (14.63(a)) and (14.63(b)) for v_{GS1} and v_{GS2} and substituting the results into Equation (14.64), we find

$$V_{OS} = \sqrt{\frac{i_{D1}}{K_{n1}}} + V_{TN1} - \left(\sqrt{\frac{i_{D2}}{K_{n2}}} + V_{TN2}\right) \tag{14.65}$$

The various difference and average quantities are defined as follows:

$$\Delta K_n = K_{n1} - K_{n2} \tag{14.66(a)}$$

$$K_n = \frac{K_{n1} + K_{n2}}{2} \tag{14.66(b)}$$

$$\Delta V_{TN} = V_{TN1} - V_{TN2} \tag{14.67(a)}$$

and

$$V_{TN} = \frac{V_{TN1} + V_{TN2}}{2} \tag{14.67(b)}$$

Combining Equations (14.66(a)) and (14.66(b)), we have

$$K_{n1} = K_n + \frac{\Delta K_n}{2} \tag{14.68(a)}$$

and

$$K_{n2} = K_n - \frac{\Delta K_n}{2} \tag{14.68(b)}$$

Similarly,

$$V_{TN1} = V_{TN} + \frac{\Delta V_{TN}}{2} \tag{14.69(a)}$$

and

$$V_{TN2} = V_{TN} - \frac{\Delta V_{TN}}{2} \tag{14.69(b)}$$

Noting that $i_{D1} = i_{D2} = I_Q/2$ and substituting Equations (14.68(a)) through (14.69(b)) into Equation (14.65), we obtain

$$V_{OS} = \sqrt{\frac{I_Q}{2}}\left[\frac{1}{\sqrt{K_n + (\Delta K_n/2)}} - \frac{1}{\sqrt{K_n - (\Delta K_n/2)}}\right] + \Delta V_{TN} \tag{14.70}$$

If we assume that $\Delta K_n \ll K_n$ then Equation (14.70) reduces to

$$V_{OS} = -\frac{1}{2}\sqrt{\frac{I_Q}{2K_n}} \cdot \left(\frac{\Delta K_n}{K_n}\right) + \Delta V_{TN} \tag{14.71}$$

Equation (14.71) is the offset voltage in a MOSFET diff-amp as a function of the differences in conduction parameters and threshold voltages.

Example 14.10 **Objective:** Calculate the offset voltage in a MOSFET diff-amp stage for a given mismatch between input transistors.

Consider the diff-amp in Figure 14.19 with transistor parameters $K_{n1} = 105\,\mu A/V^2$, $K_{n2} = 100\,\mu A/V^2$, and $V_{TN1} = V_{TN2}$. Assume $I_Q = 200\,\mu A$.

Solution: From Equation (14.66(a)), the difference in conduction parameters is

$$\Delta K_n = K_{n1} - K_{n2} = 105 - 100 = 5\,\mu A/V^2$$

From Equation (14.66(b)), the average of the conduction parameters is

$$K_n = \frac{K_{n1} + K_{n2}}{2} = \frac{105 + 100}{2} = 102.5\,\mu A/V^2$$

The magnitude of the offset voltage is, from Equation (14.71),

$$|V_{OS}| = \frac{1}{2}\sqrt{\frac{I_Q}{2K_n}} \cdot \left(\frac{\Delta K_n}{K_n}\right) = \frac{1}{2}\sqrt{\frac{200}{2(102.5)}}\left(\frac{5}{102.5}\right) = 0.0241\,V \Rightarrow 24.1\,mV$$

Comment: A 5 percent difference in conduction parameter values between the input MOS transistors produces an offset voltage of 24.1 mV.

Test Your Understanding

14.18 Assume the MOSFET diff-amp shown in Figure 14.19 is biased with a current $I_Q = 150\,\mu A$. Let $V_{TN1} = V_{TN2}$. Assume the nominal conduction parameter value is $K_n = 50\,\mu A/V^2$. Determine the maximum variation ΔK_n such that the offset voltage is limited to $V_{OS} = 20\,mV$. (Ans. $\Delta K_n = 1.63\,\mu A/V^2$)

Comparing the results of Examples 14.8 and 14.10 shows that typically the offset voltage for a MOSFET diff-amp is substantially larger than that of a bipolar diff-amp. The difference can be explained by comparing Equation (14.71) for the MOSFET diff-amp and Equation (14.59(b)) for the bipolar diff-amp. The offset voltage for the MOSFET diff-amp is directly proportional to the percent change in conduction parameter values, whereas the offset voltage for the bipolar diff-amp is proportional to the logarithm of the percent change in the I_S current parameters. In addition, the offset voltage for the MOSFET pair is proportional to

$$\sqrt{I_Q/K_n} = V_{GS} - V_{TN}$$

which is typically in the range of 1–2 V. In contrast, the offset voltage for the bipolar pair is proportional to

$$V_T \approx 26\,mV$$