6

LINEAR CIRCUIT APPLICATIONS

In this chapter we discuss some of the most frequently encountered linear circuit applications of operational amplifiers. These include differential DC amplifiers, bridge amplifiers, analog integrators, differentiators, line-driving amplifiers, ac-coupled feedback amplifiers, current-to-voltage converters, reference voltage sources, voltage regulators, current amplifiers, and charge amplifiers. The details of these applications are given in the sections which follow. Inverting, noninverting, and summing amplifiers are discussed in the basic theory of Appendix A.

6.1 Differential DC Amplifiers

The amplifiers to be discussed in this section are most descriptively known as differential DC amplifiers, denoting the fact that they amplify the difference between two signals and that the inputs are direct-coupled. Other common terms used for this basic type of amplifier are transducer amplifier, bridge amplifier, data amplifier, instrumentation amplifier, difference amplifier, and error amplifier. Such amplifiers are easily realized through the use of one or more operational amplifiers with linear

feedback. The idealized characteristics of these amplifiers are infinite input impedance, zero output impedance, no dc offsets or drift, zero amplifier noise, a constant gain factor with no gain error, and complete rejection of signals common to both inputs (infinite common-mode rejection). Inputs are typically from transducers which convert a physical parameter and its variations to electrical signals. Examples of such transducers are thermocouples, strain-gage bridges, etc. Several types of such differential DC amplifiers, of varying complexity and performance characteristics, are discussed in the following paragraphs.

6.1.1 Differential DC amplifiers using one operational amplifier[2,6,7] The circuit of Fig. 6.1a has the virtue of simplicity, using only one operational amplifier and four matched resistors. The presence of a common-mode voltage e_{cm} and a differential voltage $e_1 - e_2$ are characteristic of most transducers. The common-mode voltage may represent a dc level, as in a bridge, or may be noise pickup. If an ideal operational amplifier is assumed, the following equations apply:

$$e_3 = (e_{cm} + e_2)\frac{R_4}{R_3 + R_4}$$

$$\frac{e_{cm} + e_1 - e_3}{R_1} = \frac{e_3 - e_o}{R_2}$$

Combining these gives the resulting equation for output voltage,

$$e_o = e_{cm}\frac{R_4R_2 + R_4R_1 - R_2R_3 - R_2R_4}{R_1(R_3 + R_4)} - \frac{R_2}{R_1}e_1 + \frac{R_4}{R_3}\frac{1 + R_2/R_1}{1 + R_4/R_3}e_2$$

If $R_2/R_1 = R_4/R_3$, the above equation reduces to $e_o = (R_2/R_1)(e_2 - e_1)$. The resistor ratios R_2/R_1 and R_4/R_3 must be carefully matched in order to ensure the rejection of common-mode signals. The value of these resistor ratios sets the gain for differential signals. These equations illustrate the performance of the circuit when one is dealing with zero source impedances and nonzero common-mode signals. For zero source impedance the gain is determined solely by the feedback resistors and, if these resistors are matched in pairs as indicated, common-mode signals are rejected completely. Actually, of course, the operational amplifier has been assumed ideal in having infinite input impedance, infinite gain, and infinite common-mode rejection. If these factors are given real values and their effects evaluated, it will be found that the finite input impedance of the operational amplifier and its inherent finite common-mode rejection will place limits on the overall common-mode rejection of the closed-loop differential amplifier. The finite open-loop gain will limit the gain accuracy of the overall circuit.

Figure 6.1b illustrates a model for unbalanced source impedances and their interactions with the finite resistances of the amplifier feedback network. An analysis similar to that for the circuit of Fig. 6.1a yields

$$e_o = e_{cm}\frac{R_2(R_{S_1} - R_{S_2})}{(R_1 + R_{S_1})(R_3 + R_{S_2} + R_4)} + \frac{R_2}{R_1 + R_{S_1}}\left[\frac{1 + (R_1 + R_{S_1})/R_2}{1 + (R_3 + R_{S_2})/R_4}e_2 - e_1\right]$$

Note that, if the source impedances are nonzero but equal, the only effect is a gain error due to the source loading. However, if the source impedances are also unequal, the common-mode rejection is degraded. Input bias currents (I_{B1}, I_{B2}) and input voltage offset (V_{OS}) of the operational amplifier will cause dc offset errors at the output of the differential amplifier circuit. Bias current (I_{B2}) from the noninverting side of the operational amplifier flows through the parallel combination of R_4 and R_3 to create a dc error voltage at the noninverting input terminal. This dc voltage effectively adds to the offset voltage of the operational amplifier and is amplified by the factor $(R_2 + R_1)/R_1$. Bias current (I_{B1}) from the inverting input of the operational amplifier flows principally through resistor R_2 and causes an output offset adding to the other two components to give the total dc offset error of

$$E_{OS} = V_{OS}\frac{R_2 + R_1}{R_1} + I_{B1}\frac{R_3R_4}{R_3 + R_4}\frac{R_2 + R_1}{R_1} - I_{B2}R_2$$

Tracking between the two bias currents reduces the bias-current-induced error term by as much as a factor of 10. The principal limitations of this circuit are its low input impedance and the difficulty of varying the gain. The input impedance, of course, is determined by the feedback and input resistors. If these resistors are made large in order to increase the input impedance the dc errors due to bias currents will be proportionately increased, thus placing an upper limit on the feasible values of input impedance. The gain of the differential amplifier can be changed only by varying the ratios of the feedback resistors. Because of the necessity of maintaining the equality of the resistive ratios, it is quite difficult to continuously vary the gain. Gain steps can be achieved if the common-mode rejection is carefully adjusted at each gain setting. The differential amplifier circuit of Fig. 6.2 is a similar type of circuit with the added feature of a gain vernier which allows the gain to be continuously varied without affecting the common-mode rejection of the circuit. The output voltage is

$$e_o = 2\left(1 + \frac{1}{K}\right)\frac{R_2}{R_1}(e_2 - e_1)$$

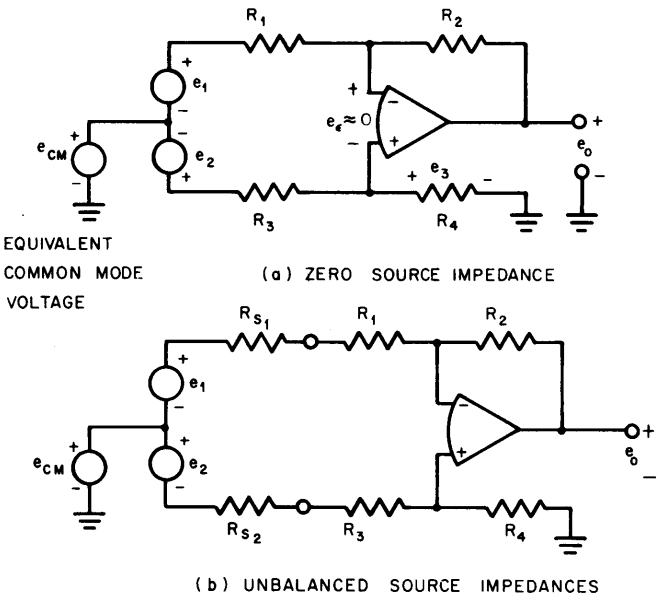


Fig. 6.1 Simple differential amplifier.

Note, however, that this circuit requires four matched resistors of value R_2 and two matched resistors of value R_1. The gain is an inverse function of the setting of the vernier potentiometer and as such is highly nonlinear. The potentiometer can, however, provide approximate linearity over limited ranges. The circuit still suffers from the limitations of low input impedance. The dc offset errors are much the same as those for the circuit of Fig. 6.1.

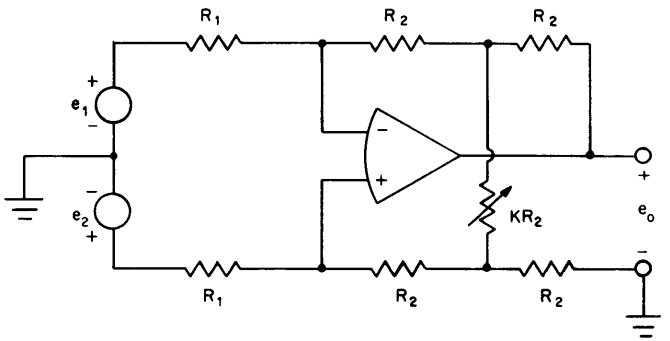


Fig. 6.2 Simple adjustable-gain differential amplifier.

6.1.2 Differential DC amplifiers using more than one operational amplifier[2,7] The circuit of Fig. 6.3 provides another low impedance alternative to those of Figs. 6.1 and 6.2. The two amplifiers required operate in the inverting mode and need not have a noninverting capability. Thus they can be chopper-stabilized amplifiers for low drift, or they may be FET input types which may have rather poor linearity when used noninverting. The output voltage is

$$e_o = \frac{R_2}{R_1}(e_2 - e_1)$$

The gain can be easily varied, in steps or continuously, by changing the value of R_2, without affecting the common-mode rejection properties. Good common-mode rejection requires four closely matched resistors of value R_1. Note that the dc offset error is approximately four times that of a single amplifier, if it is assumed that the offset errors add, as given by the expression

$$E_{os} = \left(1 + 2\frac{R_2}{R_1}\right) V_{os2} + 2\frac{R_2}{R_1} V_{os1}$$

$$= \left(1 + 4\frac{R_2}{R_1}\right) V_{os} \qquad \text{(worst case)}$$

Since the common-mode rejection of the operational amplifiers is not a factor, the common-mode rejection of the closed-loop amplifier can be trimmed to quite high values simply by allowing a small amount of adjustability of one of the R_1 resistors. The common-mode voltage capability of the circuit is limited only by the output voltage capability of the unity-gain inverter. This capability can be increased by making the gain of amplifier A_1 less than unity. The gain of amplifier A_2 must then be increased accordingly, however, which increases the output offset

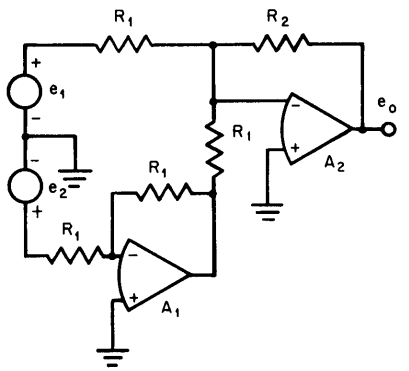


Fig. 6.3 Differential DC amplifier using inverting operational amplifiers.

error. Another differential DC amplifier circuit using two operational amplifiers is shown in Fig. 6.4. This circuit provides the high input impedance lacking in the circuits discussed up to now. For this circuit

$$e_o = \left(1 + \frac{R_4}{R_3}\right)(e_2 - e_1) \quad , \quad \text{if } \frac{R_1}{R_2} = \frac{R_4}{R_3}$$

Again, equality of the two resistor ratios is required in order for the circuit to reject common-mode signals. The operational amplifiers, since they operate in the noninverting mode, must have good common-mode properties. The input impedance at each terminal of the differential amplifier is simply the common-mode input impedance of the operational amplifiers. This can be quite large (10 MΩ and up), depending on the type of operational amplifier used. For fixed gains, or gain steps, the circuit is quite useful, but it is not feasible for continuously variable gain. Also, since the input voltage of the upper amplifier must be less than $R_1/(R_1 + R_2)$ times the output saturation voltage, the common-mode voltage range is very limited at low values of overall gain. This is not considered a serious limitation since such amplifiers are usually used at gains of 10 or greater. The differential DC amplifier circuit of Fig. 6.5 overcomes most of the weaknesses of the circuits discussed up to this point. Analysis of the circuit yields the following equations:

$$e_3 = \left(1 + \frac{R_2}{R_1}\right) e_1 - \frac{R_2}{R_1} e_2 + e_{cm}$$

$$e_4 = \left(1 + \frac{R_3}{R_1}\right) e_2 - \frac{R_3}{R_1} e_1 + e_{cm}$$

$$e_o = e_4 - e_3$$

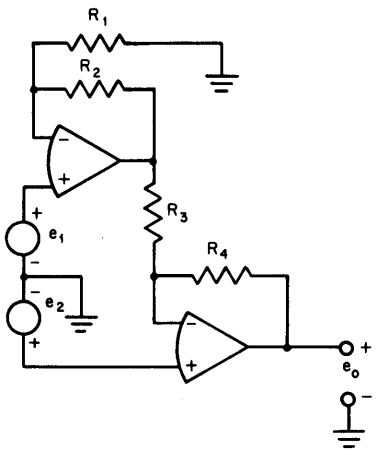


Fig. 6.4 High input impedance differential amplifier.

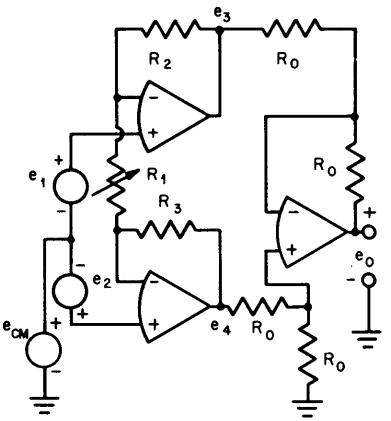


Fig. 6.5 High input impedance adjustable-gain differential amplifier.

If $R_2 = R_3$, the output voltage is

$$e_o = \left(1 + \frac{2R_2}{R_1}\right)(e_2 - e_1)$$

The two input amplifiers constitute a differential buffer amplifier with a gain of $1 + 2R_2/R_1$ for differential signals, and unity gain for common-mode signals. The noninverting configuration of these input amplifiers ensures high input impedance at both inputs. The gain is easily varied by a single resistor R_1. The effects of mismatch in resistors R_2 and R_3 is simply to create a gain error without affecting the common-mode rejection of the circuit. The resistors R_o of the output amplifier must be accurately matched, or trimmed, to ensure the rejection of common-mode signals at this point. This final amplifier acts simply as a differential-input to single-ended-output converter. Feedback impedances in both stages can be relatively low in value to minimize the effects of bias current, since these feedback elements do not affect the input impedance of the differential amplifier. Usually, all the gain of this differential amplifier is in the input stage, thus ensuring that only the offset voltages of these two operational amplifiers are significant in determining the output offset. Since the output voltage offset is proportional to the difference of the voltage offsets of these two amplifiers, it is desirable to use amplifiers whose voltage offsets tend to track with temperature. Such techniques are the basis for some low-drift differential amplifier modules. The bias currents of these input amplifiers will flow through the impedance of the source and will thus generate additional offset voltage which will appear at the output of the differential amplifier amplified by the differential gain factor. The use of amplifiers with FET input stages will greatly reduce this effect.

6.2 Bridge Amplifiers[2]

Probably the most common use for a differential DC amplifier is in amplifying the output signal from a transducer bridge, such as a strain gage. The most straightforward way of doing this is with one of the high impedance amplifiers discussed in the preceding section. Such a strain-gage bridge, with one active bridge arm, is shown in Fig. 6.6. The following equations describe its operation:

$$e_2 = V\frac{R}{2R + \Delta R}$$

$$e_1 = \frac{V}{2}$$

$$e_2 - e_1 = -\frac{V}{4}\frac{\delta}{1 + \delta/2}$$

where

$$\delta = \frac{\Delta R}{R}$$

$$e_o = K(e_2 - e_1) = -\frac{KV}{4}\frac{\delta}{1 + \delta/2}$$

$$e_o \approx -KV\frac{\delta}{4}, \quad \text{if } \delta \ll 1$$

The output signal is a linear function of the variation of the active element only for small percentage changes in the element. If larger changes are to be measured, the exact equation must be used and a conversion or linearization performed at some point in the data-gathering process.

It is sometimes desirable to use an amplifier less complex than the fully developed differential instrumentation amplifier for amplifying the output signal from a bridge. There are several such circuits which use only a single operational amplifier, such as the one shown in Fig. 6.7. This

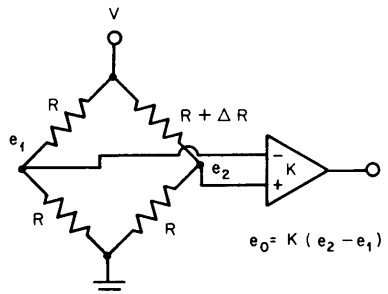


Fig. 6.6 Bridge amplifier.

circuit forces the differential output voltage of the bridge to be zero since opposite sides are connected directly to the inputs of an operational amplifier with feedback. Thus the amplifier is used to measure the current flowing into the bridge under short-circuit conditions. The resulting output voltage is

$$e_o = \frac{R_F}{R} \frac{\delta}{1+\delta} \frac{V}{(2+\delta)/(1+\delta) + R/R_F}$$

If $\delta \ll 1$ and $R_F \gg R$, this equation reduces to the approximate form

$$e_o \approx V \frac{\delta}{2} \frac{R_F}{R}$$

Note that here again the equation for the output voltage of the bridge amplifier is a nonlinear function of the variation of the active bridge element, but for small deviations the nonlinearity is negligible. For the simplified, approximate form of the equation, it has also been assumed that the values of resistance in the bridge are much smaller than the resistors R_F. The bridge resistance appears in the gain equation, thus requiring that the values of the bridge elements be insensitive to temperature in order that the gain of the amplifier be stable with temperature. If the assumption that R_F is much greater than the nominal bridge resistance applies, there is no loading effect.

The dc offset voltage generated at the output of the bridge amplifier as a result of the input offset voltage and bias currents of the operational amplifier is given by

$$E_{OS} = V_{OS} \frac{2R_F + R}{R} + (I_{B2} - I_{B1})R_F$$

where I_{B1} and I_{B2} are input bias currents. The main advantage of this circuit is its simplicity. It does require an amplifier which has reasonably good common-mode rejection.

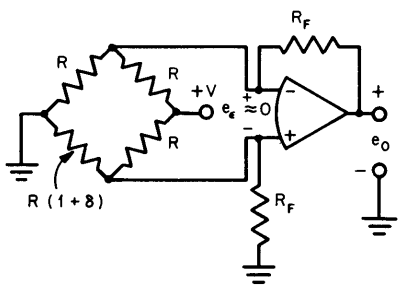


Fig. 6.7 Bridge current amplifier.

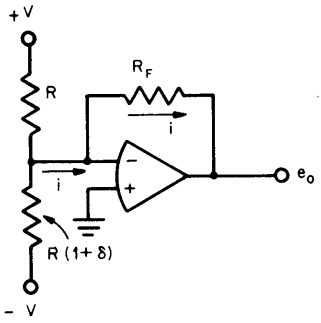


Fig. 6.8 Half-bridge current amplifier.

Where the rejection of common-mode noise signals is not a problem, the half-bridge measuring circuit of Fig. 6.8 is sometimes used. Here also the output of the bridge is connected directly to the input terminal of the operational amplifier, as is the feedback through R_F. Since the other input of the operational amplifier is held at ground potential, the output of the half-bridge is held at zero voltage, and the amplifier responds to the short-circuit output current

$$e_o = -iR_F = -V\frac{R_F}{R}\frac{\delta}{1+\delta}$$

If $\delta \ll 1$

$$e_o \approx -V\frac{R_F}{R}\delta$$

Because the amplifier operates single-ended, the amplifier used can be chopper-stabilized for lowest possible drift and dc offset errors. Also, the maximum voltage supplied to the bridge, or half-bridge, is not limited by common-mode voltage limitations of the operational amplifier, as it is in those circuits which use the noninverting input of the operational amplifier. Thus it is possible to increase the sensitivity of the bridge by increasing the supply voltage within the limitations of the bridge elements and the ability of the amplifier to supply the current flowing through the feedback resistor.

The major drawback of the half-bridge circuit is its inability to reject noise pickup, as is normally accomplished by the differential type of bridge amplifier. Consequently, the noise and ripple of the half-bridge supply must be very low, and all wiring must be kept short and well shielded. As in the previous bridge amplifier, the gain is a function of the bridge elements. This can be a serious drawback if the bridge elements are sensitive to environmental factors other than the one that it is desired to measure. The output dc offset voltage of the half-bridge

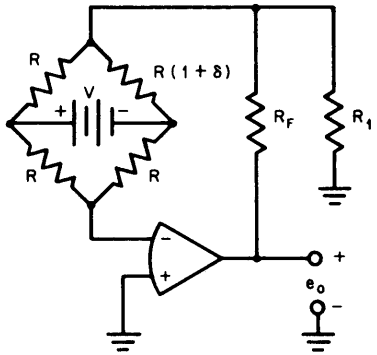


Fig. 6.9 Inverting bridge amplifier.

amplifier is given by the expression

$$E_{OS} = V_{OS}\left(1 + \frac{2R_F}{R}\right) - I_{B1}R_F$$

where I_{B1} is the input bias current.

Figure 6.9 illustrates another bridge amplifier using a single operational amplifier in the inverting mode. Thus it is once again possible to use a single-ended chopper-stabilized amplifier with its attendant low drift. The amplifier output voltage is

$$e_o = V\left(1 + \frac{R_F}{R_1}\right)\frac{\delta}{4(1 + \delta/2)}$$

which, for $\delta \ll 1$, reduces to

$$e_o \approx V\left(1 + \frac{R_F}{R_1}\right)\frac{\delta}{4}$$

Another advantage of this circuit, not shared by the preceding two, is that the gain is not dependent upon the absolute value of the bridge resistors. The output voltage is proportional to the open-circuit coltage of the bridge since the input to the amplifier draws negligible signal current. The inverting input of the operational amplifier is maintained at virtual ground by the high open-loop gain. Since the gain is a function of R_F and R_1, it can be varied easily with either resistor. A small-valued potentiometer can be added in series with either resistor for calibration purposes. This type of bridge amplifier can be very accurate and is recommended when it is necessary to detect very small bridge signals. The primary disadvantage is that a floating bridge supply is required. Since it uses a single-ended amplifier it does not have the common-mode rejection capabilities of the true differential amplifier. However, careful shielding and filtering to remove noise can help to eliminate this problem.

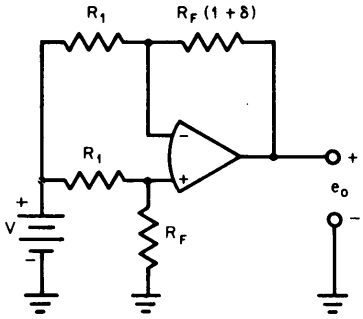


Fig. 6.10 Wide-deviation bridge amplifier.

The output voltage offset as a function of input offset voltage and bias currents is similar to that of the inverting amplifier circuit. That is,

$$E_{OS} = \frac{R_F + R_1}{R_1}(V_{OS} - I_{B1}R) - I_{B1}R_F$$

where I_{B1} is the amplifier input bias current.

The final bridge amplifier circuit to be discussed is that given in Fig. 6.10 where the output voltage is directly proportional to the transducer deviation even for large fractional changes in the active element:

$$e_o = -V\frac{\delta R_F}{R_1 + R_F}$$

This particular circuit should be used whenever the deviation of the active element is large enough so that the linear approximations made in the previous bridge equations are no longer valid. Examples are semiconductor strain gages that have high gage factors, thermistors, etc. The bridge elements must be so matched that the two input resistors are equal and the active element is equal to the value of R_F when the bridge is at null. Calibration is somewhat difficult since it requires the trimming of two values of resistance to maintain null while varying sensitivity.

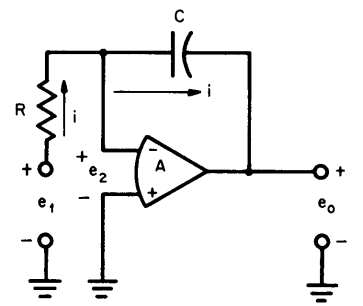


Fig. 6.11 Analog integrator.

6.3 Analog Integrators[1,5,8]

The analog integrator is extremely useful in computing, signal processing, and signal generating applications. It uses an operational amplifier in the inverting configuration, as shown in Fig. 6.11. The equations of operation are derived by assuming an ideal operational amplifier of gain A. These are

$$\frac{e_1 - e_2}{R} = i$$

$$e_2 - e_o = \frac{1}{C}\int_0^t i\,dt = \frac{1}{RC}\int_0^t (e_1 - e_2)\,dt$$

$$e_2 = -\frac{e_o}{A}$$

If $A \rightarrow \infty$, then $e_2 \rightarrow 0$ and $e_o = -(1/RC)\int e_1\,dt$. As in the inverting amplifier, the summing point is held at a virtual ground by the high gain of the amplifier and its feedback network. Since no current flows into the input terminal of the operational amplifier, all the input current $i = e_1/R_1$ is forced to flow into the feedback capacitor, causing a charge voltage to appear across this element. Because one end of the capacitor is tied to the virtual ground point, the output voltage of the amplifier equals the capacitor charging voltage. The overall integrator circuit has the low output impedance normally associated with a feedback amplifier.

The dc offset and bias current of the analog integrator are taken into account in the more realistic model of Fig. 6.12. Because these dc errors exist, the output of the integrator now consists of two components: the integrated signal term and an error term

$$e_o = -\frac{1}{RC}\int e_1\,dt + \frac{1}{RC}\int V_{OS}\,dt + \frac{1}{C}\int I_B\,dt + V_{OS}$$

The error term itself is made up of a component due to the input offset

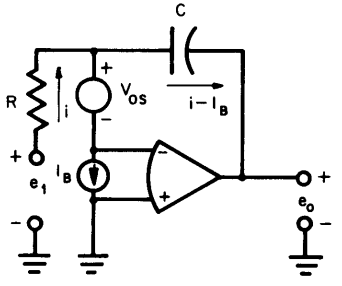


Fig. 6.12 Effect of offset voltage and bias current in an integrator circuit.

voltage and another due to the input bias current. The integral of the dc offset voltage results in a ramp voltage, a linearly increasing term whose polarity is determined by the polarity of the input offset voltage. In addition to this ramp voltage error, the input offset voltage creates an output offset voltage equal to it in value. The bias current flows almost entirely through the feedback capacitor, charging it in ramp fashion, similar to the ramp voltage due to input offset voltage. These two ramp voltage errors will continue to increase until the amplifier reaches its saturation voltage or some limit set by external circuitry. These error components usually set the upper limit on feasible length of integration time. The error component due to bias current can be minimized by increasing the capacitance of the feedback element. This can be done only by decreasing the value of the input resistor, if a specific value of the RC time constant is to be achieved. A lower limit usually exists on R, because of current limitations and loading of the input signal source.

The effects of bias current can be reduced by inserting a resistance R between the noninverting input of the amplifier and ground. This equalizes the resistances at the two inputs and changes the effects of bias current to that of offset (difference) current. Thus, in the equation for output voltage, I_B, the bias current, should be replaced by I_{os}, the offset current, if the compensating resistor is used. The error ramp due to voltage offset is fixed by the chosen value of RC time constant.

In order to realize the performance possibilities of an operational amplifier as an integrator, a feedback capacitor must be selected with a dielectric leakage current which is less than the bias current of the amplifier. Polystyrene and Teflon are usually the best choices for the ultimate in long-term integrating accuracy. If shorter integration times are required, the requirements on capacitor quality can accordingly be relaxed. Mylar capacitors may then prove satisfactory, or silver-mica types, if small values of capacitance, corresponding to high-speed integration, are to be used.

The choice of the type of amplifier is also governed by the length of computing time and the desired accuracy. Chopper-stabilized amplifiers are usually used for long-term integrators because of their superior long-term dc stability. FET amplifiers are used for medium-length integration because of their low bias current. Amplifiers with bipolar transistor input stages may be used in very short-term integration such as in signal generation (sweep generation, triangle waves, etc.).

If the finite gain and bandwidth are taken into account, their effects on the integrator response function may be evaluated. The open-loop frequency response of the amplifier is approximated by a single pole located at $1/\tau_o$, and a low-frequency gain of A_o.

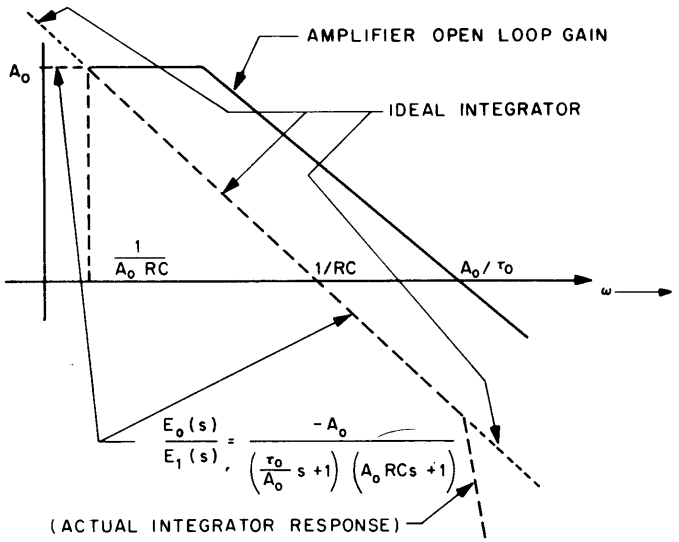


Fig. 6.13 Bode plots; amplifier, integrator.

The resulting integrator response function is

$$\frac{E_o}{E_1}(s) \approx \frac{-A_o}{(\tau_o/A_o s + 1)(A_o RCs + 1)}$$

if $A_o \gg 1$ and $A_o RC \gg \tau_o$. This function has two poles on the real axis, as opposed to the ideal integrator function which has a single pole at the origin. In Fig. 6.13 the frequency response of this approximate integrator is compared with the response of an ideal integrator, along with an open-loop frequency response of the operational amplifier. Note that the response of the real integrator departs from the ideal response only at the extremes of frequency. At low frequencies the departure is due to the finite gain of the operational amplifier. At high frequencies, it is due to the finite amplifier bandwidth.

The transient response of the integrator is studied in Fig. 6.14 by calculating the response to a step function. The response of an ideal integrator to a step function $-E/s$ would be a linear ramp voltage increasing to infinity. The step response of the practical integrator is a close approximation of this ramp throughout most of the signal range:

$$e_o(t) = A_o E\left(1 - \frac{e^{-t/A_o RC}}{1 - \tau_o/A_o RC} + \frac{e^{-t/\tau_o}}{A_o RC/\tau_o - 1}\right)$$

In order to compare the ideal and real responses, it is necessary to examine the responses for very small and very large time. For small values of

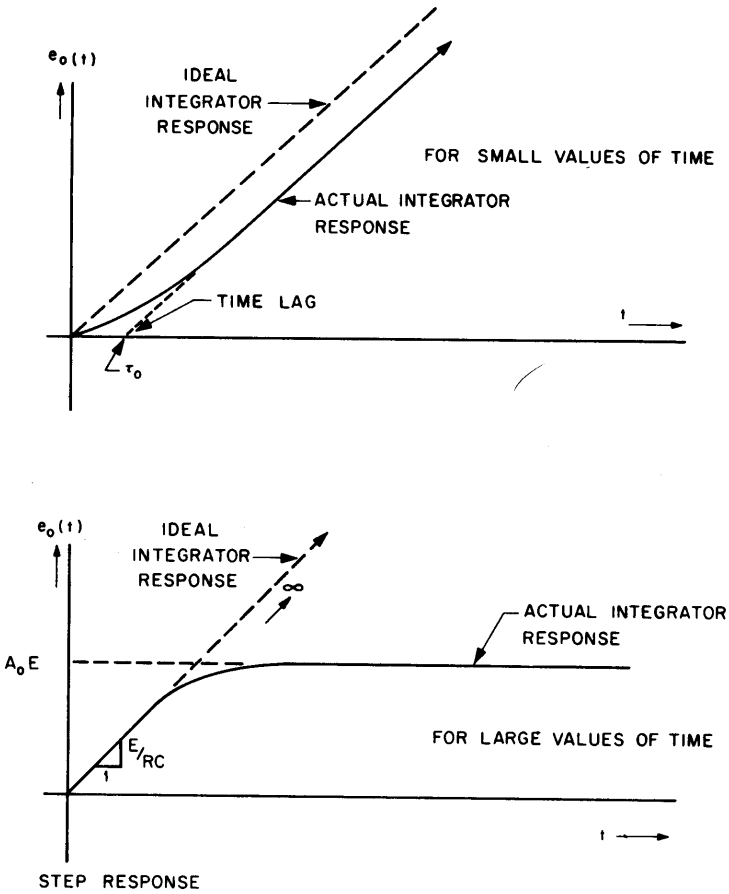


Fig. 6.14 Step response of integrator.

time the response is approximately

$$e_o(t) \approx E\left(\frac{t}{RC} + \frac{\tau_o}{RC} + \frac{e^{-t/\tau_o}}{RC/\tau_o}\right)$$

For large values of time the response is approximately

$$e_o(t) = A_oE(1 - e^{-t/A_oRC})$$

For small values of time the principal error effect is caused by the finite bandwidth, which causes a time lag error in the actual response. For large values of time the output signal would approach an exponential with time constant A_oRC and final value A_oE. For accurate computation, the

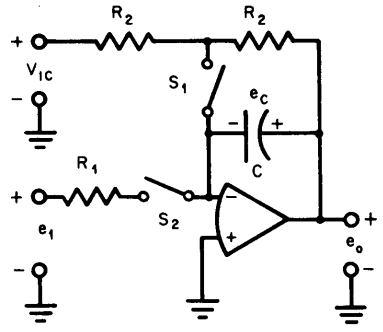


Fig. 6.15 Three-mode integrator.

integration should be terminated at a time much less than A_oRC and an output amplitude much less than A_oE.

Figure 6.15 illustrates the switching techniques used to initiate and terminate the period of the integration. This integrator circuit has three modes. The first of these is RESET, in which the initial conditions are established by placing an initial charge on the capacitor. This is done by closing switch S_1 to allow the output voltage to rise to the negative of V_{IC}. If switch S_1 is then opened and S_2 is closed, the circuit begins integration of the input signal e_i beginning at the value $-V_{IC}$. This is the second or INTEGRATE mode. If both switches are held open, the output voltage will hold its latest value and will not respond to input or initial condition voltages. During this HOLD mode, the only discharge of the capacitor is due to the bias current of the amplifier and dielectric leakage in the capacitor. Since electronic switch modules are commonly used for the mode control function in place of the simple switches shown, any leakage current flowing from these switches must be added to amplifier bias current in calculating the decay of the capacitor voltage during HOLD, or during the INTEGRATE mode.

Although the analog integrator is a linear device, its maximum rate of change of output signal can lead to slew rate distortion for signals of relatively high frequency and large amplitude. The inherent slew rate limit of the operational amplifier places one of these limitations on the operation. However, another limitation, usually much more restrictive, is that placed on the rate of change of capacitor voltage by the output current limits of the amplifier. The expression for this is

$$\left(\frac{de_c}{dt}\right)_{max} = \left(\frac{de_o}{dt}\right)_{max} = \frac{I_{lim}}{C}$$

where

$$I_{lim} = \text{output current limit}$$

The time required for the amplifier to RESET to initial conditions is

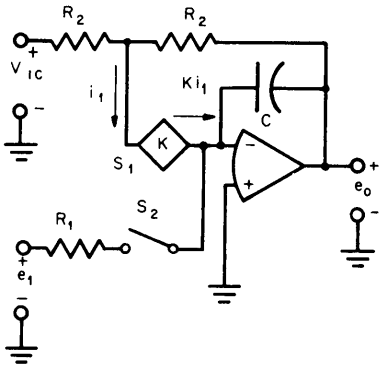


Fig. 6.16 Current amplifying switch used for integrator reset.

limited by the RC time constant of the RESET network and also by the slew rate achievable in the closed-loop circuit. If a reset switch which has a large current gain factor is used, the reset time can be considerably reduced. The use of such a switch is illustrated in Fig. 6.16, where the circuit is shown in the RESET state. Analysis of the circuit yields the equation for the output voltage,

$$e_o = -e_i(1 - e^{-Kt/R_2C})$$

This is again the equation of an exponentially increasing voltage. Here, however, the time constant is R_2C/K, reduced by a factor equal to the current gain of the switch. The RESET time can potentially be reduced by the factor K, if the operational amplifier and switched current amplifier do not reach their current limits, thus limiting the slew rate. Maximum current is required at $t = 0$, the initiation of the RESET mode.

6.4 Differentiators[2,3,6]

By interchanging the resistor and capacitor of an integrator circuit we obtain the inverse function, differentiation. However, as will be shown, the differentiator circuit (Fig. 6.17a) has some troublesome properties. If the usual single-pole open-loop gain function is assumed for the amplifier the transfer function of the differentiator circuit may be reduced to

$$\frac{e_o}{e_i} = \frac{-RCs}{1 + (1/A_o)(\tau_o + RC)s + (RC\tau_o/A_o)s^2}$$

This transfer function has the form

$$H(s) = \frac{-H_o s}{1 + (\alpha/\omega_n)s + s^2/\omega_n^2}$$

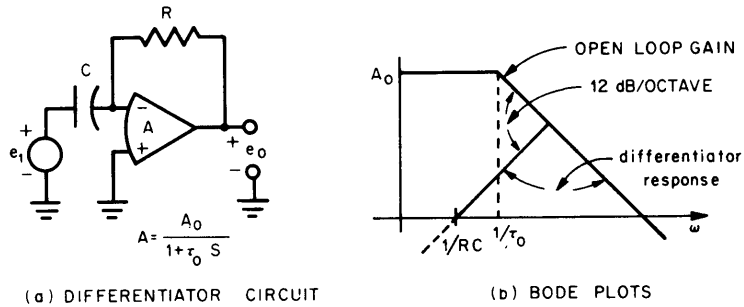


Fig. 6.17 Differentiator using an operational amplifier. (a) Differentiator circuit; (b) Bode plots.

where

$$\omega_n^2 = \frac{A_o}{RC\tau_o}$$

and

$$\alpha \text{ (damping factor)} = \sqrt{\frac{(\tau_o + RC)^2}{RC\tau_o}\frac{1}{A_o}} \ll 1$$

Thus the damping factor α is very small, indicating a lightly damped circuit response and complex poles near the $j\omega$ axis. Such a response would also be indicated by the 12 dB per octave rate of closure of the Bode plots (Fig. 6.17b). Thus the differentiator circuit as shown has a tendency toward instability. If the amplifier open-loop gain has an attenuation rate of greater than 6 dB per octave over a portion of its Bode plot, the circuit may well oscillate. Another problem with this differentiator circuit is its high gain at high frequencies. This allows the high-frequency components of amplifier noise to be amplified even though the signal may not have high-frequency components. Thus the high-frequency output noise may obscure the differentiated signal.

The modified differentiator circuit of Fig. 6.18a is usually preferred as a means of eliminating the problems of the simpler circuit. Two additional real poles are introduced by use of R_1 and C_F. This creates a very stable system and reduces the high-frequency noise. The poles are placed sufficiently high in frequency to prevent significant phase-shift error in the signal frequency range. The modified frequency response is shown in Fig. 6.18b.

6.5 Line-driving Amplifiers

One of the primary areas of application for the operational amplifier is that of buffering between a signal source and the desired load. Usually

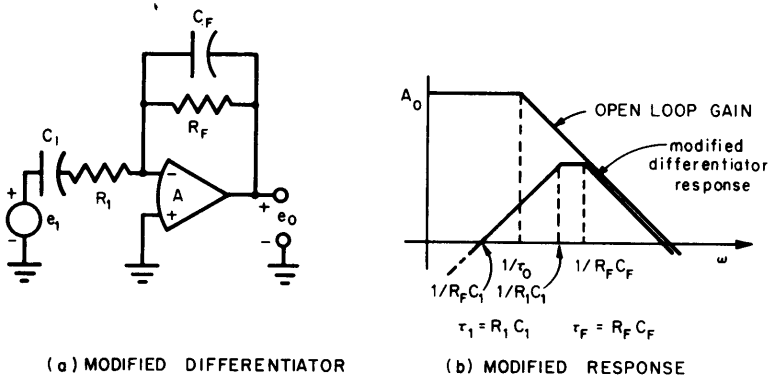


Fig. 6.18 Modified differentiator with improved noise and stability. (a) Modified differentiator; (b) Modified response.

the signal source is very limited in power, has relatively high internal impedance, and is low level. The load is relatively low in impedance (possibly capacitive) and requires high-level signals. Thus the amplifier must provide impedance buffering, signal scaling, and power gain. Needless to say, it must be stable under the desired conditions of loading and feedback and must have sufficient gain and bandwidth to ensure accurate response to input signals. A typical example of such an application is the line-driving amplifier.

When data signals must be transmitted over long signal lines from a remote measuring station, the line-driving amplifier is usually required. Figure 6.19 illustrates a simulated load of this type. The capacitance is that of a shielded cable and may be as little as a few picofarads or as much as several microfarads. If the output impedance of the amplifier is considered, the equation for effective open-loop gain, A′(s), becomes

$$A'(s) = A(s)\frac{R_p}{R_p + R_o}\frac{1}{1 + R_qC_Ls}$$

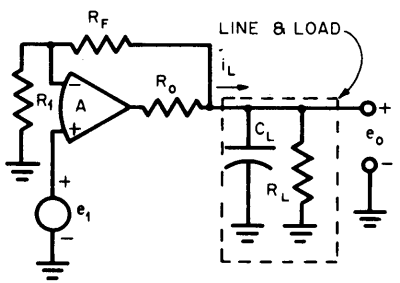


Fig. 6.19 Line-driving amplifier.

where

$$R_p = \frac{1}{1/R_F + 1/R_L} \qquad R_q = \frac{1}{1/R_F + 1/R_L + 1/R_o}$$

where A(s) is the unloaded open-loop gain, and R_o is the dynamic output impedance of the operational amplifier. If A(s) is approximated by a single-pole transfer function

$$A(s) = \frac{A_o}{1 + s/\omega_o}$$

then the effective (loaded) open-loop gain becomes

$$A'(s) = \frac{R_p}{R_p + R_o} \frac{A_o}{1 + s/\omega_o} \frac{1}{1 + R_q C_L s}$$

A Bode plot of this transfer function, for $s = j\omega$, is shown in Fig. 6.20, along with a plot of the unloaded open-loop gain. Note that the effect of the resistive loading is to reduce the open-loop gain, lowering the entire curve. Thus resistive loading alone reduces the unity-gain bandwidth and will consequently reduce closed-loop bandwidth by the same factor. This bandwidth reduction factor is extremely important for fast line drivers since the very low impedance of the line can severely degrade the bandwidth unless the operational amplifier has very low output impedance. The capacitive component of load impedance introduces another pole in the gain function at $s = -1/R_qC_L$. This causes an additional "break" in the frequency response and a rolloff of −12 dB per octave above the frequency $\omega = 1/R_qC_L$. If the closed-loop gain curve intersects this section of the effective open-loop gain curve, the amplifier will be marginally stable with unacceptable transient response.

There are a number of techniques for dealing with the problems of loading. The most satisfactory of these is to choose an amplifier with very low open-loop output impedance or to create one by adding a power booster stage to an available operational amplifier. This will reduce the

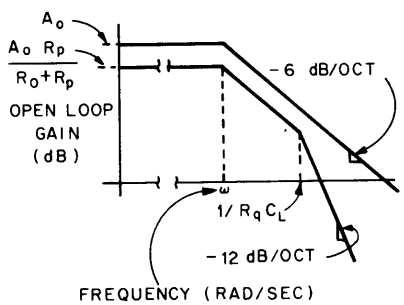


Fig. 6.20 Effect of loading on open-loop gain.

gain and bandwidth loading factors caused by the load resistance and will increase the frequency at which the additional pole occurs. The higher in frequency this pole occurs, the more stable the closed-loop response will be. The power output stage also supplies the current necessary to meet the condition

$$i_{L\,max} = C_L \left(\frac{de_o}{dt}\right)_{max}$$

As an example, the amplifier must be capable of supplying 63 mA to the capacitive load if $C_L = 10{,}000$ pF and the output voltage is a 10-V sine wave at 100 kHz.

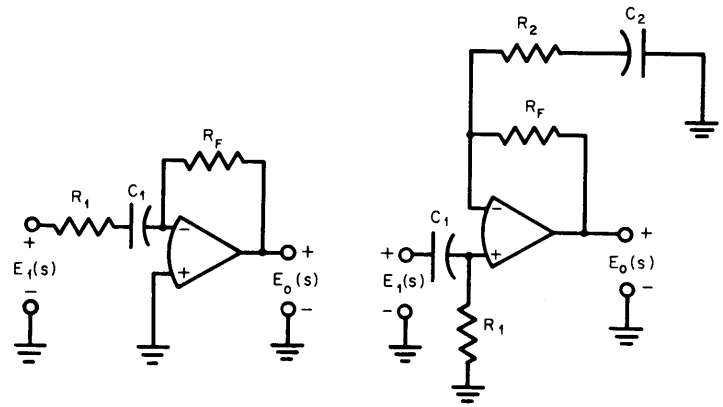
6.6 AC-coupled Feedback Amplifiers[2,6]

Although the operational amplifier is designed to amplify dc signals, it has a rather broad frequency response and is consequently quite useful for strictly ac signals. The feedback network can be tailored for exactly the desired passband. One of the simplest ac amplifiers is that shown in Fig. 6.21a, where the closed-loop gain is given by

$$\frac{E_o}{E_i}(s) = -\frac{R_F}{R_1}\frac{s}{s + 1/R_1C_1}$$

The dc gain is zero, and the high-frequency gain approaches $-R_F/R_1$. The lower cutoff frequency is

$$f_c = \frac{1}{2\pi R_1 C_1}$$



(a) INVERTING CIRCUIT (b) NONINVERTING CIRCUIT

Fig. 6.21 Ac-coupled feedback amplifiers.

The dc output offset voltage E_{OS} is equal to the dc input offset voltage, plus the dc offset voltage generated by the input bias current flowing through R_F.

$$E_{OS} = V_{OS} \times 1.0 + I_{B1}R_F$$

A noninverting ac amplifier is shown in Fig. 6.21b. The response is given by

$$\frac{E_o}{E_1}(s) = \frac{s}{s + 1/R_1C_1} \frac{(R_2 + R_F)C_2s + 1}{R_2C_2s + 1}$$

Both of the circuits of Fig. 6.21 have relatively low input impedance above the cutoff frequency, determined by the resistors denoted R_1 in both cases.

The circuit of Fig. 6.22 is an ac amplifier whose input impedance is "bootstrapped" to a high value. Resistor R_2 provides a decoupling for dc input signals. However, for high-frequency signals the voltage across R_2 becomes very small. Consequently, very little current flows through R_2, and the effective input impedance is very high.

The analysis of the circuit is greatly simplified if it is assumed that $e_2 = e_4$ $(A \rightarrow \infty)$. Then we may write the equations

$$\frac{e_1 - e_2}{X_2} = \frac{e_2 - e_3}{R_2}$$

$$\frac{e_o - e_2}{R_F} = \frac{e_2 - e_3}{X_1}$$

$$\frac{e_2 - e_3}{R_2} + \frac{e_2 - e_3}{X_1} = \frac{e_3}{R_1}$$

where

$$X_1 = \frac{1}{j\omega C_1} \quad \text{and} \quad X_2 = \frac{1}{j\omega C_2}$$

If these equations are solved for e_2, the input impedance may be calculated from

$$Z_{in} = \frac{e_1}{i_{in}} = \frac{e_1X_2}{e_1 - e_2}$$

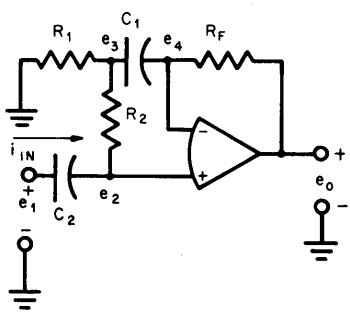
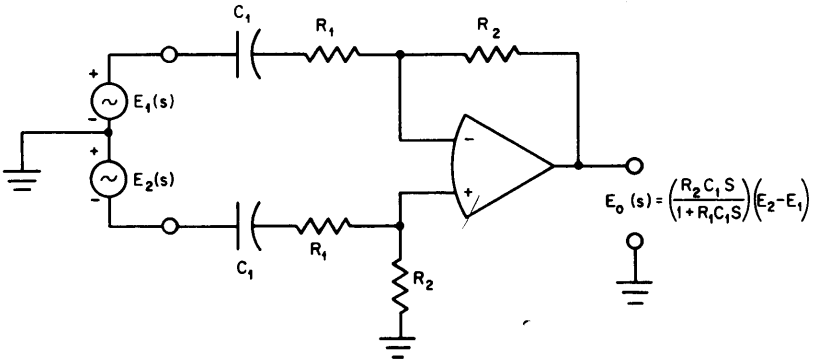


Fig. 6.22 Bootstrapped ac amplifier.

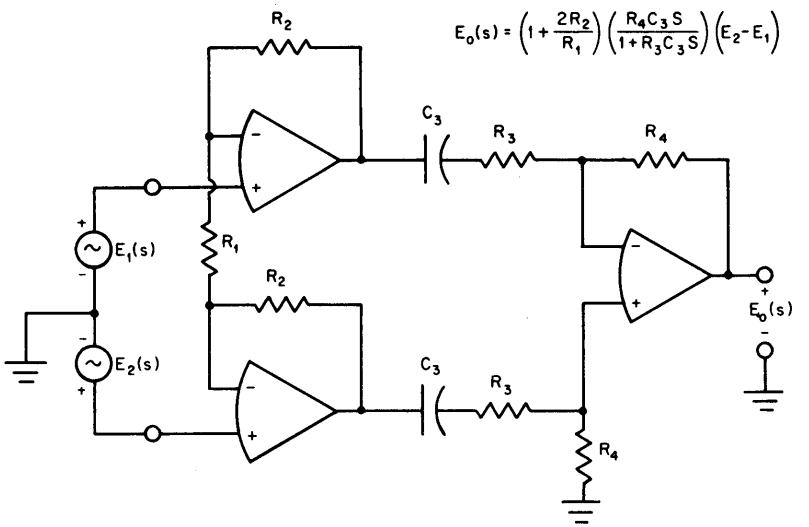
which yields

$$Z_{in} = X_2 + R_2 + R_1 + \frac{R_1 R_2}{X_1}$$

As the frequency increases, X_1 and X_2 approach zero and the input



(a) SIMPLE ONE-AMPLIFIER CIRCUIT



(b) HIGH INPUT IMPEDANCE CIRCUIT

Fig. 6.23 Differential ac amplifiers. (a) Simple one-amplifier circuit; (b) high input impedance circuit.

impedance becomes very large. As frequency increases still further, the open-loop gain decreases and the condition $e_2 = e_4$ is no longer enforced. The input impedance then decreases.

Differential ac amplifiers are also easily realized through the use of operational amplifiers. Two examples are shown in Fig. 6.23. That of Fig. 6.23a introduces simple dc decoupling into the familiar differential DC amplifier circuit. The circuit of Fig. 6.23b provides high input impedance while decoupling dc signals in the second stage. The dc offset voltages of the first-stage amplifiers are removed by the capacitive coupling. The dc offset voltage of the second-stage amplifier is multiplied by the dc gain, 1.0.

6.7 Voltage-to-Current Converters[2,7]

In applications such as coil driving and transmission of signals over long lines, it is sometimes desirable to convert a voltage to an output current. With operational amplifiers this is quite easily done. Several realizations of the voltage-to-current converter (VIC) will be examined in this section.

The simplest VICs are those for floating loads. The circuits of Fig. 6.24a and b are the prime examples of this type. The circuit of Fig. 6.24a is a simple inverting circuit. The input current is given by

$$i_1 = \frac{e_1}{R_1}$$

since R_1 is terminated at the virtual ground of the summing junction. This same current flows through the feedback load impedance Z_L in the feedback loop. The current i_1 is independent of the value of Z_L. Both the signal source and the operational amplifier must be capable of supplying the desired amount of load current. The circuit of Fig. 6.24b

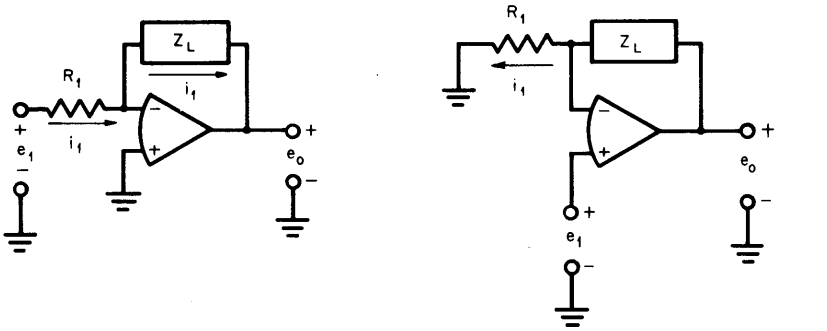


Fig. 6.24 Voltage-to-current converters, floating load.

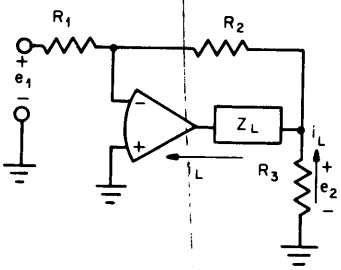


Fig. 6.25 Current amplifying circuit.

operates in the noninverting mode and, hence, presents a high impedance to the driving source. The current is again given by the equation

$$i_1 = \frac{e_1}{R_1}$$

and, again, i_1 is the load current. Very little current, however, is required from the signal source, because of the high input impedance of the noninverting amplifier.

Another VIC for a floating load is shown in Fig. 6.25. Here, most of the current is provided by the amplifier and only a small portion by the signal source. Analysis of the circuit yields the following equation for load current:

$$i_L = \frac{e_1}{R_1}\left(1 + \frac{R_2}{R_3}\right)$$

The resistor R_3 provides a convenient means for scaling the current. The resistor R_1 can be made relatively large to minimize the loading of the signal source. The amplifier must be capable of providing all the current to the load and must also be capable of output voltage equal to

$$e_{o\,max} \approx i_{L\,max}(Z_L + R_3)$$

For loads which are grounded on one side, there are also circuits which give voltage-to-current conversion. The single amplifier circuit of Fig. 6.26 acts as a current source controlled by e_1,

$$i_L = -\frac{e_1}{R_2}$$

if

$$\frac{R_3}{R_2} = \frac{R_F}{R_1}$$

If these ratios of resistances are matched, the circuit will function as a true source of current with very high internal impedance. A mismatch of the ratios will be seen as a decreased internal impedance of the current source. Fluctuations in effective load impedance will then cause fluctua-

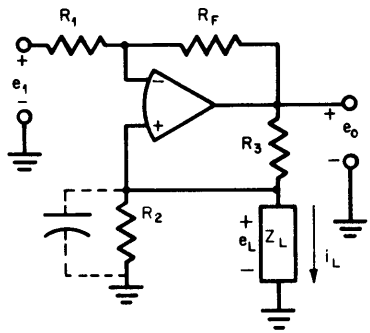


Fig. 6.26 VIC, grounded load.

tions of the output current. The operational amplifier for the circuit of Fig. 6.26 must have an output voltage range sufficient to provide the maximum load voltage plus the voltage drop across R_3. Normally, R_1 and R_2 will be chosen to draw small currents, and R_F and R_3 will be made small to minimize voltage drops.

The circuit of Fig. 6.27 utilizes two inverting amplifiers to drive a current into a grounded load. This current is given by the expression

$$I_L = e_1 \frac{R_5R_F/R_4R_1}{R_3 + Z_L[1 + R_3/R_2 - (R_5/R_4)(R_F/R_2)]}$$

If resistors are selected so that

$$1 + \frac{R_3}{R_2} = \frac{R_5R_F}{R_4R_2}$$

then

$$i_L = \frac{e_1}{R_3}\frac{R_5R_F}{R_4R_1}$$

In particular, if

$$R_1 = R_F = R_4 = R_5$$

then

$$i_L = \frac{e_1}{R_3}$$

and

$$R_2 = R_F - R_3$$

If R_1 is large, very little current is drawn from the signal source and very little flows through the feedback elements. Then the output voltage is given by

$$e_{o\,max} \approx I_{L\,max}(Z_L + R_3)$$

Note that, in the circuits of Figs. 6.26 and 6.27, when the load is open-circuited the positive feedback is equal to the negative feedback. This is

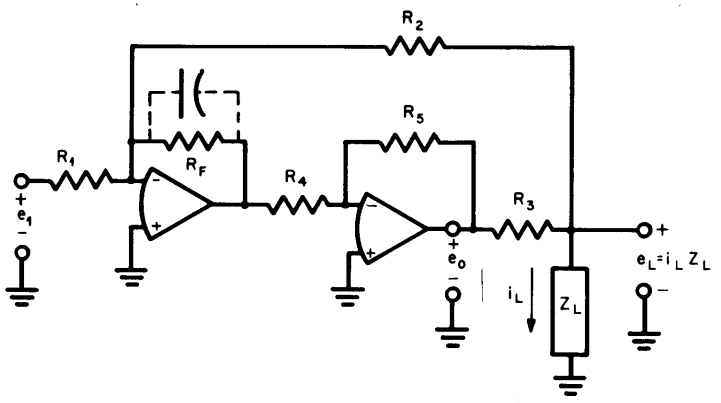


Fig. 6.27 Two-amplifier VIC, grounded load.

equivalent to an open-loop condition. The stabilizing capacitors shown by dotted lines are therefore desirable to prevent excessive noise and possible oscillations. Figure 6.28 illustrates a modified form of the two-amplifier VIC which provides the additional feature of very high input impedance. The expression for output current as a function of input voltage is

$$i_L = \frac{e_1(R_5/R_4)(1 + R_F/R_2 + R_3/R_2)}{R_3 + Z_L(1 + R_3/R_2 - R_5R_F/R_2R_4)}$$

If we again select resistors such that

$$1 + \frac{R_3}{R_2} = \frac{R_5R_F}{R_2R_4}$$

and

$$R_F = R_4 = R_5$$

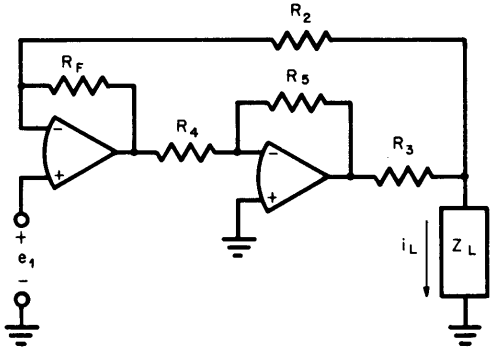


Fig. 6.28 Buffered VIC, grounded load.

then

$$i_L = \frac{2e_1R_F}{R_2R_3}$$

and

$$R_2 = R_F - R_3$$

6.8 Reference Voltage Sources and Regulators[2,6,7]

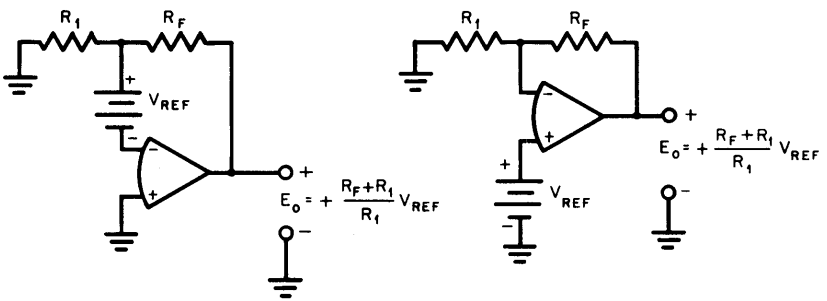
Because of its high input impedance and easily adjustable gain, the operational amplifier may be used as a reference voltage source with very low output impedance and substantial output current capability. Two circuits for use with standard cells are shown in Fig. 6.29. In both instances the output voltage is given by

$$E_o = V_{REF}\left(1 + \frac{R_F}{R_1}\right)$$

The circuit of Fig. 6.29a can be used with single-ended amplifiers (such as chopper-stabilized types), as well as those with differential input. The circuit of Fig. 6.29b is used if the reference source or cell must be grounded on one side. The only current drawn from the cell is the input bias current of the amplifier plus a term given by

$$I_i = \frac{E_o}{AR_i} = \frac{V_{REF}(1 + R_F/R_1)}{AR_i}$$

where R_i is the differential input impedance of the operational amplifier. This component of current is negligible in comparison with bias current for most amplifiers. The reference voltage cell is, for all practical purposes, isolated from any load being driven. The effective output



(a) SINGLE-ENDED CIRCUIT (b) NONINVERTING CIRCUIT

Fig. 6.29 Reference voltage sources.

impedance R_{OUT} is given by

$$R_{OUT} = \frac{R_o}{A\beta}$$

where

$$\beta = \frac{R_1}{R_1 + R_F}$$

and

R_o = open-loop output impedance

The load regulation is therefore given by

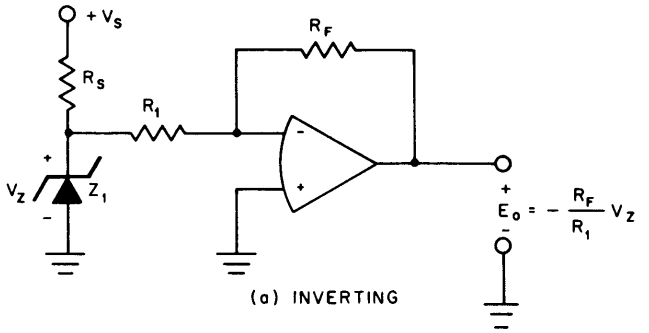
$$\text{Regulation } \% = \frac{R_o}{A\beta R_L} \times 100$$

where R_L is the minimum load impedance.

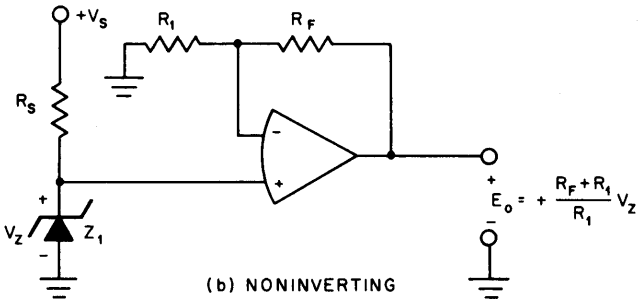
Similar circuits for use with zener diodes are shown in Fig. 6.30a and b. The loading conditions on the zener diodes are constant and the load regulation is the same as derived for the circuits of Fig. 6.29. Regulation with respect to the input voltage V_s depends upon the dynamic resistance of the reference zener diode Z_1. The circuit of Fig. 6.29c further reduces this regulation due to input voltage by providing the output reference voltage as the source for the zener diode current. The dc voltage V_s now functions only as a "startup" voltage through the network of R_2, R_3, and D_1.

6.9 Voltage Regulators

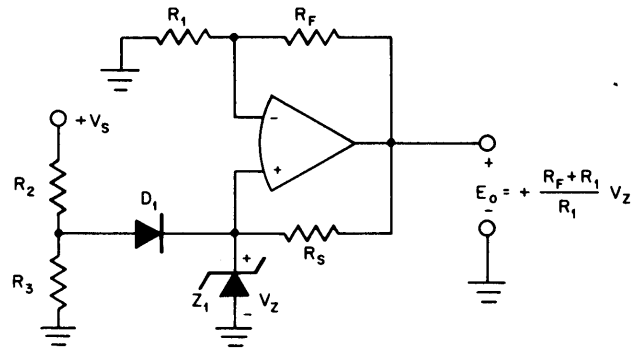
Any one of the voltage references described in the preceding section may be considered a voltage regulator, with extremely tight regulation characteristics. Where higher output currents are required, a power booster can be added, inside the feedback loop. However, in speaking of voltage regulators, it is more usual to consider operation from a single source of unregulated dc voltage, rather than the dual supplies tacitly assumed in the reference voltage circuits. Figure 6.31 shows such a regulator. The amplifier, which normally operates on dual power supplies of opposite polarity, is biased for operation on a single unregulated power supply. The negative supply terminal is grounded and the noninverting input is biased at the zener voltage. The zener diode Z_1 operates at constant load current, since the output current is provided by the transistor Q_1. If the amplifier has a minimum (balanced) supply rating of $\pm V_m$, then V_s must be larger than $2V_m$. Similarly, if $\pm V_M$ is the maximum (balanced) supply rating, V_s must not exceed $2V_M$. The amplifier will saturate as the output voltage approaches either supply voltage. This determines



(a) INVERTING



(b) NONINVERTING



(c) NONINVERTING WITH REGULATED ZENER DRIVE

Fig. 6.30 Zener reference sources.

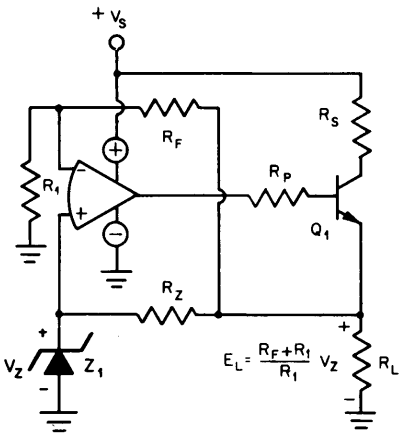


Fig. 6.31 Voltage regulator.

the limit on output; the common-mode voltage range sets the lower limit on zener voltage.

Although the amplifier may have an internal current limit, the resistor R_p is required to protect against short circuit in this type of regulator. This is because a short circuit to ground is equivalent to a short circuit to negative supply. This causes a power dissipation equal to twice that of a short circuit to ground when operating on balanced dual supplies. Thus the internal protection may not be sufficient. The value of R_p should be chosen to limit the amplifier short-circuit current to approximately one-half the internal current limit value when the output is at positive saturation voltage. The resistor R_s provides current limiting to protect Q_1.

The load regulation of this type of regulator can exceed 0.01 percent, since the effective output impedance is very low. The line regulation is increased beyond that of the zener by using the output voltage as excitation for the zener.

6.10 Current Amplifiers

Current amplifiers, or current-to-voltage converters, are realized very simply by using operational amplifiers. An ideal current source has infinite output impedance and output current which is independent of load. Photocells and photomultiplier tubes are basically current sources with output impedance which is finite but very large. For small load impedances, the output impedance may be considered infinite.

The current-to-voltage converter of Fig. 6.32 presents almost zero load impedance to ground because the inverting input appears as a virtual ground. The input current, however, flows through the feedback resistor,

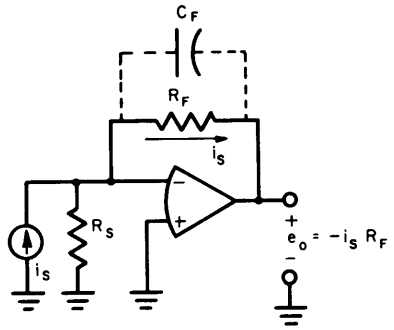


Fig. 6.32 Current amplifier (current-to-voltage converter).

generating an output voltage

$$e_o = -i_s R_F$$

The actual input impedance of the current-to-voltage converter, Z_{in}, taking into account the finite gain A and differential (open-loop) input impedance Z_{id}, is

$$Z_{in} = \frac{Z_{id}}{1 + (Z_{id}/R_F)(1 + A)} \approx \frac{R_F}{1 + A}$$

The lower limit on measurement of current input is determined by the bias current of the inverting input. For greatest resolution, FET or varactor bridge amplifiers are usually used.

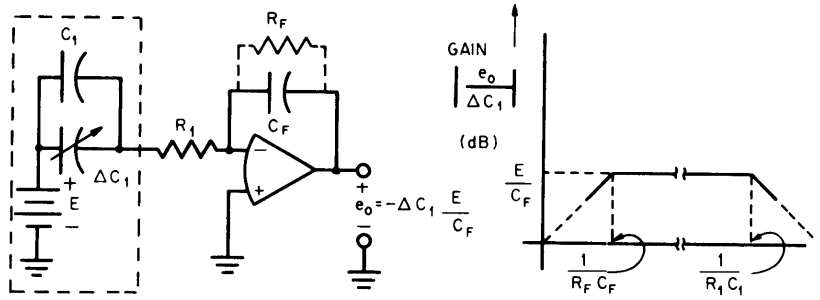
The gain of the amplifier for dc offset voltage and noise voltage is given by

$$\frac{R_F + R_s}{R_s} \approx 1.0 \qquad \text{since } R_s \gg R_F$$

Thus errors due to these parameters are very small. However, current noise can be a factor because of the very large impedances. Since most such measuring circuits are used for very low-frequency signals, it is usual to parallel R_F with a capacitor C_F to reduce the high-frequency current noise. Output impedance of the current-to-voltage converter is very low because of the nearly 100 percent feedback.

6.11 Charge Amplifiers

Some transducers, such as capacitance microphones and some types of accelerometers, operate on the principle of conversion of the measurement variable into an equivalent charge. The equivalent circuit of such a transducer may be represented by a battery and capacitor in series, as shown in Fig. 6.33a. As the capacitance varies, the charge also changes



(a) CHARGE AMPLIFIER CIRCUIT (b) FREQUENCY RESPONSE

Fig. 6.33 Charge amplifier operation.

according to the equation

$$\Delta q = \Delta C_1 E$$

When the transducer is connected to the inverting input of an operational amplifier as in Fig. 6.33a, this charge flows into the feedback capacitor C_F. The resultant change in charge on C_F generates an output voltage,

$$e_o = -\Delta C_1 \frac{E}{C_F}$$

Since the operational amplifier requires a dc path from each input to common (for bias current flow) it is necessary to insert the resistor R_F. In the absence of this resistor, the capacitors will build up a dc charge until the output voltage reaches saturation. This resistor limits the lower cutoff frequency of the charge amplifier. For stabilization purposes, and sometimes for protection of the amplifier input stage, it is also desirable to insert the series resistor R_1. This resistor limits the upper response frequency as shown in Fig. 6.33b.

The gain, or sensitivity of the charge amplifier, in its passband is given by

$$\frac{e_o}{\Delta C_1} = -\frac{E}{C_F}$$

and can be varied only by changes in C_F. It is usually desirable to use a small value of C_F consistent with the desired frequency response and a reasonable value of R_F. FET amplifiers are usually the first choice for charge amplification, because of their high input impedance, low bias current, and wide bandwidth.

Another common form of charge amplifier is shown in Fig. 6.34. Here the amplifier operates as a noninverting buffer with gain. Charge

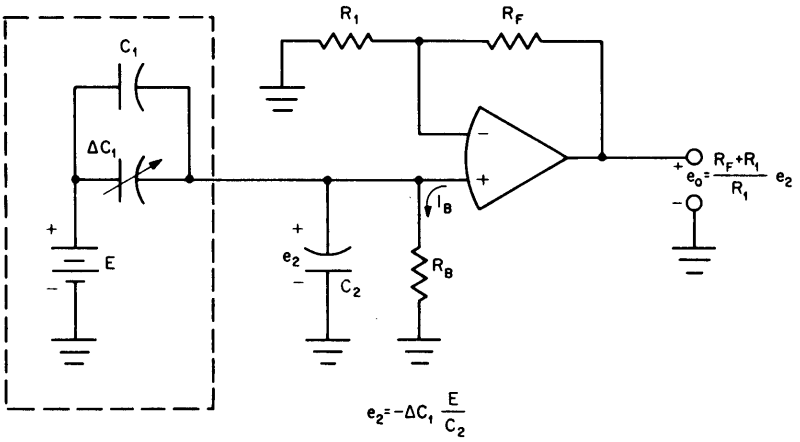


Fig. 6.34 Alternative charge amplifier circuit.

flows into, and out of, the capacitor C_2 as the capacitance of the transducer varies. Once again these capacitance variations are converted into voltage variations at the amplifier output. An amplifier with FET input stage is usually also required in this circuit to minimize the bias and noise currents. The resistor R_B provides the dc path for this bias current and limits the low-frequency response of the circuit.

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7

OPERATIONAL AMPLIFIERS IN NONLINEAR CIRCUITS

Some of the more interesting applications of operational amplifiers require the use of nonlinear feedback networks. By the use of such networks the amplifier with feedback can be made to approximate transfer curves, linearize transducers, limit the amplitude of signals, perform mathematical operations, and do a variety of other tasks. Basic to most of these nonlinear feedback networks is the use of the voltage-to-current characteristics of semiconductor junctions: diodes, zener diodes, and transistors. In some applications, the large-signal switching properties of such elements are used, whereas in others the nonlinearity of the junction itself is utilized. In this chapter we present a discussion of such circuits and their applications. Since the operation of diode limiter networks is basic to a great many of the circuits considered in this chapter, the first section is devoted to a brief discussion of the operation of these simple circuits. The remainder of the chapter treats feedback limiters, diode function generators, logarithmic amplifiers, and analog multipliers. Each of the sections concludes with a brief discussion of the primary areas of application for each functional circuit.

7.1 Diode Limiter Networks

In this section we present a discussion of idealized series and shunt limiter networks. The operation of these may be best understood by first considering some basic models for limiters.

7.1.1 Basic limiter models[1,4,6] The idealized model for the limiting element consists of an ideal diode in series with a floating bias source, as shown in Fig. 7.1a. When the signal voltage equals the bias voltage, the ideal diode conducts, with the amount of current dependent upon the resistance of the circuit containing the limiter. A series limiter is shown in Fig. 7.1b along with its transfer curve. For input voltage less than V_B the diode D is nonconducting and output voltage is zero. When e_i exceeds V_B, the output voltage follows the input. The shunt limiter of Fig. 7.1c provides an alternative means of obtaining an abrupt transition in the slope of the transfer curve. For output voltage e_o less than V_B the diode is nonconducting, and the circuit acts as a simple resistive divider. As input voltage is increased, however, the output eventually reaches the value V_B, and the diode begins to conduct, thus preventing further increases in e_o.

Both the series limiter and the shunt limiter find useful application as a part of the feedback network of an operational amplifier. Figure 7.2 illustrates a simple inverting amplifier circuit in which a diode and series bias source are used to provide a limit on the output voltage of an operational amplifier. For output voltage less than V_B, the output is a simple linear function of the input voltage with gain equal to the ratio $-R_F/R_1$. When the output reaches V_B the diode conducts, preventing further increase in e_o. If the input voltage increases still further, the additional input current passes through the limiting elements, generating no additional voltage at the output. The summing point remains at a virtual ground. Actually, of course, all practical limiting circuits will have some internal impedance, usually nonlinear, which modifies the ideal behavior described here. Also, floating bias sources are rather impractical in most cases and must be approximated by other means. These more practical limiters are discussed in the following sections.

7.1.2 Series limiters A practical and very close approximation to the ideal series limiter discussed above is achieved through the use of a silicon diode and a zener diode as shown in Fig. 7.3a. When the input voltage exceeds the sum of the zener voltage and the forward voltage of the silicon diode, the combination conducts. The output voltage then approximately follows the input. Because the two diodes have finite

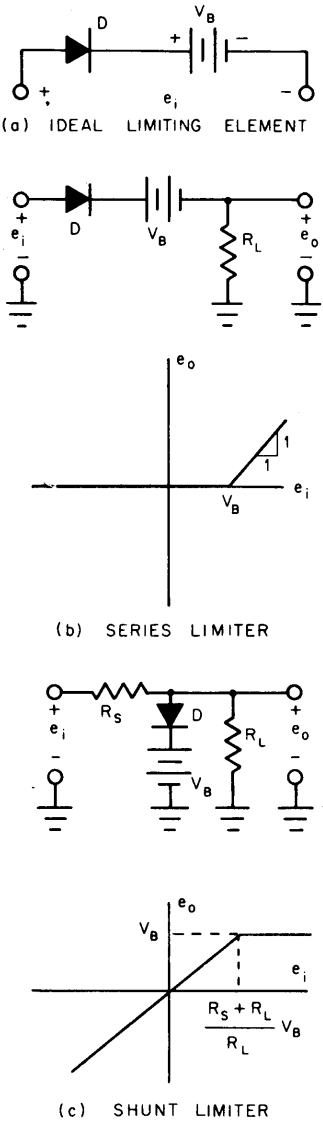
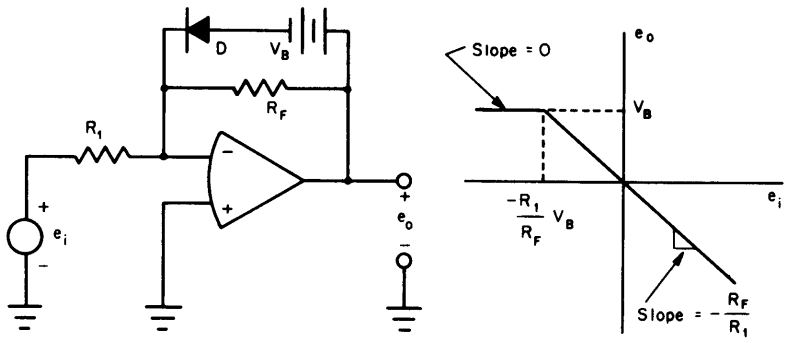


Fig. 7.1 Limiter concepts: (a) ideal limiting element; (b) series limiter; (c) shunt limiter.

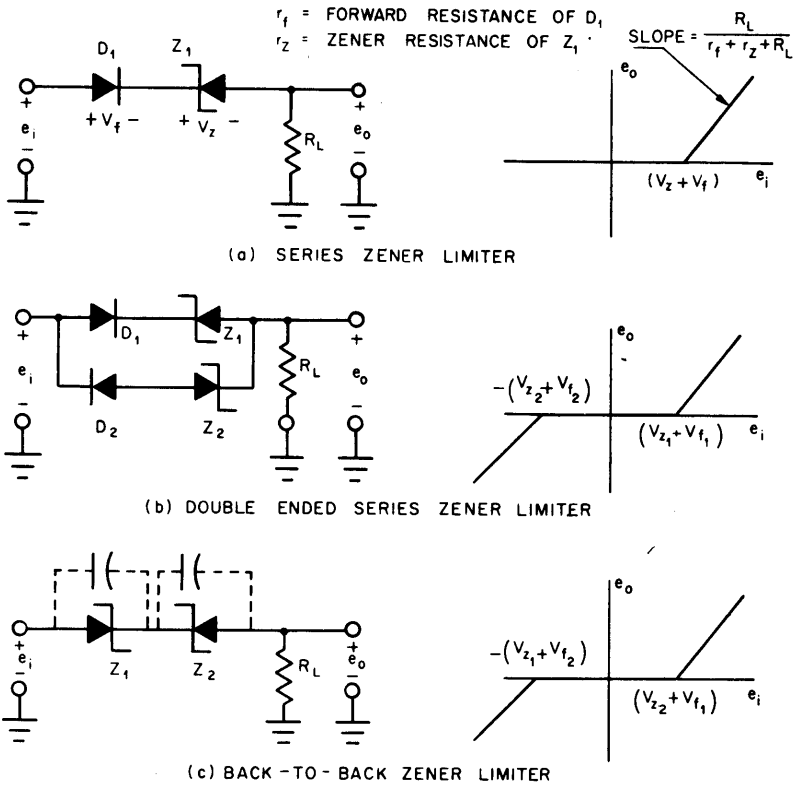
ON resistances, the output does not follow the input exactly but is attenuated slightly by this series resistance. A double series limiter can be formed as shown in Fig. 7.3b by paralleling two such combinations of diodes in opposite polarities.

An even simpler method of obtaining a double series limiter is to use



(a) FEEDBACK LIMITER ON INVERTING AMPLIFIER (b) TRANSFER FUNCTION

Fig. 7.2 Operation of a feedback limiter. (a) Feedback limiter on an inverting amplifier; (b) transfer function.



(a) SERIES ZENER LIMITER

(b) DOUBLE ENDED SERIES ZENER LIMITER

(c) BACK-TO-BACK ZENER LIMITER

Fig. 7.3 Series limiters using zener diodes: (a) series zener limiter; (b) double-ended series zener limiter; (c) back-to-back zener limiter.

back-to-back zeners, as shown in Fig. 7.3c. Here the function of the silicon diodes is served by the zener diodes in their forward-conducting region. This circuit suffers from the high junction capacitance of the zeners and may present feedthrough problems at high frequency. The method of Fig. 7.3b is somewhat superior in this respect, especially if low-capacitance silicon diodes are used for D_1 and D_2. The transition between the ON and OFF states will actually not be a sharp one, as shown in the figure, but will have a degree of rounding determined by the diode and zener characteristics and by the value of the load resistor R_L. This resistor could equally well be the summing resistor of an operational amplifier network. In this case, it would be terminated in a virtual ground instead of true ground.

Another type of series limiter is shown in Fig. 7.4. Here the biasing is accomplished through the use of an external reference voltage and a shunt resistor. The diode begins conducting when the junction voltage e_i exceeds the forward voltage drop of the diode. The breakpoint voltage V_B is given by the expression $V_B = V_f(1 + R_1/R_2) + V_R(R_1/R_2)$ and can easily be varied by adjustment of R_2. Such limiters are useful in the piecewise approximation of functions, a topic to be discussed later in the chapter.

7.1.3 Shunt limiters A simple means of realizing a shunt limiter is shown in Fig. 7.5a where, again, the combined silicon diode and zener diode are used as the actual limiting elements. The circuits of Fig. 7.5b and c are actually the duals of the double series limiting elements of Fig. 7.3. The circuit of Fig. 7.5b achieves lower shunt capacitance than that of 7.5c and is therefore preferable for high-frequency applications.

As another approach to shunt limiting, the resistive divider shunt limiter of Fig. 7.6a is quite useful where it is necessary to accurately adjust the breakpoint voltage V_B. When the output voltage e_o equals the reference voltage V_R, plus the diode forward voltage, the diode conducts and prevents further increase in e_o. The actual value of input voltage at which the breakpoint occurs is determined by the ratio of R_1

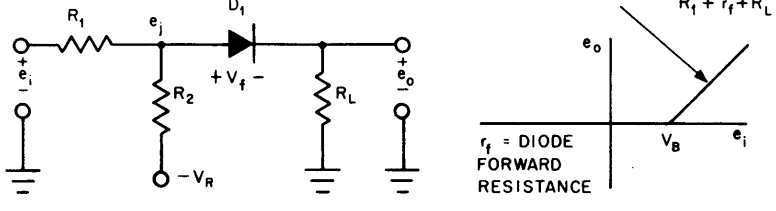


Fig. 7.4 Externally biased series limiter.

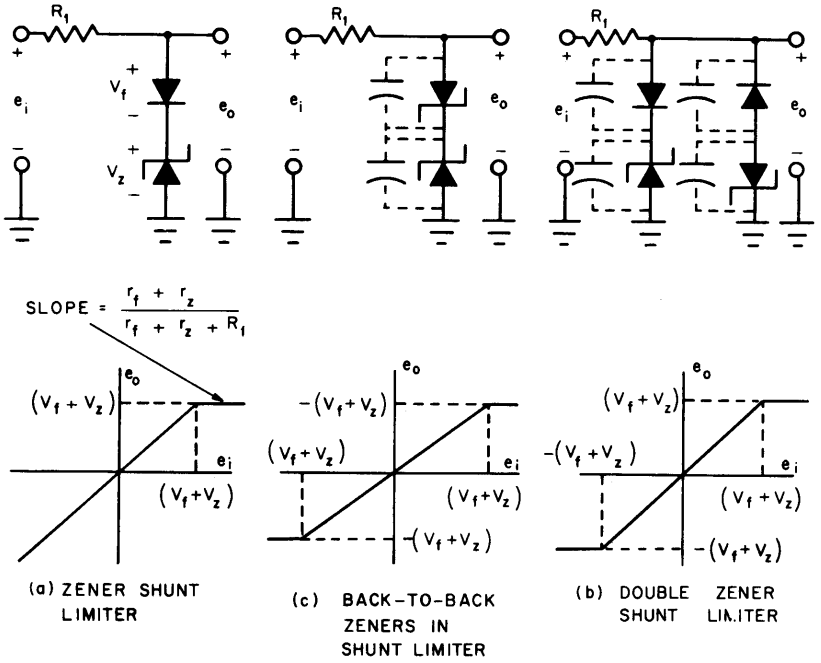


Fig. 7.5 Practical shunt limiters: (a) zener shunt limiter; (b) double zener shunt limiter; (c) back-to-back zeners in a shunt limiter.

and R_L and by the value of V_R.

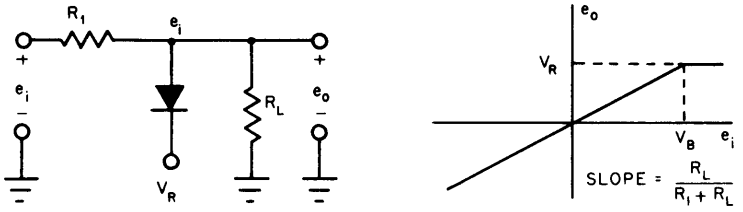
$$V_B = V_R \frac{R_L + R_1}{R_L}$$

An additional, negative breakpoint can easily be achieved, as in Fig. 7.6b, by adding another diode and reference source.

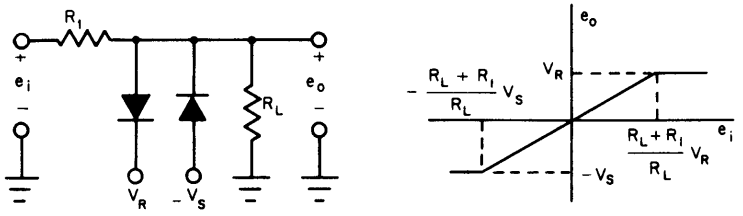
Another practical limiter circuit is the bridge limiter circuit of Fig. 7.7. This is actually a form of shunt limiter which provides a double limit and partial compensation of the temperature-sensitive characteristics of the diodes. The breakpoints, of course, still exhibit rounding because of the gradual turnoff of the diodes. The breakpoint voltages, or limits, are easily varied through the bias resistors R_1 and R_2, or by varying $+V_c$ and $-V_c$.

7.2 Feedback Limiters[1,2,4,6]

In the preceding section we discussed the operation of several series and shunt limiting networks. In this section we will illustrate some circuits which use networks of this type to obtain feedback limiting. Three dif-



(a) SIMPLE EXTERNALLY BIASED SHUNT LIMITER



(b) DOUBLE SHUNT LIMITER WITH EXTERNAL BIASING

Fig. 7.6 Externally biased shunt limiters: (a) simple externally biased shunt limiter; (b) double shunt limiter with external biasing.

ferent approaches will be considered. They are resistive ratio methods, zener diode feedback limiters, and precision limiters.

7.2.1 Resistive ratio methods In the feedback limiter, series or shunt limiting networks provide an abrupt change in the feedback ratio, and hence the closed-loop gain, of the operational amplifier. The resistive divider feedback circuit of Fig. 7.8a makes use of a simple series limiting

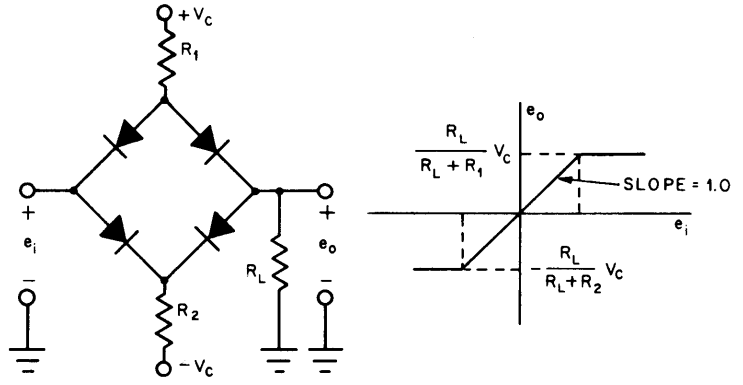
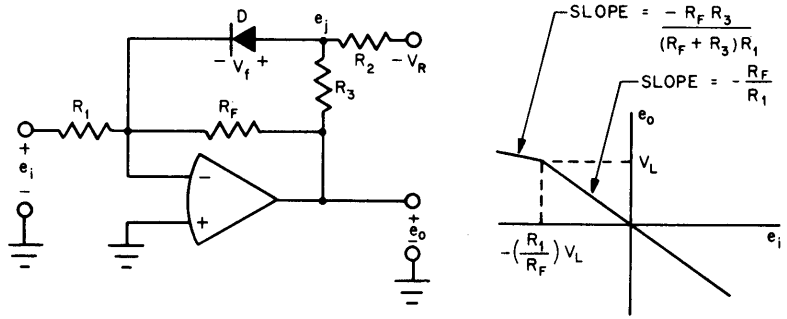


Fig. 7.7 Diode bridge limiter.

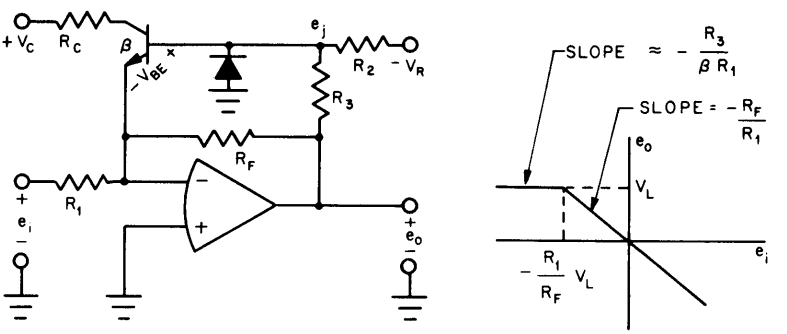
circuit. The diode begins conduction when the voltage e_j exceeds the forward voltage V_f. The output voltage is then limited at the value

$$V_L = \frac{R_3}{R_2} V_R + \left(1 + \frac{R_3}{R_2}\right) V_f$$

The gain before limiting is $-R_F/R_1$ and, after the limit occurs, is $-R_F R_3/(R_F + R_3)R_1$. The slope, or gain, in the limit region can be made to approach zero if $R_3 \ll R_1$. Since such small values of R_3 may be impractical, the circuit of Fig. 7.8b may be used to obtain slope ≈ 0. This is done by adding a transistor to the circuit. This transistor then provides the necessary current to the summing junction while drawing only relatively small base current through R_3. Total current into the summing point remains zero both before and after limiting occurs. The diode to ground protects the transistor from reverse breakdown of the base emitter junction. The limit voltage in this case is given by the



(a) SIMPLE FEEDBACK LIMITER



(b) FEEDBACK LIMITER WITH TRANSISTOR

Fig. 7.8 Resistive divider feedback limiters: (a) simple feedback limiter; (b) feedback limiter with a transistor.

expression

$$V_L = \frac{R_3}{R_2} V_R + \left(1 + \frac{R_3}{R_2}\right) V_{BE}$$

The circuits of Fig. 7.8 are quite useful because of the ease with which the limiting level can be varied. If a "soft" limit is sufficient, the circuit of Fig. 7.8a is used. If "hard" limiting is necessary, the transistor limiter of Fig. 7.8b is preferable. Both circuits suffer from the temperature sensitivity of the diode and transistor forward voltage drops, V_f and V_{BE}. Also, they cannot limit at voltages smaller than V_f or V_{BE}. The capacitance of these limiters is rather low; consequently they perform well in high-frequency applications.

7.2.2 Zener diode feedback limiters Two circuits which may be categorized as zener diode feedback limiters are shown in Fig. 7.9.

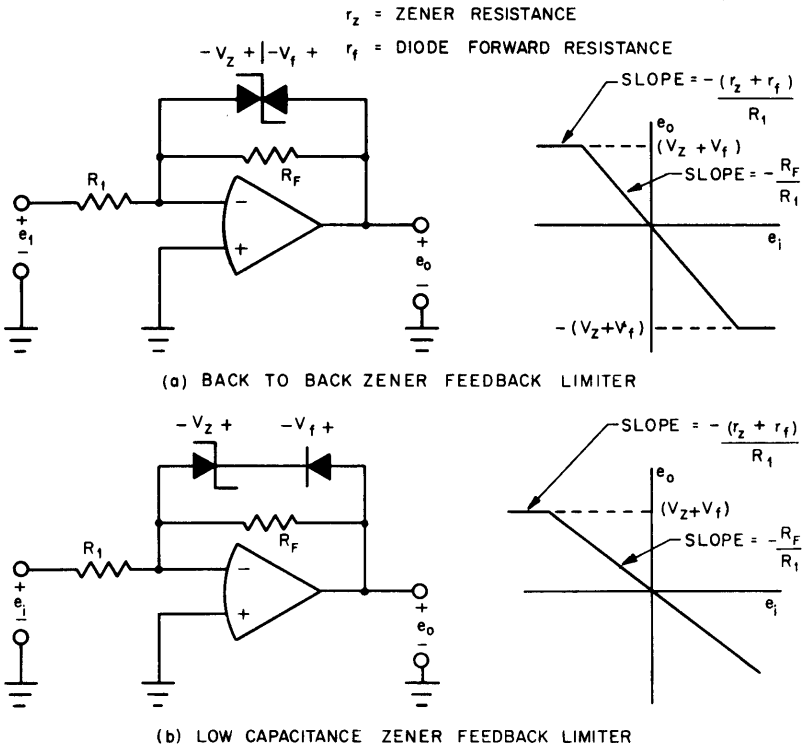


Fig. 7.9 Zener diode feedback limiters: (a) back-to-back zener feedback limiter; (b) low capacitance zener feedback limiter.

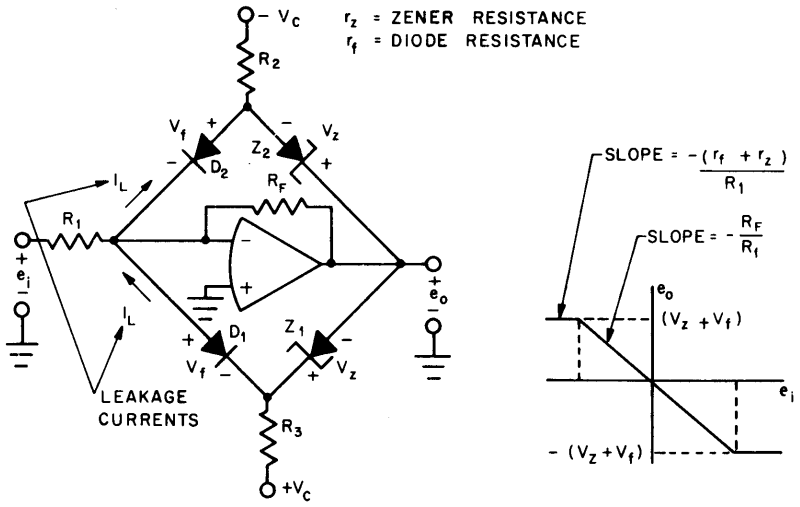


Fig. 7.10 Zener diode bridge feedback limiter.

Either of these limiters works satisfactorily at low frequency. The circuit of Fig. 7.9b provides lower capacitance than that of 7.9a and therefore is better at high frequency. The limits are set by the zener voltage and forward voltage drop of the diode. For good limiting action, the ON value of resistance of the diodes must be negligible in comparison with R_F and the OFF resistance must be much larger than R_F. Zener diodes selected for such limiters should have a sharp "knee" to avoid distortion of the transfer curve as the output voltage approaches its limit. Another zener diode feedback limiter is the bridge circuit shown in Fig. 7.10. This is a double-ended version of the zener limiter of Fig. 7.9b with the addition of external biasing to obtain sharper transition between the ON and OFF regions of the limiter. The small leakage currents through the silicon diodes in the OFF state will tend to cancel at the summing junction. In applying the circuits shown in Figs. 7.9 and 7.10, it should be noted that zener diode limiters are useful mainly for protection against overvoltage and not as a means of obtaining precisely known limits for signal processing or computation purposes.

7.2.3 Precision limiters As discussed in earlier sections, the actual limiting elements (diodes, zener diodes, and transistors) have finite resistance and nonlinear temperature-sensitive switching characteristics. These characteristics contribute to a "rounding" of the breakpoint area of the limiter characteristics as illustrated in Fig. 7.11. Ideally, the breakpoint would be sharp and well defined, plus being insensitive to

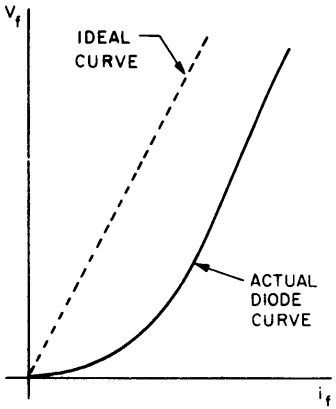
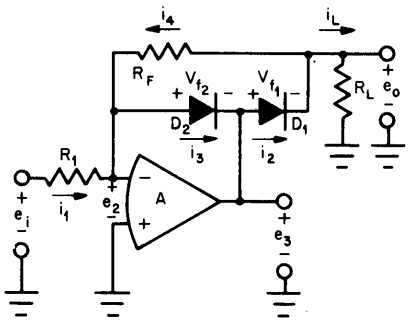


Fig. 7.11 Practical limiter characteristic near the breakpoint.

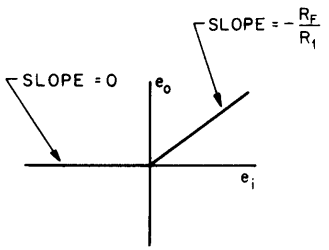
temperature. Circuits which achieve such characteristics are referred to as precision limiters. In the precision limiter of Fig. 7.12, the high open-loop gain of the operational amplifier is used to reduce the effect of the diode nonlinearity and temperature sensitivity. The operation of the circuit can be analyzed by the usual techniques except that the relationship of current and voltage in the diodes must be taken into account. This relationship is given by

$$v_f = \frac{nkT}{q}[\ln (i_f - I_o) - \ln I_o] = f(i_f)$$

For silicon diodes this voltage has a maximum value of approximately +0.6 V for full-conduction. For $e_3 > 0$ ($e_1 < 0$) the current i_3 will be zero because $e_2 \approx 0$ and D_2 is back-biased. Essentially all input current



(a) PRECISION LIMITER CIRCUIT



(b) PRECISION LIMITER TRANSFER CURVE

Fig. 7.12 Precision limiter operation. (a) Precision limiter circuit; (b) precision limiter transfer curve.

i_1 flows through R_F, generating an output voltage

$$e_o = -R_F i_1 = -\frac{R_F}{R_1} e_i, \quad e_i < 0$$

If the finite amplifier gain and diode nonlinearity are taken into account, the expression becomes

$$e_o = \frac{(-R_F/R_1)e_i}{1 - (1/A\beta)[1 + f(i_2)/e_o]}$$

where

$$\beta = \frac{R_1}{R_1 + R_F}$$

Note that the effect of the diode forward voltage $f(i_2)$ is reduced by the loop gain $A\beta$ of the closed-loop circuit. Thus, the "rounding" of the turn-on region virtually disappears.

For $e_3 < 0$, diode D_1 no longer conducts and all the input current i_1 flows through D_2. Theoretically, the output voltage is then exactly equal to zero. The expression for e_o, considering finite gain and the diode nonlinearity, is

$$e_o \approx -\frac{f(i_1)}{A} \frac{R_L}{R_F + R_L}, \quad e_i > 0$$

This is an extremely small voltage, probably less than the dc offset voltage of the amplifier. Thus the precision limiter provides a good approximation of ideal diode behavior, reducing the diode nonlinearity, temperature sensitivity, and forward voltage drop by a factor equal to the loop gain of the amplifier. A simpler analysis of the precision limiter can be made where the diode is represented by the linear model of a resistance, a bias source, and an ideal diode. Using this analysis, it is seen that the effects of diode resistance and internal bias voltage are reduced by the same factor, $A\beta$.

Nonzero precision limits can also be achieved, using the circuit shown in Fig. 7.13. Here, a diode bridge limiter gives both positive and negative limits. Because the diode bridge is inside the feedback loop, the nonlinearity, temperature sensitivity, and forward resistance of the bridge are all reduced by the loop-gain factor. Thus the limits are sharp and relatively independent of diode parameters.

7.2.4 Applications of limiters The simple series and shunt limiters described earlier in this section are used extensively in diode function generators which are discussed in later sections of this chapter. The limiter applications to be discussed here are principally those for feed-

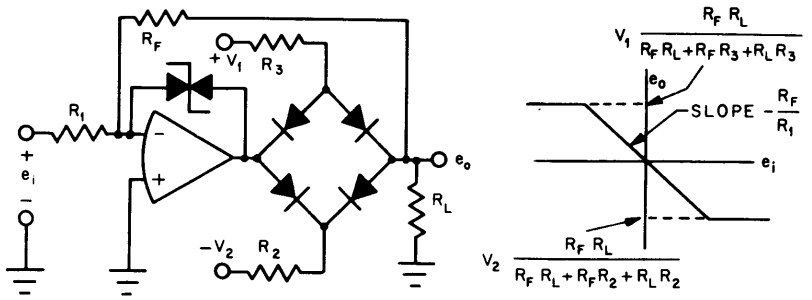


Fig. 7.13 Precision bridge limiter.

back limiters. As mentioned earlier, one of the primary reasons for using a feedback limiter is to prevent overload of the amplifier output stage. In many amplifiers, particularly chopper-stabilized types, a considerable time is required to recover from saturation of the output stage. The feedback limiter, by preventing such saturation, ensures fast recovery when the output voltage reaches the preselected limit. In circuits where input bias current is to be kept to a minimum, the bias current decoupling technique shown in Fig. 7.14 may be necessary. Here the resistor R_D shunts the bias current to ground since the diodes D_1 and D_2 are operating with zero voltage drop and zero current when the limiter is OFF. When the circuit is limiting, of course, the diodes conduct the feedback current.

Another of the basic applications for a feedback limiter is in comparator circuits. The limiter determines the ON and OFF voltage levels for the comparator output (see Chapter 9 for more details of comparators). As another application, limiters are often used with operational amplifiers for signal generation. Usually such use is in conjunction with a comparator for generation of square waves. Triangle and ramp wave-

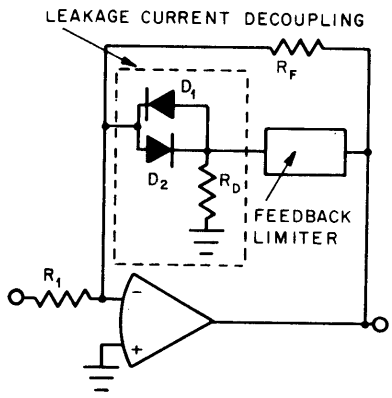
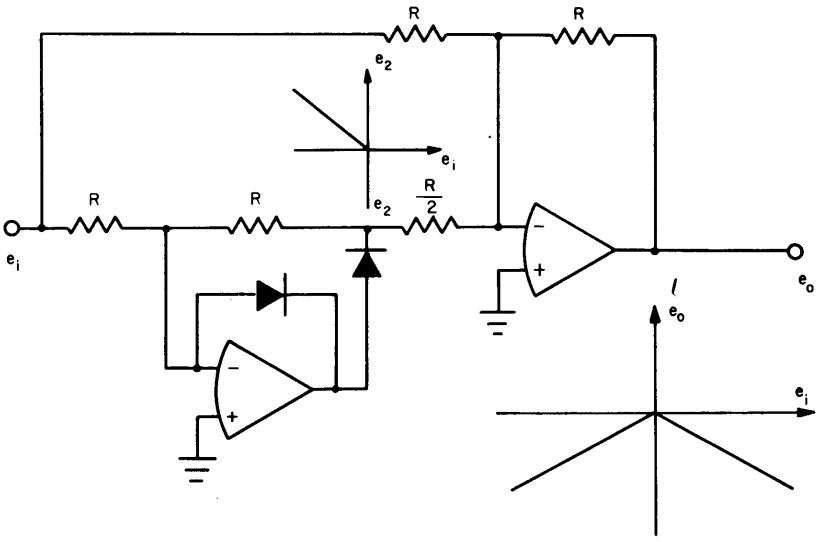
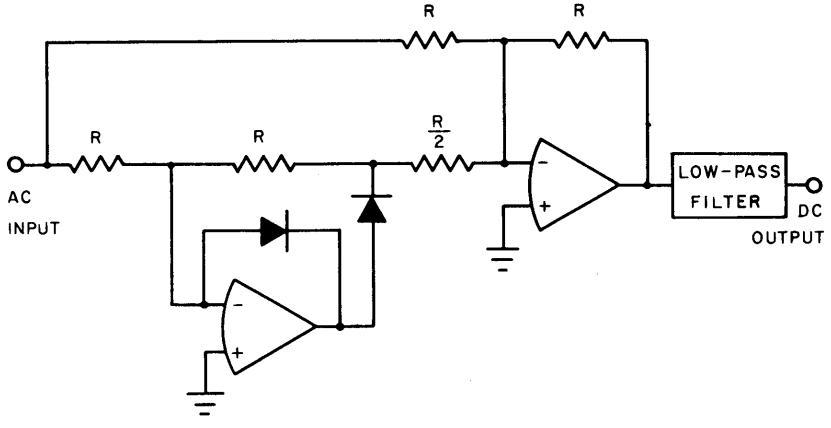


Fig. 7.14 Use of a leakage current decoupling circuit.



(a) ABSOLUTE VALUE CIRCUIT



(b) PRECISION A C TO D C CONVERSION

Fig. 7.15 Precision rectification. (a) Absolute-value circuit; (b) precision ac to dc conversion.

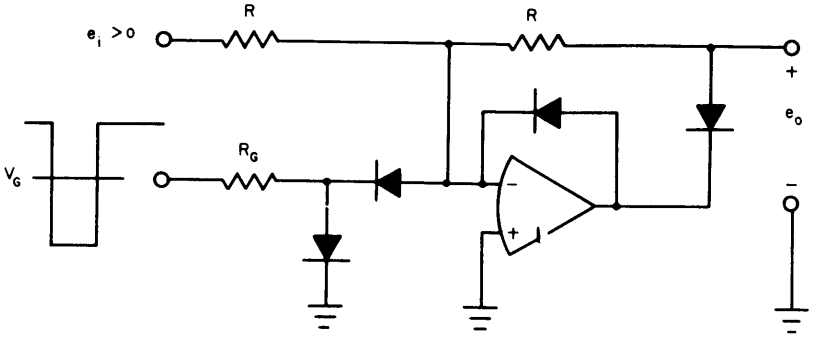


Fig. 7.16 Precision gate circuit.

forms can also be generated if an integrator follows the limiter or comparator (see Chapter 10 for more detail on signal generation).

Some limiters have breakpoints determined by an external reference voltage. Thus these levels can be easily changed by making the reference a variable or programmed voltage. This feature also makes possible the use of limiters for modulation of pulses and square waves (see Chapter 11).

The precision rectifier circuit discussed in Sec. 7.2.3 is useful in a variety of applications. As an example, the absolute-value circuit of Fig. 7.15a performs the function of precision full-wave rectification. With the addition of a low-pass filter as shown in Fig. 7.15b, the circuit achieves precision ac to dc conversion. Another interesting use of the precision rectifier circuit is shown in Fig. 7.16. Here the circuit functions as

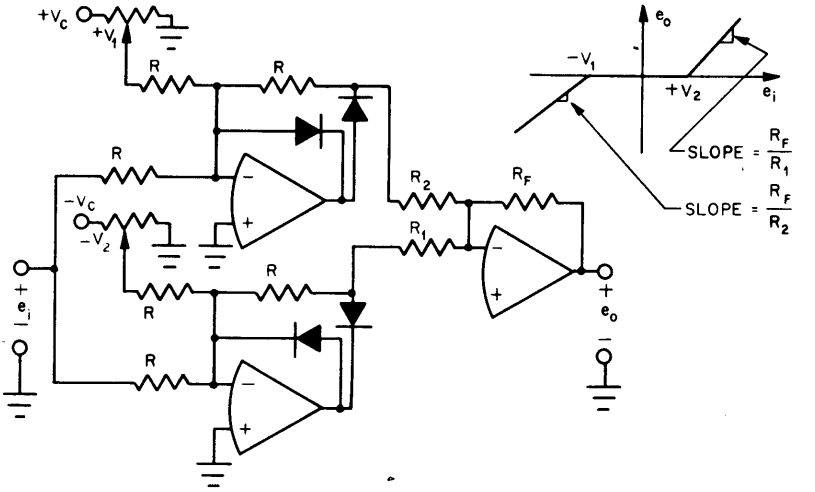


Fig. 7.17 Precision deadspace circuit.

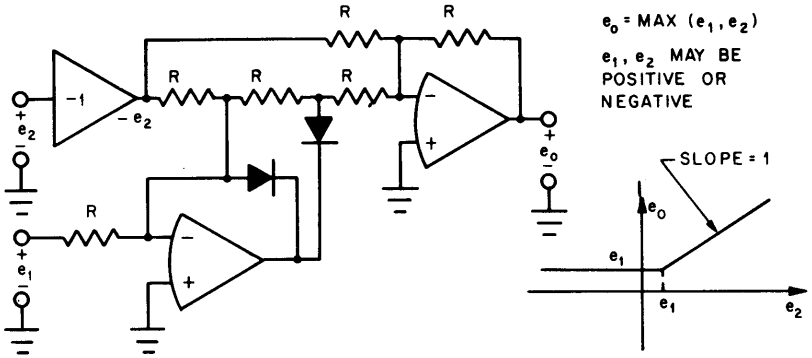


Fig. 7.18 Precision maximum selector.

a precision gate for positive signals. The negative gating signal V_G drives the limiter into its OFF region. If V_G is larger than the largest expected signal level, no signal can pass through the precision gate. Other uses of the precision rectifier principle are shown in Fig. 7.17 (precision deadspace circuit), and Fig. 7.18 (precision maximum selector).

7.3 Diode Function Generators[1,5,8–10]

The approximation of nonlinear functions is achieved with operational amplifiers by use of appropriate nonlinear feedback networks. The most general way of generating such functions is through the use of piecewise linear approximation, as shown in Fig. 7.19. The accuracy of such an approximation is determined by the number of line segments used. The complete piecewise curve is obtained by the summation of individual line segments whose "breakpoint" voltages and slopes are determined separately for each segment. Figure 7.20 illustrates how such segments may

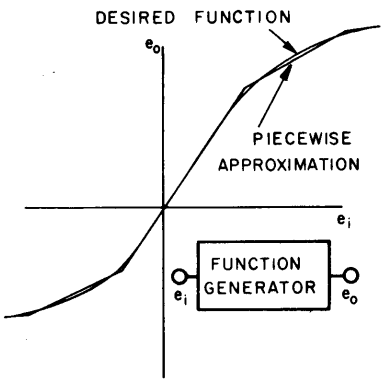


Fig. 7.19 Piecewise approximation of a nonlinear function.

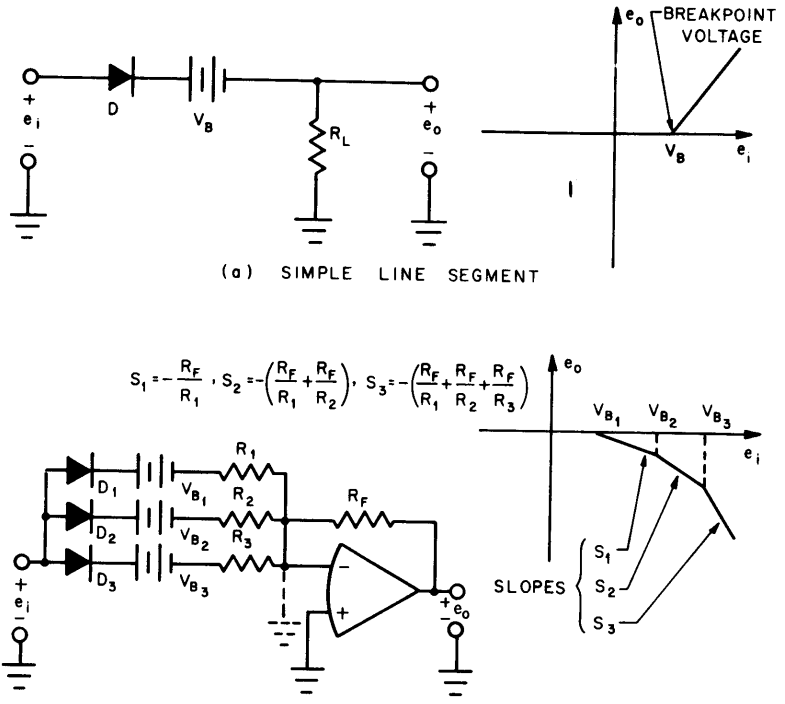


Fig. 7.20 Generation of piecewise approximation: (a) simple line segment; (b) summation of line segments.

be generated with simple limiter circuits and summed by the operational amplifier. The amplifier summing junction is a summation point for the currents from the breakpoint networks and the resistor R_F provides the scaling function. A more practical means of obtaining the desired line segments is through the use of series and shunt limiters as shown in Fig. 7.21. Note that each of the diode breakpoint circuits of Fig. 7.21 can be represented as a nonlinear transconductance. By using such networks as feedback elements, as shown in Fig. 7.22b, we obtain the inverse function.

As discussed earlier, the forward conduction characteristics of the silicon diode are somewhat temperature-sensitive and can cause changes in the breakpoints of the curve. This effect can be compensated partially by the methods shown in Fig. 7.23. In both cases the forward voltage drop of the breakpoint diode is compensated by a similar voltage drop in series with the biasing source. In the shunt limiter, the base-to-emitter voltage drop offsets much of the temperature sensitivity of the diode forward

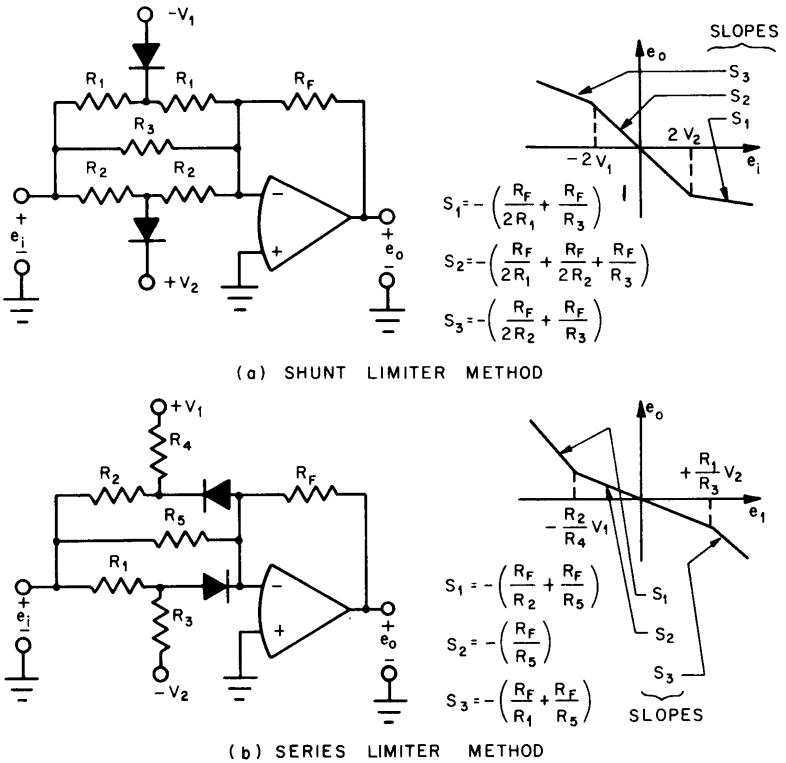
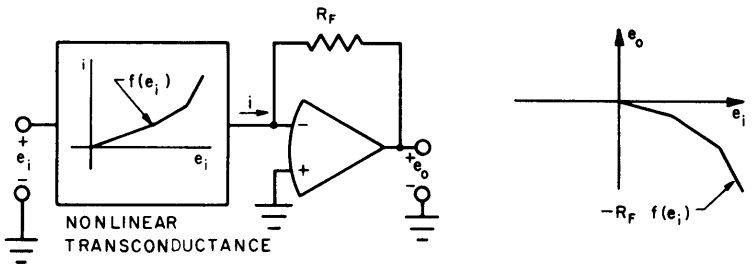


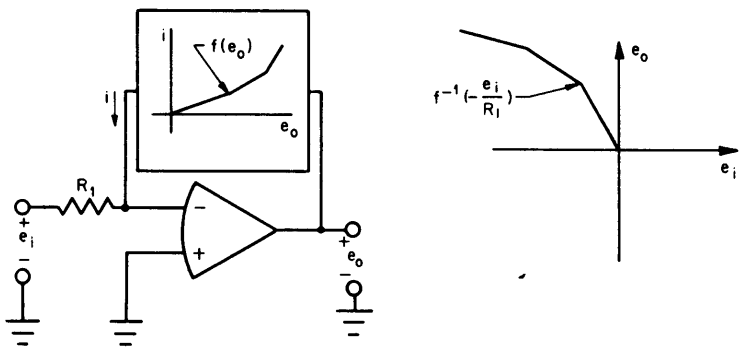
Fig. 7.21 Practical diode function generator circuits: (a) shunt limiter method; (b) series limiter method.

voltage. In the series limiter, a second diode acts as a temperature-compensating element for the breakpoint diode.

A more flexible approach to the approximation of nonlinear functions is illustrated in Fig. 7.24. The figure shows a variable diode function generator (VDFG) wherein both the locations of the breakpoints and the slopes of the line segments are individually adjustable. Note that the slopes can be positive, negative, or zero. The breakpoints can easily be made variable or can be temperature-compensated as in Fig. 7.23. This particular version of the VDFG is of the shunt type. A series-type VDFG is shown in Fig. 7.24b. As still another approach, the precision limiter, with its ability to simulate ideal diodes, can be used to generate line segments whose breakpoints are precisely known and which are temperature-insensitive. A simple version of such a function generator is shown in Fig. 7.25. Each breakpoint requires an operational amplifier, which made this approach prohibitive in cost before the advent of the



(a) USE OF NONLINEAR TRANSCONDUCTANCE

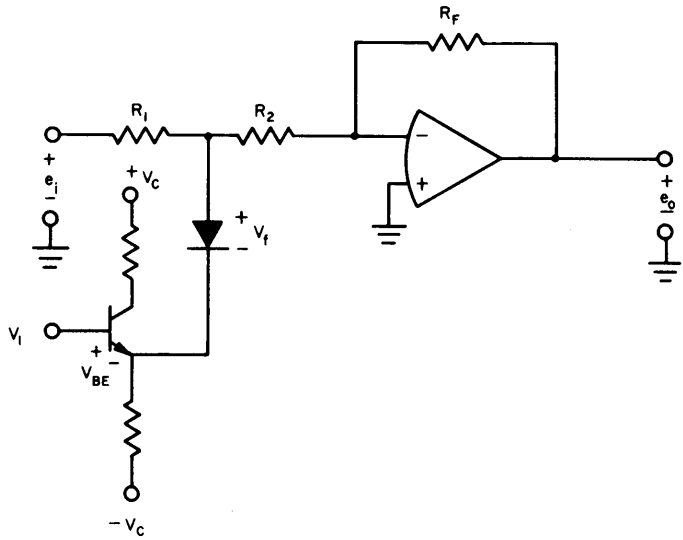


(b) INVERSE FUNCTION

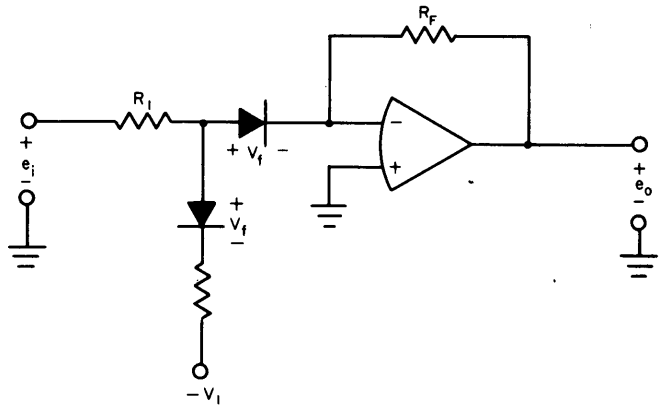
Fig. 7.22 Use of nonlinear transconductance to obtain an inverse function. (a) Use of nonlinear transconductance; (b) inverse function.

integrated-circuit operational amplifier. The principal drift factor in this circuit is not the diode junction but is actually the input voltage drift of the operational amplifiers, which are at least two orders of magnitude better than an uncompensated diode. The breakpoints are sharp, rather than rounded—a fact which may be a disadvantage of this technique. The technique is easily adapted to arbitrary function generation where both the breakpoints and the slopes are adjustable.

7.3.1 Applications of diode function generators One of the more obvious uses of the function generators which have been described above is in the linearization of response curves. Primary examples are the linearizing of thermocouples, thermistors, and pressure transducers. The nonlinearity of the transducer is balanced by a compensating nonlinearity of the function generator, thus achieving a composite function which is linear. The general procedure is illustrated in Fig. 7.26. As another approach the diode function generator can be used for waveform generation when its input voltage is a linear sweep such as a triangle wave.

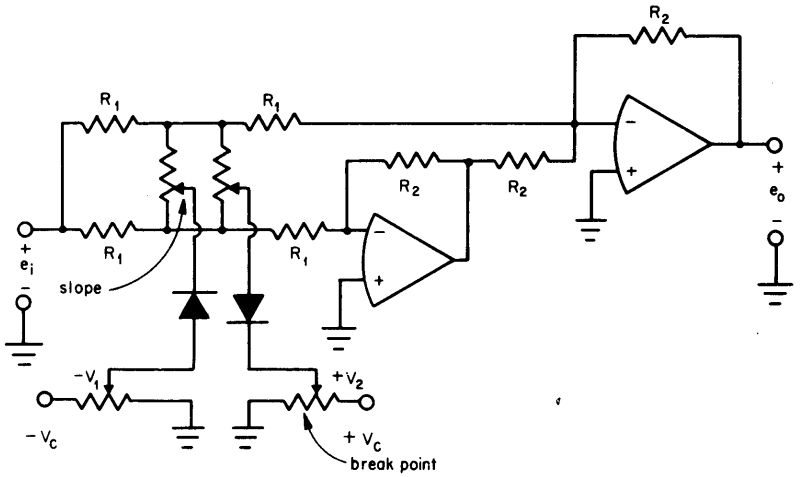


(a) TEMPERATURE COMPENSATED BREAKPOINT - SHUNT LIMITER

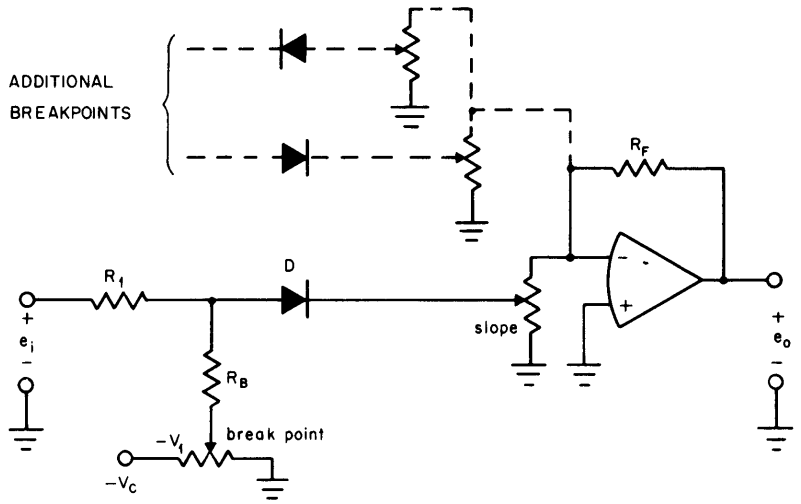


(b) TEMPERATURE COMPENSATED BREAKPOINT - SERIES LIMITER

Fig. 7.23 Compensation of breakpoint temperature drift. (a) Temperature-compensated breakpoint shunt limiter; (b) temperature-compensated breakpoint series limiter.



(a) SHUNT LIMITER DIODE FUNCTION GENERATOR



(b) SERIES LIMITER DIODE FUNCTION GENERATORS

Fig. 7.24 Variable diode function generators: (a) shunt limiter diode function generator; (b) series limiter diode function generator.

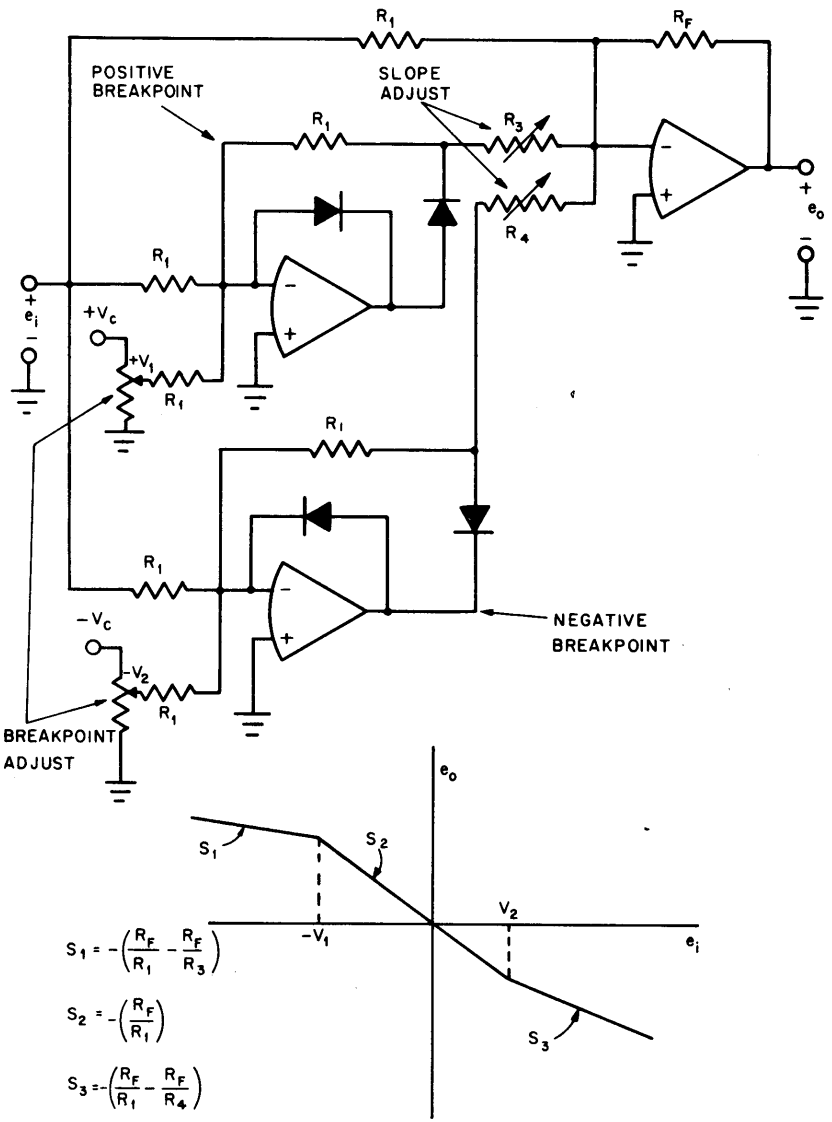


Fig. 7.25 Precision limiter diode function generator.

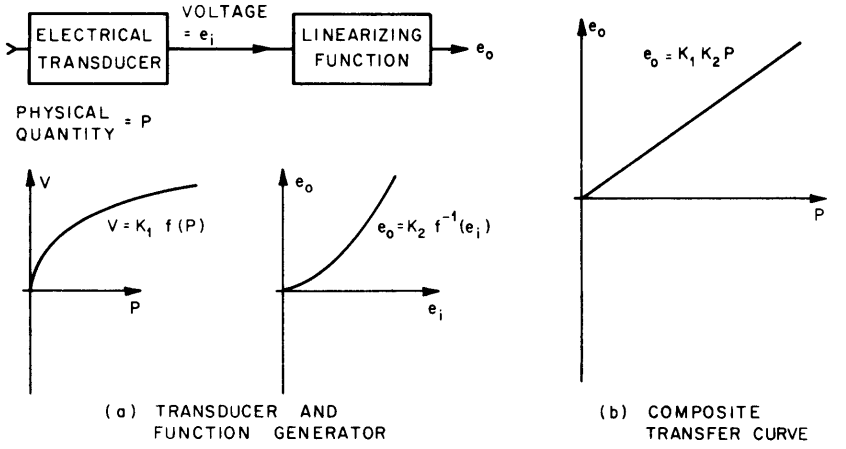


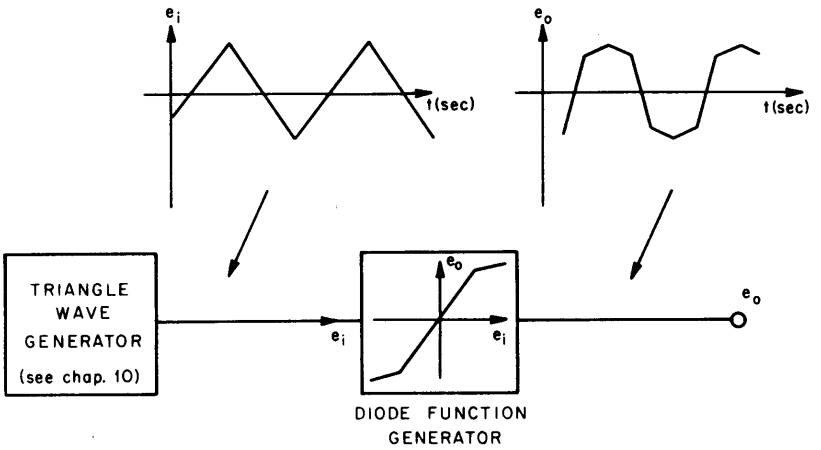
Fig. 7.26 Linearization of a transducer using a function generator. (a) Transducer and function generator; (b) composite transfer curve.

Either arbitrary functions, as shown in Fig. 7.27a, or common functions, such as the sine wave shown in Fig. 7.27b, can be generated. This method is especially attractive for the generation of very low-frequency waveforms. Other well-known functions such as the square and square root of an input voltage can be accurately approximated by the diode breakpoint method. Such function generators are extremely time-consuming to design for good accuracy, because of the large number of breakpoints and the interaction of all adjustments. However, these devices are available commercially and can be used for a variety of functions. Some examples are shown in Fig. 7.28. Other interesting areas for the application of function generator techniques are the simulation of physical effects in computation, the realization of nonlinear sensitivities for control systems, and the compression of signals having wide dynamic range. These applications are illustrated in Fig. 7.29.

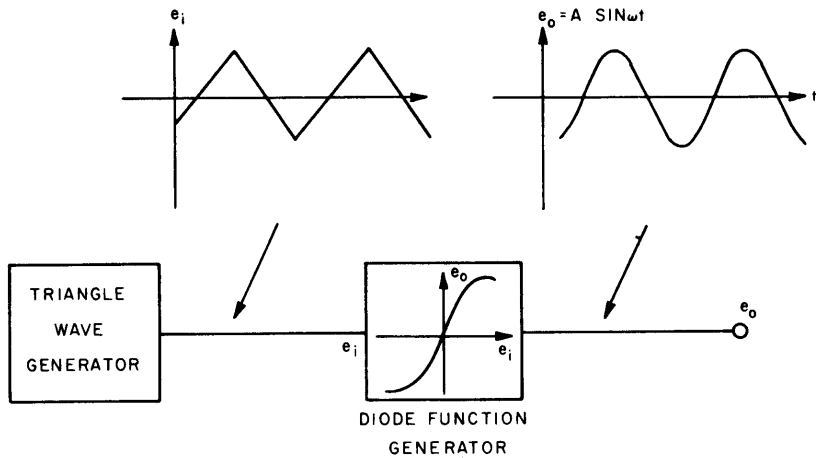
7.4 Logarithmic Amplifiers[2,15]

In the preceding sections of this chapter we have discussed the use of nonlinear feedback networks to provide limiting and function generation. The diode function generators (DFG) which were discussed used the large-signal switching properties of the diode. In this section we shall present a treatment of logarithmic amplifiers. Such amplifiers use the nonlinear volt-ampere relationship of the p-n junction itself. This relationship is given by

$$i_f = I_o(e^{v_f/\eta V_T} - 1)$$

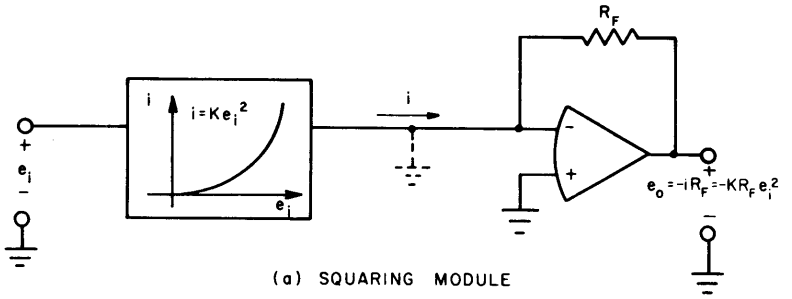


(a) GENERATION OF ARBITRARY WAVESHAPES

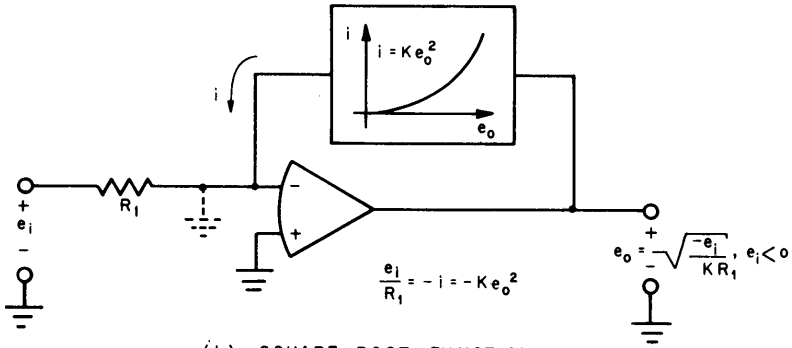


(b) SINE WAVE GENERATION

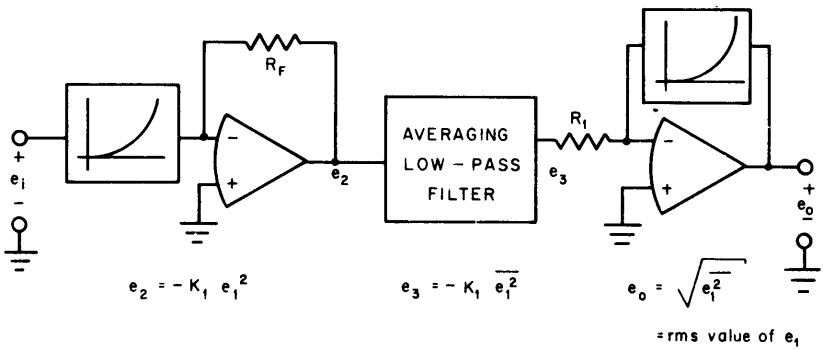
Fig. 7.27 Use of diode function generators for waveform generation. (a) Generation of arbitrary waveshapes; (b) sine-wave generation.



(a) SQUARING MODULE

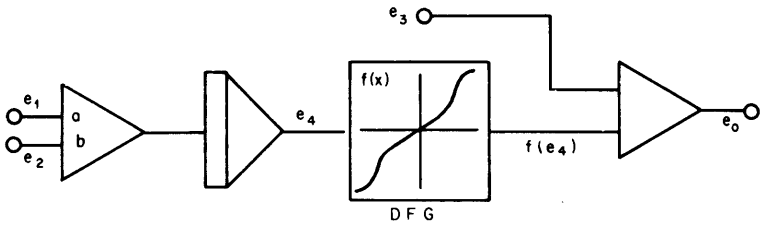


(b) SQUARE ROOT FUNCTION

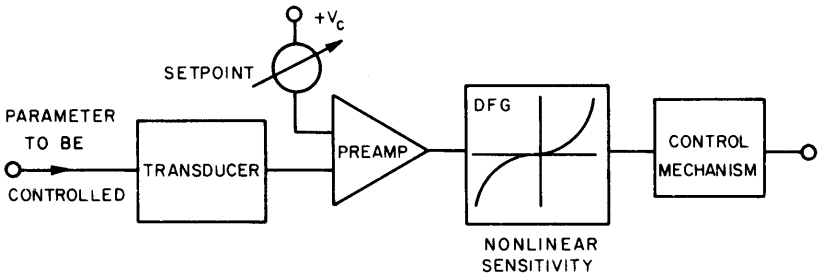


(c) RMS CIRCUIT

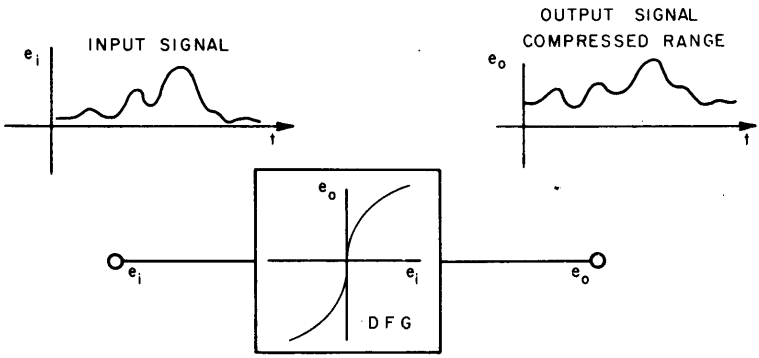
Fig. 7.28 Use of squaring function. (a) Squaring module; (b) square-root function; (c) rms circuit.



(a) USE OF DFG IN ANALOG SIMULATION



(b) USE OF DFG IN CONTROL SYSTEM



(c) USE OF DFG FOR SIGNAL COMPRESSION

Fig. 7.29 Applications of a diode function generator (DFG). (a) Use of a DFG in an analog simulation; (b) use of a DFG in a control system; (c) use of a DFG for signal compression.

where I_o = reverse saturation current

$I \approx 2$ for small currents in silicon devices

$$V_T = \frac{k}{q} T \approx \frac{T}{11{,}000} \text{ volts; T in °K}$$

If we restrict the operating region of v_f so that $e^{v_f/\eta V_T} \gg 1$, the logarithmic relationship may be expressed as

$$\ln i_f = \ln I_o + \frac{v_f}{\eta V_T}$$

or

$$v_f = \eta V_T (\ln i_f - \ln I_o)$$

Ignoring temperature effects for the moment, η, V_T, and I_o may be considered as constants. If the diode is connected in the feedback path of an operational amplifier, as shown in Fig. 7.30, the output voltage of the amplifier is a logarithmic function of the input voltage. The derivation of the logarithmic relation proceeds as follows:

$$i_1 = \frac{e_i}{R_1} \qquad i_f = i_1$$

$$v_f = \eta V_T \left(\ln \frac{e_i}{R_1} - \ln I_o \right)$$

$$e_o = -v_f = -\eta V_T \left(\ln \frac{e_i}{R_1} - \ln I_o \right)$$

In considering the temperature compensation of such an amplifier, it should be noted that there are actually two separate temperature effects to be compensated: a temperature-sensitive scale factor, ηV_T, and a temperature-sensitive offset term, $\eta V_T \ln I_o$. The saturation current term can be removed or reduced by the use of a current source and a second, matched diode, D_2, as shown in Fig. 7.31. The current source forces a constant current I_R through D_2, which in turn generates the voltage V_f'. If the two diodes are perfectly matched, the V_T and I_o terms for the two diodes will be equal and the $\ln I_o$ term will be absent from e_3.

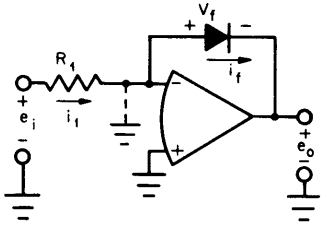


Fig. 7.30 Simple logarithmic amplifier.

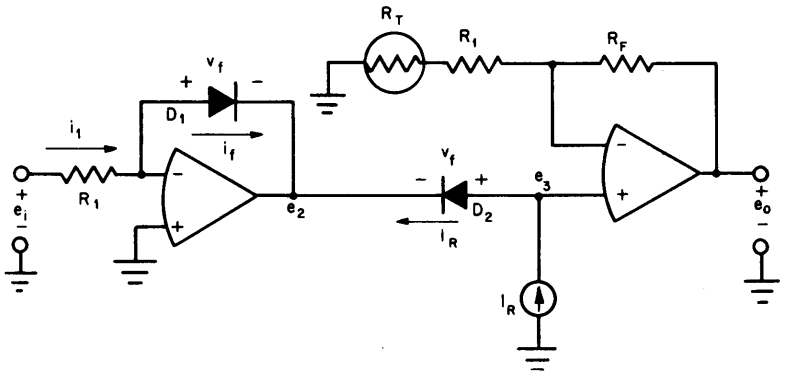


Fig. 7.31 Temperature-compensated logarithmic amplifier.

Thus we may write

$$e_3 = e_2 + V_f = -\eta V_T \left(\ln \frac{e_i}{R_1} - \ln I_o - \ln I_R + \ln I_o \right)$$

$$e_3 = -\eta V_T \ln \frac{e_i}{R_1 I_R}$$

The only remaining temperature sensitivity in e_3 is that of the scale factor term. This can be compensated in the output amplifier by making its gain temperature-sensitive and compensating for the V_T factor. This is most easily done by using a temperature-sensitive resistor R_T in the feedback network as shown in Fig. 7.31. The output voltage is then given by

$$e_o = -\frac{R_F + R_1 + R_T}{R_1 + R_T} \eta V_T \ln \frac{e_i}{R_1 I_R} = K_1 \ln (K_2 e_i)$$

The gain of the output amplifier determines the constant K_1, and the values of I_R and R_1 determine the constant K_2. Together, they determine the range of input voltage which will drive the output amplifier through its rated range.

The dynamic range of a logarithmic amplifier of the type described in this section is limited by several independent factors. The diode itself follows the logarithmic relationship between v_f and i_f rather closely over as much as 6 decades of i_f. However, i_f contains not only the input signal current i_1 but also the input bias current and the noise current of the operational amplifier, plus currents generated by the input offset voltage and input noise voltage applied across R_1. If the maximum current allowed to flow through the diode (for accurate logging) is 1 mA, then R_1 must be 10 kΩ, if the maximum input voltage is to be 10 V. If we assume an amplifier which has an input bias current of 10 nA and

an input offset voltage of 1.0 mV, the dynamic range of input signal for percent accuracy is 100 mV to 10 V—a range of 40 dB. The limitation is provided by the offset voltage. In order to achieve a dynamic range of 80 dB at 1 percent accuracy we must have a total error current of less than 1 nA. An amplifier with FET input will have a bias current of the order of a few picoamperes. However the input offset voltage must then be less than 10^{-9} A $\times$ 10^4 Ω = 10 μV. This is a very difficult figure to maintain, particularly over a long period of time and over a range of temperatures. The noise voltage of the amplifier e_n, also generates an error current, $i_n = e_n/R_1$, which must be considered as a part of the total error if transient signals with a broad frequency spectrum are being measured. These problems are not as formidable if the signal source is a high impedance source of current, as shown in Fig. 7.32. In such a case the input signal current flows through the feedback diode, generating a voltage proportional to the logarithm of the input current. Since the source resistance is extremely large, the effective voltage gain of the circuit is small, and the voltage offset and noise of the amplifier are not so critical as error sources. The principal sources of error are bias current and noise current, which can be made very small if an FET operational amplifier is used. Note that in the log amplifiers discussed the input signal must be unipolar. It may, however, be negative or positive, depending on the orientation of the diodes.

Another variation of the logarithmic amplifier is the log-ratio circuit shown in Fig. 7.33. Here there are two input signals (e_1,e_2) which are converted to temperature-sensitive logarithmic voltages (e_3,e_4) by the diodes D_1 and D_2 and amplifiers A_1 and A_2. The relations are

$$e_3 = -\eta V_T \left(\ln \frac{e_1}{R_1} - \ln I_o \right)$$

$$e_4 = -\eta V_T \left(\ln \frac{e_2}{R_1} - \ln I_o \right)$$

Amplifier A_3 acts as a difference amplifier with gain. By subtracting e_3 from e_4, the temperature-sensitive offset terms $\eta V_T \ln I_o$ tend to cancel

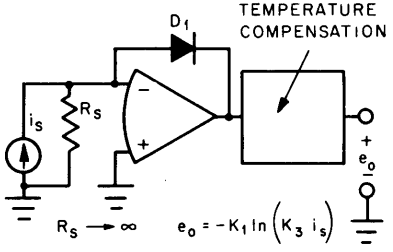


Fig. 7.32 Logarithmic current-to-voltage converter.

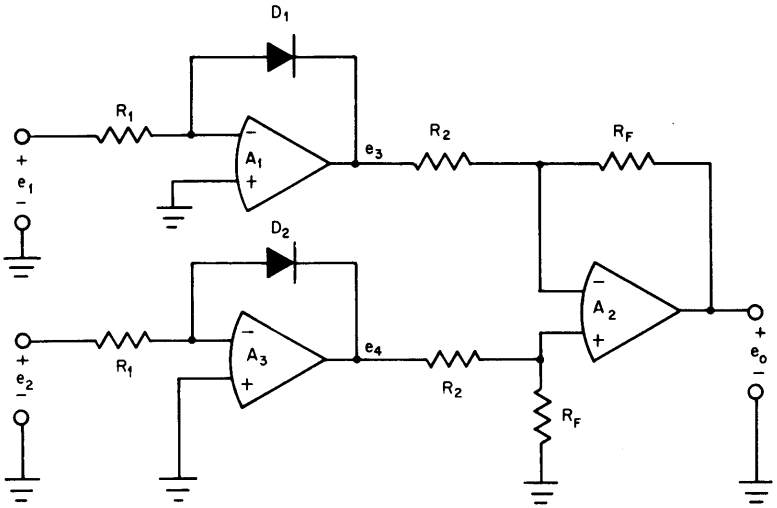


Fig. 7.33 Log-ratio amplifier.

each other. The output voltage is

$$e_o = \frac{R_F}{R_2}(e_4 - e_3) = \frac{R_F}{R_2}\eta V_T \ln \frac{e_1}{e_2}$$

The temperature-sensitive gain term ηV_T can be canceled from the expression for e_o if R_F/R_2 is made to have a compensating temperature sensitivity.

The antilog function also can be obtained by using a diode with an operational amplifier as shown in Fig. 7.34. The following relationships apply,

$$e_2 = e_i \frac{R_1}{R_1 + R_2}$$

$$e_3 = e_i \frac{R_1}{R_1 + R_2} - \eta V_T(\ln I_f - \ln I_o)$$

but, also,

$$e_3 = -\eta V_T(\ln i_2 - \ln I_o)$$

Therefore

$$e_i \frac{R_1}{R_1 + R_2} = \eta V_T \ln \frac{I_f}{i_2}$$

$$e_o = +i_2 R_F$$

$$-e_i \frac{R_1}{R_1 + R_2} = \eta V_T \ln \frac{e_o}{R_F I_f}$$

$$e_o = R_F I_f \ln^{-1}\left[-e_i \frac{R_1}{(R_1 + R_2)\eta V_T}\right]$$

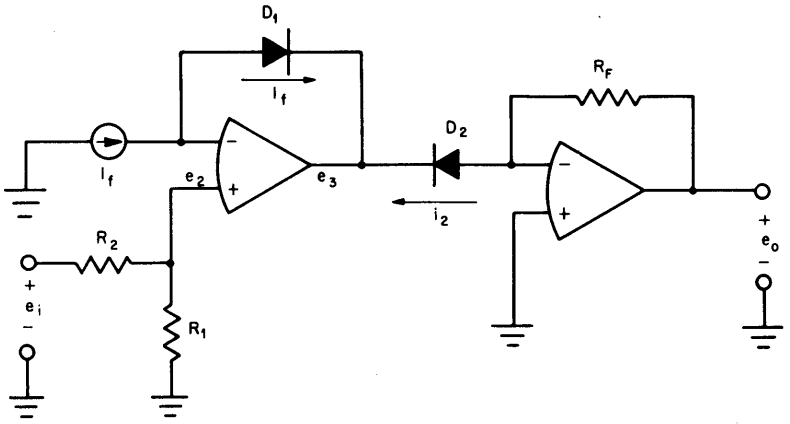


Fig. 7.34 Antilog amplifier.

Once again the temperature-sensitive offset terms, $\eta V_T \ln I_o$, cancel if the diodes are well matched. The temperature sensitivity of the proportionality factor $R_1/(R_1 + R_2)\eta V_T$ can be eliminated if the resistive divider (R_1,R_2) can be made to have a compensating sensitivity. The current generator I_f and feedback resistor R_o are adjusted for proper scaling. The dynamic range of the antilog amplifier is determined by the noise, voltage offset, and bias current of both amplifiers. This means that for wide dynamic range, such as 80 dB, both amplifiers must have voltage offset and noise less than about 10 μV. This is extremely difficult to achieve with normal operational amplifier designs.

7.4.1 Applications of log amplifiers The log and antilog amplifiers described above can be used in combination for the generation of arbitrary functions by raising the input to a power, as shown in Fig. 7.35. The exponent α is obtained by simply multiplying $\ln e_1$ by a constant through a coefficient network. The voltage e_2 is proportional to $\ln e_i$; thus

$$e_2 = \alpha K_1 \ln K_2 e_i$$

The output voltage is proportional to the antilog of e_2:

$$e_o = K_3 \ln^{-1} K_4 e_2 = K_3 e^{K_4 e_2}$$
$$e_o = K_3 (K_2 e_i)^{\alpha K_1 K_4}$$

The value of the coefficient can be greater or less than 1.0, if a scaling amplifier is used, thus allowing a variety of functions. For special situations where the function is to remain fixed, the scaling of the log and antilog amplifiers can include the coefficient α.

Another of the primary uses of the logarithmic amplifier is the com-

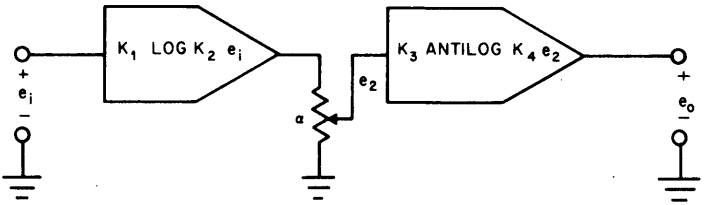


Fig. 7.35 Raising variables to a power with log techniques.

pression/expansion of signals having wide dynamic range. Consider as an example the logarithmic amplifier with characteristic

$$e_o = -10 \log e_i$$

where $-10\ V \leq e_o \leq +10\ V$. A plot of this characteristic is shown in Fig. 7.36. The input signal range is from +100 mV to +10 V, which corresponds to an output range of $-10 \leq e_o \leq +10$ V. Input signals in the range $+0.1\ V \leq e_i \leq +10$. are expanded to an output range of $0\ V \leq e_o \leq +10$ V. Input signals in the range $+1.0\ V \leq e_i \leq +10$ V correspond to an output range of $-10\ V \leq e_o \leq 0$ V. Thus each decade of input range is represented by equal increments of output voltage. This makes somewhat easier the reading and recording of input data having a wide dynamic range. An ac compression amplifier with a psuedo-logarithmic response can be achieved with the circuit of Fig. 7.37a. The diodes D_1 and D_2 generate the logarithmic response for positive and negative output voltages, respectively. The resistor R_F is required because of the discontinuity in the log curve at zero. This feedback resistor modifies the curve near zero as shown in Fig. 7.37b. The transfer curve of this compression amplifier will vary with temperature and cannot be effectively temperature-compensated in the output scaling amplifier. Thus it is useful only under temperature-controlled conditions or for very "rough" signal compression.

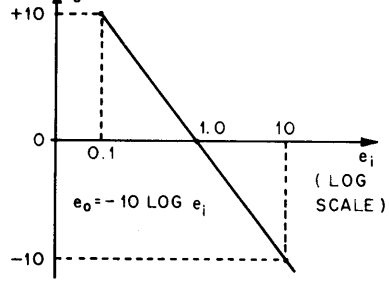


Fig. 7.36 Two-decade log amplifier gain curve.

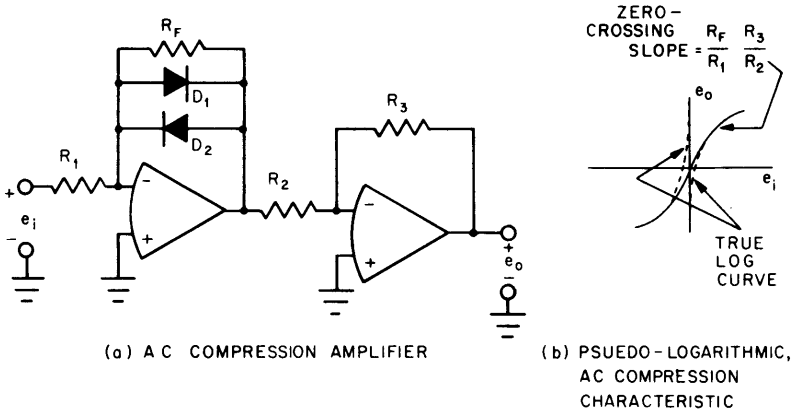


Fig. 7.37 Ac log compression technique. (a) Ac compression amplifier; (b) psuedo-logarithmic, ac compression characteristics.

7.5 Analag Multiplication and Division[1,11–14,17]

In the preceding sections of this chapter we have discussed operational amplifier nonlinear circuits which provide limiting, function generation, and logarithmic amplification. Another frequently encountered nonlinear application of operational amplifiers is for accurate multiplication and division of analog signals. The six most common solid-state methods are logarithmic, quarter-square, triangle averaging, time division, variable transconductance, and current ratioing. There are other techniques for multiplying, but these six are the most suitable for all-solid-state instrumentation. Together, they span a wide spectrum of accuracy, speed, and cost.

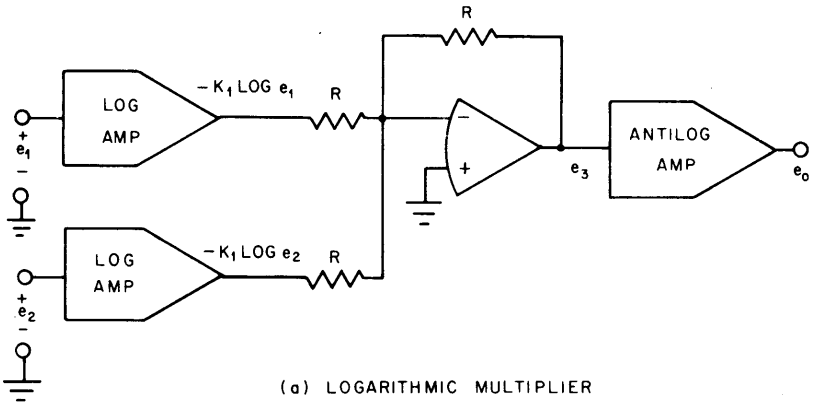
7.5.1 Logarithmic multiplier The first multiplier to be discussed is the logarithmic type shown in Fig. 7.38a. The log and antilog amplifier techniques discussed in the preceding section are used in this circuit. It is only necessary to take the log of each input, sum these inputs, and then take the antilog of the sum. The result is the product of the two inputs. In terms of the variables shown in Fig. 7.38a,

$$e_3 = K_1 (\ln e_1 + \ln e_2) = K_1 \ln e_1 e_2$$

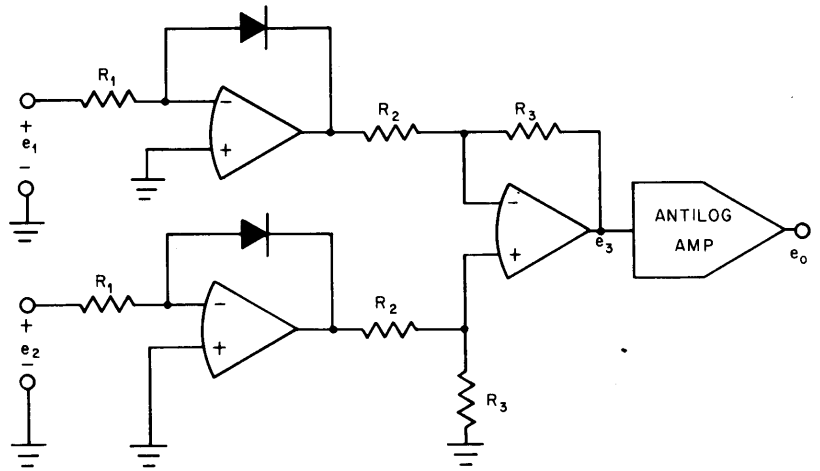
and

$$e_o = K_2 \ln^{-1} \frac{e_3}{K_1} = K_2 e_1 e_2$$

Division can be accomplished by subtracting the logarithms of the two inputs and then taking the antilog. This can most easily be accom-



(a) LOGARITHMIC MULTIPLIER



(b) LOGARITHMIC DIVIDER

Fig. 7.38 Multiplication and division by log techniques. (a) Logarithmic multiplier; (b) logarithmic divider.

plished with the log-ratio circuit of Fig. 7.38b. Here,

$$e_3 = K_1 \ln \frac{e_1}{e_2}$$

$$e_o = K_2 \ln^{-1} \frac{e_3}{K_1}$$

$$e_o = K_2 \frac{e_1}{e_2}$$

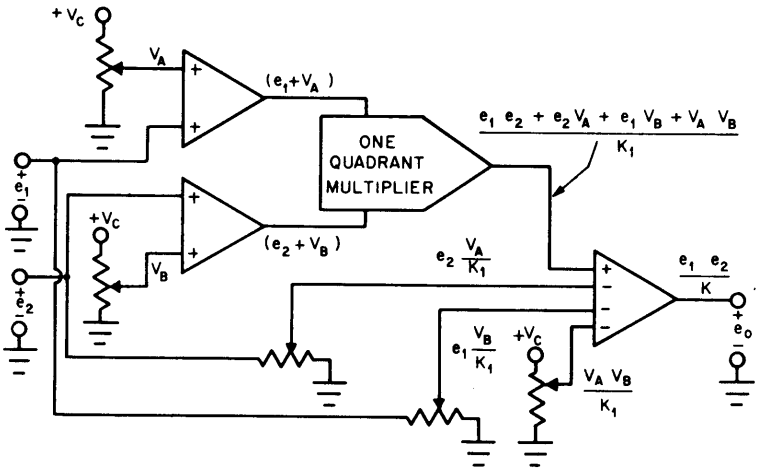


Fig. 7.39 Two- and four-quadrant multiplication obtained from a single-quadrant multiplier.

The logarithmic technique of multiplication and division is, of course, useful only for unipolar inputs, or one-quadrant operation, as it is sometimes described. Actually, however, any single-quadrant multiplier can be converted to two- or four-quadrant operation by the technique shown in Fig. 7.39. It is only necessary to subtract from the output all unwanted terms in e_1 and e_2, and the constant term. The addition of V_A and V_B to the input variables ensures that the inputs to the multiplier remain unipolar.

The logarithmic approach, unfortunately, suffers from rather strong temperature sensitivity. This can be compensated to a certain extent by methods previously discussed. However it is difficult to achieve better than 1 percent overall accuracy even for a moderate temperature range. Because of its basic simplicity, however, the logarithmic method may be attractive where accuracies of 1 to 5 percent are satisfactory and where careful temperature compensation is not required.

7.5.2 Quarter-square multiplier The quarter-square multiplier makes use of the equation

$$\frac{(X+Y)^2-(X-Y)^2}{4}=\frac{(X^2-X^2)+(Y^2-Y^2)+2XY+2XY}{4}$$

$$=XY$$

to obtain the product. The squared terms are usually obtained through the use of special diode function generators, using the piecewise linear

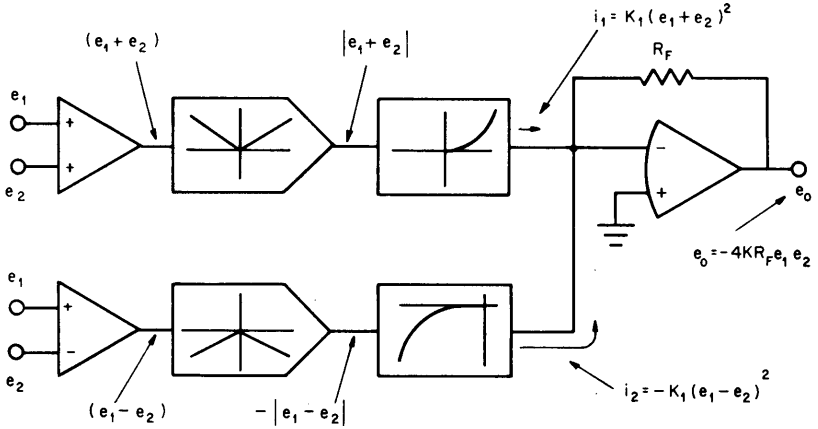


Fig. 7.40 Quarter-square multiplier.

techniques outlined earlier in this chapter. Squaring modules with 10 breakpoints can approximate the function

$$i_{sc} = Ke_1^2$$

to within ± 0.1 percent of full scale. The term i_{sc} is the output short-circuit current to ground, or virtual ground. The circuit of Fig. 7.40 illustrates one means of obtaining multiplication through the quarter-square relationship. This method of multiplication is useful over a wide frequency range, which is its most attractive feature. Its principal disadvantages are the complexity and cost and the fact that the maximum error voltage, although small as a percentage of full scale, may exist at low input levels. This statement is illustrated by the typical error curve of Fig. 7.41. The "ripple" in the error curve arises from the piecewise linear approximation used in the squaring modules. Additional errors are introduced by dc offset shift as a function of temperature.

7.5.3 Triangle-averaging multiplier The method of multiplication known as triangle averaging is illustrated in Fig. 7.42. The voltage e_3 is

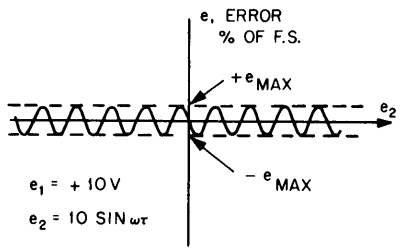
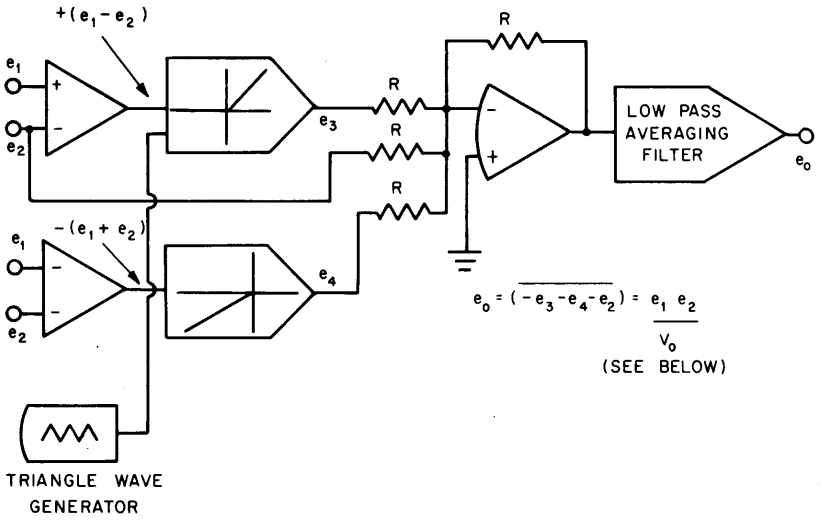
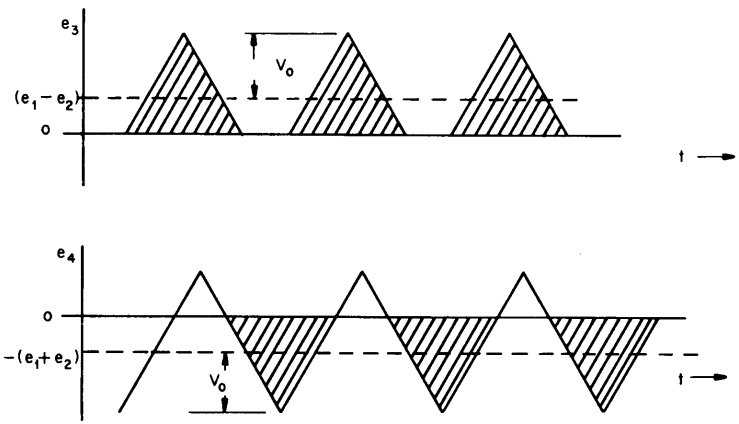


Fig. 7.41 Typical error curve of a quarter-square multiplier.



(a) TRIANGLE AVERAGING MULTIPLIER



(b) MULTIPLIER WAVE FORMS

Fig. 7.42 Illustration of the triangle-averaging multiplier: (a) triangle-averaging multiplier; (b) multiplier waveforms.

the half-wave rectified sum of the triangle wave and $e_1 - e_2$. Only the positive part of the waveform is retained, and this is time-averaged by a low-pass filter. The resulting average value is

$$\bar{e}_3 = \frac{1}{2}\left(\frac{1}{2} + \frac{e_1 - e_2}{2V_o}\right)(V_o + e_1 - e_2)$$

Similarly

$$\bar{e}_4 = -\frac{1}{2}\left(\frac{1}{2} + \frac{e_1 + e_2}{2V_o}\right)(V_o + e_1 + e_2)$$

The sum of the two voltages is

$$\bar{e}_3 + \bar{e}_4 = -e_2 - \frac{e_1 e_2}{V_o}$$

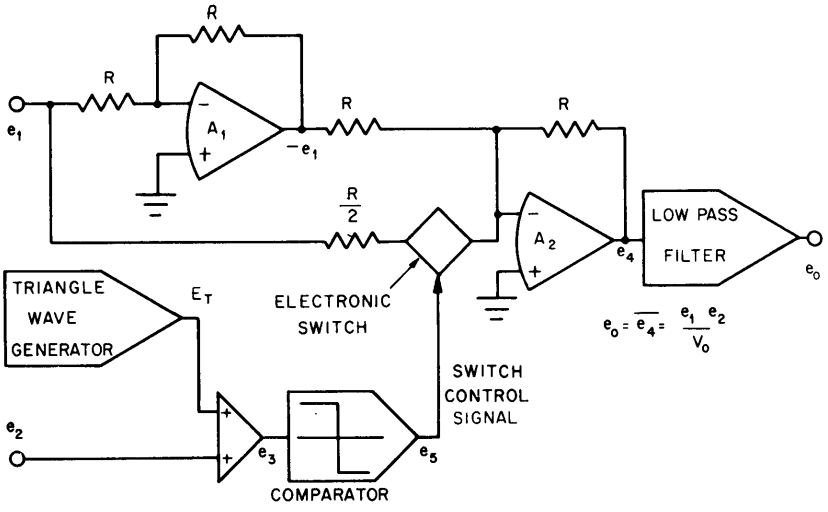
If the e_2 term is removed in a summing amplifier, the resulting voltage is the desired product. The frequency response of such multipliers is necessarily quite restricted because of the low-pass averaging filter at the output. This filter must effectively eliminate the carrier frequency and must therefore have a cutoff frequency well below the fundamental of the triangle wave. Increasing the frequency of the triangle wave to improve the overall frequency response leads to problems of capacitive coupling of carrier frequencies to the output as well as linearity problems in the triangle waveform. The linearity of the triangle wave and the sharpness of the peaks of the waveform are the principal limitations on the accuracy of this method of multiplication. (See Chapter 10 for triangle-wave generators.)

7.5.4 Time-division multiplier Another carrier technique of multiplication is the so-called time-division multiplier illustrated in Fig. 7.43. It is necessary to generate a square wave whose average value depends upon both of the input signals. In this method of multiplication a triangle wave is once again used. However, instead of clipping and averaging as in the triangle-averaging multiplier, the triangle wave is used to control an electronic switch. The triangle wave is summed with one of the input signals, e_2, and the sum is applied to a zero-biased comparator. The resulting asymmetric square wave has a duty cycle determined by the magnitude and polarity of e_2. That is,

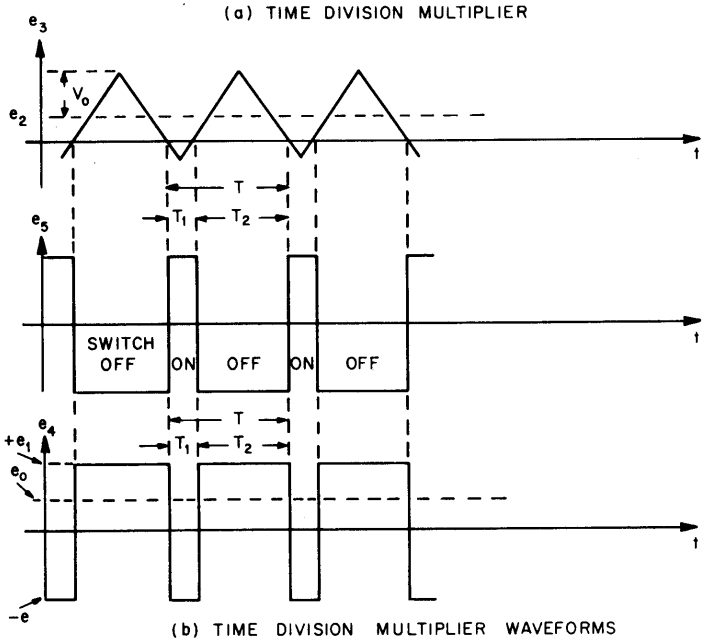
$$T_2 = \frac{e_2 + V_o}{2V_o} T$$

$$T_1 = \frac{V_o - e_2}{2V_o} T$$

This square wave in turn controls the electronic switch. Amplifier A_2 transmits $+e_1$ when the switch is at ON, and $-e_1$ when the switch is at OFF. Since the duty cycle of e_4 is proportional to e_2 and the magnitude is $\pm e_1$, the resulting average value is proportional to the product. When



(a) TIME DIVISION MULTIPLIER



(b) TIME DIVISION MULTIPLIER WAVEFORMS

Fig. 7.43 Illustration of the time-division multiplier. (a) Time-division multiplier; (b) time-division multiplier waveforms.

this waveform is averaged by a low-pass filter, the result is equal to the product, which a scaling factor.

$$e_o = \bar{e}_4 = e_1 \frac{e_2 + V_o}{2V_o} - e_1 \frac{V_o - e_2}{2V_o}$$

$$e_o = \frac{e_1 e_2}{V_o}$$

The time-division multiplier suffers from much the same problems as the triangle-averaging type. Accuracy depends strongly upon the linearity, symmetry, and "sharpness" of the triangle wave. The resistors used in the feedback networks of A_1 and A_2 must be precisely matched, taking into account the series resistance of the switch. Offset voltage of the comparator will appear as an error term added to e_2. The switching time for e_4 to change from $+e_1$ to $-e_1$ is a critical error factor and must be small compared with the period T. This places a stringent limit on the upper frequency of the carrier and thus on the frequency response of

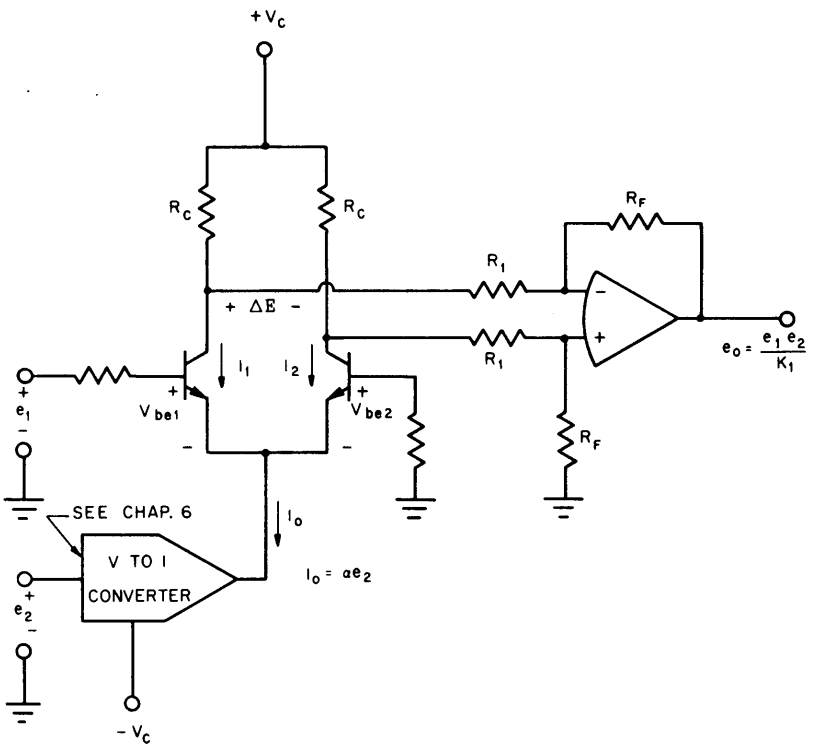


Fig. 7.44 Variable transconductance multiplier.

the multiplier. There are numerous variations of the triangle-averaging and time-division multiplier circuits. However, the examples given illustrate the techniques and some of the design limitations.

7.5.5 Variable transconductance multiplier Perhaps the simplest multiplication technique is the variable transconductance method illustrated in Fig. 7.44. This method depends upon the current through the matched pair of transistors being proportional to one of the input signals, e_2. Assuming that the transistors are a perfectly matched pair, the differential collector current (and consequently the differential collector voltage) is proportional to the product of e_1 and e_2. The result is derived as follows:

$$I_1 = I_{SE} e^{\frac{qV_{be1}}{kT}}$$

$$\frac{\Delta I_1}{\Delta V_{be1}} = \frac{q}{kT} I_1$$

$$I_o = I_1 + I_2 = 2I_{SE} e^{\frac{qV_{be1}}{kT}}$$

$$\Delta I_1 = \frac{q}{2kT} I_o \Delta V_{be1}$$

$$\Delta I_2 = \frac{q}{2kT} I_o \Delta V_{be2}$$

$$\Delta I_1 - \Delta I_2 = \frac{q}{2kT} I_o \overbrace{(\Delta V_{be1} - \Delta V_{be2})}^{e_1}$$

$$\Delta E = R(\Delta I_1 - \Delta I_2) = R_c \frac{q}{2kT} \alpha e_2 e_1$$

$$e_o = \frac{R_o}{R_1} R_c \frac{q}{2kT} \alpha e_1 e_2 = \frac{e_1 e_2}{K_1}$$

The differential input operational amplifier provides proper scaling and conversion to a single-ended output. Because of the extreme temperature sensitivity of this method of multiplication, it is of limited usefulness. Both the scale factor and the dc level will tend to drift, the latter because of unavoidable mismatch between the multiplying transistors. The linearity is also rather poor and ac feedthrough is appreciable. The ac feedthrough is measured by grounding one of the inputs and applying a sine wave to the other input. The output should be zero but actually contains a component of the input sine wave. This is particularly true when e_2 is grounded and the ac signal is applied at e_1. The variable transconductance method is important chiefly because of its relation to

the current-rationing method to be described next. This method, the basic principles of which were first described by Gilbert,[17] is a vast improvement over the variable transconductance method although it uses the same basic relationships of the semiconductor junction.

7.5.6 Current ratioing multiplier One realization of the *current ratioing multiplier* is shown in Fig. 7.45a. The heart of this multiplier is the gain cell shown in Fig. 7.45b. This device ensures that the currents i_3, i_4 in the collectors of transistors Q_3, Q_4 remain in a constant ratio equal to the ratio of the external currents I_7 and I_8. The currents I_1, I_7, and I_8 are generated by constant current sources. The currents and voltages of the gain cell are related by the equations

$$\begin{aligned} I_7 &= K_1 e^{\alpha_1 V_{d1}} \\ I_8 &= K_2 e^{\alpha_2 V_{d2}} \\ I_3 &= K_3 e^{\alpha_3 V_{be3}} \\ I_4 &= K_4 e^{\alpha_4 V_{be4}} \end{aligned}$$

where

$$\alpha = \frac{q}{kT}$$

If the transistors and diodes are matched to make α's equal and K's equal, then

$$\frac{I_7}{I_8} = e^{\alpha(V_{d1} - V_{d2})}$$

and

$$\frac{I_4}{I_3} = e^{\alpha(V_{be4} - V_{be3})}$$

The loop equation can be written

$$V_{d1} + V_{be3} = V_{be4} + V_{d2}$$

or

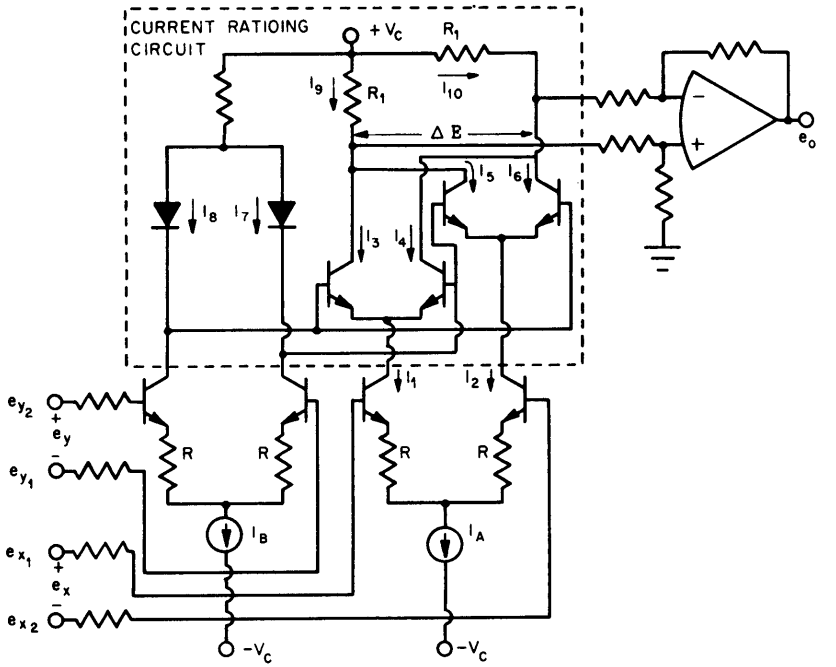
$$V_{d1} - V_{d2} = V_{be4} - V_{be3}$$

and, if this is substituted into the expression for I_4/I_3, the result is

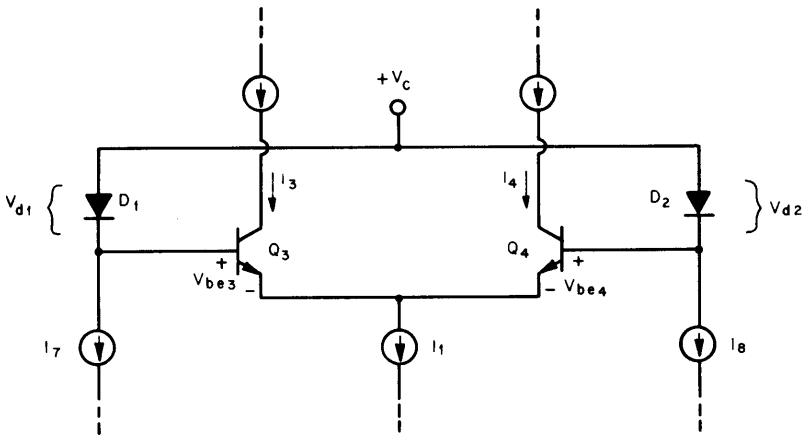
$$\frac{I_7}{I_8} = \frac{I_3}{I_4}$$

In the multiplier circuit of Fig. 7.45a, the gain cell concept is used to enforce the conditions

$$\frac{I_4}{I_3} = \frac{I_8}{I_7} \quad \text{and} \quad \frac{I_6}{I_5} = \frac{I_7}{I_8}$$



(a) MULTIPLIER CIRCUIT



(b) GAIN CELL

Fig. 7.45 Current ratioing multiplier. (a) Multiplier circuit; (b) gain cell.

Other necessary relations are

$$I_1 = I_3 + I_4 \qquad I_9 = I_3 + I_5$$
$$I_2 = I_5 + I_6 \qquad I_{10} = I_6 + I_4$$
$$I_1 + I_2 = I_A \qquad I_7 + I_8 = I_B$$
$$e_X = R(I_1 - I_2) \qquad e_Y = R(I_8 - I_7)$$

Combining the above equations and using a considerable amount of simple algebra, the relationship for ΔE is obtained:

$$\Delta E = R_1(I_9 - I_{10}) = \frac{(-e_Y/R)(+e_X/R)}{I_B} R_1$$

With constant I_B and proper scaling the output voltage is

$$E_o = \frac{(e_{X_1} - e_{X_2})(e_{Y_1} - e_{Y_2})}{10}$$

Accurate multiplication requires that the transistors used be dynamically matched, a requirement that makes monolithic construction attractive for this type of multiplier. However, it has been found possible to achieve 1 percent accuracy of multiplication through the use of carefully matched discrete transistors.

The current ratioing multiplier has several desirable features which give it the potential for widespread use. These are:

1. Good linearity
2. Wide bandwidth
3. Differential input
4. Stability with temperature
5. Low ac feedthrough
6. Low cost

7.5.7 Analog dividers Any of the multipliers discussed in the preceding pages can be used as analog dividers by using the feedback circuits of Fig.

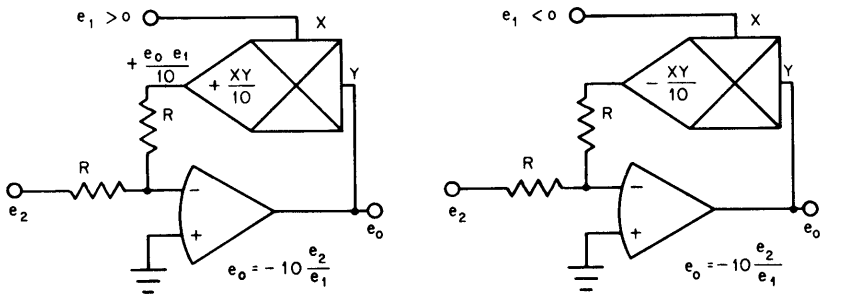


Fig. 7.46 Analog division techniques. (a) Positive denominator voltage; (b) negative denominator voltage.

7.46a and b. Note that only two-quadrant operation is possible because the voltage e_4 must be of opposite polarity to e_1. For $e_1 < 0$, the multiplier must provide polarity reversal whereas for $e_1 > 0$ the multiplier must generate $+ e_1 e_o/10 = -e_2$ to ensure stable operation (negative feedback). The principal limitation of such feedback dividers is the large error term as $e_2 \to 0$. This error term severely limits the dynamic range of the divider, especially where the error of the multiplier may have its largest value when the input signals are small (such as in the quarter-square multiplier). The best multipliers for use in feedback division are those whose error curve passes smoothly through the origin (such as the triangle-averaging and current-ratioing types).

7.5.8 Squarers and square rooters One of the most obvious applications of an analog multiplier is for computing the square of a signal voltage. Such calculations are quite common in power measurement, rms level measurement, and in computations of vector magnitude. Figure 7.47 illustrates such an application. The square-root function is obtained by using the multiplier as the feedback element, such as in the case of the divider circuit. The operational amplifier enforces the conditions

$$\frac{e_1^2}{10}\frac{1}{2R} + \frac{e_2^2}{10}\frac{1}{2R} = \frac{e_o^2}{10}\frac{1}{R}$$

$$e_o^2 = \frac{e_1^2}{2} + \frac{e_2^2}{2}$$

$$e_o = \sqrt{e_1^2 + e_2^2}$$

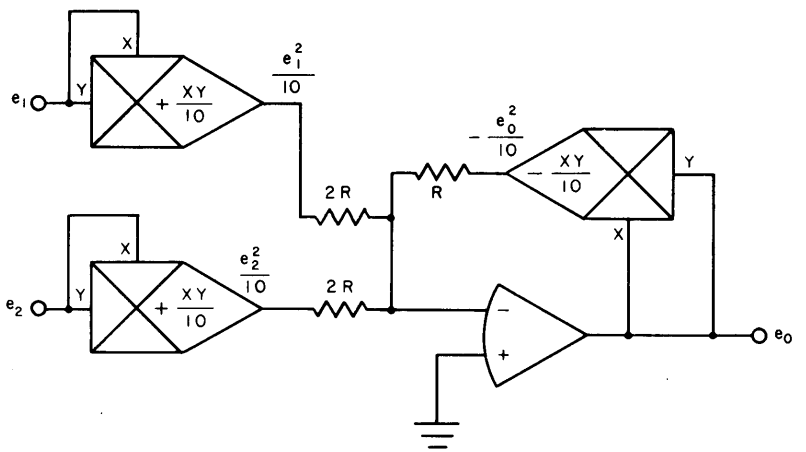


Fig. 7.47 Multipliers used in vector magnitude computation.

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8

ACTIVE FILTERS

The operational amplifier, especially the integrated-circuit operational amplifier, proves to be an extremely useful active device in the realization of active RC networks. Operational amplifiers have high input impedance, low output impedance, large open-loop gain, and low cost. These qualities are used to advantage in the circuits to be discussed in this chapter. Enough has been discussed about operational amplifiers in the first chapters of this book so that we will not dwell on their properties here.

We will begin our discussion of active filters in Sec. 8.1 by making statements about active filters in general. Then in Sec. 8.2 we will discuss transfer functions and their parameters. Useful formulas are presented to help evaluate the effects of tolerances and temperature coefficients of resistors and capacitors. In Sec. 8.3 we will then describe several realizations and provide design equations and sensitivity equations. The basic sensitivity relations are derived and discussed in Appendix C. After we have become familiar with the circuit realizations, we will discuss tuning (Sec. 8.4), how operational amplifier characteristics affect filter performance (Sec. 8.5), and, briefly, the characteristics of resistors and capacitors (Sec. 8.6). The chapter concludes with a set of filter design and tuning tables (Sec. 8.7).

8.1 Active Filter Characteristics

The active element, in this case the operational amplifier, in active networks is necessary to permit the realization of complex left hand plane poles using only resistors and capacitors for the passive elements. The operational amplifier permits the use of reasonable-valued resistors and capacitors even at frequencies as low as 10^{-3} Hz. An added bonus is the isolation afforded by the low output impedances of individual stages so that network stages can be designed and tuned independently with minimal interaction. Other active elements, the negative immittance converter and the gyrator, can be implemented with operational amplifiers but for practical reasons are not widely used.

Active filters have some characteristics of their own that make them sufficiently different from passive filters that one who uses them must be aware of these differences. For example, active filters usually have single-ended inputs and outputs and thus do not "float" with respect to the system power supply or common as a passive RLC network can. Amplifiers used for active elements have a limited input and output voltage range (± 10 V for most operational amplifier circuits) and an output current capability of a few milliamperes.

The outputs of active filters built with operational amplifiers have a dc voltage offset which drifts with ambient temperature changes. The voltage offset might range from a few microvolts up to several hundred millivolts. Drifts may range from 1 to 100 μV/°C or even more from a multiple-pole low-pass filter built up of many pole-pair stages. The inputs of active filters may have a bias current; this would be true for low-pass and band-reject filters and may be true for bandpass and high-pass filters, depending upon the particular circuit realization. The bias current may range from a few picoamperes for field-effect transistor operational amplifiers to a few microamperes for bipolar transistor and integrated-circuit amplifiers.

Active filters can provide excellent isolation capabilities, that is, a high input impedance ranging from a few kilohms to several thousand megohms if input buffer amplifiers are used, and a low output impedance ranging from a few hundred ohms down to less than 1 Ω. Unity-gain bandwidths as high as 100 MHz are available in operational amplifiers and permit filter designs in the vicinity of 1 Mc. Slewing rate, which is related to full-power response, is the limiting factor for large-signal characteristics. Frequencies as low as 10^{-3} Hz are possible, but filters at these frequencies can become rather bulky because of capacitor sizes. Active filters can have voltage gain, as much as 40 dB in low-frequency low-Q filters.

The primary advantage of active filters is their small size and weight for low-frequency applications and their ruggedness.

All types of responses are possible: the old standards, Butterworth, Chebyshev, and Bessel (Thompson), single-tuned and stagger-tuned bandpass as well as other responses that meet special needs.

The range of Q's possible for active filters extends up to Q's of a few hundred. However, high-Q networks capable of maintaining stability of their characteristics, in the face of element changes with time, temperature, voltage, and frequency, require more expensive (and usually larger size) resistors and capacitors and generally more operational amplifiers than low-Q (less than 10) filters. These facts will become apparent as individual circuits are discussed.

8.2 Pole Pairs, Network Functions, and Parameters

The circuits to be described realize a single-pole or a single complex pole pair. More complicated filters are then built up from these individual building blocks. This approach permits ease of design and tuning of a complex filter, an important practical matter, by reducing interactions between elements. This approach also permits a single systematic approach to answering the question: What happens to the response of a filter if the network element values are not accurate and if they drift with time and temperature?

The filter network functions that are of most interest are magnitude, phase, and group delay. The network parameters that are important are some characteristic frequency, Q, and passband gain. In this section these functions and parameters will be briefly examined for single-pole and complex-pole-pair networks for low-pass, high-pass, and bandpass networks. These relations will all be useful in the next section for deriving the sensitivity functions of these network realizations.

8.2.1 Low-pass network functions

Single Pole. The single-pole low-pass transfer function in the complex frequency variables is

$$H(s) = \frac{H_o\omega_o}{s + \omega_o}$$

The magnitude of the transfer function for the response to sinusoidal steady-state excitation is

$$|H(j\omega)| = G(\omega) = \left(\frac{H_o^2\omega_o^2}{\omega^2 + \omega_o^2}\right)^{1/2}$$

The phase is

$$\phi(\omega) = -\arctan\frac{\omega}{\omega_o}$$

and the group delay is

$$\tau(\omega) = -\frac{d\phi(\omega)}{d\omega} = \frac{\cos^2\phi}{\omega_o}$$

Complex Conjugate Pole Pair. The complex-conjugate-pole-pair low-pass transfer function and the sinusoidal steady-state magnitude and phase functions are

$$H(s) = \frac{H_o\omega_o^2}{s^2 + \alpha\omega_o s + \omega_o^2}$$

$$|H(j\omega)| = G(\omega) = \left[\frac{H_o^2\omega_o^4}{\omega^4 + \omega^2\omega_o^2(\alpha^2 - 2) + \omega_o^4}\right]^{1/2}$$

$$\phi(\omega) = -\arctan\left[\frac{1}{\alpha}\left(2\frac{\omega}{\omega_o} + \sqrt{4 - \alpha^2}\right)\right] - \arctan\left[\frac{1}{\alpha}\left(2\frac{\omega}{\omega_o} - \sqrt{4 - \alpha^2}\right)\right]$$

The relation for phase given above is expressed in a form suitable for general computer use since, on many computers, the arctan function can be determined only for the principal angle. Note that α^2 is usually never greater than 4. If it is, the poles will no longer be complex. The Q of a complex pole pair equals $1/\alpha$.

The group delay for a complex conjugate pole pair is

$$\tau(\omega) = \frac{2\sin^2\phi}{\alpha\omega_o} - \frac{\sin 2\phi}{2\omega}$$

8.2.2 High-pass network functions

Single Pole. The single-pole high-pass transfer function and the sinusoidal steady-state magnitude, phase, and delay functions are

$$H(s) = \frac{H_o s}{s + \omega_o}$$

$$G(\omega) = \left(\frac{H_o^2\omega^2}{\omega^2 + \omega_o^2}\right)^{1/2}$$

$$\phi(\omega) = \frac{\pi}{2} - \arctan\frac{\omega}{\omega_o}$$

$$\tau(\omega) = \frac{\sin^2\phi}{\omega_o}$$

Complex Conjugate Pole Pair. The complex-conjugate-pole-pair high-pass transfer function and the sinusoidal steady-state magnitude, phase, and delay functions are

$$H(s) = \frac{H_o s^2}{s^2 + \alpha\omega_o s + \omega_o^2}$$

$$G(\omega) = \left[\frac{H_o^2\omega^4}{\omega^4 + \omega^2\omega_o^2(\alpha^2 - 2) + \omega_o^4}\right]^{1/2}$$

$$\phi(\omega) = \pi - \arctan\left[\frac{1}{\alpha}\left(2\frac{\omega}{\omega_o} + \sqrt{4 - \alpha^2}\right)\right] - \arctan\left[\frac{1}{\alpha}\left(2\frac{\omega}{\omega_o} - \sqrt{4 - \alpha^2}\right)\right]$$

$$\tau(\omega) = \frac{2\sin^2\phi}{\alpha\omega_o} - \frac{\sin 2\phi}{2\omega}$$

8.2.3 Bandpass network function The complex-conjugate-pole-pair bandpass transfer function is

$$H(s) = \frac{H_o\alpha\omega_o s}{s^2 + \alpha\omega_o s + \omega_o^2}$$

where

$$\alpha = \frac{1}{Q} \quad \text{and} \quad Q = \frac{\omega_o}{\omega_2 - \omega_1} = \frac{f_o}{f_2 - f_1}$$

and where f_2 and f_1 are the frequencies where the magnitude response is -3 dB from H_o, the passband gain which occurs at $\omega_o = 2\pi f_o$. The sinusoidal steady-state transfer function may be written in the form

$$H(j\omega) = \frac{H_o}{1 + jQ(\omega/\omega_o - \omega_o/\omega)}$$

Thus, the magnitude, phase, and delay functions are

$$G(\omega) = \left[\frac{H_o^2}{1 + Q^2(\omega/\omega_o - \omega_o/\omega)^2}\right]^{1/2} = \left[\frac{H_o^2\alpha^2\omega_o^2\omega^2}{\omega^4 + \omega^2\omega_o^2(\alpha^2 - 2) + \omega_o^4}\right]^{1/2}$$

$$\phi(\omega) = \frac{\pi}{2} - \arctan\left(\frac{2Q\omega}{\omega_o} + \sqrt{4Q^2 - 1}\right) - \arctan\left(2Q\frac{\omega}{\omega_o} - \sqrt{4Q^2 - 1}\right)$$

$$\tau(\omega) = \frac{2Q\cos^2\phi}{\omega_o} + \frac{\sin 2\phi}{2\omega}$$

8.2.4 Band-reject network function A band-reject filter can be realized by performing the operation $1 - H_{BP}(s)$, where $H_{BP}(s)$ is a bandpass

transfer function (Fig. 8.1). If $R' = RH_o$ (bandpass)

$$H(s) = -\frac{s^2 + \omega_o^2}{s^2 + \alpha\omega_o s + \omega_o^2}\frac{R_F}{R}$$

Since this filter is very closely related to the bandpass filter, its properties will not be discussed.

8.3 Filter Realizations[1,2]

In this section we shall present some realizations for active filters. The operational amplifier filter circuits to be analyzed, and for which design procedures and sensitivity equations are given, are the infinite-gain multiple feedback, controlled source, infinite-gain state-variable feedback, and negative immittance converter realizations. Another realization sometimes used is the infinite-gain single-feedback type. This type involves the use of bridged-T and twin-T networks as well as requiring the cancellation of unwanted zeros and poles. Thus this type requires many elements to realize a transfer function with complex poles and is therefore uneconomical. Trimming and adjustment of bridged-T or twin-T networks is difficult since the passive elements interact to a high degree in such networks. For these reasons this circuit will not be discussed. Single real pole realizations will not be shown since these are rather trivial and easy to design. In addition, single-operational-amplifier single-pole circuits are rather uneconomical.

Design procedures given in this section are only suggested procedures. Other choices are possible, and as one gains experience with these circuits, it becomes desirable to design procedures for minimizing sensitivity in certain network parameters or to ensure a convenient spread of element values. In the design procedures given, the capacitors are always made equal. In addition, one usually starts the design process by selecting the capacitor value because there are fewer standard values of capacitors than there are resistors. Resistors are less expensive than capacitors and are more easily used in trimming schemes. In some cases the passband gain

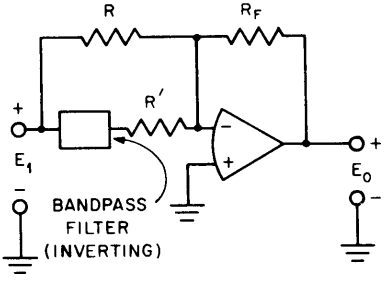

Fig. 8.1 Band-reject filter.

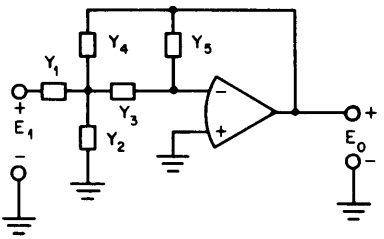

Fig. 8.2 Infinite-gain multiple-feedback circuit.

H_o is a free parameter. It is often convenient to let H_o be a variable which can be used as a parameter for determining optimum, or at least small, sensitivities of certain parameters. An example of this is given in the controlled-source circuit designs. Also, letting H_o be a free parameter simplifies complicated design equations.

8.3.1 Infinite-gain multiple-feedback circuits Figure 8.2 illustrates the infinite-gain multiple-feedback connection for a pair of complex conjugate s-plane poles with zeros restricted to the origin or infinity. The amplifier is used in its inverting configuration, with the + input grounded. Each element Y_i represents a single resistor or capacitor. The voltage transfer function is

$$\frac{E_o}{E_1}(s) = \frac{-Y_1Y_3}{Y_5(Y_1 + Y_2 + Y_3 + Y_4) + Y_3Y_4 + (1/A_{OL})[(Y_3 + Y_5)(Y_1 + Y_2 + Y_4) + Y_3Y_5]}$$

In the limiting case as A_{OL} approaches infinity we obtain

$$\frac{E_o}{E_1}(s) = \frac{-Y_1Y_3}{Y_5(Y_1 + Y_2 + Y_3 + Y_4) + Y_3Y_4}$$

Examples that follow show how these five elements may be chosen so as to realize low-pass, high-pass and bandpass network functions.

Low Pass. The infinite-gain multiple-feedback circuit for a low-pass network function is shown in Fig. 8.3. The voltage transfer function is

$$\frac{E_o}{E_1}(s) = \frac{-1/R_1R_3C_2C_5}{s^2 + (s/C_2)(1/R_1 + 1/R_3 + 1/R_4) + 1/R_3R_4C_2C_5}$$

Note that this circuit produces a signal inversion, as will all circuits realized by this technique.

For this circuit, following the notation of the low-pass network function,

$$H_o = \frac{R_4}{R_1}$$

$$\omega_o = \left(\frac{1}{R_3R_4C_2C_5}\right)^{1/2}$$

$$\alpha = \sqrt{\frac{C_5}{C_2}}\left(\sqrt{\frac{R_3}{R_4}} + \sqrt{\frac{R_4}{R_3}} + \frac{\sqrt{R_3R_4}}{R_1}\right)$$

$$\phi = \pi + \phi_{LP}$$

$$\tau = \tau_{LP}$$

Note that the phase inversion has been incorporated into the phase function. A tuning procedure for this circuit would be first to adjust ω_o with R_3 at a frequency of 10ω, as outlined in the section on tuning. Then adjust α with R_1 at the α peaking frequency.

The sensitivities of the network parameters to circuit element changes follow. Remember that the open-loop gain of the operational amplifier is assumed to be infinite (at least very large), and so sensitivity functions for open-loop gain changes are not considered.

$$S_{R_3}^{\omega_o} = S_{R_4}^{\omega_o} = S_{C_2}^{\omega_o} = S_{C_5}^{\omega_o} = -\frac{1}{2}$$

$$S_{C_5}^{\alpha} = -S_{C_2}^{\alpha} = \frac{1}{2}$$

$$S_{R_1}^{\alpha} = \frac{1}{\alpha\omega_o R_1 C_2}$$

$$S_{R_3}^{\alpha} = \frac{1}{2} - \frac{1}{\alpha\omega_o R_3 C_2}$$

$$S_{R_4}^{\alpha} = \frac{1}{2} - \frac{1}{\alpha\omega_o R_4 C_2}$$

$$S_{R_4}^{H_o} = -S_{R_1}^{H_o} = 1$$

Note that $S_{C_2}^{\alpha}$ and $S_{C_5}^{\alpha}$ are constant and opposite in sign and so are $S_{R_1}^{H_o}$ and $S_{R_4}^{H_o}$.

DESIGN PROCEDURE

Given: H_o, α, $\omega_o = 2\pi f_o$

Choose: $C_2 = C$, a convenient value

$C_5 = KG$

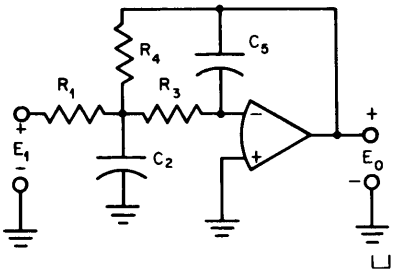

Fig. 8.3 Multiple-feedback low-pass filter.

$$\text{Calculate: } R_4 = \frac{\alpha}{2\omega_o C}\left[1 \pm \sqrt{1 - \frac{4(H_o + 1)}{K\alpha^2}}\right]$$

$$R_1 = \frac{R_4}{H_o}$$

$$R_3 = \frac{1}{\omega_o^2 C^2 R_4 K}$$

For best results H_o should be less than 10 for circuits with an α of about 0.1 ($Q = 10$) and can be as high as 100 for an α of about 1 ($Q = 1$) or less. These extreme limits assume that the operational amplifier has an open-loop gain of at least 80 dB at the frequency of interest. The effects of finite open-loop gain for multiple feedback circuits will be discussed later.

High Pass. A high-pass realization is illustrated in Fig. 8.4. The voltage transfer function is

$$\frac{E_o}{E_i}(s) = \frac{-(C_1/C_4)s^2}{s^2 + s(1/R_5)(C_1/C_3C_4 + 1/C_4 + 1/C_3) + 1/R_2R_5C_3C_4}$$

In terms of our high-pass network function

$$H_o = \frac{C_1}{C_4}$$

$$\omega_o = \left(\frac{1}{R_2R_5C_3C_4}\right)^{1/2}$$

$$\alpha = \sqrt{\frac{R_2}{R_5}}\left(\frac{C_1}{\sqrt{C_3C_4}} + \sqrt{\frac{C_3}{C_4}} + \sqrt{\frac{C_4}{C_3}}\right)$$

$$\phi = \pi + \phi_{HP}$$

$$\tau = \tau_{HP}$$

Tuning this high-pass filter will have to be done in the reverse order to that of the low-pass filter. First, adjust α with R_2 or R_5 at the frequency where the α peak occurs (the ω_α frequency is not known

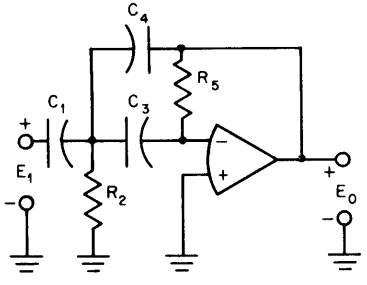

Fig. 8.4 Multiple-feedback high-pass filter.

because ω_o has not been set yet). Then adjust ω_o by adjusting R_2 and R_5 simultaneously by the *same* percentage: α will remain constant. A trimming scheme involving C_1 would be simpler. The sensitivities to element value changes are

$$S_{R_2}^{\omega_o} = S_{R_5}^{\omega_o} = S_{C_3}^{\omega_o} = S_{C_4}^{\omega_o} = -\frac{1}{2}$$

$$S_{R_2}^{\alpha} = -S_{R_5}^{\alpha} = \frac{1}{2}$$

$$S_{C_3}^{\alpha} = \frac{1}{2} - \frac{1}{\alpha\omega_o R_5 C_3}\left(\frac{C_1}{C_3} + 1\right)$$

$$S_{C_4}^{\alpha} = \frac{1}{2} - \frac{1}{\alpha\omega_o R_5 C_4}\left(\frac{C_1}{C_3} + 1\right)$$

$$S_{C_1}^{\alpha} = \frac{1}{\alpha\omega_o R_5}\frac{C_1}{C_3 C_4}$$

$$S_{C_1}^{H_o} = -S_{C_4}^{H_o} = 1$$

DESIGN PROCEDURE

Given: H_o, α, $\omega_o = 2\pi f_o$

Choose: $C = C_1 = C_3$, a convenient value

Calculate: $R_5 = \dfrac{1}{\alpha\omega_o C}(2H_o + 1)$

$$R_2 = \frac{\alpha}{\omega_o C(2H_o + 1)}$$

$$C_4 = \frac{C_1}{H_o}$$

Again, restrictions on H_o are the same as those for the low-pass case. Note that this realization requires three capacitors, a feature which might make it undesirable when compared with other circuits.

Bandpass 1. There are several configurations of the five elements which may be used to realize a bandpass function. One of the more practical configurations is the one shown in Fig. 8.5. The voltage transfer function is

$$\frac{E_o}{E_1}(s) = \frac{-s(1/R_1C_4)}{s^2 + s(1/R_5)(1/C_3 + 1/C_4) + (1/R_5C_3C_4)(1/R_1 + 1/R_2)}$$

In terms of our bandpass network function

$$H_o = \frac{1}{(R_1/R_5)(1 + C_4/C_3)}$$

$$\omega_o = \left[\frac{1}{R_5C_3C_4}\left(\frac{1}{R_1} + \frac{1}{R_2}\right)\right]^{1/2}$$

$$\frac{1}{Q} = \alpha = \sqrt{\frac{1}{R_5(1/R_1 + 1/R_2)}}\left[\sqrt{\frac{C_3}{C_4}} + \sqrt{\frac{C_4}{C_3}}\right]$$

$$\phi = \pi + \phi_{BP}$$

$$\tau = \tau_{BP}$$

Tuning this filter appears rather formidable. In practice $R_1 \gg R_2$ and so R_2 can be used to trim the Q. Then, to adjust the center frequency, R_2 and R_5 can be simultaneously adjusted by the same percentage with negligible effect on the Q.

The sensitivities of the network parameters with respect to the elements are

$$S_{R_5}^{\omega_o} = S_{C_3}^{\omega_o} = S_{C_4}^{\omega_o} = -\frac{1}{2}$$

$$S_{R_1}^{\omega_o} = \frac{-1}{2\omega_o^2 R_1 R_5 C_3 C_4}$$

$$S_{R_2}^{\omega_o} = \frac{-1}{2\omega_o^2 R_2 R_5 C_3 C_4}$$

$$S_{R_1}^{Q} = \frac{R_1}{2(R_1 + R_2)} - \frac{1}{2}$$

$$S_{R_2}^{Q} = \frac{R_2}{2(R_1 + R_2)} - \frac{1}{2}$$

$$S_{R_5}^{Q} = \frac{1}{2}$$

$$S_{C_3}^{Q} = \frac{Q}{\omega_o R_5 C_3} - \frac{1}{2}$$

$$S_{C_4}^{Q} = \frac{Q}{\omega_o R_5 C_4} - \frac{1}{2}$$

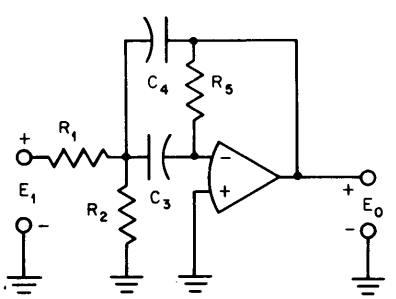

Fig. 8.5 Multiple-feedback bandpass filter.

DESIGN PROCEDURE

Given: H_o, $Q = \frac{1}{\alpha}$, $\omega_o = 2\pi f_o$

Choose: $C = C_3 = C_4$

Calculate: $Q = \frac{1}{\alpha}$

$$R_1 = \frac{Q}{H_o \omega_o C}$$

$$R_2 = \frac{Q}{(2Q^2 - H_o)\omega_o C}$$

$$R_5 = \frac{2Q}{\omega_o C}$$

Again, restrictions on H_o apply to guarantee that the design equations give fairly accurate results.

Bandpass 2. Another multiple-feedback circuit uses an additional active element to overcome some of the disadvantages of the single-amplifier circuit, especially the bandpass realization for Q's roughly between 10 and 50. High Q's realized with bandpass 1 have large spreads of element values and high Q sensitivities to element value changes. The multiple-feedback circuit with positive feedback is shown in Fig. 8.6. The voltage transfer function is

$$\frac{E_o}{E_1}(s) = \frac{s(K/R_1C_4)}{s^2 + (s/R_5C_4)(1 + C_4/C_3 - KR_5/R_6) + (1/C_3C_4R_5)(1/R_1 + 1/R_2 + 1/R_6)}$$

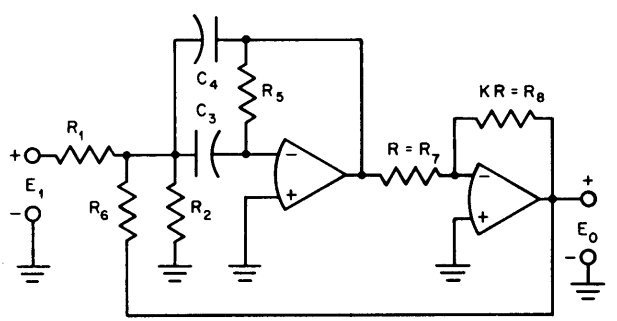

Fig. 8.6 Multiple-feedback bandpass circuit with positive feedback.

Note that the output is taken at the second amplifier. The overall signal transfer is noninverting. The circuit parameters are

$$H_o = \frac{1}{R_1} \frac{1}{(1/KR_5)(1 + C_4/C_3) - 1/R_6}$$

$$\omega_o = \left[\frac{1}{R_5C_3C_4}\left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_6}\right)\right]^{1/2}$$

$$\frac{1}{Q} = \alpha = \sqrt{\frac{1}{R_5(1/R_1 + 1/R_2 + 1/R_6)}}\sqrt{\frac{C_3}{C_4}}\left(1 + \frac{C_4}{C_3} - \frac{KR_5}{R_6}\right)$$

$$\phi = \phi_{BP}$$

$$\tau = \tau_{BP}$$

Since R_1 and R_6 are larger than R_2, R_2 is used to trim the center frequency. Note that in this circuit Q can be adjusted with K without influencing ω_o. The sensitivity of the network parameters to element value changes are

$$S_{R_1}^{H_o} = -1$$

$$S_{C_3}^{H_o} = -S_{C_4}^{H_o} = \frac{H_o}{K}\frac{R_1}{R_5}\frac{C_4}{C_3}$$

$$S_K^{H_o} = S_{R_5}^{H_o} = \frac{H_o}{K}\frac{R_1}{R_5}\left(1 + \frac{C_4}{C_3}\right)$$

$$S_{R_6}^{H_o} = -H_o\frac{R_1}{R_6}$$

$$S_{C_3}^{\omega_o} = S_{C_4}^{\omega_o} = S_{R_5}^{\omega_o} = -\frac{1}{2}$$

$$S_{R_1}^{\omega_o} = \frac{-1}{2\omega_o^2R_1R_5C_3C_4}$$

$$S_{R_2}^{\omega_o} = \frac{-1}{2\omega_o^2R_2R_5C_3C_4}$$

$$S_{R_6}^{\omega_o} = \frac{-1}{2\omega_o^2R_5R_6C_3C_4}$$

$$S_{R_1}^{Q} = \frac{-1}{2\omega_o^2R_1R_5C_3C_4}$$

$$S_{R_2}^{Q} = \frac{-1}{2\omega_o^2R_2R_5C_3C_4}$$

$$S_{R_6}^{Q} = -\frac{1}{2}\frac{1}{(1 + R_6/R_1 + R_6/R_2)} - \frac{1}{(R_6/KR_5)(1 + C_4/C_3) - 1}$$

$$S_{C_3}^{Q} = \frac{Q}{\omega_oR_5C_3} - \frac{1}{2}$$

$$S_{C_4}^{Q} = \frac{Q}{\omega_o R_5 C_4}\left(1 - \frac{KR_5}{R_6}\right) - \frac{1}{2}$$

$$S_{R_3}^{Q} = \frac{Q}{\omega_o R_5 C_4}\left(1 + \frac{C_4}{C_3}\right) - \frac{1}{2}$$

$$S_K^{Q} = \frac{-KQ}{\omega_o R_6 C_4}$$

$$S_{R_a}K = -S_{R_b}K = 1$$

DESIGN PROCEDURE

Given: $Q = 1/\alpha$, $\omega_o = 2\pi f_o$

H_o must be a free parameter.

Choose: $C = C_3 = C_4$, $R = R_1 = R_5$

K is chosen to reduce the spread of element values or to optimize sensitivity. It might typically be between 1 and 10.

Calculate: $R = \dfrac{Q}{\omega_o C}$

$$R_6 = R\frac{KQ}{2Q - 1}$$

$$G_2 = \frac{1}{R_2} = \frac{1}{R}\left(Q - 1 - \frac{2}{K} + \frac{1}{KQ}\right)$$

For this procedure, $H_o = \sqrt{Q}\,K$.

This completes the section on infinite-gain multiple-feedback realizations. A few general comments are in order. An advantage of this realization is that the output impedance is low; thus networks may be cascaded with negligible interaction. A disadvantage is that it is not possible to obtain high Q without resorting to large spreads of element values and also incurring large Q sensitivities. The multiple-feedback realization with positive feedback can overcome this and allow reasonable sensitivities up to a Q of 50.

8.3.2 Controlled-source circuits A noninverting voltage-controlled voltage source (VCVS) implemented with an operational amplifier is illustrated in Fig. 8.7. The input impedance is very large, tens to hundreds of thousands of megohms, depending upon the type of operational amplifier, and the output impedance is very low, usually less than 1 Ω for K between 1 and 10. The voltage transfer function is

$$\frac{E_o}{E_1}(s) = 1 + \frac{R_b}{R_a} = K$$

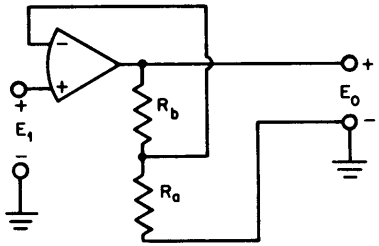

Fig. 8.7 Noninverting operational amplifier VCVS.

The sensitivities of K to the two resistors are

$$S_{R_b}^{K} = 1$$
$$S_{R_a}^{K} = -1$$

Figure 8.8 shows the controlled-source connection for a circuit which may be used to realize voltage transfer functions with a single pair of complex conjugate s-plane poles with zeros restricted to the origin or infinity. The Y_i are restricted to be single elements, R's and C's. These five elements may be chosen so as to realize low-pass, high-pass, and bandpass network functions. Realizations are possible with $K < 0$; but, since this operational amplifier circuit always has K greater than +1, these will not be discussed. The voltage transfer function is

$$\frac{E_o}{E_1}(s) = \frac{KY_1Y_4}{Y_5(Y_1 + Y_2 + Y_3 + Y_4) + [Y_1 + Y_2(1 - K) + Y_3]}$$

Low Pass. A VCVS circuit for a low-pass network function is shown in Fig. 8.9. The voltage transfer function is

$$\frac{E_o}{E_1}(s) = \frac{K/R_1R_2C_1C_2}{s^2 + s[1/R_1C_1 + 1/R_2C_1 + (1 - K)/R_2C_2] + 1/R_1R_2C_1C_2}$$

The network parameters are

$$H_o = K$$
$$\omega_o = \left(\frac{1}{R_1R_2C_1C_2}\right)^{1/2}$$

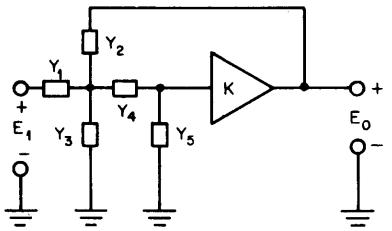

Fig. 8.8 VCVS configuration for a second-degree voltage transfer function.

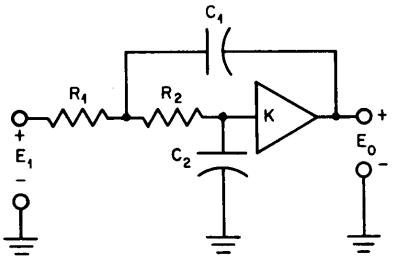

Fig. 8.9 VCVS low-pass network.

$$\alpha = \left(\frac{R_2C_2}{R_1C_1}\right)^{1/2} + \left(\frac{R_1C_2}{R_2C_1}\right)^{1/2} + \left(\frac{R_1C_1}{R_2C_2}\right)^{1/2} - K\left(\frac{R_1C_1}{R_2C_2}\right)^{1/2}$$

$$\phi = \phi_{LP}$$

$$\tau = \tau_{LP}$$

Controlled-source circuits are easier to tune than other circuit realizations. In fact, they can be adjusted over wide ranges without interaction of the network parameters. ω_o is tuned by adjusting R_1 and R_2 by equal percentages: α will not be affected. Capacitance C_1 and C_2 can be adjusted in the same way for the same result. α is trimmed by adjusting K. The sensitivities of the network parameters to element value changes are

$$S_{R_1}^{\omega_0} = S_{R_2}^{\omega_0} = S_{C_1}^{\omega_0} = S_{C_2}^{\omega_0} = -\frac{1}{2}$$

$$S_K^{H_0} = 1$$

$$S_{R_1}^{\alpha} = \frac{1}{2} - \frac{1}{\alpha\omega_0 R_1 C_1}$$

$$S_{R_2}^{\alpha} = \frac{1}{2} - \frac{1}{\alpha\omega_0 R_2}\left(\frac{1}{C_1} + \frac{1-K}{C_2}\right)$$

$$S_{C_1}^{\alpha} = \frac{1}{2} - \frac{1}{\alpha\omega_0 C_1}\left(\frac{1}{R_1} + \frac{1}{R_2}\right)$$

$$S_{C_2}^{\alpha} = \frac{1}{2} - \frac{1-K}{\alpha\omega_0 R_2 C_2}$$

$$S_K^{\alpha} = \frac{-K}{\alpha\omega_0 R_2 C_2}$$

DESIGN PROCEDURE

Given: H_o, α, $\omega_o = 2\pi f_o$

Choose: $C_1 = C_2 = C$, a convenient value

Calculate: $K = H_o > 2$

$$R_2 = \frac{\alpha}{2\omega_o C}\left[1 + \sqrt{1 + \frac{4(H_o - 2)}{\alpha^2}}\right]$$

$$R_1 = \frac{1}{\omega_o^2 C^2 R_2}$$

If H_o is large, say greater than 10, there will be large spreads in element values and high sensitivities. An interesting design procedure is to use K to vary the sensitivities of circuit parameters.

Capacitors are often the components which have the largest temperature coefficients. It is possible to set K such that the overall α sensitivity is minimum, assuming that the capacitors drift equally. In this case we set $S_{C_1}^{\alpha} = -S_{C_2}^{\alpha}$.

Choose $C = C_1 = C_2$ and let $R_1 = R_2 = R$; then $K = 3 - \alpha$ and $R = 1/\omega_o C$.

High Pass. A VCVS circuit realization of a high-pass network function is shown in Fig. 8.10. The voltage transfer function is

$$\frac{E_o}{E_1}(s) = \frac{Ks^2}{s^2 + s[1/R_2C_1 + 1/R_2C_2 + (1 - K)/R_1C_1] + 1/R_1R_2C_1C_2}$$

The network parameters are

$$H_o = K$$

$$\omega_o = \left(\frac{1}{R_1R_2C_1C_2}\right)^{1/2}$$

$$\alpha = \left(\frac{R_1C_1}{R_2C_2}\right)^{1/2} + \left(\frac{R_1C_2}{R_2C_1}\right)^{1/2} + \left(\frac{R_2C_2}{R_1C_1}\right)^{1/2} - K\left(\frac{R_2C_2}{R_1C_1}\right)^{1/2}$$

The same comments about frequency adjustment and tuning that we mentioned in the low-pass case apply for the high-pass case also. The network parameter sensitivities with respect to element value changes are

$$S_{R_1}^{\omega_o} = S_{R_2}^{\omega_o} = S_{C_1}^{\omega_o} = S_{C_2}^{\omega_o} = -\frac{1}{2}$$

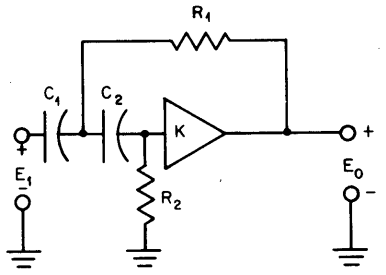

Fig. 8.10 VCVS high-pass network.

$$S_{R_1}^{\alpha} = \frac{1}{2} - \frac{1 - K}{R_1 C_1 \alpha \omega_o}$$

$$S_{R_2}^{\alpha} = \frac{1}{2} - \frac{1}{R_2}\left(\frac{1}{C_1} + \frac{1}{C_2}\right)\frac{1}{\alpha \omega_o}$$

$$S_{C_1}^{\alpha} = \frac{1}{2} - \frac{1}{\alpha \omega_o C_1}\left(\frac{1 - K}{R_1} + \frac{1}{R_2}\right)$$

$$S_{C_2}^{\alpha} = \frac{1}{2} - \frac{1}{\alpha \omega_o C_2 R_2}$$

$$S_K^{\alpha} = \frac{-K}{\alpha \omega_o R_1 C_1}$$

$$S_K^{H_o} = 1$$

DESIGN PROCEDURE

Given H_o, α, $\omega_o = 2\pi f_o$

Choose $C_1 = C_2 = C$

Calculate: $R_1 = \dfrac{\alpha + \sqrt{\alpha^2 + 8(H_o - 1)}}{4\omega_o C}$

$$R_2 = \frac{4}{\omega_o C} \frac{1}{\sqrt{\alpha^2 + 8(H_o - 1)}}$$

Naturally, $H_o = K$ must be such that R_1 and R_2 are positive-valued resistors. Again, a large H_o will result in a large spread of element values and high sensitivities. We can use the same scheme for making $S_{C_1}^{\alpha} = -S_{C_2}^{\alpha}$ as in the low-pass case.

Choose $C_1 = C_2 = C$; let $R_1 = R_2 = R$. Then $K = 3 - \alpha$ and $R = 1/\omega_o C$.

Bandpass 1. A VCVS realization for the bandpass network function is shown in Fig. 8.11. The voltage transfer function is

$$\frac{E_o}{E_1}(s) = \frac{Ks/R_1C_2}{s^2 + s\left[\frac{1}{R_3C_2} + \frac{1}{R_1C_2} + \frac{1}{R_1C_1} + \frac{1}{R_2C_1} + \frac{1 - K}{R_2C_2}\right] + \frac{1}{R_3}\left(\frac{1}{R_1} + \frac{1}{R_2}\right)\frac{1}{C_1C_2}}$$

The network parameters are

$$H_o = \frac{K}{1 + R_1/R_3 + C_2/C_1(1 + R_1/R_2) + (1 - K)(R_1/R_2)}$$

$$\omega_o = \left[\frac{1}{R_3}\left(\frac{1}{R_1} + \frac{1}{R_2}\right)\frac{1}{C_1C_2}\right]^{1/2}$$

$$\frac{1}{Q} = \alpha = \sqrt{\frac{R_3}{(1/R_1 + 1/R_2)}}\left[\sqrt{\frac{C_1}{C_2}}\left(\frac{1}{R_1} + \frac{1}{R_3} + \frac{1-K}{R_2}\right) + \sqrt{\frac{C_2}{C_1}}\left(\frac{1}{R_1} + \frac{1}{R_2}\right)\right]$$

The sensitivities of the network parameters to element changes are

$$S_{C_1}^{\omega_o} = S_{C_2}^{\omega_o} = S_{R_3}^{\omega_o} - \frac{1}{2}$$

$$S_{R_1}^{\omega_o} = \frac{-1}{2\omega_o^2 R_1 C_1 R_3 C_2} \qquad S_{R_2}^{\omega_o} = \frac{-1}{2\omega_o^2 R_3 C_1 R_2 C_2}$$

$$S_K^Q = \frac{+KQ}{\omega_o R_2 C_2} \qquad S_{R_1}^Q = \frac{-1}{2(1 + R_1/R_2)} + \frac{Q_1}{\omega_o R_1}\left(\frac{1}{C_1} + \frac{1}{C_2}\right)$$

$$S_{R_2}^Q = \frac{-1}{2(1 + R_2/R_1)} + \frac{Q}{\omega_o R_2}\left(\frac{1}{C_1} + \frac{1-K}{C_2}\right)$$

$$S_{R_3}^Q = \frac{-1}{2} + \frac{Q}{\omega_o R_3 C_2} \qquad S_{C_1}^Q = -\frac{1}{2} + \frac{1}{\alpha\omega_o C_1}\left(\frac{1}{R_1} + \frac{1}{R_2}\right)$$

$$S_{C_2}^Q = \frac{-1}{2} + \frac{Q}{\alpha\omega_o C_2}\left(\frac{1}{R_1} + \frac{1}{R_3} + \frac{1-K}{R_2}\right)$$

$$S_K^{H_o} = 1 + \frac{Q}{\omega_o R_2 C_2}$$

$$S_{R_1}^{H_o} = \frac{Q}{\omega_o R_1}\left(\frac{1}{C_1} + \frac{1}{C_2}\right) - 1$$

$$S_{R_2}^{H_o} = \frac{Q}{\omega_o R_2}\left(\frac{1}{C_1} + \frac{1-K}{C_2}\right)$$

$$S_{R_3}^{H_o} = \frac{Q}{\omega_o R_3 C_2}$$

$$S_{C_1}^{H_o} = \frac{Q}{\omega_o C_1}\left(\frac{1}{R_1} + \frac{1}{R_2}\right)$$

$$S_{C_2}^{H_o} = \frac{Q}{\omega_o C_2}\left(\frac{1}{R_1} + \frac{1}{R_3} + \frac{1-K}{R_2}\right) - 1$$

DESIGN PROCEDURE

The *general* design formulas obtained by solving the network parameter equations for the circuit elements are very complicated. The following design procedure, however, has been found to be useful. It gives a fairly good spread of element values.

Given: Q, $\omega_o = 2\pi f_o$

H_o will be a free parameter,

Choose: $C = C_1 = C_2$, a convenient value

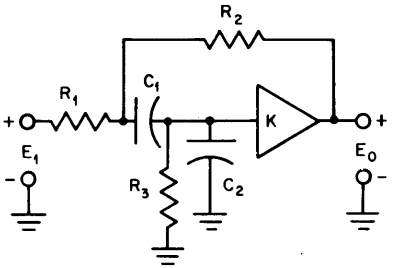

Fig. 8.11 VCVS bandpass network.

Calculate: $K = 5 - \frac{\sqrt{2}}{Q}$

$$R = \frac{\sqrt{2}}{\omega_o C}$$

Then

$$H_o = \frac{5}{\sqrt{2}} Q - 1$$

High-Q circuits will have a large spread of element values and high sensitivities. Q's should be less than 10 for best results.

Four other bandpass circuits are realizable by using the VCVS with $K > 0$. One is obtained by removing C_2 in the circuit of Fig. 8.11 and connecting one terminal to the node formed by $C_1 - R_1 - R_2$ and the other terminal to ground. Two others are generated by interchanging the locations of the resistors and capacitors in the circuit of Fig. 8.11 and the one mentioned above. These two are of less practical interest because they require three capacitors and one of the capacitors is a series capacitor at the input.

Bandpass 2. Still another bandpass realization is illustrated in Fig. 8.12. The voltage transfer function is

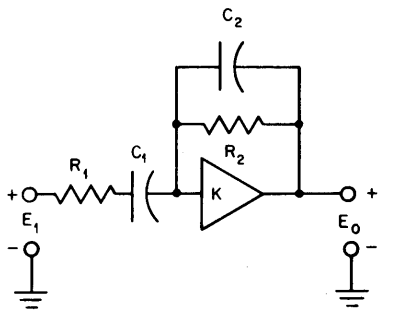

Fig. 8.12 Alternative VCVS bandpass network.

$$\frac{E_o}{E_1}(s) = \frac{s\dfrac{K}{1-K}\dfrac{1}{R_1C_2}}{s^2 + s\left[\dfrac{1}{R_2C_2} + \dfrac{1}{R_1C_1} + \dfrac{1}{R_1C_2(1-K)}\right] + \dfrac{1}{R_1R_2C_1C_2}}$$

$$H_o = \frac{K}{(1-K)(R_1/R_2 + C_2/C_1) + 1}$$

$$\omega_o = \left(\frac{1}{R_1R_2C_1C_2}\right)^{1/2}$$

$$\frac{1}{Q} = \alpha = \sqrt{\frac{R_1C_1}{R_2C_2}} + \sqrt{\frac{R_2C_2}{R_1C_1}} - \frac{1}{1-K}\left(\sqrt{\frac{R_2C_1}{R_1C_2}}\right)$$

$$\phi = \pi + \phi_{BP}$$

$$\tau = \tau_{BP}$$

The center frequency can be trimmed by varying R_1 and R_2. If this is done simultaneously so that their ratio remains constant, Q will not change. Q can be trimmed with K. Note that there is a restriction on the *minimum* value K may have for stability. Because of this restriction, the passband gain H_o will be negative. The sensitivities of the network parameters to element value changes are

$$S_{R_1}^{\omega_o} = S_{R_2}^{\omega_o} = S_{C_1}^{\omega_o} = S_{C_2}^{\omega_o} = -\frac{1}{2}$$

$$S_K^{H_o} = 1 + H_o\left(\frac{R_1}{R_2} + \frac{C_2}{C_1}\right)$$

$$S_{R_2}^{H_o} = -S_{R_1}^{H_o} = H_o\frac{1-K}{K}\frac{R_1}{R_2}$$

$$S_{C_1}^{H_o} = -S_{C_2}^{H_o} = H_o\frac{1-K}{K}\frac{C_2}{C_1}$$

$$S_K^Q = \frac{-K}{(1-K)^2}\frac{Q}{\omega_oR_1C_2}$$

$$S_{R_1}^Q = \frac{1}{2} - \frac{Q}{\omega_oR_1}\left[\frac{1}{C_1} + \frac{1}{C_2(1-K)}\right]$$

$$S_{R_2}^Q = \frac{1}{2} - \frac{Q}{\omega_oR_2C_2}$$

$$S_{C_1}^Q = \frac{-1}{2} + \frac{1}{\alpha\omega_oR_1C_1}$$

$$S_{C_2}^Q = \frac{-1}{2} + \frac{1}{\alpha\omega_oC_2}\left[\frac{1}{R_2} + \frac{1}{R_1(1-K)}\right]$$

DESIGN PROCEDURE

Given: Q, $\omega_o = 2\pi f_o$

H_o is a free parameter,

Choose: $C = C_1 = C_2$, a convenient value

Calculate: $R_1 = R_2 = \dfrac{1}{\omega_o C}$

$$K = \frac{3Q - 1}{2Q - 1}$$

Then

$$|H_o| = 3Q - 1$$

Q should be limited to about 10.

A few general comments about controlled-source realizations are in order. The Q (or α) of a circuit may be adjusted independently of ω_o by adjusting K: it is not independent of H_o, however. Networks may be cascaded without interaction occurring between them. The frequency term ω_o can be adjusted independently of α for the low-pass and high-pass cases, as discussed earlier. The characteristics of the network are sensitive to K. The circuit becomes very Q-sensitive to element value changes for high Q's.

8.3.3 Infinite-gain state-variable circuits An infinite-gain state-variable network configuration is illustrated in Fig. 8.13. This configuration makes use of operational amplifiers in the same way they would

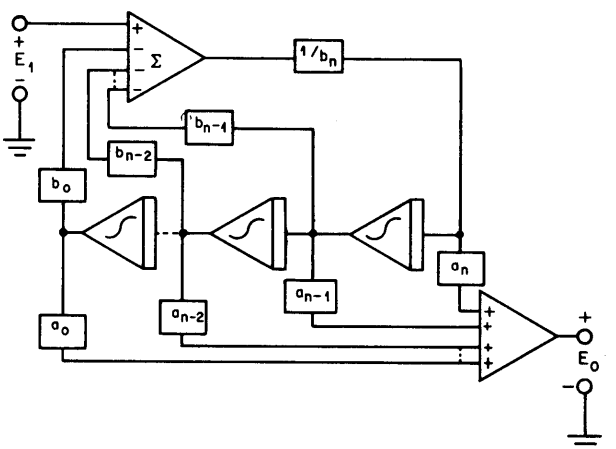

Fig. 8.13 State-variable infinite-gain network configuration.

be used in an analog computer realization of transfer functions (i.e., using integrators and summers). A second-order realization is shown in Fig. 8.14. Here the usual summing amplifier is replaced by a differentially connected operational amplifier to ease the spread in element values.

The voltage transfer function has the form

$$\frac{E_o}{E_1}(s) = \frac{a_o + a_1 s + \cdots + a_{n-1}s^{n-1} + a_n s^n}{b_o + b_1 s + \cdots + b_{n-1}s^{n-1} + b_n s_n}$$

The design procedures used in this section are simplified procedures in that $C_1 = C_2$, $R_1 = R_2$, and $R_5 = R_6$. We set $R_1 = R_2$ and $C_1 = C_2$ in order to scale adequately the output voltages of the operational amplifiers. The condition $R_5 = R_6$ further simplifies design calculations. Note that bandpass, low-pass, and high-pass realizations occur simultaneously. One merely chooses the output at a different point. In addition, one can sum the low-pass and high-pass outputs and form a pair of $j\omega$ axis zeros. The transfer functions are

$$\frac{E_{lp}}{E_1}(s) = \frac{\dfrac{1}{R_1R_2C_1C_2}\dfrac{1 + R_6/R_5}{1 + R_3/R_4}}{s^2 + s\dfrac{1}{R_1C_1}\dfrac{1 + R_6/R_5}{1 + R_4/R_3} + \dfrac{R_6}{R_5}\dfrac{1}{R_1R_2C_1C_2}}$$

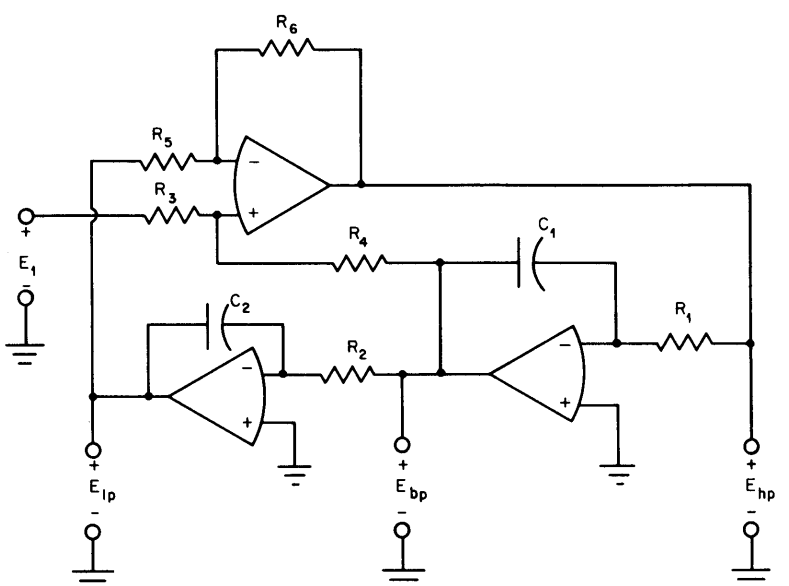

Fig. 8.14 Second-degree state-variable network.

$$\frac{E_{hp}}{E_1}(s) = \frac{s^2 \dfrac{1 + R_6/R_5}{1 + R_3/R_4}}{s^2 + s\dfrac{1}{R_1C_1}\dfrac{1 + R_6/R_5}{1 + R_4/R_3} + \dfrac{R_6}{R_5}\dfrac{1}{R_1R_2C_1C_2}}$$

$$\frac{E_{bp}}{E_1}(s) = \frac{-s\dfrac{1}{R_1C_1}\dfrac{1 + R_6/R_5}{1 + R_3/R_4}}{s^2 + s\dfrac{1}{R_1C_1}\dfrac{1 + R_6/R_5}{1 + R_4/R_3} + \dfrac{R_6}{R_5}\dfrac{1}{R_1R_2C_1C_2}}$$

The state-variable realization in general provides less Q sensitivity to element variation than a single-amplifier realization and for this reason is sometimes used for high-Q bandpass applications ($Q > 50$). Of course it requires three amplifiers, which is a disadvantage. For the low-Q low-pass and high-pass applications, it is a rather expensive circuit to use. Since some filter manufacturers use this circuit as a basic building block, the low-pass and high-pass as well as the bandpass outputs are worth some discussion.

Low Pass. The network parameters for the low-pass function are

$$H_o = \frac{1 + R_5/R_6}{1 + R_3/R_4}$$

$$\omega_o = \left(\frac{R_6}{R_5R_1C_1R_2C_2}\right)^{1/2}$$

$$\alpha = \frac{1 + R_6/R_5}{1 + R_4/R_3}\left(\frac{R_5}{R_6}\frac{R_2C_2}{R_1C_1}\right)^{1/2}$$

$$\phi = \phi_{LP}$$

$$\tau = \tau_{LP}$$

The sensitivities of the network parameters to element value changes are

$$S_{R_5}^{\omega_o} = S_{R_1}^{\omega_o} = S_{R_2}^{\omega_o} = S_{C_1}^{\omega_o} = S_{C_2}^{\omega_o} = -\frac{1}{2} = -S_{R_6}^{\omega_o}$$

$$S_{R_2}^{\alpha} = S_{C_2}^{\alpha} = \frac{1}{2} = -S_{R_1}^{\alpha} = -S_{C_1}^{\alpha}$$

$$S_{R_6}^{\alpha} = -\frac{1}{2} + \frac{R_6/R_5}{R_1C_1\alpha\omega_o(1 + R_4/R_3)} = -S_{R_5}^{\alpha}$$

$$S_{R_3}^{\alpha} = \frac{1}{1 + R_3/R_4} = -S_{R_4}^{\alpha}$$

$$S_{R_3}^{H_o} = -S_{R_4}^{H_o} = \frac{-1}{1 + R_4/R_3}$$

$$S_{R_5}^{H_o} = -S_{R_6}^{H_o} = \frac{1}{H_o}\frac{R_5/R_6}{1 + R_3/R_4}$$

DESIGN PROCEDURE

Given: α, $\omega_o = 2\pi f_o$

H_o is a free parameter.

Choose: $C = C_1 = C_2$, $R_5 = R_6 = R_3$

Calculate: $R_1 = R_2 = \dfrac{1}{\omega_o C}$

$$R_4 = \left(\frac{2}{\alpha} - 1\right) R_3$$

Then

$$H_o = 2 - \alpha$$

High Pass. The network parameters for the high-pass function are

$$H_o = \frac{1 + R_6/R_5}{1 + R_3/R_4}$$

$$\omega_o = \left(\frac{R_4}{R_5 R_1 R_2 C_1 C_2}\right)^{1/2}$$

$$\alpha = \frac{1 + R_6/R_5}{1 + R_4/R_3}\left(\frac{R_5}{R_6}\frac{R_2 C_2}{R_1 C_1}\right)^{1/2}$$

$$\phi = \phi_{HP}$$

$$\tau = \tau_{HP}$$

The sensitivities of the network parameters to element value changes are

$$S_{R_5}^{\omega_o} = S_{R_1}^{\omega_o} = S_{R_2}^{\omega_o} = S_{C_1}^{\omega_o} = S_{C_2}^{\omega_o} = -\frac{1}{2}$$

$$S_{R_6}^{\omega_o} = \frac{1}{2}$$

$$S_{R_1}^{\alpha} = S_{C_1}^{\alpha} = -\frac{1}{2}$$

$$S_{R_2}^{\alpha} = S_{C_2}^{\alpha} = \frac{1}{2}$$

$$S_{R_5}^{\alpha} = -S_{R_6}^{\alpha} = \frac{1}{2} - \frac{R_6/R_5}{R_1 C_1 \alpha \omega_o (1 + R_4/R_3)}$$

$$S_{R_3}^{\alpha} = -S_{R_4}^{\alpha} = \frac{1}{1 + R_3/R_4}$$

$$S_{R_3}^{H_o} = -S_{R_4}^{H_o} = \frac{-1}{1 + R_4/R_3}$$

$$S_{R_5}^{H_o} = -S_{R_6}^{H_o} = \frac{1}{H_o}\frac{R_6/R_5}{1 + R_3/R_4}$$

DESIGN PROCEDURE

Given: α, $\omega_o = 2\pi f_o$

H_o is a free parameter.

Again a simplified design procedure is described by setting $R_5 = R_6$.

Choose: $C_1 = C_2 = C$

$R_5 = R_6 = R_3$

Calculate: $R_1 = R_2 = \dfrac{1}{\omega_o C}$

$$R_4 = \left(\frac{2}{\alpha} - 1\right) R_3 \qquad \alpha < 2$$

Bandpass. The network parameters for the bandpass case are

$$H_o = \frac{R_4}{R_3}$$

$$\omega_o = \left(\frac{R_6}{R_5 R_1 C_1 R_2 C_2}\right)^{1/2}$$

$$Q = \frac{1}{\alpha} \frac{1 + R_4/R_3}{1 + R_6/R_5} \left(\frac{R_6}{R_5} \frac{R_1 C_1}{R_2 C_2}\right)^{1/2}$$

$$\phi = \pi + \phi_{BP}$$

$$\tau = \tau_{BP}$$

The sensitivities of the network parameters to element values change are

$$S_{R_5}^{\omega_o} = S_{R_1}^{\omega_o} = S_{R_2}^{\omega_o} = S_{C_1}^{\omega_o} = S_{C_2}^{\omega_o} = -\frac{1}{2}$$

$$S_{R_6}^{\omega_o} = \frac{1}{2}$$

$$S_{R_1}^{Q} = S_{C_1}^{Q} = +\frac{1}{2}$$

$$S_{R_2}^{Q} = S_{C_2}^{Q} = \frac{1}{2}$$

$$S_{R_6}^{Q} = S_{R_5}^{Q} = \frac{1}{2} - \frac{R_6/R_5}{R_1 C_1 \alpha_{\omega_o}(1 + R_4/R_3)}$$

$$S_{R_4}^{Q} = -S_{R_3}^{Q} = \frac{1}{1 + R_3/R_4}$$

$$S_{R_3}^{H_o} = -1 = -S_{R_4}^{H_o}$$

DESIGN PROCEDURE

Given: H_o, Q, $\omega_o = 2\pi f_o$

Again the simplified design procedure consists of setting $R_5 = R_6$.

Choose: $C_1 = C_2 = C$ $\qquad R_3 = R_5 = R_6$

$$R_1 = R_2 = \frac{1}{\omega_o C}$$
$$R_4 = R_3(2Q - 1)$$

Note that all these filters can be tuned by varying R_1 and R_2 or C_1 and C_2 simultaneously. The Q can be independently adjusted by R_4; the gain will change, however.

8.3.4 Negative immittance converter circuits A realization for an INIC[1,2] (ideal current-inversion negative immittance converter) using a differential input operational amplifier is shown in Fig. 8.15. The voltage and current relationships are

$$E_1 = E_2$$
$$I_1 = \frac{R_2}{R_1} \qquad I_2 = \frac{1}{K} I_2$$

The sensitivity of K to element value changes is $S_{R_1}^K = -S_{R_2}^K = 1$.

One reason the INIC realization might be used is its low sensitivity to element value changes as compared with other realizations. However, the INIC realization does not have a low output impedance, and isolating stages must be used if stages are to be cascaded. Since low-pass and high-pass filters have low Q's and, hence, low Q sensitivities for filters up to about six poles, we will discuss only the bandpass realization. It is probably not economical to use the INIC for low-pass and high-pass filters.

Bandpass. The INIC realization for a bandpass filter is shown in Fig. 8.16.

The voltage transfer function is

$$\frac{E_o}{E_1}(s) = \frac{-Ks/R_1C_2}{s^2 + s(1/R_1C_1 + 1/R_2C_2 - K/R_1C_2) + 1/R_1C_1R_2C_2}$$

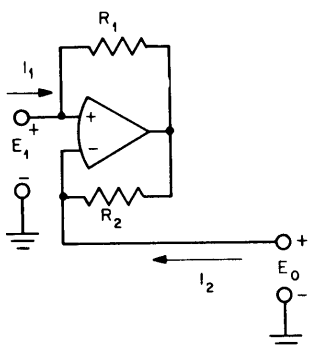

Fig. 8.15 Operational amplifier realization of the INIC.

The network parameters are

$$H_o = \frac{K}{C_2/C_1 + R_1/R_2 - K}$$

$$Q = \frac{1}{\alpha} = \frac{1}{\sqrt{R_1C_1/R_2C_2} + \sqrt{R_2C_2/R_1C_1} - K\sqrt{R_2C_1/R_1C_2}}$$

$$\omega_o = \left(\frac{1}{R_1C_1R_2C_2}\right)^{1/2}$$

$$\phi = \pi + \phi_{BP}$$

$$\tau = \tau_{BP}$$

The sensitivities of the H_o, Q, ω_o network parameters to element value changes are

$$S_K^{H_o} = 1 + H_o$$

$$S_{R_1}^{H_o} = \frac{-R_1/R_2}{C_2/C_1 + R_1/R_2 - K} = -S_{R_2}^{H_o}$$

$$S_{C_1}^{H_o} = \frac{C_2/C_1}{C_2/C_1 + R_1/R_2 - K} = -S_{C_2}^{H_o}$$

$$S_{R_1}^{Q} = \frac{Q}{\omega_o R_1}\left(\frac{1}{C_1} - \frac{K}{C_2}\right) - \frac{1}{2}$$

$$S_{R_2}^{Q} = \frac{Q}{\omega_o R_2 C_2} - \frac{1}{2}$$

$$S_{C_1}^{Q} = \frac{Q}{\omega_o R_1 C_1} - \frac{1}{2}$$

$$S_{C_2}^{Q} = \frac{Q}{\omega_o C_2}\left(\frac{1}{R_2} - \frac{K}{R_1}\right) - \frac{1}{2}$$

$$S_K^{Q} = \frac{QK}{\omega_o R_1 C_2}$$

$$S_{R_1}^{\omega_o} = S_{R_2}^{\omega_o} = S_{C_1}^{\omega_o} = S_{C_2}^{\omega_o} = -\frac{1}{2}$$

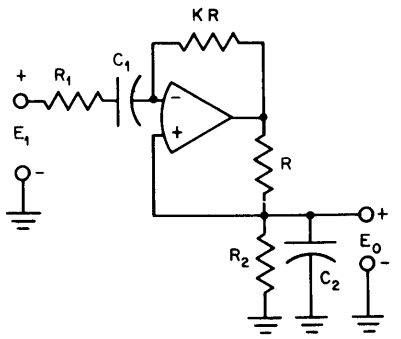

Fig. 8.16 INIC bandpass network.

DESIGN PROCEDURE

Given: Q, $\omega_o = 2\pi f_o$
Choose: $C_1 = C_2 = C$
Let $R_1 = R_2 = R'$
Then

$$K = \frac{2 - 1}{Q}$$

$$R' = \frac{1}{\omega_o C}$$

The value for R in the INIC is relatively arbitrary, but best results are obtained if it is in the 10 to 30 kΩ range.

Note that for this design procedure

$$S_K^Q = 2Q - 1 \qquad Q = \frac{1}{2 - K}$$

$$S_K^{H_o} = 2Q \qquad H_o = 2Q - 1 = \frac{K}{2 - K}$$

$$\omega_o = \frac{1}{R'C}$$

$$S_{R_2}^Q = S_{C_1}^Q = -S_{R_1}^Q = -S_{C_2}^Q = Q - \frac{1}{2}$$

$$S_{C_1}^{H_o} = S_{R_2}^{H_o} = -S_{R_1}^{H_o} = -S_{C_2}^{H_o} = Q$$

As one can see from the schematic diagram, a load at E_o will affect the circuit transfer function. Thus INIC realizations cannot be cascaded without isolating amplifiers between stages.

Note that, in general, if R_1 and R_2 are adjusted by the same percentage, the Q and gain remain constant while the center frequency varies. The same holds true for equal percentage changes in C.

Note also that adjusting K gives a Q adjustment independent of the center frequency; the gain will change, however.

8.4 Tuning Active Filter Stages

This section discusses a technique for tuning the complex-conjugate-pole-pair stage. The single-pole stage is easy to tune and will not be discussed here.

The magnitude response of a low-pass complex pole pair for several

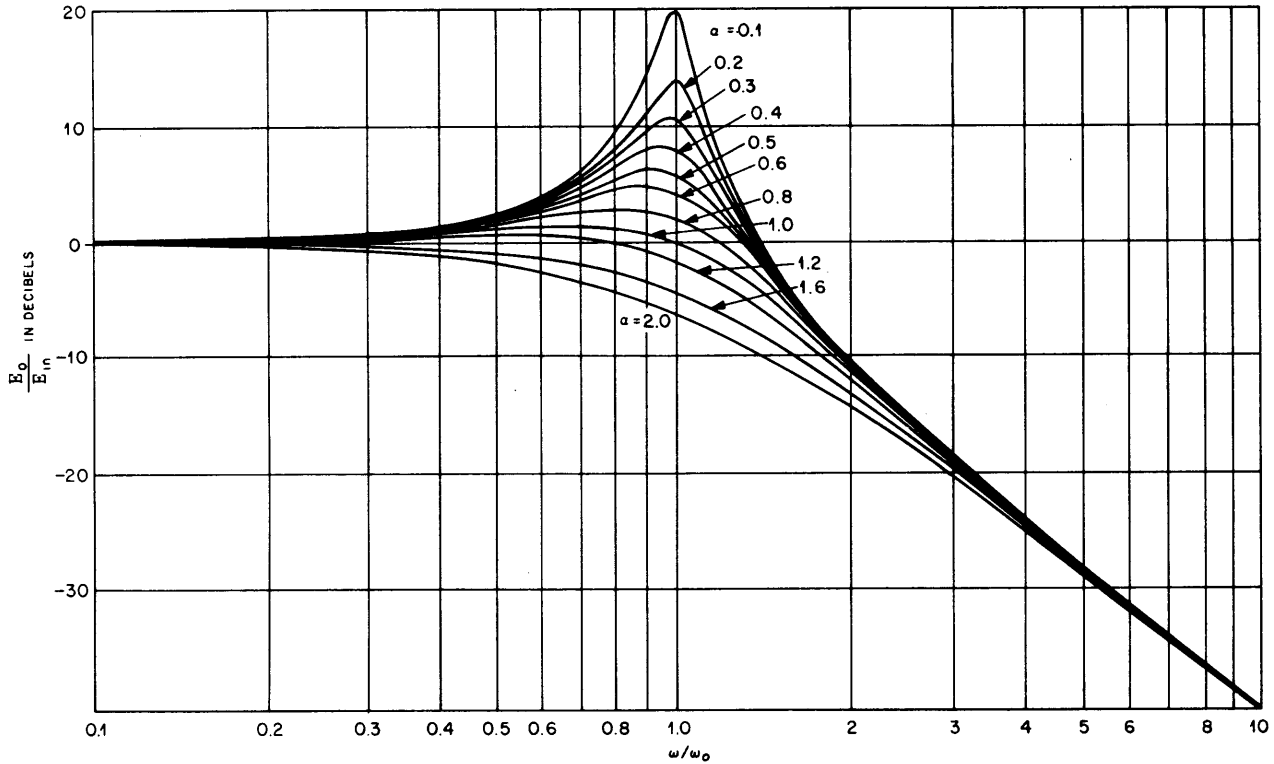

Fig. 8.17 Magnitude response of second-order low-pass filters for several values of $\alpha \leq 2$.

values of α is plotted in Fig. 8.17. Note that at $10\omega_o$ all responses have essentially the same magnitude with respect to the magnitude at direct current. Thus we can tune ω_o independently of α at this frequency. Also at some low frequency, say $0.1\omega_o$, the magnitude of the responses is essentially the same. The curves have a peak at $\omega_\alpha = \omega_o \sqrt{1 - \alpha^2/2}$ for $\alpha < \sqrt{2}$: For $\alpha \geq \sqrt{2}$ there is no peak. The frequency at which the peak occurs will be called the *alpha-peak frequency* and will be designated ω_α. This frequency will be used as a tuning frequency as will be $10\omega_o$ and $0.1\omega_o$. For those stages where $\alpha \geq \sqrt{2}$ the -3-dB frequency will be used instead of ω_α. The particular resistors or capacitors used for tuning or trimming a complex-pole-pair stage were discussed previously for each of the different circuit realizations.

The procedure for tuning the low-pass pole-pair stage is first to measure the response at $0.1\omega_o$ and then to measure the response at $10\omega_o$ and trim the element or elements necessary to adjust ω_o to give the correct response at that frequency. This may affect the response at $0.1\omega_o$, depending on the circuit realization. Now measure the response at ω_α or the -3-dB frequency, whichever is the case, and trim the α of the stage to give the correct response. This may affect the ω_o adjustment. In some realizations α can be set independently of ω_o. The response at $0.1\omega_o$ must be measured again since the α adjustment may have affected it. The gain H_o should be fairly close to the calculated value if there are no parameter effects such as those produced by capacitor leakage and dissipation factor, stray wiring capacitance or amplifier open-loop gain and frequency response limitations.

The tables at the end of this chapter (Sec. 8.7) give the ω_α or the -3-dB frequencies and the magnitude of the peak in decibels with respect to the gain at direct current.

A high-pass stage is tuned in the same manner except *that the tuning frequencies are the reciprocals of those for the low-pass stage.*

Bandpass stage tuning is, conceptually at least, simpler but practically may be more difficult because of interactions among elements. The Q is perhaps a less critical performance parameter than the center frequency. Thus it may be reasonable to adjust the center frequency only and let the Q be what it turns out to be; it will probably be close to the desired value anyway.

Those stages easiest to tune are those where the Q can be adjusted independently from ω_o. Otherwise, one has to achieve the correct values by an iterative process. The Q is adjusted at those frequencies which are -3 dB down from the peak response at ω_o. Those frequencies are

$$f_2 = \frac{f_o}{2Q} + \frac{f_o}{2Q}\sqrt{1 + 4Q^2}$$

$$f_1 = \frac{-f_o}{2Q} + \frac{f_o}{2Q}\sqrt{1 + 4Q^2}$$

where $Q = f_o/\text{bandwidth} = f_o/(f_2 - f_1)$ and $f_1 f_2 = f_o^2$.

For high Q's ($Q > 10$) one can assume arithmetic symmetry of the −3-dB frequencies about the center frequency. Then

$$f_2 = \frac{BW}{2} + f_o$$

$$f_1 = f_o - \frac{BW}{2}$$

where the bandwidth $BW = f_o/Q$.

8.5 How Amplifier Performance Affects Filter Performance

In this section we will examine how certain amplifier performance characteristics affect filter performance. These performance characteristics include dc voltage offset, bias current, voltage and current noise, and open-loop gain and are discussed in more detail in Part 1 and Appendix A.

A dc offset voltage and its drift at the *output* are often important in low-

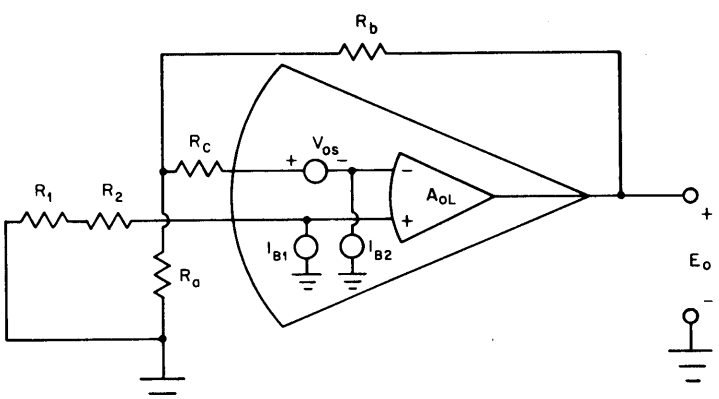

Fig. 8.18 Model for analysis of the effects of offset voltage and bias currents on a filter circuit.

pass filter applications. As an example of this type of analysis, consider the controlled-source low-pass realization shown in Fig. 8.9. At direct current the circuit becomes that of Fig. 8.18. Bias currents and the input offset voltage have been included. An additional resistor R_c has been included and can be used to equalize the current offset drift effects, as will be explained. Analysis reveals

$$E_o = \frac{1}{R_a(1 + 1/A) + R_b/A} \{I_{B2}(R_1 + R_2)(R_a + R_b) - I_{B1}[R_c(R_a + R_b) + R_aR_b] - V_{os}(R_a + R_b)]\}$$

Letting $A \rightarrow \infty$

$$E_o = I_{B2}(R_1 + R_2)K - I_{B1}(R_cK + R_b) - V_{os}K$$

where $K = 1 + R_b/\Omega_a$, the ideal closed-loop gain of the controlled-source amplifier of a controlled-source low-pass realization. R_c is used for bias current compensation. R_c may be omitted if impedances are low or if drift and offset are not critically important. Assuming the bias current I_{B1} and I_{B2} are equal, R_c should be

$$R_c = R_1 + R_2 - \frac{R_b}{K}$$

The offset and drift problems associated with other realizations are carried out in the same manner and will not be discussed here.

Output noise of active filter circuits is due to the internal voltage noise and current noise of the operational amplifier. Effects of voltage and current noise can be analyzed by using the noise models of the operational amplifier (see Appendix A). The analysis will not be carried out here since a separate chapter could easily be written on this subject. Rms noise sources are usually assumed, and this is normally the specification given in the data sheets. Low-noise amplifiers sometimes have peak-to-peak noise specified. Current noise may cause a greater noise output than voltage noise if the amplifier noise currents are flowing through large resistances, as is often the case with active filter circuits. FET operational amplifiers have very low bias current and also have low current noise. noise.

The effects of open-loop gain characteristics of operational amplifiers on the multiple-feedback bandpass circuit will now be discussed. Open-loop gain effects can be severe in the multiple-feedback circuit and especially for the bandpass realization because of the large amount of *loop gain* required for ideal performance. The open-loop gain of the operational amplifier is neither infinite nor constant for all frequencies. These prop-

erties are discussed elsewhere (Appendix A) and will not be covered here. It will be sufficient to say that for our purposes

$$A(s) = \frac{A_0}{1 + s/\omega_0}$$

where ω_0 is the -3-dB corner frequency of the operational amplifier.

The exact equation for the infinite-gain multiple-feedback realization is

$$H'(s) = \frac{-Y_1Y_3}{Y_5(Y_1 + Y_2 + Y_3 + Y_4) + Y_3Y_4 + (1/A)[Y_5(Y_1 + Y_2 + Y_3 + Y_4) + Y_3Y_4 + Y_3(Y_1 + Y_2)]}$$

If $A \rightarrow \infty$ we have

$$H(s) = \frac{-Y_1Y_3}{Y_5(Y_1 + Y_2 + Y_3 + Y_4) + Y_3Y_4}$$

Then

$$H'(s) = \frac{H(s)}{1 + [1/A(s)][1 - H(s)(1 + Y_2/Y_1)]}$$

Let us define $\beta(s) = 1/[1 - H(s)(1 + Y_2/Y_1)]$ as the *feedback ratio* (output terminal to the $-$ input), so that $A(s)\beta(s)$ is the *loop gain* of the operational amplifier. Now we can rewrite $H'(s)$ as

$$H'(s) = H(s)\left[1 - \frac{1}{1 + A(s)\beta(s)}\right]$$

Thus, the error due to finite loop gain is

$$E(s) = \frac{-H(s)}{1 + A(s)\beta(s)}$$

This equation is completely general for any infinite-gain multiple-feedback realization. Note that the phase of $E(s)$ *is not the phase error of the filter* but is the phase of the error. A plot of magnitude error ($|H(j\omega)| - |H'(j\omega)|$) and phase error [$\phi_H(j\omega) - \phi'_H(j\omega)$] for a 10-kHz bandpass filter with a gain of 10 and a Q of 20, using an amplifier with a dc gain of 100 dB and a -3-dB corner frequency of 100 Hz (unity-gain bandwidth = 10 MHz), is shown in Fig. 8.19.

Differential input impedance of the operational amplifier also affects filter performance particularly if network element impedances are large. If we include this in the analysis, we insert an admittance Y_6 from the

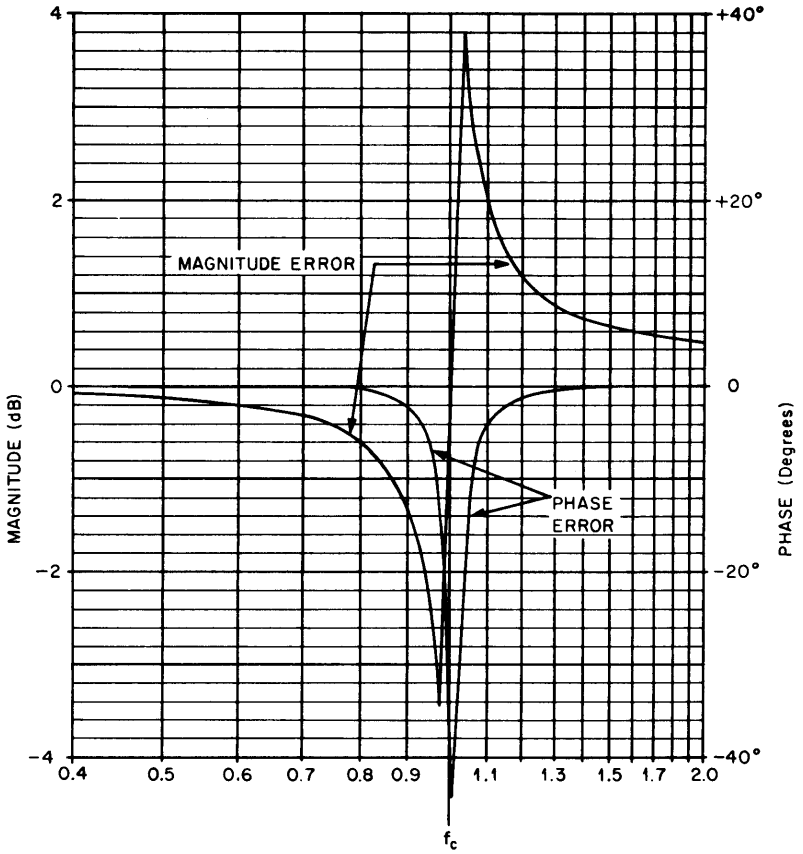

Fig. 8.19 Magnitude and phase error of a bandpass filter due to finite open-loop gain.

minus input of the amplifier to common. In this case

$$\beta(s) = \frac{1}{1 - H(s)[1 + Y_2/Y_1 + (Y_6/Y_1Y_3)(Y_1 + Y_2 + Y_3 + Y_4)]}.$$

Both open-loop gain and differential input impedance change with temperature and affect filter performance, especially at low temperatures, since they are both smaller in magnitude. The solution, of course, is to use an amplifier with more gain and higher differential input impedance or reduce circuit element impedance levels.

8.6 Circuit Elements

In this section the salient features of the resistors and capacitors most popularly used as circuit elements will be discussed.

8.6.1 Resistors Three types of resistors most often used are carbon composition, metal film, and wire-wound resistors. Carbon composition resistors have a rather poor temperature coefficient of resistance (200 to 500 ppm/°C) and are used for "room temperature" applications or in filters which may have rather loose performance tolerances with temperature, as in the low-Q stages of two- or three-pole high-pass or low-pass filters. Composition resistors are useful for trimming and padding metal film or wire-wound resistors where the relatively poor temperature coefficient causes only a small percentage change in the overall value. Carbon resistors are relatively inexpensive and are available in a wide range of values.

Bandpass filters and the high-Q stages of a high-pass or low-pass multiple-pole filter require metal film or even wire-wound resistors. Two popular temperature coefficients for metal film resistors are ± 100 ppm/°C (T0) and ± 50 ppm/°C (T2). Metal films can be purchased with a positive- or negative-only temperature coefficient and also with lower temperature coefficients (for example, ± 10 ppm/°C). The metal film resistor is probably the most commonly used resistor for filter applications and is available in a wide range of values. High-Q filters and/or filters which require especially stable parameters with temperature changes may require wire-wound resistors with temperature coefficients as low as a few parts per million per degrees centigrade. High-frequency applications will require noninductive wound resistors.

Integrated-circuit technology offers alternatives to discrete resistors: diffused resistors, thin and thick film.

Base-diffused, emitter-diffused, base pinch, and collector pinch resistors are formed simultaneously with the diffusions for the transistors of the circuit. Temperature coefficients and initial tolerances make this type of resistor marginal for active filter applications unless the filter can be designed so that its parameters depend primarily on resistance ratios.

Thin-film resistors are deposited on ceramic or glass substrates. Materials such as SnO or a SiO-Cr cermet are deposited by silk-screen methods. Others such as Nichrome, tantalum, or cermet may be deposited by evaporation or sputtering. The electrical properties of these resistors are considerably superior to those of diffused silicon resistors. An advantage of thin film over diffused or thick-film resistors is their superior long-term stability.

Thick-film resistors consist of special resistive inks screened and fired on ceramic substrates. Thick-film resistors are trimmable by means of sand blasting or laser techniques. The table following gives typical (untrimmed) parameters for several integrated circuit resistors.

Typical Parameters of Integrated-circuit Resistors

Type	Range, Ω	Temperature coefficient, ppm/°C	Tolerance, %	Matching, %
Base-diffused	100–30 k	500–2000	±10	1
Emitter-diffused	5–100	900–1500	±15	2
Base pinch	5 k–200 k	4000–7000	±50	5
Collector pinch	10 k–500 k	4000–7000	±50	10
Thin film (Ta or Ni-Cr)	30–100 k	0 ± 400	± 2	0.5
Thick film	1–10 M	0 ± 500	±20	10

8.6.2 Capacitors Capacitors present the most severe problem to active-filter designers. Capacitors which have superior characteristics such as polystyrene, Teflon, NPO ceramic, or mica are expensive and large in size. NPO ceramic is available in sizes up to about 0.05 μF for catalog items. Good-quality polystyrene capacitors can be used for the large values (10 μF) in critical applications but then are physically very large. Mica capacitors are available in values up to 0.01 μF but are larger than a Mylar or polycarbonate capacitor of the same value. Physically small ceramic capacitors such as the ceramic disk capacitors and others that have large dielectric constants (from 1,200 to 6,000) have relatively poor characteristics. Capacitance changes with temperature, frequency, voltage, and time amount to several percent. For high-Q applications these changes can make a filter stage unstable or have severe amplitude peaking or attenuation. Such filter stages are usually highly Q-sensitive to element value changes.

The merit of a capacitor dielectric from the point of view of freedom from losses is expressed in terms of the power factor of the capacitor. The *power factor* is the *sine* of the angle by which the current flowing into the capacitor fails to be 90° out of phase with the applied voltage. The *tangent* of this angle is called the *dissipation factor*. The *reciprocal* of the dissipation factor is termed the Q and is the ratio of the capacitor reactance to the equivalent series resistance.

With ordinary dielectrics, phase angle is so small that the power factor, the dissipation factor, and the reciprocal of the capacitor, Q, are, for all practical purposes, equal to each other and to the phase angle

expressed in radians. For high-quality capacitors these are practically independent of capacitance, voltage, and frequency. Although the power factor of a capacitor is determined largely by the type of dielectric it is also affected by the environment in which it operates; it tends to increase with temperature and is affected by humidity and by the absorption of moisture.

The effect of a capacitor with its power factor can be taken into account by replacing the capacitor with an ideal capacitor associated with a resistance. This resistance may be represented in series or in parallel. For lower power factors ($R_s \ll 1/\omega C)R_s$ is given by

$$\text{Series resistance} = R_s = \frac{\text{power factor}}{2\pi fC}$$

For the parallel resistance we have approximately

$$\text{Parallel resistance} = R_p = \frac{1}{2\pi fC(\text{power factor})}$$

A list of dielectric materials and representative performance features are given in Table 8.1.

Integrated-circuit capacitors are of three types; p-n junctions, MOS structures, and thin-film types. These capacitors have small values, and their values vary greatly with temperature.

The most suitable capacitor for integrated-circuit filters are those utilized in hybrid construction and are NPO ceramic chips or, for low-frequency work, tantalum capacitor chips.

TABLE 8.1 Typical Capacitor Parameters for Different Dielectrics

Dielectric	Power factor	Temperature coefficient of capacitance
Mylar	8×10^{-4}–14×10^{-4}	+250 ppm/°C 0–70°C, larger at extremes
High-quality polystrene	1×10^{-4}–2×10^{-4}	−50 to −100 ppm/°C −60 to +60°C
High-quality mica	1×10^{-4}–7×10^{-4}	0–70 ppm/°C
NPO ceramic	5×10^{-4}–20×10^{-4}	0 ± 30 ppm/°C
Polycarbonate	30×10^{-4}–50×10^{-4}	Non-monotonic Total ±1% 0–70°C, larger at extremes
Teflon	0.5×10^{-4}–1.5×10^{-4}	−250 ppm/°C −60 to 150°C

8.7 Filter Design and Tuning Tables

TABLE 8.2 Butterworth Network Parameters

Number of poles	Stage	Design		Tuning	
		α	ω_o	ω_α or -3 dB* frequency	20 log $G(\omega_\alpha)/G(o)$
2	1	1.414214	1.000000	1.000*	
3	1	a real pole	1.000000	1.000	
	2	1.000000	1.000000	0.707	1.25
4	1	1.847759	1.000000	0.719*	
	2	0.765367	1.000000	0.841	3.01
5	1	a real pole	1.000000	1.000*	
	2	1.618034	1.000000	0.859*	
	3	0.618034	1.000000	0.899	4.62
6	1	1.931852	1.000000	0.676*	
	2	1.414214	1.000000	1.000*	
	3	0.517638	1.000000	0.931	6.02
7	1	a real pole	1.000000	1.000*	
	2	1.801938	1.000000	0.745*	
	3	1.246980	1.000000	0.472	0.22
	4	0.445042	1.000000	0.949	7.25
8	1	1.961571	1.000000	0.661*	
	2	1.662939	1.000000	0.829	
	3	1.111140	1.000000	0.617	0.69
	4	0.390181	1.000000	0.961	8.34
9	1	a real pole	1.000000	1.000*	
	2	1.879385	1.000000	0.703*	
	3	1.532089	1.000000	0.917*	
	4	1.000000	1.000000	0.707	1.25
	5	0.347296	1.000000	0.969	9.32
10	1	1.985377	1.000000	0.655*	
	2	1.782013	1.000000	0.756*	
	3	1.414214	1.000000	1.000*	
	4	0.907981	1.000000	0.767	1.84
	5	0.312869	1.000000	0.975	10.20

* Butterworth filters are frequency-normalized to give -3-dB response at $\omega = 1.0$.

TABLE 8.3 Bessel Network Parameters

Number of poles	Stage	Design		Tuning	
		α	ω_o	ω_α or -3 dB* frequency	$20 \log G(\omega_\alpha)/G(o)$
2	1	1.732051	1.732051	1.362*	
3	1	a real pole	2.322185	2.322*	
	2	1.447080	2.541541	2.483*	
4	1	1.915949	3.023265	2.067*	
	2	1.241406	3.389366	1.624	0.23
5	1	a real pole	3.646738	3.647*	
	2	1.774511	3.777893	2.874*	
	3	1.091134	4.261023	2.711	0.78
6	1	1.959563	4.336026	2.872*	
	2	1.636140	4.566490	3.867*	
	3	0.977217	5.149177	3.722	1.38
7	1	a real pole	4.971785	4.972*	
	2	1.878444	5.066204	3.562*	
	3	1.513268	5.379273	5.004*	
	4	0.887896	6.049527	4.709	1.99
8	1	1.976320	5.654832	3.701*	
	2	1.786963	5.825360	4.389*	
	3	1.406761	6.210417	0.637	0.00
	4	0.815881	6.959311	5.680	2.56
9	1	a real pole	6.297005	6.297*	
	2	1.924161	6.370902	4.330*	
	3	1.696625	6.606651	5.339*	
	4	1.314727	7.056082	2.600	0.08
	5	0.756481	7.876636	6.655	3.09
10	1	1.984470	6.976066	4.540*	
	2	1.860312	7.112217	5.069*	
	3	1.611657	7.405447	6.392*	
	4	1.234887	7.913585	3.857	0.25
	5	0.706560	8.800155	7.623	3.60

* Bessel filters are frequency-normalized to unity delay $\tau(\omega) = 1$ sec at $\omega = 0$.

TABLE 8.4 Chebyshev Network Parameters, Ripple = 0.5 dB, p-p

Number of poles	Stage	Design		Tuning	
		α	ω_o	ω_α or −3 dB* frequency	20 log $G(\omega_\alpha)/G(o)$
2	1	1.157781	1.231342	0.707	0.50
3	1	a real pole	0.626456	0.626*	
	2	0.586101	1.068853	0.973	5.03
4	1	1.418218	0.597002	0.595*	
	2	0.340072	1.031270	1.001	9.50
5	1	a real pole	0.362320	0.362*	
	2	0.849037	0.690483	0.552	2.28
	3	0.220024	1.017735	1.005	13.20
6	1	1.462760	0.396229	0.383*	
	2	0.552371	0.768121	0.707	5.50
	3	0.153543	1.011446	1.005	16.30
7	1	a real pole	0.256170	0.256*	
	2	0.916126	0.503863	0.384	1.78
	3	0.388267	0.822729	0.791	8.38
	4	0.113099	1.008022	1.005	18.94
8	1	1.478033	0.296736	0.283*	
	2	0.620857	0.598874	0.538	4.58
	3	0.288544	0.861007	0.843	10.89
	4	0.086724	1.005948	1.004	21.25
9	1	a real pole	0.198405	0.198*	
	2	0.943041	0.395402	0.295	1.60
	3	0.451865	0.672711	0.637	7.13
	4	0.223313	0.888462	0.223	13.08
	5	0.068590	1.004595	1.003	23.28
10	1	1.485045	0.237232	0.225*	
	2	0.651573	0.487765	0.433	4.21
	3	0.345860	0.729251	0.707	9.35
	4	0.178208	0.908680	0.901	15.02
	5	0.055595	1.003661	1.003	25.10

* These filters are frequency-normalized so that the magnitude response at the pass-band edge passes through the lower boundary of the ripple band at $\omega = 1$.

TABLE 8.5 Chebyshev Network Parameters, Ripple = 1 dB, p-p

Number of poles	Stage	Design		Tuning	
		α	ω_o	ω_α or -3 dB* frequency	$20 \log G(\omega_\alpha)/G(o)$
2	1	1.045456	1.050005	0.707	1.00
3	1	a real pole	0.494171	0.494*	
	2	0.495609	0.997098	0.934	6.37
4	1	1.274618	0.528581	0.229	0.16
	2	0.280974	0.993230	0.973	11.1
5	1	a real pole	0.289493	0.289*	
	2	0.714903	0.655208	0.565	3.51
	3	0.179971	0.994140	0.986	14.93
6	1	1.314287	0.353139	0.130	0.08
	2	0.454955	0.746806	0.707	7.07
	3	0.124942	0.995355	0.991	18.08
7	1	a real pole	0.205414	0.205*	
	2	0.771049	0.480052	0.402	2.96
	3	0.316871	0.808366	0.789	10.09
	4	0.091754	0.996333	0.994	20.76
8	1	1.327947	0.265068	0.091	0.06
	2	0.511120	0.583832	0.544	6.12
	3	0.234407	0.850613	0.839	12.66
	4	0.070222	0.997066	0.312	2.75
9	1	a real pole	0.159330	0.159*	
	2	0.793624	0.377312	0.312	2.75
	3	0.368610	0.662240	0.639	8.82
	4	0.180942	0.880560	0.873	14.88
	5	0.055467	0.997613	0.997	25.12
10	1	1.334229	0.212136	0.070	0.05
	2	0.536341	0.476065	0.440	5.74
	3	0.280859	0.721478	0.707	11.12
	4	0.144161	0.902454	0.898	16.85
	5	0.044918	0.998027	0.998	26.95

* These filters are frequency-normalized so that the magnitude response at the pass-band edge passes through the lower boundary of the ripple band at $\omega = 1$.

TABLE 8.6 Chebyshev Network Parameters, Ripple = 2 dB, p-p

Number of poles	Stage	Design		Tuning	
		α	ω_o	ω_α or -3 dB* frequency	20 log $G(\omega_\alpha)/G(o)$
2	1	0.886015	0.907227	0.707	2.00
3	1	a real pole	0.368911	0.369*	
	2	0.391905	0.941326	0.904	8.31
4	1	1.075906	0.470711	0.305	0.85
	2	0.217681	0.963678	0.952	13.30
5	1	a real pole	0.218308	0.218*	
	2	0.563351	0.627017	0.575	5.34
	3	0.138269	0.975790	0.971	17.21
6	1	1.109145	0.316111	0.196	0.70
	2	0.351585	0.730027	0.707	9.22
	3	0.095588	0.982828	0.981	20.40
7	1	a real pole	0.155340	0.155*	
	2	0.607379	0.460853	0.416	4.75
	3	0.243009	0.797114	0.785	12.35
	4	0.070027	0.987226	0.986	23.10
8	1	1.120631	0.237699	0.145	0.65
	2	0.394841	0.571925	0.549	8.24
	3	0.179098	0.842486	0.836	14.97
	4	0.053512	0.990141	0.989	25.43
9	1	a real pole	0.120630	0.120*	
	2	0.625114	0.362670	0.325	4.53
	3	0.282589	0.654009	0.641	11.06
	4	0.137959	0.874386	0.870	17.23
	5	0.042225	0.992168	0.992	27.49
10	1	1.125921	0.190388	0.115	0.63
	2	0.414283	0.466780	0.446	7.84
	3	0.214523	0.715385	0.707	13.42
	4	0.109773	0.897590	0.895	19.20
	5	0.034169	0.993632	0.993	29.33

* These filters are frequency-normalized so that the magnitude response at the pass-band edge passes through the lower boundary of the ripple band at $\omega = 1$.

TABLE 8.7 Chebyshev Network Parameters, Ripple = 3 dB, p-p

Number of poles	Stage	Design		Tuning	
		α	ω_o	ω_α or -3 dB* frequency	$20 \log G(\omega_\alpha)/G(o)$
2	1	0.766464	0.841396	0.707	3.00
3	1	a real pole	0.298620	0.298*	
	2	0.325982	0.916064	0.891	9.85
4	1	0.928942	0.442696	0.334	1.70
	2	0.179248	0.950309	0.943	14.97
5	1	a real pole	0.177530	0.178*	
	2	0.467826	0.614010	0.579	6.84
	3	0.113407	0.967484	0.964	18.92
6	1	0.957543	0.298001	0.219	1.51
	2	0.289173	0.722369	0.707	10.87
	3	0.078247	0.977154	0.976	22.14
7	1	a real pole	0.126485	0.126*	
	2	0.504307	0.451944	0.422	6.23
	3	0.199148	0.791997	0.784	14.06
	4	0.057259	0.983099	0.982	24.85
8	1	0.967442	0.224263	0.164	1.45
	2	0.324695	0.566473	0.551	9.89
	3	0.146518	0.838794	0.834	16.71
	4	0.043725	0.987002	0.987	27.19
9	1	a real pole	0.098275	0.098*	
	2	0.519014	0.355859	0.331	6.00
	3	0.231548	0.650257	0.641	12.77
	4	0.112754	0.871584	0.869	18.97
	5	0.034486	0.989699	0.898	29.25
10	1	0.972004	0.179694	0.131	1.42
	2	0.340668	0.462521	0.449	9.48
	3	0.175474	0.712614	0.707	15.15
	4	0.089664	0.895383	0.894	20.96
	5	0.027897	0.991638	0.991	31.09

* These filters are frequency-normalized so that the magnitude response at the pass-band edge passes through the lower boundary of the ripple band at $\omega = 1$.

REFERENCES

There has been a massive amount of literature written on the subject of active filters. Extensive bibliographies are given in the two references listed below.

1. L. P. Huelsman, *Theory and Design of Active RC Circuits*, McGraw-Hill Book Company, New York, 1968.
2. L. P. Huelsman, *Active Filters: Lumped, Distributed, Integrated, Digital, and Parametric*, McGraw-Hill Book Company, New York, 1970.