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High-resolution Signal Acquisition Module Recording 18-Lead ECG for Person Authentication

Tatyana Dimitrova Neycheva, Todor Venkov Stoyanov, Vessela Tzvetanova Krasteva, Ivo Tsvetanov Iliev, Serafim Dimitrov Tabakov, Valentin Viktorovich Tsibulko and Irena Ilieva Jekova

Abstract – **This paper presents a high-resolution 16-channel ECG acquisition module with 24-bit amplitude resolution and sampling rate of 2kHz. The module is applied for collection of ECG database for the aims of development and testing of methods for person authentication via ECG. Such database could support the definition of optimal number of ECG leads and the optimal feature set and would facilitate the decision about the ECG applicability as a person biometric characteristic in different environments.**

Keywords – **ECG device, 24-bit ADC, 18-lead ECG, biometrics, person verification, identification**

I. Introduction

Nowadays, the reliability of the automatic person verification/identification is very important, considering the necessity of high security level in cases of financial transactions; access control for buildings, rooms and information; traveling, etc. Due to the technological development of compact sensors for acquisition of biological signals and the progress in biomedical signal processing for diagnostic purposes in the last decade, the idea for application of signals generated in the human's body for person authentication gains support. The analysis of the electrocardiogram (ECG) as a biometric tool was started about a decade ago, incorporating two general approaches: (i) methods, using measurements after detection of fiducial points; (ii) methods, analyzing the overall morphology of the ECG waveform. All methods rely on detailed zoom of specific temporal and amplitude ECG characteristics, and therefore, the more precisely the ECG is acquired (high sampling rate and amplitude resolution), the more reliable person verification/ identification can be supported.

Single lead ECG for person identification is acquired from palms [1] and fingers [2]. Although the described ECG devices implicitly assure comfort for the tested person, according to some authors, the reduction of the number of analyzed ECG leads limits the accuracy [3]. Others, however, report reliable identification accuracy of 94.3-95% with limited number of ECG leads [1,2]. Considering this uncertainty and the extended application of person authentication not only in social environment but also in medical setting, assisting and securing the collection of personal medical information, there is a need for high-resolution multi-channel ECG acquisition module, which could be used for collection of ECG data with redundancy. Such ECG database could be further analyzed in order to extract valuable information about the most reliable leads and features for person authentication.

This paper presents a 24-bit 16-channel ECG acquisition module, which is applied for collection of 18-lead ECG database for the aims of a detailed framework of the person verification/identification task. Such database could support the definition of the optimal number of ECG leads and feature set, and would facilitate the decision about the ECG applicability as a personal biometric characteristic in different environments.

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II. Hardware Concept

The presented ECG module provides synchronous acquisition of 16 ECG channels and one respiration channel via impedance measurement in lead I, with the capability for real-time data transfer to PC. The ECG is sampled at 2kHz, 24-bit amplitude resolution over an input range of ±400 mV (about 0.05μV/LSB).

The block diagram (Fig. 1) is including:

1) Two 8-channel Texas Instruments ADS1298R demonstration boards (ADC1, ADC2), each one embedding complete ECG Front-End module based on 24-bit, delta-sigma (ΔΣ) analog-to-digital converter (ADC) with a built-in programmable gain amplifier (PGA), internal reference, and an onboard oscillator.
2) Custom interface board providing PC connection of the ECG module. The board is based on the microcontroller Cortex STM32F103C8 and the USB to serial UART interface circuit FT232RL. The FT232RL data sheet claims operating rate at up to 3Mbps that guarantees the correct transfer of 16-channel, 24-bit data, sampled at 2kHz.

The power supply of the designed ECG acquisition module is 5V, provided via the available USB interface. The chips STM32F103C8 and FT232RL are powered directly from PC, while ADC1 and ADC2 are electrically isolated from the apart hardware according to IEC60601 standard, so that the ECG acquisition module complies with the requirements for patient safety. The DC-DC converter AM1D, rated to 6kV DC isolation, is used to produce an isolated power supply. The digital signals are

isolated by four-channel ADUM2401 magnetic isolators, rated for 5400V RMS.

A PC application under Windows is developed for data communication with the ECG acquisition module via USB. Three modes of operation are supported:

1) 12-lead standard ECG acquired via 10-electrode cable connected to 'patient cable 1';
2) 12-lead standard + 4-lead ECG acquired via 14-electrode cable connected to 'patient cable 1';
3) 12-lead standard + 7-lead ECG acquired via two 10-electrode cables connected to 'patient cable 1' and '2' (two inputs of 'patient cable 2' are not used).

Mode (1) uses only ADC1 inputs, while modes (2) and (3) use both ADC1 and ADC2 inputs. The synchronous operation is managed by ADC1, which generates the master clock (EXT_CLK) for ADC2 and provides common Wilson Central Terminal (WCT) and common potential for the driven right leg (ELEC_RL = ELEC_RA + ELEC_LA + ELEC_LL) for both ADC boards.

All data are transferred to the PC in real time. This allows user-friendly visualization and recording of multi-lead patient ECG in the experimental environment.

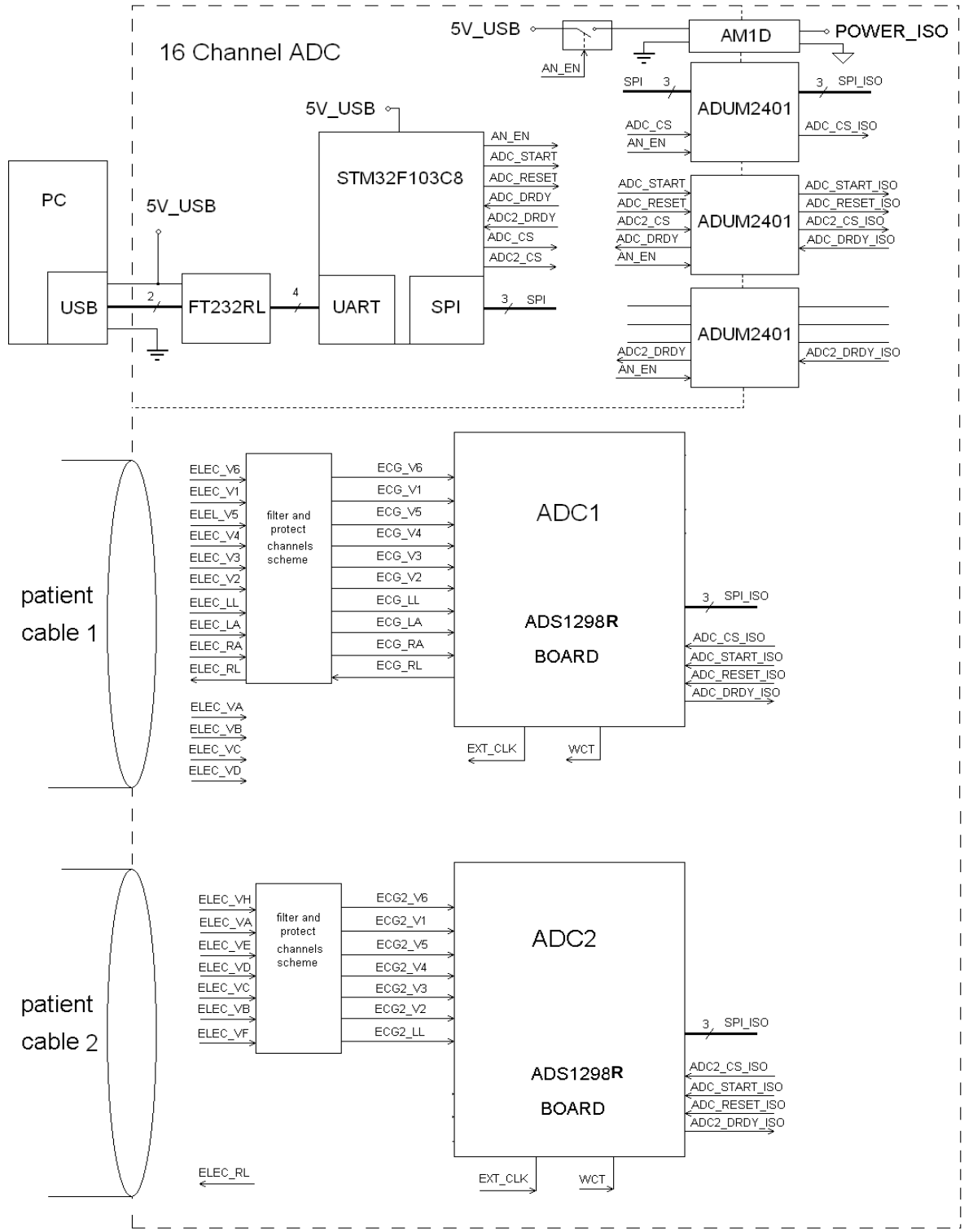

Fig. 1. Block diagram of the 16-channel 24-bit ECG acquisition module.

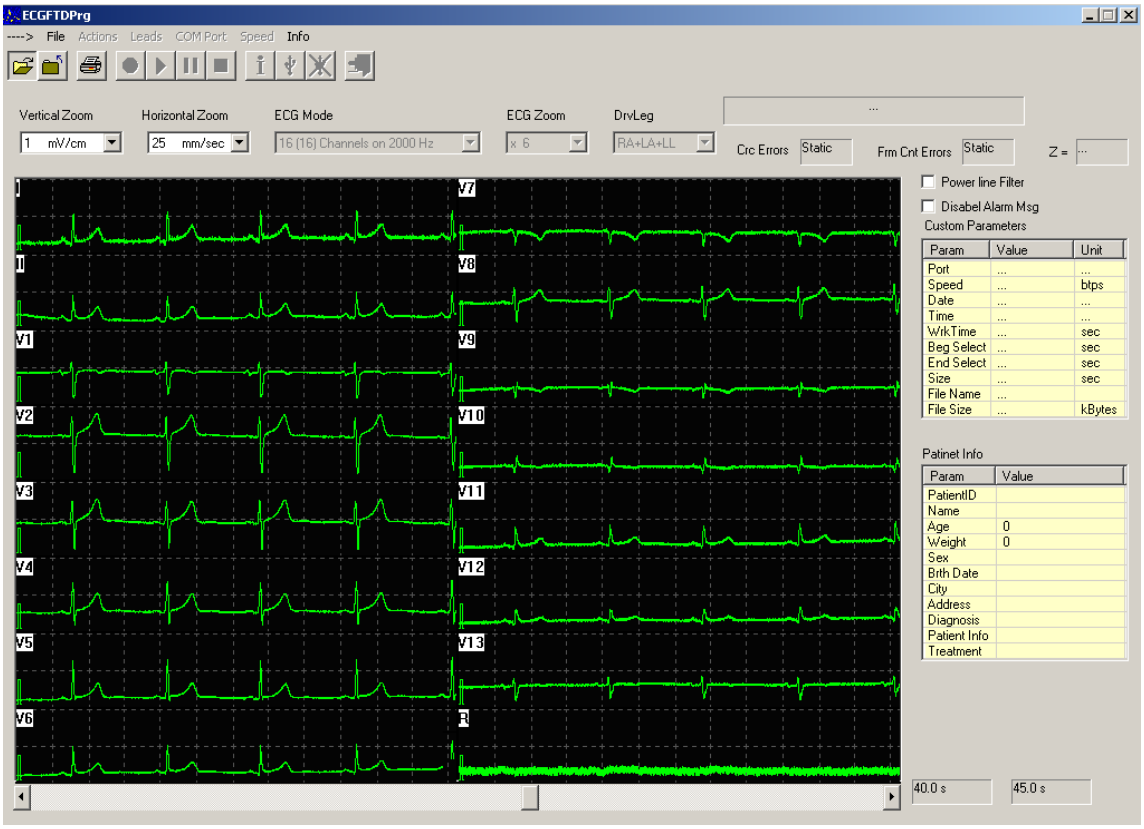

Fig. 2. Main window of the PC application for management of the real-time signal acquisition, recording and visualization of multi-lead ECG (I, II, V1-V6 (standard), V7-V13 (additional)) and one respiration channel (R).

II. PC Application

The PC application developed in Visual C++ 6.0 controls the ECG acquisition and visualization in real time, as well as the recording of signal data on the hard disk. The main window of the application (Fig. 2) contains user control tools for selection of:

- *ECG Mode* – possible acquisition of 12, 16 or 19 ECG leads;
- *Vertical Zoom* – three standard values for the possible vertical zoom: 0.5 mV/cm, 1 mV/cm, 2 mV/cm
- *Horizontal Zoom* – three standard values for the possible horizontal zoom: 12.5 mm/s, 25 mm/s, 50 mm/s;
- *ECG Zoom* – programmable hardware internal amplification. The default value is 6. Other possible values are 1, 2, 3, 4, 8, 12.

The following controls are available on the GUI toolbar:

Open a file saved on the hard disk
Close the opened file
Start saving received data to temporary memory buffer
Start data acquisition
Pause/Start the ECG curves drawing
Stop acquisition data and save the data from the temporary memory buffer to the hard disk
Show the patient's info dialog
Connect application to the device
Disconnect application from the device
Close the application

III. ECG Data for Person Authentication

The designed 16-channel, 24-bit ECG module (Fig. 3) is used for collection of ECG database dedicated to fundamental research in the area of ECG biometrics. The potential for person authentication via ECG should be studied in a multi-lead, high-resolution scale, with acquisition of the following 18 ECG leads (Fig. 4):

- Six standard peripheral leads acquired via 3 electrodes on the limbs: left arm (LA), right arm (RA), left leg (LL) (Fig. 4a);
- Six standard precordial leads (V1, V2, V3, V4, V5, V6) and one right precordial lead (V3R) acquired via 7 chest electrodes (Fig. 4b);
- Two posterior leads (V7, V8) acquired via 2 electrodes on the back (Fig. 4c);
- Frank bipolar leads (X,Y,Z) acquired via V6 and LL plus 4 additional electrodes I, E, H, M (Fig. 4b,c): X = V6 – I, Y = LL – H, Z = M – E.

Fig.3. ECG acquisition module connected to PC

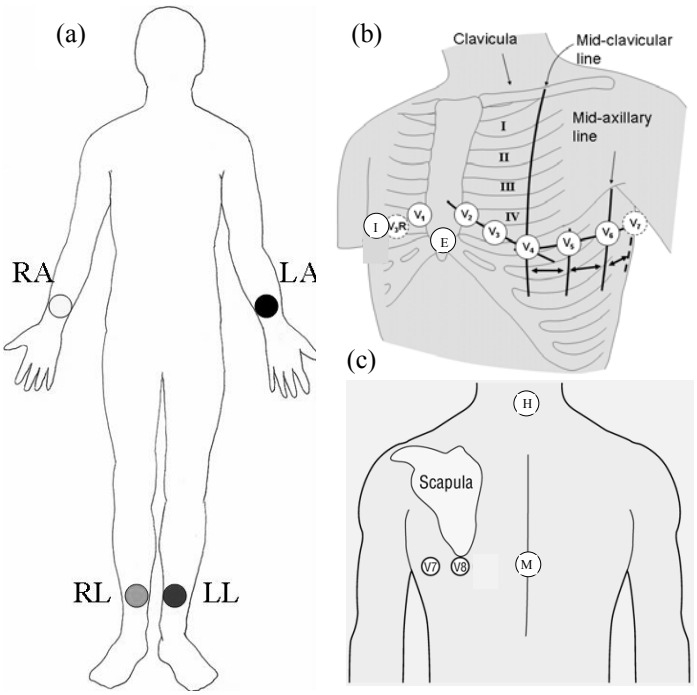

Fig. 4. ECG electrodes placement for acquisition of 18-lead ECG: 12 standard leads via RA, LA, LL, V1, V2, V3, V4, V5, V6; 1 right chest lead via V_3R; 2 posterior leads via V7, V8; 3 Frank bipolar leads (X,Y,Z) via I, E, M, H electrodes.

Figures 5 and 6 illustrate an example of 5s 18-lead ECG and 1 respiration channel acquired and recorded with the designed high-resolution ECG acquisition system. During recording, no filtering is applied to leads, keeping small details of the original ECG morphology unchanged by the filter bandwidth that might be of interest in an offline study for person authentication.

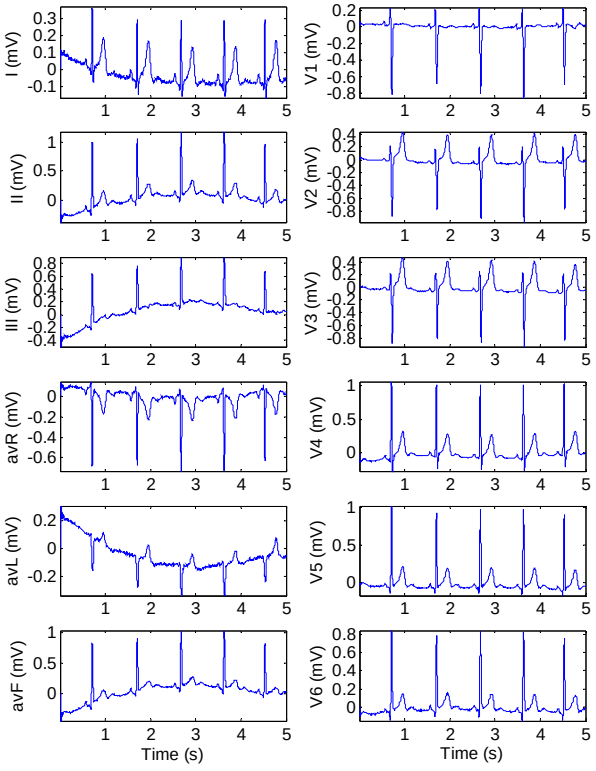

Fig. 5. Example of standard 12-lead ECG, acquired via the designed ECG module.

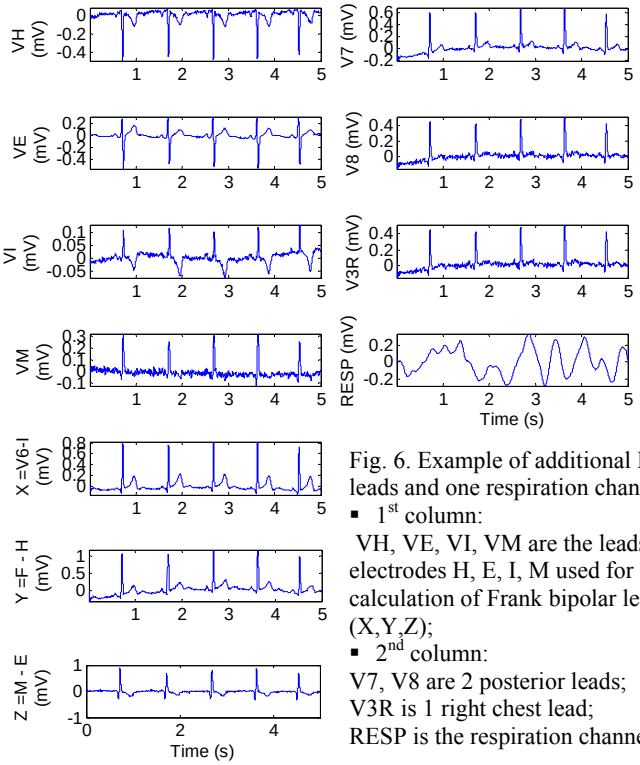

Fig. 6. Example of additional ECG leads and one respiration channel:
- 1st column:
VH, VE, VI, VM are the leads of electrodes H, E, I, M used for calculation of Frank bipolar leads (X,Y,Z);
- 2nd column:
V7, V8 are 2 posterior leads;
V3R is 1 right chest lead;
RESP is the respiration channel.

V. Discussion and Conclusions

This paper presents a 16-channel, 24-bit ECG acquisition module and a PC application for real-time data management, applied for recording of a large database for the aims of person authentication. The conditions required for collection of such database are:
- Recording of 18-lead ECG provides the opportunity to derive general conclusions about the potential of any ECG lead and the set of the most reliable leads as a biometric measure for person verification/identification;
- Recording of high-resolution ECG, sampled at 2kHz, 0.05μV/LSB provides the opportunity to study details of any temporal and amplitude relations that might help understanding of inter and intra subject differences.
- Recording of two ECG recordings per person: ECG(t1) and ECG(t2), where t2≥t1+6 months provides long-term tracking of ECG intra-individual morphology variation.

V. Acknowledgements

This study was supported by the Bulgarian Scientific Research Fund, grant T02/11.

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Applications of e-Health Standards in Personalized Healthcare Systems

Galidiya Ivanova Petrova

Abstract – **The paper presents an overview of e-Health standards used for implementation of Personal Healthcare systems (PHSs). Interoperability issues on the technical level are discussed addressing data formats and transmission protocols standardization. At the end, some recommendations for application of specific standards for development of PHSs are given. The directions for future development of e-Health standards are discussed.**

Keywords – **Personal Healthcare Systems, data exchange, e-Health standards, interoperability.**

I. INTRODUCTION

Recent advances in Information and Communication Technologies (ICT) and more specifically in wireless communication technologies and mobile computing have driven new directions in the development of e-Health sector. New and emerging concepts like mobile health (m-Health) and Personal Health Systems (PHSs) are expected to revolutionize the way the healthcare services are delivered. They are opening the way for new healthcare and wellness applications by giving the individual person a more central role in its treatment and prevention process, and by giving healthcare professionals an access to data, collected under natural activities and environment [1, 2].

One of the critical point for providing timely care for the home monitored patients is the integration of the information systems for remote health status monitoring to the hospital and clinical information systems. The important role in the integration process play the healthcare standards employed.

The goal of this paper is to provide an overview of e-Health standards applicable for implementation of PHSs and to trace future directions for development of these systems.

II. BACKGROUND

A. Personal Healthcare Systems - use case scenario

The PHSs are concerned with the individualization of treatment, prevention and well being procedures available through the healthcare system. The patient is placed in the center of the health delivery process. The main goal of PHSs is to bring continuity of care at all levels of healthcare delivery through applications for remote monitoring and remote management, spanning from location, to ambiance, and time. This continuity of care is a prerequisite for the delivery of preventive, personalized and citizen-centered health care [1]. In implementation of PHSs and Tele-heath monitoring systems employing open architecture is widely accepted approach. On Fig. 1 the basic three-tier architecture of a PHS is presented [2].

The first tier is represented by the wireless body sensor network (WBSN) which comprises sensors attached to the patient body for measurement of vital physiological parameters, and sensors in the close proximity of the patient for measurement of ambient parameters. The second tier includes Personal monitor (server) or Hub playing the role of Home Gateway. It coordinates the sensor network, derives the values of measured parameters, performs the raw data processing and sends data to the third tier. The third tier is represented by the medical servers of remote medical centers, healthcare providers, caregivers, emergency, etc. where the data are received, processed, analyzed and stored.

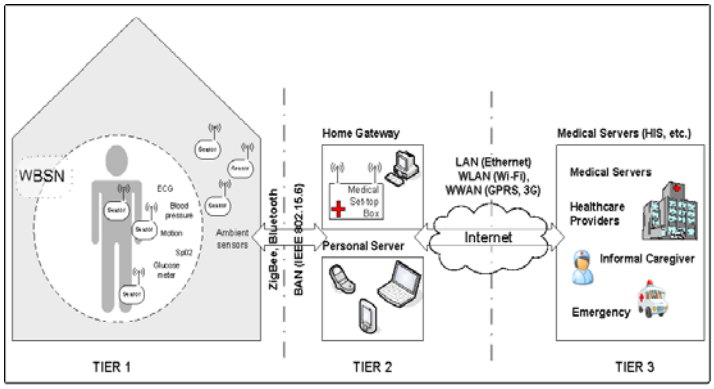

Fig.1. Basic architecture of PHS

B. Wireless Body Sensor Networks

WBSN consists of a network of miniaturized, low cost, and wireless wearable or implantable bio-sensors and actuators that are interconnected to provide continuous monitoring of the patient's physiological and contextual parameters (e.g. ECG, EEG, Heart and respiration rates, blood pressure, oxygen saturation (SpO2), body temperature, glucose level, spatial location, etc.) [2]. Every node of WBSN performs signal pre-processing including detection, amplification, filtration and discretization. In some cases, it is also possible to perform digital signal processing for analyzing the data in order to detect abnormal disease situations and creating alerts.

It is well known [3, 4] that for realization of wireless communication in WBSN the use of standard communication technologies is preferred. This approach enables compatibility on physical layer between bio-sensors of different producers to be achieved. According to [3, 4, 5] the most frequently used standard wireless technologies for implementation in WBSN are: the group of wireless local networks (WLAN – IEEE 802.11a/b/g), the group of wireless personal networks (WPAN)

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represented by IEEE 802.15.1 (Bluetooth), IEEE 802.15.3 (UWB), IEEE 802.15.4 (ZigBee), and the group of mobile cell communications (GSM, GPRS, UMTS, 3G, 4G). The choice of appropriate standard is based on the parameters specific for the particular application, while the optimum working of this application is dependant on the correct configuration of the wireless network.

C. Body Sensor Network Gateway

The BSN gateway or Personal server fulfils several main functions in the PHS. A part of these functions comprises the interfaces to the WBSN tier, the tier of medical servers and the local user interface [6]. The other part of gateway functions includes initial data processing, filtration and normalization of the values of measured physiological and ambient parameters. Finally, the gateway is also responsible for converting the format of data to be exchanged with the medical servers. For realization of the BSN gateways usually smart phones or embedded systems with additional functionalities are used [2].

Taking into consideration the interface with the medical servers, the gateway is responsible for local data storage when there is no connectivity to Internet. It is also responsible for building of reliable channel for transmission of locally stored or received in real-time data to the remote medical servers.

D. Healthcare Web Portals (medical servers)

The third tier of PHS (medical servers) is located in the respective medical center, which provides health services accessible through Internet. The main functions of the third tier include: maintaining DataBase with the Electronic Health Records (EHRs) of the associated patients and corresponding Personal Health Records (PHRs); providing local and remote access to the DataBase for reading and/or writing data for different groups of users as general practitioners, medical doctors, Clinical and Laboratory information systems (CIS and LIS), and patients themselves; as well as providing access to some additional services offered by the respective medical center. Generally, the data exchange between the PHSs and EHRs systems of CIS and Hospital information systems (HIS) for the associated patients is realized on this tier of PHS [5].

Nowadays [7], web-technologies and in particular web-services are the most preferable on the middleware level technologies for development of PHSs. Several developments exist [8] which ensure compatibility between the Service-oriented Architecture (SoA) standards and the requirements of PHS. Basically, they use computer languages for description of the web-services and the interaction between them. Typical characteristics of SoA are the untied interaction and dynamic re-configuration based on XML format of the massages.

It is worth to notice that from one side, the PHSs give new possibilities and have advantages for realization of e-Health systems and services. However, from the other side there are a number of unsolved problems and challenges related to the implementation of separate tiers and information interaction between them in the open architecture of PHSs.

The main problems which have to be solved are:

- The large number of wireless bio-sensors from different producers using variety of protocols for data exchange and various message formats;
- Frequently in the process of generation of Personal Health Records the data are not presented in the same standard as in EHRs which do not allow direct data exchange with EHRs systems of clinical and hospital information systems;
- Often for the sake of convenience, in realization of the PHSs it is preferable to generate unique web application protocols based on HTTP XML which are not directly compatible with the standards regulating the presentation and exchange of medical data in development of e-Health information systems.

In conclusion, it is worth to notice the necessity to integrate Personal Healthcare Systems to Clinical and Hospital information systems employing approved standards for PHRs and EHRs [9]. From one side, it is necessary to make compatible data exchange protocols and messages between the separate components of these systems. From the other side, it is necessary to regulate the health services provided, especially when the patient moves from one place to other.

These issues are highly topical for Bulgaria, in view of the fact that clinical paths for remote monitoring of the patients in hospitals or similar activities for the general practitioners and medical centers still are not envisaged.

III. PHS EXISTING STANDARDS

According to [9] "Interoperability in e-Health systems is important for delivering quality healthcare and reducing healthcare costs. Some of the important use cases include: coordinating the care of chronic patients by enabling the co-operation of many different e-Health systems such as Electronic Health Record Systems, Personal Health Record Systems and wireless medical sensor devices; enabling secondary use of EHRs for clinical research; being able to share life long EHRs among different healthcare providers".

On Figure 2 [10] the interoperability framework of PHS and other systems and structures within the e-Health domain is shown.

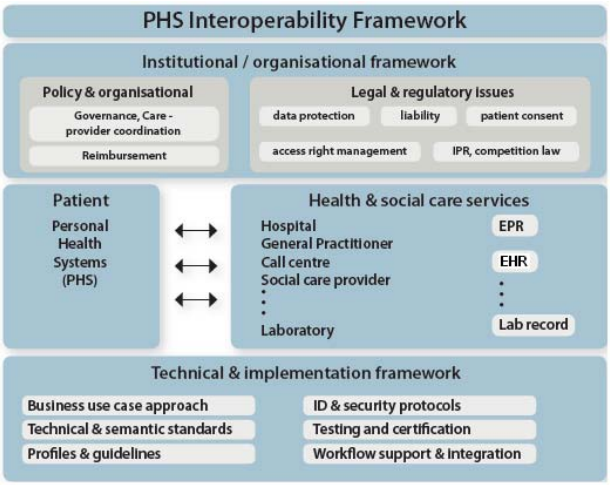

Fig.2. Interoperability framework of PHS with other e-Health systems

The characteristics of PHS are similar with these of heterogeneous distributed systems. The main tasks in their development are to achieve compatibility between separate components as well as to assure universal and smooth exchange of information between tiers in the system architecture. These issues trace the path and put the emphasis on the development of common standards for PHS.

In the last decade several projects have been lunched for development of e-Health standards with the idea to allow much better compatibility between PHSs, PHRs systems and EHRs systems. The efforts and activities ware directed to the following three major areas:

1. Applying PHS devices for measurement of vital data and personal activities;
2. Collecting and converting these data via a data hub which may be in the home or mobile;
3. Analyzing the data provided and acting upon the results by health service providers.

One of these research projects funded by the EC in 7th Framework Programme is 'SmartPersonalHealth' [11]. Main partners in this project are: Continua Health Alliance (CHA), Integrating the Healthcare Enterprise (IHE) and European Telecommunications Standards Institute (ETSI) [10, 11]. The work was based on the basic scenario in PHSs and the patient data are transferred from personal devices through a data hub (home gateway) to health services systems, e.g. electronic patient record, electronic medical record, a hospital information system or a General Practitioner patient system as illustrated on Fig. 3[10].

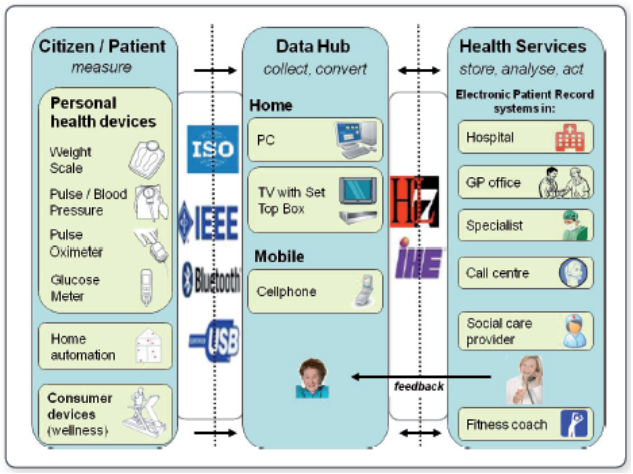

Fig. 3. Examples of personal devices and data exchange in PHS-based healthcare services

In the development of the project the e-Health standards HL7, IEEE 11073 and IHE are used [11].

- HL7 (Health Level Seven) defines a standard for exchange of medical, financial and administrative information between HIS, clinical laboratories, enterprise and pharmacy systems;
- IEEE 11073 (Medical Information Bus - MIB) standardize the physical and transport characteristics of communication between medical devices for providing of plug and play interoperability at the point of care. It facilitates the exchange of medical data acquired by patient connected medical devices.
- IHE (Integrating the Healthcare Enterprise) within the scope of the "Device Enterprise Communication (DEC)" Profile [3], provided a mapping of the IEEE 11073 Domain Information Model to HL7 version 2.5 Message format.

In order to standardized the process of measurement and transmitting data from personal health devices to the Data hub the standard IEEE 11073 is used with additional specifications of protocols for every bio-sensor. On Figure 4 [11] the Continua Health Alliance device connectivity standards are presented.

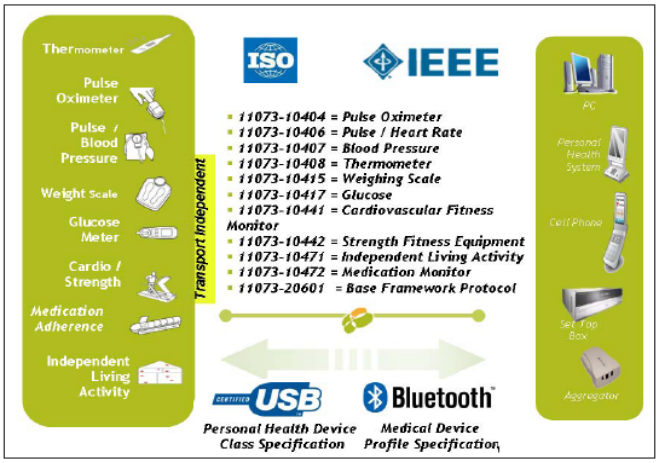

Fig. 4. Continua device connectivity standards

The lower level protocol standards for communication are constrained to USB and Bluetooth. In order to optimize the exchange of information in the personal area network interface, the ISO/IEEE 11073-20601 standard version 1.0 Personal Health Device Communication is selected. In this way the interoperability between the devices and Data hub (gateway) is achieved.

On the contrary, it is difficult to achieve the interoperability between Data hub and health services provider because the producers of PHSs and personal health devices usually are not providers of PHRs and EHRs systems [10, 11]. To facilitate this, a messaging standard supported by IHE that certify electronic health record systems was chosen (IHE's Cross-Enterprise Document Reliable Interchange (XDR) profile). To facilitate the accurate transfer of both coded patient results from personal health devices and textual summary results from patient caregivers, the HL7 Personal Healthcare Monitoring Report document format standard was chosen. This standard is close to the widely used Continuity of Care Document (CCD) standard with specific changes to accommodate device data monitoring.

General conclusion is drawn that IHE/Continua standards, from a technical point of view, provide solid and proven tools to build a modern PHS and PHRs system [5].

The main disadvantages of the device connectivity standards, developed in the frame of SmartPersonalHealth project and Continua Health Alliance, are that they are not free and comprise only USB and wireless interfaces Bluetooth and ZigBee [10,11]. Thus the application domain is restricted mainly to health monitoring in hospitals and hospices. As well, the new standard IEEE 802.15.6 directed to wireless body area networks (WBAN) divided into medical and non-medical applications [12] is not covered.

Alternative approach is employed in development of the Tele-health monitoring system for Ambient Assistant Leaving [13]. In this system using Bluetooth wireless interface the data from bio-medical sensors are send to Smart phone, which play the role of Home gateway. The Smart phone performs initial data processing, filtration and normalization of measured physiological parameters, and finally converts the data in XML format. As it is shown on Fig. 5 [13] after local storage the data are transmitted to the server of Web-based Tele-health service system which is responsible for receiving data uploaded by measurement devices, re-processing and saving the data to the corresponding DataBase location. For health management and tele-care services, the server enables the users, the families, and the healthcare providing unit access to the users' physiological conditions at any time through the Internet using personal computers or smart devices.

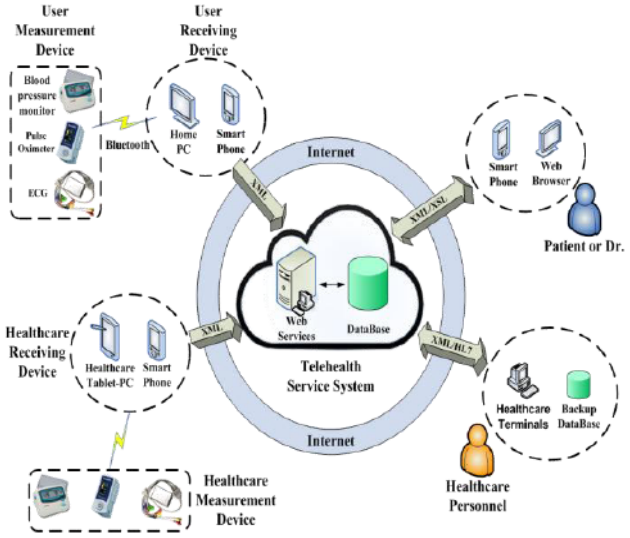

Fig. 5. Tele-health XML/HL7 systems

EHRs are transformed into XML format by obtaining the required information from the Tele-health Service DataBase, and the information is converted into a uniform standard XML data through XML/XSL. The output of the standard information formats can be divided into two types: EHRs of the HL7 format, and XML format defined by HIS. As shown on Fig. 6, the self-defined XML format is used for data transmission and information exchange.

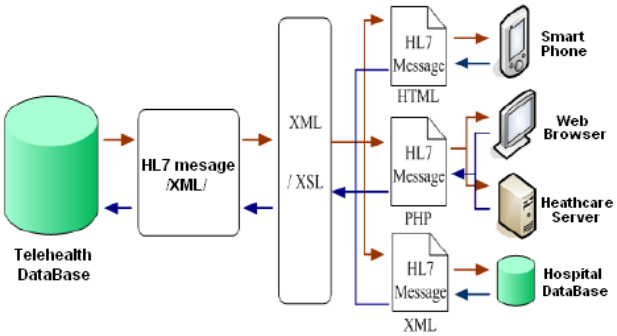

Fig. 6. The transmission and transformation of information

In this way the information is converted into a format that conforms to the HL7 standard via XML, and therefore can exchange messages with various independent hospital information systems.

Similar approach is employed in development of Home Healthcare Monitoring System (HHMS) [14]. In this project the PHS comprises from the one side a Home Healthcare Monitoring System which includes WBAN and home gateway. HHMS supports patients' daily healthcare and their quality of life by collecting useful medical and daily routine information. From the other side is the tier of medical servers represented by Hospital Management Information System (HMIS). HMISs are compliant to different healthcare standards therefore require data in standardized format. In order to solve the problem with the interoperability on the data level for information exchange among HHMS and different HMISs a mediator represented by Interoperability Mediation System (IMS) is proposed [14]. The Interoperability Mediation System behaves as a bridge between HHMS and HMIS and its working model is presented on Fig. 7. HHMS collects information in raw sensory format and stores it in XML format while HMIS follows standard structure of information based on its compliancy with the two healthcare standards - Health Level Seven Clinical Document Architecture (HL7 CDA) and openEHR. The HL7 CDA is a document markup standard that specifies the structure and semantics of "clinical documents" for the purpose of exchange, while openEHR is an open standard that describes the management and storage, retrieval and exchange of health data in EHRs. Both standards concern presentation of information in EHRs systems with specific protocols and data formats. By interoperability service of IMS sensors information in XML form is converted to HL7 CDA and openEHR instances and afterwards communicated to HMISs.

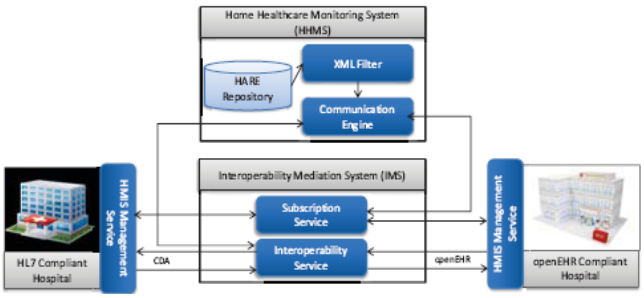

Fig. 7. IMS Working Model [14].

In this overview of the projects addressing e-Health standards used for implementation of Personal Healthcare Systems two main approaches for achieving compatibility between components and standards, and interoperability on the technical level of data formats and transmission protocols are presented. The first approach deals with the development of specifications of standards and protocols addressing WBAN tier from one side, and the interaction and information exchange between WBSN and second tier (Home gateway) from the other side. The final goal is to have common standards for producers and users of bio-medical sensors and devices as well standardization of information in PHS and EHRs systems. In this case the proposed specifications and standards by Continua Health

Alliance for compatibility between the first two tiers and the medical servers tier are the most complete.

The second approach does not deal with the standardization in the first two tiers of PHS. It allows the development of heterogeneous WBSNs employing different protocols and messages' formats. The compatibility with the standards from the medical servers tier is achieved by means of information transformation through XML. This allows successful realization of data exchange between CIS, HIS and EHRs systems which use different standards for presentation of patient data.

Both approaches employed in the described e-Health projects demonstrate practically achievable compatibility allowing development of efficient PHSs. At the moment, the described approaches for compatibility and standardization of data exchange cover only the area of various e-Health systems which could be pointed is a common drawback. Still, there are no interconnections and integrations with developments as Smart House and Smart City, and developments in the new areas of Internet-based systems for monitoring and intelligent sensor networks as Internet of Things (IoT) and Machine-to-Machine communications (M2M) [15, 16].

IV. Conclusion and Future Work

In this paper the employed approaches for integration of e-Health standards in implementation of Personal Healthcare Systems are discussed. They trace the directions for future research activities in this area.

In general, the realization of PHS and PHR systems in accordance to international standards should be preferred. However, at this point in time the examples show that projects usually need to fulfill some individual local requirements on country or organizational level.

The progress in development of standards in the area of PHSs compatible with the common standards for EHRs, CIS and HIS is the crucial point for complete integration of various e-Health systems.

The new concepts for development of Internet-based systems for monitoring and distributed automation based on IoT and M2M from one side, and integrated systems as Smart House and Smart City from the other, need the development of new complementary standards and approaches comprising and integrating the e-Health domain with them.

Acknowledgments

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Analysis of QRS Patterns in 15-Lead ECG for Person Verification

Vessela Tzvetanova Krasteva, Irena Ilieva Jekova and Roger Abächerli

Abstract – **This paper presents a method for evaluation of similarity and difference scores of QRS patterns in 15-lead ECG for the aims of person verification. An ECG database with 316 healthy subjects, including two records per subject taken >1year apart is used to simulate the real case scenario. Discriminant analysis estimates the best specificity/sensitivity for limb+chest leads (92.9/92.1%), lower for limb leads (92.1/89.6%), and the top-scored single leads: aVR (84.6/84%), II (83.8/83.5%), I (81.2/80.2%).**

Keywords – **ECG Biometrics, multilead ECG scoring, QRS patterns, Discriminant analysis, person verification.**

I. Introduction

The analysis of the electrocardiogram (ECG) as a biometric tool has been started about a decade ago in the context of two typical scenarios for application:

1) Person verification (one-to-one scenario): the ECG of the tested subject is compared to previously recorded ECG with known identity (ID). The tested person is either verified or rejected.
2) Person identification (one-to-many scenario): the ECG of the subject under identity examination is compared to previously recorded set of ECGs in a specific database. The tested person is identified as a subject with unique ID among all in the database.

Two general methods could be distinguished:

1) using measurements after fiducial points detection;
2) analyzing the overall ECG waveform morphology.

At first, the fiducial based approaches are applied. The earliest work involves 12 uncorrelated diagnostic features of P-QRS-T amplitudes and durations [1]. The inter-subject heartbeat similarities are studied via Principle Component analysis score plots. The authors report 100% identification accuracy (IDA) over a database with 20 subjects. Other authors employ 15 temporal features of the P-QRS-T segment into a set of discriminant functions [2]. They report IDA in the range from 97% to 100% over 29 subjects under various stress conditions. A two-step identification method involves temporal and amplitude measurements based on fiducial points detection together with appearance based features that capture the heartbeat patterns [3]. This combined approach provides 100% IDA when tested over 31 healthy subjects: 18 with a single ECG record [4] and 13 with more than one ECG record [5].

Fiducial independent approaches have been developed since 2006. Person identification via autocorrelation (AC) and discrete cosine transform of windowed ECG reports 100% IDA over a database with 14 subjects [6]. Another study also utilizes AC of 5s ECG for person identification and verification [7]. Classification of AC functions via discriminant analysis achieves 96.2% IDA, 87% and 99% verification sensitivity and specificity, reported for a joint dataset [4,8] and 13 healthy subjects with more than one ECG record [5]. The maximal correlation coefficient of a single-lead and 12-lead ECG is reported to provide 91.4% and 100% IDA over a database with 11 subjects [9]. Another effective method calculates the two-dimensional heart vector formed by the limb ECG leads and its first and second derivatives, reporting 98.1% IDA and 97.2% verification accuracy by a distance based approach over 74 subjects [10]. The processing of a normalized QRS complex via Multilyer perceptron provides 96.1% IDA over a database with 30 healthy subjects [11]. Recently, a human ECG identification system has been announced based on ECG decomposition in a number of intrinsic mode functions combined with Welch spectral analysis for extraction of significant heartbeat features [12]. The classification with the K-Nearest Neighbors provides 95.6% IDA over a joint dataset with 108 subjects having one ECG record with ST-segment changes [13,14] and 12 healthy subjects with more than one ECG record [5].

Majority of the cited methods are tested with small-sized ECG databases [1,2,6,8,11] or track intra-subject changes of ECG characteristics measured in very short distanced temporal intervals [2,3,7,11,12]. This might bias the reported high identification/verification accuracy from the real case scenario.

This works aims to compare inter-subject QRS patterns of 15-lead ECG and to rate leads by similarity and difference scores via Discriminant analysis for the purpose of person verification. The use of a large sized ECG-database with two different records per subject taken >1year apart aims at an unbiased accuracy report.

II. ECG Database

The ECG database is collected in the period 2004-2009, including 316 patients at the Emergency Department of the University Hospital Basel. The ECGs are acquired via SCHILLER CS-200 Excellence device with 500Hz sampling rate, 2.5μV resolution.

The database has the following content:

- Includes subjects with a healthy cardiac status, 143 man, 173 woman, aged from 18 to 89 years;
- Includes two 10s resting ECG recordings per subject taken at different times distanced from 1 to 2 years.
- All ECG recordings have a high quality signal in 15 ECG leads – limb (I, II, III, aVR, aVL, aVF), chest (V1-V6), synthesized orthogonal (X, Y, Z).

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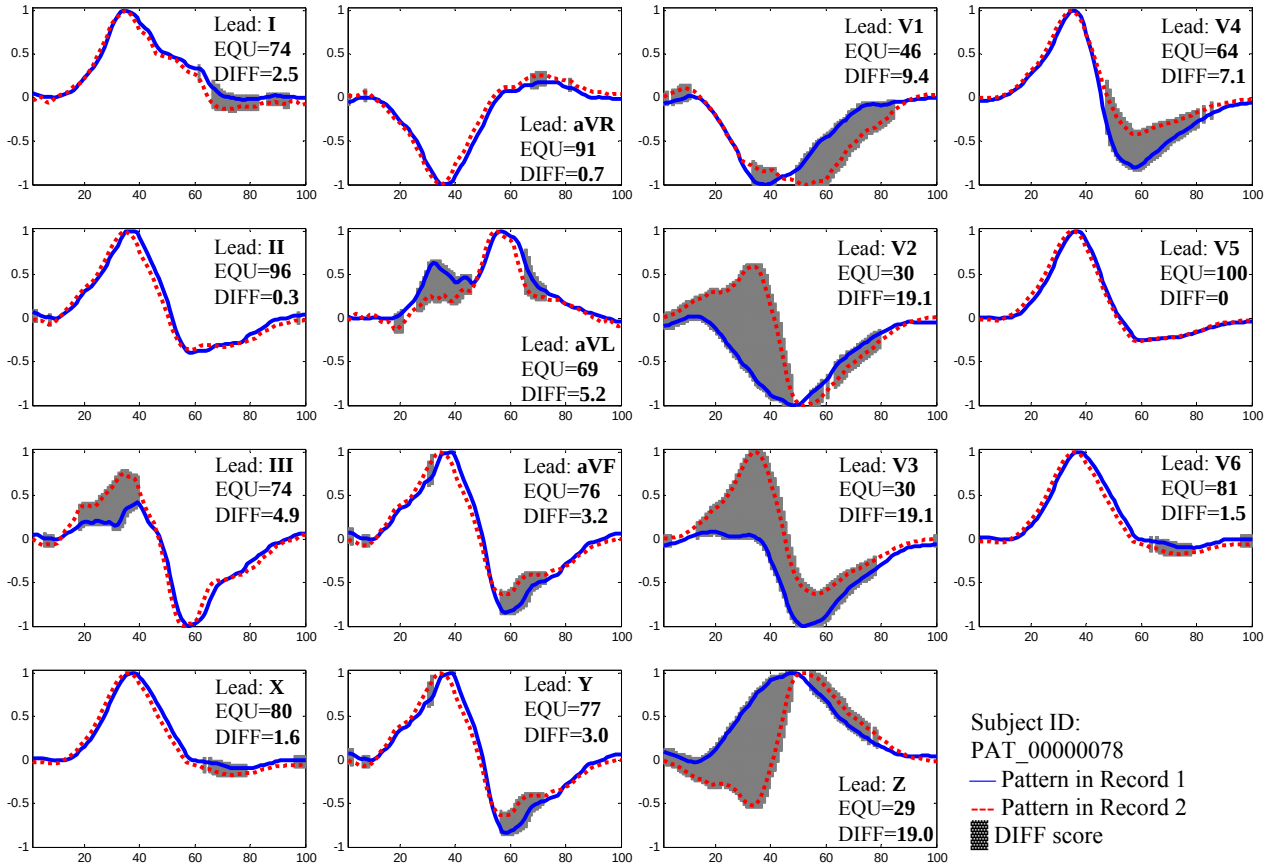

Fig. 1. Comparison of QRS patterns in all 15-leads extracted from two recordings of the same subject.

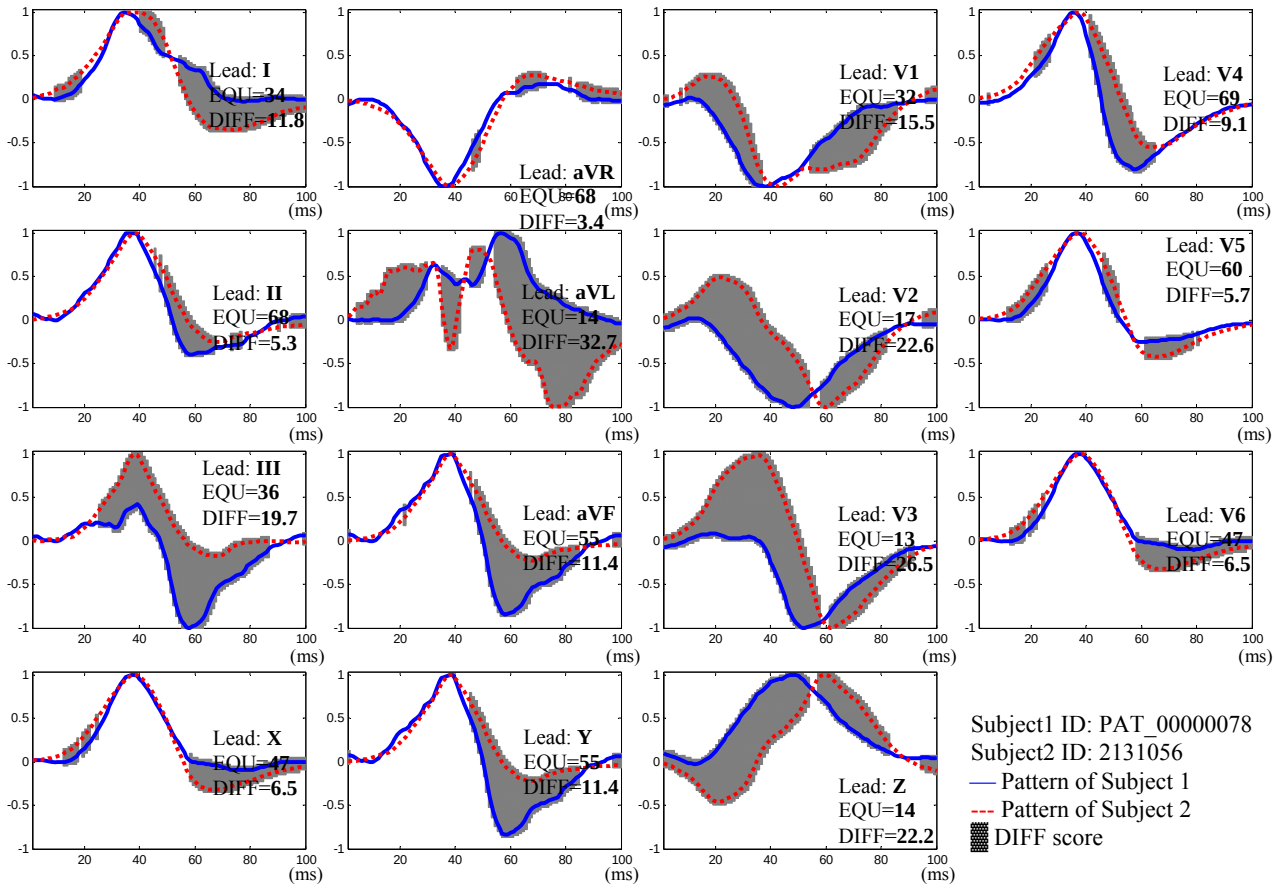

Fig. 2. Comparison of QRS patterns in all 15-leads extracted from the recordings of two different subjects.

III. METHOD

All 10s 15-lead ECG recordings are pre-filtered in a diagnostic bandwidth 0.05–75 Hz. The embedded CS-200 QRS detector is applied to locate RR-intervals, which are then fed to a baseline correction for zeroing of the mean amplitude at the P-wave beginning and the T-wave end. An improved signal-to-noise averaged PQRST patterns are then calculated for each lead.

The method considers QRS patterns extracted from the averaged PQRST patterns during cardiac depolarization, aligned for all leads within a window of 30ms before and 70ms after the R-peak of Lead I. The pattern of each lead is drawn in a normalized 2D space with x-axis [0 to 100] ms; y-axis [-1 to 1], considering y-axis normalization towards the maximal lead amplitude to avoid the influence of intra-subject and inter-lead ECG amplitude differences. The patterns of two different recordings are compared when the respective leads are overlapped in the normalized 2D space and are scored in respect of normalized piecewise equality (EQU score) and difference (DIFF score), where:

- EQU=100%, DIFF=0% corresponds to full amplitude coincidence of all pattern samples;
- EQU<100%, DIFF>0% scores the percentage of the non coinciding samples and the accumulated amplitude differences for them.

Figures 1,2 illustrate the normalized 2D space of the QRS patterns in 15-lead ECG and the calculated EQU, DIFF scores for two scenarios:

(1) One subject is compared to the same subject when its ECG is taken after >1year (Figure 1): EQU=67.8±23.6% (range: 29-100%); DIFF=6.1±6.9% (range: 0-19.1%).

(2) The first subject is compared to a different subject (Figure 2): EQU=41.9±20.7% (range: 13-69%); DIFF=14±8.8% (range: 3.4-32.7%).

IV. RESULTS

The total database statistical distributions in Table 1 show significantly higher EQU and lower DIFF scores in scenario 1 vs. 2 for all 15-leads, $p<0.05$.

Linear Discriminant Analysis (LDA) over EQU and DIFF scores is applied to estimate the potential for person verification of each lead (Fig. 3) and the different lead systems: limb, chest, orthogonal (Table 2).

The following performance indices are considered in the person verification task:

- Sensitivity (Se) scoring the correct verification rate comparing equal subjects, N=316 cases:

$$Se = \frac{\text{Total Nb Correct Verifications}}{N} * 100\,(\%)$$

- Specificity (Sp) scoring the correct rejection rate comparing all different subjects N*(N-1)=99540 cases:

$$Sp = \frac{\text{Total Nb Correct Rejections}}{N*(N-1)} * 100\,(\%)$$

The histograms (Fig.4) give a hint about the range of EQU, DIFF thresholds that provides the top performance found in limb+chest leads (Sp/Se=92.9/92.1%): >92% of equal subjects have EQU>75% or DIFF≤3%; >95% of different subjects have EQU≤80% or DIFF>2%.

TABLE 1. DISTRIBUTION OF EQU AND DIFF SCORES IN 15-LEAD ECG, ESTIMATED FOR THE TWO GROUPS OF EQUAL AND DIFFERENT SUBJECTS, PRESENTED AS: MEAN VALUE ± STD (10-90 PERCENTILE RANGE). THE INDEX MDSTD, CALCULATED AS THE DIFFERENCE BETWEEN MEANS NORMALIZED TO THE MEAN STANDARD DEVIATION IN THE TWO GROUPS IS USED TO RATE THE LEADS WITH THE MOST SEPARABLE DISTRIBUTIONS (BOLDED).

	ECG Leads	EQU score (%) Equal subjects 316 cases	EQU score (%) Different subjects 99540 cases	DIFF score (%) Equal subjects 316 cases	DIFF score (%) Different subjects 99540 cases	MDstd for EQU/ DIFF
Limb	I	90.8±13.2 (70-100)	67.7±15.9 (46-88)	1.2±2.1 (0-3.6)	5.5±3.5 (1.4-10.2)	1.59/ 1.51
	II	**89.2±14.3** (68-100)	**58.2±17.3** (36-81)	**1.5±2.4** (0-4.4)	**7.9±4.3** (2.7-13.7)	**1.97/ 1.89**
	III	65.6±24.2 (31-98)	34.0±16.5 (14-56)	8.2±7.8 (0.2-21.3)	20.7±8.6 (8.7-31.6)	1.55/ 1.53
	aVR	**93.7±11.4** (77-100)	**68.3±16.4** (46-89)	**0.8±1.7** (0-3.1)	**5.3±3.3** (1.2-9.9)	**1.83/ 1.78**
	aVL	67.6±23.7 (33-99)	36.9±16.7 (16-59)	7.7±7.5 (0.1-19.4)	19.2±8.4 (7.8-29.9)	1.52/ 1.45
	aVF	77.6±22.0 (44-100)	44.9±18.3 (22-70)	4.1±5.0 (0-11.3)	12.9±6.8 (5.0-22.5)	1.62/ 1.50
Chest	V1	77.7±22.9 (42-100)	49.5±19.5 (25-76)	3.7±5.1 (0-9.9)	10.2±5.8 (3.5-17.9)	1.33/ 1.20
	V2	69.9±22.6 (38-100)	43.3±17.9 (21-68)	6.6±6.4 (0-15.9)	14.3±6.4 (6.2-23.1)	1.31/ 1.20
	V3	66.3±22.1 (32-96)	43.4±17.8 (21-67)	8.0±6.7 (0.5-17.9)	15.5±6.8 (6.8-24.5)	1.15/ 1.10
	V4	77.0±21.0 (46-100)	53.0±19.4 (27-79)	4.7±5.4 (0-11.7)	11.4±6.6 (3.7-20.9)	1.19/ 1.12
	V5	**86.5±16.0** (64-100)	**61.6±18.8** (36-86)	2.4±3.7 (0-6.5)	7.9±5.2 (2.0-14.8)	**1.43**/ 1.24
	V6	86.6±15.1 (63-100)	64.8±18.0 (40-88)	2.1±2.8 (0-6.2)	6.3±4.0 (1.5-11.8)	1.32/ 1.22
Orthogonal	X	86.7±15.1 (63-100)	65.0±18.0 (46-89)	2.1±2.8 (0-6.2)	6.3±4.0 (1.5-11.8)	1.32/ 1.22
	Y	**77.7±21.9** (43-100)	**45.0±18.3** (40-88)	**4.1±5.0** (0-11.2)	**12.9±6.8** (4.9-22.5)	**1.63/ 1.50**
	Z	70.5±22.3 (37-100)	44.1±18.0 (21-69)	6.4±6.3 (0-15.5)	13.9±6.4 (5.9-22.8)	1.31/ 1.18
Limb		**88.2±9.3** (75-97)	**61.4±11.2** (47-76)	**1.0±1.7** (0-3.2)	**7.2±3.1** (3.4-11.3)	**2.61/ 2.58**
Chest		87.2±9.5 (71-97)	63.4±12.6 (46-80)	1.0±1.9 (0-4.1)	6.4±3.4 (2.3-11.0)	2.15/ 2.04
Orthog.		85.3±11.0 (69-98)	59.5±12.6 (43-76)	1.6±2.1 (0-4.9)	7.4±3.5 (3.1-12.1)	2.19/ 2.07

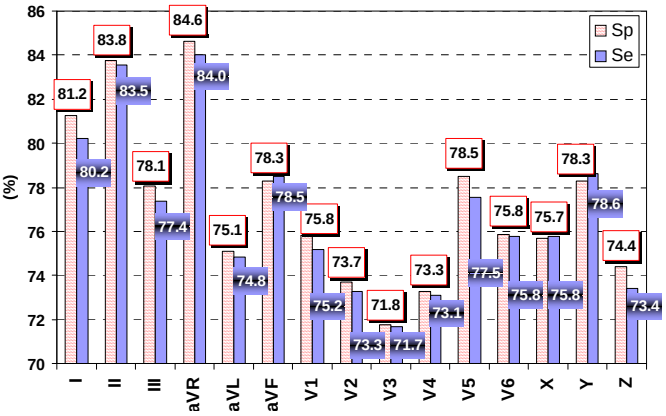

Fig. 3. Mean lead performance for person verification estimated for EQU and DIFF scores by LDA.

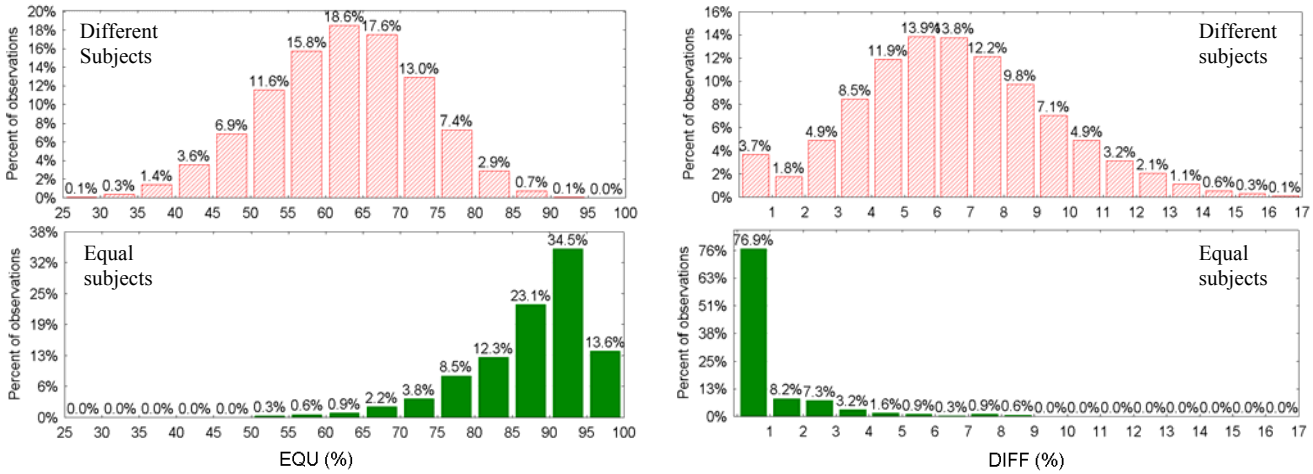

Fig. 4. Histograms of EQU and DIFF scores estimated as a summary for all leads in the top-rated Limb+Chest lead system.

TABLE 2. BEST PERFORMANCE OF DIFFERENT LEAD SYSTEMS FOR PERSON VERIFICATION ESTIMATED FOR EQU, DIFF BY LDA.

ECG leads	**Sp (%)** 99540 cases	**Se (%)** 316 cases
Limb (DIFF)	92.1	89.6
Chest (EQU)	90.1	85.4
Orthogonal (EQU)	86.6	83.5
Limb+Chest (EQU and DIFF)	**92.9**	**92.1**
Limb+Chest+Orthogonal	92.2	90.8

IV. DISCUSSION AND CONCLUSIONS

This study presents a simple method for evaluation of equality and difference of 15-lead QRS patterns that are observed between two recordings of different and equal subjects. The temporal alignment and the normalization for reducing the contribution of the height and width variability of QRS patterns in different recordings is of crucial importance for the correct EQU/DIFF measure.

The study over a large-sized database with 316 subjects provides unbiased person verification from the real-case scenario. The leads with the best separable statistical distributions are bolded in Table 1: II, aVR for limb leads; V5 for chest leads; Y for orthogonal leads; Limb over chest and orthogonal leads. LDA performance of different lead systems shows (Table 2):

(1) Limb leads have the biggest potential for person verification by DIFF score (Sp/Se=92.1/89.6%) with the top-3 rated limb leads (Fig.3): aVR (84.6/84%), II (83.8/83.5%), I (81.2/80.2%).

(2) Chest leads are the second rated for person verification by EQU score (90.1/85.4%) with the top-3 rated Chest leads (Fig.3): V5 (78.5/77.5%), V6 (75.8/75.8%), V1 (75.8/75.2%). The misplacement of the intra-subject lead positions may play deteriorating role for the total performance loss of all chest leads, with the most prominent negative influence in V3,V4,V2.

(3) Synthesized orthogonal leads have the least contribution to the person verification (86.6/83.5%), with the top rated lead Y (78.3/78.6%) in Fig.3.

(4) The combination limb+chest leads provides the best accuracy for person verification (92.9/92.1%), obtained with the common evaluation of EQU and DIFF. Further estimation of orthogonal leads deteriorates the results.

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Adaptive Incremental Estimation Filter for AC Noise in the Electrocardiogram

Dobromir Petkov Dobrev and Tatyana Dimitrova Neycheva

Abstract – **Power-line interference is a common disturbing factor in almost all biosignal acquisition applications. Many filtering procedures for mains interference elimination are available, but all of them are still not enough effective to fully overcome the problem. An interesting adaptive filtering technique for the power-line interference, called 'incremental estimation', was published in the literature. It uses a small step to increment or decrement the amplitude of the estimated interference, synthesized as a pure sine wave. This paper gives the frequency response of the filter and investigates its effectiveness with real ECG signals and Matlab simulations.**

Keywords – **Power-Line Interference (PLI), Adaptive filter, Incremental Estimation Filter (IEF), Electrocardiogram**

I. Introduction

Power-line (PL) interference is a common disturbing factor in almost all biosignal acquisition applications. As a consequence of electrode impedance imbalance and the finite value of the amplifier CMRR, some AC noise remains even when special signal recording techniques are applied (shielding, driven right leg, body potential driving, etc.). A further reduction of PLI usually is achieved by digital post-filtering. Many algorithms for PLI suppression are available, starting from simple comb filters [1], to advanced subtraction procedures and lock-in techniques [2, 3], but all of them tend to lose their efficiency when PL frequency differs from its nominal value.

Nowadays, signal processing capability of popular low-cost microcontrollers is continuously improved. Thus, modern adaptive filtering techniques become more and more popular. Adaptive techniques are advantageous in periodic noise filtering, echo cancellation, signal extraction, etc. because they change their characteristics as the noise or signal of interest change. Such filters operate like a servo system with negative control loop, which minimize a given loss or error function while optimizing the filter coefficients and extracting the noise. Usually, the filter minimizes the output signal power by minimizing the Mean Squared Error (MSE), and such approach of iteratively modifying the filter coefficients using the MSE is called the Least Mean Squared (LMS) algorithm [4, 5]. Once the output power is minimized the noise is canceled. The common disadvantage of such algorithms is their complexity, thus they are unsuitable for popular microcontrollers and real time processing.

A very clever and tricky adaptive filtering approach was published in [6]. The technique is called 'Incremental Estimation' (IE), and is invented by Davide Mortara [6]. The approach is well described also in [5] and [7].

Now, a linearized model of IE approach for frequency response evaluation is developed. The effectiveness of the approach is investigated with real ECG signals and Matlab simulations.

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II. Overview of Adaptive Incremental Estimation Approach for PLI

The operating principle of Incremental Estimation Filter (IEF) is as follows [5, 6, 7]. Let's assume that the PLI is a pure sine wave with amplitude A and frequency ω:

$$e(t) = A\sin(\omega t) \tag{1}$$

For the current n^{th} sample in discrete time processing, the Eq. (1) can be expressed as Eq. (2):

$$e_n = e(nT) = A\sin(\omega nT) \tag{2}$$

Replacing (nT) with ($nT - T$) in Eq. (2), an expression for the past sample can be found:

$$e_{n-1} = e(nT - T) = A\sin(\omega nT - \omega T) \tag{3}$$

Similarly, the same can be done for the future sample ($nT + T$), and Eq. (2) becomes:

$$e_{n+1} = e(nT + T) = A\sin(\omega nT + \omega T) \tag{4}$$

Recalling to the trigonometric identity:

$$\sin(\alpha + \beta) = 2\sin\alpha\cos\beta - \sin(\alpha - \beta) \tag{5}$$

where α and β are:

$$\alpha = \omega nT\ ,\quad \beta = \omega T \tag{6}$$

and replacing Eq. (5) in Eq. (4) gives:

$$e_{n+1} = 2A\sin(\omega nT)\cos(\omega T) - A\sin(\omega nT - \omega T) \tag{7}$$

The first term in Eq. (7) contains Eq. (2), and the second term is Eq. (3), so the Eq. (7) can be rewritten as Eq. (8):

$$e_{n+1} = 2\cos(\omega T)e_n - e_{n-1} \tag{8}$$

The term $cos(\omega T)$ is a constant determined only by the PL frequency f_{pl} and the sampling frequency f_s=1/T:

$$N = \cos(\omega T) = \cos(2\pi f_{pl} / f_s) \tag{9}$$

Replacing Eq. (9) in Eq. (8) gives a relation for the future sample of the sinusoidal noise, based on the values of the current and the past samples.

$$e_{n+1} = 2Ne_n - e_{n-1} \tag{10}$$

The output of the filter is the difference between the input and the estimated noise:

$$y_{n+1} = x_{n+1} - e_{n+1} \tag{11}$$

Thus, if the input is only noise and the estimate is exactly tracking, the filter output will be zero.

Producing the estimated signal requires multiplication by a fraction N given in Eq. (9). Such a multiplier requires floating point arithmetic, which could considerably slow the algorithm. In order to approximate such multiplier, it might be built on a summation of power-of-two fractions, which can be implemented with simple bit-shift operations and can be faster and only possible on popular microcontrollers. For example, if f_s=2kHz, N=0.9877008 could be realized as: $N \approx 1\text{-}2^{-6}+2^{-8}\text{-}2^{-11}\text{-}2^{-12} = 0.98767$.

The synthesized by Eq. (10) sine wave needs of a negative feedback control loop to adjust the sinusoidal amplitude for each sample, and thus to track the changes in the PLI.

The input signal for two neighbor samples consists of slowly varying signal or DC component, and PLI noise:

$$x_{n+1} = x_{DC_{n+1}} + e_{n+1} \tag{12}$$

$$x_n = x_{DC_n} + e_n \tag{13}$$

Assuming that the input DC level does not change significantly between samples, then an error function can be defined as:

$$f_{err} = x_{DC_{n+1}} - x_{DC_n} \approx 0 \tag{14}$$

Replacing Eq. (12) and Eq. (13) in Eq. (14) gives:

$$f_{err} = (x_{n+1} - e_{n+1}) - (x_n - e_n) \tag{15}$$

Eq. (15) can be rearranged as:

$$f_{err} = (x_{n+1} - x_n) - (e_{n+1} - e_n) \tag{16}$$

Thus, Eq. (16) presents a subtraction of the first difference of the estimated noise from the first difference of the input signal. It cancels the DC levels while simultaneously comparing and adjusting to equalize the increment in the estimated waveform to the increment in the input. That is why, the filter is called 'incremental estimation' by Mortara in [6]. In other words, the input and the estimated noise are initially high-pass filtered and after that compared. The result of comparison is the value of the error function f_{err}. If the error function f_{err}>0, the amplitude of the PLI estimate is adjusted upward by a small step size d.

$$e_{n+1} := e_{n+1} + d \tag{17}$$

If the error function f_{err}<0, the PLI estimate is adjusted downward by the same small step size d.

$$e_{n+1} := e_{n+1} - d \tag{18}$$

If the function f_{err}=0, the estimate is not changed:

$$e_{n+1} := e_{n+1} \tag{19}$$

The choice of d is empirically determined and depends on how quickly the filter needs to track the changes in the interfering noise. If d is large, then the filter quickly adapts to the noise change. With a smaller d, the filter requires a longer learning time but provides more exact tracking of the noise. If the value of d is too large or too small, the filter will never converge to a proper noise estimate. A starting value of d could be less than 1LSB, e. g. 0.25LSBs [5].

III. Frequency Response

It is more convenient for the realization and simulation of the Eq. (10) and Eq. (11) to rewrite them for one sample interval in the past:

$$e_n = 2Ne_{n-1} - e_{n-2} \tag{20}$$

Thus, the output of the filter becomes:

$$y_n = x_n - e_n \tag{21}$$

The filter frequency response can be evaluated on a linearized model shown in *Fig. 1*.

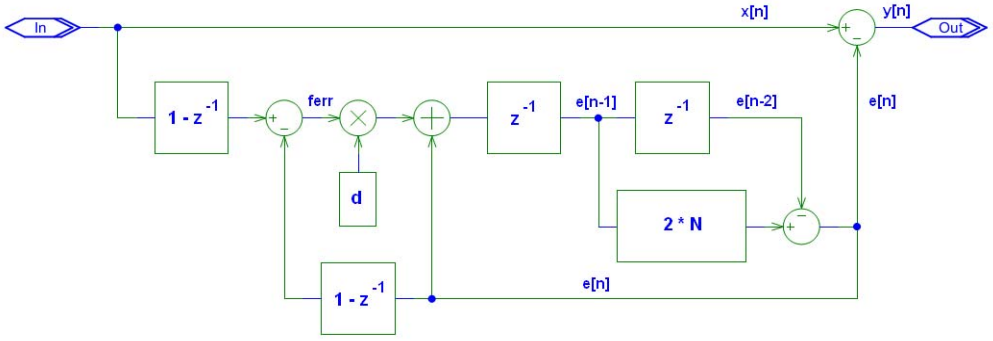

Fig. 1. Linearized model for frequency response simulation of IEF for PLI

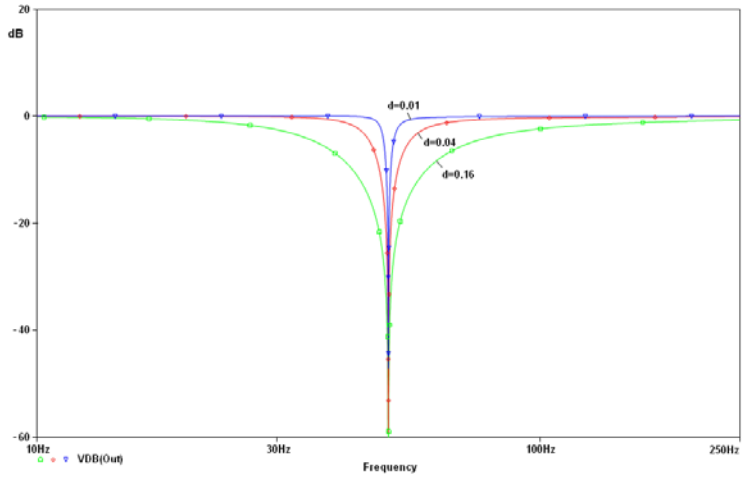

Fig. 2. Frequency response of IEF for PLI

The schematic from *Fig. 1* is simulated and the result is shown in *Fig. 2*.

Looking at the schematic in *Fig. 1* it is clear that it consists of two high-pass first difference filters. One is in series to the input signal *x[n]*. The second one is in series to the estimated signal *e[n]*. The second one also is appeared inside the control loop. So, its characteristic, towards *e[n]*, will be inverted from high-pass to low-pass, and ignoring the other blocks for sine wave generation, we can say that *e[n]* will have a combination of high-pass and low-pass response, i. e. it will exhibit a band-pass characteristic. Subtracting band-pass characteristic from the input, (i. e. from unity), the characteristic is again inverted and for the output *y[n]* the final characteristic becomes band-rejection or notch.

What about the coefficient *d*? The coefficient *d* controls the amount of the feedback and in this manner, the bandwidth, i. e. the quality factor *Q* of the whole filter.

From *Fig. 3*, when d_1=0.01 the bandwidth at 3dB is Δf_1=3.2Hz. When d_2=0.04, the bandwidth is Δf_2=12.7Hz, and when d_3=0.16, the bandwidth is Δf_3=48.6Hz.

The quality factor *Q* can be calculated according the well known formula:

$$Q = \frac{f_{pl}}{\Delta f_{3dB}} \tag{22}$$

Thus, for f_s=2kHz and f_{pl}=50Hz, when d_1= 0.01 Q_1=15.6, for d_2=0.04 Q_2=3.9, and for d_3=0.16 Q_3=1.03. When *d* is referred to 1V, the bandwidth can be expressed as [7]:

$$\Delta f_{3dB} = \frac{d \cdot f_s}{2\pi} \tag{23}$$

Replacing Eq. (23) in Eq. (22), the formula for *Q* becomes:

$$Q = \frac{2\pi f_{pl}}{d \cdot f_s} \tag{24}$$

Thus, using the Eq. (24), the calculated values of *Q* are: Q_1=15.7, Q_2=3.925, Q_3=0.98. As can be seen, the calculated values correspond to the simulated ones, and this proves the truthfulness of Eq. (23) and Eq. (24).

The consequence is that the quality factor *Q* is inversely proportional to the sampling rate f_s, and to the size of the correction step *d*.

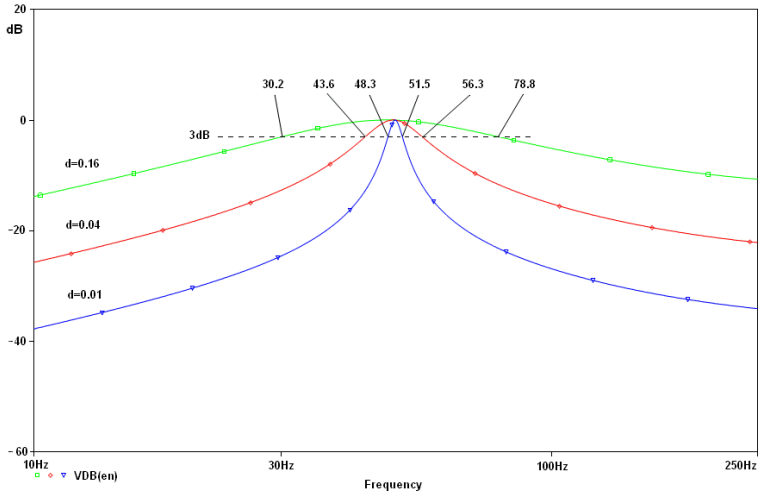

Fig. 3. Frequency response of the estimated PLI at the output *e[n]*

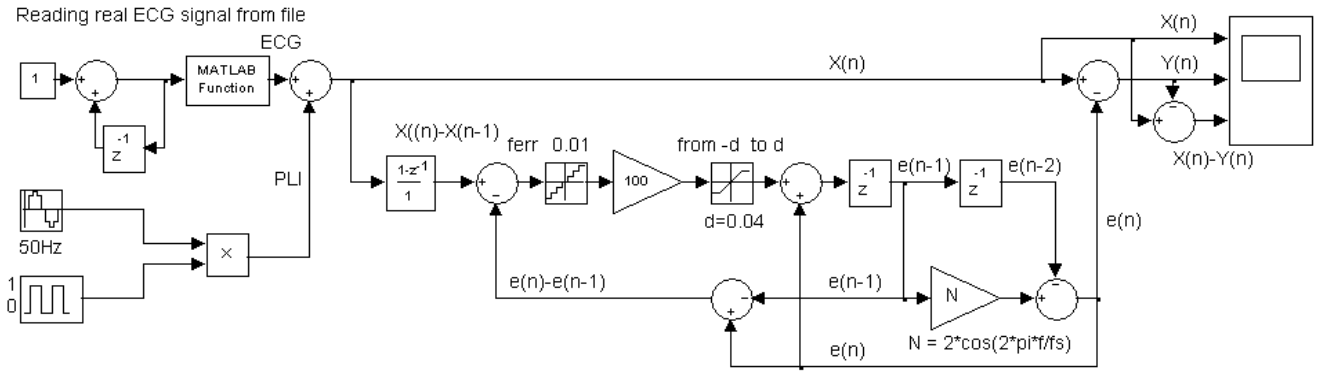

Fig. 4. Simulink schematic for IEF simulation

IV. MATLAB SIMULATIONS

Simulink schematic for IEF simulation is shown in *Fig. 4*. The simulation result is shown in *Fig. 5*, where the first trace is the ECG signal with noise, the second trace is the filtered ECG signal and the third trace is the PLI estimate, i. e. the difference between trace 1 and trace 2. 1LSB corresponds to 1.25uV.

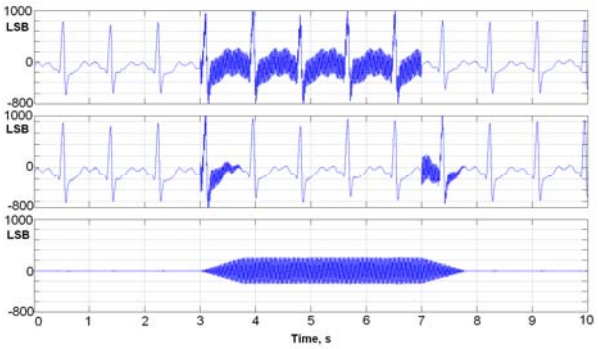

Fig. 5. IEF simulation result with real ECG signal

It can be seen that the IEF quickly tracks the PLI.

V. CONCLUSION

The IEF is presented and its frequency response is analyzed. The filter generates a sine wave and adjusts its amplitude to track the PLI. The quality factor Q is inversely proportional to the sampling rate f_s, and to the size of the correction step d. Generally speaking, to not distort the useful ECG signal, the PLI filter must have bandwidth of ±5Hz or Δf<10Hz, i. e. its Q factor must be higher than 5 or according the Eq. (24), the step size d must be lower than 30m. The filter adaptation time depends on the selected Q factor, and is inversely proportional to the step size d. The filter employs comparison of increments in the input signal and in the generated estimate. This is possible only if the input signal is slowly varying in comparison to PLI noise. Dynamic increase of the step size d can lead to faster adaptation time, but after adaptation, the step d must be returned to its nominal value to avoid generation of spurious residual noise in the ECG.

The filter behavior corresponds to the selected Q factor, and is similar to other high-Q filters [8]. The main advantages of the approach is its relative simplicity, and that the sampling rate is not needed to be multiple to the PL frequency. If the PL frequency is changed, the filter accurately can track the new value only by changing the coefficient N. This is not possible to other filters like [1, 2, 3, 8], where for maximal rejection the sampling rate must be multiple to PLI frequency.

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Software PLL for Power-line Interference Synchronization: Implementation and Results

Dobromir Petkov Dobrev and Tatyana Dimitrova Neycheva

Abstract – **Power-line interference is a common disturbing factor in almost all two-electrode biosignal acquisition applications. Many filtering procedures for mains interference elimination are available, but all of them are maximally effective when the filter notches are positioned exactly at the power-line harmonics, i. e. when the sampling rate is synchronous with the power-line frequency. Moreover, various lock-in techniques, such as automatic common mode input impedance balance, require precise in-phase and quadrature phase references, synchronous with the power-line interference. Recently a design methodology of software PLL for power-line synchronization was published. This paper describes the results of its practical realization.**

Keywords – **Software PLL (SPLL), All-digital PLL (ADPLL), Power-line Synchronization**

I. Introduction

Power-line (PL) interference is a common disturbing factor in almost all biosignal acquisition applications. As a consequence of electrode impedance imbalance and the finite value of the amplifier CMRR, some AC noise remains even when special signal recording techniques are applied (shielding, driven right leg, body potential driving, etc.). A further reduction of PL interference usually is achieved by digital post-filtering. Many algorithms for PL interference suppression are available, starting from simple comb filters [1], to advanced subtraction procedures and lock-in techniques [2, 3], but all of them tend to lose their efficiency when PL frequency differs from its nominal value. Maximal rejection is possible only when the sampling rate is synchronous with the PL frequency, because only at that case, the filter notches coincide with the PL harmonics.

A lock-in technique for input common mode impedance balance was developed [4]. The approach is based on two digitally regulated control loops to maintain resistive and capacitive input common mode impedance balance. The control loops require precise in-phase and quadrature phase references, synchronous with the common mode PL interference. If the synchronization is lost, the negative feedback can become positive, leading to instability problems and lack of convergence.

Recently a design methodology of Software PLL (SPLL) for synchronization with the PL interference was published [5]. It was shown how the PLL loop gain could be evaluated in *s*-domain, and how the *z*-domain transfer function can be derived from its analog prototype using *s* to *z* backward difference mapping. Now, the discussed SPLL is realized on STM32F407 microcontroller, and this paper gives some results of its implementation.

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II. Overview of SPLL Design

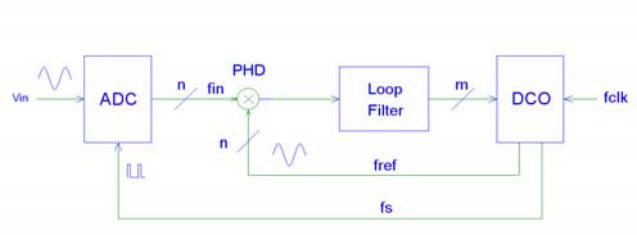


Fig. 1. Software PLL structure

The SPLL structure is shown in *Fig. 1*. It consists of three blocks: Phase Detector (PHD), Loop Filter and Digitally Controlled Oscillator (DCO). The input signal V_{in} is processed in digital form, after ADC it is *n*-bits data stream. The mixer or phase detector (PHD) simply is a multiplier. Square wave mixing greatly simplifies the mixer operation, but could be used only when the loop bandwidth is lower enough in comparison to the generated frequency. Sine wave mixing is preferable when low jitter is a must. The Loop Filter (LF) integrates the data in time, and due to averaging increases the resolution, so the DCO input could be *m*-bits ($m \geq n$) word. For proper processing at low oversampling ratios, the sampling rate f_s must be multiple to the reference frequency f_{ref}. Once the DCO range is defined to cover all variation of the input frequency with reserve, the SPLL design is reduced to the LF design. Thus, the LF must be carefully designed to provide stable system with appropriate settling time.

The loop gain is responsible for the stability of each control system. In the presented SPLL design, the loop gain analysis is derived from its analog PLL prototype, see *Fig.2*. The shown structure contains two integrators, i. e. it represents a second order transfer function. The first pole, at DC, is related to the VCO, which serves as an ideal integrator included in the loop [6, 7]. The second pole, also at DC, is due to the integrator in the Loop Filter, and must be compensated for stability by adding a zero with forward path with a coefficient k_z.

The Phase Detector gain G_{PHD} has dimension $\frac{V}{rad}$, while the VCO gain G_{VCO} has dimension $\frac{rad}{sV}$. The reciprocal value of the product $G_{PHD}G_{VCO}$ has dimension of seconds, and for simplicity can be denoted by a symbol τ_{vco}. So, the

timeconstant τ_{vco} determines the roll-off of the inherent integrator in the loop, hidden in the VCO operation.

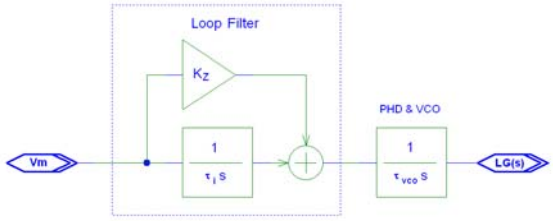


Fig. 2. PLL loop gain in analog prototype

Thus, the transfer function of the shown in *Fig*. 2 loop gain is dimension less, and can be expressed with Eq. (1):

$$LG(s) = \frac{1 + k_z \tau_i s}{\tau_i s} \cdot \frac{1}{\tau_{vco} s} \tag{1}$$

More details on analysis of Eq. (1) can be found in [5]. The goal is to be found the unity gain frequency of the open loop gain, because it determines the bandwidth and stability of the closed loop system. For τ_{vco}=1.3s, τ_i=1s and k_z=8, the open loop unity gain frequency is about 1Hz. Thus, the closed loop bandwidth will be fast enough because a bandwidth of only 0.1Hz is sufficient for tracking PL frequency.

Next, the loop gain in *z*-domain easily can be found using the backward difference mapping of *s*-plane to *z*-plane according the Eq. (2) [5, 8]. Here, $T=1/f_s$ is the sampling interval, reciprocal to the sampling frequency f_s.

$$s = \frac{1 - z^{-1}}{T} \tag{2}$$

In analog PLL usually a third pole is inserted in the LF for high-frequency filtering and reducing VCO jitter. It affects frequencies faraway from 0dB point to maintain stability. In SPLL the best and simple way for high-frequency filtering is by one PL period moving-average filter (averager). The averager effectively cancels all harmonics of PL frequency and will reduce ripples at the VCO input. Adding 1PL period averager will introduce group delay of 10ms in the loop. Evaluated at 1Hz, this delay corresponds to 3.6 degree phase lag. Adding additional delay of one sampling period at f_s=2kHz, or 0.18 degree, the total phase margin will drop by about 4 degree. The conclusion is that 1PL period averager is possible to be added in the loop, and will reduce the phase margin by 4 degree. The modified loop filter by added 1PL period averager is shown in *Fig. 3*.

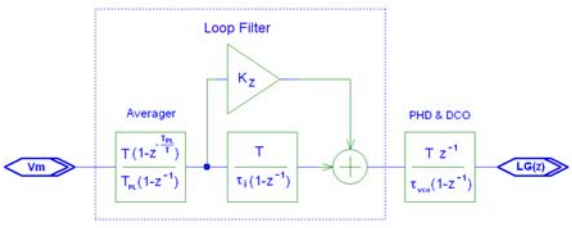


Fig. 3. SPLL loop gain in *z*-domain

The loop gain from *Fig. 3* can be written as Eq. (3):

$$LG(z) = LF(z) \cdot \frac{Tz^{-1}}{\tau_{VCO}(1 - z^{-1})} \tag{3}$$

Where LF(*z*) is the loop filter transfer function, and the second multiplicand is the transfer function of the phase detector and the DCO. The loop filter transfer function LF(*z*) includes 1PL period averager, and can be expressed with Eq. (4):

$$LF(z) = \frac{T(1 - z^{-\frac{T_{PL}}{T}})}{T_{PL}(1 - z^{-1})} \cdot \frac{T + k_z \tau_i (1 - z^{-1})}{\tau_i (1 - z^{-1})} \tag{4}$$

Adding a coefficient $k_i = \frac{T}{\tau_i}$ in Eq. (4), it can be rewritten as Eq. (5):

$$LF(z) = \frac{1 - z^{-\frac{T_{PL}}{T}}}{1 - z^{-1}} \cdot \frac{T}{T_{PL}} \cdot \frac{k_i + k_z (1 - z^{-1})}{1 - z^{-1}} \tag{5}$$

The transfer function expressed in Eq. (5) can be realized with signal flow schematic shown in *Fig. 4*.

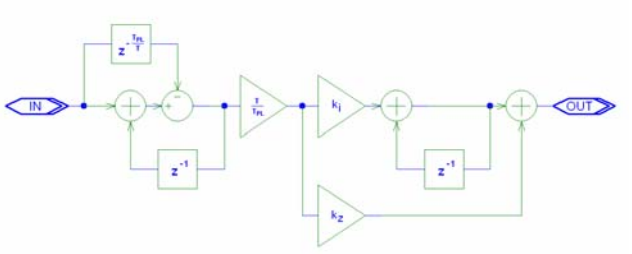


Fig. 4. SPLL loop filter realization

III. Loop Filter Optimization in Matlab

Simulink schematic for loop filter optimization is shown in *Fig.5*. Matlab simulations are run to evaluate the stability of the SPLL and to optimize the LF coefficients k_i and k_z. The goal is to achieve as fast as possible stable response.

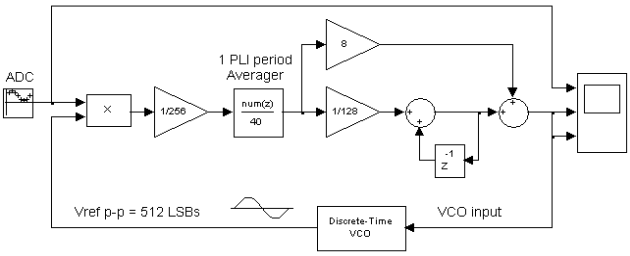
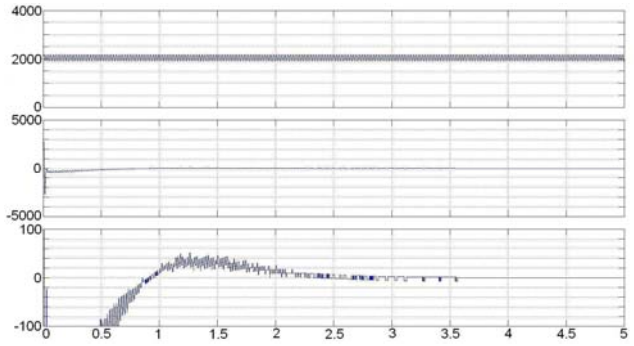


Fig. 5. Simulink schematic for LF optimization

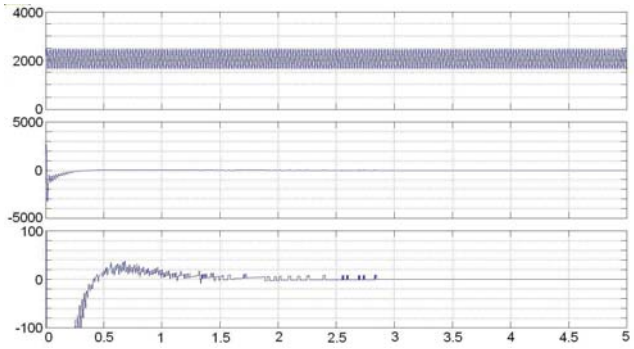
For lower DCO input jitter a sine wave mixing is used. For avoiding floating point multiplications, the DCO generates sine wave with 256LSBs amplitude. The mixer output is divided by 256 to keep the loop gain. The DCO sensitivity is 1mHz/LSB, and 1LSB corresponds to 3V/4096=0.732mV, thus the DCO sensitivity is 1.36Hz/V.

The coefficient k_z is fixed to k_z=8. The coefficient k_i was varying starting from k_i=0.5m, as was shown in [5]. It was found that fast and stable response is achieved when k_i is increased up to k_i=8m, which value easily can be implemented by a division of 128, i. e. $k_i=2^{-7}$=7.8m. The phase margin, when k_i=7.8m, drops to about 65 degree but still preserves good stability.

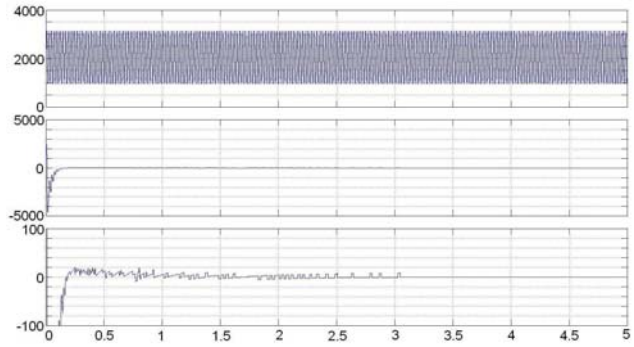
The simulation results are shown in *Fig. 6*. The first trace is the input frequency. The second and the third traces are the DCO input at a different zooms. Because the loop speed depends on the input amplitude, the stability must be checked in all possible variations of the input amplitude, i. e. in its minimum, typical and maximum values.



a) Min. V_{in}=200mV$_{pp}$, f_{in}=50Hz



b) Typ. V_{in}=600mV$_{pp}$, f_{in}=50Hz



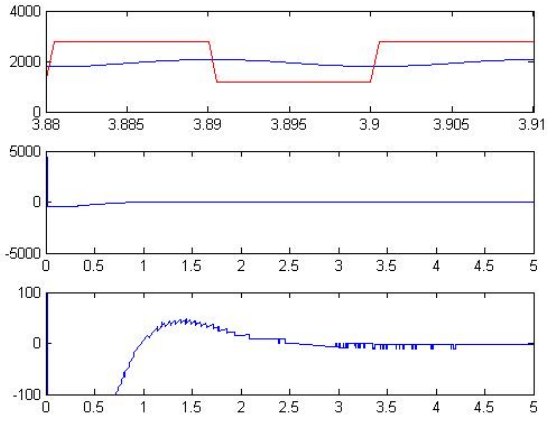
c) Max. V_{in}=1.6V$_{pp}$, f_{in}=50Hz

Fig. 6. Simulink simulation results

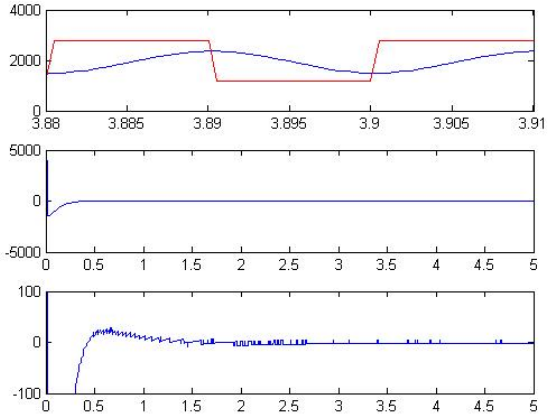
It can be seen that the settling of the DCO input has a small overshoot but the response is stable in all variations of the input amplitude.

IV. Practical Realization and Results

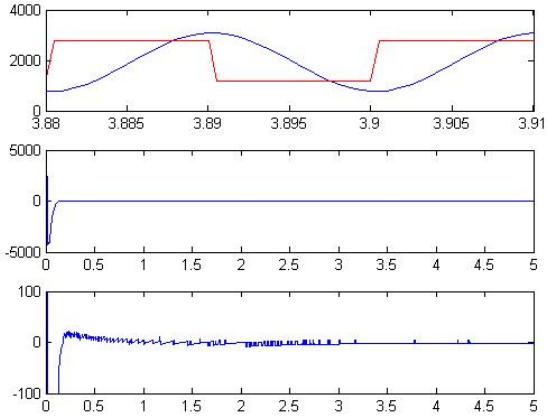
The SPLL is implemented on the microcontroller STM32F407. The microcontroller incorporates a 12-bits ADC which is used for converting the input signal. At the first trace the input frequency, and the generated reference converted in rectangular form are shown. The second and the third traces are the DCO input at a different zooms. It can be seen that the stability shown in the practical results corresponds to the Matlab simulations shown in *Fig. 6*.



a) Min. V_{in}=200mV$_{pp}$, f_{in}=50Hz

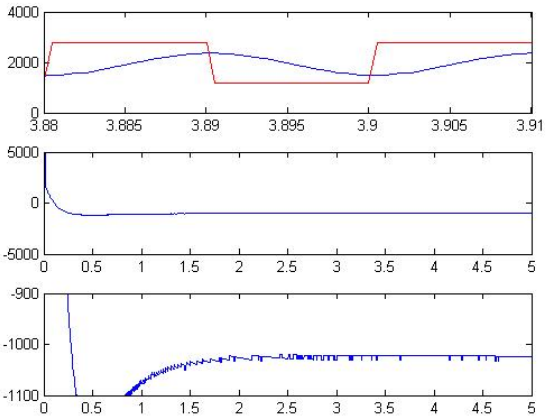


b) Typ. V_{in}=600mV$_{pp}$, f_{in}=50Hz

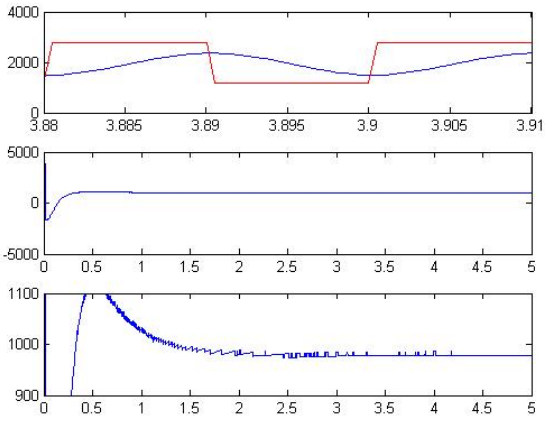


c) Max. V_{in}=1.6V$_{pp}$, f_{in}=50Hz

Fig. 7. Practical results for f_{in}=50Hz



a) Typ. V_{in}=600mV$_{pp}$, f_{in}=49Hz



b) Typ. V_{in}=600mV$_{pp}$, f_{in}=51Hz

Fig. 8. Practical results for f_{in} variation ±1Hz

Practical results when f_{in} vary ±1Hz are shown in *Fig.* 8. The DCO input is settled to about ±1000LSBs. As was noted previously, the loop speed depends on the input signal amplitude. Automatic Gain Control (AGC) of the input signal amplitude could be added in addition for constant settling time [5]. *Fig. 7* and *Fig. 8* show the real operation of the microcontroller. The shown data are in LSBs vs. Time, and 1LSB corresponds to 0.732mV. The data are transferred to PC, and are visualized with Matlab.

From the DCO input shown in the third trace in *Fig. 7* and *Fig. 8*, it can be seen that the loop has stable response in all variation of the input amplitude and frequency from V_{in}=200mV$_{pp}$ to V_{in}=1.6V$_{pp}$, and f_{in}=±1Hz. When the DCO input is settled the generated rectangular reference, derived from the used in the mixer sine wave reference, leads the input sine wave in 90 degree, see the first traces in *Fig. 7* and *Fig. 8*. To minimize the DCO input remaining ripple, the ADC sampling rate is multiple to the generated reference. Thus, the averager, included in the loop filter, is maximally effective in rejection the PL harmonics. Note, that the 1PL period averager is a comb filter with notches at all harmonics of the PL interference. It plays a very important role as a part of the loop filter for lowering the pulsation at the DCO input. Without averager the DCO will operate with higher level of ripples, due to forward path in the LF integrator, see *Fig. 4*.

V. CONCLUSION

The SPLL implementation is discussed, and real practical results of its operation are shown. The results correspond to the made simulations. The DCO input has stable response in all possible variations of the input signal amplitude and frequency. The main advantage of the approach is that the synchronization is done in software, so it has no production cost.

The SPLL purpose is to generate synchronous reference to the common mode PL interference in two-electrode amplification. It is intended for use in ECG signal processing, but can be used after easy adaptation in various digital signal processing applications, where frequency synchronization is needed.

A design methodology of SPLL was described in [5], where it was shown, how the SPLL *z*-domain transfer function can be derived from its analog PLL *s*-domain prototype. The two articles, this and the previous one [5], could be used as a SPLL tutorial because all steps in the design process are considered, from modeling and simulation to final realization and validation. Of course, to understand the subject, the reader should have at least a basic knowledge with feedback control theory, and with *s* and *z* domain transfer functions.

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Overview of Photoacoustic Imaging in the Medical Diagnostics Field

Viktor Ventsislavov Stoev

Abstract – **The acoustic and optical domains bind in the relatively novel field of photoacoustic imaging, where a short pulse of electromagnetic energy generates an acoustic wave. Capable of delivering high contrast images, the technique is drawing considerable attention as a tool for diagnosis of cancer, lipid deposits, hemoglobin concentration, brain related diseases and many more. The theory of image reconstruction has undergone extensive research in the past 20 years which, coupled with the innovations in signal generation and detection, has successfully advanced the field to the preclinical stage. In this paper we give an overview of the specifics of photoacoustic imaging and elaborate on image reconstruction, signal generation and acquisition.**

Keywords – **Photoacoustic imaging, inversion, laser, transducer**

I. Introduction

Since the discovery of X-rays, medical imaging has played an increasingly important role in the correct diagnosis and treatment of various diseases. This has prompted research institutions, universities and companies to continuously enhance our capabilities of acquiring accurate reconstructions of the inner human body. By now, many imaging techniques have emerged and evolved among which are magnetic resonance imaging (MRI), X-ray computed tomography (CT), ultrasound (US), positron emission tomography (PET), optical coherence tomography (OCT) and others.

In recent years, this pleiad has been enriched by the novel technique of photoacoustic imaging (PAI, also known as optoacoutsic imaging – OAI), which has by now matured to the preclinical stage and will soon become an essential tool for the diagnosis of diseases.

In photoacoustic imaging, acoustic waves are generated by irradiating an optically absorbing media with short pulses of electromagnetic energy. As the energy deposits, a local rise of the temperature occurs. This drives the heated medium to expand rapidly, which is followed by the generation of a mechanical stress in the form of an acoustic wave. This is referred to as the thermo-optical mechanism of stress generation [1]. A typical PA image, recorded with a hydrophone is depicted in Figure 1. Notice the distinct bipolar shape, corresponding to the expansion and shrinking of the heated domain.

The optically absorbing molecules in the human body are called chromophores and their concentration will determine the acoustic wave amplitude. However, the process of signal generation is non-linear, it depends on the concentration of chromophores, but on the laser energy and thermodynamic properties of the tissue as well. Hence, what we observe as an acoustic wave is not directly proportional to the light absorbing molecules concentration, as was initially considered [2]. Nevertheless, light absorption is dominating, which allows for high tissue differentiation - a major difference to ultrasound imaging.

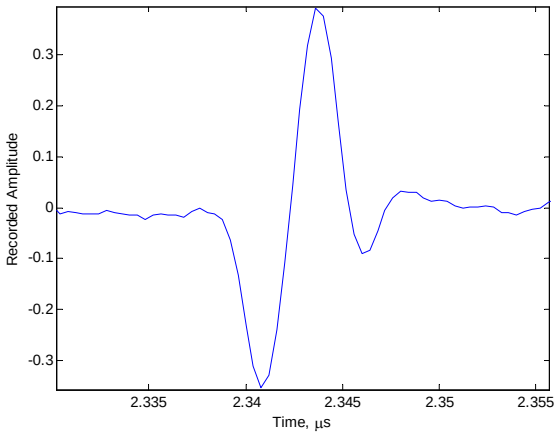

Fig. 1. Acquired photoacosutic signal representing the response of a string of hair to pulsed electromagnetic energy (the signal shape is inverted).

Apart from chromophores concentration, the signal amplitude depends strongly on the irradiation time. If it is sufficiently smaller than the time it takes for the pressure wave to propagate through the illuminated medium, the amplitude will be maximum. This is known as the stress confinement rule [3] and is the reason why nanosecond excitation sources are used in PAI.

Another distinguishing feature between ultrasound imaging and PAI is that the latter depends not only on the acoustic properties of the irradiated volume, but on the optical ones as well. The optical domain characteristics determine the penetration depth (it is deemed as the depth at which light becomes diffuse), as well as the signal amplitude, since absorption is wavelength dependent. Typically, wavelengths in the 600-900nm range are used, as penetration there can extend to several centimeters, but other wavelengths as short as 400nm and as long as 1210nm are also utilized [4]. Once the illuminated region relaxes and the acoustic wave starts to propagate, the acoustic domain properties take place into shaping the signal. The signal undergoes acoustic attenuation(A), diffraction(D), acoustic wave reflection and transmission(T). Their effect is cumulative and we denote it here asψ, where

$$\psi = TDA \tag{1}$$

These parameters define the profile of the photoacoustic signal, the bandwidth and the amplitude. A typical

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bandwidth in the tissue will span the 1 – 30 MHz range, with the amplitude of the acoustic pressure not exceeding 10kPa and the penetration depth extending to a few centimeters at best. However, these characteristics allow for a remarkably broad area of applications.

Photoacoustic imaging is suitable for blood vessel imaging and differentiation between oxygenated and deoxygenated blood, as blood is a very strong light absorber in the near-infrared region [5]. Since tumours exhibit a high microvessel density (angiogenesis in medical terms), this malignant area will show an increased level of absorption of laser light which, coupled with the high spatial resolution of PAI can be used for the detection of breast cancer [6]. Other biomedical applications include imaging of lipid deposits found in atherosclerotic plaques with wavelength of 1210nm, intravascular imaging, photoacoustic microscopy, imaging of the brain vasculature, joints and combined US-PA imaging.

In this paper, we overview different approaches to image reconstruction and photoacoustic signal generation. We focus on the model-based reconstruction method and provide several experimental results that highlight some of the applications and problems intrinsic to the photoacoustic imaging technique.

II. Theoretical Backgrounds

Imagine a volume filled with liquid with isotropic characteristics and a laser light source, capable of delivering short impulses of EM energy that meet the stress and thermal confinement requirements (heat must not dissipate during the heating process). Then a photoacoustic signal will be generated which, in the linear approximation, can be described as [7]

$$\nabla^2 p(\mathbf{x},t) - \frac{1}{c^2}\frac{\partial^2}{\partial t^2}p(\mathbf{x},t) = -\frac{\beta}{C_p}\frac{\partial H(\mathbf{x},t)}{\partial t} \qquad (2)$$

Formula (2) is known as the photoacoustic wave equation, where$p$ is the acoustic wave pressure (in Pa) and c is the speed of propagation. The source term (the right-hand side) contains two parameters namely, the specific heat capacity C_p, and the volume thermal expansion β. The source denoted as $H(\mathbf{x},t)$, is the so-called heating function and it shows us the heat deposited in the illuminated object per unit volume per unit time. The function is explicitly given as $H(\mathbf{x},t) = \mu_a(\mathbf{x})F(\mathbf{x},t)$, where the second term represents the laser fluence rate at a point in the object while, $\mu_a(\mathbf{x})$ is the absorption of the structure. It should be noted that the fluence rate depends not just on the laser source characteristics, but on the absorption (and scattering) of the structure as well. This gives a nonlinear relationship between the generated signal and the absorption occurring in the illuminated object. This is why we say that the photoacoustic images are absorption dominated, but not linearly proportional to the absorption.

A solution to equation (2) for the pressure p is the starting point for image reconstruction. Following a Fourier domain procedure a forward solution to the problem can be found by first applying a Laplace transform over the temporal component and a 3-D Fourier transform over the spatial component. The result is the $(\mathbf{k}, s)$ domain expression for the PA wave equation, which written in terms of the spectral domain Green's function is given as

$$\tilde{p}(\mathbf{k},s) = \frac{\Gamma}{c^2}\tilde{G}(\mathbf{k},\mathrm{s})s\tilde{H}(\mathbf{k},s) \qquad (3)$$

Where $\tilde{G}(\mathbf{k},\mathrm{s}) = \frac{1}{(\mathbf{k}^2+\gamma^2)}$ is the Green's function, $\gamma^2 = \frac{s^2}{c^2}$, $\mathbf{k}^2 = (\mathrm{k}\cdot\mathrm{k})$ and $\Gamma = \frac{c^2\beta}{C_p}$. The latter coefficient is called the Grüneisen coefficient, it is dimensionless and equals approximately 0.11 for water at room temperature.

However, a solution in the time domain or in frequency domain is more intuitive. Applying the inverse 3D Fourier transform to equation (3) we arrive at the desired solution in frequency domain expressed as

$$\hat{p}(\mathbf{x},s) = \frac{\Gamma}{c^2}s\int\limits_{\mathbf{x}'\in\mathbb{D}_H}\hat{\mathrm{G}}(\mathbf{x}-\mathbf{x}',\mathrm{s})\hat{H}(\mathbf{x}',s)\mathrm{d}V \qquad (4)$$

where $\mathbb{D}_H$, is the illuminated volume. To find an explicit solution to this problem in frequency domain, the inverse Fourier transform of the spectral domain Green's function is needed. For this purpose we introduce spherical coordinates, carry out the integration and use residual calculus for the integration over the radial distance [8]. The result from these steps is the solution to the photoacoustic wave equation in $(\mathbf{x},\mathrm{s})$ domain, given as

$$\hat{p}(\mathbf{x},s) = \frac{\Gamma}{c^2}s\int\limits_{\mathbf{x}'\in\mathbb{D}_H}\frac{\mathrm{e}^{-\gamma|\mathbf{x}-\mathbf{x}'|}}{4\pi\mid\mathbf{x}-\mathbf{x}'\mid}\hat{H}(\mathbf{x}',s)\mathrm{d}V \qquad (5)$$

Two approaches can be followed from here. Move to the frequency domain by taking $s = \mathrm{j}\omega$, or move to time domain by taking the inverse Laplace transform. If we consider the latter case, the solution to the wave equation based on the Green's function for lossless, homogeneous background is given in [9] as

$$p(\mathbf{x},t) = \frac{\beta}{4\pi C_p}\iiint\frac{\mathrm{d}\mathbf{x}'}{\mid\mathbf{x}-\mathbf{x}'\mid}\frac{\partial H(\mathbf{x}',t')}{\partial t'}\bigg|_{t'=t-\frac{|\mathbf{x}-\mathbf{x}'|}{c}} \qquad (6)$$

where x and x' denote the positions of the receiver and source respectively.

An important assumption, which is valid for soft tissue, is that the light pulse is short enough for thermal diffusion not to occur. This is referred to as thermal confinement. With this assumption, the delivered energy can be modeled as the product of a Dirac delta pulse and a spatially varying heating function. Then equation (6) is rewritten into a more explicit form, highlighting the received signal dependence on the initial pressure distribution p_0, as

$$p(\mathbf{x},t) = \frac{\partial}{\partial t}\left[\frac{t}{4\pi}\iint_{|\mathbf{x}-\mathbf{x}'|=ct}p_0(\mathbf{x}')\mathrm{d}\Omega\right] \qquad (7)$$

The key to image reconstruction is finding the initial pressure distribution from data recorded at different locations, outside the imaged volume, which is nothing else but the inversion of equation (7). This starting point to

image reconstruction has been used by Kruger *et al.* for filtered back-projection algorithms based on the Radon transform described in [10]. Xu *et al.* tested another algorithm, based on the Radon transform approximation with a Hilbert transform [11]. Other time-domain solutions include deconvolution algorithms [12] as well as back-projection and synthetic aperture algorithms borrowed from the ultrasound field. A model-based reconstruction approach was developed by Razansky *et al*. showing the advantages of numerical solutions [13].

Other researchers concentrated on the frequency domain algorithms. For example, Xu and Wang [14,15], developed exact frequency domain reconstruction algorithms for spherical, cylindrical and planar geometry. A more recent paper suggests that constructing an algorithm which includes the boundary conditions at the tissue-air interface might be a better choice, since this boundary is significantly affecting the received pressure. The suggested method uses a back-propagation algorithm to estimate the absorbers [16]. Cox *et al.* have proposed a fast method for calculating PA fields in liquids by applying wavenumber integral techniques from the seismic world [17].

If $s = \mathrm{j}\omega$ is substituted in Eq. (7) the explicit solution to the forward problem in frequency domain, discretized (using the mid-point rule) and rewritten as a data model for several receiver locations is given as

$$\hat{\mathbf{p}} = \hat{\mathbf{G}}\hat{\mathbf{H}} \tag{8}$$

where $\hat{\mathbf{p}}$ represents the received pressure in frequency domain for a linear array transducer, $\hat{\mathbf{G}}$ is the Green's function matrix and $\hat{\mathbf{H}}$ is a vector representing the sources.

Inverting this equation by applying the adjoint operator gives

$$\hat{\mathbf{H}} = \hat{\mathbf{G}}^{\mathrm{H}}\hat{\mathbf{p}} \tag{9}$$

where $\hat{\mathbf{G}}^{\mathrm{H}}$ is the hermitian transpose of the Green's matrix.

Equation (9) is a basic imaging procedure which is a computationally simple and stable tool for reconstructing images as it includes no matrix inverses. Although not as sophisticated as other PAI techniques, it can deliver accurate images with good quality which can be exploited in more complex algorithms. An example in-vivo image, showing a B-scan of a human forehand and underlying vasculature, reconstructed with the above imaging procedure can be observed in Figure 2. Notice that the strongest light absorbers are the skin and the blood vessels which contain the largest concentration of chromophores absorbing at 650nm.

III. METHODS

A. Instrumentation

The effective generation and registration of photoacoustic signals has also undergone extensive research, evolving in parallel to the image reconstruction.

The generation of photoacoustic signals is primarily achieved by two types of sources – powerful laser diodes capable of delivering short pulses (~100ns) with high pulse repetition rate (PRF) gravitating around 1kHz, and tunable NIR ND:YAG lasers with low PRF between 10-20Hz, but with very high energy output and very short pulse length (~30 mJ and ~10 ns respectively) [18].

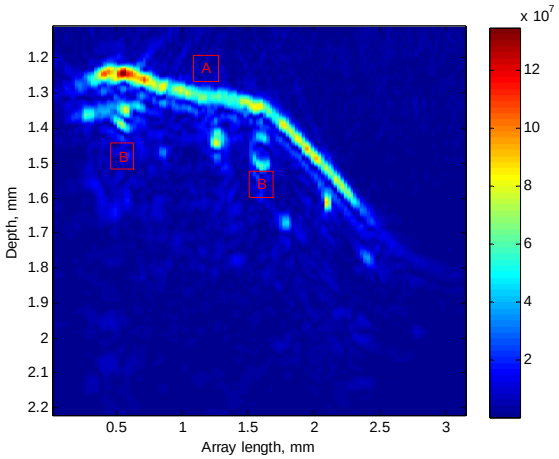

Fig. 2. Image of the skin surface and underlying blood vessels. The continuous strong signal is the skin (A), while the smaller round images are blood vessels (B).

Other laser system are also utilized, some custom build (using arrays of laser diodes at two different wavelengths) while some are commercially available and can deliver pulses with 6ns duration. In either of these cases, the goal is to achieve the conditions of stress confinement and thermal confinement.

Recently, multi-wavelength PAI systems are gaining considerable attention. Tunable NIR lasers have high power output, but are bulky and often require cooling. In comparison, laser diodes are small and do not require cooling, while achieving high PRF. This allows for signal averaging and is the reason why several laser diodes at different wavelengths are fused together with custom build transducers and used as a dual-imaging solution – PAI and ultrasound [19].

The generated photoacoustic signals tend to be very broadband spanning the 1-100MHz range. However, tissue is acting as a low-pass filter, limiting this range to several MHz, usually up to 10(30)MHz. This is still a very broad frequency band which is only partially covered by commercially available ultrasonic transducers (which are usually employed for PAI). They typically have a central frequency at several MHz and a high Q-factor.

However, as the field is maturing, array transducers specifically designed for PAI are emerging. For example, the Vevo 2100, VisualSonics, photoacoustic system is equipped with a linear array transducer (MS250) with fc= 21 MHz, consisting of 256 elements. Another example is the 30MHz piezo-composite linear array, which is a part of a custom build multi-channel receiver system [20].

B. Acquisition system

A typical acquisition system for photoacoustic imaging resembles any ultrasound system with the exception of the source – in photoacoustics it is a powerful EM wave emitter.

Several commercially available PAI systems have emerged in recent years. Some of these are the abovementioned Vevo 2100 from VisualSonics, another one is the Nexus 128 Preclinical Photoaocustic CT Scanner from Endra Life Sciences and the MSOT inSight / inVision by iThera Medical. As the field is rapidly expanding, more will definitely follow in the near future.

IV. Discussion and Conclusion

Although a rapidly developing field, photoacoustic imaging is still a relatively new technique which faces many problems from both technological and signal processing perspective.

Among all the challenges (and a major drawback) is the low signal-to-noise-ratio (SNR), intrinsic to the photoacoustic field. Apart from limiting the reconstruction accuracy (respectively diagnosis accuracy) it is also the major problem when we consider imaging depth. The most intuitive and easily achievable improvement here is averaging, which if applied over a sufficient number of acquisitions will mitigate noise and increase the SNR. This is why laser diodes are particularly attractive for PAI, as averaging over a few hundred samples can be easily achieved. Other methods for SNR improvement include averaging and normalization (L2 and L1 norm), different signal processing techniques (borrowed directly or modified respectively from other fields), as well as application of contrast agents for improved absorption [21].

From technological point of view, the major challenges include the design of broadband transducers and their integration with the light delivery system. Companies and international projects have successfully developed several such integrations with more following in the near future. An example is the MSOT system by iThera Medical [22] or the FULLPHASE project [19].

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Ranking of EEG Time-domain Features on the Negative Emotions Recognition Task

Firgan Nihatov Feradov and Todor Dimitrov Ganchev

Abstract – **The accuracy of automated emotion recognition depends on the quality of EEG signal descriptors. In the present contribution we report on an experimental evaluation of ten time-domain EEG signal descriptors with respect to their applicability to the task of negative emotions recognition. The ranking of these descriptors based on their estimated practical worth shows that the mean of the absolute values of the first difference of the normalized signal contributes for the highest recognition accuracy.**

Keywords – **Emotion recognition; Electroencephalography; EEG signals; Feature ranking.**

I. INTRODUCTION

In the last decade there is an increasing interest towards the detection of emotions from EEG signals. This is mainly due to the high demand for intelligent human-machine and brain-computer interaction interfaces, which are important part of information support, health care, and educational training applications.

Nowadays human-machine interaction technology is dominated by the statistical machine learning paradigm, which assumes the existence of datasets representative to the operational conditions of a certain application. These datasets are used for the creation of statistical model(s) representing each category of interest, or for the creation of discriminative classifiers. Given sufficient amount of representative data, the classification accuracy depends on the discriminative power of the classifier, but more importantly on the informative value of the signal descriptors fed to the classifier.

In the present work we carry out an experimental evaluation of various signal descriptors, based on the time domain EEG signal, and evaluate their applicability to the task of automated recognition of negative emotional states. In particular each descriptor from two widely-used feature sets is compared with its counterparts and with the short-time energy of an EEG signal, used as a feature [1-3].

Specifically, the first set of EEG features is the set designed by Bo Hjorth [4]. It consists of three features (*Activity*, *Mobility*, and *Complexity*) describing the amplitude, frequency, and shape of an EEG signal. In brief, *Activity* is defined as the amplitude variance of a signal. It is considered to have the necessary additive property to allow integration of different observations during the epoch into one representative figure. When computed the *Activity* has a high or low value if the high frequency components in the signal are few or respectively many. *Activity* corresponds to spectral analysis in the frequency domain. *Mobility* is calculated as the square root of the ratio between the variances of the first derivative and *Activity*, and represents the average of the frequency of the signal. This descriptor corresponds to the calculation of the standard deviation of a signal in the frequency domain. *Complexity* is a measure of details with reference to the curve shape of the sine wave.

Activity, *Mobility*, and *Complexity* were initially designed for the creation of EEG-based human-computer interfaces, but later on they have been proven universal and applicable to other tasks that rely on EEG signals, including the detection of emotional states from EEG signals [5].

The second set of features evaluated here was proposed by Picard et al. [6], who compared multiple algorithms for feature-based recognition of emotional states on a given set of data. Among these are six statistical descriptors, such as: (i) the means of the raw signal, (ii) the standard deviation of the raw signal, (iii) the means of the absolute values of the first and second differences of the raw signal, and (iv) the means of the absolute values of the first and second differences of the normalized signal. These descriptors were purposely designed for the emotion detection task and account for the physiological activity of the body and brain. These six descriptors were employed in related studies on emotion detection from EEG signals [7-9].

In Section II we outline the ten EEG descriptors evaluated in the present work. In Section III we describe the common experimental setup used in the feature performance evaluation study. In Section IV we provide details on the estimation of person-specific thresholds for the recognizer of negative emotional states. The experimental results are reported in Section V, and in Section VI we provide summary and concluding remarks.

II. FEATURE EXTRACTION

The EEG signal descriptors considered here are characterized with low complexity and all features are derived directly from the time-domain signal. In brief, first the EEG signal $x_i(n)$ is pre-processed for reducing the interference from muscular and eye movement activity, which results in the free of artefacts EEG signal $\hat{x}_i(n)$. Here the subscript *i* stands for the channel number. All channels are processed uniformly so in further discussion we drop the index *i* but it reminds implied. All features are computed for short frames of the EEG signal, obtained through a sliding window of 343.75 milliseconds which moves with a skip rate of 85.9 milliseconds. Successive frames overlap with 75%. Therefore, the total number of

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successive overlapping frames in a recording with N samples is:

$$P = fix\left(\frac{N-K+L}{L}\right), \quad (1)$$

where the operator *fix* stands for rounding towards the smaller integer number, L is the predefined step size in samples, and K is the frame size, also in samples. Next, for each frame we compute the EEG signal feature that is going to be evaluated, as follows:

a) Short-time energy:

$$E_p = \sum_{k=1}^{K} \hat{x}(k)^2, p = 1,2,...,P. \quad (2)$$

b) Mean value:

$$\mu_p = \frac{1}{K}\sum_{k=1}^{K} x(k),\ p = 1,2,...,P. \quad (3)$$

c) Standard deviation:

$$\sigma_p = \sqrt{\frac{1}{K-1}\sum_{k=1}^{K}(\hat{x}(k)-\mu_p)^2},\ p = 1,2,...,P. \quad (4)$$

d) The mean of the absolute values of the first difference of the signal (MAVFDS):

$$\delta_p = \frac{1}{K-1}\sum_{k=1}^{K-1}|\hat{x}(k+1)-\hat{x}(k)|,\ p = 1,2,...,P. \quad (5)$$

e) The mean of the absolute values of the second difference of the signal (MAVSDS):

$$\gamma_p = \frac{1}{K-2}\sum_{k=1}^{K-2}|\hat{x}(k+2)-\hat{x}(k)|,\ p = 1,2,...,P. \quad (6)$$

f) The mean of the absolute values of the first difference of the normalized signal (MAVFDNS):

$$\tilde{\delta}_p = \frac{1}{K-1}\sum_{k=1}^{K-1}|\tilde{x}(k+1)-\tilde{x}(k)| = \frac{\delta_p}{\sigma_p}, p = 1,2,...,P. \quad (7)$$

g) The mean of the absolute values of the second difference of the normalized signal (MAVSDNS):

$$\tilde{\gamma}_p = \frac{1}{K-2}\sum_{k=1}^{K-2}|\tilde{x}(k+2)-\tilde{x}(k)| = \frac{\gamma_p}{\sigma_p}, p = 1,2,...,P. \quad (8)$$

h) Activity:

$$Activity = \sigma_p^2 \quad (9)$$

i) Mobility:

$$Mobility = \frac{\sigma_d}{\sigma_p} \quad (10)$$

j) Complexity:

$$Complexity = \frac{\sigma_{dd}}{\sigma_d} / \frac{\sigma_d}{\sigma_p} \quad (11)$$

Next, statistical standardization of the calculated descriptors was performed, so that their distributions are normalized to zero mean value and unit standard deviation:

$$Z = \frac{D_p - \mu_p}{\sigma_p} \quad (12)$$

The mean value μ_p and the standard deviation σ_p are estimated for the feature of interest D_p and the process is repeated for each of the EEG channels. The subscript p is the frame index.

III. EXPERIMENTAL SETUP

The evaluation of the aforementioned ten EEG signal descriptors was carried out following a common experimental protocol, based on the Database for Emotion Analysis using Physiological signals (DEAP) [15]. All descriptors were computed from the same set of EEG signals. Each descriptor was used separately to create a classifier, which were tested on another dataset. All descriptors were ranked according to the recognition accuracy.

The DEAP database consists of recordings from thirty-two participants with a total of 40 recordings per participant. Each recording, made while the participants were watching musical video-clips, consists of 40 channels. These include 32 EEG channels, electromyographic (EMG), electrooculographic (EOG) and other channels, all taken from different parts of the head and the body. The dataset includes original and pre-processed recordings from these forty channels. Frontal face videos and detailed metadata for the participants are also included in the database. All EEG recordings were self-annotated by the subjects participating in the data collection.

The EEG recordings of 10 participants (with numbers № 2, 11, 17, 21, 22, 24, 28, 29, 30, 32) were selected for our experiments, based on the annotations of the EEG songs. We aimed at balance between the numbers of songs tagged as negative and positive for each participant. Each participant's data was split in three parts – training, development, and testing dataset, which consist of 20%, 20%, and 60% of the available recordings. However, depending on the distribution of song ratings for each participant, these percentages varied up to 5%. This led to roughly 8 to 9 recordings used for training, 8 to 9 recordings used for development, and 22 to 24 recordings used for testing, for each participant. The total number of test recordings is N_{rec}=227.

The split of recordings into these three datasets was performed in the following way: The dataset of each participant was split into two groups – *negative* and *non-negative* – depending on the like/dislike rating of the recording. Each rating provided in the database indicates the personal preferences of the participant. The like/dislike rating's range is from 1 to 9, where 1 corresponds to the lowest rating (*disliked*) and 9 is the highest rating – *liked*. In the current experiment, recordings which had like/dislike rating of 4 or lower were tagged as *negative*, while recordings with rating higher than 4 were tagged as *non-negative*. In few cases when the number of definitely tagged recordings was not sufficient a 5% tolerance was applied to the separation threshold. All EEG recordings for the selected participants were used during the experiments, which totals to 400 EEG recordings.

The classification performance of the trained models is evaluated in terms of percentage correct detections:

$$correct = \frac{H}{N_{rec}} \times 100, [\%] \quad (13)$$

In all experiments we trained an SVM classifier with radial basis function kernel. In order to find out the optimal training parameters for every emotion classifier, a series of grid searches were implemented on the development dataset. Grid searches were carried out for each of the individual descriptors, for each participant. In particular, the adjustable parameters of the SVM tuned during the grid search were:

- *boxconstraint* – the box constraint *C* for the soft margin, where *C* is a positive numeric scalar or a vector.
- *rbf_sigma* – a positive number specifying the scaling factor in the Gaussian radial basis function kernel.

The grid searches ranged between 0.1 and 100 for both parameters. The optimal values found during the grid search were used during the evaluation of each detector. A total of 200 grid searches were conducted.

IV. Detection of Negative Emotions

The evaluation of the features is conducted through the use of a detector of negative emotional states, presented in [1], which is based on the following principle:

The training data set, composed of the most indicative examples of negative and non-negative recordings, was used to train a person-specific SVM classifier. The model, generated this way, was then tuned on the development dataset, so that a person-specific decision threshold *Tr* can be computed:

$$Tr = \frac{\frac{1}{n}\sum_{f=1}^{n} D_{neg,f} + \frac{1}{m}\sum_{l=1}^{m} D_{pos,l}}{2}, \quad (14)$$

where D_{neg} and D_{pos} are the portions of development data consisting of *n* recordings with negative tags and *m* with non-negative tags (neutral or positive).

During the evaluation of each classifier, the threshold (14) was used for making a decision for each recoding. The person-specific recognition accuracy for each individual descriptor was computed based on the results for all recordings.

V. Experimental Results

Based on the common experimental setup, described in Section III, we performed a comparative study of the ten EEG descriptors. The experimental results are presented in Tables 1 and 2. In Table 1 we present the averaged classification accuracy for each individual descriptor and in Table 2 the results per participant.

In Table 1 a comparison between the recognition results, observed for each feature is shown. The first column shows the feature name, whereas the features are ordered in descending order with respect to their performance – the feature that had highest average accuracy is placed first, while the feature with lowest average accuracy is respectively placed last, on the bottom of the table. The second column shows the highest classification accuracy, observed for each feature, while in the third column the lowest achieved accuracy is shown. In the fourth column we present the average accuracy observed for each feature. In the fifth and final column we can see the percentage of successful classifications. This comparison is made, because in some cases the trained models were not able to correctly classify the signals and reach a solution for the given task.

TABLE 1. CLASSIFICATION ACCURACY ACHIEVED BY THE FEATURES

Feature name	***Max accuracy***	***Min accuracy***	***Mean accuracy***	***Successful classification***
MAVFDNS	87.0 %	59.1%	68.7 %	90 %
MAVSDNS	82.6 %	58.3%	68.6 %	80 %
Mobility	75.0 %	59.1 %	67.0 %	90 %
MAVSDS	73.9 %	59.1 %	66.6 %	100 %
Complexity	78.3 %	59.1 %	66.0 %	90 %
Energy	81.8 %	58.3 %	65.7 %	100 %
Activity	70.8 %	59.1 %	64.0 %	80%
MAVFDS	68.2 %	54.5 %	63.8 %	100 %
St. deviation	68.2 %	59.1 %	63.4 %	100 %
Mean value	72.7 %	59.1 %	62.9 %	90%

As presented in Table 1, we observed the highest classification accuracy for the mean of the absolute values of the first and second differences of the normalized signal (MAVFDNS and MAVSDNS), equal to 68.7% and 68.6%. Overall, the more complex of the six statistical features displayed higher classification capabilities, while the simpler statistical features were not as descriptive, with *Mean value* and *Standard deviation* having the lowest classification accuracy (63.4% and 62.9%) among all descriptors considered here. A performance division, based on the complexity of the feature can also be observed in Hjorth's set of features, where *Complexity* and *Mobility*, also performed well with mean accuracy of 67% and 66% respectively, while the mean accuracy of the *Activity* parameter was 64%.

In Table 2 we present detailed information about the recognition accuracy observed for each individual descriptor, on the dataset of the particular participant. The cases, in which the classifier failed detect the data correctly are marked with "X".

Although most of the examined features showed similar performance, some variations did exist. One such example are Hjorth's descriptors, which were computationally expensive but led to an increase in the recognition accuracy. Another case where difference in performance was observed was during classification with *Mean value* as a descriptor. This feature showed performance inconsistencies and the recognition accuracy varied greatly, depending on the grid searched parameters, used for the creation of the SVM classifier.

VI. Conclusions

A study of the applicability of ten time-domain features and their informative value with respect to classification accuracy capabilities was carried out on the DEAP dataset. We ranked these features with regard to the recognition accuracy.

TABLE 2. CLASSIFICATION ACCURACY OF THE EVALUATED DESCRIPTORS PER PARTICIPANT.

Features:	***Par. 02***	***Par. 11***	***Par. 17***	***Par. 21***	***Par. 22***	***Par. 24***	***Par. 28***	***Par. 29***	***Par. 30***	***Par. 32***
Mean Value	66.3 %	68.2 %	59.1 %	60.9 %	X	72.7 %	62.5 %	56.5 %	60.9 %	59.1 %
St. Deviation	61.6 %	59.1 %	68.2 %	60.9 %	68.2 %	59.1 %	62.5 %	65.2 %	65.2 %	63.6 %
MAVFDS	61.6 %	54.5 %	68.2 %	65.2 %	68.2 %	63.6 %	66.7 %	56.5 %	69.6 %	63.6 %
MAVFDNS	66.3 %	X	68.2 %	65.2 %	68.2 %	63.6 %	62.5 %	78.3 %	87.0 %	59.1 %
MAVSDS	66.8 %	63.6 %	72.7 %	65.2 %	72.7 %	68.2 %	62.5 %	60.9 %	73.9 %	59.1 %
MAVSDNS	61.6 %	63.6 %	72.7 %	X	63.6 %	68.2 %	58.3 %	82.6 %	78.3 %	X
Activity	56.3 %	59.1 %	59.1 %	X	68.2 %	X	70.8 %	65.2 %	65.2 %	68.2 %
Mobility	61.6 %	63.6 %	68.1 %	X	63.6 %	68.2 %	75.0 %	73.9 %	69.6 %	59.1 %
Complexity	61.6 %	68.2 %	59.1 %	X	63.6 %	68.2 %	62.5 %	78.3 %	73.9 %	59.1 %
Energy	58.3 %	59.1 %	63.6 %	69.6 %	68.2 %	81.8 %	66.7 %	60.9 %	69.6 %	59.1 %

The highest average accuracy was achieved with the mean of the absolute values of the first differences of the normalized signal (MAVFDNS) – 68.7%. The feature with the lowest average accuracy was mean value – 62.9%. Also, the observed results indicate an absolute increase in recognition accuracy with 0.9%, when compared to the results reported in previous related work [2].

The future research will aim at improvement of the recognition accuracy of negative emotions from EEG signals, based on combinations of the most discriminative descriptors.

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Simulation Model of PVDF Piezoelectric Transformer for Medical Applications

Orlin Plamenov Stanchev

Abstract – **The current paper proposes a simulation model of piezoelectric transformer model that utilizes the Polyvinylidene Fluoride (PVDF) material. Its piezoelectric properties and medical applications are still being researched and minor information about such model is present. The available models for conventional transducer are compared and adaptation is proposed. The piezoelectric transformer model is described and its parameters are discussed. A PSpice simulation and laboratory experiment are accomplished. The results are compared and discussed.**

Keywords –**piezoelectric transformer, PVDF, transducer model, energy transfer**

I. INTRODUCTION

The piezoelectric transformers have numerous advantages like compact shape (low height) and high efficiency due to the native driver circuit soft switching [1]. They are used for high voltage step-up applications with capacitive load. Normally PZT material is used in multilayer transformer structures. The piezoelectric transformers transfer energy using mechanical acoustic wave that propagates to small distances up to few centimeters without significant energy loss. They also obtain low EMI and can be used for powering small sensitive to interference electronic devises or for charging small batteries from distance. These qualities could be meaningful for medicine for implantable devices such as pacemakers, implantable defibrillators, brain 'Pacemakers' for Alzheimer, cochlear implants etc. In some cases the battery life is few years on account of occupying most of the volume in the device housing. Miniaturization requires smaller battery that needs to be recharged and coils with electromagnetic waves are not always the solution because they can influence sensitive electronics or cause unwanted effects on human body. Piezoelectric transformer, working with acoustic waves within the safe regulations, can be the proper solution.

The acoustic wave propagation medium between the primary and secondary transducers in the medical piezoelectric transformer is the human tissue. The acoustic impedance of the human skin is *1.99 MRayl*, bones - *5.32 MRayl* [2] and of the ordinary transducer material which is lead-zirconate-titanate (PZT) - *39.71 MRayl*. The mismatching of impedances causes energy reflection that can be major problem especially for the energy receiving unit. Therefore polyvinylidene fluoride (PVDF) is used as it has acoustic impedance equal to *2.7 MRayl* (close to human tissue and water), develops high piezoelectric activity and is flexible and tough.

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The PVDF material is extruded into thin piezo film with typical thickness between *9* and *110 μm*. Electrodes are made of silver ink [3] and piezo film elements are laminated with Mylar film [4]. All these materials are compatible with the human body and are not rejected normally.

This paper focuses on PVDF piezoelectric transformer that utilizes thickness mode vibrations. It can be considered as one or multiple transduces that transmit acoustic waves and one or multiple transduces that receive these waves. Therefore conventional piezoelectric transducer models can be used, employing electroacoustic analogous circuits for analysis of the electro-mechano-acoustics. Normally piezoelectric transformers are described using electromagnetic transformers [1] and Mason's transducer model [5]. Other option is the KLM model [6]. They are powerful tools for conventional piezoelectric transformers but they become difficult to adjust when different layers are present between the primary and secondary elements or when multiple transducer elements are used. On other hand transmission lines are useful for modelling multilayered structures where piezoelectric and non-piezoelectric layers are present. Such models are proposed by Redwood [7] and Leach [8].

This article presents a model of PVDF piezoelectric transformer that employs Leach's model because of the use of transmission lines for the mechanical analogous circuit and controlled source technique for connection between the mechanical and electrical parts. The model is implemented in the circuit simulator PSpice, which is a part from the OrCAD software tool suite [9], where driver circuit and secondary side electronics can be included to the model.

II. MODEL THEORY

The PVDF piezoelectric transformer consists of primary and secondary piezoelectric elements that will be considered as transducers. The primary side transducer performs electrical to mechanical conversation and the secondary side – mechanical to electrical.

Ultrasonic transducers operate at wide frequency range, therefore the high frequency approximation of the transducer model should be accurate enough for the whole operational range. This is hard to obtain for materials with low quality factor Q because the difference between the model and the exact solution became unacceptable. So the acoustic losses in the material must be taken into account and lossy transmission lines should be used. Some materials like the piezoelectric polymer film have frequency dependent dielectric parameters and Q factor so that the film capacitance and lossy transmission line resistive parameter varies. However the piezoelectric transformer operates at fixed sinusoidal frequency and the

PVDF lossy transmission line parameters and the piezo-film element capacitance can be accurately determined.

Leach's thickness-mode transducer model is used, because the acoustic wave propagates in direction of the film's thickness which is also the direction of the electric field (electrodes are printed on both sides of the film).

For the presented simulation model the following assumptions and simplifications are made: the piezoelectric transformer model operates only in one direction as the energy flows from primary to secondary side; the acoustic wave propagates only in one dimension; the amplitudes are small enough to work in linear regions of components.

The Leach's model consists of mechanical and electrical analogous circuits representing the electro-mechano-acoustic system.

A. Mechanical analogous circuit

The equations, describing the one-dimensional compressional acoustic wave of piezoelectric transducer, can be modified to the form of telegraphist's equations [8]. Therefore the mechanical behavior of the PVDF transducer is described with a mechanical analogous circuit which is represented by a lossy transmission line, given on Fig. 1. The lossy transmission line can be modeled with lumped segments, consisting of series inductance L' and resistance R' per unit length, and parallel capacitance C' and conductance G' per unit length [10].

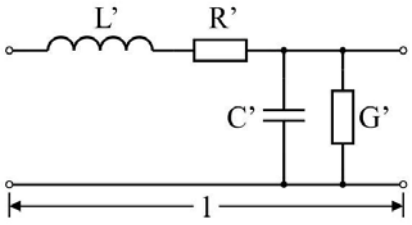

Fig. 1. Lossy transmission line

An impedance type analogy is chosen so that the mechanical force is represented by voltage and the particles velocity is represented by current. The inductance per unit length *L' [H/m]* and capacitance per unit length *C' [F/m]* are given by Eq. 1 and Eq. 2:

$$L' = \rho \cdot A \tag{1}$$

$$C' = \frac{1}{c^2 \cdot \rho \cdot A}, \tag{2}$$

where ρ is the density *[kg/m^3]* and c is the speed of sound *[m/s]* in the PVDF material, and A is the cross sectional area *[m^2]* of the acoustic beam.

The acoustic coefficient of attenuation α *[Np/m]* for frequency dependent materials like PVDF is given by Eq. 3:

$$\alpha \approx \frac{\omega \cdot \sqrt{L \cdot C}}{2 \cdot Q_M}, \tag{3}$$

where ω *[rad/s]* is the angular frequency and Q_M is the mechanical quality factor. The attenuation of the acoustic waves is represented by resistance per meter *R' [Ω/m]* which is given by Eq. 4:

$$R' = 2 \cdot \rho \cdot c \cdot A \cdot \alpha \tag{4}$$

The conductance per unit length *G [S/m]* is considered to be *0* and the transmission line length *l* is given in *[m]*.

B. Electrical analogous circuit

The electrical analogous circuit and the lossy transmission line of the primary side transducer are given on Fig. 2.

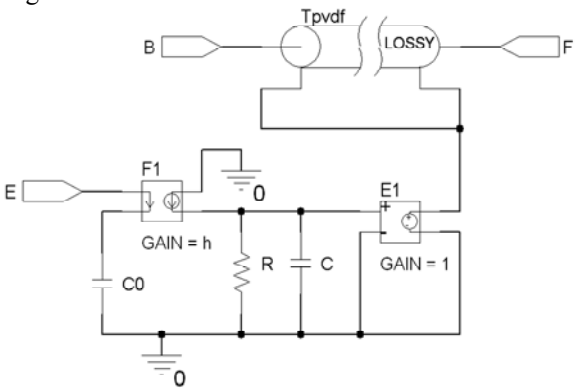

Fig. 2. Primary side transducer schematic

The transducer front and back sides are represented by ports 'F' and 'B' and the electrical port by 'E'.

The capacitance of the primary piezoelectric element is represented by capacitor C_0 and is given by Eq. 5:

$$C_0 = \frac{\varepsilon_S \cdot A}{d}, \tag{5}$$

where ε_S *[C^2/N·m^2]* is the dielectric permittivity at zero or constant strain, *A [m^2]* is the surface area of the electrodes (normally same as cross sectional area of the acoustic beam) and *d [m]* is the distance between the electrodes (normally the same as the transmission line length *l*). The dielectric permittivity of PVDF material is determined from Eq. 6:

$$\varepsilon_S = \varepsilon_R \cdot \varepsilon_0, \tag{6}$$

where ε_0 *[C^2/N·m^2]* is the dielectric permittivity of vacuum and ε_R is the frequency dependent relative permittivity of PVDF material, found from Fig. 3.

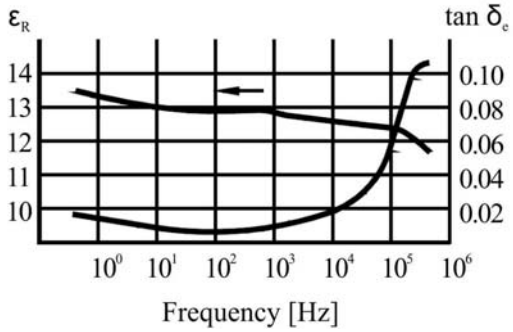

Fig. 3. Dependence of dielectric permittivity and dissipation factor of PVDF versus frequency [3]

The connection between the electrical and mechanical analogous circuits is accomplished with the current controlled current source *F1* with gain that is equal to the transmitting constant *h [N/C]* and is given by Eq. 7:

$$h = \frac{e_{33}}{\varepsilon_S}, \tag{7}$$

where e_{33} *[C/m²]* is the piezoelectric stress constant.

The resistor *R* and capacitor *C* integrates the current from *F1* and the unity gain voltage controlled voltage source *E1* isolates the integrator.

The electrical analogous circuit and the lossy transmission line of the secondary side transducer are given on Fig. 4.

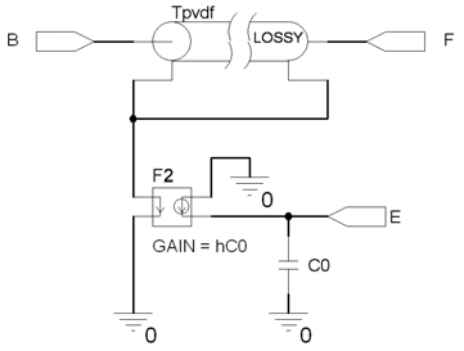

Fig. 4. Secondary side transducer schematic

The capacitance C_0 of secondary piezoelectric element is determined similarly from Eq. 5. The connection between the mechanical and the electrical analogous circuits is accomplished by current controllable current source *F2* with gain equal to the product of *h* and C_0.

III. Model Implementation

The proposed simulation model of PVDF piezoelectric transformer is implemented in PSpice (Fig. 5). The primary side transducer circuit is placed in hierarchal block *Primary Transducer* and the secondary side transducer circuit – in hierarchal block *Secondary Transducer*. The transducers' coating is represented by transmission lines *Tmyl* and the water medium – by *Twat*. The transducer backing that reflects the acoustic wave and is accomplished with aluminum plates [11][12], is represented by resistors *RAl*. The resistance is given in Eq 8:

$$R = Z_0 \cdot A, \tag{8}$$

where Z_0 is the acoustic impedance of aluminum.

The physical properties of the used materials in the PSpice simulation are summarized in Table 1.

TABLE 1. PHYSICAL PROPERTIES OF MATERIALS

Parameter	PVDF	Mylar	Water	Al
ρ [kg/m^3]	1780	1180	998.2 @ 25°C	2700
c [*m/s*]	2200	2540	1482.4 @ 25°C	6420
Q_M	13	30	-	-
ε_S [*pF/m*]	106-113	-	-	-
α [*Np/m*]	-	-	0.205 @ 500kHz	-
Z_0 [*Mrayl*]	2.7	3.0	1.48	17.33

The PVDF transducer has capacitive nature so that high *di/dt* causes very high initial currents. The combination with constant transmission mode when working as transformer causes failure of the thin electrodes and the connectors caused by the high local currents. As a result sine wave transducer excitation is used that also facilitates to determine the PVDF transmission line parameters. It is accomplished with sine voltage source *V1*.

The PVDF film transducer elements both for primary and secondary sides are FLDT1-028K piezoelectric film elements [4] with active film (electrode) area - 12 mm wide and 30 mm long. The film size is 28 μm having thickness mode resonance at frequency 39.28 MHz due to Eq. 9:

$$f_r = \frac{c}{2 \cdot d} \tag{9}$$

However the simulation model operational frequency is *500 kHz* because it is much easier to obtain in laboratory environment for experimental validation.

The 'Time Domain' PSpice simulation results are shown on Fig. 6 and simulation model parameters are given in Table 2.

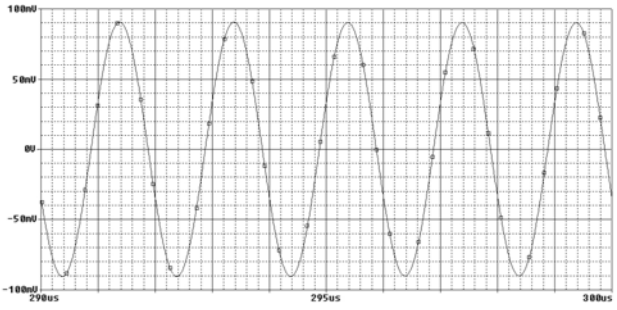

Fig. 6. Voltage over resistor *Rload* vs. time in PSpice

The piezoelectric transformer output voltage, developed over *1 kΩ* load resistor, has 'pure' sine wave shape with amplitude about 90 mV.

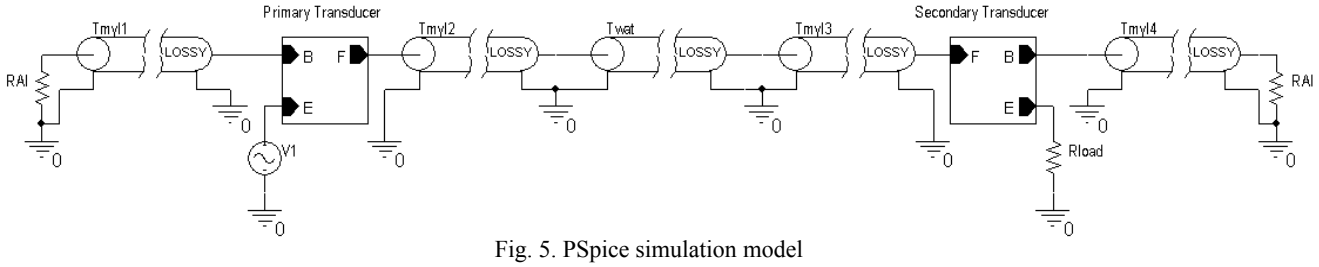

Fig. 5. PSpice simulation model

TABLE 2. SIMULATION MODEL PARAMETERS

Element	Parameters
Tpvdf	C = 322.4n, G = 0, L = 640.8m, LEN = 28u, R = 154.8k
C0	Value = 1.343n
F1	GAIN = 1.256e9
F2	GAIN = 1.687
E1	GAIN = 1
R	Value = 1k
C	Value = 1
V1	FREQ = 500kHz, VAMPL = 100V
Rload	Value = 1k
RAl	Value = 6.239k
Tmyl	C = 324n, G = 0, L = 486m, LEN = 88u, R = 50.9k
Twat	C = 1266n, G = 0, L = 359.3m, LEN = 15m, R = 6.6

IV. VALIDATION

To validate the PSpice model a physical experiment is accomplished. The experimental setup is given on Fig. 7

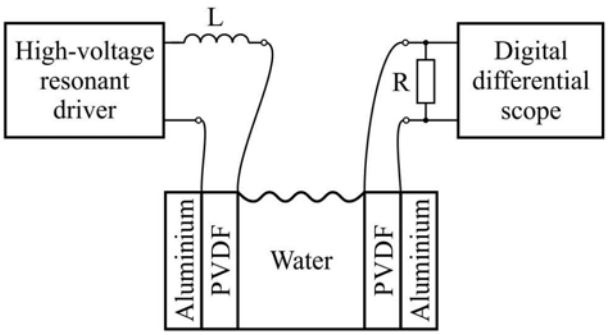

Fig. 7. Experimental setup

The two PVDF film elements (FLDT1-028K) are glued with epoxy onto vertical aluminum plates which are fixed in water environment on 15 mm distance. The primary transducer excitation is accomplished with high-voltage resonant driver and series inductor which together with the piezo-film capacitance creates LC resonant circuit, so that sine voltage with boosted amplitude is obtained.

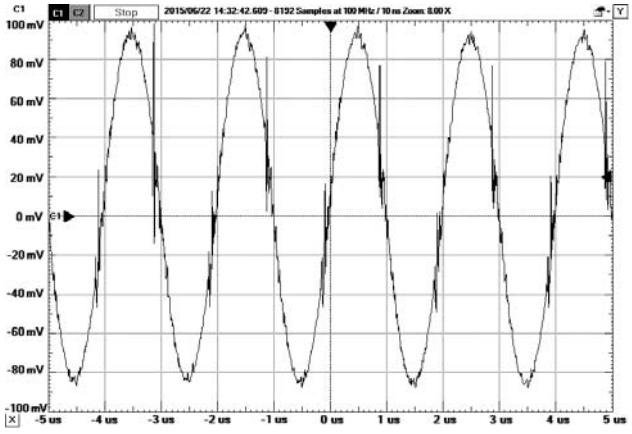

Fig. 8. Voltage over load resistor vs. time in experimental setup

The load is realized with carbon film resistor and the output voltage is digitalized and measured with battery powered digital differential scope 'Analog Discovery ™' of DIGILENT Inc. [13]. The experimental results are shown on Fig. 8. The piezoelectric transformer output voltage, developed over *1 kΩ* load resistor, has sine wave shape with moderate noise and amplitude about *90 mV* and *10 mV* positive offset, which is very similar to the simulation results.

V. CONCLUSION

The proposed PVDF piezoelectric transformer model in PSpice is a powerful tool for accurate simulation of the electrical energy transfer trough human tissue and other biological and non-biological media. The model can be used for evaluation of the potential and design of PVDF piezo-electric transformer for specific medical applications. The model is limited due to frequency variation and waveform but provides freedom for multi-material and multilayer designs.

ACKNOWLEDGEMENTS

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Graphical Representations for Analog IC Design in Deep and Ultra-Deep Submicron CMOS

Emil Dimitrov Manolov

Abstract – **The paper presents a set of simulation experiments for characterization and graphical representation of the performance of deep and ultra-deep submicron CMOS transistors. The aim is to propose a general approach for illustration of the basic capabilities and limitations of tested CMOS technologies. The results are used to determine the bias conditions and the sizes of the transistors in analog integrated circuit design.**

To this goal the key figures of merit for characterizing of CMOS technologies are discussed and test circuits for their examination by simulation are presented. The test circuits are applied for study of 45nm ultra-deep submicron CMOS technology. The obtained results are analyzed and recommendations and simple rules of thumbs for application of the presented approach in practice are given.

Keywords – **submicron CMOS, figure of merit, intrinsic gain, unity gain frequency**

I. Introduction

Reducing the channel length of the transistors is the leading trend in modern CMOS technologies. Table 1 shows the evolution of submicron CMOS technologies over the past 30 years [1, 2].

TABLE 1. EVOLUTION OF SUBMICRON CMOS TECHNOLOGIES

Type	Period	Channel length
Submicron	1985 - 1995	1µm>L_{min}>0.35µm
Deep submicron	1995 - 2003	0.35µm>L_{min}>0.1µm
Ultra-deep submicron	2003 - 2015	0.1µm >L_{min}>0.01µm

The reduction of the channel length of the transistors complicates the hand calculation models and hence the procedures of analog circuits design. The designer has to comply with a number of emerging effects and dependencies. They are studied in detail in the literature and as a result are described by complex expressions, which usually serve as guidelines in initial design [3, 4, 5]. Increasingly the designer's experience becomes a decisive factor in the design. Currently, the design of analog circuits combines the requirements for thorough knowledge of the physical phenomena and processes in semiconductors, the opportunity to work with abstract patterns and creativity to balance between the requirements and the limitations of performance. Analog design becomes a symbiosis between cutting-edge science and art.

In this situation, the task of teaching design of analog integrated circuits becomes extremely complex and responsible. Inexperienced trial-and-errors approach leads to longer design times and usually ends with redesign. Hence beginner designers should be directed consistently and with small steps towards mastering successful strategies and approaches to design.

In most analog applications, MOS transistor is used as an amplifier. To this end, it works in the field of saturation, where U_{GS}-U_T <U_{DS}. The first task that must be solved in the design of analog integrated circuits is to choose two main design parameters – gate-source voltage U_{GS} and channel length L. This is done intuitively by skilled designers, based on their experience, gained in development of many projects with different technologies. Students and beginners, however, require additional information to summarize and visualize in a compact form characteristics, capabilities and limitations of each particular used technology. Examples of such information are graphical represented figures of merit.

The paper presents a set of simulation experiments for characterization and graphical representation of the performance of deep and ultra-deep submicron CMOS transistors. The aim is to propose general approach for illustration of the basic capabilities and limitations of tested CMOS technologies. The results can be used to determine the bias conditions and the sizes of the transistors in analog integrated circuit design.

To this goal, key figures of merit for characterizing of CMOS technologies are discussed and test circuits for their examination by simulation are presented. The test circuits are applied for study of 45nm ultra-deep submicron CMOS technology, presented in [2] with BSIM4 model card for bulk CMOS. The obtained results are analyzed and recommendations and simple rules of thumbs for application of the presented approach in practice are given.

II. Basic Performance Indicators for CMOS Technologies Characterization

The selection of optimal channel length of the transistors is the key decision in initial phase of the design of analog integrated circuits. The channel length is an important factor that determines the operating area, unity-gain frequency and intrinsic (open loop) gain. The next step in the design procedure is determination of bias conditions and sizing of transistor's width.

Fig. 1 presents the transconductance of 45nm nMOS transistor in saturation ($L=2L_{min}$=90nm, W=1µm, $U_{DS}=U_{DD}$=1V) versus gate source voltage U_{GS}.

The plot can be divided in three regions of operation [6, 7]: subthreshold or weak inversion (wi) – U_{GS} from 0 V up to 450 mV and g_m from 0 µA/V up to 230 µA/V; square-law or strong inversion (si) – U_{GS} between 450 mV and 620 mV and g_m between 230 µA/V and 925 µA/V; velocity saturation (vs) – U_{GS} above 620 mV and g_m from 925 µA/V up to 1.3 mA/V.

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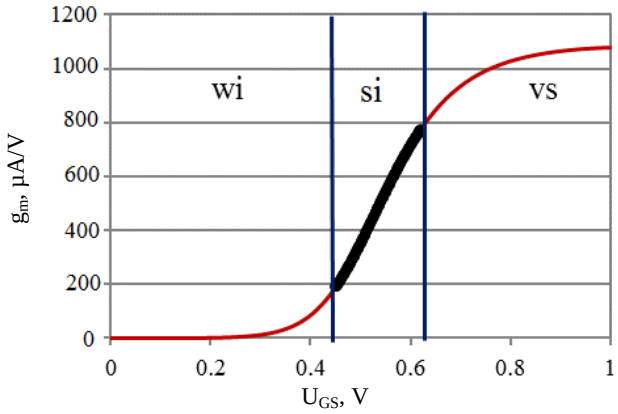

Fig. 1. Transconductance g_m, µA/V vs. gate-source voltage U_{GS},V.

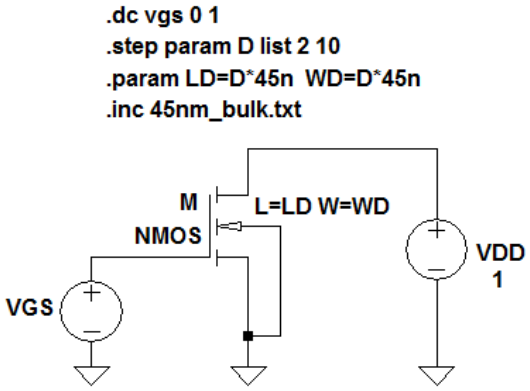

Fig. 2. Test circuit for study g_m vs. L and U_{GS}.

The weak inversion is characterized with small currents. The operation in this region is appropriate for very low-power analog applications [8]. The main disadvantage is the low-speed.

Velocity saturation occurs at high gate-source voltages. It can be modeled by adding a source degeneration resistor towards the transistor [1, 9]. The operation in this region is used only when very high speed is required. Then the transistors have to be with low sizes in order to ensure minimal parasitic capacitances.

The classical analog design is performed in central area of strong inversion [7, 10], where the drain current is directly proportional to the square of the effective voltage $U_{eff}=U_G-U_T$ and the transconductance g_m versus $U_{eff}=U_G-U_T$ is linear. In modern short channel technologies this sector is very narrow (reduced overdrive voltage), which complicates the design. One of the purposes of our study will be the examination of how the use of a channel, which is larger than the minimum allowed lengths Lmin, helps to minimize the velocity saturation and enlarges square-law region.

Another key indicator is the unity-gain frequency [7, 9, 10]. Generally it is well known that unity-gain frequency is directly proportional to the gate overdrive voltage and inversely proportional to the square of the channel length, but in the design it is important to know the specific nature of these features for the particular technology used.

The intrinsic gain presents the maximum possible small-signal low frequency gain of the transistor [7, 9, 10]. It is a function of the overdrive voltage and the channel length.

The above discussed characteristics and indicators lead to the conclusion that the channel length and the gate-source biasing voltage U_{GS} are the basic parameters, which determine the performance of the designed circuits. Our goal is to give a procedure for creation of appropriate charts which illustrate the described relations and are a basis for successful electrical design and sizing of analog integrated circuits.

III. Examination and Visualization of Basic Performance Indicators

A. Transconductance g_m versus channel length L and gate-source voltage U_{GS}

Fig. 2 presents the test circuit for study transconductance g_m vs. channel length L and gate-source voltage U_{GS}.

The simulations are carried out by using LTspice [11]. W/L ratio at all simulations remains 1. The obtained results are shown on Fig. 3. It can be concluded that increasing the channel length of the transistor leads to widening of the field of strong inversion. For example, increasing the channel length from 2·Lmin to 10·Lmin expands the strong inversion region by more than 200 mV. Unfortunately, as we shall see later, this possibility is limited due to reduced bandwidth and increased surface area of the chip.

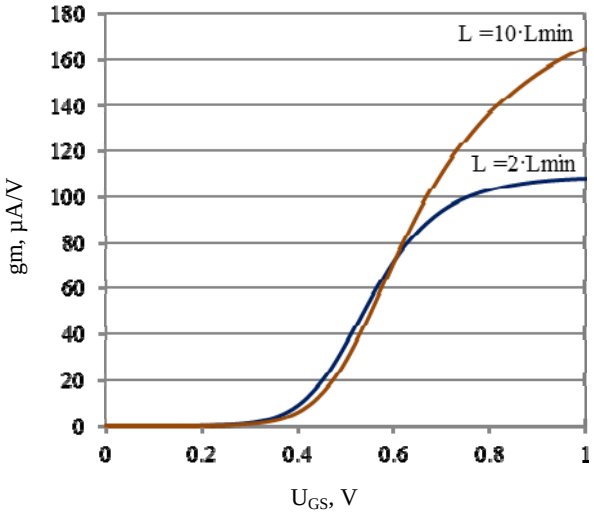

Fig. 3. Transconductance g_m vs. L and U_{GS}.

B. Unity gain frequency f_u versus channel length L and gate-source voltage U_{GS}

Fig. 4 shows the test circuit for examination of unity-gain frequency f_u versus channel length L and gate-source voltage U_{GS}. For this purpose, series of simulations were carried out with an argument L at different values of the parameter U_{GS} and W/L=1.

Fig. 5 presents the results of the simulations. The highest values of the unity-gain frequency are obtained at short channel (L=2·Lmin) for values of U_{GS} in velocity saturation. In strong inversion the frequency f_u depends almost linearly on the bias point (gate-source voltage U_{GS}), while in the velocity saturation f_u practically does not change. In strong inversion the frequency f_u is inversely proportional of the square of the channel length L, while in the velocity saturation this relation is weaker.

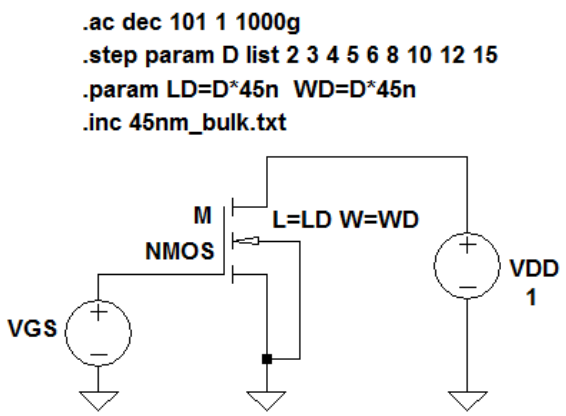

Fig. 4. Test circuit for study f_u vs. L and U_{GS}.

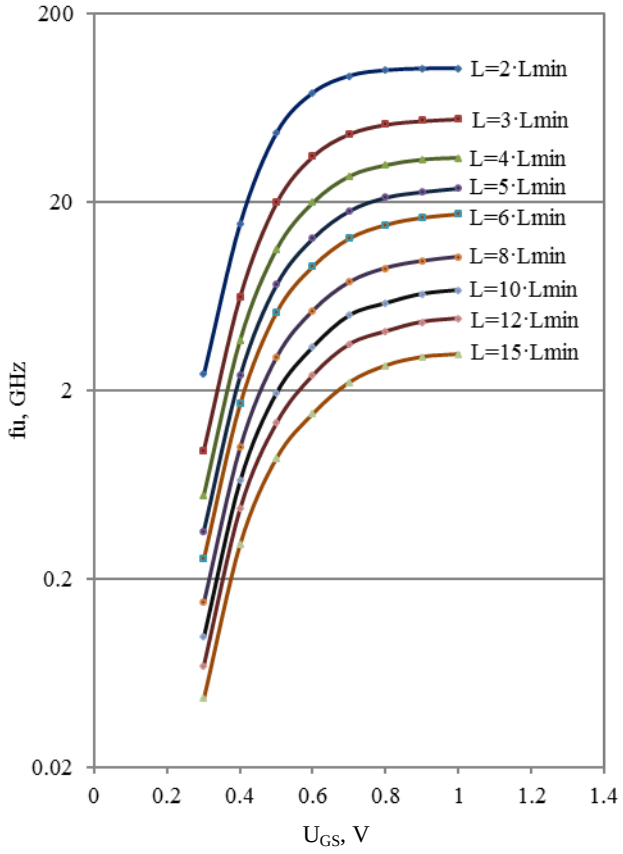

Fig. 5. Unity gain frequency f_u vs. L and U_{GS}.

C. Intrinsic gain A_u versus channel length L and gate-source voltage U_{GS}

The proposed test circuit for simulation of the intrinsic gain of the transistor is shown on Fig. 6. The parameter S is set of 1, so W / L is 1 again. To provide an open AC circuit, an ideal current source F1 is used as a load. To obtain an adequate result, the currents through examined transistor M and the load F1 have to be equal. To this aim an additional transistor M1, identical with M, is used. Because of the same U_{GS} voltage of both transistors, the current through M1 is equal to the current through M. The input of current controlled current source V-F1 is a load to the M1. Hence, because the current transfer coefficient is 1, the current through F1 is equal to the current through V and consequently to currents through M1 and M.

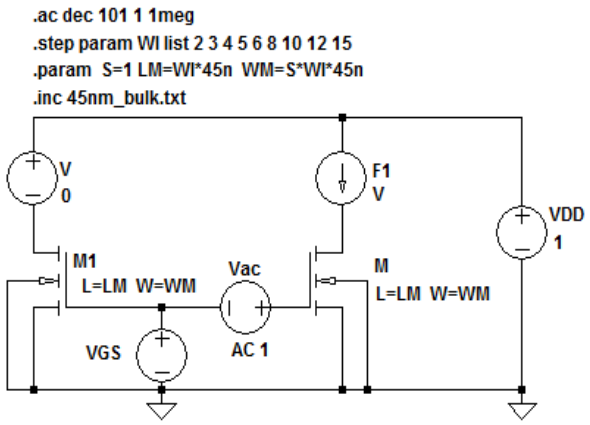

Fig. 6. Test circuits for study A_u vs. L and U_{GS}.

The results from simulations are generalized on Fig. 7. As long as the channel length L is larger, the intrinsic gain A_u is greater. The maximum gain is obtained with a voltage between 0.45 V and 0.55 V, i.e. when the transistor is in strong inversion (see Fig. 1). The values of maximum are from 60 (when L=2·Lmin), up to 440 (when L=15·Lmin).

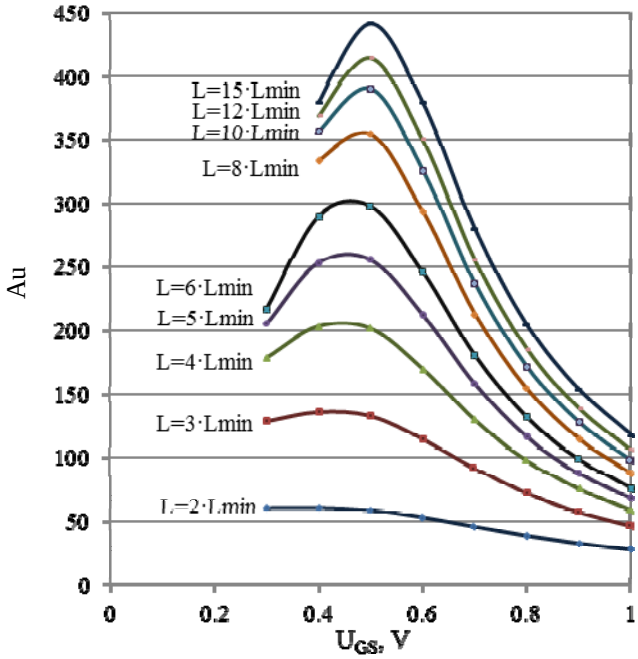

Fig. 7. Intrinsic gain A_u vs. L and U_{GS}.

D. Gain product versus channel length L and gate-source voltage U_{GS}

The presented Fig. 5 and Fig. 7 show one of the big trade-off in the analog circuit design – for high unity-gain frequency f_u the channel length L have to be smaller, while for a big intrinsic gain A_u the channel length L have to be larger. Therefore, we can never achieve both maximum gain and bandwidth of an amplifier – if the frequency increases, the gain decreases and vice versa.

Another figure of merit that is useful to evaluate practically different amplifier circuits is the gain-to-unity-gain frequency product $A_u \cdot f_u$ [10]. This quantity is presented on Fig. 8, where gate-source voltage U_{GS} is argument and channel length L is parameter. It is obtained

through multiplication of the results of simulation of unity-gain frequency f_u and intrinsic gain A_u for different values of channel length L and gate-source voltage U_{GS}. As long as the channel length L is larger, the gain-to-unity-gain frequency product $A_u \cdot f_u$ is smaller.

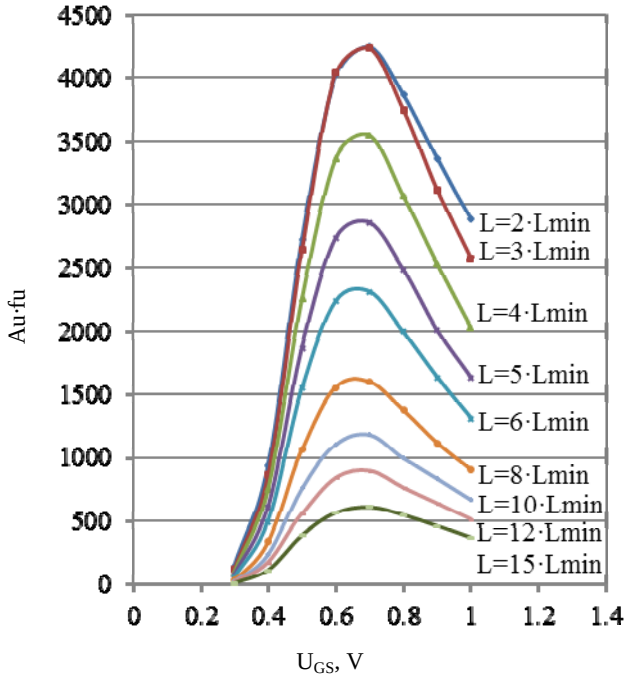

Fig. 8. Gain-to-unity-gain frequency product $A_u \cdot f_u$ vs. L and U_{GS}.

Fig. 9 gives another 3-D view of the gain-to-unity-gain frequency product $A_u \cdot f_u$, in which the channel length L and gate-source voltage are arguments together. The maximum of the product $A_u \cdot f_u$ is for L=2·Lmin and U_{GS}=0.7 V (around the border between strong inversion and velocity saturation regions). The value is up to $4200 \cdot 10^9$.

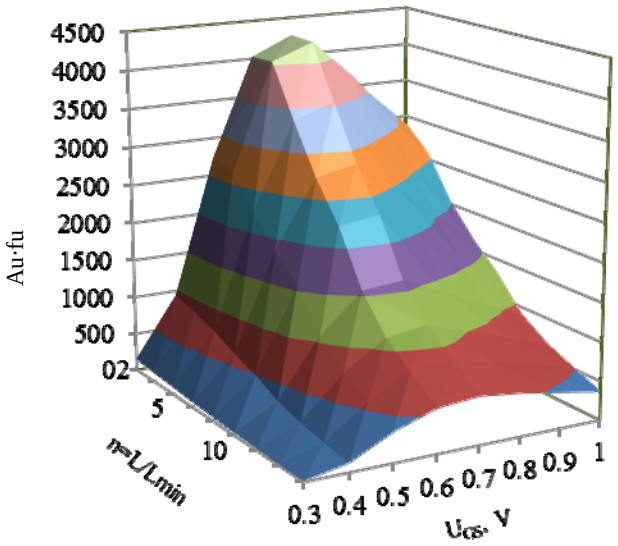

Fig. 9. 3-D view of the gain-to-unity-gain frequency product $A_u \cdot f_u$ vs. L and U_{GS}.

Using the provided graphs, designers can choose better values of the channel length and bias condition U_{GS} for every transistor in the circuit.

IV. Conclusion

The paper presents a set of simulation experiments for characterization and graphical representation of the performance of deep and ultra-deep submicron CMOS transistors in dependence of channel length L and bias conditions U_{GS}.

To this aim the key performance indicators as transconductance gm, unity-gain frequency fu, intrinsic gain Au and gain-to-unity-gain frequency product Au·fu are discussed. Test circuits for evaluation of these indicators by simulation are presented.

The proposed approach is applied to the nMOS transistor from 45nm CMOS technology. The obtained results give detailed and demonstrative illustration of the characteristics of the transistor for different values of channel length L and bias conditions U_{GS}.

The results can be used to determine the operating point and the sizes of the transistors in analog integrated circuit design.

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Comparison between Different Schematic Solutions to Achieve Constant-gm in Fully Differential Operational Amplifiers

Georgi Ognyanov Georgiev and Emil Dimitrov Manolov

Abstract – **The paper presents a comparative analysis between three schematic approaches to achieve constant-gm functionality in a fully differential operational amplifier. The goal is to draw conclusions concerning which of the techniques can fulfill best our preset requirements. The three techniques that are discussed in this paper are: constant-gm structure using dummies connected in parallel to the input differential pairs (the dummies technique), constant-gm structure using a common branch that connects the sources of the input differential pairs (the common-branch technique) and dynamic current scaling technique (the DCS technique) that relies on switching the currents of the input differential pairs. In order to compare the three techniques three operational amplifiers plus a fourth that does not have a constant-gm structure are designed and DC and AC simulations are performed. The results are presented graphically and in table and conclusions are made.**

Keywords – **constant-gm, fully-differential amplifier, dynamic current scaling.**

I. INTRODUCTION

In our modern world, electronics have entered every aspect of our lives. The integrated circuits become smaller, faster and more powerful. One of the main directions in which electronics is evolving is the increase of the working frequency. This poses a new, additional set of prerequisites that operational amplifiers must fulfill.

One of the main problems in designing high-frequency operational amplifiers is the noise [1]. In a substantial percentage of the newer and advanced applications, the operational amplifiers are used to amplify signals with small amplitudes. Then the noise at higher frequency can become comparable to the signal and thus can become a major problem. Maybe the best ways to suppress noise from a design point of view is to select operation amplifiers that have fully differential structures. They inherently possess a much better noise suppression compared to single-ended amplifiers.

Another very common problem in newer and more advanced applications is the requirement that the operational amplifier needs to work with variable voltage at its inputs and outputs (even rail-to-rail in some cases). This requirement can be fulfilled by using schematic with constant-gm in the entire input common mode voltage range.

The goal of the paper is to make a comparison between three different techniques to achieve constant-gm in fully differential amplifier with rail-to-rail input and output.

To this aim three amplifiers based on the compared techniques will be designed and simulated using a standard 0.18μm CMOS XFAB technology with 2.5V supply voltage (VDD)

In order to achieve a meaningful comparison the following design considerations have been implemented: 10μA (I) bias current for the amplifiers; 40μA (4*I) currents throught each transistor in the differential pairs when both pairs are active (input voltage in around VDD/2); the aspect ratios of the transistors are selected for operation in the saturation region [2]; the resulting unity gain frequency (F_U) should be higher than 50MHz.

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II. PROPOSED TECHNIQUES

The three techniques that compared in this paper are:

A. The dummies technique [3]

This constant-gm technique relies on two "dummy" transistors whose gates are connected to a common mode voltage VCM. The input differential pairs with the "dummies" are shown on Fig. 1. The block schematic of the entire amplifier can be seen on Fig. 3.

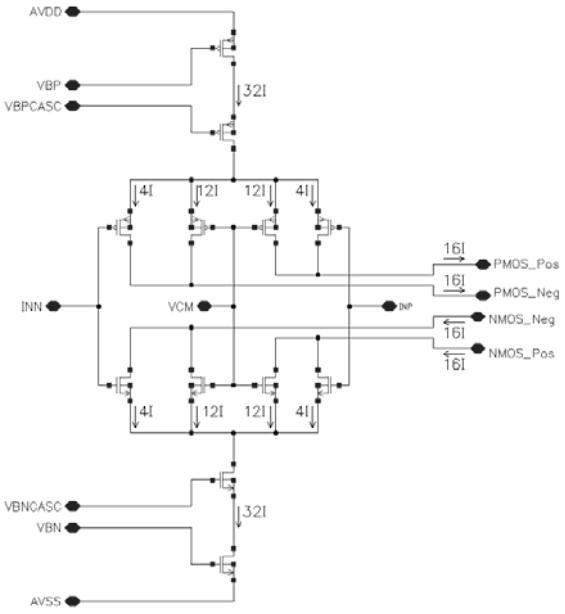

Fig. 1. Schematic with "dummies" constant-gm technique".

B. The common branch technique [4]

This technique relies on two secondary differential pairs which are added with the goal of increasing the current and the gm of the input differential pair in saturation. The input differential pairs with the "common branch" are shown on Fig. 2. The block schematic of the entire amplifier is shown on Fig. 3.

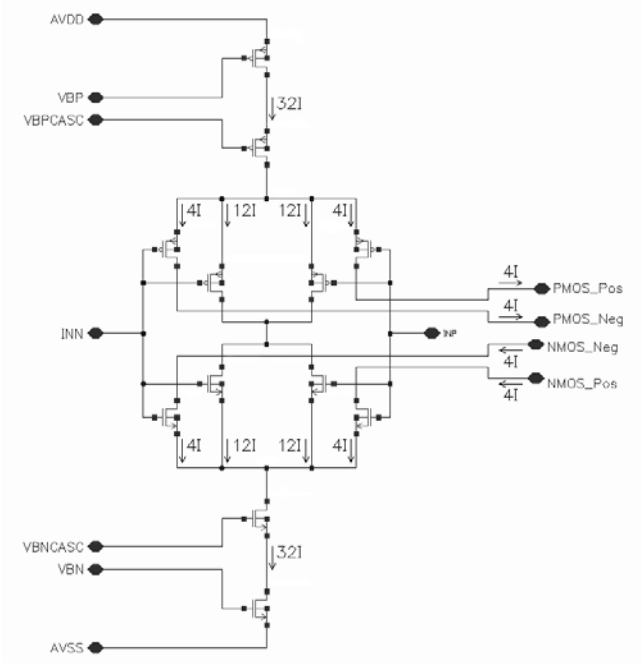

Fig. 2. Schematic of "common branch" constant-gm technique"

The common branch technique has one major drawback. The output currents from the block containing the differential pairs will not be the same - they depend on the input voltage. If only one pair is active the corresponding output currents will be four times larger compared to the case when both pairs are active. The result from this difference will be that the output impedance of the entire amplifier will vary depending on the input voltage.

C. The Dynamic current scaling technique [5]

This constant-gm technique relies on 4 pairs of switches that scale the currents coming from the input differential pairs. The switches together with their biasing circuit represent the Dynamic Current Scaling (DCS) schematic

Among the notable features of this technique is the fact that the four input currents form the differential pair block can be divided into eight at the output of the DCS block. This will reduce the gain by 6 dB but it will allow the use of two folded cascode outputs blocks with four input currents each. Potentially this can improve noise characteristics as well as offset.

By modifying the DCS a further multiplication of the output currents can be achieved (at the cost of further decrease in the gain of course) which means that in example four folded cascode outputs can be connected to one set of differential pairs.

III. SIMULATION RESULTS

Table 1 shows the achieved results after AC simulations of three amplifiers designed using the above mentioned techniques. An amplifier without any constant-gm modifications has been designed and simulated and added to the results as well to provide a better comparison.

TABLE 1. MAIN ACHIEVED CHARACTERISTICS

	AUDC [dB]	F3dB [kHz]	FU [MHz]	Variation of gm [%]	IIN [μVrms]
No const. gm	90.4	2.9	96.3	±35	250
Dummies	80.8	5.6	60	±7	194
Common Branch	90.1	2.8	90.4	±18	92
Dynamic current scaling	84.2	3.4	58	±2.2	111

Table 1 with the main achieved characteristics demonstrates the basic pros and cons of the examined techniques:

- If we look at the DC gain (AUDC) of the four simulated amplifier we can see that the common branch technique is notable for not losing on DC gain, while having a constant-gm feature.
- The DCS technique looses roughly 6 dB from the splitting of the differential pairs' currents as expected.
- The lower DC gain grants the dummies technique a slightly better 3dB frequency.
- The dynamic current scaling technique achieves an excellent result – only ±2.2 % variation of gm in the entire input voltage range.
- Despite having an impressively low variation in the gm the DCS technique also has a slightly lower unity gain frequency (F_U) similar to that of the dummies technique.
- It is of importance to note that the amplifier designed with the DCS technique has two-to-three times bigger quiescent current compared to the other amplifiers.

Furthermore on Fig.6 we can observer the gm variation of the four simulated operational amplifiers as a function of the input common mode voltage. The superiority of the DCS technique when it goes to keeping the gm of the amplifier constant in the entire input voltage range is evident.

Integrated Input Noise (IIN) is the noise at the output of the amplifier divided by its DC gain. From the simulations for integrated input noise it can be seen that the Common branch and the Dynamic current scaling (DCS) amplifiers have excellent noise characteristics compared to the other structures.

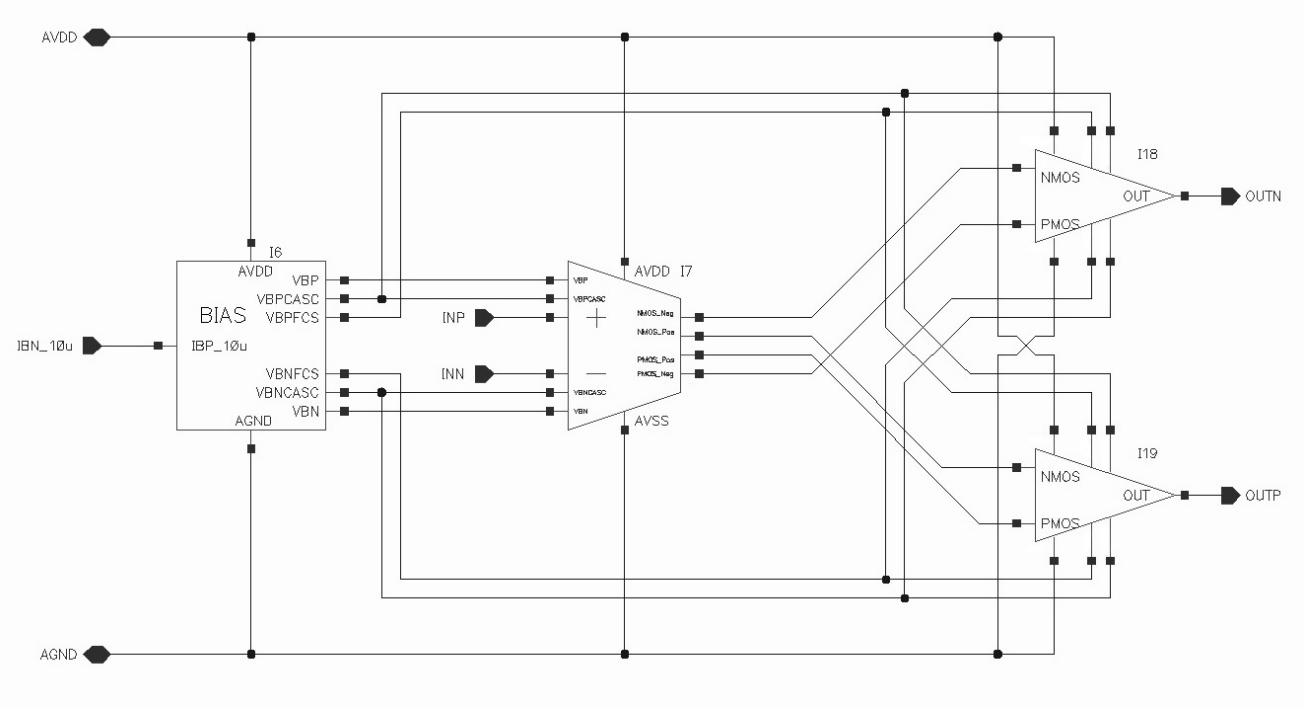

Fig. 3. Block schematic of a fully differential amplifier using either the “dummies” or the common branch techniques.

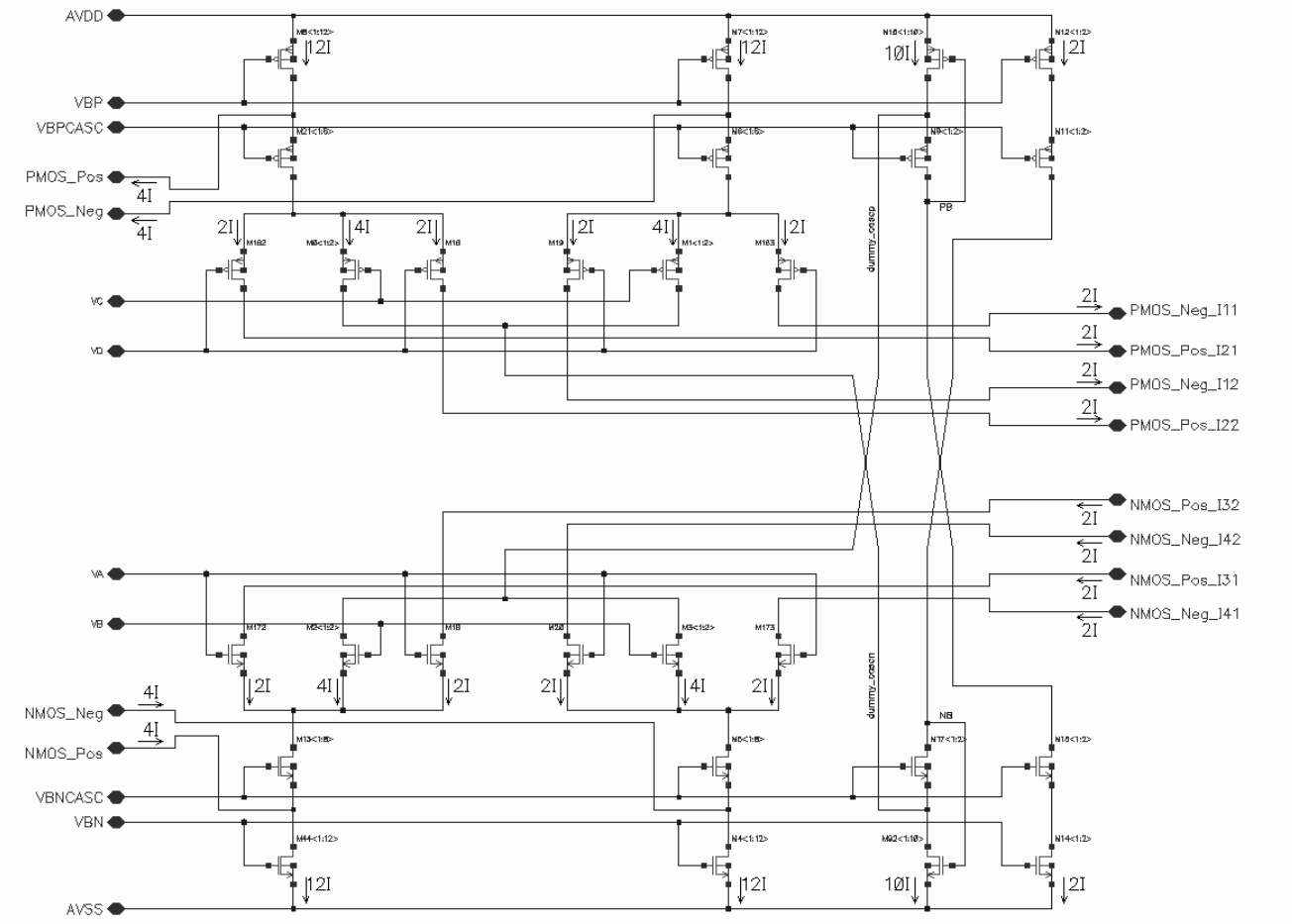

Fig. 4. Schematic of the Dynamic Current Scaling (DCS) circuit

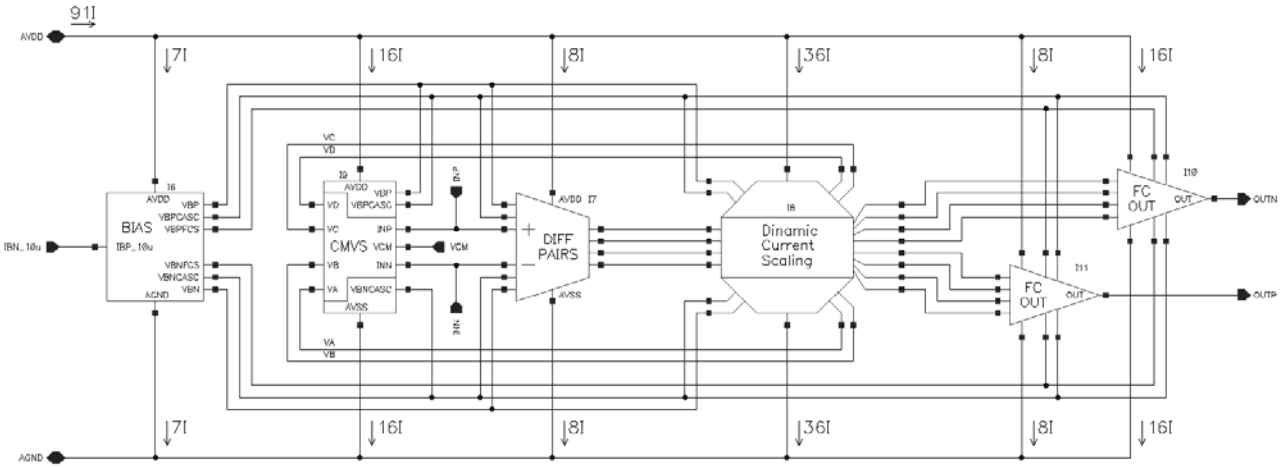

Fig. 5. Block schematic of a fully differential amplifier using Dynamic Current Scaling

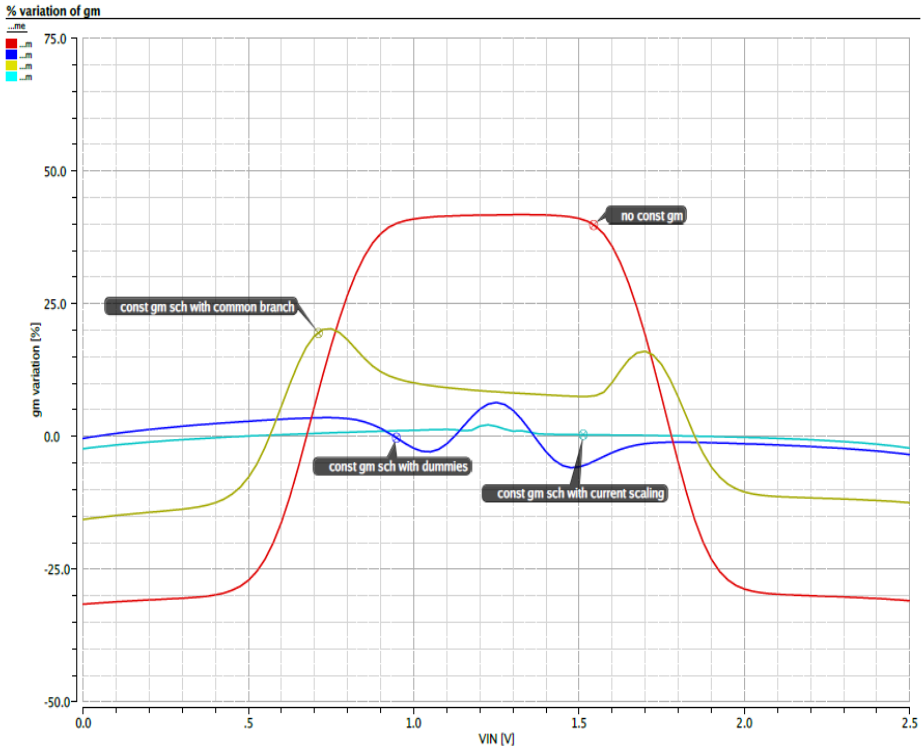

Fig. 6. Simulation result for the gm variation of the four simulated fully differential amplifiers.

IV. Conclusion

Taking into account the obtained results, we can easily see the benefits of using the dynamic current scaling technique when looking for a reliable constant-gm implementation. The more than 15 times reduction in the variation of the gm, combined with the good open loop gain and good unity gain frequency, undoubtedly makes this design one of the best possible solutions when a top priority for a designer is to keep the gm variation to a minimum. It is important to note that from [5] we can see that such design has its drawbacks – increased current consumption, complexity of the design and the need to design very carefully the circuit that control the switches, are some of the bigger issues.

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Design Considerations for Current Mode Amplifier in Deep Sub-micron CMOS Technology

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Abstract – **A design procedure for current amplifier circuit, based on a combination of theoretical and graphical methods is proposed. Computer simulations demonstrate the good matching between specified and obtained circuit parameters. The linearity of the circuit and its frequency dependence is evaluated, using THD as criterion. Monte Carlo analysis is performed to estimate the parameter deviation due to process variations.**

Keywords – **Amplifiers, current amplifiers, CMOS, low input impedance, high output impedance.**

I. INTRODUCTION

Current mode operation in analog signal processing is undergoing extensive development in the past two decades, which is primarily driven by the permanent demand for supply voltage reduction [1,2]. Current mode circuits have several significant advantages [1-4]. They allow operation at much wider range of the signal levels compared to their voltage mode counterparts. They also have wider frequency bandwidth, better linearity, their circuits are simpler and usually consume less power.

Various types of current mode circuits are proposed in literature: operational transconductance amplifier, current conveyor, single ended current amplifier, current operational amplifier, current differencing amplifier, etc. They find application in many high performance analog and mixed signal processing blocks like sensor interfaces, data converters, filters, oscillators, and others.

The design of current amplifiers has some specifics in the modern CMOS technologies, creating serious challenges in the analog design. They are primarily related to device downscaling, where short channel effects become significant. These effects include channel length modulation, hot carrier injection, velocity saturation and drain-induced barrier lowering. As a result the device characteristics deviate from those of long channel FETs, e.g. the drain current is not a square law due to velocity saturation [4]. Those effects require modification of the existing design procedures and employment of new techniques based on computer simulation and optimization. An example of such approach is given in [5,6].

The methodology described in [5] is extended in this paper to design one of the most popular current mode amplifiers (Fig. 1), using a modern CMOS technology. This circuit serves as a basis for a family of current mode amplifiers with different properties: low input impedance [4], extended frequency bandwidth [4,7], current differencing amplifiers [3], input stage of a current operating amplifier [8]. The basic characteristics of the designed amplifier are investigated by simulation: dc operating point, frequency response, linearity, sensitivity about process variation.

The used process is 32nm bulk CMOS technology, developed for SRAM, logic and mixed-signal applications from IBM. Nominal operating voltage is 1V for thin gate oxide, but high voltage transistors with medium (1.5V and 1.8V) and thick gate oxide (2.5V and 3.3V) are available. Minimum drawn gate length is 30nm for thin oxide, and 270nm for thick oxide FETs.

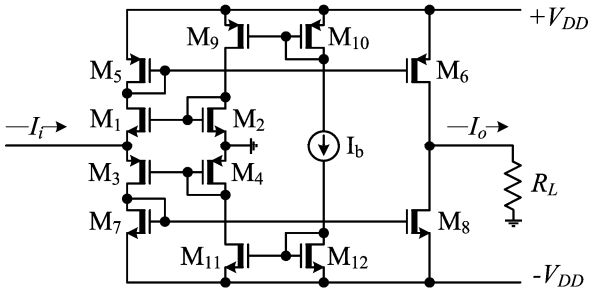

Fig. 1.The circuit of the basic current amplifier.

II. SHORT DESCRIPTION OF THE CIRCUIT

The operation of the circuit is based on several connected current mirrors. In quiescent point, the reference current I_b is copied through current mirrors M_{10}-M_9 and M_2-M_1 as a current through M_1. The same current is copied through M_3. Current mirrors M_5-M_6 and M_7-M_8 copy the identical currents through M_1 and M_3 as identical currents through M_6 and M_8 and the output current I_o is zero. When input current I_i is applied, it disbalances the currents in the upper (M_1 and M_5) and the lower (M_3 and M_7) parts of the input branch. This results as a proportional disbalance in the output branch and the difference between M_6 and M_8 drain currents flows through R_L as output current. The basic formulas for this amplifier are [3, 7, 9]:

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$$A_i = \frac{W_6/L_6}{W_5/L_5} = \frac{W_8/L_8}{W_7/L_7}\ ; \quad (1)$$

$$R_i = \frac{1}{g_{m1} + g_{mb1} + g_{m2} + g_{mb2}}\ ; \quad (2)$$

$$R_o = \frac{1}{g_{ds6} + g_{ds8}}\ , \quad (3)$$

where A_i is the current gain (output is short circuited), R_i is the input resistance, R_o is the output resistance, g_m's are the transconductances, g_{mb}'s are the back-gate transconductances and g_{ds}'s are the output conductances of the corresponding FETs.

III. Initial Design Centering

The design of the circuit, is in fact proper sizing of the devices to meet the specifications. The considerations here are focused on primary parameters: the gain, input and output impedances. The current gain is ensured simply by a proper choice of the aspect ratios of transistor pairs M_5—M_6 and M_7 – M_8 according to (1). The procedure to achieve the desired input impedance is more sophisticated. Mainly it depends on the transconductances of the input transistors M_1 and M_3, (equation (2)), but several factors cause difficulties: M_1 and M_3 are of different type – NMOS and PMOS, but g_m of the transistors should be kept equal to achieve symmetrical response for input signals with different polarity; the same current flows through both transistors; the back-gate transconductance should be taken into account.

The output impedance is defined by the output conductances of M_6 and M_8 (formula (3)). It is function of two parameters – the drain current and the channel length modulation parameter λ of these transistors according the well-known formula [2,9]

$$r_{ds} = \frac{1}{(I_{dsat}}\ . \quad (4)$$

The input and the output impedance depend on each other since: 1) the drain current of M_6 and M_8 is defined by the current through M_1 and M_3 multiplied by the current gain; 2) λ is process defined parameter. For this reason the output impedance will not be considered as design parameter here and the main focus will be on the input impedance and the symmetry of the input stage.

The bulks of the input transistors are not connected to their sources, which introduces g_{mb1} and g_{mb3} terms in formula (2). The back-gate transconductance usually is 10-20% of g_m [9]. This value can be refined by simulation of g_m and g_{mb} vs. V_{gs} shown in Fig. 2, where the back-gate effect is taken into account with V_{bs}=1.25V. The ratio g_{mb}/g_m obtained from the curves is 10-12%.

The design procedure will be illustrated by an example design of the basic current amplifier from Fig.1 with the following parameters:

- input impedance R_i<500Ω;
- power supply V_{DD}=±1.25V;
- current gain A_i equal to 1 or 5.

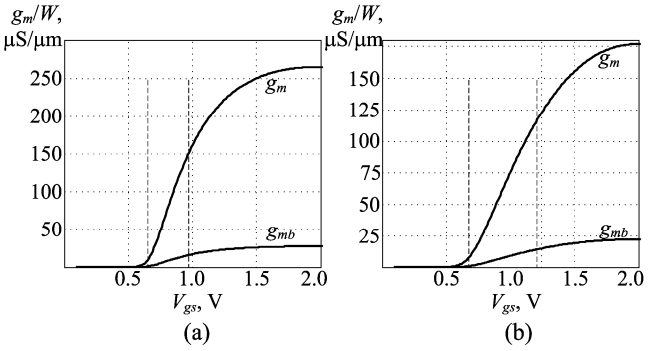

Fig. 2. Transconductances g_m and g_{mb} vs. gate-source voltage, normalized by the width: a) NMOS; b) PMOS. The drain-source voltage is 1.25 V.

The minimum gate length of the 2.5V MOSFETs in the used process is 270nm. It is good practice to use at least two times the minimum technology feature size to minimize the device mismatch. Since the process is 32nm, the minimum 2.5V transistor gate length is well over the minimum feature size. Transistors with 270nm channel length will be used to achieve maximum frequency bandwidth at the specified power supply voltage.

The specified input impedance determines the value of M_1 and M_3 transconductances. They can be estimated using formula (2), taking into account that g_m and g_{mb} for both input transistors have to be equal and using the worst case value of 10% for g_{mb}/g_m:

$$g_{m1} = g_{m2} = g_m = \frac{1}{2.2R_i}\ . \quad (5)$$

From (5) it follows that g_m must be higher than 910 µS.

The transconductances of M_1 and M_3, assuming long channel devices, are respectively:

$$g_{m1} = \sqrt{2\mu_n C_{ox}\frac{W_1}{L} I_d}\ ; g_{m2} = \sqrt{2\mu_p C_{ox}\frac{W_2}{L} I_d} \quad (6)$$

Since I_d, C_{ox} and L are equal for both transistors the transconductances of M_1 and M_3 are equal if:

$$W_1/W_2 = \mu_p/\mu_n\ . \quad (7)$$

Due to the short channel effects this expression is not quite accurate and graphical methods will be applied for obtaining proper widths of M_1 and M_3.

Drain current and transconductance vs. V_{gs} for NMOS transistor, normalized by channel width are plotted simultaneously on Fig. 3(a). The first step is to select a normalized value for g_m – it is better to be in the middle of the area, where g_m is linear function of V_{gs} (marked by dashed lines in Fig.2)[5]. The choice here is 91µS/µm and it directly gives W_1=10µm. Next step is to find V_{gs} of M_1 and its normalized drain current as it is shown in Fig. 3(a). They are V_{gs}=830mV and I_d/W=9µA/µm, which gives I_d=90µA. The normalized value for the drain current of M_1 should be in the area of the square law dependence. If it is not, different starting point should be selected.

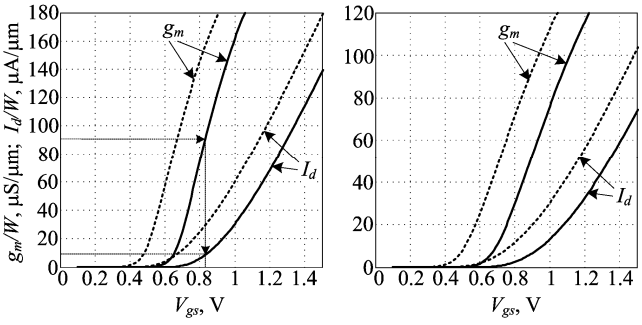

Fig. 3. Plots of normalized g_m and I_d vs. V_{gs}: (a) NMOS; (b) PMOS. Dashed curves are at V_{bs}=0, solid lines are at V_{bs}=1.25V.

The M_3 channel width has to be set to a value, which ensures the same transconductance at the same drain current as in M_1. A convenient way to do this is to plot a family of $g_m(I_d)$ curves at different channel widths (Fig. 4). The target point "a" (I_d=90µA and g_m=910µS) falls between W=24µm and W=25µm and approximately corresponds to W=24.7µm. This value is used to calculate the normalized values for g_m/W=36.8µS/µm and I_d/W=3.6µA/µm of the PMOS transistor. To make sure M_3 operates in saturation these points are cross-checked in Fig. 3 (b). It should be in the region where g_m/W increases linearly and I_d/W changes quadratically.

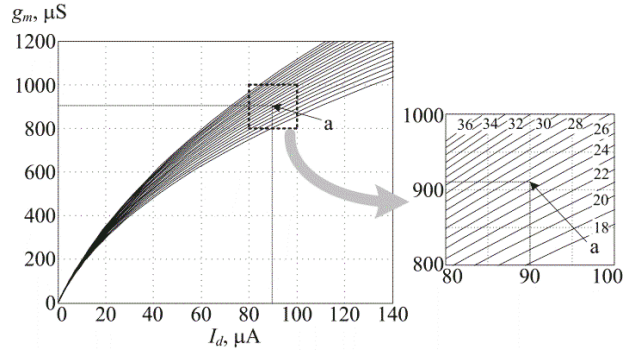

Fig. 4. Family of curves $g_m(I_d)$ for PMOS at different channel widths. In the zoomed picture the channel widths are marked on the corresponding lines.

The obtained widths provide matching of the input transistors pairs (M_1/M_3). The same sizes will be used for the other pairs (M_2/M_4, M_5/M_7, M_9/M_{11} and M_{10}/M_{12}), since they ensure the necessary current for proper operation. The output transistors M_6/M_8 are an exception since their sizes is defined by the current gain.

This is first approximation for the device sizes assuming no channel length modulation. In reality, the drain current depends on drain-source voltages, which are unknown initially. An operating point analysis returns the real picture in the circuit. It is done at I_b=90µA and the received parameters of interest are shown in the first row in Table 1. The reason for the deviation from the desired values is the large difference between real V_{ds} values (V_{ds1}=601mV, V_{ds3}=586mV) and V_{ds}=1.25V used in simulations so far.

The values of g_m and I_d through M_1 and M_3 are lower than the target values, which is consequence of the non-ideality of the current mirrors. They are compensated by increasing of the referent current to I_b=133µA applying parametric analysis and using the value of M_1 and M_3 transconductances as a criterion. The results are given in the second row of Table 1. It can be further optimized by a new parametric analysis, taking as a parameter the ratio between the widths of PMOS and NMOS transistors, and using as a target the difference between g_{m1} and g_{m3}. The third row of Table 1 shows that the matching is very good at widths W_1=10µm and W_3=23.7µm.

The widths of M_6/M_8 should be 5 times larger when A_i=5 (W_6=50µm and W_8=118.5µm) and the same as the other transistors widths at A_i=1.

TABLE 1: CHANGE OF THE BASIC PARAMETERS OF M1-M4 DURING THE DESIGN ITERATIONS

Itera-tion	I_{d1}, µA	g_{m1}, µS	I_{d3}, µA	g_{m3}, µS	I_{d2}, µA	g_{m2}, µS	I_{d4}, µA	g_{m4}, µS
I	67.6	758	67.6	750	80.3	849	77.5	823
II	95.8	911	95.8	927	116	1032	112	1028
III	95.5	909.5	95.5	910.5	116	1032	111	1010

IV. EVALUATION OF THE DESIGNED AMPLIFIER

After final device sizing and confirming that the desired operating point is achieved, it is necessary to check and investigate the other circuit parameters. The frequency dependent parameters of the amplifier – current gain and the magnitude of the input impedance at different load resistances – are considered first and their plots are given in Fig. 5. The current gain at short circuited output (R_L=1Ω and R_L=10Ω) is about 10% higher than the desired value. If an exact gain of 1 is required, the widths of the output transistors (W_6 and W_8) should be modified accordingly. The current gain decreases as the load resistance becomes comparable to the output impedance of the amplifier. The output impedance can be calculated by (3), where g_{ds6} and g_{ds8} are directly obtained from the simulation and it is 12.4kΩ. The corner frequency at -3dB decreases as R_L increases: ~2.3GHz at 1Ω, 10Ω, 100Ω; 1.82GHz at 1kΩ; and 664MHz at 10kΩ. This dependence is basically due to the increased output voltage when R_L is high, which increases the Miller effect of the drain-gate capacitance of M_6 and M_8.

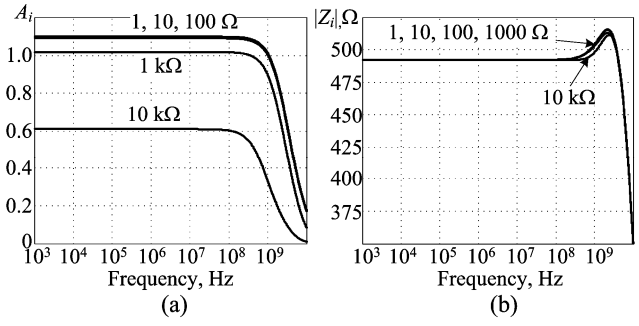

Fig. 5. Frequency responses of (a) the gain and (b) the input impedance of the amplifier, designed for A_i=1, at different loads.

The input impedance shown on Fig. 5(b) practically is constant up to 1GHz. Its value is 492Ω - very close to the specified upper limit for this parameter. This limit was used as a target parameter in the design – thus, there is a very good convergence between the target and the simulated input impedance. However, a good practice is to provide some margin for the target in order to compensate possible deviations due to process variations, temperature etc.

The amplifier, designed for A_i=5 has similar behavior. Its simulated low frequency gain is a bit higher than specified – 5.46, and the input impedance does not change. Due to the bigger output transistors and higher currents through them, the corner frequency is lower and vary from 1.04GHz at R_L=1Ω to 175MHz at R_L=10kΩ. Output impedance is also lower – 2.52kΩ.

The linearity of current amplifiers is usually demonstrated by DC transfer characteristic (output vs. input current). The plot is impressive, however it does not describe well the non-linearity as it is very close to straight line and a numerical criterion is missing. Also, there is no information on how non-linearity is affected by the frequency. These weaknesses are avoided here and in Fig. 6 are shown the dependence of the amplitude of the output current and its total harmonic distortion (THD) from the amplitude of the input current. This is done at two different frequencies – 1kHz and 300MHz, and at two different loads - 1Ω and 1kΩ. Obviously, nonlinear distortion represented by THD increase at high frequency, but this can be seen only on the plot of THD in Fig. 6(b).

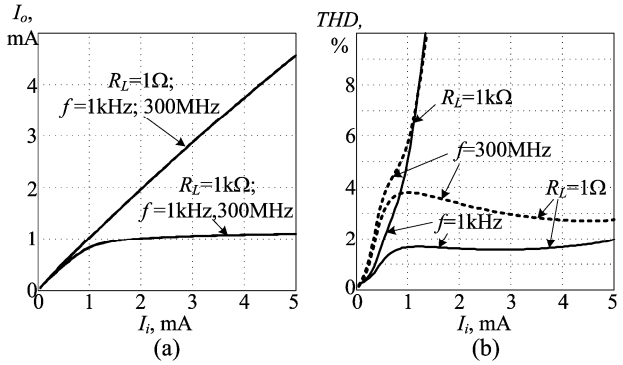

Fig. 6 (a) Dependence between amplitudes of the output and input currents at two different loads and two different frequencies; (b) THD of the output current vs. the amplitude of the input current.

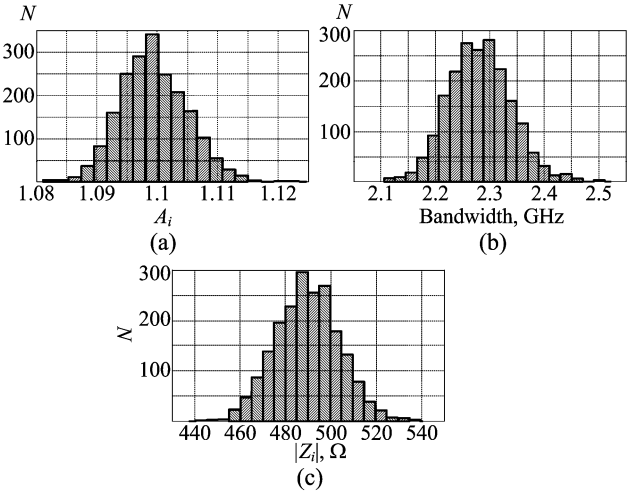

Fig. 7. Monte Carlo analysis of the circuit (2000 runs): (a) current gain; (b) frequency bandwidth at -3dB; (c) input impedance.

The last investigation is about the influence of the process variations. It uses the information about statistical variations during chip manufacturing, included in the IBM process design kit for this technology [10]. The histograms on Fig. 7 demonstrate the deviation of the three major parameters: current gain, bandwidth determined at -3dB and input impedance. The main conclusion is that they are reasonably stable and the variations are within ±10% for the bandwidth and input impedance and ±3% for the current gain.

V. CONCLUSION

The considerations concerning the design of a current amplifier, done in the paper, are focused mainly on several targets: ensuring of the desired gain and input impedance of the amplifier, and achieving good symmetry between upper and lower halves of the amplifier. While the first two are small signal parameters, the last one (symmetry) determines the linearity of the circuit. The difficulties in the design are caused by the different types of transistors, used in the upper and bottom parts of the circuit, and by the typical problems existing in the modern short channel technologies. The procedure, proposed here to overcome these problems, combines the basic theoretical formulas, graphical methods and computer simulation. Its target is proper sizing of the transistors at optimal operating point.

The considerations are illustrated by design of a current amplifier. This example demonstrates the good matching between the specified parameters and those, obtained by computer simulation of the designed amplifier. The sensitivity concerning the process variation is investigated by Monte Carlo analysis. It is small, since the used process (IBM CMOS32LP) is well established, but also due to the good design centering, achieved by the proposed procedure.

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Computer Investigation of CMOS Operational Transconductance Amplifier (OTA) with Improved Linearity Implemented on AMS 0.35 µm Process

Atanas Tanev, Ivan Stefanov Uzunov, Sotir Ouzounov and Marin Hristov Hristov

Abstract – **Transistor circuit of a single stage fully differential OTA implemented on AMS 0.35 µm process is investigated with simulations. The focus of the investigation is the linearization of the output current and the operation of the common-mode feedback circuit (CMFB). Total harmonic distortion of less than 1% is targeted as criterion for linearity. Different linearization techniques and their circuit implementation are implemented and compared. The OTA frequency response is also simulated and commented.**

Keywords – **amplifiers, operational transconductance amplifier, non-linear distortions, common-mode feedback.**

I. INTRODUCTION

Operational transconductance amplifiers (OTA, G_m amplifiers) are widely used as basic building blocks in many analog circuits and systems like active filters, variable gain amplifiers, data converters, etc [1]-[5]. They have several attractive properties: wide tunability of their G_m; high speed; low noise; ability to work at low supply voltages. OTA based bandpass filters with center frequency below 1 Hz, as well filters at 300 MHz are reported in the literature [6],[7]. The variability of the specs for the versatile applications and continuously modified properties of the new technological processes are the main driving forces for intensive investigation of these amplifiers for more than 25 years [4].

Ideally, the OTA is a voltage controlled current source: infinite input and output impedances; output current proportional to the input voltage ($i_{out} = G_m v_{in}$); infinite wide frequency response; completely linear; no output noise. The real OTA is realized as single- or multi-stage fully differential circuit in the most implementations in integrated circuits (IC) due to the well known advantages of the differential circuits [1],[2]. Its basis is the classical cascode differential pair. Many enhancement have been introduces for improving different performance aspects. The problems, which must be solved by the designer, are versatile and depend on the application: achieving the desired G_m (less than 1 nA/V for very low frequency filters, hundreds mA/V for HF applications); G_m tuning in desired range; increasing the output impedance; extension of the frequency response; robust common mode implementation; small dependence from temperature, process and voltage variability; low output noise. However, in majority of applications, the basic problem in the transconductance amplifiers is their linearity. It is a inherent problem, caused by the nonlinear characteristics of the transistors (quadratic dependence of the drain current from the overdrive voltage in the case of CMOS) and the necessity of working with low supply voltages. Many efforts have been invested in transconductor linearization and the progress has been substantial: the first proposed OTAs had a maximum input voltage of 30 mV, while nowadays the achievable linear range is about 1 V at supply voltages significantly lower [4],[7].

Degeneration resistors placed in series with the sources of the differential pairs and creating negative feedback are the classical way for improving the linearity [8]. Its basic advantage is the simplicity. If g_m is the transconductance of the transistors in the pair and R_{deg} is the value of the degeneration resistors, then the third order nonlinear product in the output current is proportional to $1/(1+g_m R_{deg})^3$. On the other hand, G_m of the whole OTA is reduced $1+g_m R_{deg}$ times, and that much is increased the output noise [5]. Some improvement of the method is proposed in [7] where dynamic resistances, created by MOS transistors, are used instead of linear resistors.

The OTA core in the second linearization method consists of two differential pairs with parallel connected inputs and outputs, which are crossed and have the same dynamic loads. In the crossed outputs the output currents of the pairs are subtracted. The parameters of the differential pairs, basically transistor sizes and tail currents, must be chosen in a way ensuring canceling the nonlinear components and preserving the linear component in the output currents of the pairs. Both conditions require different differential pairs and keeping relatively strict relationships between the parameters of the pairs. This makes the method frequency limited and sensitive to the temperature, process and bias voltage variations, which is its main drawback.

Versions of this method are applied in many practical circuits [5],[6],[9]-[11]. Very small transconductances for ultra low-frequency filters are realized in the same way [6]. Another application is shown in [9], where small degeneration source resistors for better linearity are used also. A further development of this method is given in [5],[10]. Both papers describe complete OTAs, consisting of three identical OTAs. The individual OTAs are not

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compensated for linearity. One of them is used as main OTA in the complete circuit and the other two together with additional elements (some specific attenuators) separate the nonlinear components and subtract them from the output current. The identity of the individual OTAs makes this method insensitive to temperature, process and supply voltage variations and extends the frequency band of operation. A drawback of the method is increased complexity of the circuit.

There are also other approaches. One of them is based on using of basic differential pairs, working in triode or weak inversion region and biasing in different ways the source dc voltage of the pair [12],[13] to achieve linearized transfer characteristic. Yet another method uses adaptive biasing of the tail current of the differential pair, making it depending on the input signal [14]. The source dc voltage must be stabilized in this case too. Bulk driven differential pair is proposed in [15]. The linearity in the circuit there is improved also by additional amplifiers placed in feedback in each arm of the pair.

In this paper we investigatethe OTA proposed in [7]. It is attractive due to its high frequency of operation and simplicity. In this paper we have studied the porting of the circuit to a specific technology process in its optimization for THD of 1%. The THD is derived from the output current.

II. Circuit Description

The investigated CMOS OTA, as it is given in [7], is shown in Fig. 1. It consists of a single differential pair M_1 and M_2 having transistors M_7 and M_8 as dynamic load. The DC drain voltages are set by a CMFB circuit, which is a pseudo-differential amplifier, formed by M_{cf1}-M_{cf4}. Resistors R_s monitor the average of OTA drain voltages and feed it to the input of CMFB amplifier. It is compared there with the desired common-mode voltage V_{CM} and the difference signal, taken from the drain of M_{cf2}, is returned to the gates of M_7 and M_8.

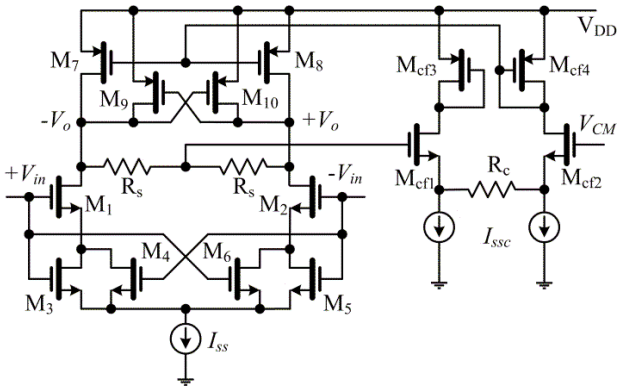

Fig. 1. Circuit of the investigated OTA.

Transistor pairs M_3-M_4 and M_5-M_6 form the degeneration resistors, linearizing the circuit. They operate in triode region and each transistor in the pair is controlled by a half of the input voltage with an opposite polarity. Thus, if the channel resistance of one of the transistors in the pair increases, the same resistance decreases in the other transistor. This reduces the unfavorable effect of the degeneration resistors on G_m of the OTA. The linearizing effect of the dynamic degeneration resistors depends on the ratio

$$a = \frac{\left(W/L\right)_{M1-2}}{\left(W/L\right)_{M3-6}} \quad (1)$$

where $a = 2$ is recommended in [7] as optimal for 0.13 μm process.

A negative resistance, formed by M_9 and M_{10}, is placed at the output for reducing the output conductance of the circuit. It is introduced due to the specific application of the circuit in [7] – for realizing high-Q bandpass active filters.

The simulations are done with AMS 0.35 μm CMOS process used in the education, which differs from 0.13 μm process in [7]. All transistor sizes are kept the same in the most of the simulations: $W = 10$ μm, $L = 0.35$ μm. They are the default sizes recommended for the process [16]. The value of the resistors R_s must be large and it is 100 kΩ, while the value of R_c is 1 kΩ. The tail current I_{ss} of the OTA is chosen to be 100 μA and the supply voltage is 3.3 V in all simulations.

III. CMFB and DC Bias

The goal of first simulation is determining of the currents I_{ssc} in the CMFB circuit. This circuit is a satellite circuit and it is important to reduce overall power consumption, by minimizing I_{ssc}. These simulations investigate the dependence of the output voltages (the voltage at "$-V_o$" node is chosen as representative) from I_{ssc}. OTA inputs "$+V_{in}$" and "$-V_{in}$" are connected to a 1.3 V dc voltage source. Fig. 2(a) shows the corresponding dependencies at three different voltages for V_{CM}: 1.25 V, 1.75 V and 2.25 V. The plots have two distinct parts: raising initial part, when the output voltages depend strongly from I_{ssc}; and a horizontal part, when this dependence is small and V_o is approximately equal to V_{CM}. The value of I_{ssc} should be at the beginning of the horizontal part – a minimum power consumption of the CMFB circuit is ensured in this way. The transition between both parts is at different value of I_{ssc} if the common-mode reference voltage V_{CM} varies. A conclusion from Fig. 2(a) is that $I_{ssc} = 25$ μA could be a good choice – it is the smallest value, which guaranties normal operation when V_{CM} increases up to 2.25 V. The effect of this choice will be examined also in the next simulations.

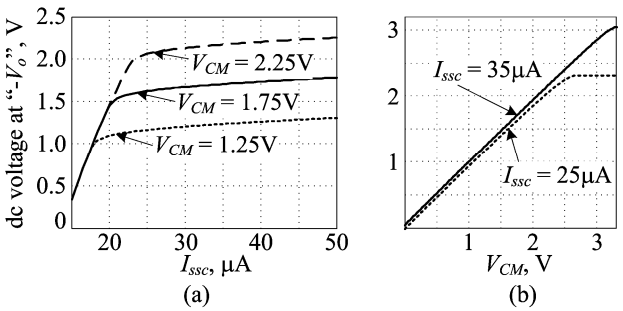

Fig. 2. Dependence of dc output voltage (at node "$-V_o$") from: (a) currents I_{ssc}; (b) common-mode reference voltage V_{CM}.

The plots from the next simulation, illustrating how dc output voltage is controlled by the common-mode reference voltage V_{CM}, is shown in Fig. 2(b). They confirm that 25 μA is the lowest boundary for I_{ssc}, since a horizontal part appears in the corresponding plot, when V_{CM} is above 2.5 V. This limitation does not exist in the plot at I_{ssc} = 35 μA – it demonstrates linear dependence of the output voltage from V_{CM} in the whole range from 0 to 3.3 V (V_{DD}).

The other simulations, which results are plotted in Fig. 3, investigate the changes of dc output voltage when some of the parameters of the basic differential pair vary. Fig. 3(a) shows that the output voltage does not depend on the common-mode input voltage (the plots are at I_{ssc} = 25 μA). The tail current I_{ss} affects the output voltage more significantly (Fig. 3(b)). There are again two areas in the plots: one with small dependence from I_{ss} and second, in which the output voltage rapidly drops down. These areas are visible in the plots for I_{ssc} = 25 μA and the boundary between them defines the upper limit for I_{ss}. This limit depends also from V_{CM} and it is between 110 and 130 μA for the considered plots. Upper limit for I_{ss} when I_{ssc} = 35 μA exists too but it is outside of the plotted area, i.e. the increased value of I_{ssc} increases also the robustness of the circuit versus variation of the tail current.

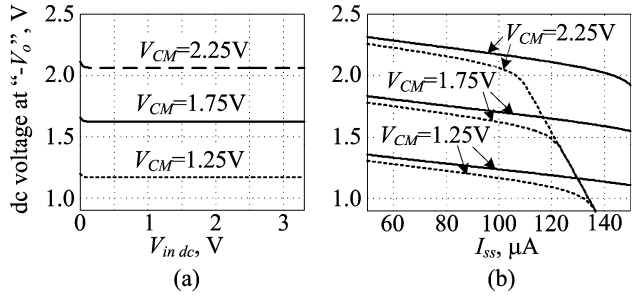

Fig. 3. Dependence of dc output voltage (at node "-V_o") from: (a) common-mode dc input voltage (at the gates of M_1 and M_2); (b) tail current I_{ss} (dotted lines are at I_{ssc} = 25 μA, continuous lines are at I_{ssc} = 35 μA).

The simulations in this section established the minimal values for the currents I_{ssc} in the CMFB amplifier, ensuring proper operation. They depend from few parameters: transistors dimensions, supply voltage, tail current in the basic differential pair, and upper limit for the common-mode reference voltage. Simulations, similar to the shown here, should be done for accurate determining of these currents in every specific case.

IV. Linearization of the Amplifier

The linearity of the amplifier and its dependence from the ratio *a*, defined by formula (1), is investigated briefly in [7]. The optimal value a = 2 is found by plotting G_m vs. differential input voltage at different values of *a*. Numerical criterion for linearity of the OTA itself is not presented in [7], instead are given measured data for IP3 of a G_m-C filter, realized by this OTA.

The OTA linearity is investigated here by using THD of the differential output current as a criterion. An AC voltage source with frequency of 1 kHz is placed at the input, and the output current is taken as the current through a capacitor with a large value (range of mF) connected between points "-V_o" and "+V_o" in Fig. 1 (short-circuited output). THD of 1% (-40 dB) is taken as conditional limit for linearity – the input voltage is increased until reaching this limit. This approach allows to evaluate the OTA linearity independently and to investigate its frequency dependence.

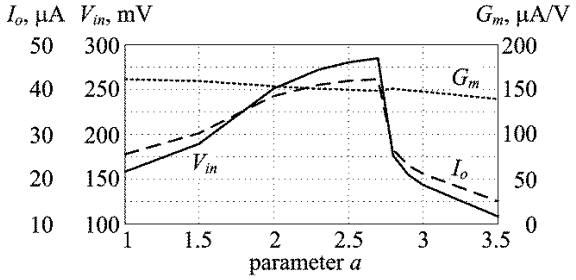

Fig. 4. The maximal undistorted amplitudes and G_m vs. parameter *a* from formula (1).

The first investigation is concerning the influence of the parameter *a* on the amplitudes of the input voltage V_{in} and output current I_o, at which is achieved the conditional limit for linearity (they can be considered as maximal undistorted amplitudes). The transistor sizes are as in the previous simulations and only the widths of M_1 and M_2 are varied for settling the desired value of *a*. The corresponding plots are shown in Fig. 4. The value of G_m is calculated as ratio between maximal undistorted amplitudes.

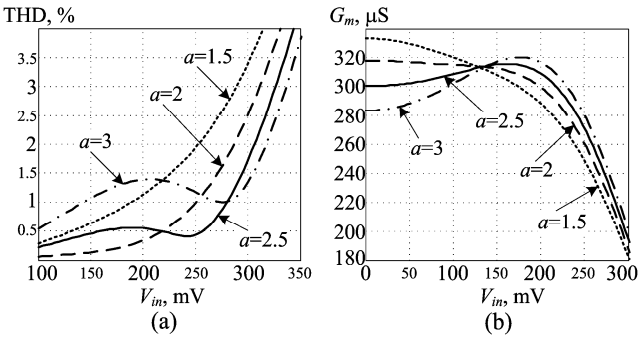

Fig. 5. (a) THD of the output current vs. amplitude of the input voltage; (b) G_m vs. amplitude of the input voltage.

The optimal value for *a*, which is seen in Fig. 4, is about 2.5 and it is different from the value given in [7]. Possible reasons for this difference could be difference in the processes, different transistor sizes, but the major is the different criteria for linearity. THD, chosen as criterion here, has interesting behavior, illustrated in Fig. 5(a). It has ripples when $a > 2$, which increase when *a* increases, but are still moderate if $a \leq 2.5$. These ripples extend the area where THD is less than 1%. This observation is confirmed by the plots of the differential G_m (= dI_{out}/dV_{in}) vs. amplitude V_{in}, shown in Fig 5(b). G_m has approximately flat behavior for lower values of *a* and it is in maximally wide area at a = 2. Above these value appear ripples, which increase with *a*. These ripples initially do not increase significantly the nonlinearity and the value of the parameter *a* can be optimized depending on the limit for the tolerated nonlinear distortion.

The simulation of maximal undistorted amplitudes and of G_m, done at a = 2.5, shows that they do not change significantly up to frequencies of 10 MHz (Fig. 6).

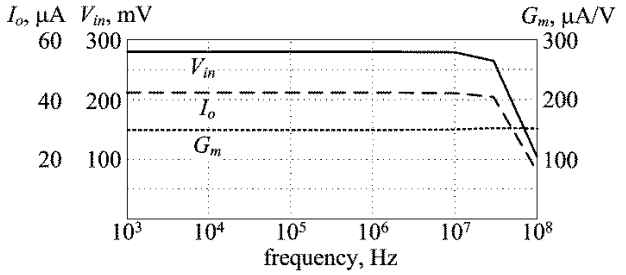

Fig. 6. Dependence of the maximal undistorted amplitudes and G_m from the frequency (a = 2.5).

V. Frequency Response

The frequency dependence of G_m in the OTA's is presented usually by one pole approximation [3]:

$$G_m = \frac{G_{m0}}{1+\left(s/\omega_c\right)}, \qquad (2)$$

where G_{m0} is the low-frequency value and ω_c is the -3 dB cut-off frequency. This approximation works for multi-stage amplifiers, but it cannot be used in the considered case.

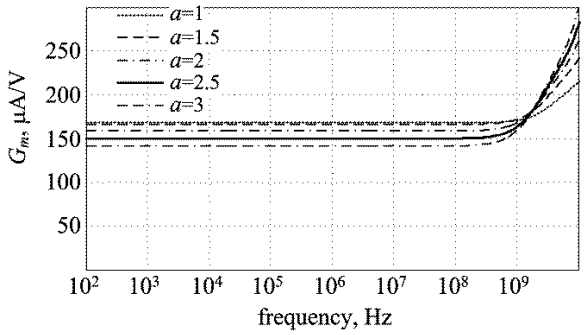

Fig. 7. Frequency dependence of G_m at different values of a.

Fig. 7 shows the frequency dependences of G_m at different values of the parameter a. All they are constant up to few hundreds of MHz and then start to raise. The increasing at very high frequencies is caused by the capacitances C_{gd} of M_1 and M_2. They connect directly the input with the output of the amplifier – point "+V_{in}" with "-V_o" and "-V_{in}" with "+V_o". These capacitances transfer a current, which increases with frequency, from the ideal voltage source at the input to the short circuiting capacitor at the output.

VI. Conclusion

The transistor level simulations, presented in this paper, analyzed the achievable linearity with a state-of-art OTA implementation, when using 350 nm AMS process. The paper studied the optimization of CMFB circuit power and the extension of the linear range of operation of the amplifier. A power consumption of 0.56 mW was achieved with 170 uA dc biasing current in the circuit.

The linearity is optimized by using of THD as a simple numerical criterion for linearity. A linear range of 270 mV for the amplitude of the input voltage was achieved. This approach allows easy to estimate the undistorted magnitudes of the input and output signals and also to determine the frequency limits of the considered linearization method.

The frequency response of the circuit is also investigated briefly. It is shown that the frequency dependence of G_m does not follow the one pole approximation given usually in the literature. This effect is caused by the parasitic gate-drain capacitances in the transistors in the differential pair.

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Acoustic Dispersion Analysis of the Resonant Modes in FBAR

Dobromir Georgiev Gaydazhiev

Abstract – **A procedure to build a two dimensional finite element model (FEM) of thin film bulk acoustic wave resonator (FBAR) and obtain the dispersion curves of its resonant modes is described in this article. A classic parallel plate device is analyzed and the dispersion curves of its main spurious harmonics are given.**

Keywords – **FBAR, acoustic waves, resonant modes, dispersion**

I. Introduction

Film Bulk Acoustic Wave Resonators (FBAR) are piezoelectric devices essential for the modern wireless telecommunication systems. Due to their high power handling capabilities, high quality factors and good temperature stability they are widely used for realizing stable bandpass filters with good selectivity in the modern RF front-ends [1], [2].

The FBAR devices consist of thin layer of piezoelectric material placed between two metal electrodes. When alternating electrical signal is applied at the electrodes, an acoustic wave is exited due to the reverse piezoelectric effect. The piezoelectric materials have anisotropic properties in the different directions of their crystallographic lattice and the acoustic waves travel at different speed depending on their direction and on the geometry of the piezoelectric layer [3]. This effect causes dispersion of the acoustic waves. To determine the resonant frequencies and to be able to design an FBAR device, the effects of wave dispersion have to be studied in detail.

The dispersion of the main resonant modes of field bulk acoustic wave resonator is analyzed in this article. A classical aluminum nitride (AlN) parallel plate resonator is studied using finite-element modeling (FEM) tools. The primary objective is to obtain the dependence of the acoustic velocity on the wavenumber for all major modes that are excited by parallel plate electrodes. This relation is essential in the FBAR design process. For the sake of simplicity, the electrodes are assumed to be infinitely thin in all calculations and simulations in the article.

II. FBAR Structure

In its simplest and most widely used configuration the FBAR devices consist of a piezoelectric material placed between the plates of a parallel capacitor as shown in Fig.1. When an electric field is applied between the plates, an acoustic wave travelling in parallel to the electric field is excited. The device resonates only for the frequencies that satisfy the relation:

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$$f = \frac{V_{WAVE}}{\lambda}\ , \qquad (1)$$

where V_{wave} is the speed of propagation of the acoustic wave and λ is the wavelength [3]. Typically aluminum nitride (AlN) is used as piezoelectric material, although other materials, such as zinc oxide (ZnO) and cadmium sulfide (CdS) have been used in the past. All those materials are crystals with anisotropic properties in the different directions of their crystallographic lattices. This, of course, applies to the V_{wave} as well. The finite dimensions and anisotropic properties constitute the wave dispersion that is observed in those devices for certain modes.

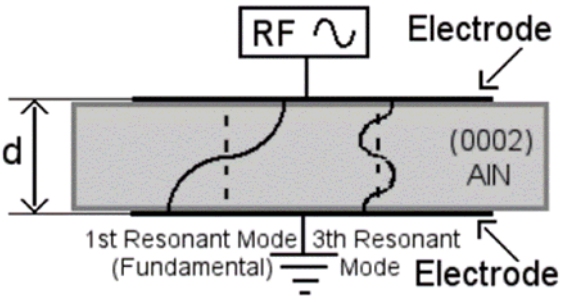

Fig. 1. Structure of an FBAR device [3].

A standing wave will form for acoustic waves with wavelengths that satisfy:

$$\lambda = \frac{2d}{n}\ , \qquad (2)$$

where n=1,3,5... represents the different longitudinal modes (harmonics), and d is the spacing between the electrodes. The first and third modes, excited by the parallel plate electrodes, are marked in Fig. 1. Due to the finite dimensions of the resonator and the anisotropy of the active material, acoustic energy is reflected in other directions and the device will also resonate at other "more complex" modes: transverse (shear), Lamb and other [3]. Most often the resonators are designed to operate at the primary longitudinal harmonic (n=1), while all other modes are considered parasitic and measures should be taken in the design phase to suppress them.

III. Acoustic Dispersion and Resonant Modes.

Dispersion is a physical phenomenon in which the phase velocity of a wave is dependent on its frequency. The dispersion is usually caused by [4]:

- geometric boundary conditions, i.e. reflections by the walls of a waveguide,

- specific material properties of the transmission medium, i.e. crystals with anisotropic properties.

The bulk acoustic wave piezoelectric resonators are usually designed to work with the longitudinal modes. There the wave travels in parallel to one of the crystal axes and is reflected by the perpendicular plates of the electrodes and no dispersion should occur. However, due to the finite dimensions of the devices, a portion of the acoustic energy is reflected in other directions, which excites other modes that are dispersive: transverse waves with horizontal polarization (Fig. 2) [5], Lamb waves (Fig. 3) [3].

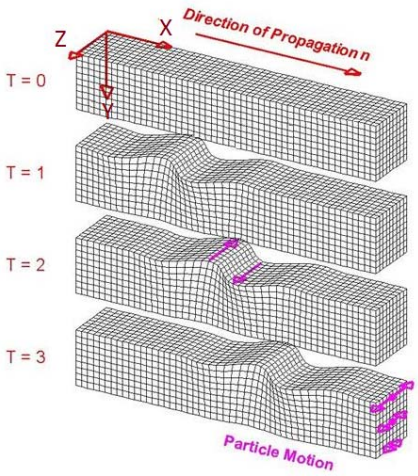

Fig. 2. Shear waves with horizontal polarization (SH) [6].

The SH waves exhibit lateral particle motion, that causes transverse wave propagation. The Lamb waves have elliptical particle motion and depending on its direction are categorized as symmetric or antisymmetric. The symmetric modes are denoted as S_i, and the antisymmetric as A_i, where i is the mode order.

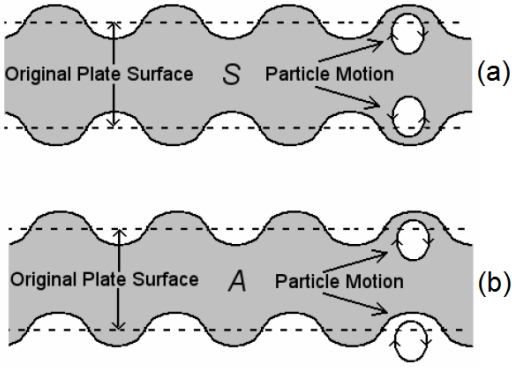

Fig. 3. Lamb acoustic waves: (a) symmetric and (b) antisymmetric [3].

IV. Two-dimensional FEM Analysis of FBAR

The dispersion of the resonance modes of a classic FBAR structure with parallel plate electrodes is studied. FEM software is used for the analysis. A two dimensional model of the structure is built (Fig. 4). Using 2D model significantly reduces the number of vibration modes, compared to a three dimensional model. This allows to easily isolate the primary shear and Lamb resonance modes excited by the parallel plates and requires much less computational resources. For the same reason, it is assumed that the electrodes have infinitesimal thickness and weight, which eliminates the mass loading effect. Aluminum nitride is used as piezoelectric material in the model. It has thickness of 10 µm and the C-orientation axis of the crystal is perpendicular to the electrode plates. Its *length* is variable. To examine the dispersion, Floquet periodicity is applied to the sidewalls of the AlN resonator. The wave number $ka=\pi n/length$, *where* $n=1,2,...,$ is swept from 0 to $\pi/5$µm to obtain the dispersion as a function of ka. This is roughly equivalent to running a parametric analysis along the device *length,* with values ranging from infinitely long device down to device with length of 5 µm.

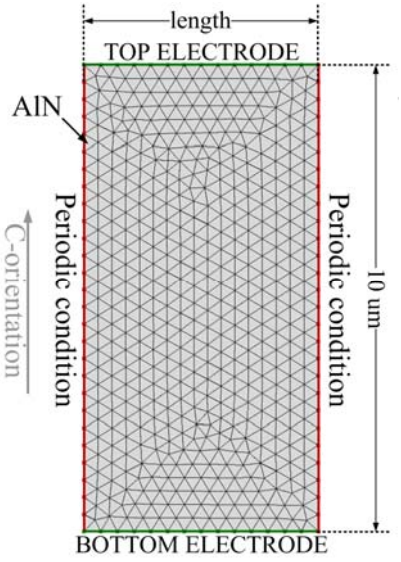

Fig. 4. Two dimensional finite element model of a FBAR device, used to determine its resonance modes and their acoustic dispersion as function of the wavenumber *ka*.

The purpose of this dispersion analysis is to determine the properties of the spurious modes that have similar resonance frequencies to the main resonance and design the device geometry accordingly to reduce their influence.

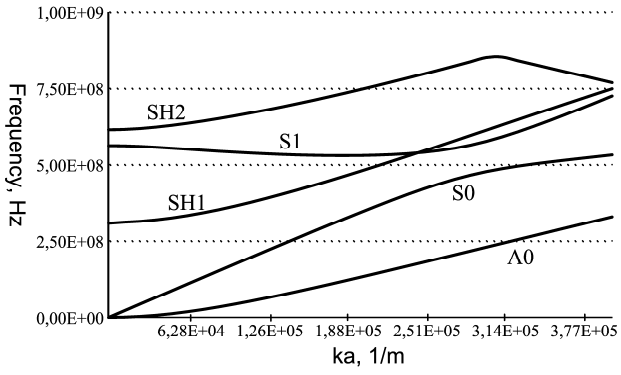

Fig. 5. Acoustic dispersion of the main Lamb and shear modes in the analyzed FBAR.

The dispersion curves of the spurious modes with frequencies close to the designed resonator frequency are shown in Fig. 5. Among them are three Lamb harmonics –

A0, S0 and S1, and two SH harmonics – SH1 and SH2. The resonance frequency of the first longitudinal harmonic can be calculated using formulas (1) and (2). Since the device is 10 μm thick and the longitudinal acoustic speed in C-oriented AlN is around 11000 m/s, in the given example the main resonant frequency is around 550 MHz. Depending on the values of *ka*, modes S1, S0 and SH1 may match the main resonant frequency. SH2 is close to it for small values of the wavenumber. The dispersion curve of mode S1 is very close to the main resonant mode for device lengths down to around 12.5 μm (*ka*=2.51e-5) or larger lengths multiples of this number. This means that S1 will interfere with the main resonant mode almost regardless of the device length. In those cases the S1 mode has to be suppressed using other measures. Most commonly they include designing specific shape of the terminals or specific shape of the device itself (apodization) to ensure the unwanted mode is suppressed. To properly design an apodized device a 3D FEM analysis has to be used to verify that all the unwanted modes are suppressed.

V. CONCLUSION

The main resonance modes of a classic parallel plate FBAR device are reviewed and a procedure to build a two dimensional finite element model is described. The proposed FEM model is used to simulate the behavior of the device and obtain the dispersion curves of the main spurious resonant modes. They are either shear (SH1, SH2) or Lamb modes (A0, S0, S1). All those harmonics show relative strong acoustic dispersion.

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Transient Analysis of Electronic Circuit Derived from the Active Site β-lactamase Hydrogen Bonding Network

Rostislav Pavlov Rusev

Abstract – **A Verilog-A circuit derived from a Hydrogen Bonding Network located in the active site of β-lactamase protein is developed for the purposes of microelectronics. The transient circuit analysis showed that the protein is able to process information like conventional the microelectronic circuits. At identical sine signal input, circuit outputs are similar to the outputs of an amplitude limiter, current source, and modulator.**

Keywords – **Hydrogen bonding network, Verilog-A, proteins, Cadence**

I. Introduction

Bimolecular information processing is of great interest to contemporary electronics [1]. It is brought forth by the functional characteristics of biomolecules and the biochemical and biophysical processes that take place in the biomolecules [2]. These phenomena allow for the construction of elements that could process information [3].

In the present paper we will present the functions of a protein Hydrogen Bonding Network (HBN) and code them in Verilog-A language [4] in Cadence Design Framework [5], [6]. Afterwards, we will examine the circuit properties to process signals.

II. Model and Equations

Hydrogen Bonding Networks (HBNs) formed in the active site of the β-lactamse protein are shown in Fig. 1 [7].

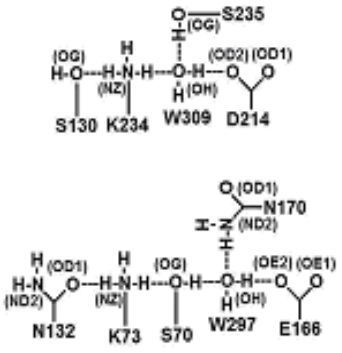

Fig. 1. HBNs in the active site of free enzyme β-lactamase

Charge (proton) transfer is investigated in [8] using the theory of Marcus [9]. The *K*-parameter of proton transfer is calculated by Marcus theory in analogy to the electron transfer parameter for each of the hydrogen bonds. Based on the calculations it is concluded that the higher the K parameter, the easier the transfer between donor and acceptor becomes and hence, the greater the protein current will be. After calculation of *K*, a block-element for each HBN donor and acceptor is set up and these block-elements are coded in Matlab [10]. Next, AC and DC analyses are performed; the results of these AC and DC analyses are compared to previous Matlab results.

Similarly, we set up a circuit of block-elements in Cadence Design Framework in Verilog-A language (Fig. 2). Here, we take into account the fact that the proton transfer in the two HBNs, viz. nucleophilic and electrophilic HBNs, occurs at the same time. The transfer in the two HBNs is also influenced by the pH of the environment. Hence, the respective electronic circuits are inseparably linked or integrated and so we place the respective block-elements into a common aggregated or integrated equivalent circuit. By analogy to the common pH of the environment, we input identical voltage to the inputs of the equivalent circuit.

In Fig. 2 Uin1 designates the input of the first circuit that is analogical to the "nucleophilic" HBN. In this circuit, the T1 block-element corresponds to the K73NZ lysine. The lysine is strong proton donor so in the equivalent circuit it is interpreted as a voltage controlled current source. The S70OG residue is substituted by the T2 block-element, which is a three-terminal element with identical input and output voltages but different input and output currents.

In the equivalent circuit the water molecule W297 is identified with T3 block-element which has two inputs and one output.

The T4 block-element corresponds to the strong proton acceptor E166 which can form different hydrogen bonds. The T4 is a three-terminal element with one input and one output.

The other block-elements, T5 and T6, correspond to asparagine residue N132 and N170. Asparagines might be simultaneously proton-donors and proton-acceptors, therefore the respective block-elements can alternate the current direction with the S switch in the equivalent circuit.

Uin2 designates the input of the second electrical circuit of the integrated equivalent circuit. This circuit is functionally analogical to the electrophilic HBN which also has three outputs. T10 represents a voltage controlled current source as well because it corresponds to the strong proton donor K234NZ. With this block-element (as with T1) the output voltages are identical to the input voltage and the currents are different.

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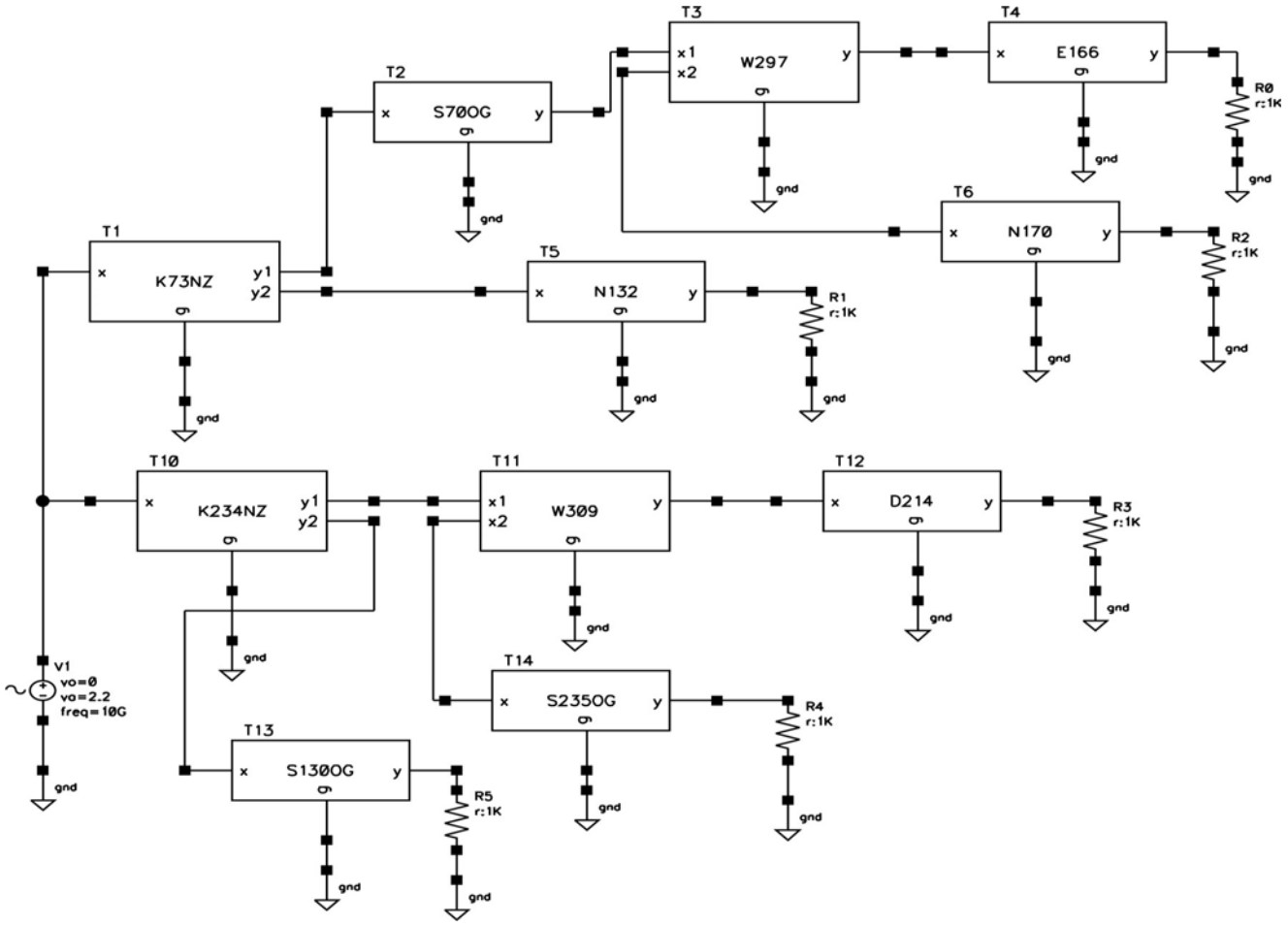

Fig. 2. Equivalent circuit in Cadence Spectre editor.

T11 block-element is analogical to the water molecule W309; the block-element has two inputs and one output.

The D214 residue is juxtaposed to t12 block-element with one input and one output; the latter is the output of the overall circuit.

The three-terminal block-element T13 is similar to S130OG. Its input and output voltages are identical but the currents are different.

The last T14 block-element is functionally analogical to S235OG and it has the same functions as S130OG (and T13 respectively).

Below are listed the equations modeling the equivalent integrated circuit in accordance with the switch position.

Equations 1 and 2 describe the T1 block-element.

$$U_1 = U_{in} \quad (1)$$

$$I_1 = 3\times10^{-5}U_1^3 - 5\times10^{-5}U_1^2 - 7\times10^{-5}U_1 + 0.0013; \quad (2)$$

Equations 3 and 4 describe the T2 block-element.

$$U_2 = 1.0451\times U_1 - 0.1194; \quad (3)$$

$$I_2 = -0.0236\times U_2^3 + 0.0379\times U_2^2 + 0.124\times U_2 + 1.3046; \quad (4)$$

Equations 5 and 6 describe the T3 block-element.

$$U_3 = 1.0179\times U_2 - 0.039; \quad (5)$$

$$I_3 = 0.0015\times U_3^3 - 0.0015\times U_3^2 - 0.0171\times U_3 + 0.0859; \quad (6)$$

Equations 7 and 8 describe the T4 block-element.

$$U_4 = 0.9703\times U_3 + 0.0589; \quad (7)$$

$$I_4 = I_3 = I_{out1}; \quad (8)$$

Equations 9 and 10 describe the T5 block-element.

$$U_5 = 0.0457\times U_1^2 + 1.2273\times U_1 - 0.8501; \quad (9)$$

$$I_5 = 0\times U_5 + 0.0001; \quad (10)$$

Equations 11 and 12 describe the T6 block-element.

$$U_6 = 1.0544\times U_3 - 0.0933; \quad (11)$$

$$I_6 = 0.0058\times U_6^2 + 0.0367\times U_6 + 0.7113; \quad (12)$$

Equations 13 and 14 describe the T10 block-element.

$$U_{10} = 0.9701\times U_1 + 0.2072; \quad (13)$$

$$I_{10} = 4\times10^{-5}\times U_{10}^4 - 6\times10^{-5}\times U_{10}^3 - 0.0002\times U_{10}^2 + 0.0004\times U_{10} + 0.00252; \quad (14)$$

Equations 15 and 16 describe the T11 block-element.

$$U_{11} = 0.9835\times U_{10} + 0.1438; \quad (15)$$

$$I_{11} = 2\times10^{-5}\times U_{11}^3 - 13\times10^{-6}\times U_{11}^2 - 0.00015\times U_{11} + 0.00048; \quad (16)$$

Equations 17 and 18 describe the T12 block-element.

$$U_{12} = 0.9683 \times U_{11} + 0.458; \quad (17)$$

$$I_{12} = I_{11}; \quad (18)$$

Equations 19 and 20 describe the T13 block-element.

$$U_{13} = 1.1009 \times U_{10} - 0.3571; \quad (19)$$

$$I_{13} = 10^{-5} \times U_{13}^4 + 2 \times 10^{-5} \times U_{13}^3 - 8 \times 10^{-5} U_{13}^2 + 2 \times 10^{-5} \times U_{13} + +0.0015; \quad (20)$$

Equations 21 and 22 describe the T14 block-element.

$$U_{14} = 1.034 \times U_{11} - 0.1986; \quad (21)$$

$$I_{14} = 0 \times U_{14} + 0.0001; \quad (22)$$

Afterwards, the equations are coded in Verilog-A and implemented in Cadence to perform a dynamic analysis. The excerpt of the code is listed in Fig. 3.

```
// VerilogA for slA, S70OG, veriloga

`include "constants.h"
`include "discipline.h"
module S70OG (x, y, g);
inout x, y, g;
electrical x, y, g;
electrical Vin;
 analog
  begin
  V(Vin) <+ V(x, g);
  V(y) <+ 1.0451*V(Vin)-0.1194;
  I(x, y) <+ (-
0.0236*V(y)*V(y)*V(y)+0.0379*V(y)*V(y)+0.124*
V(y)+1.3046)*10e-12;
   end
endmodule


// VerilogA for slA, S130OG, veriloga

`include "constants.h"
`include "discipline.h"
module S130OG(x, y, g);
inout x, y, g;
electrical x, y, g;
electrical Vin;
 analog
  begin
  V(Vin) <+ V(x, g);
  V(y) <+ 1.1009*V(Vin)-0.3571;
  I(x, y) <+ (10e-
5*V(y)*V(y)*V(y)*V(y)+2*10e-5*V(y)*V(y)*V(y)-
8*10e-5*V(y)*V(y)+2*10e-5*V(y)+0.0015)*10e-
12;
  end
endmodule
```

Fig. 3. Verilog-A code.

III. TRANSIENT ANALYSIS

The equivalent integrated circuit is functionally analogical to hydrogen bonding networks in the protein's active site. It has 2 inputs and 6 outputs. The transient analysis is performed with sine AC voltage to the two inputs with amplitude between –2.2 and + 2.2 V and frequency of 1 MHz. The output voltages follow the form and frequency of the input voltage but the currents are different. The current in the first output is shown in Fig. 4. It reveals that the current is positive and modulated. The same relation is observed in Matlab simulations as well [9].

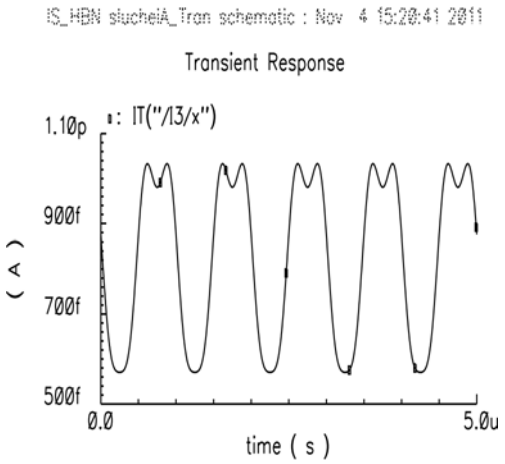

Fig. 4. Output current vs. time relation at output 1.

In Fig. 5 the current versus time relation at output 2 is plotted. Simulations show that this output is similar to the output of a current source, i.e. the current does not depend on voltage changes.

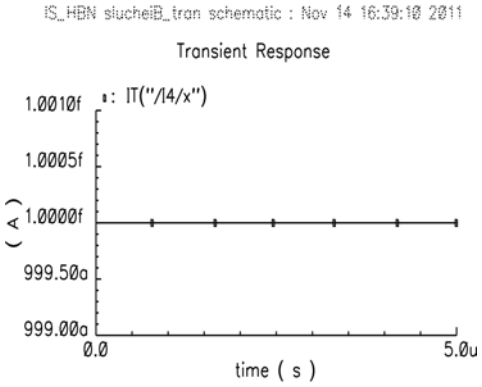

Fig. 5. Output current vs. time relation at output 2.

The output dependence of time at output 3 is given in Fig. 6. The signal here is bottom-limited, i.e. the circuit can operate as amplitude limiter.

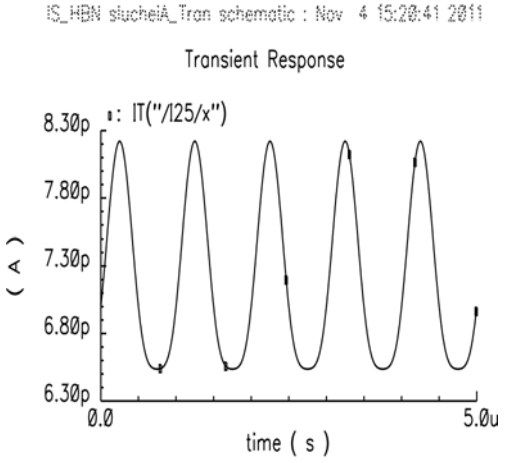

Fig. 6. Output current vs. time relation at output 3.

The other outputs 11 and 12 have differently modulated signals (cf. Fig. 7 and Fig. 8).

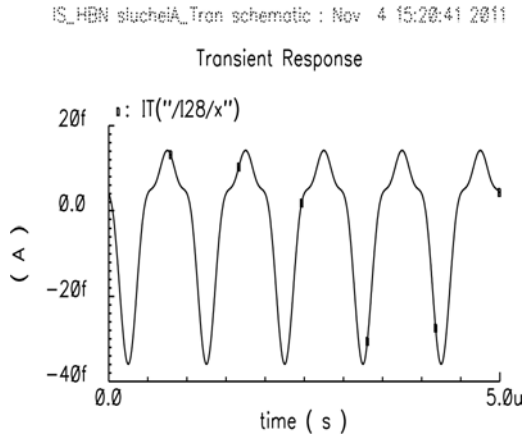

Fig. 7. Output current vs. time relation at output 11.

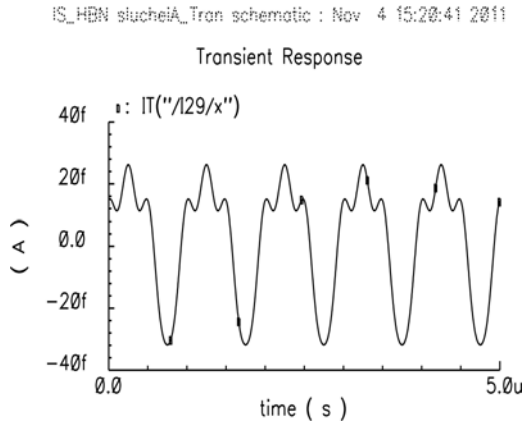

Fig. 8. Output current vs. time relation at output 12.

At the last output 14 we also have a current source with the same magnitude as in Fig. 5, therefore it is not depicted in a figure.

IV. Conclusion

The developed equivalent circuit based on HBN in the active site of the protein shoed that the protein can process information similarly to the conventional microelectronic circuits. The equivalent circuit outputs has the shape of amplitude limiter, current source, and modulator at identical sine input signal.

Acknowledgment

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Cloud Computing in Collaborative Learning in Electronics

Tania Krumova Vasileva, Vassiliy Platonovich Tchoumatchenko and Mariana Dimitrova Manoeva

Abstract – **The paper considers introduction of new pedagogical practices in engineering education to answer requirements of 21st century. It discusses restructuring of Semiconductor Devices course to establish team work on shared reports. Leveraging the cloud to create a self-paced, learner-centered environment is described. Using the new collaborative practices and activities to ensure an enjoyable implementation experience during the pilot course is emphasized. Results from conducted pilots are highlighted. Advantages of cloud collaborative technologies for deeper learning are also commented.**

Keywords – **Cloud Computing, Collaborative Learning, Electronics Education**

I. Introduction

Our world is changing at an unprecedented pace. Skills like critical thinking, communication, collaboration and creativity will be essential for students to take on the challenges and opportunities that lie ahead. In today's world, information and knowledge are increasing at such an astronomical rate that no one can learn everything about every subject, and the jobs that students will get after they graduate may not yet exist.

The revolutionary development of the technology allows access to information in the real world anywhere, at any time. This is even more pronounced for young people who have grown up with technology as an integral and ever-present part of their lives. Today's students are natural investigators, researchers and synthesizers of information. Using technologies in which students are already well versed is a powerful way to support independent, enquiry-based learning and collaboration [1].

Cloud computing environment promotes education with a dynamic content and course delivery. It provides highly scalable and elastic services to end users to exploit technology computing benefits for active learning. These collaborative tools are also very useful for teachers, but the role of the teacher need to change [2].

Universities need to adapt and develop new ways of teaching and learning that reflect a changing world. The purpose of education should be to prepare students for success after graduation. For this reason, students need to be taught how to process, parse, and use information, and they need adaptable skills which they can apply in all areas of life [3].

To answer these challenges we aim at developing pedagogical practices that support collaborative learning in technology-rich environment. The paper discusses efforts done and the experience in restructuring pedagogical practices that offers collaborative learning in the cloud at the Department of Electronics in the Technical University of Sofia. A case study of applying "trialogical" approach to learning in Semiconductor Devices course and the use of cloud computer technologies to support collaborative learning is reported.

II. The Educational Problems and Challenges

The arrival and rapid dissemination of digital technology in the last decades of the 20th century creates a big discontinuity between generations. Today's students are no longer the people our educational system was designed to teach [4]. Loads of information is coming to them via the Internet and everything they do is through the screen: writing, the learning, the reading, downloading and listening to music, designing and even communicating with the world. As a result of this ubiquitous environment and the interactions with it, today's students think and process information fundamentally differently from their predecessors. They are used to receiving information really fast. They like to parallel process and multi-task, and function best when networked.

The problem is that today educational system is designed by assumption that learners are the same as they have always been, and that the same teaching methods will work as before. But this is no longer valid. Our students have changed radically [4]. When teaching them sequentially, steps by steps, giving the same tasks as others students, forcing to write individually the same reports as others, they very fast lose interest and motivation to learn, start rewriting reports from others just to sign for the semester.

This way of conducting training allows some students just to attend in classes without being actively involved in the tasks during the semester. Teachers cannot assess the progress of students as they evaluate the final product of their work. Since the multiple tasks are the same for all students most of them just copy the reports from their colleagues without understanding. Because assessment is based on individual final product, the teacher has thoroughly to conduct face-to-face examination of each student in order to evaluate him correctly.

Realizing that the students are quite different from

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before it's high time to change our view on education. We need to reconsider both the methodology and pedagogical approaches. The human element is a critical component of the educational process. For educators learning new ways to do old stuff is a very hard task.

For the Semiconductor Devices course the educational challenge was to increase the commitment and motivation of students and to meet the requirements of business for:

- Better practical training;
- Team work on common task;
- Shared responsibility for the quality of the overall product;
- Distribution of tasks in line with the specified deadline.

The problem was how to restructure the Semiconductor Devices course in order to:

- Achieve systematic training during the semester,
- Acquire improved students' knowledge and competencies
- Stimulate circuit design and using simulation for project verification,
- Transfer the initiative towards student - teacher direction

III. COURSE RESTRUCTURING

In order to achieve these objectives and resolve problems a new trialogical educational approach [5] was introduced with using cloud computing technologies, up-to-date communication tools for student-teacher connection, continuous monitoring and assistance students' activities.

The problem was how to re-design our course to better promote students' knowledge work competencies and how to implement the trialogical design principles [6] in own teaching. It was inappropriate to use previous experience in conducting collaborative project based learning [7] since these students at their 3rd semester of study haven't any engineering background. We decided to reconstruct the whole course and to adapt design principles as summarized in Table 1 in order to give students opportunity to work collaboratively in group with clear role of each participant.

Trialogical approach was used to address:

- Team work on shared object (report)
- Continuous and prolonged work (within 2 weeks) before the laboratory work.
- Strengthening the tasks of circuit design using devices' data sheets and simulation of the circuits, calculations of circuit's currents and parameters
- Continuous monitoring and teacher assistance in this process, providing help on request
- Reporting on the individual contribution of each team member to the overall project
- Respect to meet the deadline (after the prescribed date the project is locked for editing)

This approach permits for educational methods of direct student-educator contact that are not face-to-face, but are mediated through new communications technologies. Online communication allows students and academics to remain separated by space and time, but to sustain an ongoing dialogue.

TABLE 1. IMPLEMENTING THE TRIALOGICAL DESIGN PRINCIPLES

Design Principle	Implementation in own teaching
DP1: Organizing activities around shared objects	Collaboratively development and preparation of shared reports. Students choose team partners according their interests and preliminary experience.
DP2: Supporting integration of personal & collective agency and work	Motivate students to manage tasks distribution between team members by giving students' responsibility to be team leader in turn. Combining participants' own interests in shared reports through assessment process – the quality of the reports and the responsibilities to deadlines are evaluated with better grade.
DP3: Emphasizing development and creativity through knowledge transformations and reflection	Support flexible use of various kinds of knowledge: theoretical, literary sources; practical examples and cases; pictures, interactive training tools; Make students comment on each other's work throughout the semester, having opponent groups who comment on each other's first drafts not only final report.
DP4: Fostering long-term processes of knowledge advancement	Continuous working process – two week pre-lab design & analysis phase, performing several simulation of explored device characteristics, design circuit using this device and calculate circuit and device parameters. Planning and start writing the documents, sharing the drafts, getting feedback from the teacher, improving the report, using forums and blogs for discussing problems and exchanging views and opinions.
DP5: Promoting cross-fertilization of knowledge practices and artifacts across communities	Students use up-to-date cloud computing and communication tools in order to plan, perform, and organize and wright shared reports. Students and teachers collaborate on solving a shared problem.
DP6: Providing flexible tools for developing artifacts and practices	*Google Drive, Docs, Sheets* – for collaborative editing, reviewing and commenting *Google calendar* – to set deadlines and to monitor progress – assignments, intermediate stages reporting, deadline for final report submission *Google applications*: *Gmail, Calendar, Drive u Google+* for student – teacher communications For in-team communications students can choose their preferred tools (chat, conferences, e-mail, forums)

IV. COURSE ORGANIZATION

Our efforts were aimed at changing the practical training to obtain better skills and competencies. Students work collaboratively in teams of 2-3 persons on shared common report, which is continuously monitored, taking into account the individual contribution of each team member.

Preliminary work performed before starting the laboratory sessions consists of: teams' formation, creating Gmail accounts of all students, development of templates with

tasks to be done for all pre-lab projects and final reports, preparing guidelines for practical laboratory tasks.

Practical training is organized in two-week cycles with the main phases in each cycle as shown in Fig.1.

The environment consists of public cloud based services, combined in a way that supports collaborative electronic design reports development (see Figure 1). All participants had to register individual Google accounts. The teacher was responsible for creating a Google Docs document for each project report and sharing it with the team.

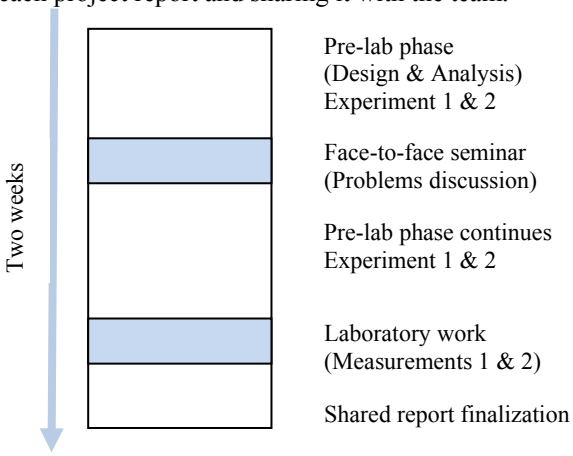

Fig. 1. The main phases of two week work cycle

The goal of pre-lab phase is students to be prepared in advance on device features, which they will explore during the laboratory session. Team need to develop shared report, which includes theoretical and practical topics. Activities during this phase involve schematic capture, graphic drawing, calculation of device parameters, circuit design as well as design verification by simulation.

Intermediate seminar session is predicted for discussion of common problems and difficult subject questions, faced by most students as well as problems with cloud tools used. Activities include questions, answers, slides and computer presentations, and explanation how to use ICT tools.

In the laboratory session students perform practical work with measurement instruments to explore particular devices in different mode of operation, various temperature conditions and signal frequencies. All measured data are filled in directly in shared document by using students' smartphone or computers. There is Wi-Fi in the classroom and students are allowed to access the shared report.

Finalization of shared report includes graph drawing from measured data, parameter calculations, answering problem questions, making conclusions etc.

Students' knowledge is evaluated continuously during the semester and by final exam test. The shared report grade is based on next criteria: material organization, depth of material presentation, handling of questions, resolving problems and clear conclusions on simulation results and measured data. Commenting activities and communications between students and teachers are also appreciated.

V. Cloud Environment

A significant part of the work is done outside regular class (design and analysis, consultations on projects, discussions, teachers' commenting during design phase, in team communications etc.). The environment consists of public cloud based services, combined in a way that supports team work for collaborative development of shared reports (see Fig. 2).

Google Drive, Docs, Sheets are used for collaborative development of a common shared object in the cloud; Google calendar – to set deadlines and progress monitoring (assignments, intermediate stages reporting, deadline for submission of final project).

Fig. 2. Collaborative cloud tools used

All participants had to register individual Google accounts. Completed document on the long-term group work is created in Google Drive as a shared document with the possibility of collaboration between the team members and the teacher. In the shared report can be uploaded files, Word documents, graphics, pictures, waveforms from simulation, measured data from lab exercises and others.
As a specific tools for analysis phase is used LTspice® – free circuit simulation, schematic capture and waveform viewer tool. http://www.linear.com/designtools/software/.

For inter team communications students can choose their preferred tools (chat, conferences, e-mail, forums). For student–teacher communications are used Google applications: Gmail, Calendar, Drive и Google+.

VI. Result from Pilots

The pilots were conducted with 6 students group during autumn semester of bachelor degree courses in Electronics and Computer Systems and Technologies.

In order to describe their opinion and experience of the course and collaborative work students are asked to answer through SurveyMonkey https://www.surveymonkey.com/ to several statements before and after the course and also to following open questions: How would you characterize your overall experience in the course? What has been positive or impressive in the course? What has been challenging or disturbing in the course?

The students' (N=97) answers to the seven statements before and after the course, concerning their ability to work collaboratively in group, are shown in Fig. 3.

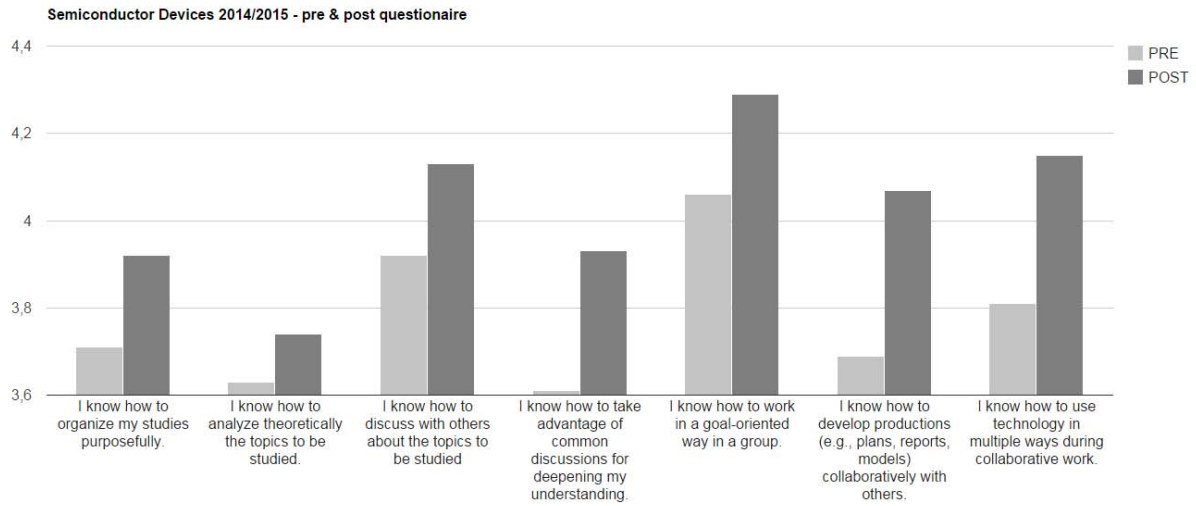

Fig.3. Average of the students' answers concerning the seven statements at the beginning and at the end of the course in Semiconductor Devices

Students consider their first experience to work in teams as very positive, challenging and useful to understand the benefits of collaborative working. Most of them are satisfied with the new way of course delivering and declares that their expectations were exceeded. Innovative way of working in teams using up-to-date cloud computer technologies was appreciated. The positive aspects identified from students are mainly related to the possibility to use and learn new tools, to study in an innovative and engaging way, to have immediate support from teachers by receiving timely feedback and help. The opportunity to work at any time at any place is reported as an advantage, which helps them to manage their free time in more effective way. Students commented that have understood how important is the expertise and commitment of others in development of common products. They also noticed that during team work they started knowing their colleagues better than before, which helps in improving their everyday social contacts and even make new friends.

Some students reports for difficulties in distribution work between team members, for insufficient opportunity to learn from their own mistakes and those of their colleagues and lack of habit to comply with fixed deadlines for projects' submission since after the deadline, the project is locked for editing.

VII. CONCLUSION

The paper considers the problems faced in education of engineering disciplines and an attempt to resolve part of them by introducing new educational practices promoting collaborative learning in bachelor degree course. The "trialogical approach" of learning is applied to the compulsory course on Semiconductor devices in order to introduce team work on shared common report. The benefits of collaborative learning include:

- Development self-management and leadership skills.
- Promotion of active student-teacher interaction.
- Increase in student responsibility.
- Critical thinking and problem solving
- Exposure to diverse perspectives
- Collaboration across networks
- Accessing and analyzing information
- Preparation for real life social and employment situations.

The drawbacks include difficulties in precise evaluation of personal contribution of each team member and inability to force lazy students to actively contribute to the common work. Based on upper mentioned outcomes we will try to improve the next course release by dividing role between students in the team and rotating these roles during the semester and forcing them to comment each other's work.

ACKNOWLEDGEMENTS

The work reported in this paper is a part of the EU project "Promoting Knowledge Work Practices in Education – KNORK", at the TU-Sofia, and was supported by the LLL Program of the European Community.

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Application of Trialogical Design Principles to Practical Education in Networking Technologies

Stela Angelova Stefanova and Radostina Stefanova Gercheva

Abstract – **This paper discusses a course re-design to promote new pedagogical practices applying a trialogical approach. The results from pilot course in Global Networks Education of 12 grade classes in Technology School "Electronic Systems" associated with Technical University of Sofia are demonstrated.**

Keywords – **collaborative learning, knowledge practices, knowledge work competences**

I. INTRODUCTION

The Partnership for 21st Century Learning (P21) [1] has developed a vision for student success in the new global economy.

To help practitioners integrate skills into the teaching of core academic subjects, P21 has developed a unified, collective vision for learning known as the Framework for 21st Century Learning [2]. This Framework describes the skills, knowledge and expertise students must master to succeed in work and life; it is a blend of content knowledge, specific skills, expertise and literacies.

Every 21st century skills implementation requires the development of core academic subject knowledge and understanding among all students. Those who can think critically and communicate effectively must build on a base of core academic subject knowledge.

Within the context of content knowledge instruction, students must also learn the essential skills for success in today's world, such as critical thinking, problem solving, communication and collaboration.

When a school or district builds on this foundation, combining the entire Framework with the necessary support systems - standards, assessments, curriculum and instruction, professional development and learning environments - students are more engaged in the learning process and graduate better prepared to thrive in today's global economy.

The graphic shown in Fig. 1 represents each element distinctly for descriptive purposes, the Partnership views all the components as fully interconnected in the process of 21st century teaching and learning [2].

A. Key Subjects and 21st Century Themes

Mastery of key subjects and 21st century themes is essential to student success. Key subjects include English, reading or language arts, world languages, arts, mathematics, economics, science, geography, history, government and civics.

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In addition, schools must promote an understanding of academic content at much higher levels by weaving 21st century interdisciplinary themes into core subjects:

- Global Awareness;
- Financial, Economic, Business and Entrepreneurial Literacy;
- Civic Literacy;
- Health Literacy;
- Environmental Literacy.

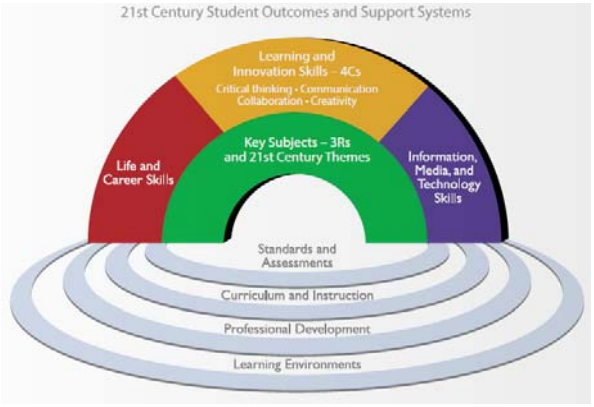

Fig. 1. Components of 21st Century Teaching and learning

Learning and Innovation Skills

Learning and innovation skills are what separate students who are prepared for increasingly complex life and work environments in today's world and those who are not. They include:

- Creativity and Innovation
- Critical Thinking and Problem Solving
- Communication and Collaboration

Information, Media and Technology Skills

Today, we live in a technology and media-driven environment, marked by access to an abundance of information, rapid changes in technology tools and the ability to collaborate and make individual contributions on an unprecedented scale. Effective citizens and workers must be able to exhibit a range of functional and critical thinking skills, such as:

- Information Literacy;
- Media Literacy;
- Information, Communications and Technology (ICT) Literacy.

Life and Career Skills

Today's life and work environments require far more than thinking skills and content knowledge. The ability to navigate the complex life and work environments in the globally competitive information age requires students to pay rigorous attention to developing adequate life and career skills, such as:

- Flexibility and Adaptability;

• Initiative and Self-Direction;
• Social and Cross-Cultural Skills;
• Productivity and Accountability;
• Leadership and Responsibility.

Developing a comprehensive framework for 21st century learning requires more than identifying specific skills, content knowledge, expertise and literacies. An innovative support system must be created to help students master the multi-dimensional abilities that will be required of them. The Partnership has identified five critical support systems to ensure student mastery of 21st century skills [2]:

• 21st Century Standards;
• Assessments of 21st Century Skills;
• 21st Century Curriculum and Instruction;
• 21st Century Professional Development;
• 21st Century Learning Environments.

B. Key features of 21st Century Pedagogy

The key features of 21st century pedagogy are [3]:

• building technological, information and media fluencies;
• developing thinking skills;
• making use of project based learning;
• using problem solving as a teaching tool;
• using 21st century assessment with timely, appropriate and detailed feedback and reflection;
• It is collaborative in nature and uses enabling and empowering technologies;
• It fosters Contextual learning bridging the disciplines and curriculum areas.

To answer these challenges the KNORK (Promoting Knowledge Work Practices in Education) project [4] aims at developing pedagogical models and technology to support collaborative practices in technology-rich environment. KNORK is a 3 year, EU-funded integrated project with 9 partners from 4 countries. The partners represent the synergies between high education institutions and secondary schools in each country.

The paper discusses efforts done in the Technology School "Electronic Systems" associated with the Technical University of Sofia to reconstruct a course and pedagogical practices applying a trialogical approach in Global Networks education. The results from pilot course in Global Networks education in 12 grade classes are highlighted.

II. Trialogical Approach

Present-day students will be employed in positions representing modern knowledge work. These involve abilities of group work, collaborative learning, networking, working in multidisciplinary and multicultural teams, complex problems, and dealing with uncertainty and confusion. This requires new pedagogical practices to be developed to promote necessary competences. Trialogical approach to learning [5] is one possible solution to these challenges.

Trialogical approach builds on the assumption that learning is not just individual knowledge acquisition (monological) or social interaction (dialogical), but activity is organized around transforming, or creating shared knowledge objects (see Fig. 2). While the acquisition and participation approaches provide valuable resources, respectively, for understanding individual and social aspects of learning, these metaphors do not appear to provide tools for understanding deliberate processes of advancing and creating knowledge typical of knowledge-intensive work in the present age. The *trialogical* approach is intended to elicit innovative practices of working with knowledge within educational community [5].

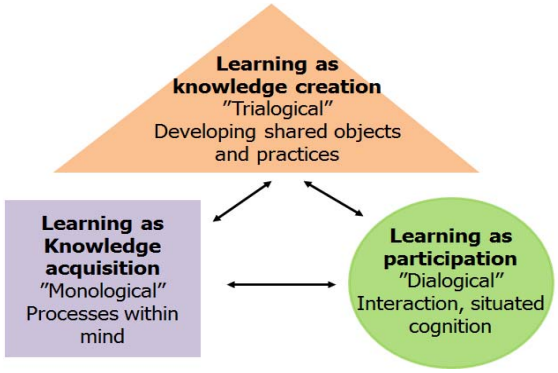

Fig. 2. Three metaphora of learning

III. Course Description and Course Plan

A specialized course in the field of Global Networks, giving the students opportunity to obtain:

• Practical knowledge in networking;
• Ability to use up-to-date professional tools, services and equipment to design networks;
• Skills in teamwork;
• Knowledge in how to manage their work in terms of tasks and time distribution for fulfilling deadlines;
• Ability to present and report their work, considering the problems they face and how they are resolved, or why these problems cannot be resolved.

The practical training of the students in the Global Networks course consists in two major projects during the term, which are made on weekly basis.

The Course Plan has the following main aspects:

Pedagogical context - The students should have passed the specialized courses Local Networks, Informatics, Information technologies from the previous school years.

Previous achievements - The course is taught during the first term of the fifth year and students are expected to use the knowledge, they have obtained previously, for the project.

Prerequisites - Local Networks, Information technologies.

Objectives - The course is designed to give the student an understanding of the different design steps and tools required to carry out operating network.

Knowledge and understanding

• Explain and understand networking basics;
• Explain and understand operation of switches, routers, wireless controllers, access points and firewalls;
• Apply the theoretical knowledge to a project.

Skills and ability - After finishing the course students should have abilities to:

• Use modern professional tools for network design and implementation;
• Work efficiently as a group;
• Manage their work in terms of tasks and time distribution for achieving deadlines;
• Present and report their work considering the problems they face;
• Hold and evaluate, discuss and justify the proposed solutions;
• Make peer reviews and comment results.

ICT tool(s) - Networking equipment such as routers, switches, cables, etc. Google Doc, Google Application, Google Drive, Google Sites.

Preparations before the course - Find potential projects. Prepare the platform (Google Apps): create folders for the groups, the workspaces, upload learning material, allocate projects themes according the groups, create project development agenda.

IV. COURSE RE-DESIGN

We re-design our course to ensure possibilities for collaborative work of student teams on common shared tasks. The trialogical design principles, described in section II, are used in the process of course re-organization. The implementation of the principles of trialogical approach can be summarized in following way:

DP1: Organising activities around shared objects

• Teams organization - students will have the ability to choose their teams by yourself.
• Collaborative development of common project, and preparation of shared;
• Task distribution between the members of a team;
• Activities: regular meetings for discussion of project tasks and preliminary review of the used tools and the progress of the project development.

DP2: Supporting integration of personal and collective agency and work

• Coordinating participants – team members will choose the partners they want to work with;
• Motivating students to distribute tasks between team members take the responsibility for the project deadline;
• Collective responsibility - in the group each member takes the responsibility for their project tasks.

DP3: Emphasizing development and creativity through knowledge transformations and reflection

• Discussion and analysis of problems the teams faced during their collective work on the common project;
• Thoughtfully and creatively establish, conduct and operate the project development;
• Practice already gained knowledge and skills in using dedicated networking equipment to solve the tasks of the project.

DP4: Fostering long-term processes of knowledge advancement

• Prolonged working process with iterative network configuration – performing number of analysis of the designed network to refine the network parameters and characteristics;
• Planning and writing the documentation, sharing the drafts, asking the teacher and other students for feedback, improving the project and project documentation, submitting respective report and presenting the obtained design and simulation results;
• Using forums, blogs and social media for discussing problems and talk about their points of view and opinions.

DP5: Promoting cross-fertilization of knowledge practices and artifacts across communities

Students contribute with specialists from the ICT industry. Industry professionals, teachers and students discuss and analyze collaborative experience. Students use modern professional tools in order to plan, organize, and execute the project tasks and write project documentation.

DP6: Providing flexible tools for developing artifacts and practices

Students use the tools for collaborative work:
• Google Docs for collaborative editing and commenting; Google Drive for file sharing; Google+ for discussions;
• Project management – Google Apps;
• Google Calendar - very useful for project scheduling - related events by sending RSVP invitations;
• Google Sites – for designing of course site;
• Face to face and virtual meetings – Skype.

V. COURSE ORGANIZATION

The Global Networks course in the Technology School "Electronic Systems" is re-designed to be project oriented. Working in teams of 2 persons, the students are required to performing number of analysis of the designed network to refine the network parameters and characteristics. During the long term projects teams have to gather information, discuss the given problem in collaborative environment, analyze and troubleshoot the network topology applying pre-defined networking technologies and protocols. The students have to document their work at every step of the development process and to upload in Google Drive project space. In the end of the two or three weeks long projects students will have to present their presentations for the given topics. The students will have weekly assignments, developed collaboratively-shared presentations in the field of Global networks. These homework activities are presented, discussed and analyzed in class.

The assessment is based on the written project report and the discussion with the project team. The evaluation criteria are: fulfillment of design goal according given technical specifications, quality of the design solution, meeting the deadlines for submission of intermediate and final reports, quality of the written reports.

VI. COLLABORATIVE LEARNING PLATFORM

During the long term projects and weekly assignments on the subject of Global Networks students have to gather information, discuss the given problem in collaborative environment, collect the needed information, analyze the topics for the presentations. Most of developments take place outside the regular classes. For their intra-team

communication, the students are free to choose whatever tools they prefer (chat, conferencing, email). For student-teacher communications we decide to use the Google tools (see Fig. 3): Groups, Gmail, Docs, Talk, Calendar, Drive and Google+. Students were encouraged to submit their questions as emails instead of chat messages.

The students will have to document their work at every step of the development process of long term projects and weekly assignments. They have to create, edit and comment the collaborative documents in the different Google Drive Spaces.

Fig. 3. Collaborative workspace structure

These homework activities are presented, discussed and analyzed in the class and uploaded in Google Site of the Global Networks Course (See Fig. 4., and Fig. 5.).

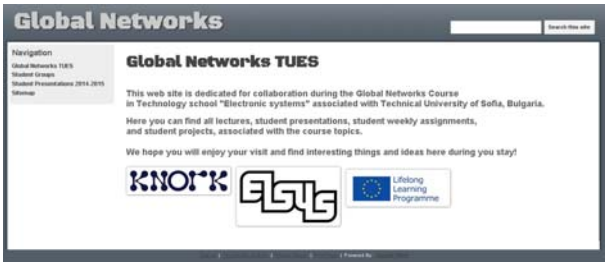

Fig. 4. Home Page of Google Site of Global Networks Course

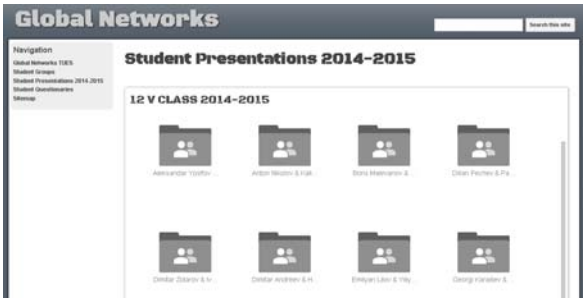

Fig. 5. Students Projects in Global Networks Course

VII. Results from Pilot Course

The pilot course is conducted with one class of 29 students – 12 grade class (31 weeks). Each team had to choose a project subject from a list provided by the teacher. In addition to the project work, students were required to submit several homework assignments.

All participants had to register individual Google accounts. The teacher was responsible for creating a Google Docs document for each project report and sharing it with the team.

We manage to transform course from classical face to face teaching to using project based approach in order to motivate student and increase students motivation, their knowledge work competences and digital skills. The main results and experiences can be generalized as follows: 1) Students work in a collaborative environment with shared documents; 2) Experience in the use of modern cloud technology; 3) Experience in the rearrangement of the course content; 4) Creation of a web-based Global Networks course platform.

In the beginning of the course a pre-survey was done through Survey Monkey. A questionnaire was sent to the students in order to find out more about their background and study skills. After the course the post-questionnaire is done to evaluate students' self-reflections concerning knowledge work practices related to their experiences in the implemented Global Networks course and to observe their progress. The students were asked several questions: 1) I know how to organize my studies purposefully; 2) I know how to analyze theoretically the topics to be studied; 3) I know how to discuss with others about the topics to be studied; 4) I know how to take advantage of common discussions for deepening my understanding; 5) I know how to work in a goal-oriented way in a group; 6) I know how to develop productions (e.g., plans, reports, models) collaboratively with others; 7) I know how to use technology in multiple ways during collaborative work.

The 29 students' answers to the seven statements after the course are reported in Fig. 6 together with their answers to the statements before the course.

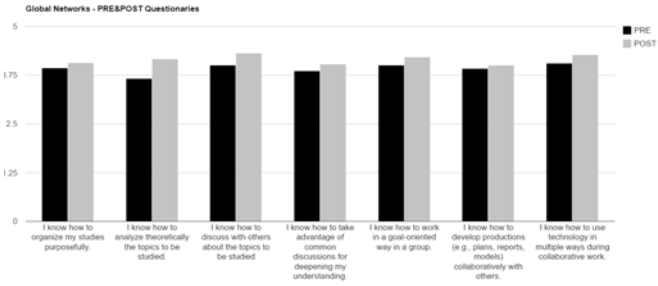

Fig. 6. Average of the students' answers

VIII. Conclusion

The paper discusses a course redesign to promote new pedagogical practices, which were successfully used for improving obligatory course Global Networks in secondary education.

Pilots' results are focused on students' collaboration for shared outcomes. Students learned knowledge work practices - information analysis and presentation, sharing, commenting, using digital tools and team work. We need to find ways to promote even further the collaboration between the students and monitor their group and individual progress. The Global Networks course has room for improvement in the following directions: 1) Optimal distribution of students in groups - not only according to their desire; 2) Criteria for evaluation of responsibilities in teams, according to the complexity of the project; 3) Update the criteria for the assessment of current tasks and

defining the severity of these criteria in forming the final course grade of the individual team members.

ACKNOWLEDGEMENT

This paper is a part of the EU project “Promoting Knowledge Work Practices in Education – KNORK”, at the Technology School “Electronic Systems” associated with Technical University and was supported by the Lifelong Learning Program of the European Community.

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Analyzing Collaborative Artefacts in Project Based Courses

Vassiliy Platonovitch Tchoumatchenko

Abstract – **The paper explores the problems and suggests some solutions in evaluating contributions of each author in collaboratively created artefacts. It reflects our experience of using Google Docs and other cloud based instruments in project based courses for undergraduate students. A new tool for analyzing document's revisions and contributions is discussed.**

Keywords – **Google Docs, collaborative writing, project based learning.**

I. Introduction

In the last two years, several engineering courses at the Technical university of Sofia were re-designed using trialogical design principles and modern digital technology. The courses were restructured from traditional face-to-face to project oriented adopting and applying modern online learning platforms, cloud collaboration tools and social software.

Introducing new technologies and paradigms in established engineering courses is always challenging. In addition to the core subject matter, students had to learn new tools and development workflows.

Overall, the trialogical approach was well accepted and considered as an appropriate path for transforming students' individual course work into more collaborative activities.

Writing collaboratively, however, takes coordination and awareness of who has done what. Each student's activity and contributions to the collaborative project is influential (but not definitive) in determining the final grade. On the other hand, being able to analyze how the project report evolved over time can reveal interesting patterns of collaborative writing.

II. Related Work

Collaborative writing is on the increase and many researchers have created tools to analyze documents evolution. One such tool, DocuViz [1], displays the entire revision history of Google Docs, showing more than the one-step-at-a-time view now shown in revision history. DocuViz is potentially useful in cases such as: To authors themselves to see recent "seismic activity," indicating where in particular a co-author might want to pay attention, to instructors to see who has contributed what and which changes were made to comments from them, and to researchers interested in the new patterns of collaboration made possible by simultaneous editing capabilities.

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Another tool for analyzing Google Docs history is Draftback [2]. It shows the timeline of the changes, and below it, a "map" that tells where in the document each of those revisions happened. Draftback is implemented as a Chrome extension and is able to playback the complete history of every single character.

Unfortunately, none of these tools is open source. This makes it difficult to adapt and integrate them in our collaborative learning infrastructure.

III. Infrastructure for Collaborative Learning

The infrastructure for collaborative learning [3] consists of public cloud based services, combined in a way that supports electronic design workflow (fig. 1). Working in small teams, the students are required to design a digital integrated circuit. The design workflow is based on HDL modelling, verification and synthesis. The main design artefacts (VHDL models and test-benches) are text files; therefore we are able to borrow many tools and workflows from the software development community. Projects are hosted on GitHub [4] – one repository per project. In parallel with the code development, the teams are required to create and maintain a Google Docs document which is one of the major deliverables. Initially the document contains the technical specifications of the design. Later on, the students have to add description of the implemented algorithms and architectures, argumentation of the tradeoffs made and the results from the simulation, synthesis and physical design. Most of development takes place outside the regular classes. For their intra-team communication, the students are free to choose whatever tools they prefer (chat, conferencing, email). For student - teacher communications we decide to use the Google tools: Gmail, Docs, Talk, Calendar, Drive and Google+. Students were encouraged to submit their questions as emails instead of chat messages.

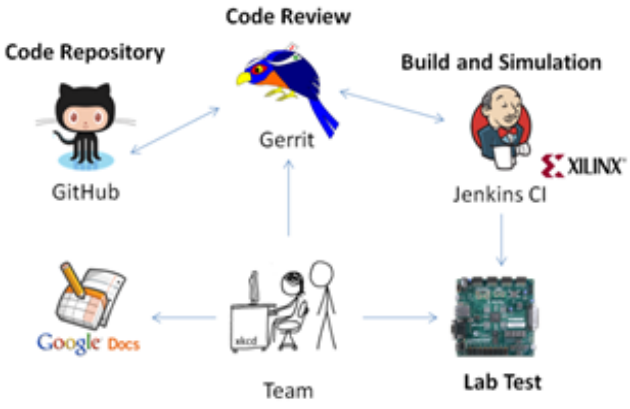

Fig. 1. Collaborative workspace

IV. Collaborative Artefacts Evolution

A. GitHub Revision History

GitHub is optimized for hosting software projects. It provides a very detailed history of commits for each repository (fig. 2). Each commit is attributed to an author. A single commit usually consists of changes in multiple files. Each change can be individually inspected (fig. 3). In the majority of cases, the tools provided by GitHub are more than adequate for analyzing the evolution of the students projects.

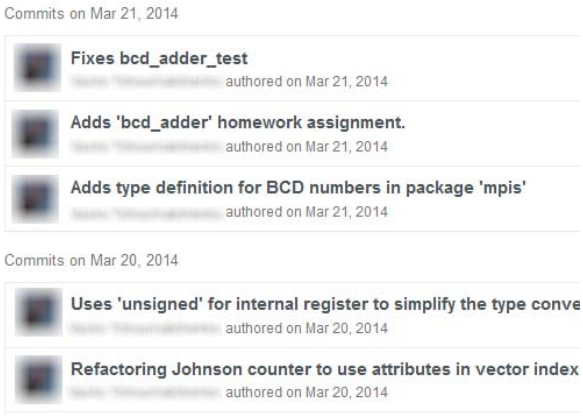

Fig. 2. GitHub commits history view

Fig. 3. GitHub diff view

B. Google Docs Revision History

The functionality offered by Google Docs with respect to exploring documents history is rather limited. At a file level, there is an activity view (fig. 4), that provides a good overview of when and who created or modified a particular document.

At document level, we have a revision history (fig. 5) which shows a timeline of the changes, but no information about the scope of each change. Therefore a simple formatting modification and a substantial text contribution are indistinguishable in the revision history view. Clicking on a particular revision, reveals the document content with all relevant text changes colored. It's quite frustrating that there is no way to quickly locate the changes – the user has to scroll through the document and look for a colored text. Some changes as added or deleted figures are not indicated at all.

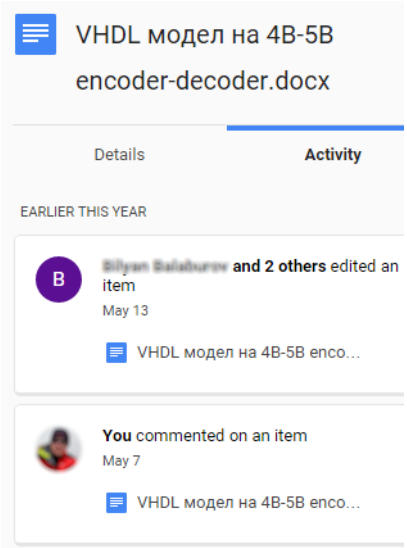

Fig. 4. Activity view.

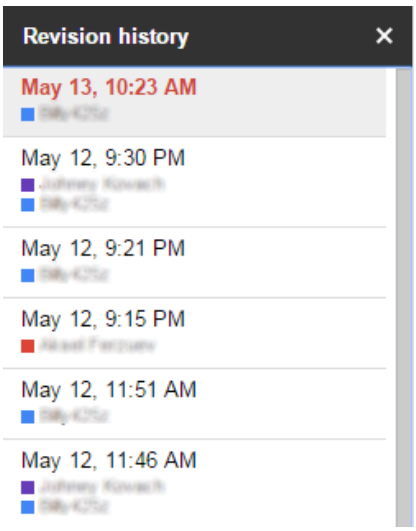

Fig. 5. Revision History View

V. A New Tool for Exploring Google Docs History

To facilitate the exploration of collaboratively created project artefacts, we developed a new application for analyzing Google Docs revision histories. The following design requirements were specified:

- The changes in each revision should be visualized in a way, similar to the one used by GitHub (fig. 3).
- The application should find word-level changes.
- Formatting changes (e.g. fonts, colors) should be ignored.
- It should be possible to show all contributions of a particular author.

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8B/10B encoder/decoder е устройство което, [-първо кодира 8 битова-]{+извършва както кодиране на 8-битова+} дума в [-10 битова, след ^Y-]
[-което информацията се пренася-]{+10-битова, ^Y+}
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[-от 10 бита отново на 8.-]{+обратното декодиране.+} На схемата долу е представена точно такава система. Тя се използва
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съставен от 8 битов паралелен вход и 10 битов изход. Този 10 битов изход е зареден във
високоскоростен [-Serializer (това е 10 битов Shift регистър с-]{+преобразувател от+} паралелен [-вход и сериен ^Y-]
[-изход).-]{+в последователен код .+}
След [-което-]{+това+} информацията се предава до високоскоростен Deserializer (10 битов Shift
регистър с паралелен изход и сериен вход) в страната на приемника и се преобразува от
серийна до паралелна. Декодера [-обръща информацията-]{+преобразува данните+} от 10 [-битова до-]{+битови в+} 8 [-битова.-]{+битови.+} Когато се
използва 8B/10B кодираща схема, серийното предаване на информацията е DC – балансирано,
това означава че се изпраща еднакво количество от нули и единици за даденатa дължина на
предаваната информация и максимална run-length без преходи от 5. Run-length се дефинира
като максималния брой на нулите и единиците предавани в серийния пренос на информацията.
Тези две характеристики помагат във възстановяването на информацията и [-clock-a-]{+синхронизация на^Y+}
{+тактовия сигнал+} в приемника.
```

Fig. 6. Differences between two revisions – wdiff format

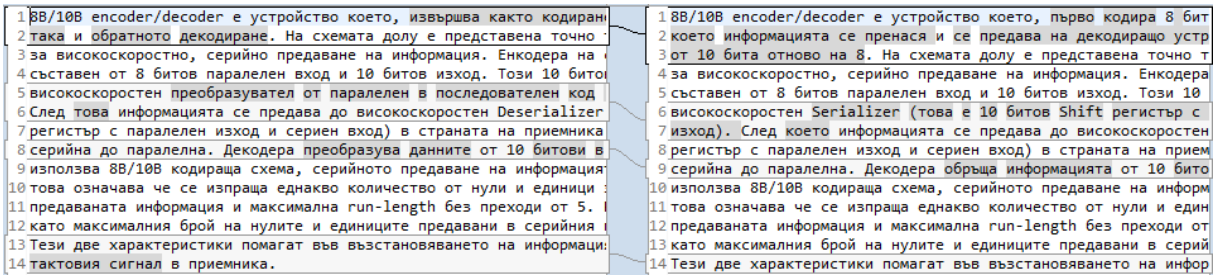

Fig. 7. Differences between two revisions – UI mockup

- The application should use public Google Docs API [5].
- The application should be cross-platform – both desktop and mobile devices should be supported.

To fulfill the cross-platform requirement, the document history exploration tool was implemented as Google Chrome extension [6]. This allows for a natural UI integration – the user can open a Google Docs document in her Chrome browser and then start the application from the browser's toolbar.

The application's UI is still work in progress. Presently, the differences between revisions are shown as text based output (fig. 6). The added and deleted words are marked in a way similar to the output of the wdiff utility [7]. In the final implementation, the compared text will be shown next to each other and the differences will be indicated by different colors (fig. 7).

VI. Conclusions

We presented in this paper our experience in analyzing the artefacts of collaborative design projects. We have implemented an application that shows the changes in each document revision and the contributions of each author in a more usable format than the native Goggle Docs revision history. We believe that such tool can be useful both for the authors of the document and for the professor, who evaluates the project.

Acknowledgement

The work in this paper is a part of the EU project "Promoting Knowledge Work Practices in Education – KNORK" at the Department of Electronics - Technical University of Sofia, which is supported by the Lifelong Learning Program of the European Community.

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[3] T.Vasileva, V. Tchoumatchenko, S. Stefanova, Introducing Trialogical Knowledge Practices in Higher and Secondary Education, The 3rd Electronic International Interdisciplinary Conference (EIIC), Virtual Conference, September, 1 - 5, Slovakia, 2014, pp. 580-585, ISBN: 978-80-554-0921-4
[4] https://github.com/
[5] https://developers.google.com/drive/v2/reference/
[6] https://developer.chrome.com/extensions
[7] http://www.gnu.org/software/wdiff/

Web Based Tool for State Machines Design

Vassiliy Platonovitch Tchoumatchenko

Abstract – **The paper describes a web based tool for designing finite state machines (FSM). The user specifies a state machine by drawing a diagram, from which the tool generates a synthesizable VHDL model. The intended application of the software is to help student in learning HDL based design of electronic circuits.**

Keywords – **Finite State Machine (FSM), state diagram, VHDL**

I. Introduction

In the context of electronic design automation, a finite-state machine (FSM), or simply a state machine, is a mathematical model used to design sequential logic circuits. It is defined by a list of states, the triggering condition for each transition and the output values. The state machines are convenient formalism for specifying the behavior of control circuits. As such they are often used in the digital circuits design.

FSMs can be represented graphically, which would help the designer to visualize and design in a more efficient way. Most modern digital IC design flows are based on hardware description languages (HDL). Therefore, the designer requires a straightforward way to convert the visualized design to HDL code in order to simulate and implement it. The procedures for such conversions are well defined and can be implemented as a design automation tool. Such tool can be especially helpful for students, who are learning digital design and HDLs.

The task of converting state diagrams to HDL code is addressed be several existing tools, both open-source and commercial – [1], [2], [3] and [4]. What these tools have in common is that all require local installation. Since our goal is to move as much as possible of the student's design works in a web-based collaborative environment, this is a serious drawback.

II. Tool Structure

The tool consists of state diagram editor; JSON store and HDL model generator services (fig. 1). The user interface is implemented in JavaScript and HTML5, which makes it accessible on both mobile devices and desktop computers [5], [6].

The serialized state diagrams are persisted in a JSON store – which can be either a private database installation (e.g. CouchDB) or a cloud based service like GitHub [7].

Once the state diagram is finished, it is sent to the selected HDL generator. At the time of writing, the VHDL generator is already available and a System Verilog generator is under development. The state diagram is analyzed and suitable messages are produced if inconsistencies are found. After the validation, a HDL model is generated and transferred back to the UI. The HDL generators are implemented as web services.

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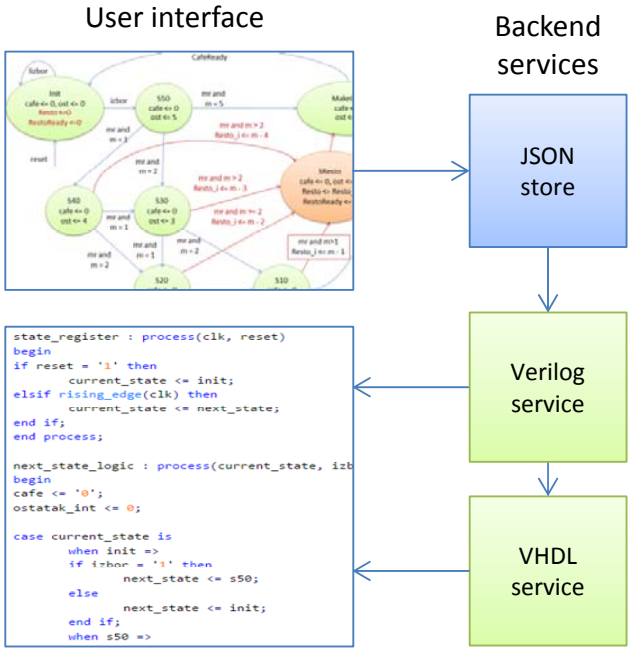

Fig. 1. Components of the FSM tool

III. Tool Functionality

A. State Diagram Editing

The primary design entry method of the FSM tool is a state diagram editor (fig.2). Both Moore and Mealy state machines (fig. 3) are supported. If the output assignments are defined only in the states, than a Moore state machine will be generated. Alternatively, if there is output assignments associated with the transitions, the tool produces model of a Mealy FSM.

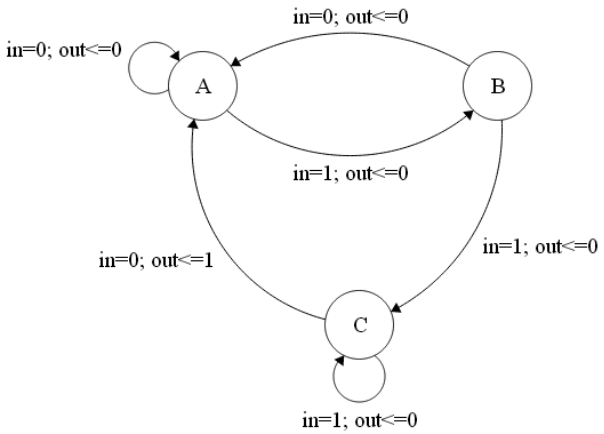

Fig. 2. FSM state diagram

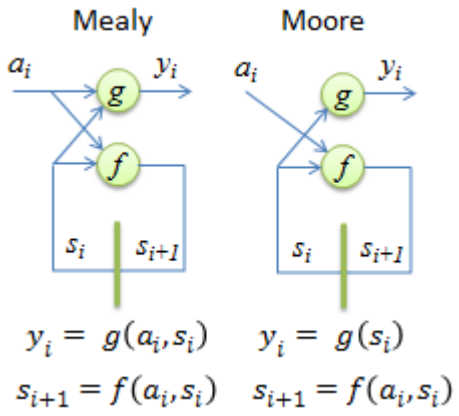

Fig. 3. State machine types: (a) Mealy, (b) Moore

B. HDL Code Generation

By default, the VHDL code generator implements a three-process approach to structuring the FSM code (fig. 4). One sequential process models the state register (fig. 5a) and two combinational processes describe the next state logic (fig. 6) and the output logic (fig. 7). For smaller state machines, the user has an option to choose a two-process architecture, where the two combinational processes are merged into one.

The VHDL generator uses symbolic state enumerations (fig. 5b), so that the actual state encoding can be decided at the synthesis stage. This allows the designer to explore the effect of the state encoding algorithm (e.g. one-hot vs Gray vs binary) on the produced circuit. The next state logic process contains code for recovering from parasitic states (fig. 6a).

```
architecture v1 of sequence_recognizer is
    type fsm_states is (a, b, c);
    signal current_state : fsm_states;
    signal next_state : fsm_states;
begin

state_register: process(clock, reset)
begin
    if(reset = '1')then
      current_state <= a;
    elsif(rising_edge(clock))then
      current_state <= next_state;
    end if;
end process;
```

a

b

Fig. 5. Symbolic state type (a) and state register (b).

```
nsl: process (current_state, input)
begin
  case current_state is
  when a =>
    if(input = '1')then
      next_state <= b;
    else
      next_state <= a;
    end if;
  when b =>
    if(input = '1')then
      next_state <= c;
    else
      next_state <= a;
    end if;
  when c =>
    if(input = '0')then
      next_state <= a;
    else
      next_state <= c;
    end if;
  when others =>
    next_state <= a;
  end case;
end process;
```

a

Fig. 6. Next state logic process.

```
ol: process (current_state, input)
begin
  case current_state is
  when a =>
    output <= '0';
  when b =>
    output <= '0';
  when c =>
    if(input = '0')then
      output <= '1';
    else
      output <= '0';
    end if;
  when others =>
    output <= '0';
  end case;
end process;
```

Fig. 7. Output logic process.

IV. EDUCATIONAL APPLICATIONS

The described tool is include in the HDL based IC design workflow used by some of the 4-th and 5-th year students at the Department of Electronics, TU-Sofia.

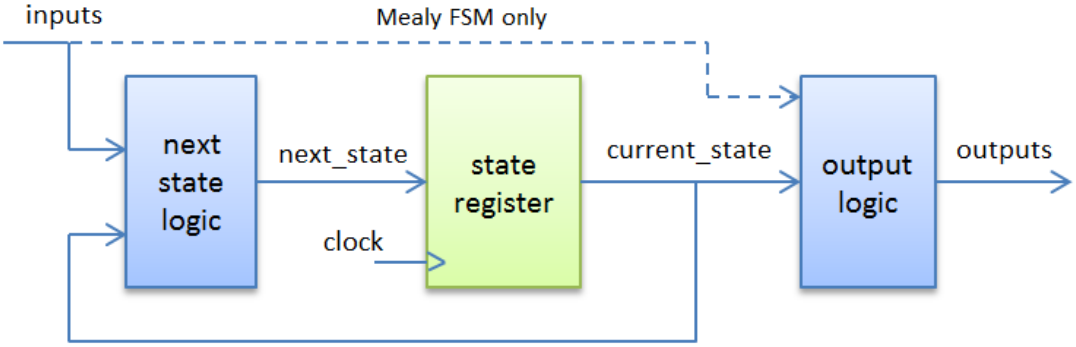

Fig. 4. Three-process FSM architecture.

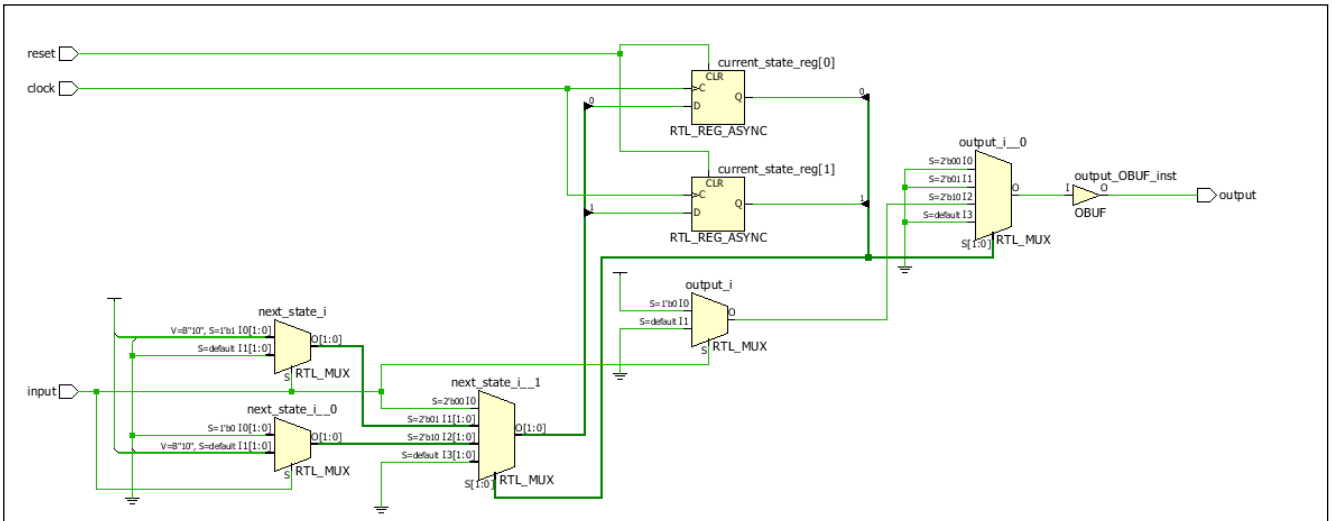

Fig.8. Synthesized circuit (Xilinx Vivado)

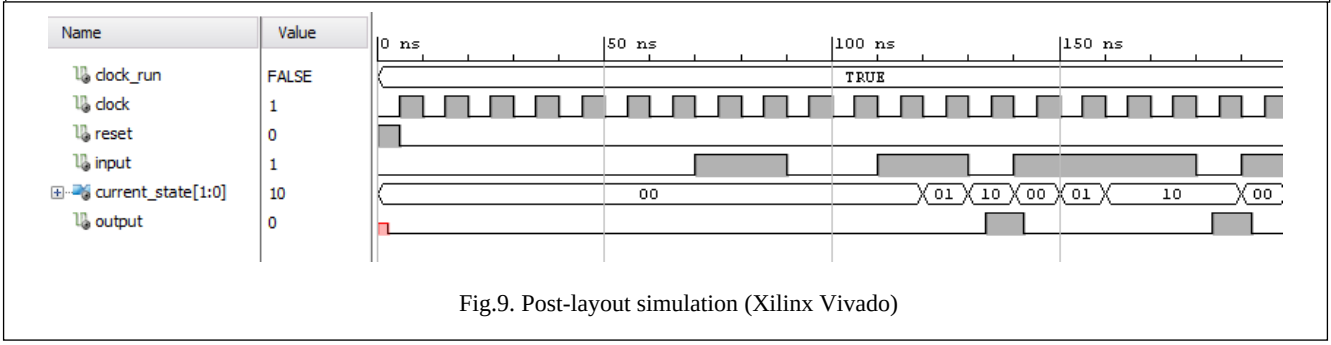

Fig.9. Post-layout simulation (Xilinx Vivado)

The students are required to work on multiple homework assignments and a final project. They can accomplish most of the front-end design (design entry and simulation) and all of the report preparation by using web based tools – EDA Playground [9], Google Docs, and the FSM tool described in this paper.

For the synthesis, physical design and post-layout simulation (fig. 8, 9), the students can use Xilinx Vivado [10]. It is available in the lab or the students can install a free Vivado version on their own computers.

V. Conclusion

The paper considers features, architecture and software implementation of the developed design automation tool for converting state diagrams to VHDL code. The web based nature of the FSM design tool facilitates its integration with similar design automation tools for code editing and HDL simulation. Together they can be used to support on-demand, self-paced learning of digital IC design.

Acknowledgements

The work in this paper is a part of the EU project "Promoting Knowledge Work Practices in Education – KNORK" at the Department of Electronics - Technical University of Sofia, which is supported by the Lifelong Learning Program of the European Community.

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Teaching Stepper Motors and Brushed DC Motors Using the Medium Voltage Digital Motor Control Platform, Part I - Stepper Motors Control

Ivan Petrov Maradzhiev, Tsvetana Grigorova Grigorova and Svetoslav Tsvetanov Ivanov

Abstract – **Development of the modern power electronics puts serious challenges to the teaching of the industrial electronics students, due to the complexity of the necessary knowledge and skills. In this paper we discussed the teaching methodology of stepper motors control, using Texas Instruments platforms and the main points of the students teaching process during the laboratory work.**

Keywords – **Stepper motors, Microstepping, Digital motor control**

I. INTRODUCTION

Development of the modern power electronics puts serious challenges to the teaching of the industrial electronics students, due to the complexity of the necessary knowledge and skills. Experience shows that power electronics as a subject is not readily assimilated by students because of the different areas involved [1]. Although students expressed interest in power electronics integrated with digital controls and digital signal processor (DSP), the conventional teaching arrangement did not give them needed background and knowledge [3].

For the postgraduate students the laboratory experiments are very important part from the education and can help students assimilate the theoretical concepts of very complex subjects. In order to prepare students for the employers organizations requirements [2] we offered students an eligible course entitled “Electronic converters for motors control" as a part of the Master's program in "Electronics". Discipline is fundamental to the knowledge and skills of students in the field of power electronic circuits and devices for motor control (Stepper motors, Brushed DC, Brushless DC and AC motors). One major part of it is focus on digital motor control. The use of the digital motor control allows more complex and more intelligent types of motor control. During the last three years, we have seen a noticeable increase of student interest in this subject, as evidenced by the number of registered, which is more than 80% from all students from the Master's program in" Electronics".

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In this paper we discussed the teaching methodology of stepper motors control, using Texas Instruments platforms. As a development environment was chosen the Medium Voltage Digital Motor Control (DMC) kit, DRV8412-C2, from Texas Instruments (TI), which provides a great way to learn and experiment with digital control of medium voltage motors. In the DRV8412 DMC kit are included two brushed DC motors and 8-wire bi-polar stepper motor [5].

The present report examines the implementation of one of the control methods for bipolar stepper motor - microstepping and the main points of the students teaching process during the laboratory work.

II. MICROSTEPPING OF BI-POLAR STEPPER MOTORS

At the beginning of the laboratory session, the teacher gives a brief explanation, presenting an overview of the experiment and the relation with the theory.

Stepper motors are a good choice when precise control of the movement is required. They are used for applications in which to control the rotation angle, the speed and position of the rotor are required. Their advantages have obtained their place in the various fields of the engineering, such as medical equipment, robotics, automotive and others. There are different methods to control stepper motors. One of them microstepping works on the principle of gradually transferring current from one winding to another. This is achieved by pulse-width modulating the voltage across the windings of a motor. The duty cycle of the signal charging one winding is decreased as the duty cycle of the signal charging the next winding is increased. The desired motion of a stepper motor is linear. Good implementations of microstepp drive strive to get as near to this linear motion as possible [4]. Figure 1 shows a waveforms of torque vs. rotor position for an ideal two-winding stepper motor [4].

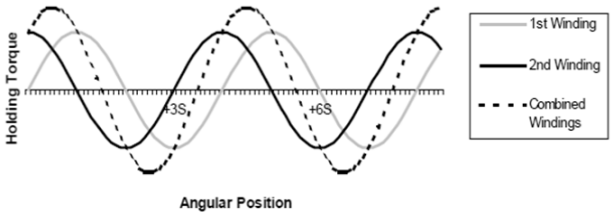

Fig.1. Torque vs. angular position for an ideal two winding motor

The torque curve for one winding of the ideal two winding stepping motor in Fig. 1 can be expressed by the following equation:

$$T_1 = H \sin\left(\frac{\pi}{2}\frac{\theta}{S}\right) \quad (1)$$

$$T_2 = H \cos\left(\frac{\pi}{2}\frac{\theta}{S}\right), \quad (2)$$

where: T_1 – torque of the first winding; H- holding torque; S – step angle, [rad]; θ – shaft angle, [rad].

In an ideal motor, the torque produced by each winding is proportional to the current in that winding. As a result, if we want to hold the motor rotor at the angle θ, we can do so by setting the currents through the motor windings to the values given in Eq. 3 and Eq. 4.

$$I_1 = I_{MAX} \sin\left(\frac{\pi}{2S}\theta\right) \quad (3)$$

$$I_2 = I_{MAX} \cos\left(\frac{\pi}{2S}\theta\right), \quad (4)$$

where I_{MAX} is maximum current through the motor windings.

A. The Medium Voltage Digital Motor Control (DMC) kit description

At the beginning of the laboratory work, students are given a tutorial that guides them through the hardware description, the experiments and the actions to be performed in each step.

Fig.2 shows the block diagram of the DRV8412 evaluation kit (DRV8412-C2-KIT). It consists of the DRV8412 motor driver, a C2000 Piccolo F28035 MCU controlCARD, example software, code development environment (Code Composer Studio) and the motor.

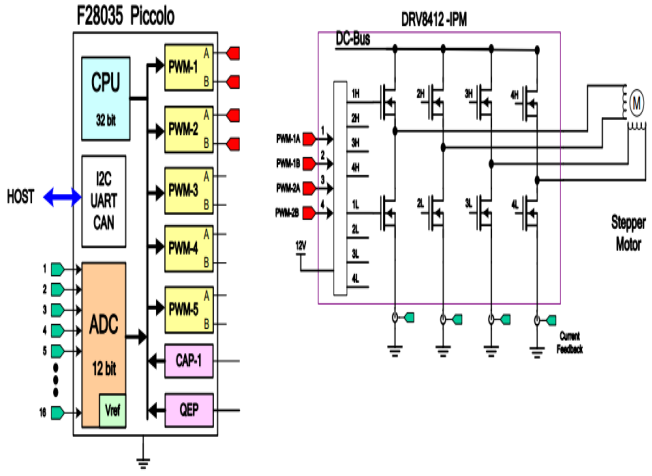

Fig. 2. Stepper motor drive implementation

This system demonstrates current-controlled microstepping of a bi-polar stepper motor. The stepper motor is driven by a H-bridge, which is provided by the DRV8412 Dual Full-Bridge PWM Motor Driver IC. The Piccolo F28035 MCU controlCARD generates four pulse-width modulation (PWM) signals, two for each motor phase. Two phase currents of each motor phase are measured from the H-bridge and sent to the F28035 device through four analog-to-digital converters (ADCs). In addition, the DC-bus voltage is measured and sent to the F28035 through an ADC [5].

This highly integrated, robust motor control and driver solution allows developing for stepper motors.

For the proper work we put Mode Jumpers as follows: M1=H, M2 = M3 = L (mode 2 of DRV8412). This mode means: dual full bridges or four half bridges with OC latching shutdown. The software available with the kit is completely open source and allows both to be studied from the students and to be modified. Furthermore, there is a possibility to change the motor control algorithm, and can be choose between modes microstepping with different sizes of step, quarter step, half step and a full step. Thus, students acquire practical skill and obtained knowledge about the most common methods for the stepper moors control. Also, students can change the base electrical frequency of pulses, references voltage and current for the used motor.

Except the development board the necessary equipment includes a personal computer with an installed development environment Code Composer Studio v6.0, the oscilloscope and current probe.

B. Projects Organization

The project is built up into three levels, with each level test modules and software is checked for the proper operation of the hardware [6]. The platform allows change and adjustment of various parameters in real time. The project can be configured in Stepper-Settings.h header file and can range from whole stepping to 128 microsteps/step.

```
define   BUILDLEVEL LEVEL1

#define WHOLE_STEPPING          2
#define HALF_STEPPING           3
#define QUARTER_STEPPING        4
#define MICROSTEP_8             5       //8-microsteps
per step
#define MICROSTEP_16    6       //16-microsteps per step
#define MICROSTEP_32    7       //32-microsteps per step
#define MICROSTEP_64    8       //64-microsteps per step
#define MICROSTEP_128   9       //128-microsteps per step
#define MICROSTEPS      HALF_STEPPING
// Define the system frequency (MHz)
#if (DSP2803x_DEVICE_H==1)
#define SYSTEM_FREQUENCY 60
#elif (DSP280x_DEVICE_H==F2808)
#define SYSTEM_FREQUENCY 100
#endif
// Define the ISR frequency (kHz)
#define ISR_FREQUENCY 10
// Select the motor
#define Motor 1
// Define the base quantites
#define BASE_VOLTAGE    66.32   // Base peak phase voltage
(volt), maximum measurable DC Bus
#define BASE_CURRENT    7.2  // Base peak phase current
(amp) , maximum measurable peak current
#define BASE_FREQ       200     // Base electrical frequency
(Hz)
```

Here is reported some examples, included in the development kit. Fig. 3 shows diagram for the whole

project. Level 1 of the project verifies the target independent modules, duty cycles and PWM update. The results, which are illustrated correspond to 128 microsteps/step.

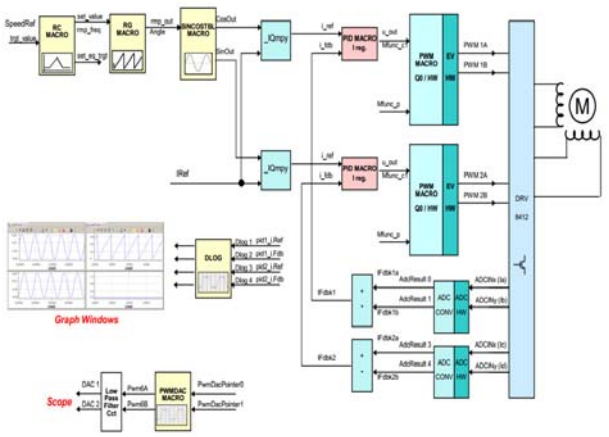

Fig.3. System Build Block Diagram

At first level of the project the motor is disconnected. In this level students test the sin/cos table module (SINCOSTBL_MACRO) and PWM generator (PWM_MACRO). For these purpose the reference speed SpeedRef value and voltage Vref across the motor are specified. Depending on SpeedRef value RG_MACRO module via RC_MACRO produce discrete angle. SINCOSTBL_MACRO module takes that discrete angle as input and outputs the sin and cos of that angle from a look-up table. The outputs of the SINCOSTBL_MACRO are then scaled by VRef to obtain the desired amplitude. The range of the angle input is dependent on the desired number of microsteps per step.

The students can be monitored the outputs of the SINCOSTBL_MACRO and RG_MACRO using the graph windows of the Code Composer Studio 6.0 (CCS) as shown at Fig. 4

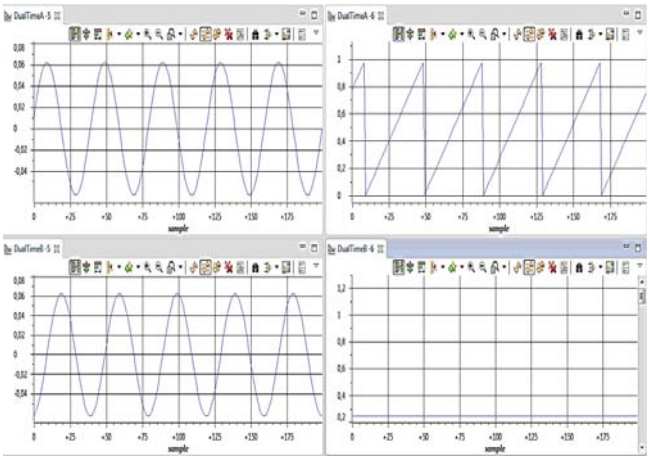

Fig. 4. CCS 6.0 Graph Windows for BUILDLEVEL = 1

The outputs of the SINCOSTBL_MACRO are scaled by VRef and then specified to the PWM_MACRO. The duty cycle of the PWM outputs should vary sinusoidally at the frequency specified by SpeedRef.

Then students check the PWM test points on the board to observe PWM pulses (PWMA and PWMB for Phase A and PWMC and PWMD for Phase B), as shown in Fig.5.

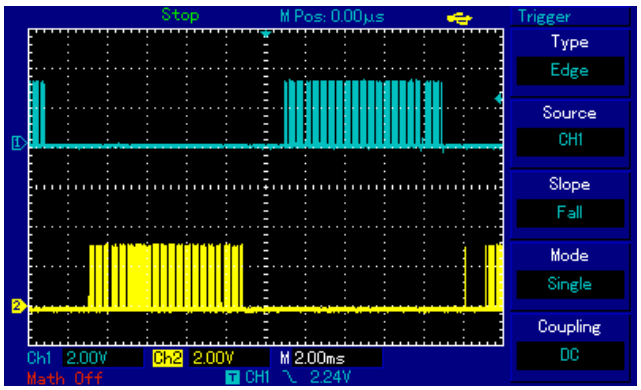

Fig. 5. 1 - PWMA and 2 -PWMB switching waveforms

After the Level1 incremental build is completed successfully, the motor is connected to the board. In this level verifies the analog-to-digital conversion [6]. In the software, the key variables which can be adjusted are VRef (for changing the motor voltage in per-unit) and SpeedRef (for changing the motor electrical speed in per-unit).

The motor starts spin slowly. In the CCS watch window can be monitored the generated references sin and cos signals and currents through the two phase motor windings as shown in Fig. 6. The top two graphs show the cos and sin voltage waveforms that are being generated. The bottom two graphs show the corresponding ADC sampled current waveforms. It is shown that the current waveforms are different from sin waveforms.

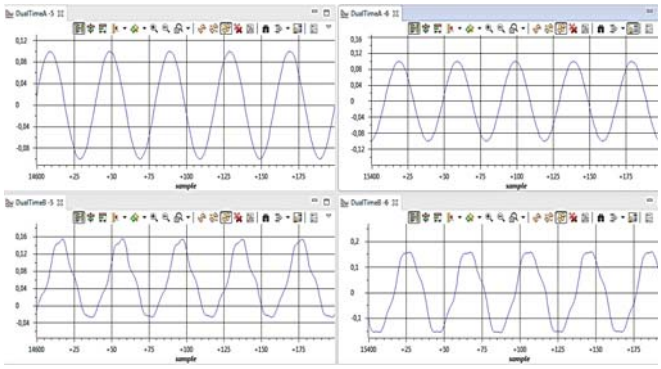

Fig. 6. Build Level 2 graph showing generated sinusoidal voltages and current feedback

Fig. 7 illustrates the phase A current.

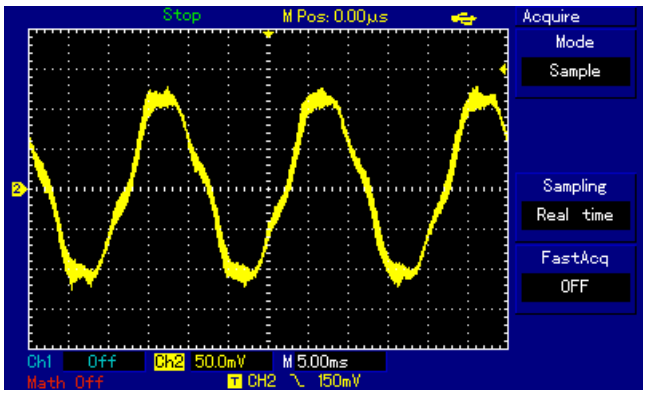

Fig. 7. Phase A current

The Level 3 section verifies the current regulation performed by PID_REG3 module. This module is consisted from two PID controllers. To confirm the operation of current regulation, the gains of these two PID controllers are necessarily tuned for proper operation. This can be configured in Stepper.c:

```
// Initialize the PID_REG3 module for I
        pid1_i.Kp = _IQ(2.16);        //for 24V DC bus
        pid1_i.Ki = _IQ(T*128.1);
        pid1_i.Kd = _IQ(0/T);
        pid1_i.Kc = _IQ(0.006);
  pid1_i.OutMax = _IQ(0.95);
  pid1_i.OutMin = _IQ(-0.95);

        pid2_i.Kp = _IQ(2.16);        //for 24V DC bus
        pid2_i.Ki = _IQ(T*128.1);
        pid2_i.Kd = _IQ(0/T);
        pid2_i.Kc = _IQ(0.006);
  pid2_i.OutMax = _IQ(0.95);
    pid2_i.OutMin = _IQ(-0.95);
```

In this project build two quadrature sinusoidal motor currents are dynamically regulated by using PID_REG3 module. The steps are explained as follows: Set values for Iref (for changing the motor current in per-unit) and SpeedRef (for changing the motor electrical speed in per-unit). Figure 10 shows the graphs for this build level. The top two graphs show the commanded cos and sin current waveforms. The bottom two graphs show the corresponding current feedback waveforms. If PID gains are adjust properly, the feedback currents will track the commanded currents.

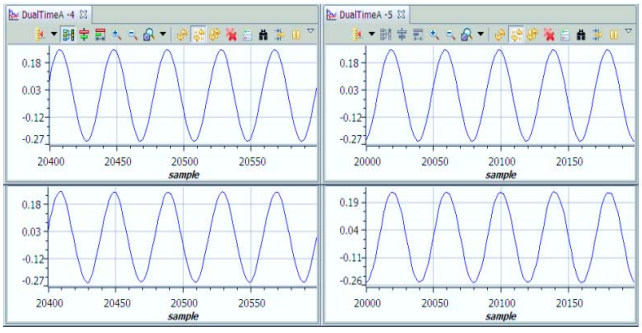

Fig.8. Build Level 3 graphs of commanded and regulated motor currents

Fig. 9 illustrates the phase A current.

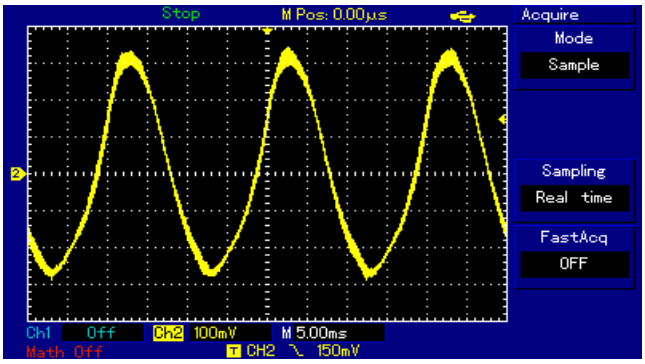

Fig. 9. Phase A current

As mentioned above, the development environment allows the testing, the study and comparison to other methods for control of the stepper motors, i.e. microstepping with different sizes of step, quarter step, half step and a full step.

The laboratory works are organized so that after investigation of these different control methods, the students made conclusion about their advantages and disadvantages.

III. Conclusion

Development of the modern power electronics puts serious challenges to the teaching of the industrial electronics students, due to the complexity of the necessary knowledge and skills. Although students expressed interest in power electronics integrated with digital controls and digital signal processor (DSP), the conventional teaching arrangement did not give them needed background and knowledge.

As a development environment was chosen the Medium Voltage Digital Motor Control (DMC) kit, DRV8412-C2, from Texas Instruments (TI), which provides a great way to learn and experiment with digital control of medium voltage motors. The present report examines the implementation of one of the control methods for bipolar stepper motor - microstepping and the main points of the students teaching process during the laboratory work.

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Teaching Stepper Motors and Brushed DC Motors Using the Medium Voltage Digital Motor Control Platform, Part II - Brushed DC Motors Control

Tsvetana Grigorova Grigorova

Abstract – **The paper shows the teaching methodology of the Brushed DC motors control, using Texas Instruments platforms. The present report examines the implementation of the control methods (bipolar and unipolar) for BDC motors and the main points of the students teaching process during the laboratory work. The software available with the kit is completely open source, which allows students to create their own projects and thus to better understand the basics of applying DSP in power electronics and digital motor drive control. The experimental results are presented.**

Keywords – **Digital motor control, Brushed DC motor**

I. INTRODUCTION

The power electronics as a subject is not readily assimilated by students because of the different areas involved, the complexity of the necessary knowledge and skills [1,5]. Furthermore, students expressed interest in power electronics integrated with digital controls and digital signal processor (DSP). The students need to graduate with skills that make them easily marketable to potential employers.

Taking into consideration these trends in the education of the modern power electronics and motor drives in [4] is explained about offered an eligible course entitled “Electronic converters for motors control" as a part of the Master's program in "Electronics". As a development environment the Medium Voltage Digital Motor Control (DMC) kit was chosen, DRV8412-C2, from Texas Instruments (TI), which provides a great way to learn and experiment with digital control of medium voltage motors. In the DRV8412 DMC kit are included two brushed DC motors and 8-wire bi-polar stepper motor [6].

Universal brushed DC and stepper motors comprise the majority of motor applications given their low cost and simplicity of control. The teaching methodology of stepper motors control, using Texas Instruments platforms, was discussed in [4]. The present report examines the implementation of the control methods (bipolar and unipolar) for Brushed DC (BDC) motors during the laboratory work.

The software available with the kit is completely open source which allows students to create their own projects and thus to better understand the basics of applying digital signal processor (DSP) in power electronics and digital motor drive control [3].

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II. BRUSHED DC MOTOR CONTROL PWM MODULATION TECHNIQUES

At the beginning of the laboratory session, the teacher gives a brief explanation, presenting an overview of the experiment and the relation with the theory. The teaching process is focused on the different PWM techniques, along with their advantages and disadvantages, in an effort to pick the one that is right for a particular motor control application.

The brushed DC motors are driven by the conventional H-bridge configuration (Fig.1). With the flexibility of four switches, a number of different control methods (bipolar or unipolar) can be used to produce fourquadrant output voltage and current as no two switches in the same leg conduct simultaneously [2].

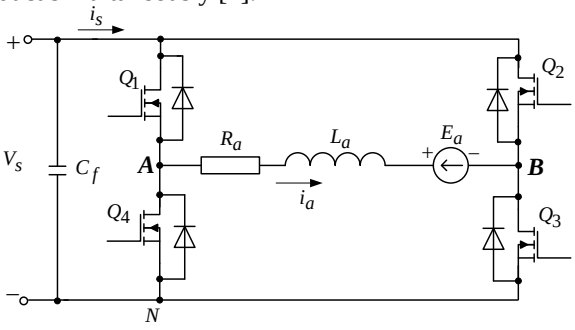

Fig.1. Four-quadrant H-bridge converter

A. PWM with unipolar voltage switching

PWM with unipolar voltage switching, in classic view, is realized as follows (Fig. 2): a triangular waveform is compared with the control voltage v_{cont} and $-v_{cont}$ for determining the switching signals for leg A and leg B of the H-bridge, respectively. A comparison of v_{cont} with v_{tri} controls leg A transistors, whereas leg B transistors are controlled by comparing $-v_{cont}$ with v_{tri}. As a result all three output voltage states, namely $\pm Vs$ and 0V, are possible.

B. PWM with bipolar voltage switching

A triangular waveform is compared with the one control voltage v_{cont} for determining the switching signals for leg A and leg B of the H-bridge, respectively. For example, when $v_{cont} > v_{tri}$ high side FET in half bridge A and low side FET in half bridge B will be on and low side FET in half bridge A and high side FET in half

bridge B will be off. Otherwise, a high side FET in half bridge B and low side FET in half bridge A will be on. As a result, only two voltage output states, are possible, *+Vs* and *– Vs*.

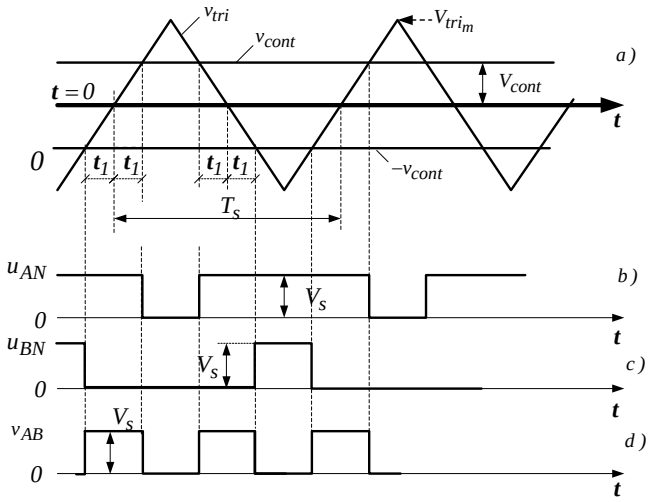

Fig. 2. PWM with unipolar voltage switching

C. The Medium Voltage Digital Motor Control (DMC) kit description

At the beginning of the laboratory work, students are given a tutorial that guides them through the hardware description, the experiments and the actions to be performed in each step. Except the development board, the necessary equipment includes a personal computer with an installed development environment Code Composer Studio v6.0, an oscilloscope and a current probe.

Fig.3 shows the block diagram of the DRV8412 evaluation kit (DRV8412-C2-KIT). It consists of the DRV8412 motor driver, a C2000 Piccolo F28035 MCU controlCARD, example software, code development environment (Code Composer Studio) and the motors. The DRV8412 is high-performance, integrated dual full-bridge motor driver with an advanced protection system [7].

The F28035 device generates the four pulse-width modulation (PWM) signals needed to drive the DRV8412 Dual-Full-Bridge PWM Motor Driver. Two input currents of each motor are measured from the H-bridge and 4 ADCs send these currents to the F28035 device. This system demonstrates current control of a Brushed DC Motor. The examples start out with a single axis demonstration and end with a multi-axis demonstration. Dependent of Mode Jumpers – DRV8412 mode can be set to enable/disable cycle-by-cycle (CBC) current limit, latched over-current (OC) and parallel or dual full-bridge mode – generally four operation modes [7].

D. Projects Organization

Using the included project in the kit one PWM sequence is generated that appears on output PWM-A or output PWM-B depending on the motors rotation (for one H-bridge). With the resulting signals unipolar and bipolar PWM technique for motor control can be accomplished, which is determined by the operating mode of the driver DRV8412. These projects are built up into four levels - on each level the modules are tested and the software is checked for the correct operation of the hardware [7]. The platform allows change and adjustment of various parameters in real time. This can be configured in 2xDC_Motor-Settings.h header file.

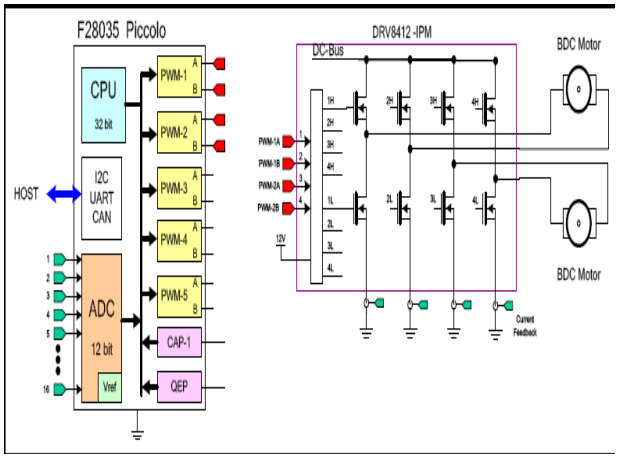

Fig. 3. Dual-Axis, Brushed DC Motor Drive

For the proper work we put mode 2 of DRV8412. As mentioned above, the software available with the kit is completely open source and allows both to be studied from the students and to be modified. Furthermore, it is possible to change the different PWM techniques. Thus, students acquire practical skill and obtained knowledge about the most common methods for PWM control of the BDC.

The triangle carrier signal, which is used to perform PWM sequences digitally, represents the increase of the value of the counter TBCTR from 0 (0x0000) to a given value for a time equal to a half-period of the modulated signal (TBPRD), which is set by the function **PWM_Macro**, and depends on the output of the PID controller, and therefore the reference current IRef. Since ePWM module works with the frequency of the processor core, so in the span of time TBPRD the value, which the TBCTR counter reaches, is the value recorded in the register TBPRD.

At Level 1 step, the motor is kept disconnected. This section describes the steps for a “minimum” system check-out, which confirms operation of system interrupt and the peripheral dependent PWM_MACRO (PWM initializations and update) modules. Open 2xDC_Motor-Settings.h and select level 1 incremental build option by setting the BUILDLEVEL to LEVEL1 (#define BUILDLEVEL LEVEL1). The variable, named “IsrTicker” , will now keep on incrementing - confirm this by watching the variable in the watch window, which verifies that the system interrupt is working properly. The corresponding block diagram for this level is shown on Fig. 4.

In the software, one of the key variables to be adjusted is VRef1 (for changing the motor voltage in per-unit).

In this level we will test the PWM Generator Macro (PWM_MACRO). The VRef1 value is specified to the PWM_MACRO via the RC_MACRO module (RC Ramp Controller). The rate of change of the PWM duty cycle is therefore slew rate limited and will not change instantaneously with VRef1. When VRef1 is positive, PWMA should show a switching frequency – a square

wave with a duty cycle corresponding to the magnitude of VRef1 and PWMB should be held low. Then students check the PWM test points on the board to observe PWM pulses (PWM_A and PWM_B), as shown in Fig.5.

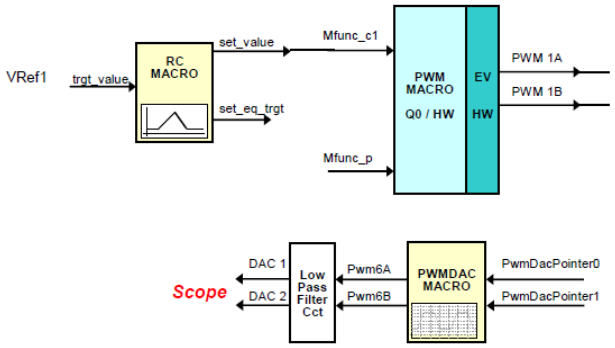

Fig.4. Level 1 -Incremental System Build Block Diagram

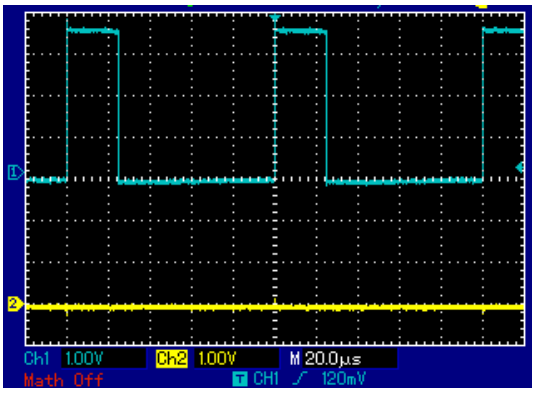

Fig. 5. 1-PWMA and 2- PWMB for VRef1 = 0.25

When VRef1 is negative PWM_B should show a switching frequency, square wave with a duty cycle corresponding to the magnitude of VRef1 and PWM_A should be held low – Fig.6.

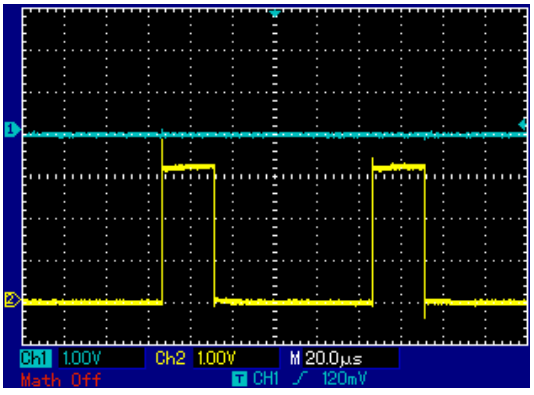

Fig. 6. 1-PWMA and 2- PWMB for VRef1 = -0.25

After successfully testing Level1, operation moves to Level 2, where the analog-to-digital conversion is verified. In this phase the motor is connected to the board. In the software, one of the key variables to be adjusted is **Vref1**.

After the previous build phases are completed successfully, Level3 verifies the current regulation performed by the PID_REG3 module. The corresponding block diagram for this level is shown in Fig. 7. To confirm the operation of the current regulation, the gains of these two PID controllers are necessarily tuned for proper operation.

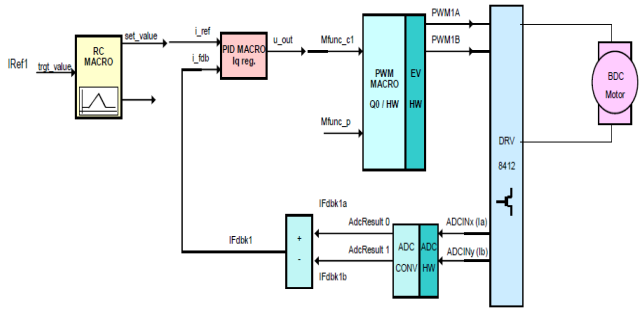

Fig. 7. Block diagram for Level 3

On level 4 two motors are connected to the device, and the previous phases are completed successfully. This build verifies the multi-axis concept - which is two DC motors running simultaneously with current control. The block diagram of this level is presented in Fig. 8.

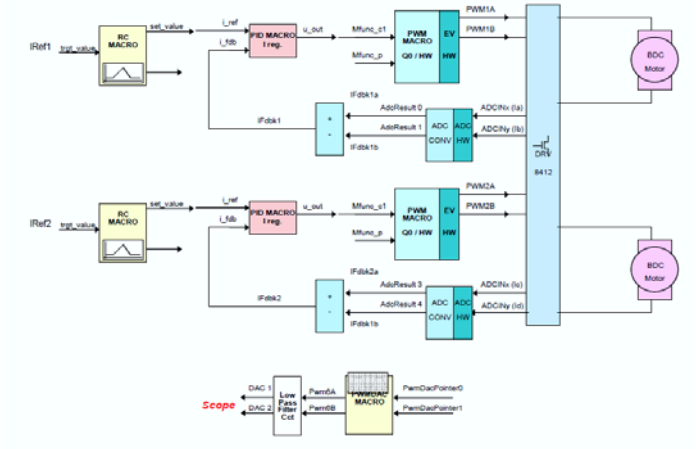

Fig. 8. Block diagram for Level 4

III. Experimental Results

In this section the realization of the PWM techniques for motor control using the included project in the kit is discussed. The experimental results are obtained using the default PWM frequency of 10kHz.

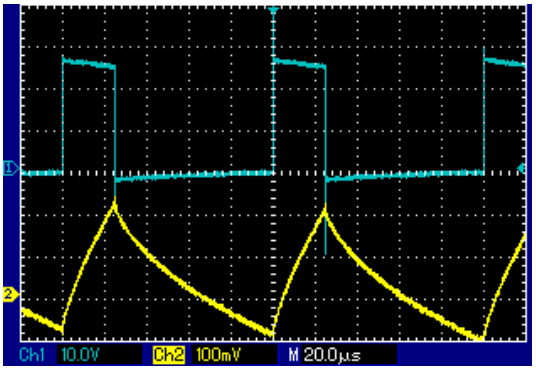

Fig.9. Output voltage (trace1) and output current (trace2)

The first example shows how using the H-Bridge configuration (Fig.1) to create a two-quadrant unipolar drive, i.e. forward motion with positive torque, or reverse motion with negative torque. With the control signals shown in Fig.5 the unipolar modulation for forward direction can be realized as follows: low side FET in half

bridge B is turned on continuously, while PWM signal to high side FET in half bridge A is applied. The output voltage and current waveforms for duty ratio D = 25% are shown in Fig.9 (forward).

If we want the motor to spin in the other direction (Fig.6), then continuously turn on low side FET in half bridge A and PWM high side FET in half bridge B instead. The output voltage and current waveforms for reverse direction and duty ratio D = 25% are shown in Fig. 10.

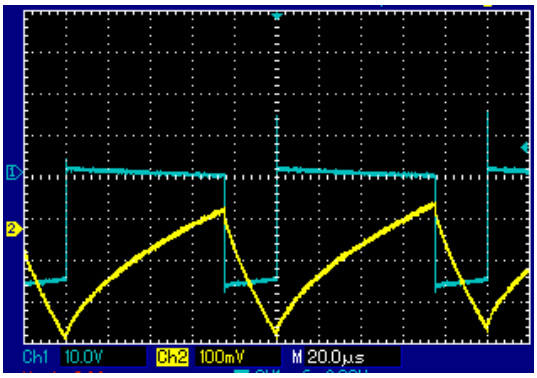

Fig. 10. Output voltage (trace1) and output current (trace2)

The second example shows how the H-Bridge configuration (Fig.1) can be used to create a bipolar PWM. DRV8412 is switched on mode 4. It is necessary ePWM1 processor module to simultaneously generate two PWM sequences (ePWM1A and ePWM1B). These two signals are connected to the inputs and PWM_A PWM_B of DRV8412. Both control signals must be opposite, so as to switch both pairs in the bridge circuit, i.e. they are inverted relative to one another. In the classic bipolar PWM signals for generating ePWM1A and ePWM1B triangular signal from the register TBCTR of ePWM1 module is used as well as the value of the register CMPA.

The duty ratio D is defined through variable VRef1. The VRef1values are from 0 to 1. The waveforms for duty ratio D = 75% are shown in Fig. 11.

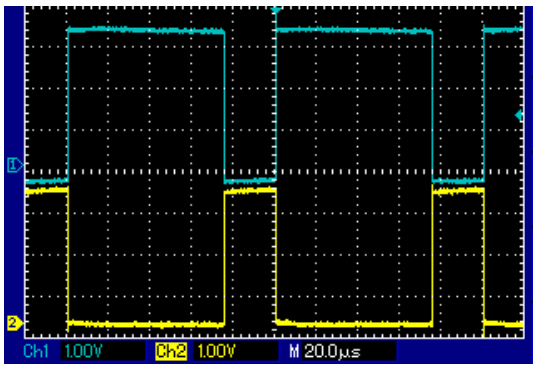

Fig. 11. 1- ePWM1A and 2 - ePWM1B) signals

The waveforms for duty ratio D = 25% are shown in Fig. 12.

The laboratory works are organized so that after studying these different control methods, the students can make conclusion about the advantages and disadvantages. As mention above, the software available with the kit is completely open source and allows both to be studied by the students and to be modified. Using multi-axis concept (Fig. 8) in [3] is presented the Master's thesis results of the software realization for controlling one DC motor with bipolar PWM and the other DC motor with unipolar PWM in the same mode of the driver DRV8412. This removes the need for hardware changes in the kit while the various methods of modulation are studied. Moreover a 4-Quadrant Unipolar technique with double PWM output frequency is shown.

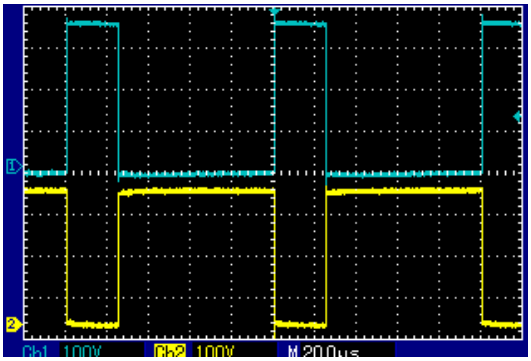

Fig. 12. Fig. 7. 1- ePWM1A and 2 - ePWM1B) signals

IV. CONCLUSION

The paper presents the teaching methodology of the Brushed DC motors control by using Texas Instruments platforms. The present report examines the implementation of the control methods (bipolar and unipolar) for BDC motors and the main points of the students teaching process during the laboratory work. The software available with the kit is completely open source, which allows students to create their own projects and thus to better understand the basics of applying DSP in power electronics and digital motor drive control. The experimental results are presented.

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Comparing Validation of Self-acquired Learning in the ICT Company Sector and in VET Schools/centers in Bulgaria

Rosen Kirtchev Petkov

Abstract –**The current paper will compare the approaches and tools in the public and private sector in terms of validation of self-acquired learning with examples from the ICT. The material starts with some historical overview of the validation of self-acquired learning and then shows the tendencies of the validation approaches in the ICT company sector during the last years. Further, the validation of self-acquired learning in the vocational schools and centers has been explored. The nowadays tendencies of introducing units of learning outcomes have been discussed. The recent changes of the vocational area legislation in Bulgaria have been summarized. At the end of the paper, some results of the innovative projects, related to the topic, have been presented.**

Keywords – **self-acquired learning, ECVET, units of learning outcomes**

I. INTRODUCTION

The validation of self-acquired learning is undergoing significant changes last few years. The fast development of online provision of information and training materials, the dynamic of the labour market, the need of shorter duration of trainings, the flexibility of training methods and many other reasons determine the appearance of different methods for validation of self-acquired learning.

The companies used certification methods of self-acquired experience since many years. For example, the ICT sector has employed many validation approaches last few decades. It worth to mention the CompTIA A+ certification for beginners in the IT world, CISCO, Microsoft and other certification systems.

The private Vocational Education and Training (VET) centers also tried to be flexible last few years and try to employ open and distance education methods not only to satisfy the variety of trainees but also to reduce the cost of the training. But, being the officially licensed centers, they had to respect the VET law which was quite inflexible in the past (we mean, in Bulgaria). The options for validation of self-acquired learning have been introduced officially since the end of 2014.

VET schools (mostly public ones today) are least flexible in terms of introducing new forms of learning and validation. Being conservative institutions that have to respect visions and capacity of the teachers, the opinion of students and their parents, VET schools will probably introduce such innovative approaches like validation of self-acquired learning or dual education system in longer period, step by step.

The paper will try to explore the different and common approaches in the validation of self-acquired learning in the corporate sector and in the VET centers and schools.

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II. VALIDATION OF SELF-ACQUIRED LEARNING IN THE ICT COMPANY SECTOR

Some years ago, the validation of self-acquired learning in the company sector was product oriented and in some cases emphasizing only on the practical skills. Also, the certification process was not so flexible in terms of dates for exams and the organization of the exams itself. Some exams were offline or face-to-face and this also made the process slower. But, situation changes nowadays.

In the business sector, the validation of work/project based experience has always been an important issue. In the corporate sector, concerning the validation, there are so called *company certificates* and *third party certificates*. Third party certificates are certificates issued by organizations or associations that don't cover their own products/services. Examples of third party certificates are Microsoft, CISCO, Apple certificates, example of third party (company independent) certificates are CompTIA certification programmes. If we move away from the ICT sector, some of the well-known examples of third party tests are TOEFEL and GRE ones.

Last few years, there are rapid changes in the validation approaches. Companies are structuring better their certification process, including respective knowledge and skills, they are emphasizing more on the area of working (e.g. networks, servers maintenance) not only on the skills related to their commercial product. Other interesting novice is the usage of nowadays concepts and some ideas from the public sector (formulating units of learning outcomes, for examples).

It is also worth to say that there are also many hidden (internal) procedures in companies related to the validation of the employee's experience. Here, we will focus mainly on publicly announced certification programmes.

Last but not least, there are different forms of blended learning where the combination of formal, informal, non-formal and self-acquired learning could occur.

Let see some of the nowadays examples in the ICT company sector. There are simpler certification systems where the test covers certain area and requires certain experience in advance. For example, the general parameters of ComTIA networking certification, Fig. 1, [4], look like:

The CompTIA Network+ce program is included in the scope of this accreditation, and may be kept current through the CompTIA Continuing Education program.

Test Details		
Exam Codes	**N10-005** JK0-019 *(for CompTIA Academy Partners only)*	**N10-006** JK0-023 *(for CompTIA Academy Partners only)*
Launch Date	1-Dec-11	28-Feb-15
Number of Questions	Maximum of 100 questions	Maximum of 90 questions
Type of Questions	Multiple choice and performance-based	Multiple choice and performance-based
Length of Test	90 Minutes	90 Minutes
Passing Score	720 (on a scale of 100-900)	720 (on a scale of 100-900)
Recommended Experience	• CompTIA A+ Certification • (9) months of networking experience	• CompTIA A+ Certification • (9) months of networking experience
Languages	English, Japanese, German, Simplified Chinese, Korean, Spanish, Traditional Chinese	English at launch (2/28/15) Japanese and German - in development

Fig. 1. ComTIA network certification programme

Of course, each company (or related training organizations) usually offers training possibilities for beginners or for people who like to increase the chance to pass the tests.

Interesting phenomena could be seen in Microsoft certification programmes, Fig. 2, [3], where the certification path is very flexible and modern. Here, you could verify your knowledge and skills in certain unit or in combination of $_{\text{units}}$. So, the certificate contains details of the units you passed. This approach is similar to the European Credit System for Vocational Education and Training (ECVET) approach and definition of so called *units of learning outcomes*, introduced and recommended by the EU last few years.

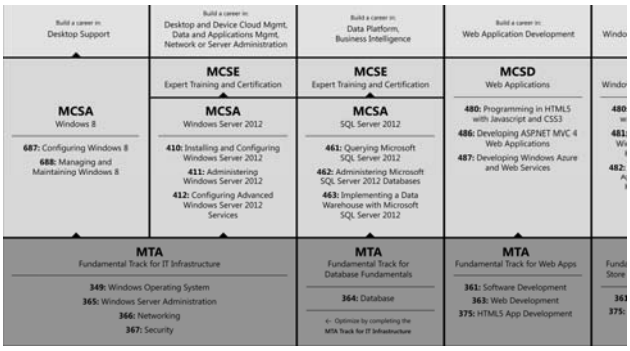

Fig. 2. Paths in Microsoft Technology Associate (MTA) test

For example, if you have interests in the area of IT infrastructure and configuring operating systems, networks, you could pass exams 349, 365, 366 or 367. Recently, the exam for cloud technology and mobile devices, number 368 has been added. You will get the certificate when passing one of the above exams. In the certification programme, there is also a description of ways of getting the certificate, ways of licensing of institutions that could issue such certificates etc.

The question who certifies, the quality of the organization that is licensed to issues certificates is also interesting. One of the ways the certifying organization could demonstrate the quality is to obtain some world-known certificate for quality, for example, ISO/ IEC 17024: 2012 [5]. ISO/IEC 17024 gives the criteria/principles for the establishment of certification programme for individual clients.

It is also curios to see how these certificates are demanded by the employers [6]. Here is one figure (Fig. 3) of research about certificates demanding, in the social networks or in jobs portals:

	Dice	Indeed	JustTechJobs	LinkedIn	SimplyHired	TechCareers
CompTIA CTT+	0	8	4	6	18	4
MCT	6	33	25	198	67	9
CCSI	7	67	214	56	138	13
CCI	0	0	0	0	4	1
ACT	0	40	16	9	13	0

Fig. 3. Results from research of tom'sIT Pro about demanding of certificates

III. VALIDATION OF SELF-ACQUIRED LEARNING IN THE VET CENTERS AND VET SCHOOLS

Validation of self-acquired learning in the VAT centers or in the VAT schools depends on two factors, the first one is the formal legislation and the second is the management of schools. The considerations here cover mainly Bulgaria VET sector but most of the cases are similar to many EU countries.

Last few years, there were several attempts to make amendments to the existing laws regulating VET. Finally, in 2014, the new VET law has been approved by the BG Parliament and the validation of self-acquired learning has been accepted [1]. The new Order N:2 of the Ministry of Education and Science, published in the beginning of 2015, provided more details about implementing the validation procedures in VET schools or centers [2]. So, the doors are open for all practitioners, students or youngsters who would like to validate their experience and receive officially recognized certificate.

There is a difference in the type of education in the VET centers and VET schools defined in the Law for the Vocational Education and Training. The term used for VET centers is *training*, the training could be *initial* and *continuing*. The term used for VET schools is *professional education* and the education there includes also the minimum subjects to receive secondary education level.

In 2008, European Parliament and the European Council have introduced the European Qualification Framework [7]. Here, 8 levels of qualification have been described. The term *units of learning outcomes* have been also introduced. The learning outcomes are described as set of knowledge, skills and competencies. There is a recommendation for the member countries to point out in the issues diplomas/certificates the respective level according to the EQF. An year later, in 2009, the European Credit (Transfer) System in Vocational Education and Training, called shortly ECVET has been introduced. The ECVET aim is to contribute the process of recognition,

accumulation and transfer of credits between the training organizations.

In line to the above considerations, the problem of new professions and their validation rises. In the above mentioned Order 2 of the Ministry of Science and Education there are certain approaches in this case.

Last few years there are some projects of the Ministry of Education and Science, National Agency for Vocational Education and Training (NAVET), Bulgarian Camber of Commerce and Industry and Syndicates related to the topic. They started in parallel to the law changes so some of their findings are not corresponding to the recent legislation changes. But, they are useful as they show the willingness of the state and the business to move in this direction.

One of the first EU projects related to validation of self-acquired learning in the ICT&Arts area is the CREATE project (create-validate.org), coordinated by the author of this paper [8]. The project offers methodology, training materials and concrete online tools for the validation of self-acquired learning in two new professions, web design and computer animation. The project started in 2011 and was one of the pioneering projects in the area, Fig. 4:

Fig. 4. The project CREATE (Validation of self-aCquired learning and cREdits trAnsfer in web design and compuTEr animation), www.create-validate.org

CREATE project uses the latest recommendations of EU related to ECVET points allocation and dividing the material in Units of learning outcomes. Each learning outcome consists of knowledge, skills and competencies. CREATE project also demonstrates different tools for validation of knowledge, skills and competencies- tests, online games, e-portfolio.

In principle, there are several steps in the validation process design. The first one is to determine the main areas/topics to be validated, the second one is formulating the units of learning outcomes. Each unit consist of outcomes, outcomes consist of knowledge, skills and competencies. Then, the methods for evaluation should be selected and respective ECVET points for each unit should be allocated. Last but not least, the ECVET level should be appointed if the desired units are passed successfully. In all those processes, the main stakeholders should participate- employers, trainers, policy-makers, students. Fig. 5 shows how the main page of the tools for some units of learning outcomes look, you could see the unit title/description, educational goal and dedicated ECVET points, as well as the type of the validation tool- test, game, ePortfolio etc.:

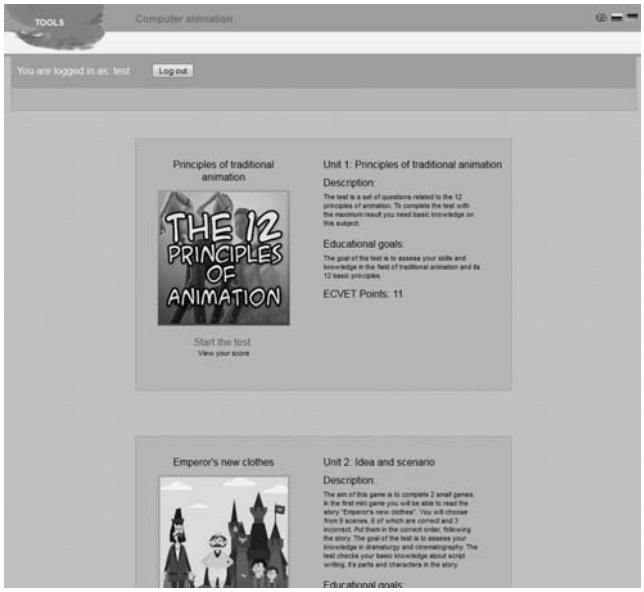

Fig. 5. Tools page for units of learning outcomes in the field of computer animation (The validation tool for the first unit is a test, the tool for the second unit is a game)

CREATE project has been piloted in some vocational schools in Bulgaria, Germany and Ireland. The feedback showed the applicability of the approach. The developed Manual could help the organizations (VET schools, centers of companies) to develop their own certification/validation system. The concrete tools in the two subjects (web design and computer animation) could be a model for the development of system and tools for other training subjects.

IV. E-PORTFOLIO METHOD AS VALIDATION METHOD

The electronic portfolio (ePortfolio or e-portfolio) is very useful method for self-awareness, for self-assessment or external assessment, for communication and presentation purposes, for identification of some problems or training needs of students etc. Depending of the purpose, ePortfolio could be organized in very different ways.

One of the functions of ePortfolio could be the assessment of the level of knowledge, skills and competencies. As a set of artifacts, the portfolio could also show the progress of such competencies during the years.

ePortfolio could be used in formal, informal or non-formal education, it is a method for encouraging the owners to reflect and analyze their achievements, it is a good method for facilitating self-awareness.

ePortfolio for Your Future project (my-eportfolio.org), leaded by the author of the paper, was one of the pioneering international projects in the area of electronic portfolio [9]. The project includes methodology and tools how to use eportfolio for self-assessment purposes. ePortfolio 4YF project also offers multimedia self-assessment game and motivation test (Fig. 6).

Fig. 6. The project ePortfolio 4YF (ePortfolio for Your Future), www.my-eportfolio.org

There is example portfolio system where the users could create the layout of their portfolio depending of the purposes and their vision. In the portfolio the user could state the strong points of his/her personal and professional features. When playing the game, the user will receive feedback about his/her personality. Then the user could compare them with own opinion expressed in the ePortfolio. The comparison of self-opinion (portfolio) and results from validation (game tool, tests) could help the users to reflect on their work, study and achievements.

ePortfolio systems are becoming more and more popular when applying for a job. As an addition to the CV, they could show the several of multimedia data and artifacts of the applicant professional development. Some universities and schools are developing their own portfolio systems but nowadays public portfolio systems (for example, Behance) and social networks (for example, Linkedin, Facebook) are also offering portfolio development features.

The manuals we have developed in the frame of the CREATE and ePortfolio 4YF projects could help VET trainers, teachers and managers of training organizations (VET centers and schools) how to use modern media to organize procedures for validation of self-acquired learning. Also, these training materials (free to access and in several languages) could be useful for all teachers and experts willing to use the advantages of validation of self-acquired learning.

V. CONCLUSION

The above considerations have attempted to show some aspects of corporate sector validation procedures and VET schools/centers validation procedures in self-acquired learning. There are several common tendencies we could observe:

- both sectors are trying to make the process flexible and results transferrable, that is why last few years the companies are also forming units of outcomes when designing their certification procedures;
- both sectors are trying to reach wider audience using open and distance approaches in the validation; the employment of new media and communications is quite visible;
- both sectors and trying to make the validation human- independent using games, tests and other computer based instruments;

The private and public sector, the business and the VET scools/centers are exchanging experience in these new tendencies in the assessment. The competent implementation of the validation of self-acquired learning is expected to wider the access to education and certification.

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[4] CompTIA Network+ certificates, http://certification.comptia.org/getCertified/certifications/network.aspx
[5] Standard ISO/IEC 17024, http://en.wikipedia.org/wiki/ISO/IEC_17024#ISO.2FIEC_17024:2012
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Using Logisim Digital Circuit Simulator for Examining Power Electronics Digital Control Systems

Tsveti Hristov Hranov and Nikolay Lyuboslavov Hinov

Abstract – **Logisim is a program used for digital circuits simulation – gates, flip-flops and latches. This paper presents a simple method, which allows simulation of circuits, designed for the power electronics devices, based on digital control units.**

Keywords – **Logisim, Simulation, Digital Control Circuits, Power Electronics**

I. Introduction

A variety of software for circuit simulation is available in the internet – both free and commercial. Most of them are strictly specialized for electrical circuits, whilst others are for functional simulation. Logisim is an educational tool for functional design and simulation of digital logic circuits [1]. Unlike other electrical simulators it is not as strict as other similar products – for example when you design your circuits it doesn't require from you to define voltage levels, impedance matching and time delay propagation; instead the focus is on the functional description of the logic elements [2]. The software is intended primary for embedded systems engineers, but it can be successfully used in the power electronics field for evaluations of digital control and protection circuits. The simple interface and workflow makes it suitable for focusing on the working mechanism rather than deciding voltage levels, logic product families, parasitic effects or switching characteristics – it gives you answer to the question whether this circuit is suitable functionally for the application or not.

II. Capabilities and User Interface

The software consists of a single java archive (.jar), which bundles all the tools, elements and libraries. This makes it very compact, portable and cross-platform – it is open-source, with special educational intention. The starting screen is similar to the one shown on Fig. 1. The main window is divided in five parts: on top there is the menu bar and the toolbar, on the left is the explorer and attribute plane and on the right is the drawing canvas, on which users draw their schematic project. In order to do that they use the primitives from the explorer menu – gates, plexers, latches, flip-flops and some special elements such as buses, clock sources, transistors, transmission gates, LEDs, buttons, registers, RAM, ROM and others. They can be included in the schematic by simply dragging the desired element into the canvas. The wiring is done by simply clicking on a port (which is denoted by a small dot on every element) and dragging the wire to the desired destination.

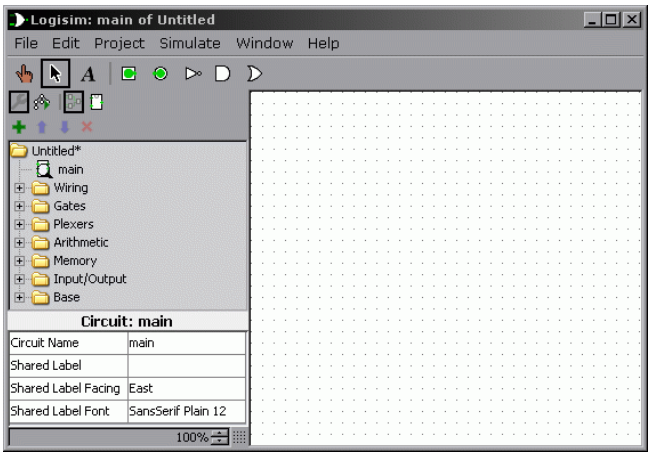

Fig. 1. Logisim main window at start-up

The schematic can be evaluated using the ports (both input and output), probes and clock sources. This is done using the “Poke Tool” (a little hand with index finger on the toolbar) and clicking on the various input ports or clock sources in the schematic. There is support also for automatic clock generation, which can be accessed through the “Simulate” menu, the “Ticks Enabled” option. Tick rate can be set up using “Tick frequency” in the same menu. Also in the same file there can be created several “Sub-circuits” which can be used to make the main schematic more compact and clear to read. This can be done using the “Project” menu, “Add circuit...” option. The circuit appearance can be modified with basic polygon drawing tools using “Modify circuit appearance”. Last but not least is a feature to analyze and log circuit behavior, which can be used to synthesize circuit or examine the circuit's functional states. For ease of use elements can be copied, cut and pasted, actions can be undone all via the “Edit” menu. The “File” menu allows for loading, saving, printing and exporting the project in various graphical formats.

III. Application Examples

To illustrate the functionality of the software we will discuss two types of circuits used in power electronics: a protection circuit and pulse-drive circuit.

A. Protection circuit

The protection circuits are fine examples of asynchronous digital logic device, which is expected to

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react in rare and time-unpredictable moments. Therefore its functional evaluation and testing before design is most critical. For our example we will discuss a circuit which monitors for simultaneous activation of switches in one leg in bridge inverter circuits, such as the one given on Fig. 2. [9, 10]

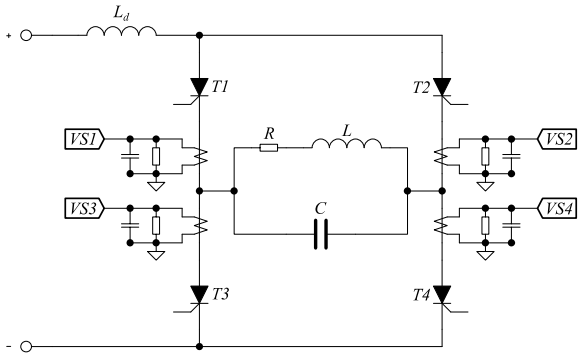

Fig. 2. Thyristor bridge inverter with current transformers

A leg is called the series of two thyristors – in the circuit the two legs are formed by *T1*, *T3* and *T2*, *T4*. A simultaneous firing of those thyristors leads in shorting the supply block, which could lead to a disastrous scenario. The protection circuit must detect this and counteract to it by stopping the supply source. This is done through the current transformers, which create signals for the gates shown on Fig. 3. The resistors and capacitors are there due to the nature of thyristor commutation – since it is not instantaneous, the capacitor gives the required time delay between the pulses [10], in which the current through the thyristors fall to zero in order not to confuse the system. However if the pulse is still there after the time delay has passed this indicates that there is a short in the leg, which should lead to immediate stopping of the supply unit.

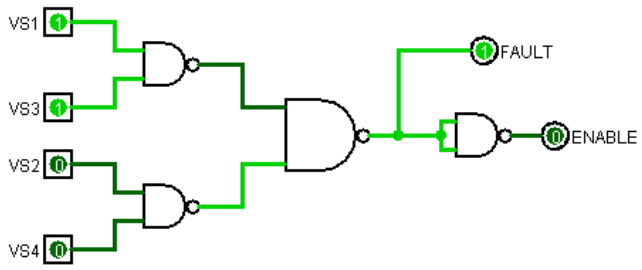

Fig. 3. Bridge Inverter digital protection circuit

The circuit is quite simple, yet effective – the inputs of the two NAND elements are connected to the current sensors for each switch, in a manner that single gate is connected to the two switches in a single leg. The outputs are compared with another NAND gate [3, 4], which will be active when either one of the legs is conducting (that is the power supply is shorted). The function of the schematic can be evaluated with the poke (hand) tool – individual bits can be toggled and the result will be displayed in real-time with the different signals in the wires.

B. Pulse-drive circuit

The control circuit of an AC-mains controlled rectifier is a fine example of a complex synchronous circuit. It has to be synchronized with the mains frequency and have a stable clock in order to precisely generate a proper delay angle. The example circuit is shown on Fig. 4 [7, 8]. The thyristors are fired during the corresponding half-waves after a defined time delay, which multiplied by the angular frequency ω has the dimensions of an angle – delay angle. In order to do this, the control circuit must detect the zero-crossing, and properly time the moment for the firing impulse [6, 8]. This is usually done with a comparator and a reference voltage, which are not shown here for clarity.

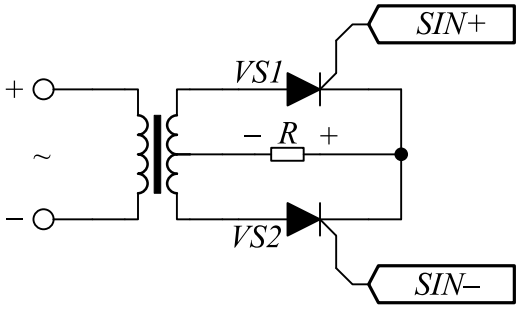

Fig. 4. Full wave controlled rectifier with thyristors and center-tap transformer

The idea is to use the built-in mechanisms of Logisim for clock generation – the clock element. This block changes state (“0” and “1”) at predefined “Ticks” – which can be set via the attribute plane (“High duration” and “Low duration”). The asymmetry in the durations allows even generation of Pulse-width modulation (PWM). The digital control circuit is shown on Fig. 6. The mains frequency is simulated via one clock element and the digital clock by another [5]. The main element is a four bit counter, which is triggered to count on a rising edge (for the positive half-wave) and on a falling (for the negative half-wave). It is encapsulated in a sub-circuit and shown as a single element here. When the counter is overflowing, the AND gate is generating a firing pulse for monovibrator and via the feedback is resetting the T-triggers, thus disabling the further counting. The conduction angle can be varied via the frequency of the clock pulses on the counter's counting input. This frequency should be always a ratio between the clock frequency, and this ratio should be greater in order the counter to overflow before the other half-wave takes place.

Another feature that is interesting to illustrate is the ability to simulate the designed circuit and log the inputs and outputs. This is done via the menu “Simulate”, option “Logging”. Then a window with three tabs pops up (Fig. 5) – in the first tab “Selection” you select which signal states you want to log. You can even log the state of buses and change the view radix. In the second tab “Table” you can observe the states in real-time as soon as you start the simulation.

The third tab “File” allows you to choose the file in which you want to log the states. You can start and stop the file logging anytime using the button above the file selection dialog. The “Include Header Line” option puts a line with the signal names – quite handy with many signals. The simulation can be started and stopped via the menu “Simulation”, option “Ticks Enabled”. You can observe the signal values in real-time and even if there are input ports

or buttons in the schematic they can be clicked to simulate an asynchronous event.

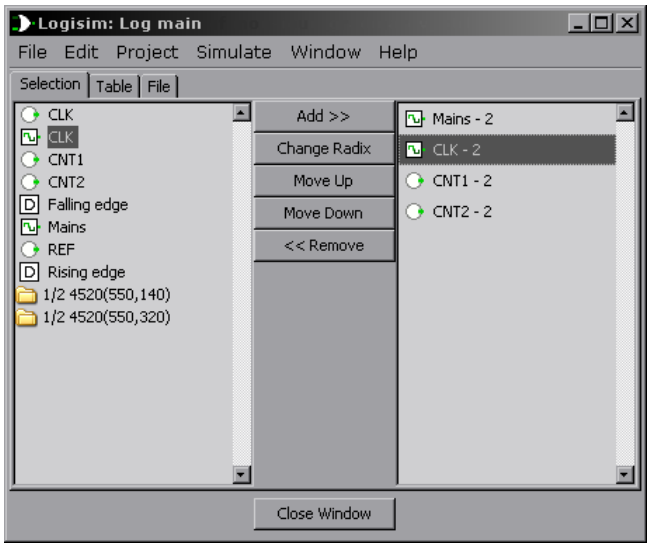

Fig. 5. Simulation logging window

The export file format is plain text, so it is quite easy to create tables and do Boolean and arithmetic operations on the signals. The logged signals can be imported another software and the user can generate the waveforms of the various signals. For our example we will use the software "Graph", which in-depth discussion is not placed here. In order to accomplish this we do some data formatting using spreadsheet software (sorting into columns, formatting the values etc.) and import the values as point series, where *x* is the time and *y* is the logical level. An example waveform is given on Fig. 7. For clarity is added also the mains sinusoid, to illustrate the working principle of the controlled rectifier. This assists also when you need to create waveforms and function diagrams for fine preview – for example posters, journals and books. The exported graphics are of vector type, which are best known for the precision and high resolutions capability without distortion like the raster images. The built-in tool for function analysis and evaluation can be used to precisely trace the values with respect to time, to see for example where multiple blocks switch to.

IV. Conclusion

Logisim is an excellent education tool which can be used to study and simulate digital circuits. Its simplicity allows the designers to focus on the functional analysis, rather than bothering in such early stages with details like operating voltages, timings, impedances and so on. This cuts the time to evaluate the performance of the solution and if there are required modifications, they can be easily done without this to lead to entire redesign of previous blocks. As a downside it can be pointed out that this version doesn't support direct export of the waveforms – it must be used in conjunction with other software. In our opinion this software is not so familiar in Bulgaria, whose introduction is one of the main goals of this paper. It is intended only for digital simulation and so it lacks elements like capacitors and inductors, which are usually used for setting time-constants. Last but not least thing to note is that this software is completely open-source and available to the public to be used and modified freely, which benefits a lot the academic institutions.

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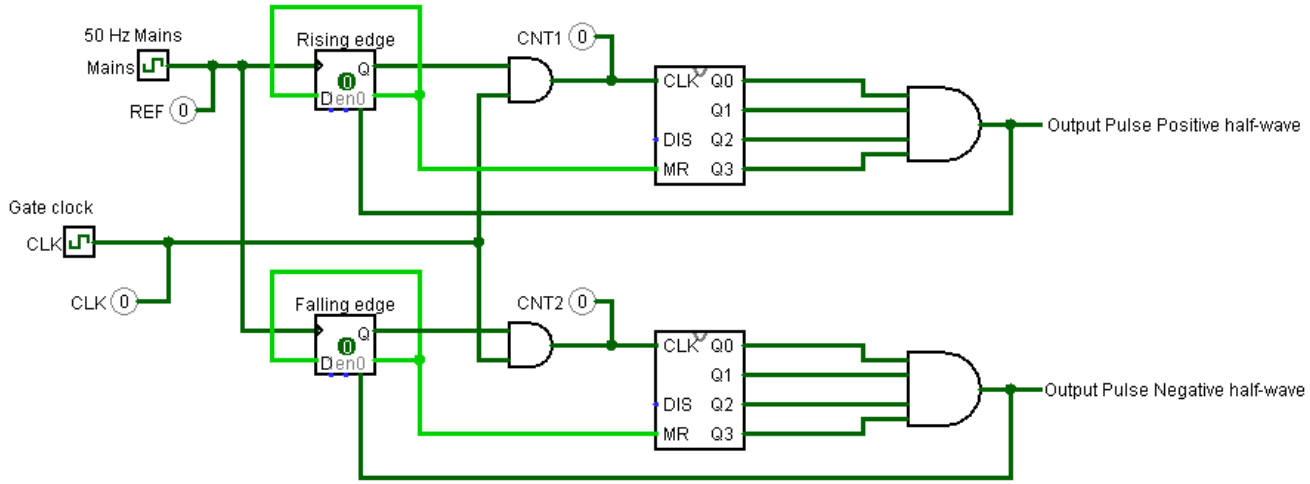

Fig. 6. AC-mains controlled rectifier pulse generating circuit

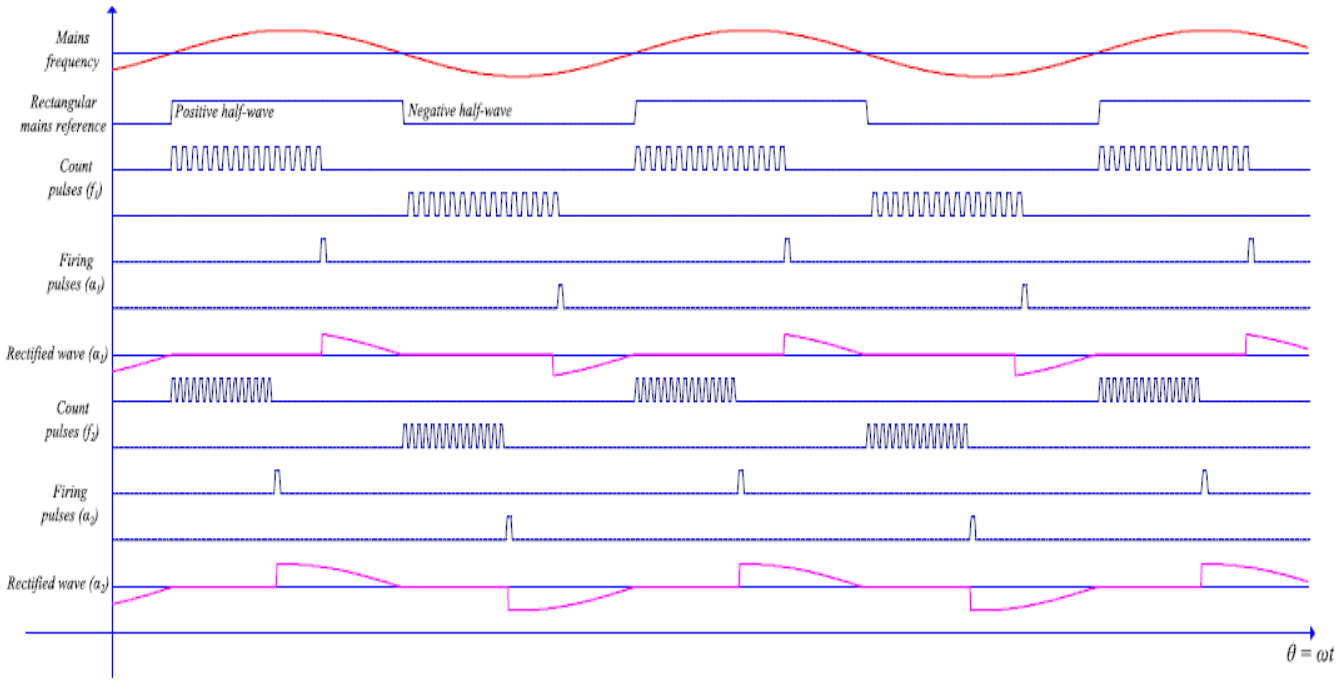

Fig. 7. Waveforms of the controlled rectifier

Software Environments Applicable in Teaching Analog and Mixed Signals Circuits Design

Daniela Antonova Shehova

Abstract – **Contemporary requirements for the transformation of the educational process in tertiary technical educational institutions in a modern educational environment for the preparation of future engineers demands that students master methods of learning some of which are of increasing importance, and involve the simulation examination of electronic circuits.**

The paper presents an interactive development of the concept of analog and mixed signal circuits through the use of suitable software environments.

Special emphasis has been put on the prospects of using these environments in the teaching of analog circuits design to the students from the corresponding specialties in the Technical college of Smolyan.

Keywords – **simulation research, software environments, electronic means**

I. INTRODUCTION

Innovational engineering education demands that its contents be updated in accordance with the knowledge of world's information resources. It aims the acquiring of a certain amount of knowledge, skills, and complex preparation of the specialists in the area of engineering and technology through the use of innovative educational methods and techniques. Such are the innovative educational technologies that consist of a complex of modern paradigms of the educational process; methods and modern educational techniques; educational information resources aimed at the development of innovative educational environment for the professional training of engineering specialists who acquire a complex of professional and social competences and innovative thinking [1].

The electronic tools for teaching are modern educational means that provide an opportunity not only to demonstrate processes that are difficult to replicate within the training environment, but also to clarify the influence of certain parameters on the processes under investigation in the electronic devices. This allows their use as simulators of laboratory equipment and for the development of skills to run modeled processes. They lower costs in the cases when experimentation with physical equipment will prove difficult due to financial or technical impediments [2].

The fact is that the improvement of the measuring devices leads to the increase in costs for the equipment necessary for the labs. This is the reason why this integrated approach of the combination of software and physical tools of training and education in the courses of analog circuits design is widely used as an alternative of expensive physical lab equipment.

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II. FACTORS DETERMINING THE CHOICE OF SOFTWARE ENVIRONMENTS AS ELECTRONIC TOOLS FOR TEACHING THE COURSES IN ANALOG AND MIXED SIGNALS CIRCUITS DESIGN

The use of software environments as electronic tools for practical training is the basis for the modernization of the educational system of any country as well as an important element of European educational policy. The idea for the application of electronic tools and models in the practical training of technical specialties directly corresponds with ISO 9001 – educational quality management system which is concordant with the Higher Education Act.

The use of software environments as modern electronic educational tools in the courses in analog and mixed signals circuits design has the following premises:

- It is a widely known fact that when technical specialties are concerned the specifics of the fast changes in technologies and equipment development presents financial burdens when buying modern equipment for highly specialized applications (electronics, communications technologies etc.). This leads to difficulties for the technical universities and colleges and limits their being up to date with the trends of these changes. One way out of this situation is the approbation of experimental simulation exploration of electronic circuits in the teaching process;
- Software environments for teaching analog and digital devices through circuits modeling and analysis are used with free licensing for students. Their interface is constantly being improved and their capabilities are being extended;
- Young generations possess much better computer literacy and are keenly interested in new technologies;
- The number of students who work full time but want to continue their education and to improve their qualifications is also increasing;

The laboratory in which students are taught can be used for laboratory experimentation in various courses in the curriculum and for conducting various short-term training courses. The software applications are identical for all the workstations in the laboratory which themselves are connected in a local area network. The students conduct practical and laboratory experiments integrating the theoretical material taught with the acquiring of professional experience.

III. SOFTWARE ENVIRONMENTS WITH FREE ACCESS USED IN THE TEACHING OF ANALOG AND MIXED SIGNALS CIRCUITS DESIGN

When using software environments as electronic tools of training the most important factor is the careful decision that is to be made as to which environment to use. The major criterion is the presence of a wide spectrum of applicability in several different courses included in the curricula. With regard to the improvement of the quality of the educational process and the optimization of the economic costs it is advisable to take into consideration the following factors when choosing a software environment:

- Wide spread of the software applications;
- Potential for maintenance and updating of the software applications;
- Availability of literature suitable for the teaching of the software applications;
- Requirements as to the parameters of the computer hardware to be used.

The following software products have been chosen for the teaching of analog and mixed signals circuit design in accordance with the aforementioned considerations.

A. NI Multisim

NI Multisim is an intuitive simulation educational environment that has libraries with over 26 thousand components (fig.1) of well-established and leading manufacturers of semiconductor components like Analog Devices, Infineon, Semiconductor and Texas Instruments [3]. The schematics behavior is evaluated through 20 modern SPICE analyses and 22 controlling and measuring devices (fig.2) that visualize the circuits behavior which students can investigate in the laboratories.

Fig. 1. Component libraries

Fig. 2. Controlling and measuring devices

NI Multisim is an appropriate training environment as it can be applied in: teaching the theoretical basics of analog circuits design; conducting laboratory experiments. It offers a complete approach in the innovative exploration of electronic circuits through the integration of the design of electronic circuits with the interactive simulation and analysis. Through the tuning and managing the virtual measuring devices the behavior of the scheme is visualized by using the "what if" scenario.

In the teaching of the students of analog circuits design in the Technical college of Smolyan the following simulation models developed within the NI Multisim software environment are being used:

- inverting and non-inverting amplifier designed with Operational Amplifiers (Op Amps);
- integrators and differentiators;
- sine wave oscillations generators;
- pulse generators,

which have been presented in previous publications. The simulation experiment precedes the laboratory experimentation with physical models which gives the students the opportunity to enhance their theoretical knowledge and to be aware of the implications of the laboratory experimentation results. Fig. 3 shows the schematics of a rectangular pulses generator designed with an integral timer in the graphics module schematic capture. The behavior of the schematics is explored with an oscilloscope and frequency meter. In this way knowledge is acquired at three levels: mastering of the theoretical fundamentals, simulation and experimentation. The verification of the simulation results increases the motivation of the students in order to acquire new knowledge.

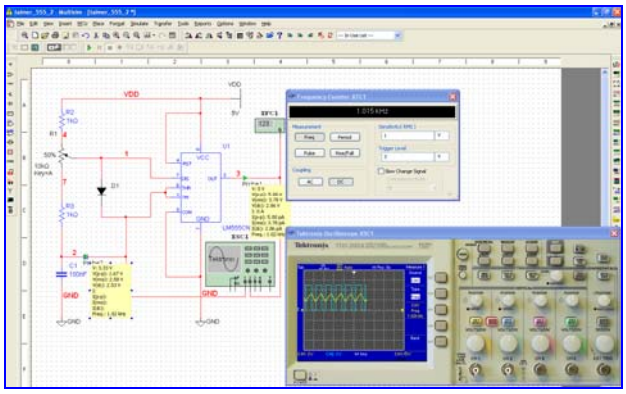

Fig. 3. Simulation exploration of a simulation exploration of a rectangular pulses generator

B. TINA-TI

TINA-TI is a free application – a product DesignSoft for Texas Instruments. It is fully functional but does not support some of the features present in the full version of TINA. The TINA-TI software package is intended for use in the teaching of electronic circuits through simulation and analysis. It works with linear and non-linear analog, digital and mixed circuits and offers a library containing more than 10,000 components. The schematic analysis is done with the help of about 20 analysis modes or 10 virtual instruments. The schemes explored can be edited while working and the results obtained can be analyzed.

- The software application offers analog macromodels: Amplifiers and Linear Circuits;
- Switched Mode Power Supplies;
- Noise Sourses;
- Sensor Simulators,

and each of them has been tested and is available to the user. They provide fast and effective way of simulating the efficiency of the circuits. Fig. 4 shows the simulation model of a generator of rectangular and triangular pulses created in the graphics editor Schematic Editor of the software environment and the oscillograms resulting from the oscilloscope readings.

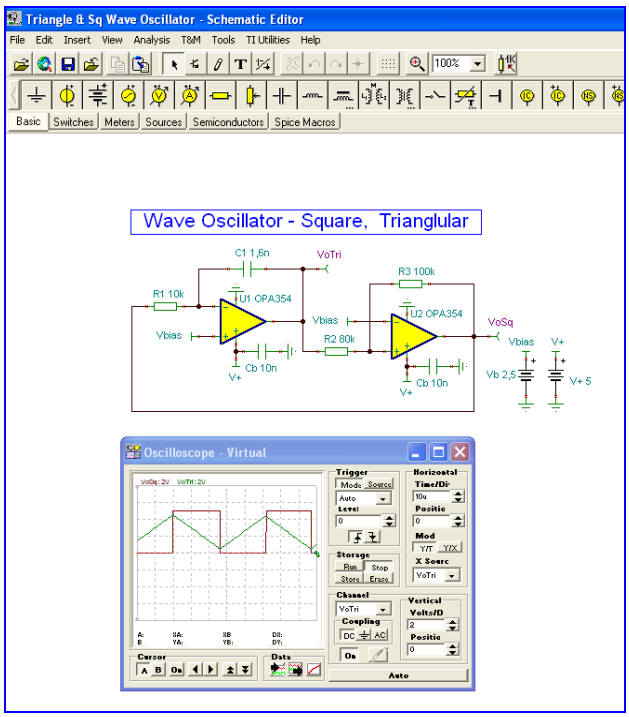

Fig. 4. Simulation model of a generator of rectangular and triangular pulses

TINA-TI possesses improved instruments (transfer functions and time responses) for the computation of calculations [4]. They are helpful in the self-study process of the students which includes writing papers and developing projects as well as exam preparation. They are conductive for the deeper understanding of the processes realized in the circuits and save valuable time by eliminating the need to check results of the computations based on formulae.

C. OrCAD

OrCAD is design software which prepares students from the corresponding specialties for the future engineering challenges through high precision design and visual interactive simulations. The different stages of the design process use various programming modules: graphical editor for the design, editing and storing of electronic circuits OrCAD Capture which can utilize extensive component libraries, including some available over Internet (registered users can access over 200 000 components); analog and analog-to-digital simulator PSpice A/D; graphical editor for the design of printed circuit boards OrCAD PCB Editor; an application for analysis of parasitic effects in printed circuit boards OrCAD Signal Explorer; an application for automated routing of printed circuit boards SPECCTRA for OrCAD; interface module SLPS for the integration of PSpice end MATLAB/Simulink [5]. OrCAD is suitable for the design and exploration of electronic circuits in the courses studied in accordance to the accepted curriculum. Fig. 5 shows the overall scheme of inverting Schmitt trigger, while fig.6 shows the analysis of the processes in time domain visualized in Probe.

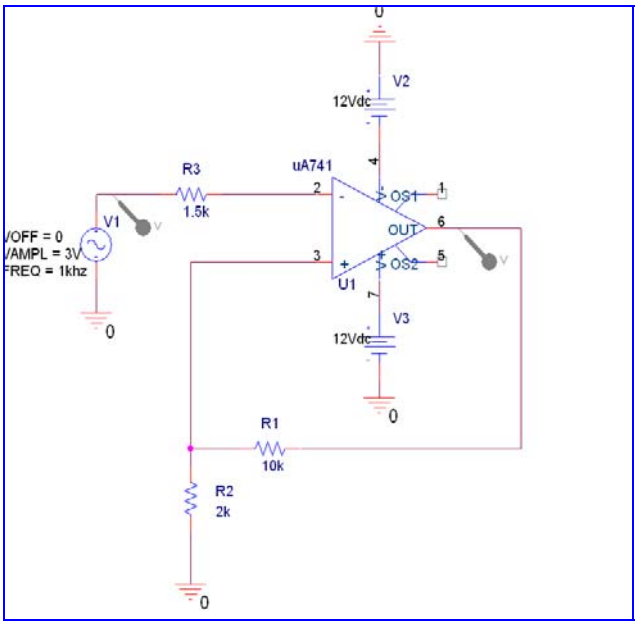

Fig. 5. Overall scheme of inverting Schmitt trigger

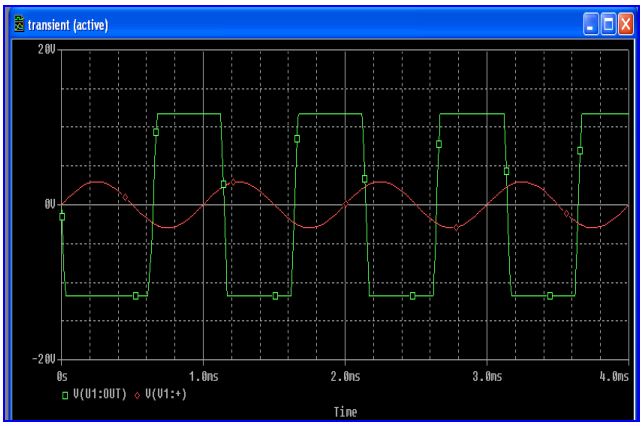

Fig. 6. Analysis of the processes in inverting Schmitt trigger in time domain

Table 1 compares the principal features of the software environments NI Multisim, TINA–TI и OrCAD, used in the courses in analog circuits design for students in the Technical college of Smolyan, studying in Communications and computer technologies and pursuing an associate degree. The software environment NI Multisim is used in the laboratory experiments, TINA-TI is used by the students in their self-study, while OrCAD is used for working on papers and projects.

In future is yet to come creation of analog circuits models in environments of LT Spice and WEBENCH® Designer. Both of them can regard as virtual laboratory for modeling of analog circuits.

TABLE .1 COMPARISON BETWEEN THE MAJOR FEATURES OF THE SOFTWARE ENVIRONMENTS NI MULTISIM, TINA TI AND ORCAD, USED IN THE EDUCATIONAL PROCESS IN THE TECHNICAL COLLEGE OF SMOLYAN

Software environment / **Features**	NI Multisim *National Instruments*	TINA TI *Texas Instruments*	OrCAD *Cadence*
Components (number)	26 000	10 000	200 000
3D virtual components	present	present	-
Virtual measuring devices (number)	22	10	-
LabVIEW instruments	present	-	-
Graphical editor	Schematic Capture	Schematic Editor	OrCAD Capture
Simulation Feature	SPICE	SPICE	PSpice
Analyses (number)	20	10	10
Educational applications	Conducting laboratory experiments	For: ▪ Self-study preceding lab experimentation; ▪ Preparation of projects and papers; ▪ Exam preparation.	For computer modelling and design of electronic circuits

IV. CONCLUSION

The paper discusses software environments used in the courses in analog circuits design taught to the students from the corresponding specialties in the Technical college of Smolyan. By using their features the lecturer and the trainees can work with existing models, and also design models through the combination of existing elements. Computer technologies allow the modelling of investigations into the properties of non-existing objects.

The electronic laboratory experimentation sessions promote the re-creation of the processes encountered in the physical technical devices being studied and the opportunities for their experimental exploration. The combination of the electronic and physical tools of education has an innovative character and creates a synergic effect on the quality of the educational and training process.

ACKNOWLEDGEMENT

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Computer Modeling of Transmitter of a Digital Communication System

Angel Hristov Chekichev, Daniela Antonova Shehova, Velislava Hristova Raydovska and Zlatin Ilkov Hunev

Abstract – **The report offers a computer model of the transmitter part of a digital communication system for data transmission, which was developed in the environment of Matlab Simulink.**

Keywords – **digital communication system, digital transmitter.**

I. Introduction

In the digital transmission of the information, fundamentally the new methods for signal processing allow creating devices with unique features, unavailable for the methods of analog signal processing.

The architecture of the digital communication systems ensures efficient use of the spectrum and the energy resource of the communication channel in ever-changing conditions of signal distribution in it [1].

The aim of the report is to provide a computer-based method for examination of the behavior of the transmission part of the digital communication system based on block-diagram, which was developed in the graphical environment for imitation modeling Simulink.

II. Digital Transmitter – Conceptual Block Scheme

It's presented conceptual block scheme of a digital transmitter in figure 1.

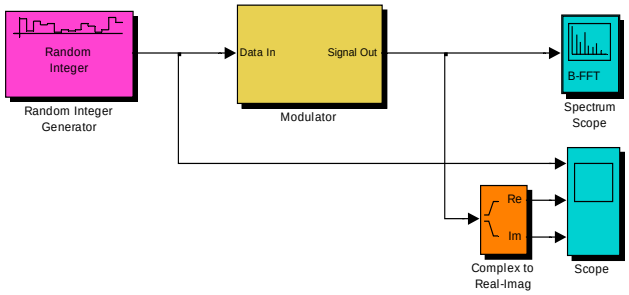

Fig. 1. Conceptual block scheme of a digital transmitter

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The model of a digital communication system allows the committing of a simulation examination under input data's shown in Table 1.

Table 1. The input data's for modeling of a digital communication system

№	Type manipulation	Positional of the constellations	Multiplicity of the constellation
0	BPSK	2	1
1	QPSK	4	2
2	8PSK	8	3
3	16PSK	16	4
4	32PSK	32	5
5	16QAM	16	4
6	32QAM	32	5
7	64QAM	64	6
8	128QAM	128	7
9	256QAM	256	8

In figure 2 are visualized signal constellations under different kinds of manipulations, and in figure 3 – their energy efficiency [2].

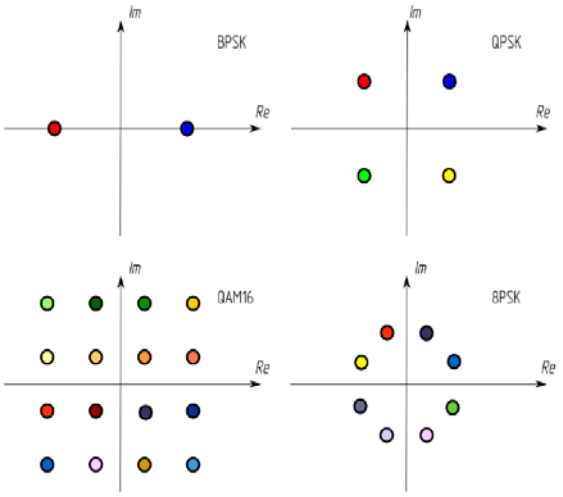

Fig. 2. Signal constellations under different kinds of manipulations

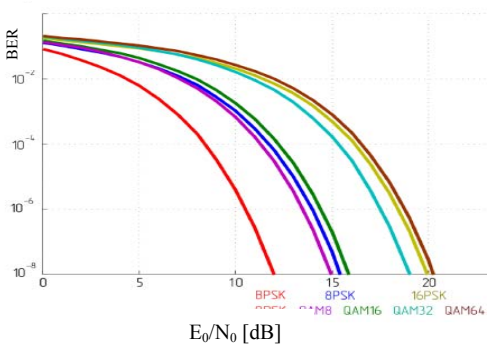

Fig. 3. Energy efficiency of kinds of digital manipulations

For the creation of the conceptual block scheme of a digital transmitter (fig. 1.) the following blocks are used [4]:

- Random Integer Generator – generator of random numbers;

In the settings of the generator of random numbers it is required to set positional assembly (M-ary number) according to the version (Table 1) and the sampling frequency - Sample Time 1/9600, which corresponds to the symbol rate of transmission data's 9600 baud/sec.

- Complex to Real-Imag – block for distribution of the real and the imaginary parts of a complex signal;
- Scope – the input signal of the oscilloscope is the signal from datas, according to the output complex signal of transmitter, which are distributed in the block Complex to Real-Imag;
- Spectrum Scope – analyzer of signal spectrum (spectrum-analyzer).

In the settings of Spectrum Scope it is necessary to indicate the size of the window of the fast Fourier transform - 1024 and includes a buffer input signal with buffer size - 1024 discretes.

- Modulator – it is formed by the signal of the transmitter and is constructed as a Subsystem presented in Fig. 4.

III. Modulator – Shaper of the Signal in the Digital Transmitter

An important block in the transmission part of the digital communication systems (fig. 1) is the modulator, which forms the signal, emitted by the transmitter. The modulator is constructed as a Subsystem, structure of which is shown in fig. 4.

For clear study processes, the formation of the signal in the modulator made by given below blocks:

- 1-D Lookup Table – correlation table (the veracity);
- Raised Cosine Transmit Filter – forming filter with characteristic feature of cosine increases;
- Gain – signal amplifier;
- Discrete-Time Eye Diagram Scope;
- Discrete-Time Signal Trajectory Scope – block, for display the trajectory of the vector of the complex signal envelope on the plane;
- Discrete-Time Scatter Plot Scope – block, for display of the diagram of the scattered signal.

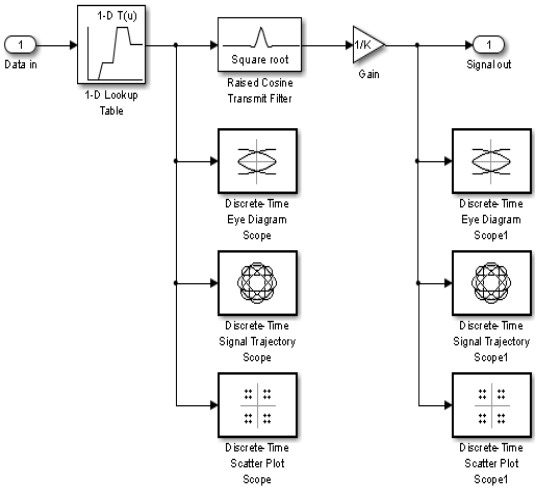

Fig. 4. The structure scheme of the shaper of a signal in the digital transmitter

TABLE 2. THE CORRELATION TABLE FOR VARIOUS TYPE MANIPULATIONS

Manipulation	Positional of the constellations	Datas for the transmission				Output of shaper of the complex envelope			
BPSK	2	0		1		-1-1j		+1+1j	
QPSK	4	0		1		-1+1j		+1+1j	
		2		3		+1-1j		-1-1j	
QAM16	16	0	1	2	3	-3+3j	-1+3j	+1+3j	+3+3j
		4	5	6	7	-3+1j	-1+1j	+1+1j	+3+1j
		8	9	10	11	-3-1j	-1-1j	+1-1j	+3-1j
		12	13	14	15	-3-3j	-1-3j	+1-3j	+3-3j

A. Block 1-D Lookup Table

For the proper functioning of the Subsystem, the appropriate setting in Function Block Parameters: 1-D Lookup Table has to be carried out.

In the determination of the correlation table (1-D Lookup Table) the correlation between the vector input symbols and the points of signal assembly are proved.

In the field Breakpoints of the dialog box for parameter settings of the block 1-D Lookup Table, the vector input symbols, according to the position assembly (Table 2) are proved. For example, for 16QAM it is: [0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15] (fig. 5.). For manipulations of higher-order a method for automatic generation of vectors in MATLAB is being used.

In the field Table Data the points of constellations, corresponding to the input symbol are proved, as for 16QAM they are:
[-3+3*i -3+1*i -3-3*i -3-1*i -1+3*i -1+1*i -1-3*i -1-1*i +3+3*i +3+1*i +3-3*i +3-1*i +1+3*i +1+1*i +1-3*i +1-1*i], (fig. 5.).

The correlation table for various type manipulations, needed for the setup of this block is shown in TABLE 2.

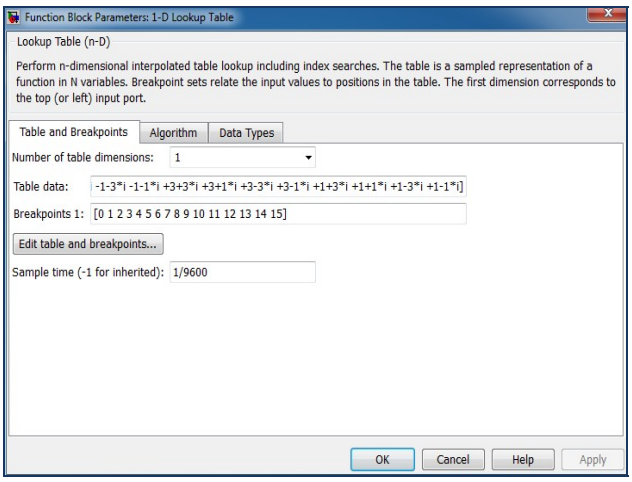

Fig. 5. Parametric settings of block
1- D Lookup Table

B. Block Raised Cosine Transmit Filter

Restriction of the signal spectrum is carried out by a block Raised Cosine Transmit Filter. Filter settings for the performed simulation studies are reported in TABLE 3.

The complex signal from the output of the forming filter enters in Gain, in which its norming is carried out.

The transmission factor of the amplifier is equal to 1/K and is estimated with the formula:

$$K = \sqrt{\frac{1}{N}\sum_{i=0}^{N-1}|s_i|^2}\ , \qquad (1)$$

in which N – positioning assembly (constellation).

The parameter settings made in the functional block Raised Cosine Transmit Filter are shown in fig. 6, and fig. 7 illustrate the fundamental characteristics of the Filter.

TABLE 3. SETTINGS OF RAISED COSINE TRANSMIT FILTER

Settings of Raised Cosine Transmit Filter		
1.	Filter Type	Square Root
2.	Group Delay	5 symbols
3.	Rolloff Factor	0.8
4.	Upsampling factor	8
5.	Input Processing	sample based

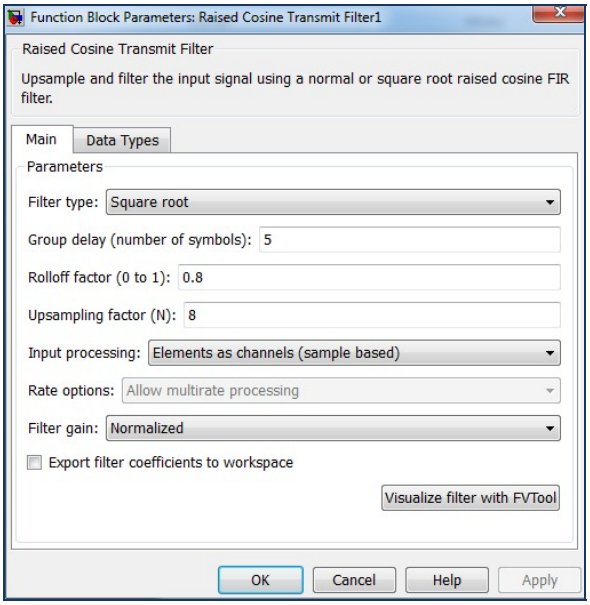

Fig. 6. Parametric settings of block Raised Cosine Transmit Filter

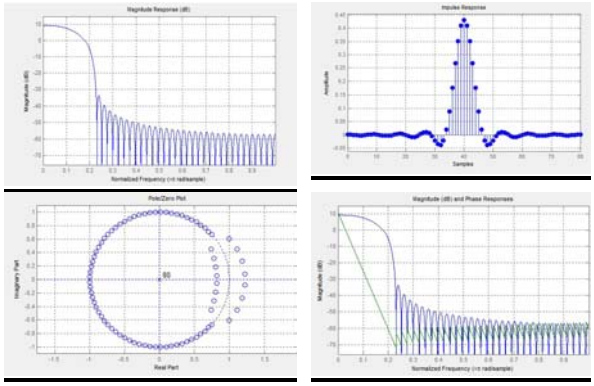

Fig. 7. Basic characteristics of the Filter

As it was already explained the blocks Discrete-Time Eye Diagram Scope, Discrete-Time Signal Trajectory

Scope, Discrete-Time Scatter Plot Scope are designed for viewing the processes of the forming signal in the modulator. The results from the simulation studies are shown in fig. 8.

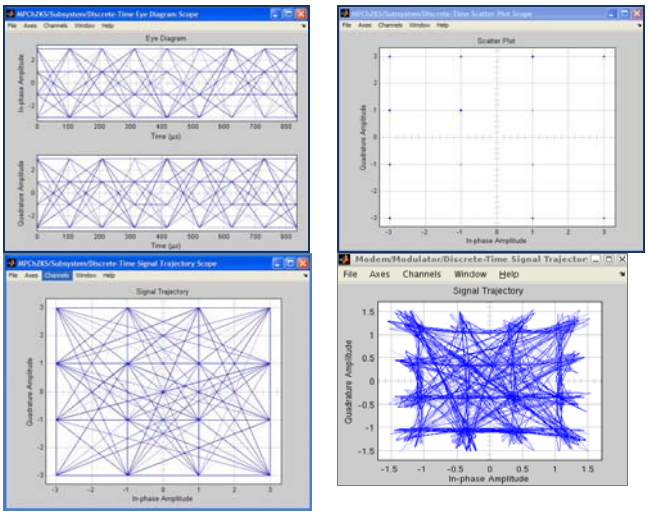

Fig. 8. Blocks for display of the information for the forming signal

The spectrum of the formed signal in the transmitter of the digital communication system from fig. 1 was observed with the virtual Spectrum Scope.

The parametric settings for optimal functioning of the block are shown in fig. 9, and in fig.10 the spectrum of the formed signal is displayed.

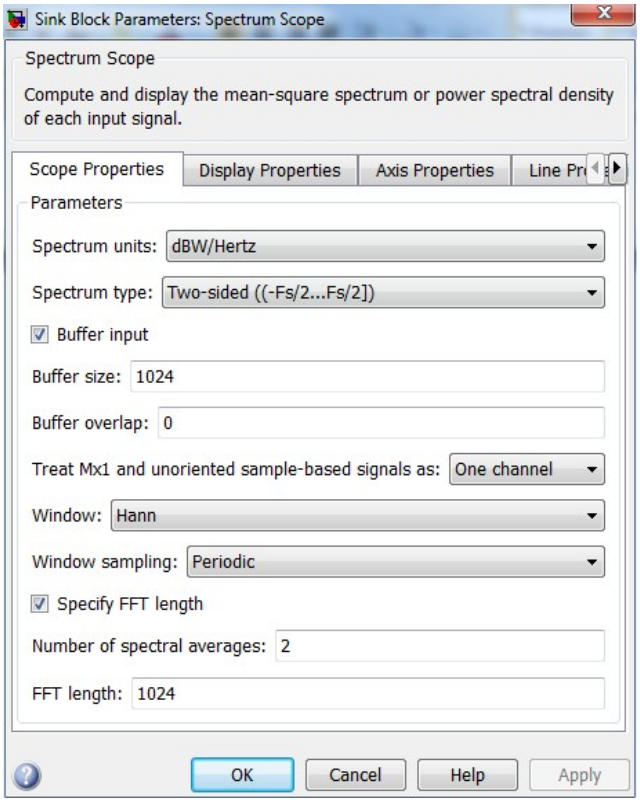

Fig. 9. Parametric settings on Spectrum Scope

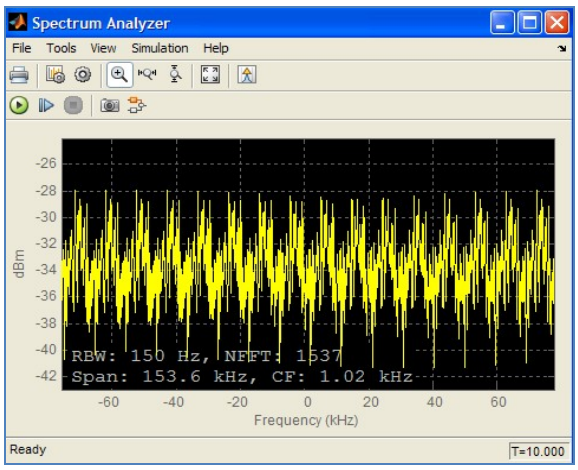

Fig. 10. The spectrum of the formed signal

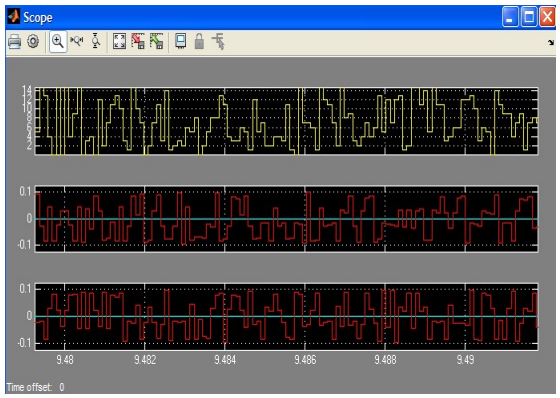

Fig. 11. Waveforms, observed with triple-channel oscilloscope transmitter output

IV. Conclusion

The creating of a computer model of the transmitter of a digital communication system provides an opportunity to visualize the forming process of the transmitted signal. In a subsequent report the authors will present models of the communication channel and the receiving part of the communication system, and a comprehensive computer model of a digital communication system will be build.

Acknowledgement

The authors would like to acknowledge the support of the "Research & Development" division of Plovdiv University in the project: НИ15-КС-016/24.04.2015.

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Software Management of 3D Printer

Slavi Yasenov Lyubomirov, Milena Ilcheva Nedeva, Milena Krasimirova Bundeva and Ivaylo Detelinov Uzunov

Abstract – **This current report „Software management of 3D printer“– a working model is a continuation of another report which reviews a hardware platform for making a 3D printer. The aim of this report is to present the software realization, configuration and programming of a firmware for the realized working model of a RepRap 3D printer.**

Keywords – **Firmware, model of a RepRap 3D printer**

I. Introduction

The main conceptual aspect considered in this report, is a modern 3D printing technology which turns a 3D computer model (CAD) into a real physical object depending on the size of the used model. Open Source technology called FDM (Fused Deposition Modeling) consists of series of thin layers of molten thread of the used material to achieve the shape of the desired object. This makes the three – dimensional (3D) print entirely different from the traditional technology, in which the shaping form of the desired object usually takes material.

The type of technology for printing a 3D model includes materials such as ABS and PLA.

ABS (acrylonitrile butadiene styrene) – this kind of plastic is used in monitors, coffee machines, TVs, mobile phones production.

PLA (polylactide) – this kind of plastic is made by bio - degradable products, such as cornstarch and potato starch, sugar beet and other raw starch containing materials [1].

II. Firmware of a RepRap 3D printer

The main software management of a REPRAP 3D printer, this report features consists of three parts:

- firmware;
- software for communication and control of RepRap 3D printer;
- Bench software Slicer and CAT.

Fig.1 represents a scheme of a printer software management from the creation of a 3D CAD model to its sending to the printer for printing.

Firmware is a specialized software micro – programme, which programs and is stored in a printer`s microprocessor. In the memory it is stored as ROM, EPROM and flash - memory.

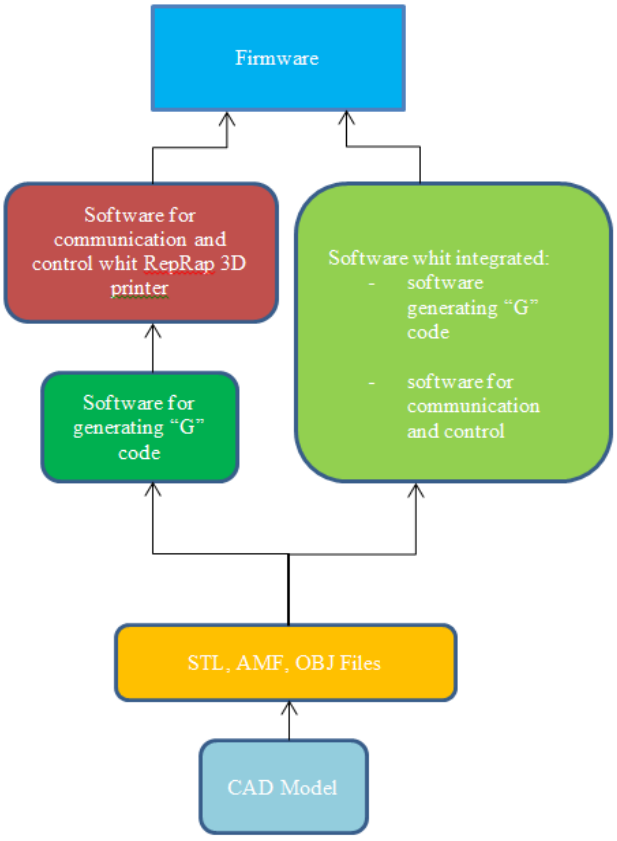

Fig. 1. Scheme presenting software management of a printer

These programs have all embedded systems, such as the RepRap in the 3D printer. In this way it affects all components of the device and synchronizes their functions in the best possible way. A program used for shaping a detail is made by the "G" and "M" languages. Commands /codes/ with address "G" are called preparatory and are responsible for the setting of the machine to perform a certain task. Codes with address "M" are called auxiliary.

The "G" and "M" languages are a popular name of a programming language, developed for the management of machines with digital – programme management.

A. Commands for linear movement

Commands for linear movements are the most widely used G-codes. They define most of the movements of the RepRap 3D printer, which could be linear with ultimate speed or circular with defined submission. These commands include all the instructions for interruption or

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modification of submission. All the functions in a firmware read or generate "G" and "M" commands.

Fig.2 shows a block scheme for the management of firmware of a 3D printer. Apart from the G-codes in a working model of a RepRap 3D printer, auxiliary "M" commands are also used [1, 2, 3].

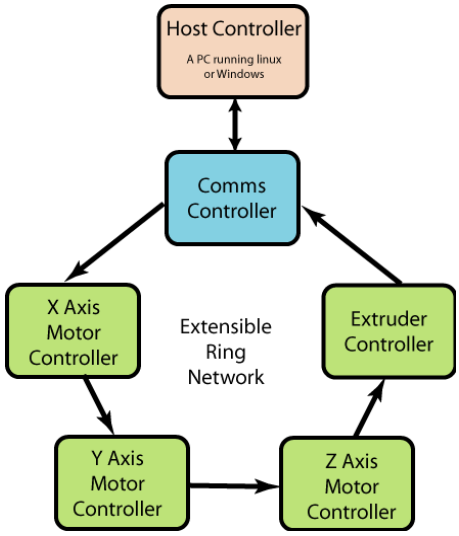

Fig. 2. Management of a firmware

The Programming of the controller, which manages the printer, is carried out by PC and by USB interface in connection.

In recent years, with the development of microcontroller's extension and the enlargement of their scope of options, that enables pre-programming of systems and the increase in the random access memory and program memory capacity, interfaces, and their number of digits, lead to a fast advancement of high level preprogrammed systems. These systems have disposal of standard interfaces such as:

- RS 232;
- USB;
- Ethernet,

And they are elaborated by new companies as open code projects in which the final product does not require an expensive programming hardware from every programmer or an amateur [1].

Preprogrammed systems are factory preloaded with a miniature microprogram named bootloader, whose aim is to allow the user to preprogram the system without the modification of a standard company programmer. These systems were further developed thanks to their mass production as an open code software and free software, which makes them attractive, easy to use and most important-cheap enough for the mass user to use effectively. The programming of such controller, for example for RepRap 3D printer, requires a computer and development environment Arduino.

The development environment Arduino is written in Java and is based on Processing. It uses an AVR-GCC compiler and the programming language is accomplished by is Wiring, which resembles the programming language C++.

B. Setting of a firmware for RepRap 3D printer

- Hardware setting

Before compiling and "sending" the firmware to the device memory, it is necessary to configure the RepRap 3D printer to ensure its proper working .The settings for the configuration file are very important "Configuration.h" [4, 5].

One of the main steps is the configuration of the serial port, which is located on the printed circuit board (PCB). On the basis of the values of the resistor, the temperatures of the extruder and the heated bed, which is responsible for the RepRap 3D printer that prints work, are calculated. This resistor is shown in fig. 3.

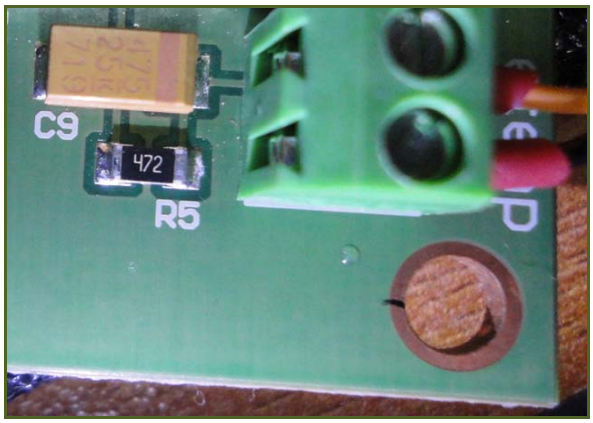

Fig. 3. Serial resistor

It can be seen that its notation 472 which means that the resistor is 4700 Ω. Preset the configuration constant SERIAL_R to 4700

```
#define SERIAL_R 4700
```

Next step is to choose a value for speed of communication. This is the speed used for communication between software which manages the printer interface of Marlin firmware.

```
#define BAUDRATE 115200
```

The third step is to choose the number of sensors to use. It is achieved through configuration of constants. We have to bear in mind, that the developed 3D printer has a sensor of the extruder part and sensor of the bed, units are given only to „TEMP_SENSOR_0" and TEMP_SENSOR_BED.

```
#define TEMP_SENSOR_0      1
#define TEMP_SENSOR_1      0
#define TEMP_SENSOR_2      0
#define TEMP_SENSOR_BED    1
```

The type of the used sensor (thermistor) is EPCOS NTC G560 B57560G107F 100K - 100000 Ω. The value of the configuration constant is E_NTC 100000.0.

```
#define E_NTC 100000.0
```

The type of plastic which is used by default is ABS.

To set the starting temperature 0 °C, the following relation is used [3]:

$$C = K - 273{,}15. \quad (1)$$

The value of the configuration constant is ABS_ZERO - 273.15

#define ABS_ZERO -273.15

These values of the configuration file are very important because the proper temperature of printing depends on them.

It is known that analog – digital converter is 10 bit (by the previous article) and it has a range of 2^{10}, which means that it is between 0 and 1023, so in this case the resistance of the thermistor will be R = V.RS/(1023 - V). The temperature resistance is calculated by the following formula:

$$r_e = R.e^{-\frac{BETA}{T}}, \quad (2)$$

Where:

BETA is coefficient with size [K] and its value is from 2000K to 5000K and T is calculated by this formula (3)

$$T = \frac{B}{\ln\left(\frac{R}{r_\infty}\right)}, \quad (3)$$

where:

R is the resistance of the thermistor,

B is coefficient with size [K] – from 2000K to 5000K,

r_∞ is temperature resistance.

#define E_BETA 3974.0
#define E_RS SERIAL_R
#define E_NTC 100000.0
#define E_R_INF (E_NTC*exp(-E_BETA/298.15))

Here the minimal temperature is calculated when the heater turns off. What follows is to check whether the thermistor is connected properly or whether it is damaged. In case it is, it will not switch off. Here the constants are HEATER_0_MINTEMP 1 for heater of the extruder and BED_MINTEMP 1 for the heated bed

#define HEATER_0_MINTEMP 1
#define BED_MINTEMP 1

The heater will switch off when it reaches the maximum preset temperature in order to avoid overheating. This function is used to protect the heater and inputs of the plate.

MINTEMP is used to protect the thermistors , where constants are HEATER_0_MAXTEMP 275 for the heater of extruder and BED_MAXTEMP 150 for the bed heater.

#define HEATER_0_MAXTEMP 275
#define BED_MAXTEMP 150

Manual setting of a firmware

These settings are:

- configuration of final stop blocks;
- stepper motor;
- base area where the printing is made;
- steps for certain unit, in this case per millimeter.

The setting in which one of the axis reaches the final switch for the starting point of the coordinate for either axis. Permitted values are: true and false.

#define min_software_endstops true

A setting in which the axis does not exceed the limits preset - permitted values are: true and false

#define max_software_endstops true

Maximum range from 0 to the final switch, which an axis could go is introduced by constants X, Y, Z in millimeter:

#define AXES_MAX_LENGTHS {190, 190, 200}

Normal velocity mm/min

#define HOMING_FEEDRATE {10*60, 10*60, 1*60, 0}
Rapid speed mm/min

define FAST_HOME_FEEDRATE {50*60, 50*60, 3*60, 0}

After all settings have been adjusted, maybe the most important is to tune the settings of the RepRap 3D printer and the number of steps per millimeter the stepper engine can make.

It is known that there are 4 axis, so the steps must be set for axes X, Y, Z and feed motion of the material of the extruder E.

#define DEFAULT_AXIS_STEPS_PER_UNIT {80.0000, 80.0000, 4000, 561}

It is particularly important while doing these settings to know the specifications of stepper engine – degree of step, model of strap, number of teeth of the gear - wheel, the distance between carvings of a sprig and micro steps of the driver.

The chosen model strap is GT2 with interdental distance of 2 mm, the gear-wheel used has 20 teeth with distance between the carvings of the sprig 0,8 mm and micro steps of the driver 16;

The Formula for the steps per millimeter for axes X and Y is:

$$\text{Steps per millimeter} = \frac{\left(\frac{360^o}{1{,}8^o}\right).16}{2.20} = 1454{,}55 \quad (4)$$

Where:

dbts - the distance between the teeth of the strap;
msd – micro steps of the driver.

There is no strap, so for axis Z, the formula is transformed and reduced to:

$$\text{Steps per millimeter} = \text{steps per millimeter on axis Z} \quad (5)$$

The formula for the extruder E for steps per millimeter is the following:

(6)

If:
The number of detents of the big gear = 45;
The number of detents of the small gear = 11;
The diameter of the working part of the feed = 7mm;
The result is:

$$\frac{(200.16).\left(\frac{45}{11}\right)}{7.3,14159} = \frac{13088}{21,99}.\frac{100}{105,7} = 561 \text{ steps/mm.}$$

In this way the already adjusted firmware is ready to be compiled and transferred to the memory of the controller.

III. CONCLUSION

The technology used in the 3D printer production leads to some basic conclusions, formulated as follows:

Technology enables making a lot of unique products and articles made to order;

It enables the production of more complicated forms, which is impossible through the means of traditional methods. It is hard to enumerate all the examples, of the utility of 3D printing. One thing is certain – this technology is yet to enter in our everyday life, medicine, manufacture, and art and security services;

3D printing will certainly develop in next years, as one of the fifth leading trends, which will change the technologies and the world in 2015.

The best thing is that the 3D print “opens the door” for creativity and innovation.

ACKNOWLEDGEMENT

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Software Platform for Security Alarm System

Slavi Yasenov Lyubomirov, Velislava Hristova Raydovska, Angel Hristov Chekichev and Milena Ilcheva Nedeva

Abstract – **The concept of the proposed paper is to develop a software supporting the operation of security alarm system. The system was presented in a previous report at a scientific forum [1]. The main tasks are highlighted in the paper and they are: the choice of language and platform for application of the security system; choice of language and platform for the mobile application management of alarm systems; compilation of applications and test applications in a real environment.**

Keywords – **firmware, security alarm system, mobile application, programming environment.**

I. INTRODUCTION

We are witnesses of the continuous development of microcontrollers and microprocessors, as an integral part of embedded systems, which are increasingly used in a variety of areas: automation, telecommunication, wireless telecommunications, handheld devices, cars, automated vehicles, telematics, medical systems, monitoring and control and more. The application for the monitoring and control is the subject of development, described in this paper.

We live in an innovative society in which the technology accompanies every aspect of our daily life. Along with that comes the need for safe and effective methods of protection for our homes, properties, expensive equipment, on which the business depends, and other aspects of our everyday life. In order to achieve an effective protection we need a system that combines fast notification when there is an intrusion into the protected object or when dangerous conditions arise. The system must have a possibility of control and management from any remote point.

Nowadays, the manufacturers of security alarm systems offer a variety of interesting solutions for security of objects. There are some solutions that are closer to the development, which are described in the paper, but the idea for the realization of this project is up to few questions:

- Is it possible to create a system, which will perform its requested objectives and needs, only with the knowledge and skills of the students acquired in the process of training at the Technical College – Smolyan?
- Is it possible to realize an application for remote control of signal - security system? Most of the available systems are enabling the possibility of control by sending an SMS with a specific content.

But what would happen if the owner of this system forgets what the content and the syntax of the message should be.

- Is it possible to realize the project with hardware and open source software, in order to be as competitive as the commercial products of the same kind on the market?

The security system which was constructed, works on the basis of the modern microcontroller Atmega 2560. It has capabilities for a wide range of sensors, adequate differentiation, separation of the signals and timely communication with the user via GSM module [2, 5].

II. SOFTWARE PLATFORM SELECTION

Before the realization of the system, a detailed selection of the hardware components has been made. This description is given in a previous report of the authors. It is a fact that development environment and programming language must work well in this kind of development.

It is also necessary to take into account the following circumstances when choosing a software platform:

- The implementation of the hardware platform must be able to realize the basic functions, i.e. it contains relevant inputs for monitoring and corresponding outputs for control;
- The choice of software platform must be reduced to a suitable programming language and development environment that supports the microprocessor system, from which the alarm systems are built.

III. ENVIRONMENTAL DEVELOPMENT AND PROGRAMMING LANGUAGE SELECTION

Considering the above circumstances, for the realization of the system is used an Arduino platform, whose programming environment is similar to the language Processing / Wiring. It is known that the software is an open source and completely free, which allows us its modifying and usage without any licensing agreements.

The developmental environment of Arduino includes a text editor for writing code, a message box, a text console toolbar for main functions and a variety of menus to facilitate users. The environment allows a communication between hardware and Arduino environment, testing the program and uploading the executable file in development board.

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Another key point is that the Arduino IDE is written in JAVA, which makes it a multiplatform application that enables us to use it on different operating systems: Windows, Mac OS X and Linux [3, 4 and 5].

It is logical to use Arduino frameworks for the realization of the software part. The main advantages are:

- Arduino`s developmental environment, which enables writing a code and uploading an appropriate hardware very easily;
- it is written in JAVA, which allows it to be run by different operating systems;
- there is an integrated test editor with coloring of the source code;
- there is an integrated compiler, which converts the source code into machine;
- there is an integrated debugger for checking the code;
- there is an excellent compatibility with Arduino`s hardware.

The basic structure of the language for Arduino is relatively simple and is consisted of at least two parts - function setup() and loop(). These two required parts (or functions) "wrap" the block`s statements. Besides that, external functions may be declared. If necessary they are called out from one of the two main functions subsequently, so the external functions appear as components of the basic functions.

IV. Block Diagram of the Software Platform

The program structure is illustrated by the block diagram in Figure 1.

There are described the characteristic variable declarations at the beginning of the program (and they are not only for that language). The libraries, that are used, are defined at the beginning too. Behind their definitions a description of the two statutory functions Arduino platform, setup() and loop() is made. In the course of their work these two functions call out other external actions that are described. These are the AutoTurnOn() and the GSMSetup() functions for The Function setup() and temperature() and sendSMS() for the Function loop () . Foreign functions that are called out from setup(), are unconditionally executed. There are no circumstances in the body of this function, due to the fact that it is performed only once, when the device starts working. Foreign functions in the body of the loop() can depend on some conditions, i.e. they can or cannot be called out, although they are described in the program [3, 4, 5].

A. The function AutoTurnOn()

Typical of the GSM module, which is used in this project, is that it cannot be switched after the supply of the power system until the moment you press and hold the button S_PWR for two seconds. This action can be performed programmatically, through the terminal of the GSM module, which is responsible for this task and is connected to terminal 23 digital pin on the Arduino Mega 2560. Part of the code is as follows:

```
/***this function turn on the GSM module***/
void AutoTurnOn(){
  pinMode(23, OUTPUT);
  digitalWrite(23,LOW);
  delay(1000);
  digitalWrite(23,HIGH);
  delay(2000);
  digitalWrite(23,LOW);
  delay(3000);
}
```

While analyzing the algorithm of the function AutoTurnOn() we can notice that it describes programmatically the actions that would be applied if the module was used manually.

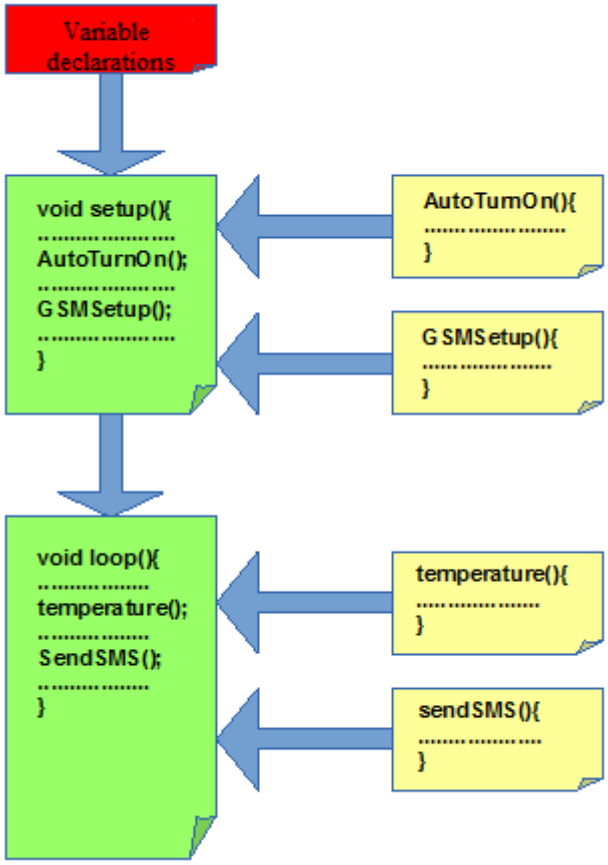

Fig. 1. The block diagram of the program security system

B. The function temperature ()

The value obtained from the temperature sensor at specific analog input from the microprocessor, is converted into a digital form. The software realization is carried out by function temperature(), which performs the algorithm. Part of the code is as follows:

```
/***Temperature function***/
void temperature(){
SensorValue=analogRead(A5);
Sensormilivolts=(SensorValue/1023)*5000;
kelvin=Sensormilivolts/10;
celsius=kelvin-273.15;
fahrenheit= ((celsius * 9)/5 +32);
```

```
  // Serial.print(kelvin);
  // Serial.println(" Kelvin");
  Serial.print(celsius);
      Serial.println(" Celsius");
      // Serial.print(fahrenheit);
      //Serial.println(" Fahrenheit");
      delay(200);
  }
```

C. The function GSMSetup()

This feature adjusts the GSM module according to its necessary needs. The setting is done by sending specific IT commands to the module.

```
  /***This function setup GSM module***/
  void GSMSetup(){
      gsm.println("AT+CMGF=1"); // set SMS mode to
        text
      delay(1000);
      gsm.println("AT+CNMI=2,2,0,0,0");
      delay(1000);
```

D. Description of the function

There are two methods for transmission of SMS. In the first PDU Mode, the message is in the form of a string of hexadecimal numbers. Activated by "AT + CMGF = 0". The second method, which is used, is the Text Mode. In this case the message is in the form of a text that can be read easily. Sending a command "AT + CNMI == 2,2,0,0,0" to GSM module is of particular importance. Thus the incoming messages are not stored by the module in the memory of the SIM card and the module forwards them directly to the TA (Terminal Adaptor).

E. The function "sendSMS ()"

The function "sendSMS ()" sends SMS to a fixed number upon activation of any of the sensors. The microprocessor system detects which sensor is activated and sends a text message with a specified content [1]. For example, if there is a glass breaking, the contents of SMS-s will be "ALARM acoustic", if there is a high temperature in the room; the contents will be "WARNING High Temperature", etc.

```
  /***This function send SMS***/
  void sendSMS(){
      gsm.print("AT+CMGS="); // now send message...
      gsm.write((byte)34);// ASCII equivalent of "
      gsm.print(phoneNumber);
      gsm.write((byte)34); // ASCII equivalent of "
      gsm.println();
      while(gsm.available())
          Serial.write((byte)gsm.read());
      delay(500);
      Serial.println();
      gsm.print(alarm[i]); // our message to send
      gsm.write((byte)26); // ASCII equivalent of Ctrl-Z
      // this will send the
        following:AT+CMGS="phonenumber"<CR>
      // message<CTRL+Z><CR>
      delay(500);
      gsm.println();
      while(gsm.available())
      Serial.write((byte)gsm.read());
      delay(500);
      Serial.println();
      delay(15000); // The GSM module needs to return to
        an OK status
  }
```

It cannot be determined to which kind of category belong this software application. Rather, it belongs to another kind of category, which is called software for embedded systems. We would say that for the realization of the program the methodology "writing code and fixing " is being used. The reason for this is that the project is relatively small and the problems are being removed from the beginning of the process of work until the end. This is attractive choice when the time for product development is greatly reduced, because the code writing begins immediately and therefore achieves results quickly.

The disadvantage of the methodology occurs if some serious architectural problems are found later through the development process, because it requires large parts of the code to be rewritten. There are alternative models that can help capturing such problems at an earlier stage, when changes are easier and cheaper to be made.

The next step is the building process. It is known that programming errors are removed at this process, of course, if there are any. The several errors were found during the compilation. They were mostly of syntactic and algorithmic nature. The errors were removed until the successful compilation of the program.

Checking the size of the application and the required enough memory, which is available to the Arduino - board where you boarded- are an important aspect. The Arduino board which was chosen has a 256 Kbyte memory. The application has a size about 12 Kbyte, so that the available memory is sufficient for our application.

It is necessary to implement the process of upload or upload the application of the Arduino development board upon successful compilation. Re-checking the source code for errors is being done during the upload.

V. Environment for Implementation of the Mobile Applications - J2ME

When developing a mobile application- a java 2 micro edition (j2me) is being used. It combines the limited resources jvm JavaScript virtual machine and a set of APIs (apis) application development for mobile devices. APIs cannot be run on traditional JavaScript virtual machine. They are compatible only with jvm, provided by j2me environment. This is due to the fact that mobile devices have limited resources of memory. The environment j2me is installed by the manufacturer of the mobile device and the applications' developers have no relation to this process.

There are seven steps of creating MIDlet. These steps are: design, coding, compilation, verification of the compliance, created packages, test and an upload device. Some of these steps may be omitted, but the design, writing the code and the compiling process are required.

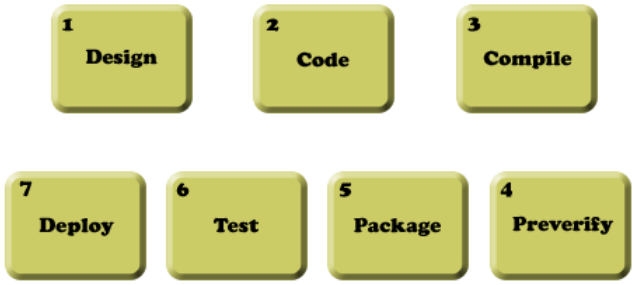

Fig. 2. The Steps at creating a MIDlet

The next stage is when the application is ready to be used in a real environment. It must be installed at a real device. There are two ways to accomplish this. The first is via a USB cable or a Bluetooth wireless communication. Most devices supporting JAVA, allow installing the application. The second way is more interesting-It opens the application to the outside world via Internet. The device must be connected to the Internet via its built-in browser. Before that we should upload mobile application at a WEB server. We should bear in mind what the size of the contents of the host will be, because it will be accessed from the mobile browser, which has limited resources. The application can be downloaded and installed on the mobile device when the host is available.

VI. Testing the Application in a Real Environment

The application testing is the final step. We need a certain period of operation of the system in a real environment because a few things must be established:

- If the application is stable at work, i.e. If there are periods in which it works and others in which it does not work;
- If the application affects the temperature of the system. It is possible for the system to be overloaded due to programming errors and this can affect the temperature of the microprocessor and other components;
- If the application responds to our expectations, i.e. If It performs all the functions which are set in in the source code;

The findings from the testing of the application are as follows:

- Whether the application works stable. There are no periods when the application does not serve its purpose;
- The work of the application does not influence the temperature of the system during continuous operation;
- The application meets our expectations, all the functions, described in the source code, are operating normally.

VII. Conclusion

The advantage of our application is that it is not necessarily a specific text message to be remembered. It is easy for usage and is protected from an unauthorized access.by password

The product is able to compete with similar commercial products at the market. The functionality has still unused additional opportunities, thanks to the Arduino platform. Its cost is similar to the cost of its competitors, but when it is implemented at mass production, the price will decline.

Acknowledgement

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Isolating Real-time from Processor-intensive Processes in Embedded Multi-core Systems

Piet Cordemans, Nico De Witte, Jens Vankeirsbilck, Willem Melis and Jeroen Boydens

Abstract – **Multi-core embedded systems allow to isolate critical processes on a CPU, while management is provided by a single operating system. This provides an opportunity to address real-time and security issues. We try to determine if processes can be effectively isolated under heavy processor load in a setup with the *Radxa*, a quad-core embedded system, and Linux *cgroups*. In our experiment we measure the variance of a time-critical signal while stressing the system. We explore different scenarios and determine the optimal configuration.**

Keywords – **Embedded operating systems, multi-core, soft-realtime**

I. INTRODUCTION

Linux is in essence a time-sharing, multi-user operating system, which is focused on maximizing throughput. In order to prevent starvation due to prioritization, fairness is guaranteed in scheduling processes. Although a high-throughput of processes is a desirable property of an OS, Linux cannot preempt processes when executing system calls, or preempt kernel processes. Moreover the difference between minimal and maximal response time of a processes, this is known as jitter, cannot be limited for certain time-critical processes. In effect Linux sacrifices deterministic scheduling and cannot guarantee real-time behavior in favor of throughput and focusing on usability from a user perspective [1].

In contrast, a Real-Time Operating System (RTOS) favors deterministic scheduling and minimizes jitter for real-time critical processes, which are desirable properties when dealing with embedded hardware.

Nevertheless, embedded Linux is the favored OS for embedded systems despite the lack of real-time features.

A. Multi-core organization

As multi-core embedded systems are adopted, the organization of CPU's offer opportunities to isolate time-critical from data-intensive processes. This is called the planar pattern, in which a control plane and data plane are defined [2]. By assigning the necessary hardware resources to the control plane, the time-critical processes are no longer interfered by the processes in the data plane, which utilize the other hardware resources. In order to optimize the utilization of hardware all resources which are not needed in the control plane are assigned to the data plane.

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The planar pattern can be applied in two general hardware configurations. On the one hand is the Symmetric Multi-Processing (SMP) organization, which involves a single OS to manage all available cores. In a SMP configuration all memory is shared which facilitates communication between processes. Furthermore it allows for an optimal use of resources and is flexible when more processes are added to the system.

On the other hand is Asymmetric Multi-Processing (AMP) organization, in which no longer a single OS manages all cores. Different configurations are possible to assign operating systems, real-time operating systems or no OS at all to a single CPU or a group of CPU's. In this setup isolating processes can be achieved by assigning these processes to separate operating systems.

In this paper we evaluate a technique called *cgroups* to isolate time-critical processes in a SMP organization. This should allow to combine the benefits of a SMP architecture with isolation of real-time critical processes.

Several approaches of adopting real-time behavior have been examined for embedded Linux. Papaux et al. [3] describe virtualization on an embedded system with KVM and measure performance degradation. However they do not consider jitter and variability in real-time critical processes. They rather focus on throughput of the virtualized system.

Varanasi and Heiser [4] developed a hypervisor which supports the hardware extensions of ARM. They conclude that virtualization extensions reduce hypervisor complexity and make it a viable approach with minimal instruction cycle overhead. They mention real-time support with a real-time clock which is configured as a pass-through device. However their implementation does not support a multi-core architecture.

Brandt et al. [5] describe a scheduler which supports a mix of best-effort, hard- and soft-real time processes. This scheduler is not compatible with the Linux operating system and does not support multi-core processing.

Considering reliability, two approaches have been examined. On the one hand Lee et al. [6] proposed a task remapping technique in order to increase reliability. It depends heavily on an extensive compile-time analysis.

On the other hand in [7] Huang et al. implemented a fault-tolerant task scheduling system for multiprocessor embedded systems. It considered both transient and permanent problems and optimally uses hardware and software redundancy.

Brandenburg et al. [8] presented a case study which evaluates different real-time scheduling algorithms.

This paper is organized as followed. In Section 2 the principles of *cgroups* are introduced. Next in Section 3 the setup and results of the experiments are given. In Section 4 the results are discussed. Finally future work is indicated.

II. CGROUPS

Cgroups is a Linux kernel feature since version 2.6.24 and has had a major redesign since version 3.14. It allows to limit, prioritize and isolate CPU usage and other resources such as memory and I/O for a collection of processes.

A. CPUsets

CPUsets is a part of *cgroups* which maps processes to specific banks in memory or to a logical CPU or set of logical CPU's. They extend process scheduling with a set of hooks in order to manage dynamic process scheduling on multi-core systems.

CPUsets communicate through the file system rather than using system calls. A virtual file system is mounted in which a hierarchical system of *CPUsets* is described. *CPUsets* are hierarchical in two ways. A child spawned of a process in a CPUset, automatically belongs to that CPUset. Moreover, a child of a CPUset is limited to the resources assigned to its parent. When a CPUset consists only of resources which are exclusively assigned to it and its children, this CPUset is called an exclusive CPUset.

B. Scheduling

CPUsets extend the behavior of the scheduling system by a set of hooks, which manipulate process attributes such as affinity, real-time priority and the nice factor.

The load balancer is responsible for assigning processes to specific cores. Each process has an affinity attribute which binds the process to a specific queue of a core. Affinity is important to avoid trashing the cache by switching a process from one core to another all the time. When a specific process is isolated on a specific core, *CPUsets* manipulate all affinity attributes so that the load balancer assigns the specific process to the queue of the chosen core, while other processes are assigned to the queues of other cores.

The scheduler assigns time slices in a time window to the specific processes in its queue. It assigns a virtual runtime variable, which indicates how much of the processor time has been used by the process. As Linux employs a fair scheduler in the default scheduling policy, this means that the process with the lowest virtual runtime value has a higher priority. However there is the minimum granularity, which indicates the minimum time that is assigned to a process in the window regardless of its priority.

Setting the nice factor also changes the time which is assigned to a specific process. This attributes to a weight, which is relative to all the weights of all processes in the queue of the scheduler. Increasing the nice factor will result in a lower priority and vice versa.

Changing the real-time priority factor immediately interferes with scheduling the next process.

Finally, *CPUsets* do not guarantee exclusive access to the variables which manipulate priority of tasks. However if another system tries to manipulate priority while *CPUsets* are active, the system call is intercepted and an error is returned which indicates that *CPUsets* will maintain priority.

III. EXPERIMENTS

Four experiments are conducted in different scenarios. One experiment without process isolation and three experiments with isolation of a time-critical process from CPU bound processes in different configurations. The general setup of the experiments is shown in Figure 1.

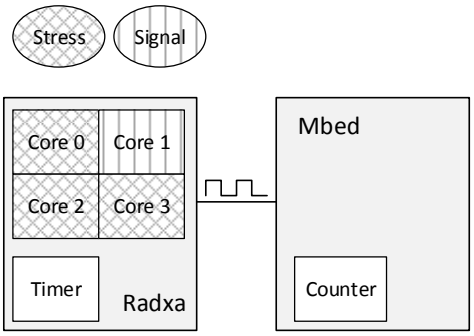

Fig. 1. Setup measurements of the time-critical signal

These have been conducted on the *Radxa Rock Pro* board which is built with the RK3188, a quad-core ARM Cortex-A9 processor [9]. This processor has a maximum clock frequency of 1.6GHz, all cores contain a L1 data and instruction cache of 32 KB and the processor has a shared 512 KB unified L2 cache. The board provides 2 GB of memory.

In our experiments we used a *Debian Wheezy* distribution based on the Linux 3.18 kernel. The *cgroup* package was obtained through the *aptitude* package manager.

The *Radxa* runs two programs. On the one hand, it generates a "time-critical" square wave signal with a period of 200 ms. This signal is generated through a real-time POSIX timer with a resolution of 1 ns. The timer runs asynchronously from the processor and notifies the timer trigger event to the handler process. On the other hand, the *Radxa* runs a CPU workload generator called *stress*, which spawns threads and waits for them to complete [10].

Each edge of the time-critical signal triggers the counter of an independent microcontroller, the *Mbed* LPC1768 [11]. The counter allows to measure the interval of the edges of the time-critical signal with resolution of 40 ns. This measurement is compared with the nominal value of 100 ms:

$$\Delta t_n = |t_n - t_{nominal}| \quad (1)$$

As the time-critical signal represents a task which needs to adhere to real-time constraints, values Δt_n larger than 0 represent the latency in scheduling that task. Variance in latency is expected as scheduling issues arise in the different scenarios.

In a real scenario real-time constraints are determined by the application, however in this case these are arbitrarily determined as follows. A context switch on this hardware is expected to take a couple of microseconds. When taking the extreme CPU-bound stress into account the range in which we want to observe variance is up to a factor 4 of a

normal context switch. Therefore in this case when jitter exceeds 15µs the value is considered as an extreme value.

In each scenario 2048 batches of 50 edges are counted. All data and artefacts of these experiments are available at *github* [12].

A. Baseline

In the baseline experiment no processes are isolated. In a first scenario no stress is applied. Figure 2 shows the discrete probability distribution function (pdf) of Δt.

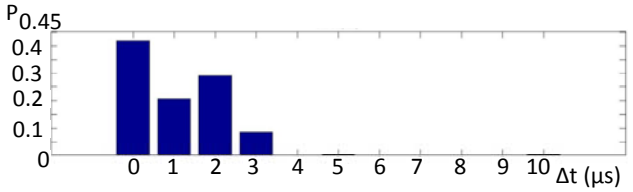

Fig. 2. No isolation, no stress: sample mean $\bar{y} = 0.0034\mu s$ and sample variance $\sigma_y^2 = 2.1461$

In a second scenario in the experiment without process isolation, CPU-bound stress is applied. I.e. 16 threads which executes an infinite loop calculating the square root of a single variable. The sample mean of Δt in this scenario is 327.5195 µs, a value larger than the period of the signal. This effect is due to extreme values in 26 of the 2048 samples, of which 14 are in the millisecond range. Figure 3 shows the discrete pdf of Δt smaller than 15 µs in this scenario.

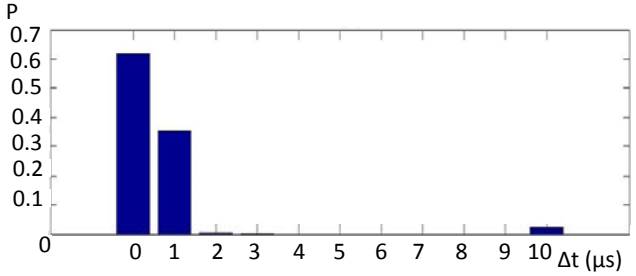

Fig. 3. No isolation, with CPU-bound stress, 16 threads, values of Δt < 15µs: $\bar{y} = 0.6048\mu s$ and $\sigma_y^2 = 0.2568$

B. Isolating core 1

In this experiment, core 1 is isolated in an exclusive CPUset and only the time-critical process is assigned to it. The other cores handle the 16 threads of the CPU intensive process. Figure 4 shows the discrete pdf of Δt in this scenario. There were no extreme values.

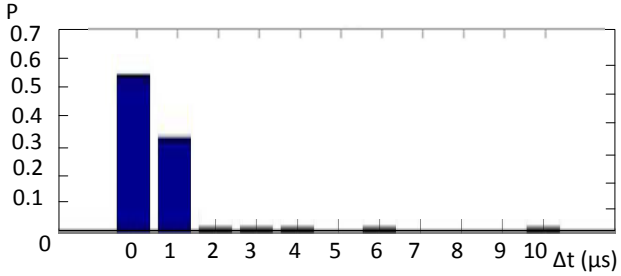

Fig. 4. Core 1 isolated, with CPU-bound stress, 16 threads, values of Δt: and $\sigma_y^2 = 0.2943$

C. Isolating core 0 and 1

This experiment isolates both core 0 and core 1in an exclusive CPUset with only the time-critical process assigned to it. Core 2 and 3 execute 16 threads of the CPU intensive process. Figure 5 shows the discrete pdf of Δt. There was a single extreme value (30µs).

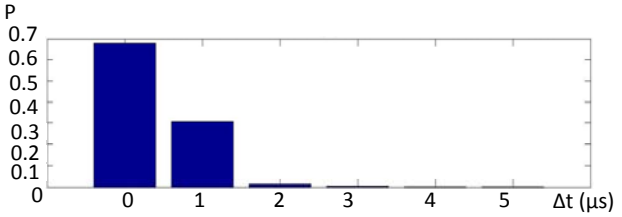

Fig. 5. Core 0 and 1 isolated, with CPU-bound stress, 16 threads, values of Δt < 15µs: and $\sigma_y^2 = 0.2523$

D. Isolating half of core 1

In the fourth experiment a timeshare equal to half of all time available on core 1 is attributed to the time-critical process. The other cores and remaining slots on core 1 are executing the stress process. In this scenario there are 503 extreme values larger than 100 µs with maximum values in the range of 10 ms.

IV. Discussion

When considering only time-critical processes which do not exceed a jitter of 15µs, the baseline experiment indicates a larger sample mean value and a smaller sample variance in the scenario with CPU-bound processes. In a standard configuration, process preemption allows scheduling in a deterministic fashion in almost 99% of the time. However depending on a situation where the time-critical task is interleaved and scheduled frequently, the expected jitter is unacceptable.

Isolating core 1 allows to fully utilize the other cores while isolating the time-critical process fully on a hardware level. Core 1 has been chosen as core 0 deals with OS related interrupts which might interfere with the time-critical process. However core 2 or 3 are equivalent in this respect. In this scenario, the sample mean is lower when compared to the baseline experiment with CPU-bound stress, while sample variance is higher. Nevertheless isolating core 1 prevents extreme jitter an indication that considering all sample values in this case accounts for the higher sample variance.

As core 0 shares memory caches with core 1, as well as deals with OS interrupts, the effect of isolating both cores considers a more prudent approach than isolating only a single core. Both sample mean and variance are lower, however a single extreme value has been measured. We conducted 6 additional experiments with 102 400 samples while isolating respectively core 1 and both core 1 and 0. These experiments indicated that extreme values occur in both scenarios once, never exceeding a maximum value of 30 µs.

The final experiment isolated half of the available time on core 1. This resulted in a considerable worse scenario

than the baseline experiment with CPU-bound stress or the other isolation experiments. This is due to the implementation of attributing time shares of the core to a specific process. Whereas isolation of a core is achieved by manipulating the load balancer, assigning half of the time is the responsibility of the scheduler. However the scheduler can only perform a context switch when a tick occurs. As the ticks have a period of 10 ms, any real-time system requiring jitter lower than this value cannot rely upon this feature of *cgroups*. In essence the granularity of time slices is too large to reliably schedule the time-critical process every 100 µs.

V. Future Work

In our experiments we applied a CPU-bound load in order to stress the OS and hardware system. However, CPU-bound congestion might not be the only cause of failing to meet real-time criteria. When the memory busses are saturated, the virtual memory system might fail to load the pages associated with the time-critical process, causing extra jitter. In a future experiment we will force a memory bus congestion and check the effect of process isolation on shared caches and main memory. Furthermore we can apply a combined set of processes, which induce CPU-bound as well as memory-bound stress.

Further, we might consider virtualization solutions for process isolation, like KVM and LXC. Virtualization is a technique popular in server environments, so the specific real-time constraints of an embedded system process need to be mapped onto these solutions. These techniques could be comparatively evaluated with *Cgroups*.

VI. Conclusion

In this paper we evaluated the performance of *cgroups* on a multi-core embedded system. *Cgroups* are used to isolate critical real-time processes under CPU-bound stress in a SMP architecture. They allow to define *CPUsets* which manipulate the load balancer and schedulers. In a configuration which isolates the real-time process to an exclusive CPUset we conclude that process isolation is effective and considerably reduces jitter when compared with a configuration without *cgroups* enabled. When the scheduler is manipulated, for instance when trying to assign half of a window of a CPU to the critical task, jitter increases immediately up to the size of a time slice.

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Integration of Soft Errors in Functional Safety: A Conceptual Study

Jens Vankeirsbilck, Hans Hallez and Jeroen Boydens

Abstract - **Embedded systems are used for both safety and non-safety critical applications. Safety critical systems must have a very low failure rate, as a failure can cause injury or even death. This paper presents soft errors as a cause for failure. Soft errors are systematic failures that lead to bit-flips in registers or other memory regions and affect the software in execution. The soft error and its detection techniques are linked to requirements imposed by the functional safety standards.**

Keywords – **Functional Safety, Soft Errors, Embedded Systems**

1. INTRODUCTION

Embedded systems are used more and more for different types of applications, e.g. brake-by-wire, video streaming, drones, etc. From a safety point of view, those applications can be divided into two categories: safety critical or non-safety critical applications. Safety critical systems are systems whose actions can decide over life, injury or even death. Non-safety critical systems are often infotainment systems.

A safety critical system, as any system, will fail once in a while. Such a failure can have many causes: a software bug, resistor short-circuit, rising temperature, etc. In this paper, the soft error is presented as a cause of failure. A soft error is a disturbance of hardware caused by external factors which affect the software in execution. These external factors can be radiation, fast temperature increase, etc. If the software is not aware of the occurrence of a soft error, the program memory can be corrupted leading to unstable behavior and unpredictable states. When using critical hardware components this can possibly lead to very dangerous situations.

The next two sections will discuss the two main domains of the research, respectively functional safety and soft errors. Then we will present some links between the two domains and use those links to join the domain of soft errors with that of functional safety. To conclude, future work is presented and conclusions are drawn.

II. FUNCTIONAL SAFETY

Embedded systems used as safety critical systems must comply with a functional safety standard, whose goal is to reduce the risk of physical injury or damage to health of people either directly or indirectly. This section will discuss the generic functional standard IEC 61508 and some differences made by more domain specific functional safety standards.

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2.1 Demystifying IEC 61508

The most generic functional safety standard is IEC 61508. As described by [1] and [2], it is an "umbrella" document covering multiple industries and applications. Its basic purpose is to create requirements intended to achieve reliable systems that either work properly or fail in a predictable manner. It is based on two concepts on which we will elaborate in the following sections:

- The Safety Life-Cycle, a detailed engineering design process which reduces failures due to systematic errors.
- The Safety Integrity Levels, quantified levels of failure rates.

2.1.1 Safety Life-Cycle

The Safety Life-Cycle is a model to eliminate systematic errors. IEC 61508 defines systematic errors as errors that lead to failures that are deterministically related to a certain cause. They are typically design mistakes. Software errors are considered systematic errors.

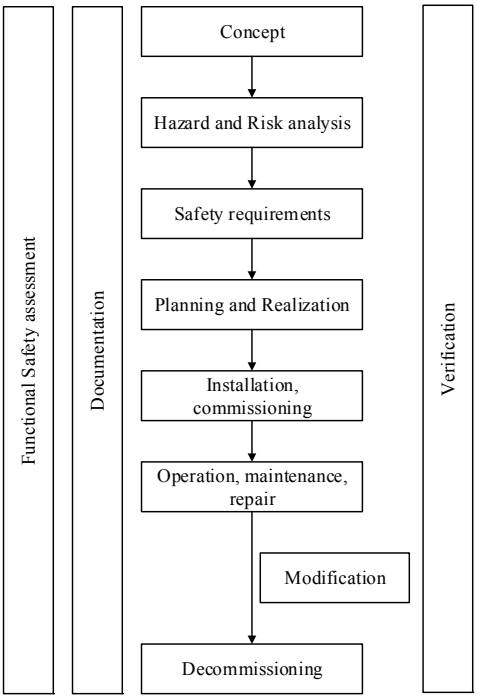

Fig. 1. Safety Life-Cycle

The Safety Life-Cycle addresses these errors by providing a classical, step-sequential waterfall engineering process. As Fig. 1 shows, it starts with the concept of the product and ends at its decommissioning. Each phase has to be documented and verified before moving to the next one.

2.1.2 Safety Integrity Level

Next to systematic failures, IEC 61508 also addresses random hardware failures. These are failures attributable to specific components and can be quantified. These quantifications result in a failure rate. The failure rates of components can be found in external or in-house failure rate databases or can be estimated using mathematical models. Once known, they help to predict the performance of the system.

IEC 61508 uses the concept of Safety Integrity Levels (SIL) to express excellence of the performance of components and the systems. The idea is to divide the "spectrum" of integrity into four discrete levels and then lay down requirements for each level. The higher the SIL, the more stringent the requirements. For IEC 61508 (and many other standards) the four levels are given in Table 1.

TABLE 1 SAFETY INTEGRITY LEVELS

SIL	High Demand (dangerous failures/hr)	Low Demand (PFD)
4	$\geq 10^{-9}$ to $< 10^{-8}$	$\geq 10^{-5}$ to $< 10^{-4}$
3	$\geq 10^{-8}$ to $< 10^{-7}$	$\geq 10^{-4}$ to $< 10^{-3}$
2	$\geq 10^{-7}$ to $< 10^{-6}$	$\geq 10^{-3}$ to $< 10^{-2}$
1	$\geq 10^{-6}$ to $< 10^{-5}$	$\geq 10^{-2}$ to $< 10^{-1}$

A distinction between high demand and low demand systems must be made. For high demand systems, e.g. car brakes, it is necessary to know the failure rate per hour since there is a high probability of suffering the hazard immediately each failure occurs. High demand systems are defined as systems that are used more than once per year. Low demand systems are used less than once per year. For low demand systems the failure rate alone is of little use since the hazard is not incurred immediately each failure occurs. The demand of the system is infrequent, so failures may well be dormant. Therefore low demand systems are characterized using the probability of failure on demand (PFD), it is necessary to know the chance of failure when you actually need the system.

2.2 Specific Industries

To compensate the generic character of IEC 61508, many industry domains have created their own functional safety standard, starting from IEC 61508.

- Medical: the medical domain has a general functional safety standard: IEC 60601 [3], which describes all requirements to build a complete medical system. Recently, IEC 62304 has emerged as a standard to describe the software development processes for medical systems. A difference between IEC 61508 and IEC 60601 is that IEC 60601 does not use SIL to categorize different medical systems.
- Railway: the railway domain has three standards, EN 50126 which describes Reliability, Availability, Maintainability and Safety; EN 50128 [4] describes the software development processes; and EN 50129 describes System Safety. A difference between the EN 5012X and IEC 61508 is the introduction of Software Safety Integrity Levels (SSIL) by the EN 5012X series.

III. SOFT ERRORS

This section discusses the second domain of our research: the soft error. First the main causes of the soft error are presented and secondly the possible effects of a soft error on the embedded system are listed.

3.1 Cause

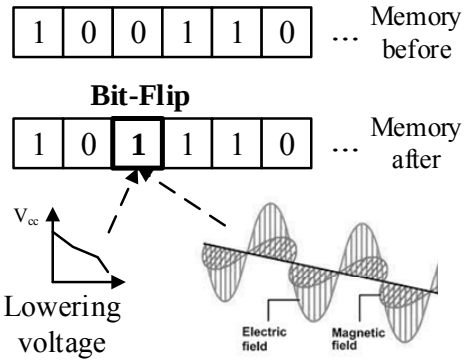

Fig. 2. Cause and Effect of a Soft Error

Fig. 2 depicts the two main causes of soft errors: the manufacturers, symbolized by the graph 'lowering the supply voltage', and the work environment, symbolized by the electromagnetic wave.

One cause of a soft error is the current trend followed by manufacturers. To satisfy their customers, manufacturers of embedded systems or components used by embedded systems have decreased the supply voltage, decreased the size… of those systems. While this has many advantages, e.g. increased battery lifetime, increased transistor density so the same die area can house more computing power… it also has one big disadvantage: the devices are now much more susceptible to soft errors.

Another cause of soft errors is the work environment of the embedded system, which is nowadays filled with radiation emitted from other electrical appliances, WiFi hotspots, natural background radiation, contaminated packaging, etc.

The radiation leads to highly energized particles that can pass through the embedded system, affecting its hardware. As described by Baumann [5], the passing particle can create a short pulse which can flip a transistor from open to close or vice versa. Due to the decreasing scale and supply voltage of the embedded system, the energy needed by the particle to flip the transistor has decreased, leading to a higher occurrence of soft errors.

3.2 Effects

Fig. 2 shows the primary result of a soft error: a bit of a memory location is flipped. That faulty bit does not necessarily have an effect on the system.

Fig. 3 is a simplified adaptation of the flowchart provided by Mukherjee [6] and shows how certain conditions have to hold before the bit-flip affects the system or the software in execution.

The first condition is that the faulty bit has to be read. Since soft errors are transient errors, overwriting the bit will discard the previous value, masking the bit-flip.

Secondly the bit has to be an Architectural Correct Execution or ACE bit. An ACE bit is a bit necessary for correct execution, e.g. a bit from the program counter. If a bit is un-ACE, thus unnecessary for correct execution, it cannot affect the system or software. An example of an un-ACE bit is a bit of the branch predictor. A branch predictor is a structure that tries to predict which branch has to be taken based on previous decisions. If a bit is flipped in this structure, or any other prediction structure, the performance of the system may be affected, but it will not affect correct execution.

If both conditions hold, the faulty bit is read and it is an ACE bit, the bit-flip will affect the software in execution. The effect on the software largely depends on the location of the bit-flip: Main Memory, General Purpose Register, Program Counter or Stack Pointer. Generally speaking, the effects can be divided into two categories:

- Data flow corruption, leading to wrong intermediary and output values.
- Control flow corruption, affecting the execution order of the instructions. A control flow error leads to a jump to unintended instruction.

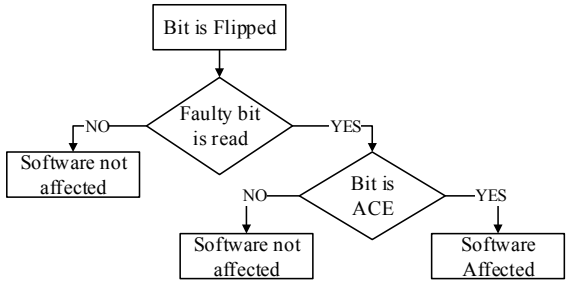

Fig. 3. Simplified flowchart to determine if the Bit-flip will affect the software.

Embedded systems are often used to control parts of its environment, an actuator, a servomotor... through I/O. This I/O is often memory mapped in the Main Memory of the embedded system. A bit-flip affecting a memory mapped I/O register may not affect the software in execution, but can affect the environment, e.g. controlling an actuator when it is actually prohibited. This can create very dangerous situations!

IV. INTEGRATION

To be able to join soft errors and functional safety, soft errors must be classified as systematic or random hardware failure. The failure to take into account is not the failure of the software, but the bit-flip since the software only fails due to the occurrence of a bit-flip.

To be able to classify the bit-flip, we took a look at the definitions for the failures given by IEC 61508:

- A systematic failure is a failure related in a deterministic way to a certain cause, which can only be eliminated by a modification of the design or of the manufacturing process, operational procedures or other relevant factors.
- A random hardware failure is a failure occurring at a random time, which results from one or more degradation mechanisms.

By analyzing the definitions, we conclude that a soft error is a systematic error. The bit-flip can always be traced back to a certain cause, be it e.g. EMI or rising temperature, and it can only be eliminated by a design modification.

4.1 Reducing the failure rate

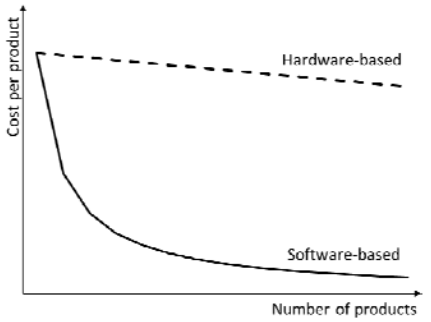

Fig. 5. Cost of soft error detection and recovery

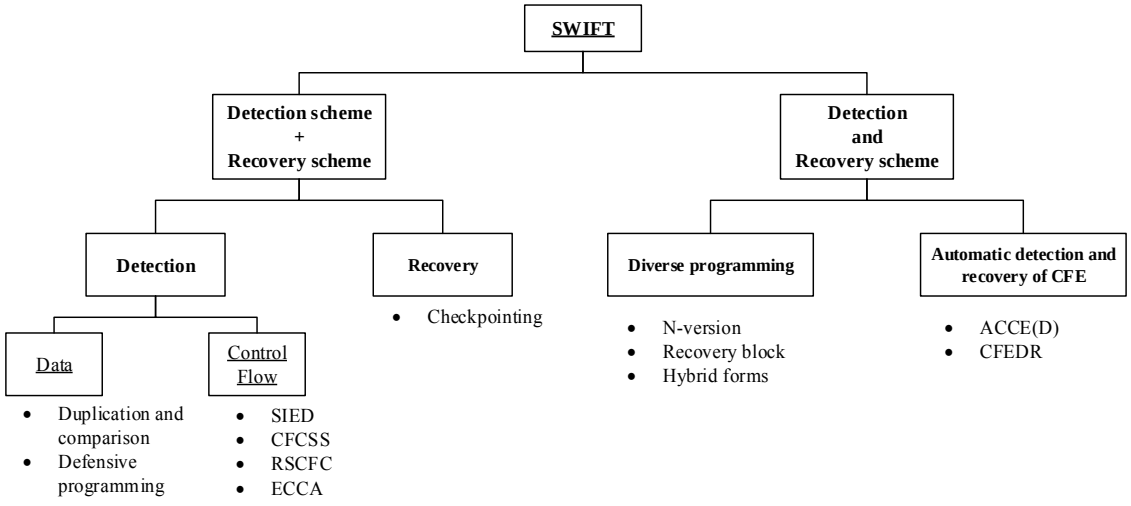

Fig. 4. Software implemented fault tolerance techniques

Functional safety is about reducing the risk of system failure. Soft Errors play a role in the failure rate of the device, so detecting and recovering from them will reduce the rate. Adding a detection and recovery technique reduces the number of soft errors that have an effect on the software, resulting in a reduced failure rate for the system.

Detecting and recovering from soft errors can be hardware-based or software-based. As Fig. 5 shows, detecting soft errors through software is more cost efficient. Hardware-based means adding components, e.g. a shield, to the PCB, which means this must be added for each product. This represents a nearly constant cost per product. Software-based detection techniques represent a high cost at development time, but once the software is completed it can be applied to each product, lowering the cost significantly for each product sold. Therefore future research will focus on software implemented detection and recovery techniques.

A second reason to focus on software implemented techniques is to ease compliance with functional safety standards. IEC 61508 states that: System software should include software for diagnosing faults in the system hardware, error detection for communication links and online detection of the application of software modules. The software in execution should be tested for control and data flow. Since data and control flow corruption are effects of a soft error, adding a software implemented detection and recovery technique ensures those corruptions are detected, and thus helps compliance with IEC 61508.

V. Future Work

Future research will focus on software implemented detection and recovery techniques or software implemented fault tolerance (SWIFT). Fig. 4 gives an overview of existing SWIFT techniques. The techniques have been grouped by their ability. The left group of techniques all have their specific function, e.g. SIED is meant to detect control flow errors and duplication is used to detect data flow errors. The right group of techniques detect and recover from the effects of the soft error, e.g. the diverse programming techniques use multiple versions of the program and a voter to decide on the correct result, masking the effect of the soft error.

First we will further complete the list by performing a literature study.

Once the list of existing SWIFT techniques is more or less complete, research will focus on implementing the techniques while complying with the rules of functional safety. Although soft errors and its detection techniques can theoretically be joined with functional safety, research will have to determine if this can be translated in practice. Software implemented techniques must comply with the software rules imposed by functional safety. Functional safety standards demand the use of a programming language subset, to force the programming language to be fully and unambiguously defined. Moreover, the standards demand the use of a coding standard and demand the limitation of certain programming constructs, e.g. pointers. These rules could make it impossible or very hard to implement existing soft error detection and recovery techniques.

VI. Conclusion

This paper discussed how to join the domain of functional safety and soft errors. This is done by proving that a soft error is a systematic error and can only be eliminated by a design modification.

The two domains are also joined since adding a soft error detection and recovery technique helps comply with IEC 61508, the most generic functional safety standard. IEC 61508 states that the system software should have diagnostics to be able to detect malfunction. Soft error detection techniques are in fact diagnostic techniques, so compliance with the standard is eased by implementing a detection technique.

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Mains Frequency Deviation Measurement by Using Elements of the Subtraction Procedure Based on Xilinx FPGA

Dimiter Hristov Badarov and Georgy Slavchev Mihov

Abstract -**The subject of the article is an application of a programmable logic devices from the FPGA XILINX family and elements of the subtraction procedurefor the power-line frequency deviation measurement. The synthesized structural diagram includes programmable input attenuator, input stage, analog-to-digital converter, SPI interface unit, CPU core and LCD display. The mains frequency deviation measurement is performed by the soft CPU core implemented in the FPGA. Software algorithms for 'two point' averaging digital filtering and calculation of the mains frequency deviation are developed which minimizes the usage of FPGA resources.**

Keywords– **Frequency Measurement,Mains Frequency, FPGA, Deviation Measurement, Two Point Averaging, FIR Filter, Subtraction Procedure.**

I. INTRODUCTION

The frequency of the utility grid is maintained in tight interval by precisely balancing the amounts of generated and consumed power. For this purpose a high precision measurement of the mains frequency is needed.Typically this is done by direct measurement of the period of the mains voltage and calculating its frequency [1]. The method requires 'direct' signal from the mains. Sometimes in data acquisition systems we need to know the deviation of the mains frequency from its nominal value but cannot use 'direct' mains signal [2]. For this purpose the frequency deviation measurement using the 'two point' FIR digital filter is developed. It offers significant advantages over the classical direct period measurement method:

– does not need a 'direct' signal from the mains

– low sampling rate (200*Hz*) is enough for fast, high accuracy measurement

– does not need dedicated input for the frequency deviation measurement (the 'parasitically' induced hum can be used)

The frequency deviation measurement is implemented on a FPGA (Field-Programmable Gate Array) integrated circuit of Xilinx Spartan-3E family.

The FPGA logic devices are used to implement any logical function.

A Hardware Description Language (HDL) or logical diagrams are used for configuring of the FPGA.

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II. STRUCTURE OF THE MAINS FREQUENCY DEVIATION METER

The structural diagram of the mains frequency deviation meteris represented on Fig. 1. The mains signal is first fed to the input of the programmable attenuator. The right attenuation is chosen so that the signal always remains within the dynamic range of the following stages [5]. Then the signal is fed to the amplifier-limiter where it is buffered and level shifted to the half of the input dynamic range of the ADC (Analog to Digital Converter). Then the signal is fed to the input of the 12-bit ADC. The digital information from the ADC is transferred to the FPGA via SPI interface. All further signal processing is carried by the microprocessor core implemented into the FPGA [6].There is 12-bit RAM (Random Access Memory) implemented into the FPGA [6]. The data from the ADC is stored into the RAM memory during the processing. The results from the calculations are visualized on the LCD display.

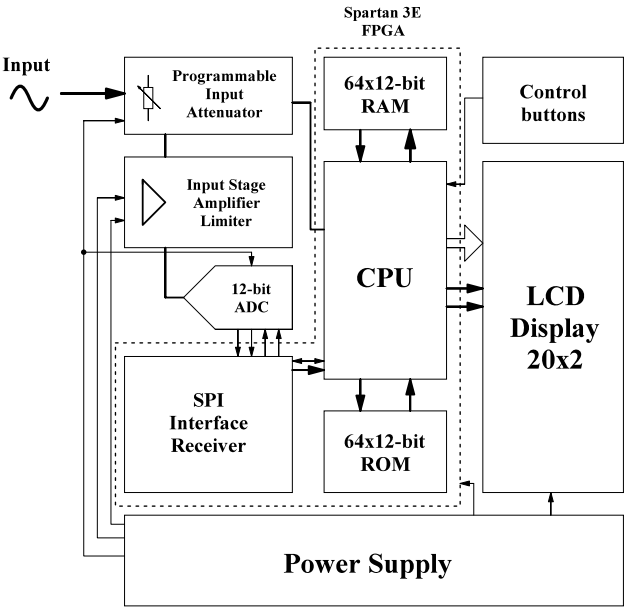

Fig. 1. Multifunctional analyser structural diagram

III. INPUT STAGE

The circuit diagram of the input stage is represented on Fig. 2. The first stage is the input attenuator which is a resistive voltage divider. The attenuation is programmed by switching the resistance to ground by reed relays. There are three different attenuations possible: 1:1; 10:1 and 100:1. The next stage is a non-inverting voltage follower built with the Texas Instruments operational amplifier NE5534.

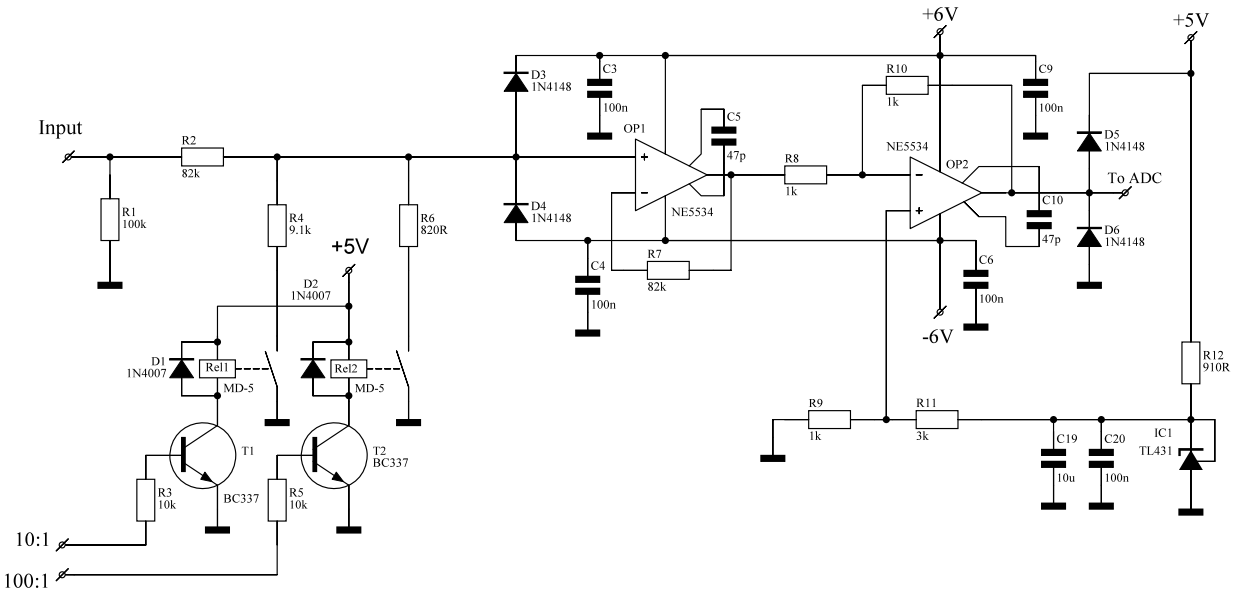

Fig. 2. Input stage schematic diagram

This stage matches the relatively high output impedance of the attenuator with the lower impedance of the next stage. There is a diode limiter at the input of the amplifier for overvoltage protection. The next stage is an inverting amplifier and level shifter. It's function is to shift the level of the signal to the half of the dynamic range of the ADC. This is needed because of the single polarity input range of the ADC. D5 and D6 are overvoltage protection for the ADC input. The bipolar power supply for the operational amplifiers is built with the AIMTEC AM1D-0512DZ DC-DC converter.

IV. Frequency Deviation Measurement Algorithm

The signal samples from the ADC are sent to the FPGA where the microprocessor is performing the software processing. For the purposes of the frequency deviation measurement a 'two point' FIR filter is implemented [3][7]. This is a truncated filter which is performing averaging over two data points in the measured signal period [4]. Its working principle is given by the Eq. (1):

$$Y_i = \frac{X_{i-n/4} + X_{i+n/4}}{2}, \qquad (1)$$

where X_i stands for input samples, Y_i stands for filtered samples, n is the ratio between the sampling rate Φ and the mains frequency F ($n = \Phi/F$).

The value of $n/4$ must be an integer number. That is why a $\Phi = 200$ *Hz* sampling rate is chosen. This is the lowest frequency which is exact multiple of $F = 50$ *Hz* and satisfies the upper condition with its minimal integer value of 1.

The frequency response of the filter is a cosine function with coefficient of 1 for the frequencies $f = 0$ and 0 for the mains frequency $f = F$ (see Eq. 2)

$$K(f) = \cos\frac{\pi n f}{2\Phi}. \qquad (2)$$

The impulse response with the frequency and phase responses of the 'two point' filter are represented on Fig. 3.

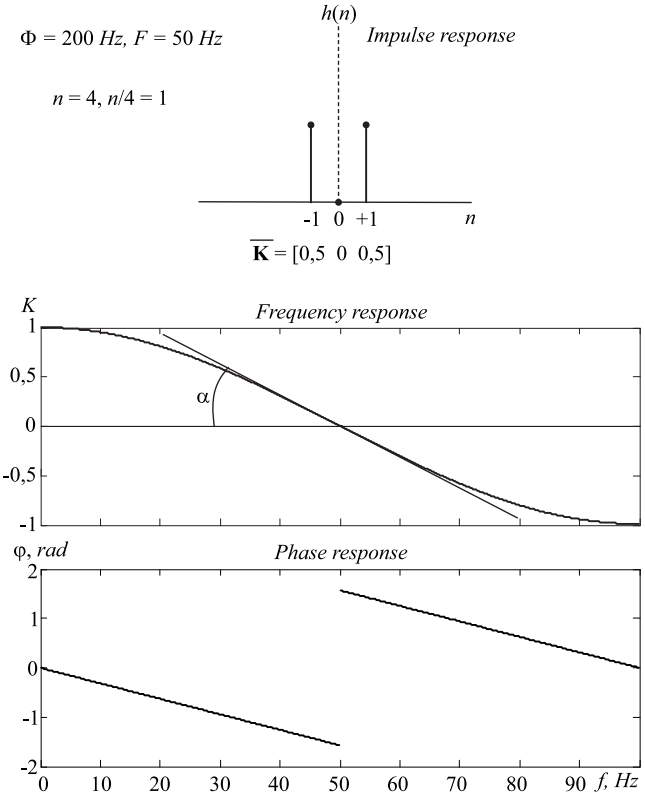

Fig. 3. Filter impulse, frequency and phase responses

For small frequency deviations the transfer function can be approximated according to the formula

$$\frac{\Delta K}{\Delta f} = \tan\alpha. \qquad (3)$$

The usage of 'two point' filter for mains frequency deviation measurement has several major advantages over the rest of the filters:

– simplified calculations are reducing the processor speed needed for real time operation;
– the transfer function of the filter crosses steeply the *x* axis at 50 *Hz* this leads to better sensitivity of the frequency deviation measurement;
– the transfer function crosses the *x* axis symmetrically which reduces the measurement error and it is equivalent for positive and negative frequency deviations.

For the chosen sampling rate Φ = 200 *Hz* the equations are significantly simplified.The current output sample is calculated by

$$Y_i = \frac{X_{i-1} + X_{i+1}}{2}. \quad (4)$$

The difference between the current output sample and the corresponding input sample represent samples B_i of the power-line signal. It is calculated by

$$B_i = X_i - Y_i, \quad (5)$$

and stored into a temporary buffer.
The frequency deviation is calculated using the formula

$$\Delta f \approx -K(f)\frac{\Phi}{2\pi}, \quad (6)$$

where$K(f)$ is given by

$$K(f) = \frac{B_i - B_{i-4}}{2(B_{i-1} - B_{i-3})}. \quad (7)$$

Using these equations the deviation of the mains frequency can be calculated fast and easily.

V. Experimental Results

The input stage testing is performed with PC with a 16-bit 192kHz sampling rate sound card and installed Right Mark Audio Analyzer software. The software performs automatic measurement of various parameters of an audio system. It generates testing signals which are fed from the Line-out of the sound card to the tested circuitry. Then the signal from the output of the tested circuitry is fed back to the sound card Line-in input.

The following parameters are tested: frequency response, noise level, dynamic range, THD + noise, intermodulation distortion and crosstalk between channels.

The testing shows a frequency response from DC to 40 kHz ±0.25 dB (Fig. 4), noise level below -70 dB, THD lower than 0.04% (Fig. 5), inter modulation distortion lower than 0.2 % in the whole spectrum from 1 kHz to 50 kHz and inter-channel crosstalk about -42 dB.

The measurement of the mains frequency deviation using the ‘two point’ FIR filter is showing good results with high accuracy. The required processing speed for a real time operation is small. The algorithm is tested in MATLAB and the results are represented on figure 6, 7 and 9. The real frequency of the test signal is represented by the red graph, and the measured frequency with the ‘two point’ filter method is represented by the black graph. The two graphs are closely matching and for that reason for better visibility they are slightly misaligned.

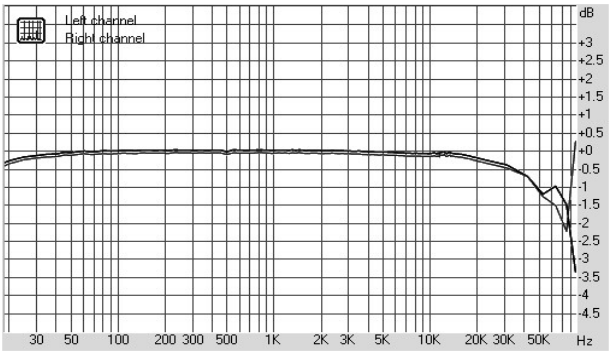

Fig. 4.Input stage frequency response

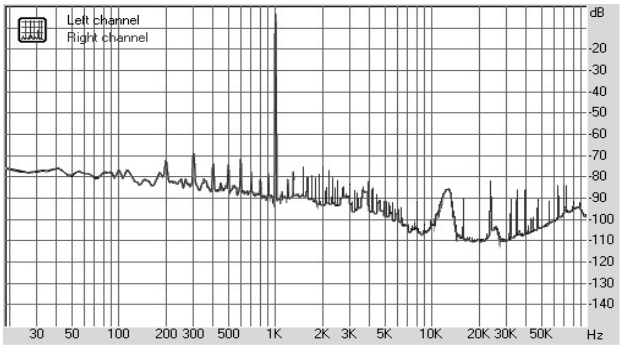

Fig. 5.Input stage spectrum of the output signal with 1 kHz sine wave test signal

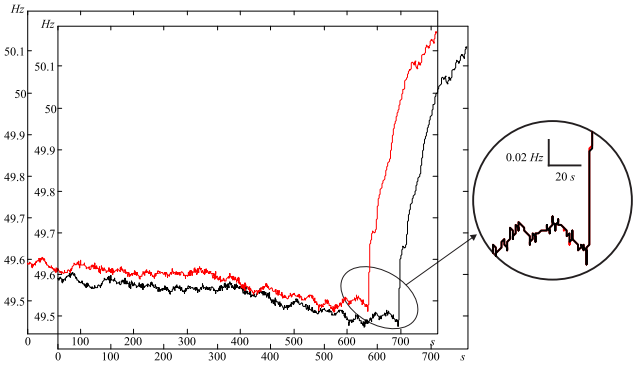

Fig. 6.The actual mains frequency and the measured frequency

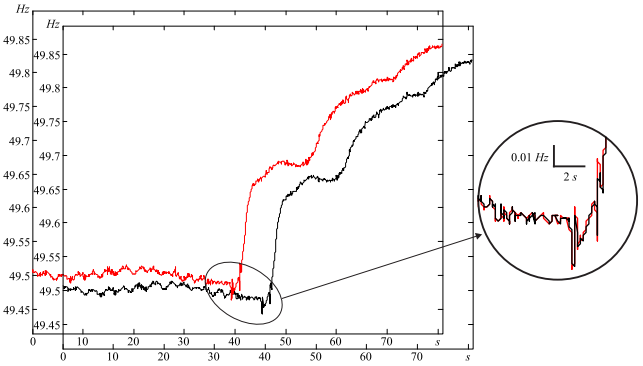

Fig. 7. The actual mains frequency and the measured frequency

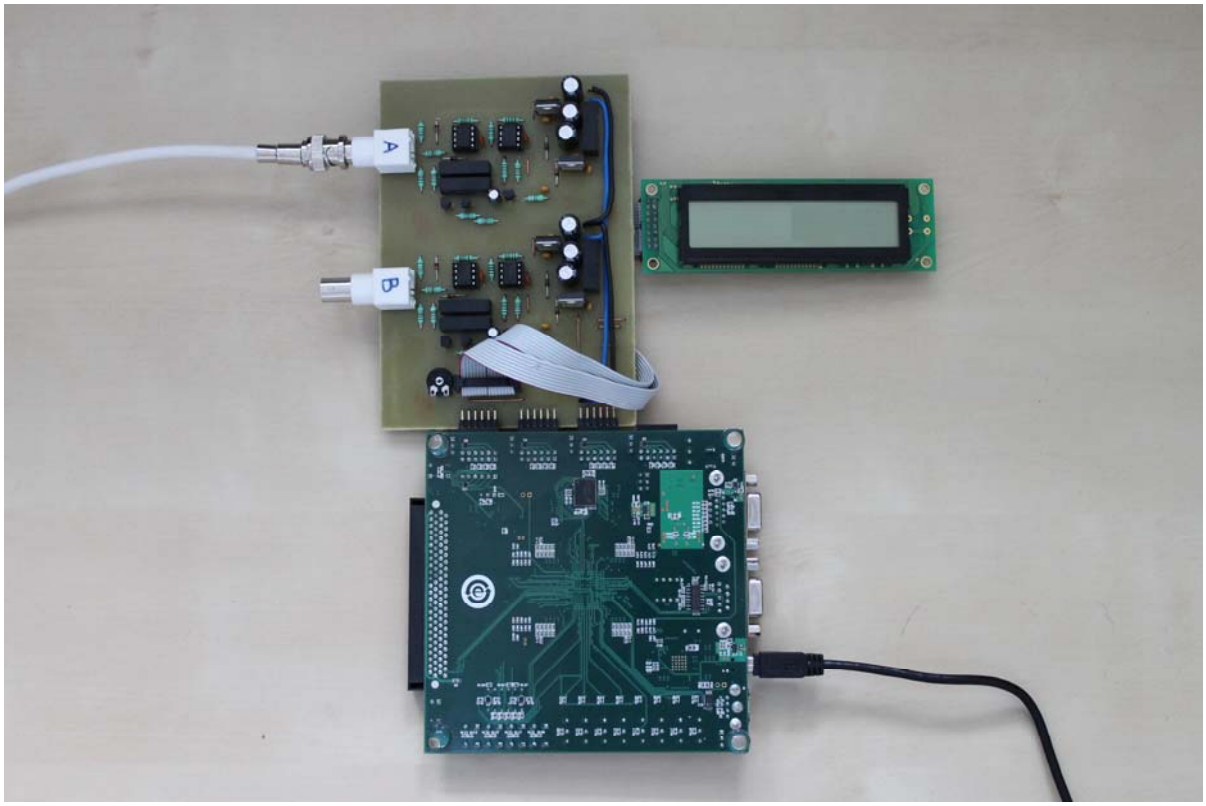

Fig. 8.Developed board with input attenuators, input stages, power supply, ADC and LCD display

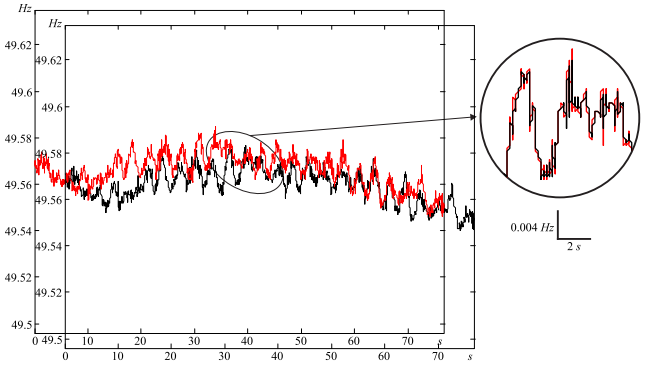

Fig. 9. The actual mains frequency and the measured frequency

VI. Conclusion

The results from the input stage testing are showing good flat frequency response.

The noise level of -70 dB is low enough to prove the concept but a good point for development is lowering the noise floor up to at least a –100 dB. This can be achieved by using resonant DC-DC converters for power supply, as well as using a lower noise operational amplifiers.

The 'two point'filter method for mains frequency deviation is showing good accuracy over a wide range of mains interference amplitudes. This makes it possible to implement the method in different embedded systems where the exact mains frequency is important to be known. It can be used in further signal processing for mains interference suppression.

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Realization of a Home Automation Network with Two Gateways Based on Open Source Hardware

Galidiya Ivanova Petrova, Grisha Valentinov Spasov and Georgi Aleksandrov Pazhev

Abstract – **The paper presents a realization of a home automation network with two wireless gateways based on open source hardware. Many of the home automation networks consist of a PC based machine (working as a gateway), a wireless network of sensors, smart systems for metering of water, electricity and gas consumption, actuators for heating, ventilation and air-conditioning (HVAC) and wireless alarm systems. The advantages of the proposed approach are the low cost, additional functionality and scalability together with better sustainability toward power supply disturbances. The described home automation network is based on microcontroller Olinuxino A13 with installed Android 4.0 operating system, used as Internet gateway, and microcontroller Olimexino 328 used as wireless sensor gateway. The communication inside the network is based on CNDEP protocol. A new adapted version of the communication protocol CNDEP, initially designed for data exchange in distributed embedded systems, is described.**

Keywords – **Smart home, Home automation network, Open source hardware, Bluetooth wireless gateway, Olimexino, Android, CNDEP protocol.**

I. INTRODUCTION

As stated in [1] the primary objectives of a smart home are to increase home automation, facilitate energy management, and reduce environmental emissions. A smart home is a residence equipped with a communications network, linking sensors, domestic appliances, and devices, that can be remotely monitored, accessed or controlled [2].

As defined in [3] the home automation is the residential extension of building automation. Home automation systems are used for monitoring and control applications for home user comfort, efficient energy management and security. These automation systems may span a variety of different networks including various sensor networks, smart systems for metering of water, electricity and gas consumption, networks for control of home environment as heating, ventilation and air-conditioning (HVAC) systems, and alarm systems networks. In general case, to handle interconnections between these networks gateways are needed.

Usually, the binding in heterogeneous networks use gateways in order to provide transparent operation of applications [4]. In this approach the gateways must implement the functionality of the protocol stacks of the networks which they connect. Traditionally, this is achieved with one of the controllers or workstations in the network. From one side, it connects a home automation network to Internet and plays the role of Internet portal, and from the other side it realizes the interfaces and protocol interactions to corresponding sensors, metering systems, actuators and alarm systems.

The alternative approach is to distribute the functionalities in two or three layers employing hierarchical structure. The first layer comprises the sensor networks with corresponding sensor gateways where the data and protocols are converted to the common format. By means of Internet gateway the second layer provides all the Internet functionalities and corresponding applications. The Internet gateway plays the role of server in the interaction with the third layer. The third layer usually is represented by Internet portals of smart grid energy control centers, security providers, central heating systems, etc.

Considering the home automation systems this approach is more perspective for future development as it allows easy integration of different types of sensor networks to the existing solutions. The advantage of such an open platform concerning the scalability of the system is obvious.

However, the implementation of a smart home system at the moment is affordable for limited group of users due to the costs associated with the purchase of smart appliances, metering systems, monitors, devices, along with installation and support services. Focusing on energy consumption and management services, high costs of the necessary technologies and difficult user interfaces are highlighted as key barriers in the literature [2] for wider spreading.

The aim of this paper is to present a realization of home area networks (HANs) and automation system for a smart home based on hierarchical structure employing low cost open source hardware and software platforms.

II. INITIAL REALIZATION OF SENSOR NETWORKS

One possible low cost solution for implementation of sensor gateway in wireless sensor networks is the employment of open source hardware platform Arduino and integrated Bluetooth module. In realization of the experimental sensor network the Arduino-compatible platform Olimexino 328 is used [5]. It consists of a 8 bites microcontroller ATmega 328 with built-in temperature sensor, 8 analog inputs, 14 programmable digital inputs (or outputs) and USB interface for connecting with a PC. The digital inputs/outputs could be programmed to realize 1-wire, I^2C and UART digital interfaces. The USB interface is used for programming the microcontroller. In addition, it

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works as a virtual RS232 interface, so it could be used for data exchange with a PC, which does not support this physical interface.

The initial realization of experimental sensor networks is shown on Figure 1. They are based on three different physical interfaces - I^2C and 1-wire for indoors temperature measurement and UART for energy consumption measurement.

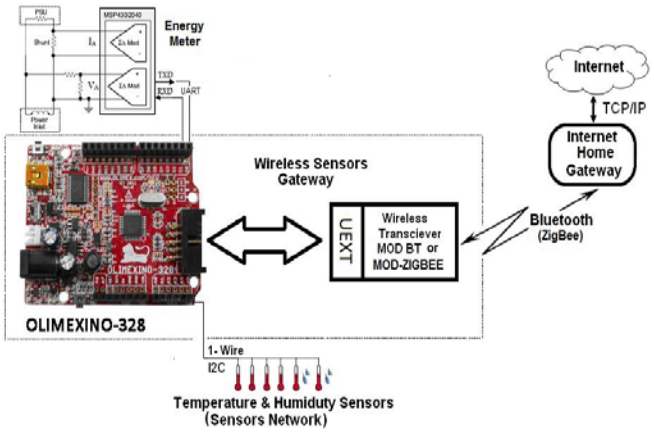

Fig. 1. Initial realizations of experimental sensor networks

For measurement of the temperature TCN75A from Microchip and DS18B20 from MAXIM sensors are used, while for energy metering the Microchip MCP39F501 Power Monitor PICtail module is connected to Olimexino 328 microcontroller. The wireless sensor gateway is realized by a Bluetooth transceiver (MOD-BT) connected to the UEXT interface of Olimexino 328. It is connected to the Internet gateway (gateway to the Internet-based network) realized with an industrial PC [6]. The applications for home monitoring and control of home environment devices are running on the Internet gateway.

III. Realization of Home Automation Network

The realization of the home automation network is based on the developed wireless sensor networks but instead of using industrial PC, the Internet gateway is realized with the open hardware platform OlinuXino – A13 WiFi, which is a low cost, very compact single board Linux computer with embedded WiFi [7]. Its features 32 bites CPU ARM9-Cortex-A8, working on 1GHz clock and very low power consumption, embedded WLAN WiFi, and easy integration of Bluetooth and Zigbee interfaces through UEXT connector and LAN ETHERNET through USB, makes it very good choice for implementation as Internet gateway. The power supply for OlinuXino – A13 WiFi is optional - with power supply adapter or autonomous with rechargeable Li-Po battery, which assures better sustainability toward power supply disturbances at low cost. The platform is working with LINUX-based Operating system Android 4.0. Although both Linux platforms Ubuntu and Android 4.0 are recommended by the producer of OlinuXino – A13 WiFi [7], Android 4.0 has been preferred due to the option to use Android SDK Tools for future Cloud applications based on Google Cloud Platforms.

The implementation of a home automation network with OlinuXino - A13 WiFi as Internet Gateway and one wireless sensor gateway is presented on Figure 2. The proposed solution allows easy integration of up to seven wireless gateways through Bluetooth interface to one Internet gateway, thus improving the scalability of the system. The different types of sensors, for example to measure humidity, to detect fire or gas leakage, additional alarm detectors for indoors presence of a human or an animal, and for notification of the presence of unwanted objects could be easily connected to the existing solution. This is an essential advantage of such an open platform.

Through WiFi WLAN a Smart phone or PDA device is connected to the Internet gateway. The Smart phone is used for local monitoring of the system parameters, the initialization of sensors' and alarms' modes, as well for the integration of new sensor types to the home automation network.

The connection of the Internet gateway to the Smart grid of energy control centers, security providers and central heating systems from the third layer of the hierarchical structure is realized through Internet by means of LAN ETHERNET or WiFi.

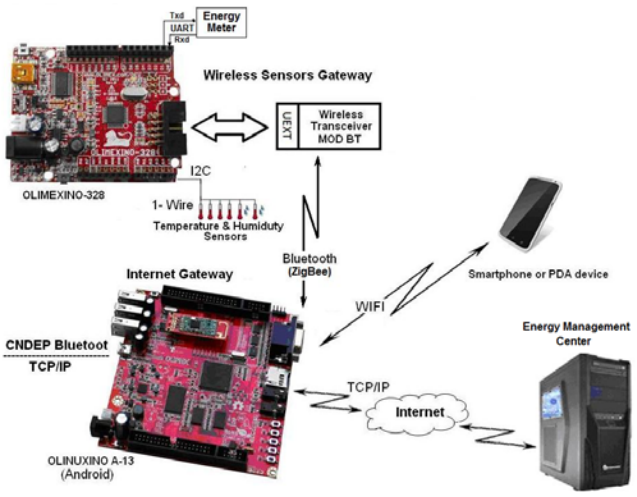

Fig. 2. The implementation of a home automation network with OlinuXino - A13 WiFi as Internet Gateway and wireless sensors gateway.

Although the Internet gateway could be realized using Olimexino 328 with added Ethernet and WiFi shields, and Bluetooth module (MOD-BT), the realization with OlinuXino – A13 WiFi has been preferred due to the easier integration to the third layer. With Olimexino 328 the integration to the third layer is possible by means of simple Web server [8], which makes more difficult the employment of SOA or RESTful web service technology. The prices for both platforms are comparable but the additional advantage of OlinuXino – A13 WiFi working with Android OS concerning the possibility to use multi-treat applications is also taken into consideration.

IV. Description of CNDEP Protocol

The communication protocol CNDEP is initially designed for data exchange in Internet-based distributed embedded systems [9]. There are three available versions

of this protocol at the moment: CNDEP – TCP/IP, CNDEP – 485 and CNDEP - Bluetooth. The basic version is CNDEP – TCP/IP. The other two versions are implemented in particular applications as sensor networks based on interface RS-485 or physical layer RS-Bluetooth [6]. Since CNDEP is intended for use in networks of controllers connected to a LAN (Ethernet, WiFi) and applications based on the TCP/IP protocol stack, the utilization of Bluetooth interface requires several changes in the basic protocol. The CNDEP-Bluetooth protocol version is adapted for applications where the data have to be exchanged between wireless sensor gateways and the Internet gateway. First, the Internet gateway sets the initial configuration parameters (default settings) of the sensors in the sensor networks. Then, in the monitoring mode the exchange of data generated in the sensor nodes is initiated by the sensor gateway (Olimexino-328). When it is necessary the default settings of sensor parameters could be changed by the Internet gateway submitting commands across the network. The communication protocol CNDEP is adapted for implementation in the home automation network and several extensions are added. For example, there are one extension for configuration of new sensors connected to the sensor gateway and another extension for self-identification from the client part.

The message formats are presented in Figure 3. There are two types of packets: packet for sending commands (request) and packet for sending a reply (response). Both begin with ASCII character STX (Start of Text) and end with character ETX (End of Text).

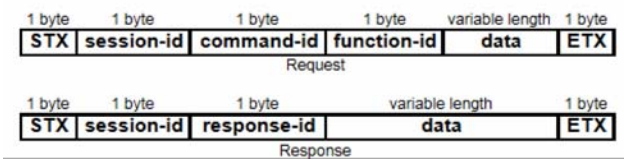

Fig. 3. Message formats

After the start symbol a field session-id follows, which is used to identify a session in case of re-transmission. The field command-id is used to represent the command to the corresponding sensor note. There are 5 types of commands used: TEST, GET, SET, CONFIG and SSID.

- TEST command is used for testing the connection between the Internet gateway and the corresponding sensor nodes through the sensor gateway;
- GET command is used when the Internet gateway requests data through the sensor gateway from a particular sensor node;
- SET command is used for sending the settings of parameters for sensors and actuator nodes;
- CONFIG command is used for sending meta-data which describe new sensors attached to the sensor networks, and definitions of their corresponding functions for execution of the commands SET and GET;
- SSID command is used for setting up the session identifier from the client-side.

In the function-id field the type of parameter to be measured is specified, which determines the corresponding sensors for data extraction. Also some additional options concerning the measurement procedure could be set. In the packets for sending commands (request) the data field contains the arguments of the commands, while in the packets for sending reply (response) this field contains the data extracted from the sensors. In the response-id field the type of response, sent from the sensor gateway is determined. The possible types of responses are: error, OK and data transfer.

The CNDEP is asymmetric protocol from the type client-server. The server scenario in the home automation network is realized from the sensor gateway in the request/response interactions. The server side decodes the received request from the client (Internet gateway in this case), performs the command, generates and sends the corresponding response. The working state diagram on the server side is presented on Figure 4. A new state (Save) in the execution of the commands CONFIG and SSID is added. This was done with the aim to add the security policy with interaction type 'Resurrecting Duckling'[10], which provides additional mechnisms for defence against external intrusion through wiress interfaces in the home automation network.

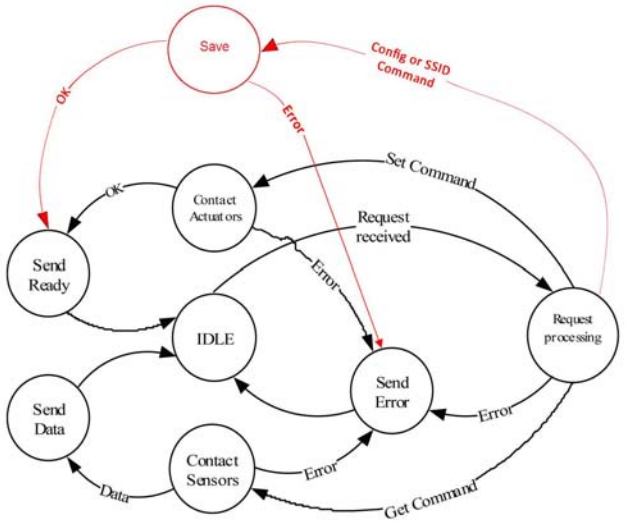

Fig. 4. Working state diagram on the server side

The sensor gateways are configured by the end user of the home automation network depending on the sensors attached to them. The Internet gateway sends configuration message (message with CONFIG command) to the corresponding sensor gateway to set the description of SET and GET functions. The function description consists of basic microinstructions that are supported by each gateway - commands for reading and sending data through interfaces 1-wire, I^2C, UART; commands for reading data from analog sensors and commands for control of the actuators via GPIO (General Purpose Input / Output) interface.

The functional diagram of the application for interaction of the Internet gateway (OlinuXino - A13 WiFi platform) with the sensor gateways is presented on Figure 5. The application comprises three processes (activities), one

service, one integrated database and two broadcast receivers. The 'Configure Gateways' activity is used for adding the definitions of the functions to the corresponding sensor gateway. These definitions are stored in the database and they are sent as CONFIG messages to the sensor gateway. The 'Configure Internet Gateway' activity is used for constructing and adding rules for data extraction (rules type GET) and rules for setting up the behavior of the sensor gateway (rules type SET). The data extracting rules are unconditional. Command GET is sent to set the function to be performed. The rules for setting the behavior are executed based on the user pre-defined condition. All these rules are also stored in the database. The 'View All Gateways' activity is used to display the status of each sensor gateway. The values obtained from the sensors in result of performance the assigned GET rules are visualized.

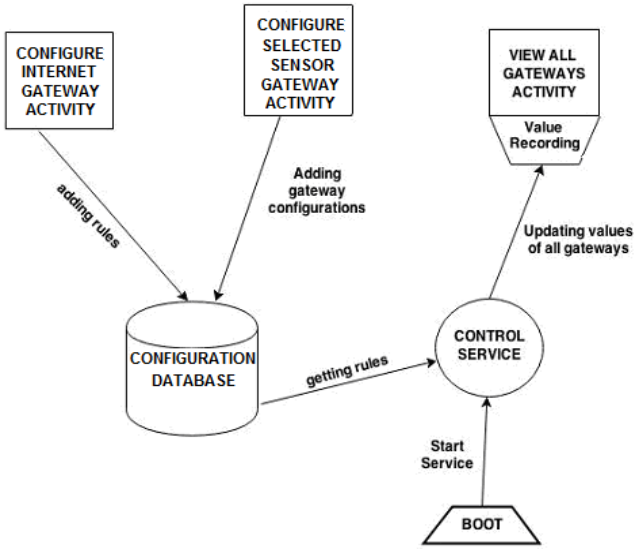

Fig. 5. Functional diagram of the application for OlinuXino A13.

The Control service is the core of this Android application. First, it retrieves the user defined GET and SET rules from the database. Then performs these rules and updates the information for the status of each sensor gateway, which is displayed on the 'View All Gateways' activity. The 'Configuration Database' allows better and easier configuration and re-configuration of the home automation network according to the user requirements.

V. Conclusion and Future Work

A low cost realization of a home automation network with two gateways based on open source hardware is presented in this paper. The communication between the sensor gateways and the Internet gateway is realized through Bluetooth wireless interface. The communication within the network is based on CNDEP protocol initially designed for data exchange in distributed embedded systems. A new adapted version of the CNDEP- Bluetooth protocol with several extensions is described. The advantages of the proposed solution are low cost, additional functionality and scalability of the system together with better sustainability toward power supply disturbances.

Employing this platform specific algorithms for energy efficiency of smart homes could be investigated experimentally. For profesional realization headboards as AVR-T-3244 and A13-SOM-512 could be used. Moreover, asymmetric encryption in the CNDEP protocol could be added and possibility for transfer of public keys using the Near Field Communication interfaces. While, the private keys for each gateway can be stored on their internal read-only memories.

The future research is directed toward adaptation of the home automation system to the Internet of Things (IoT) technology and integration to the Smart Grid and Smart Sity systems.

Acknowledgments

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Power Management in Embedded Systems: A Static Power Approach

Lubomir Valeriev Bogdanov and Racho Marinov Ivanov

Abstract – **The following paper focuses on an energy reduction technique in embedded systems called Static Power Management (SPM). The SPM is applied at compile time and aims at powering and/or gating off unused and inactive peripheral modules in the system. By investigating a particular example we try to gain data for future optimization algorithms.**

Keywords – **static power management, SPM, embedded systems, energy reduction.**

I. Introduction

Embedded systems executing bare-metal and single-threaded firmware (i.e. no OS) expose a good level of compile-time predictability. One could take advantage of this feature and use it for energy reduction. This is where the Static Power Management, or SPM, could be used [1]. Unused peripheral modules in a microcontroller or in an embedded system can be gated off to reduce dynamic power consumption. Some implementations allow for a complete power down of a module. The latter reduces static and leakage consumption.

Theoretically an SPM algorithm can be implemented easily – whenever there is no hardware access to a peripheral, it can be switched off. But practically this is a daunting task. The time of the powering on and off, as well as the initialization of the module, could seriously harm the energy optimization. The purpose of this paper is to assess an application before and after using an SPM.

II. Test Setup

A. Basic explanation

For a test system we have chosen a typical closed-loop embedded system for object control. The block diagram is shown in Figure 1. Here we have a source of data that could be analog and/or digital. Usually the input data is fed into a converter that transforms it to a set of digital values. Those values are then processed and sent to an output converter. The signals from this converter are used by an actuator that controls the object of interest.

Having in mind this theoretical setup, we have used an ARM Cortex-M4 based microcontroller (Texas Instruments' LM4F232H5QD) to develop such a system. It is shown in Figure 2. As it can be seen from the figure there is no object to be controlled. This is because it is irrelevant from software point of view. Furthermore this would allow us to modify the processing pseudo-algorithm for our needs.

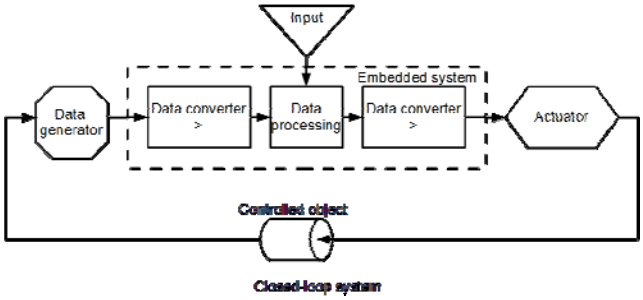

Fig. 1. Closed-loop embedded system.

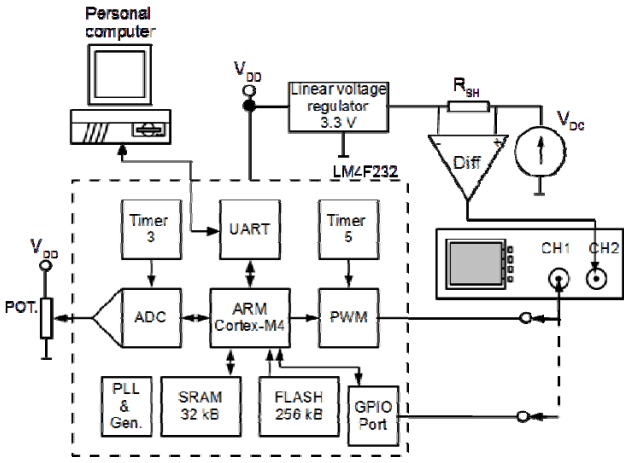

Fig. 2. System under test.

The firmware that we are testing reflects the closed-loop concepts. The original (non-instrumented) program is shown below with pseudo-code. The main loop of the program is

```
init( );

while(1){

set_gpio_pin( );

adc_val = measure_adc( );
pwm_val = process_data(adc_val);
set_pwm(pwm_val);
printf_uart(msg);

clear_gpio_pin( );

delay_ms(1);
}
```

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separated with a toggle of a GPIO pin and a small delay for oscilloscope synchronization. Along with the current measurements, we are able to estimate the energy consumption for one period of the firmware. The algorithm starts with ADC measurements that represent the input data conversion part. The analog values are kept constant during the measurements. They can be adjusted by the potentiometer POT in Figure 2. The converted samples are fed to a processing function. The calculations that we perform are dummy. Then the processed data is passed to a function that sets the duty cycle of a PWM module correspondingly. The PWM is the output converter. It is monitored by an oscilloscope to make sure that the firmware is alive during the measurements. Between the processing part and the PWM module we have inserted some asynchronous data communication (UART) because usually such systems are controlled remotely.

B. Used modules

To make a conclusion of the above-mentioned peripherals we will list them. Those will be the modules that will be switched on/off during the experiment. They are shown in Table 1. Unfortunately the manufacturer does not provide information about the current consumption of the separate modules. This is normal since a microcontroller is a software controlled device. Some currents are provided under some specific frequencies and conditions (such as all peripherals on, all peripherals off, sleep modes, etc). Therefore we cannot anticipate the current consumption of a separate module. That's why we have chosen to measure the current before and after the optimization, as many researchers in the same field do.

TABLE 1. USED MODULES

Peripheral	Type	Function
ADC	Analog-to-digital converter	Converts analog values to digital values
ARM Cortex-M4	Microprocessor	Executes instructions
PWM	Pulse-Width-Modulator	Generates voltage impulses with variable length
UART	Universal Asynchronous Receiver-Transmitter	Communication module for sending/receiving bytes on the RS232 interface
Timer	Timer	Asserts interrupts at given time periods.
FLASH	Memory	Program memory
SRAM	Memory	Data memory
GPIO	General-Purpose Input Output	Module for software control of the pin levels in a micro-controller

III. STATIC POWER MANAGEMENT

A typical SPM algorithm for optimizing energy consumption checks at compile time for parts in the firmware code where certain modules of the microcontroller are inactive or are not used at all. Depending on the power management features, the clock signal supplied to the module could be gated off or even its entire supply voltage could be switched off [2]. The first case allows the programmer to initialize the module only once and reduce its dynamic power consumption during the inactive periods. The second case requires multiple initialization and will lead to dynamic power reduction, as well as leakage power, during the inactive periods [3] [4].

In this case study we focus on 4 variations of the application. The first three investigate optimization dependence on inactive-active transition time of the module, while the fourth one concerns optimizations with changes in the execution model of the firmware.

There are three possible scenarios that could affect the SPM optimization:

- The execution time of the main processing t_{EXEC} is less or equal to the execution time of the functions that make the active-inactive transitions $t_{A\text{-}IT}$

$$t_{EXEC} \leq t_{A-IT} \quad (1)$$

- Time t_{EXEC} is considerably greater than $t_{A\text{-}IT}$

$$t_{EXEC} >> t_{A-IT} \quad (2)$$

- Time t_{EXEC} is considerably greater than $t_{A\text{-}IT}$ and interrupts from timers are used

$$t^*_{EXEC} >> t^*_{A-IT} \quad (3)$$

The instrumented program differs from the original one by the additional API calls for the state transitions. The code is shown below. Other high-level source code transformations exist and are revised in [5].

```
init( );

while(1){

        set_gpio_pin( );

        init_adc( );
        adc_val = measure_adc( );
        disable_adc( );

        pwm_val = process_data(adc_val);
        set_pwm(pwm_val);

        init_printf( );
        printf_uart(msg);
        disable_printf( );

        clear_gpio_pin( );

        delay_ms(1);
}
```

As it can be seen, the PWM module is not turned off as this would affect the control of the object. On the other hand the ADC could be turned off because no conversion

takes place while the bodies of the other functions are being executed. The only negative effect in this case could be slower response time which should be assessed by the developer as whether is admissible or not.

The origin of the instructions and data of the microprocessor could also affect the energy consumption. For this reason we have setup another experiment and have investigated execution from RAM and ROM. Modifications to the start-up code and linker script are required. To make a more general conclusion we have used several microcontrollers (LM4F232, LPC1114, MSP430FR5739). The experiment is described later in this section.

The compiler used is a GCC cross compiler. The target architecture is ARM Cortex-M and the cross compiler prefix is ‘arm-none-eabi-‘. The LM4F232 tests were performed with the following command line parameters:

```
-mthumb -mfloat-abi=softfp -Os -ffunction-sections -
fdata-sections -MD -std=c99 -Wall -pedantic -
DPART_LM4F232H5QD -c
```

The LPC1114 and MSP430FR5739 tests were performed with:

```
-D__REDLIB__ -D__USE_CMSIS -DDEBUG -D__CODE_RED -O0 -
g3 -Wall -c -fmessage-length=0 -fno-builtin -
ffunction-sections -fdata-sections -mcpu=cortex-m0 -
mthumb -MMD -MP
```

As it can be seen from the above, in the first case we use optimizations for size of the code and in the second one – no optimizations at all. Those parameters were taken from the respective manufacturer’s integrated environments and were not changed. The effects of the optimization levels are irrelevant to this experiment.

The linker used is a GCC’s LD. Again, the prefix is ‘arm-none-eabi-‘. The linker script changes include:
- relocation of the .text section to SRAM, right next to the .data and .bss sections;
- relocation of the vector table in SRAM;
- changes in the start-up code to copy the .text section and vector table to SRAM.

The address range of the SRAM was provided in the respective microcontroller datasheets.

A. Measurement equipment and statistical analysis.

The measurement equipment used in this experiment is a shunt-resistor and a differential amplifier based one. More information about it is published in [6]. The error of the Idd current readings is 0,33 % in the range 0 ÷ 300 mA.

The number of measurements performed was once per each test case. As mentioned before, when we talk about optimizations, seldom is someone doing absolute measurements. What we need here is one measurement before and one measurement after the optimization.

B. Execution time t_{EXEC} commensurable with transition time $t_{A\text{-}IT}$

The original program was measured to consume 112 µJ per one period (one while(1) loop). The instrumented program in the first case had the process_data( ) function simplified down to one line of code with a dummy calculation. As expected, the resulting SPM optimization yielded 144 µJ per period (increase of 29 %). The time period was increased as well (52 %). Therefore we can conclude that the optimization was unsuccessful.

C. Execution time t_{EXEC} greater than transition time $t_{A\text{-}IT}$

In the second example we increased the time of the process_data( ) function by adding more computations. Thusly we simulate negligible time for the transitions. The original program now consumes 15 555 µJ per cycle. With the help of SPM this was reduced to 14 256 µJ (8,4 %). The time was increased with 0,6 %.

D. Execution time t_{EXEC} greater than transition time $t_{A\text{-}IT}$ using timers.

In the third case we used timers that trigger wake events every 0.5 s. During the rest of the time the system is sleeping. It appears that the wake-up of the system costs additional 5066 µJ which increased the consumption of the original program to 20 621 µJ per cycle. Despite this, the SPM was successful – the energy was reduced to 18343 µJ (11 %) per cycle. The increase in time was 1,3 %.

Figure 3 shows graphical view of the results. With SPM the execution time of one period is inevitably increased. The API functions that are inserted for clock gating and power switching introduce this overhead.

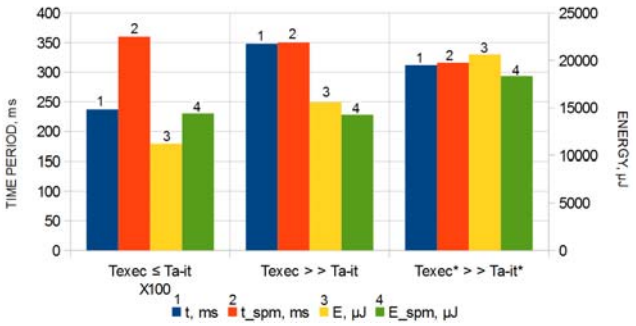

Fig. 3. Time period and energy consumption change before and after applying SPM.

E. SPM with change in the execution model.

Changing the instructions’ address of execution may lead to energy reduction. This is dictated by the fact that volatile and non-volatile memories have different static and dynamic power consumption, as well as access times. The most common scenario in an ARM Cortex-M based microcontroller is to execute parts of the program in read-only and random access memory. The other concept is to store the program in ROM and at start-up relocate it to RAM. We used two more microcontrollers for the experiment. Their architectures are listed in Table 2.

Every instruction has a load memory address (LMA) and a virtual memory address (VMA) [7]. The LMA is the address at which the instruction is stored. In our case this is

the read-only memory. The VMA is the address of the instruction when it is executed.

TABLE 2. TARGET MICROCONTROLLERS

Microcontroller	Microprocessor	Architecture	ROM
LM4F232	ARM Cortex-M4	Harvard	Flash
LPC1114	ARM Cortex-M0	Von Neumann	Flash
MSP430FR5739	MSP430	Von Neumann	FRAM

Here we investigate execution from ROM and RAM. The RAM case is accomplished by modifying the start-up code of the firmware to relocate the vector table. The linker script is modified to have the appropriate LMA and VMA for each microcontroller and its respective address map. Once set-up, the addresses of the running code were verified with a debug adapter.

The tests were conducted with 3 different applications:

- Computationally intensive (processData)
- Memory access intensive (copyBuffer)
- External communication intensive (sendOnUART)

One might think that executing code from non-volatile memory consumes more energy than the case with the volatile one. The test, however, yielded different results (shown in Table 3). It can be seen that the technology of the non-volatile memory could make read/write accesses faster and more energy efficient. A proof for this is the communication application run on an MSP430FR5739 where the execution from RAM consumes more energy compared to the ROM execution. We also have 4 cases where there is little or no difference for the memory used.

TABLE 3. ENERGY CONSUMPTION OF CODE EXECUTED FROM ROM AND RAM

Arch / Test	Harvard (SRAM + Flash)	Von Neumann (SRAM + Flash)	Von Neumann (SRAM + FRAM)
processData	$E_{FLASH} \approx E_{SRAM}$	$E_{FLASH} > E_{SRAM}$	$E_{FRAM} = E_{SRAM}$
copyBuffer	$E_{FLASH} > E_{SRAM}$	$E_{FLASH} > E_{SRAM}$	$E_{FRAM} = E_{SRAM}$
sendOnUART	$E_{FLASH} > E_{SRAM}$	$E_{FLASH} = E_{SRAM}$	$E_{FRAM} < E_{SRAM}$

IV. CONCLUSION

The work presented in this paper could help in the making of an SPM optimization algorithm. The important information gathered here is that the energy reduction by the means of static power management comes always at a prize and that would be the execution time of the application. However we still consider this as a successful method because for a small time degradation we achieve decent energy reduction (values close to 10 %). Furthermore the SPM algorithm should provide the programmer with means of excluding modules from the optimization as this might interfere with the system's behavior (in our case this was the PWM module).

The SPM should also be supplied with information about the execution times of the application of interest and the active-inactive transition times. This would allow the prediction of the optimization outcome. In the cases where the A-IT times are greater or equal to the main application's duration the optimization will fail. Otherwise the SPM will succeed.

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Practical Implementations of Cloud Computing Technologies for Smart Metering in Electrical Power Systems

Mitko Petrov Shopov

Abstract **The paper presents a practical implementation of a system for smart metering in electrical power systems that makes use of cloud computing technologies and IoT. The use of cloud computing technologies increase reliability and protection of collected data (it is stored and replicated in multiple secure, commercial-grade storage systems) and eases the software developers in management of remote devices – the actual devices are managed through web services and provided REST-based interfaces. Two M2M cloud platforms are considered in the paper – Digi device cloud and DeviceHive.**

Keywords – **Distributed Embedded Systems, M2M, IoT, Cloud computing, Device cloud, Power systems, DeviceHive**

I. INTRODUCTION

With the development of sensor networks, wireless mobile communication, embedded system and cloud computing, the technologies of Internet of Things (IoT) have been widely used in areas such as Smart Meter, public security, Smart homes and so on [1]. There are three essential components of IoT [2]: embedded devices – consisting of both low cost/low power devices and high-end gateways; scalable connectivity – each embedded device should be connected; cloud-based mass device management – centralized management of distributed devices.

II. BACKGROUND

The joint use of distributed embedded systems and cloud computing technologies is an extension to the efforts of integrating monitoring and control within the business information systems. The aim is to support the binding of monitoring and management of physical processes from the environment with the business logic and business processes [3].

A. Machine-to-machine

Machine to machine (M2M) is a broad term used to describe any technology that enables networked devices – wired or wireless - to exchange information and perform actions without the manual assistance of humans. As such the M2M is an integral part of IoT. The support of legacy devices and devices without proper communication capabilities, will require the use of M2M gateways/aggregation points. These gateways could also be used for some local intelligence and value-added services [2].

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A. Smart metering

One of the applications of M2M is smart metering. It integrates communication capabilities with electrical power systems and delivery infrastructure to automate monitoring and control. Dynamically linking utility supply with demand could result in optimization of resource consumption [2].

Smart meter is an advanced power meter that represent advanced metering infrastructure for enabling an automated, two-way communication between the utility meter and the utility provider. The smart meters are equipped with two interfaces: power reading interface and communication gateway interface [4].

A. Cloud-based applications

Some of the advantages of moving the server applications within the cloud are [5], [6], [7]:

- Application development: Development on the cloud will shorten development and prototyping time;
- Device heterogeneity: all the computation and storage is performed on the cloud infrastructure. The end-devices should only implement the communication protocol;
- Flexibility and scalability: Elastic resources allocation. Software updates does not affect end-devices;
- Mobility: Smart meters needs to be connected to Internet. All the computations are on the cloud infrastructure;
- Common user interface: Decoupling the computation infrastructure and the input system, enables multiple user interfaces to exist side by side allowing user-centric customization.

III. CLOUD-BASED SMART METERING APPLICATIONS

In this section, a practical implementation of a smart metering system will be described. The proposed implementation uses a power meter sensor PST04 [8], an M2M gateway and two different cloud platforms – Digi device cloud [9], and DeviceHive [10].

A. Power meter

The PST04 power meter measure the values of the main parameters of the three phase electric power system – voltage, current, frequency, active power, reactive power, power factor, active energy and reactive energy [8]. These transducers are developed at Development Laboratory for Semiconductor Circuit Engineering at Technical University of Sofia. They have two-wire instrumental serial interface, which enables development of industrial network [11].

B. M2M gateway

The M2M gateway is based on the hardware platform ConnectPort X4 [12]. It offers Ethernet, Zigbee, WiFi communication interfaces and USB/RS232 serial interfaces. It can be configured to route and filter the traffic between different networks. The gateway comes with a custom version of Linux-based operating system and a python-based framework Device Integration Application (DIA) [12].

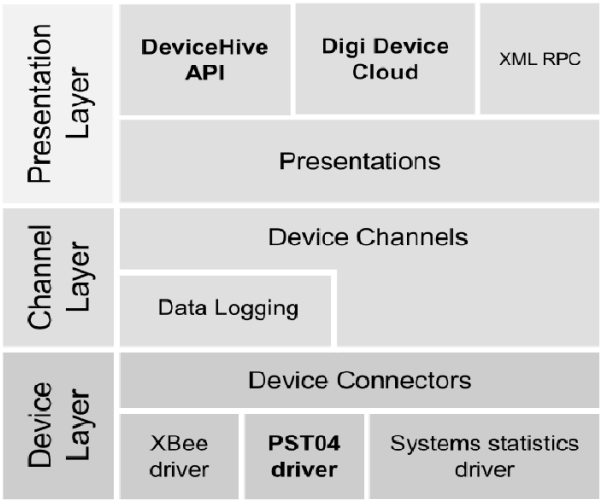

Fig. 1. Device integration architecture [12]

DIA framework provides the core libraries and functions for remote data acquisition, control and presentation between devices and information systems. Its functionality is distributed in three layers as shown on figure 1. The function of device layer is to provide connectors that extract real-world data, represent it as a set of properties and publish them to the appropriate channel on the next layer. Channel layer provides and manages publish-subscribe infrastructure that gives ability to create, remove, and publish to a channel, read from channel and subscribe for channel changes. Presentation layer provides the interface with the outside world. It could be as simple, as a telnet connection or a form of web service interface and even device cloud integration [12]. Using DIA as a basis two components are designed and implemented – (i) PST04 device driver and (ii) presentation driver for communication with DeviceHive cloud. The integration with Digi device cloud is already included.

The PST04 device driver implements the communication protocol of the sensor, extracts its data and loads it into the appropriate data channels. Based on the publish-subscribe mechanism, presentation drivers are automatically notified and uploads the data to its associated cloud services – Digi device cloud and DeviceHive, where it is stored and further processed.

A. Digi device cloud

Digi device cloud is a M2M cloud-based device management platform that includes a variety of APIs. It allows remote management of devices as well as insight into the cloud application health and current state of your entire device network [9].

Devices upload data to data streams on device cloud which are then available for push notifications, alarms, or retrieval by web services clients. Device communication can be achieved using device cloud devices, DIA, or custom cloud adapters (figure 2).

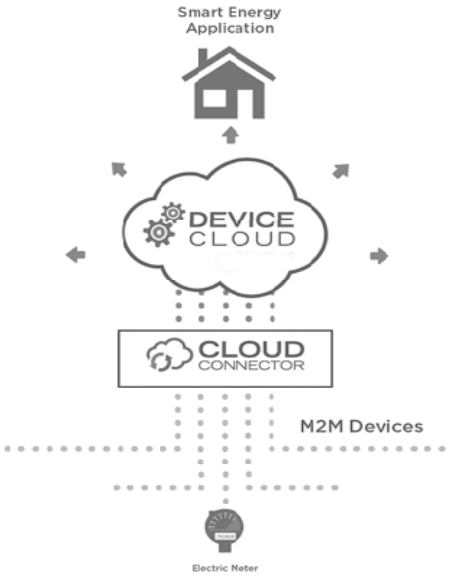

Fig. 2. Digi Device Cloud [9]

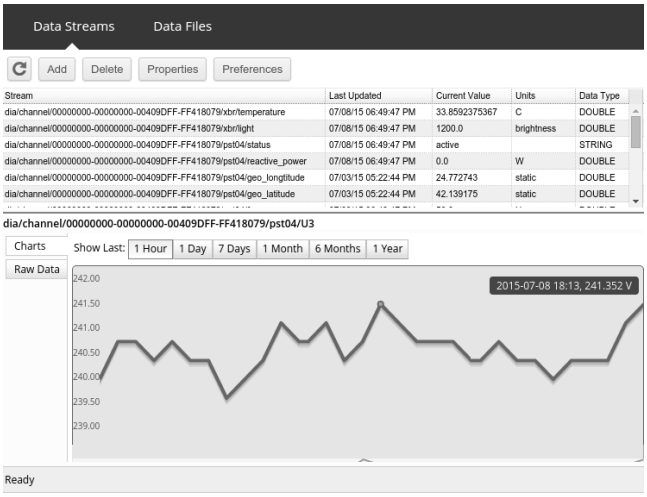

Fig. 3. Digi device cloud data streams for PST04

Time-series data involves two concepts: data points and data streams. Data points are the individual values which are stored at specific times, while data streams are containers of data points. Data streams contain metadata about the data points held within them. Data streams and

the data points they hold are addressed using hierarchical paths. Device cloud's data streams service is a REST API to store and access time series data in device cloud [9].

Digi device cloud provide interface for graphical representation of collected data streams (figure 3). The data can be visualized aggregated for different pre-defined time periods. Raw data is also available and can be accessed and managed by external service. Digi device cloud provides a standard HTTP API that allows many ways to access data.

B. DeviceHive

DeviceHive is an open-source M2M framework. It contains a set of services and components that allow establishing a two-way communication with remote devices using cloud technologies as a middleware. The devices can be anything connected: sensor networks, smart meters, telemetry, smart home devices and etc [10].

DeviceHive framework consists of devices, organized in networks, server application working in the cloud and client applications (figure 4). Devices that are not capable of connecting directly to the cloud, uses an intermediate node called gateway, which is responsible for communication with DeviceHive cloud and for managing devices (through some custom or binary protocol). Each device has one or more equipments, i.e. sensors or actuators. Clients can manage only those devices that are part of a network, the client has permission for.

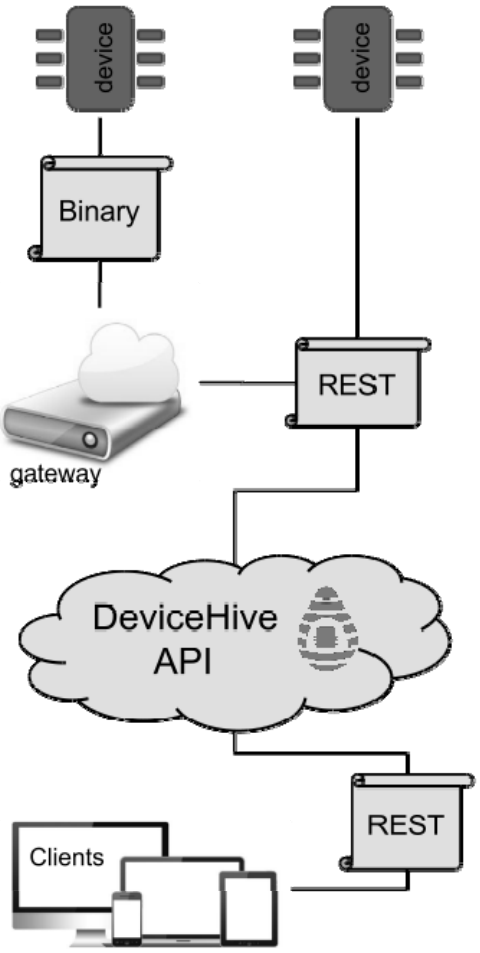

Fig. 4. DeviceHive Framework [10]

- In the presented implementation the PST04 sensor is a binary device, and its integration with the DeviceHive uses the M2M gateway discussed above. The M2M gateway operation flowchart is shown on figure 5. Blocks marked with gray are related to DeviceHive framework support. All the other blocks are implemented in the presentation driver (figure 1). The presentation driver first initialize DIA channels. In the next step, the DeviceHive framework is initialized, which includes connection to the cloud application, authorize the application with its credentials and obtain list of available networks. Then the application register the PST04 device and its equipment to DeviceHive.

After all the initialization and registrations are done, the presentations driver waits for: (i) commands received from DeviceHive, execute the command and responde with the result; (ii) notifications from the DIA channel layer, extract data and push it to the DeviceHive.

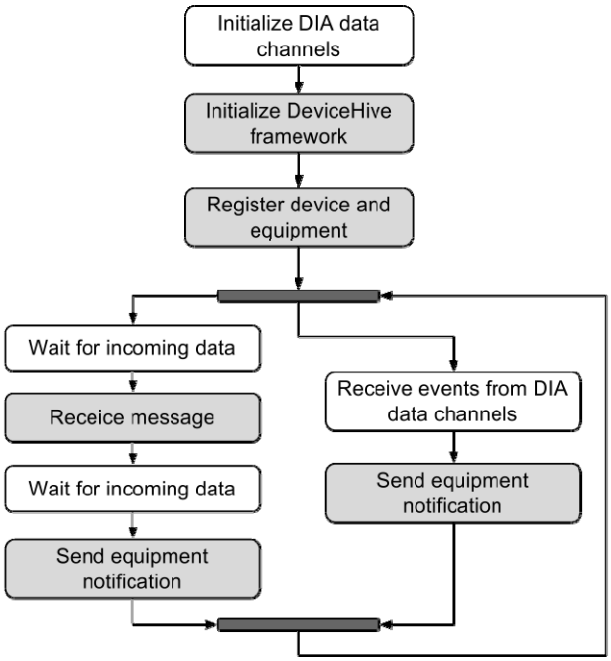

Fig. 5. Flowchart of device-to-cloud operations

For the management of DeviceHive devices a simple Android application is developed. It uses the provided REST API and its functionality includes authentication to DeviceHive, select a network from authorized, view devices and equipment, send commands and receive notifications (figure 6). The application can be configured to receive both synchronous and asynchronous notifications.

DeviceHive does not provide graphical representations of collected data series as Digi device cloud do. This could be provided by external services, through the use of the provided RESTful API interface.

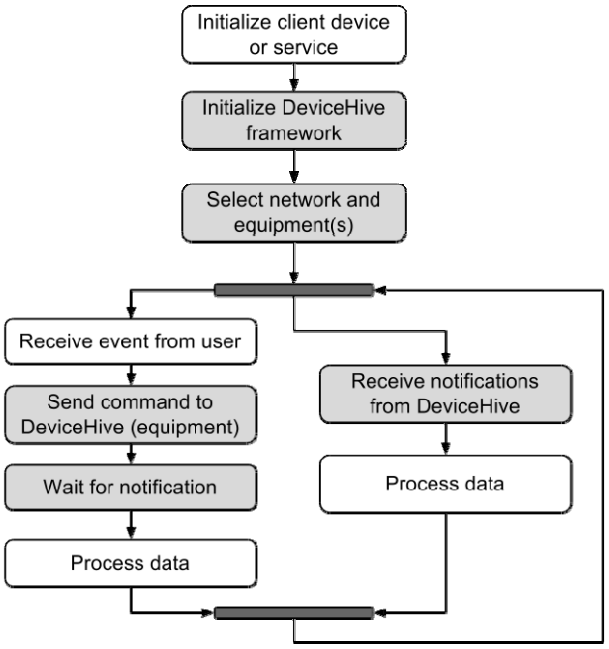

Fig. 6. Flowchart of client-to-cloud operations

IV. CONCLUSIONS

The paper presents a practical implementation of a system for smart metering in electrical power systems that makes use of cloud technologies and IoT. The use of cloud computing technologies increase reliability and protection of collected data (it is stored and replicated in multiple secure, commercial-grade storage systems) and eases the software developers in management of remote devices – the actual devices are managed through web services and provided REST-based interfaces. Two cloud platforms are considered in the paper – Digi device cloud and DeviceHive.

The Digi device cloud has the benefit of providing ready to use set of devices, that requires minimum to no programming for connecting it to the cloud. It also provides some extra services like graphical representation of collected data and device health monitoring. One of the disadvantages of Digi device cloud, however is that it is closed for development and cannot be hosted on your own private environment. On the other hand, DeviceHive is an open-source platform and can be further developed, extended, and hosted in private environment. It still has lack of some functionality, particularly in client-side services. The future work includes developing some new client-side services and extending the functionality of both the Android client application and M2M gateway.

ACKNOWLEDGMENTS

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Performance Evaluation of AES Symmetric Key Encryption Modes in an Ambient Assisted Living System

Velislava Grishina Spasova and Ivo Tzvetanov Iliev

Abstract – **This paper presents state of the art review of cryptographic practices as well as a performance evaluation of symmetric key encryption algorithms on an Allwinner A13 based ARM embedded system - part of a fall detection Ambient Assisted Living solution. The evaluated algorithms are 5 modes of the AES (Advanced Encryption Standard) symmetric encryption algorithm.**

Keywords – **Symmetric Key Encryption, Embedded System, Ambient Assisted Living**

I. INTRODUCTION

Ambient Assisted Living is a multidisciplinary area whose focus is in building solutions that ensure higher quality of life and independence of the elderly and people with disabilities. One of the major requirements to these systems which they share with the somewhat broader area of the Internet of Things (IoT) is to ensure very high privacy, security and data integrity [1-3].

Encryption and authentication are two of the major mechanisms for better application security. In terms of encryption, there are two fundamentally different groups of generic encryption algorithms – symmetric encryption algorithms and asymmetric encryption algorithms [4].

Characteristic of symmetric encryption is that both communicating parties share a common secrete key. This key is used for both encryption and decryption, thus specific measures for secure key distribution have to be taken. The most widely used symmetric encryption algorithm currently is AES (Advanced Encryption Standard) which is a block cipher with a 128, 192 or 256 bit key (128 bit keys are most widely used). AES is considered both cryptographically secure and relatively fast. It can be used in a variety of modes in order to extend the basic block cipher into a stream cipher which can be used to encrypt arbitrary length of data, such as multimedia data. The AES modes whose performance evaluation is presented in this paper are: CBC (Cipher Block Chaining), CTR (Counter), OFB (Output Feedback), CFB (Cipher Feedback) and GCM (Galois Counter Mode) [5].

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The other group of encryption algorithms is asymmetric algorithms. Characteristic of them is that a couple of public key - private key is used. The public key is publicly available to everyone while the private key is kept secrete by the party which generated the key couple, and is used only for decryption. The most widely used asymmetric algorithm is RSA (named after the names of its inventors – Rivest, Shamir and Adleman). In contrast to AES, RSA cannot be extended to encrypt large data such as multimedia – the maximum amount of data that can be encrypted by it ranges in the order of 100-400 bytes depending on the length of the key (1024 – 4096 bits) [5].

As both RSA and AES have their benefits and drawbacks, they are often combined into a hybrid scheme. In it RSA is used for private key exchange between the communicating parties (as a more secure alternative to the classic Diffie-Hellman key exchange algorithm) and once the communicating partied have agreed on a shared secret key, AES is used for the actual data encryption.

In recent years much research effort is focused towards encryption algorithms that are specifically tailored to images and a lot of chaos-based schemes have been proposed [6-8]. Unfortunately, due to the high complexity of the security domain and the corresponding cryptographic attacks, it is not enough for an algorithm to be mathematically and cryptographically secure – most of these new algorithms have been broken by side channel attacks [9, 10]. Thus, it is recommended to either use only established and well tested algorithms and implementations, or to at least integrate them into new schemes [5].

Finally, it should be noted that only encryption is not enough for safe data transmission. Authentication is also needed in order to ensure the authenticity and data integrity of the communicating parties. Some block cipher modes combine encryption with authentication (such as GCM mode) but the majority of encryption algorithms do not encompass authentication. For the purposes of this study the encryption algorithms were paired with the most widely deployed mechanism for authentication – HMAC (Hash-based Message Authentication Codes) [5].

The remainder of this paper is divided as follows – Section II presents a brief overview of the AAL platform that was used for the performance evaluation, as well as the architectural overview of the cryptographic module. Section III presents the results of the experimental evaluation of data encryption with the following modes: CBC, CTR, OFB, CFB and GCM. Finally, Section IV concludes the paper.

II. System Overview

The system that was used as an experimentation platform is an AAL gateway. The architecture of the system is presented at Figure 1.

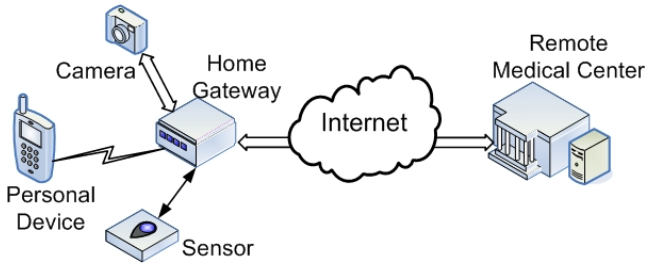


Fig. 1. AAL system architecture.

The gateway serves as the control unit of a home-sized distributed system which contains a variety of sensors such as accelerometer, camera, etc. It is also responsible for communication over the Internet with a remote medical center. As the transmitted information is predominantly personal (e.g. vital parameters, pictures of the user, information about his/her physical condition) all data should be encrypted and authenticated before transmission. The device used as a gateway is A13-OlinuXino-WiF based on the A13 microcontroller with ARM Cortex A8 core. It has a variety of communication interfaces such as WiFi and Ethernet, 512 MB RAM and 4 GB flash memory. The board runs Debian Linux

The cryptographic module that we have set up as well as the communication protocol between the gateway and a remote server are presented at Figure 2.

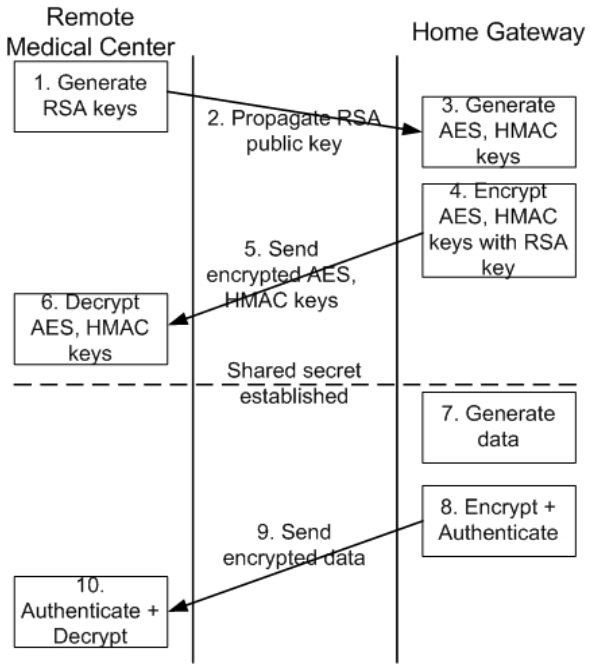


Fig. 2. Cryptographic module.

Before any encryption can take place, the two parties (in our case the gateway and the remote server) have to establish a common secret key. RSA is used for the key exchange. First, the remote server generates a 2048 bit private key - public key pair and sends the public key to the gateway. Then, the gateway generates a 128 bit AES secret key as well as a 256 or 512 bit HMAC secret key, encrypts them with the server's public key and sends them back to the server. Than, the server decrypts the message and extracts the two secret keys and the shared secret between the server and the gateway is established.

Once the server and the gateway have shared the authentication and encryption keys, the actual data transmission can take place. The gateway deploys an 'encrypt-then-authenticate' policy, according to which it first encrypts the data to a ciphertext and then authenticates the ciphertext, thus granting protection against active attacks. Consequently at the server side, the server first authenticates the received message and if it is valid, it proceeds to decryption.

III. Experiments and Results

For the experiment a test image has been re-sized into 5 with different resolutions – 120x160 pixels (19.2 Kpx), 240x320 px (76.8 Kpx), 480x640 px (307.2 Kpx), 720x960 px (691.2 Kpx) ND 960x1280 px (1228.8 Kpx), where Kpx stands for kilo pixels. It is highly unlikely that images with higher resolutions will be transmitted through the system so this dataset is exhaustive of the use cases.

For the experiment every image resolution has been encrypted with every one of the 5 AES-128 modes: CBC, CFB, OFB, CTR and GCM, and for the modes without authentication has been authenticated with HMAC with underlying hash function SHA-256 or SHA-512 (thus with 256 or 512 bit key). All the tests are run 100 times each and the results have been averaged. The tests are implemented in Python with the *cryptography* module [11]. The results from this runtime-based performance evaluation are presented at Figure 3.

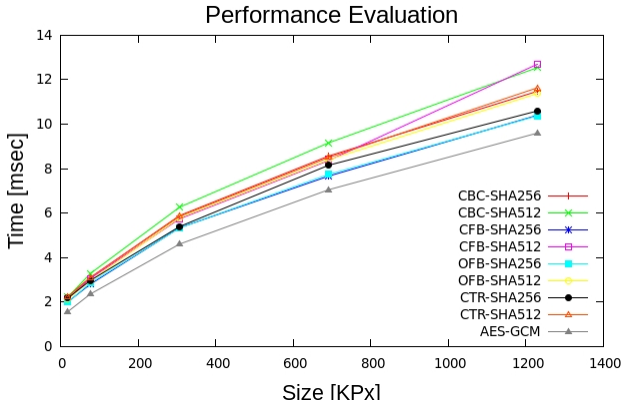
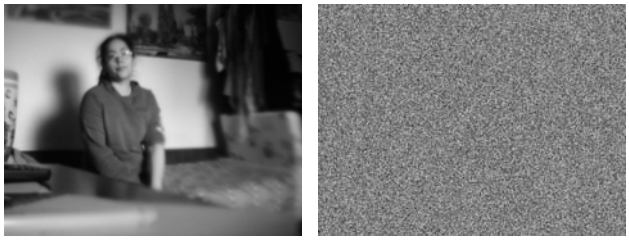


Fig. 3. Performance Evaluation of AES-128 encryption modes.

As it can be seen from the figure, all the modes have similar performance which is in the milliseconds range even for the largest image resolutions. Out of these GCM mode performs the best and has the added benefit of

automatic authentication. On the other hand this mode uses one key for both encryption and authentication which could be a drawback if the security of the system is somehow compromised. In reality any scheme – GCM or a combination of one of the other modes plus authentication, provides enough security with low additional processing cost. An example of un-encrypted image and its corresponding encrypted image with the GCM mode are presented at Figure 4.a and Figure 4.b.



a b

Fig. 4. Un-encrypted image and its corresponding encryption in AES-GCM mode.

IV. CONCLUSION

In this paper we have presented an overview of the requirements to privacy and security from the perspective of Ambient Assisted Living as well as a snapshot of the established state of the art cryptographic practices. An implementation of a secure data transmission system on a fall detection AAL platform has been illustrated. An evaluation of the runtimes of five of the most common modes of the AES cryptographic standard has been presented. Through this experiment we have proved that we don't have to sacrifice real-time responses for better security and that it is feasible to develop a secure system on an embedded platform with limited resources.

Future work will be concentrated on extending this system with algorithms which are more focused on image encryption as opposed to the currently deployed generic AES schemes.

ACKNOWLEDGEMENT

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Blended Approach in the Embedded Software Design

Ivan Georgiev Buliev, Teodor Borislavov Grigorov and Jordan Nikolov Kolev

Abstract – **The main purpose of the proposed approach is to facilitate and accelerate the embedded software development using a multiplatform software development environment and the development of virtual devices drivers for screen visualization and interactive models for I/O components of an embedded system. The whole development may take place on the PC in a simulation mode. Finally the virtual drivers are replaced by the actual subroutines for the real devices and the software is recompiled, programmed and run in the embedded system itself.**

Keywords – **Embedded software development, virtual drivers, software simulation**

I. Introduction

A. Challenges, faced by the embedded SW design

Embedded systems are everywhere around us – from mass products like smartphones and numerous other gadgets, through commercial, industrial, and military applications, to high-level scientific and research instrumentation. Regardless of the application specifics, the embedded systems have many common features and meet more or less common requirements. Among them are: real time implementations, flexible specifications, versatile platforms, multiple periphery, harsh environment, short time-to-market, cost restrictions, user friendly interface is a must (where applicable), highly competitive market, etc.

Although the traditional design flow and available tools for hardware and software development are continuously refined, the need of further improvement in the field is out of doubt.

B. Traditional design flow and tools

During the years, for various reasons, the C programming language has been widely accepted as the high-level language for programming Embedded systems. The traditional embedded software design usually involves a kind of Integrated Development Environment (IDE). The IDEs usually offer a plain text editor for code writing, extended with language-dependent syntax highlighting, an optimised C/C++ compiler, and a debugger able to connect and "speak" to the target system via different types of programming and debugging interfaces. Commercial products offer fast and convenient software design flows. Open source IDEs and compilation and debugging toolchains are also available. The usual sequence of actions is shown in the diagram in Figure 1.

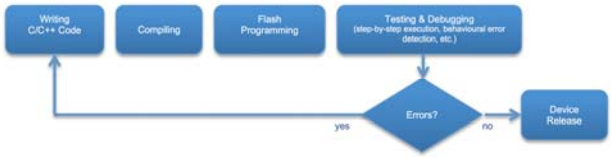

Fig. 1. Traditional design flow of the embedded software development.

Although the process seems straight forward, a number of particularities usually hinder the fast development and require careful and sometimes very detailed testing and step-by-step debugging. The compilation takes time. The programming of the flash memory also takes time and depending on the complexity and the program size, this time may be significant. Organising the debugging, setting up the break points, the code execution and the step-by-step execution through the various debug interfaces (JTAG, SWD, BDM, HID-based, etc.) are in general also time consuming. In some cases, as for example applications with externally imposed real-time functionality, the debugging is not only difficult but also even impossible.

In comparison to the programming for personal computers, perhaps two main differences can be distinguished. The embedded systems monitor and control separate either single-wire or grouped number of digital inputs and outputs but not necessarily multiples of eight, while the smallest container in ANSI C is the character, i.e. the byte. The other particularity is the presence in the personal computers and the absence in the embedded systems of the standard input/output console and the keyboard. Based on the teaching experience of the authors, these two differences are in the same time the main challenges in front of the young embedded software developers, usually having experience in programming personal computers.

In the same time, those who understand and adopt the differences start combining the two types of experience in their favour. Some advanced concepts from the personal computer software domain seem partially applicable in the embedded software design and presented below.

C. Attractive concepts from the personal computer programming

The personal computer programming continuously generates new ideas and concepts. Normally, they concern and are applied for computer systems of higher complexity, running operating systems (OS). Some of them however seem attractive for the embedded software design, as well.

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The application-driver model

Using of drivers is usually related to applications, which are run from a given operating system. This is also valid for the embedded software development for more complicated designs [1]. However, simpler embedded system designs could also benefit. If their firmware were structured appropriately, changing a single system component would not need much effort. For example replacing a monochromatic LCD with a true colour RGB display would be done fast, if the display output functions are based on a limited set of low-level functions, which will only need to be replaced. This is actually the generic idea of using drivers.

Virtualization

Virtual device drivers are a particular type of device drivers [2], [3]. They are used to replace and emulate real hardware device, especially in the quite popular recently virtual environment. In such an environment, a file can be interpreted as a CDROM drive with inserted disk in it for example. One could perhaps not find immediate application of the virtual drivers in an embedded system programming but we actually developed this idea and we present some results in the next sections of this paper.

Multi-platform SW development environments

The times when the only programming language for embedded systems was Assembler are far in the past now. Developers still use it but the high-level programming languages give much greater flexibility today. Among them, the C/C++ language is undoubtedly recognized as the most popular. The ANSI version of the C/C++ language is usually extended by the manufacturers to better meet the microcontroller particularities. Missing data types, as for example – bit, are usually added in a non-standard way. This makes the developed C/C++ application code actually non-portable and moving from one architecture to another is not straightforward.

Recently multi-platform compilers and libraries have been developed and offered as commercial products. Limited but open source versions are also released. One such platform that allows OS-independent application programming is Qt [4]. Again the presence of an OS is a prerequisite, and direct using of Qt for embedded programming is not worth in case of simple applications.

The advantages of the three above-mentioned technologies were exploited. In the present paper we present the developed by us approach for faster embedded software development and verification and we provide some successful examples.

II. Blended Approach for Embedded Software Design

A. Combining advanced practices

The main idea in our approach is to transform to a large extent the embedded software development into a software development for a personal computer.

One of the basic differences between the embedded systems and the universal computers is in the variety and the number of peripheral devices. A common personal computer has a screen as an output device and a keyboard and mouse as input devices. The embedded systems can have as I/O devices buttons, LEDs, LED-based indicators, intelligent LCD displays, touch screen panels, etc. but they may have also a plenty of sensors connected and providing different type of data.

No matter how many and different the peripheral devices are, almost always they can be attractively visualized on the screen of the personal computers. The input devices can be emulated with the help of the keyboard and the mouse. The sensor outputs may be modeled as sliders, the relay or transistor outputs may be manually switched on or off by clicking on small push buttons, etc.

B. Practical virtualization in the embedded SW design

Therefore, we suggest using of a multiplatform software development environment, allowing programing of graphical user interface (GUIs) applications and the development of virtual devices drivers and screen visualization and interaction models for the different I/O components of an embedded system. Then the whole development may take place on the PC in a simulation mode. At the end the virtual drivers are replaced by the actual subroutines for the real system devices and the software is recompiled, programmed and run in the embedded system itself. Using ANSI C/C++ for the common part of the code is a requirement but it is not a significant limitation in comparison with the significant acceleration in the software development process, by avoiding the continuous time-consuming uC reprogramming and stiff debugging. Conditional compilation using different keys for the PC and the embedded system provides the means for creating even a common project. The diagram in Figure 2 illustrates the main concept.

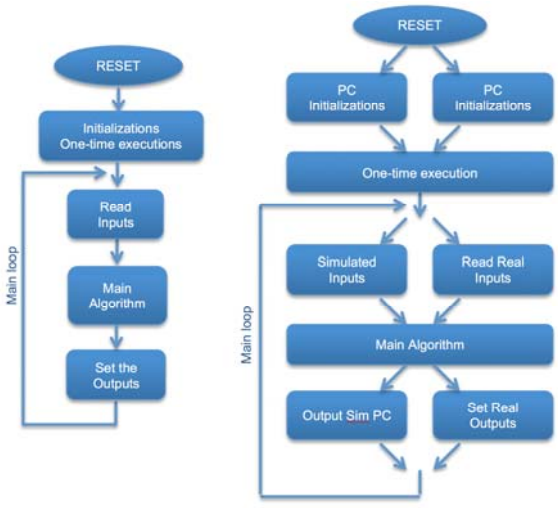


Fig. 2. Diagram, presenting the main concept

One time-consuming task in the software development is the organising and the rendering the various GUI screens. Using the virtualization approach we could cope much faster that initially planned. Figure 3 shows one of the GUI

screens as designed in the PC application. Figure 4 shows the real screen of the manufactured equipment.

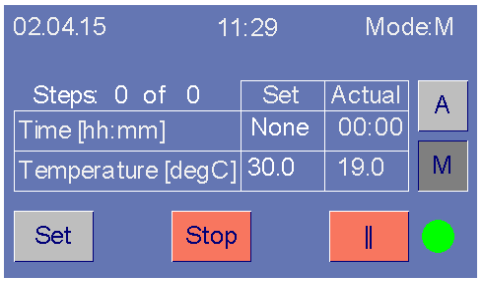


Fig. 3. A screenshot from the PC simulator application

Fig. 4. The same screen from Fig. 3 on the display of the real device.

The main slow-down however in the software development for this task was due to the duration of the real experiments. Significant time was needed for the real cooling or warming of the chamber. What we did was to virtualise the sensors and simulate their output with the help of common graphical controls in Windows – sliders, buttons, etc. (Figure 3).

This allowed to faster reach (although simulated) the conditions, requiring system response and thus provided means for much faster behavioural algorithm testing.

The project trees for the PC simulator application and the embedded application follow the concept from Figure 2 and are shown in Figure 5a.

The projects use the same header files and the same C source files. In Qt the C source files are #included within the C++ source files. The project files for Qt and MPLABX are absolutely independent. Specific and different C compiler keys were defined in each of them. This allowed the inclusion/exclusion of code segments in the common files depending on the platform for which the compilation took place. Figure 5b illustrates the conditional code compilation in case of PIC microcontroller or personal computer.

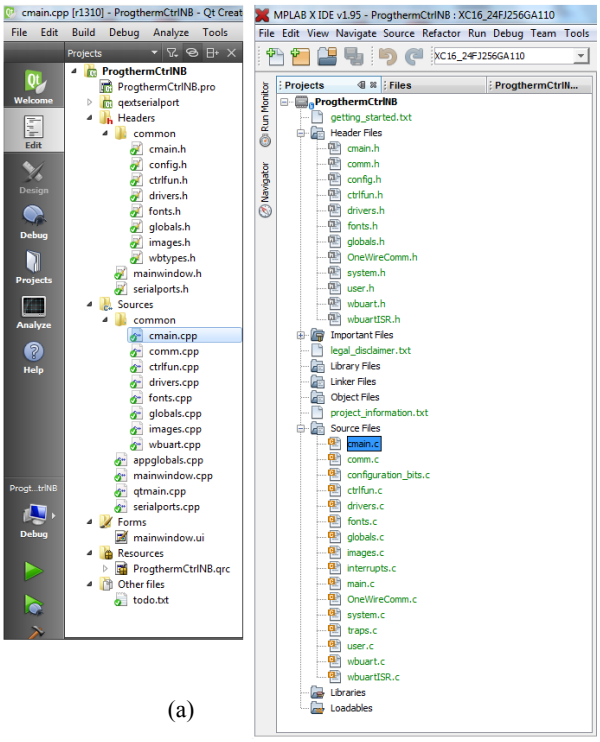
Porting the software from the simulator to the real device took about half a day. Final software refinements took few more days. Thanks to the applied blended approach, a significant reduction in the development time was achieved.

The suggested approach has been successfully applied in three different applications, provided as examples in the next section.

III. Successful Implementation Examples

A. Programmable thermostatic chamber

Physical experiments are performed at a wide range of the ambient temperature. The programmable thermostatic chamber that was developed has a working space of 50 dm^3 where a physical equipment and instrumentation can be placed. The temperature of the working space is controlled versus time in a range from -15^{0}C to +60^{0}C by a program.



(a)

```
// E2P related functions
int WriteE2P(short addr, char n, char *src)
{
   int res = GSUCCESS;

#ifdef WINEBOTSIM
   // QT
   for (int i=0; i<n; i++)
      e2pMemory[addr+i] = src[i];
#else
   // MPLABX
   char   *p, i;
   uint8_t AddrH, AddrL;

   AddrH = addr/256;
   AddrL = addr%256;
   p = src;

   Start_my_I2C3();
   res = Write_address_I2C3(EEPROM|EWRITE);
   res = Send_data_I2C3(AddrH);
   res = Send_data_I2C3(AddrL);
   for(i=0; i<n; i++)
      res = Send_data_I2C3(*p++);
   Stop_my_I2C3();
#endif
   return res;
}
```

(b)

Fig. 5. Project trees for the PC simulator application and the embedded application (a), and part of the code illustrating the different low-level implementation of writing to an I^{2}C EEPROM (b).

The program can be either entered manually at the device LCD touch panel or loaded from external computer as a preliminary prepared file. The number of time-temperature steps can be up to 255 with a total duration up to one month. A log file with temperature and time data can be recorded on an external computer.

B. ECETD

ECETD (Electro-Chemical Etching of Track Detectors) is intended for processing (etching) of general-purpose polycarbon compact discs (CD). The material of the CDs, i.e. polycarbon, being exposed to ionization radiation, particularly caused by Radon decay, keeps the tracks of the resulting alpha particles. The intensity of tracks is an integral estimate of the intensity of the ionization radiation on the place where the CDs are stored. This can be used for monitoring of ambient radiation in living areas. The tracks are very small and can be visualized by using of electron beam microscopy only. The etching process realized in ECETD makes the tracks visible by optical microscopes or even with unaided eyes. ECETD consists of a HV digital synthesizer (up to 4 kV, 6 kHz), electronic control, power supply modules and thermostabilized by Peltier coolers/heaters processing platform. Controlled parameters are: the processing high voltage, etching current, processing platform temperature, and duration of etching. The parameters are using the combination of a coloured LCD and a touch panel on top of it. An activity log can be created on an external computer through a USB connection. The manufactured device is shown in Figure 6.

Fig. 6. The ECETD device.

The software development also benefited significantly from the application of the above-described approach. GUI screens composition, touch screen input and device reactions were preliminary programmed and tested in a simulation mode and later ported to the embedded device.

C. Wine dispensers

Much more complex network system of wine dispensers was developed also with the partial support of the presented approach. Such automated wine dispensers are used in restaurants, wine shops, bars, wine tasting rooms, etc. They offer to the customers the opportunity to purchase small doses wine either for degustation (e.g. 20-30ml) or a full glass for pleasant consuming. The wine is dispensed from original bottles, which are being kept at the most suitable temperature for the respective wine sort. To preserve the wine in the bottles, to avoid oxygenation and prevent it from losing its genuine flavour, taste and colour, the wine is dispensed out from the bottle with the help of low-pressure nitrogen or argon gases. The tasks performed by the embedded controller include: temperature control of bottle section, gas pressure control, volume control of dispensed doses, RFID access control, etc. Main computer keeps a database for the wine bottles installed in the dispensers as well as for those stored in the shop.

Fig. 7. The wine dispenser

The challenge in the software development was not only the design of the GUI screens and the main algorithm programming but also the implementation of the network communication, allowing the simultaneous work of a number of wine dispensers connected to a main computer. The communication protocol was tested and tuned in a simulation environment, using two personal computers, one of them playing the role of the dispenser.

IV. CONCLUSIONS

The successful implementation of the three different products undoubtedly confirms not only the feasibility but also the benefits from the approaching the problems using a combination of simulations and real implementations and testing.

Qt and MPLAB proved to be able to be used in common projects. It would be also of interest to investigate and confirm the possibility to use together for example Qt and Eclipse and GCC for ARM development. Commercial IDEs (e.g. Freescale's CodeWarrior, TI's Code Composer) are based on Eclipse could eventually bring benefits as well.

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Improving the Resolution in Direct Inductive Sensor-to-Microcontroller Interface

Zivko Kokolanski, Ferran Reverter, Cvetan Gavrovski and Vladimir Dimcev

Abstract – **The paper describes an improved direct inductive sensor to microcontroller interface by incorporating external MOSFET transistors. In such a way, the measured discharging time interval can be increased (through the discharging time constant) which results in increased resolution for a given time base. The experimental results show that the resolution of the measurements can be significantly improved in comparison to the basic low pass filter and high pass filter topology. Moreover, such circuit can be used to interface inductive sensors with lower inductance.**

Keywords – **Inductive sensor, microcontroller, sensor interface, resolution**

I. INTRODUCTION

Inductive sensors are widely used to measure position, speed, displacement, vibration, and other process variables, especially in harsh environments [1]. Generally, a change in the process variable is reflected into variation of the inductance of the sensor. In order to obtain a useful signal from such sensors to embedded systems such as microcontrollers, usually a combination of signal conditioning electronic circuits in between the sensor and the microcontroller are used [2]. The signal conditioning circuits are usually performing some of the following tasks: 1. Inductance-to-alternating current (AC) voltage conversion, root mean square (RMS)-to-direct current (DC) voltage conversion and analog-to-digital (AD) conversion; or 2. Inductance-to-frequency conversion and logic level translation. Such complex signal conditioning increases the space, cost and power consumption.

In recent years, several interface circuits for inductive sensors with direct digital output were proposed [3]-[6], thus eliminating the need of AD converter. The interface circuit can be simplified even more by means of direct sensor-to-microcontroller interface. In the last decade, a lot of papers have been published on direct interface for resistive and capacitive sensors [7], as well as their differential [8], [9] and bridge configurations [10]. Recently the direct interface was also applied to inductive sensors in low pass filter (LPF) topology [11]-[13] given in Fig. 1, and high passes filter (HPF) topology [14], [15] given in Fig. 2. In both cases, a microcontroller is used to excite the *RL*/*LR* circuits and measure its transient response (charging/discharging time) through the sensor (L_x) and the calibration (L_c) inductance. Afterwards, a single point calibration is used to estimate the sensor inductance.

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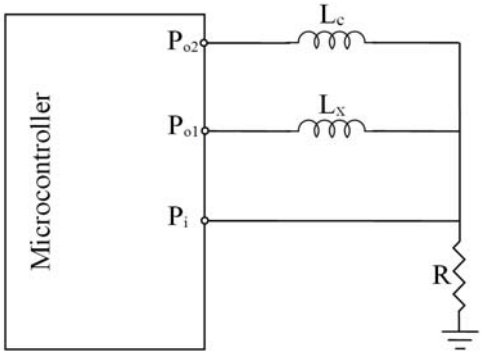

Fig. 1. Direct inductive sensor-to-microcontroller interface in low pass filter (LPF) topology

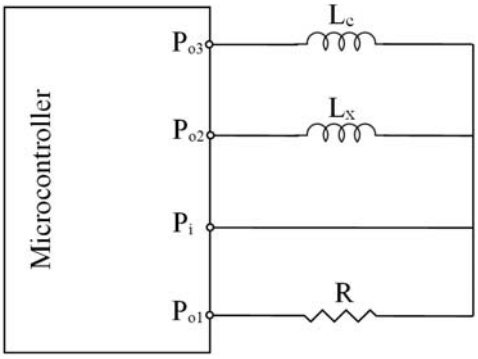

Fig. 2. Direct inductive sensor-to-microcontroller interface in high pass filter (HPF) topology

However, one of the major restrictive factors in both LPF and HPF circuit topologies is the microcontroller's maximal output current sink/source capability (typically around 20-30 mA) which limits the minimal external resistor *R* value, and consequently limits the charging/discharging time constant. In this context, the HPF is advantageous over the LPF topology and offers a larger time constant, i.e. higher resolution for a given time base (at the expense of more microcontroller interface pins). Nevertheless, for typical microcontroller clock frequencies up to 20 MHz, the measurements are roughly restricted to the millihenries range which rigorously limits the application to different inductive sensors. In this paper, a possibility to increase the discharging time constant with external MOSFET transistors (thus, increase the resolution) is given.

II. OPERATING PRINCIPLE

The modified direct sensor-to-microcontroller interface circuit in HPF topology with external MOSFET transistors is given in Fig.3. The circuit uses three N-channel (T_1-T_3) and one P-channel (T_4) MOSFET transistors in between the passive network and the microcontroller. According the

measurement procedure, two RL circuits are formed: circuit formed by R and L_x, and one formed by R and the reference inductor L_c. Each RL circuit is measured in two phases (first and second phase). The state of the microcontroller pins during the first and the second phase are given in Fig. 4 and Fig. 5 respectively. In the first phase of the RL circuit formed by R and L_x, the port P_{o1} is in a logical "0" state (turning off T_1), the port P_{o2} generates a logical "1" (turning on T_2), the port P_{o3} is in a logical "0" (turning off T_3 and turning on T_4), and the port P_i is configured as "input". In such a way, the microcontroller generates a transient pulse (through the MOSFET "driving" circuit) at the input of the RL_x circuit. In the meanwhile the microcontroller measures (with the built in timer) the discharging interval (exponential discharging voltage from the power supply voltage V_{dd} to the lower threshold voltage V_{tl} of P_i) seen by the input port P_i. Afterwards, the microcontroller ports are configured for the second phase as given in Fig. 5. Now the transistor T_4 is "off" and T_3 is "on" discharging the stored energy in L_x through R. The second phase lasts typically 7÷9 times the time constant ($\approx L_x/R$). The first and the second phase of the RL circuit formed by R and L_c are performed similarly (only the transistor T_1 is on and T_2 is off). The voltage waveforms of the characteristic signals during the measurements are given in Fig. 6. Hence, the sensor inductance is then estimated by using the single point calibration as:

$$L_x = \frac{t_x}{t_c} L_c , \qquad (1)$$

where t_x is the measured discharging time interval through L_x, and t_c is the measured discharging interval through L_c. Note that the duration of the time intervals t_x and t_c are proportional to the time constants L_x/R and L_c/R respectively. It is clear that the time constants can be increased by decreasing the value of R. However, R is limited by the maximal drain current of the MOSFET transistors (I_d) and by the maximal allowed peak current through the sensor (I_p) so that

$$\frac{V_{dd}}{R + 2R_{dson}} \le I_d , I_p , \qquad (2)$$

where it is assumed that $R_{dson1}=R_{dson2}=R_{dson3}=R_{dson}$ (R_{dson} is the drain to source ON-resistance of the N-channel MOSFET transistors T_1-T_3). The current technology easily offers small-size MOSFET transistors with drain currents in the order of amperes, whereas the output sink/source currents of the microcontroller ports are in the order of milliamperes. Therefore, the modified interface circuit allows using much lower value of the external resistor R (comparing to the circuits given in Fig.1 and Fig.2), limited mainly by the maximal allowed peak current through the sensor I_p. For a given time base, this will result in increased measurement resolution.

III. Evaluation of the Measurement Resolution

According (1) it is clear that the resolution of the measurements is mainly limited by the quantization of the timer in the microcontroller when measuring t_x and t_c. Hence, the resolution of the time-to-digital conversion can be expressed, assuming only quantization effects, as:

$$N = \log_2\left(\frac{t_{x\max} - t_{x\min}}{T_0}\right), \qquad (3)$$

where t_{xmax} and t_{xmin} are the discharging time intervals for the maximal and the minimal sensor inductance respectively, and T_0 is the effective time base of the timer.

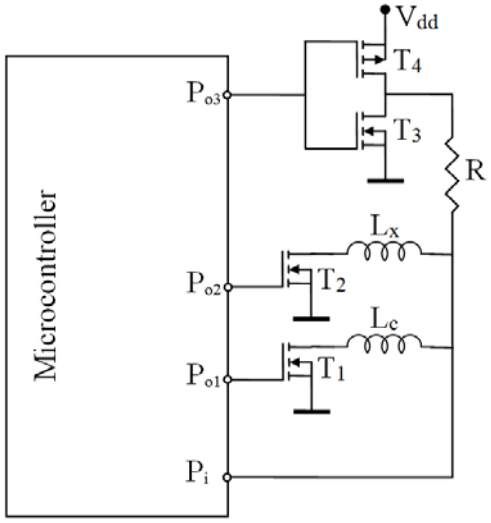

Fig. 3. Improving the time constants of the inductive sensor interface circuit with external MOSFET transistors

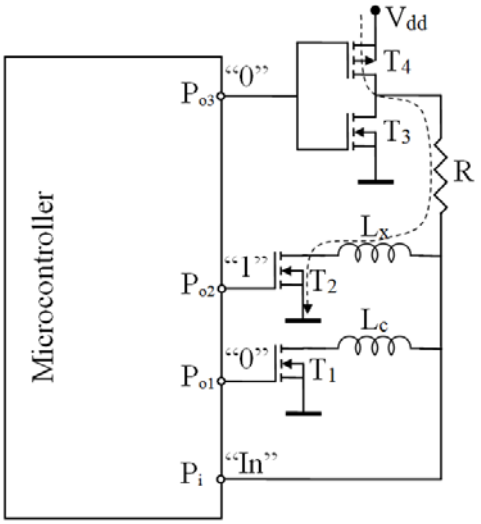

Fig. 4. State of the microcontroller pins during the "first" phase of the inductive sensor interface circuit

However, the measurement also suffers from trigger noise effects, thus decreasing the resolution. The effective number of bits (ENOB) of resolution can be expressed, assuming both quantization and trigger noise effects, as:

$$ENOB = N - \log_2\left(\frac{\left|\sqrt{u_q^{\,2} + u_n^{\,2}}\right|_{\max}}{u_q}\right), \qquad (4)$$

where uq is the quantization uncertainty, and un is the uncertainty due to noise effects. In direct sensor-to-

microcontroller interface the start of the measurement is synchronous with the timer, therefore according [16] the quantization uncertainty is given with:

$$u_q = \frac{T_0}{2\sqrt{3}} \quad (5)$$

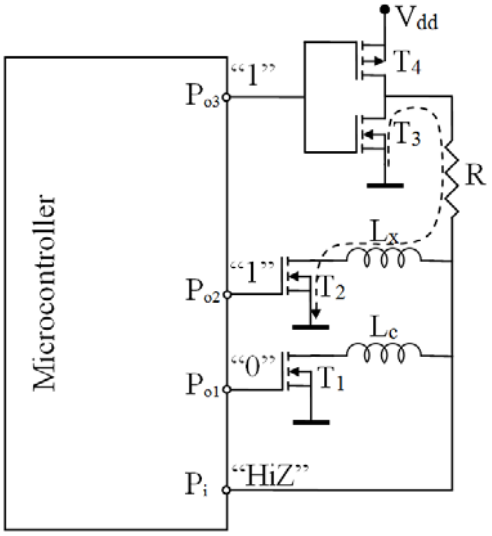

Fig. 5. State of the microcontroller pins during the "second" phase of the inductive sensor interface circuit

The noise related uncertainty is usually not defined in the microcontroller datasheet, therefore it can be evaluated by using a Type A evaluation, i.e. by statistical analysis of series of observations, given with:

$$u_n = \pm\frac{\sigma}{\sqrt{n}}, \quad (6)$$

where σ is the standard deviation of n consecutive readings of t_x.

IV. Experimental Results and Discussion

The experiments were performed by using a general purpose 8-bit microcontroller PIC16F877A with clock frequency of 20 MHz. A prototype board capable for implementation of all direct inductive sensor-to-microcontroller topologies (HPF, LPF and HPF with MOSFET transistors) was designed. The prototype board is given in Fig. 7. To reduce the noise effects, a special attention was paid to designing printed circuit board (PCB) ground plane and power supply decoupling. To emulate the extreme points of an inductive sensor, a decade inductance box was used. The minimal sensor inductance was 1 mH and the maximum inductance was 9 mH (for inductive sensors like [17]).

According the manufacturer datasheets, the maximum output current sink/source for PIC16F877A is 25 mA. Hence, having in mind the implementation conditions for achieving maximal resolution, the external resistor value for the LPF configuration was 300 Ω, and for the HPF configuration it was 100 Ω.

To implement the improved interface circuit, the following MOSFET transistors in SO-8 package were used: IRF7311 (dual N-MOS transistor) and IRF7307 (complementary N,P-MOS transistor). The maximal allowable continual drain current of the N-MOS transistors is 5.2 A, and -4.3 A for the P-MOS transistor. However, we assumed a maximum allowable sensor pulse current of 100 mA and therefore we choose an external resistor of 47 Ω. The experimental results are summarized in Table 1.

TABLE 1. SUMMARIZED EXPERIMENTAL RESULTS

PARAMETER	HPF		LPF		HPF+MOSFET	
	t_x [μs]	σ [μs]	t_x [μs]	σ [μs]	t_x [μs]	σ [μs]
L_x = 1 mH	8.6	/	3.2	/	18.2	/
L_x = 8.8 mH	77.4	0.06	27	0.015	165	0.19
N [bits]	8.42		6.89		9.52	
u_q [μs]	0.058		0.058		0.058	
u_n [μs]	0.019		0.005		0.06	
ENOB [bits]	8.4		6.8		9.0	

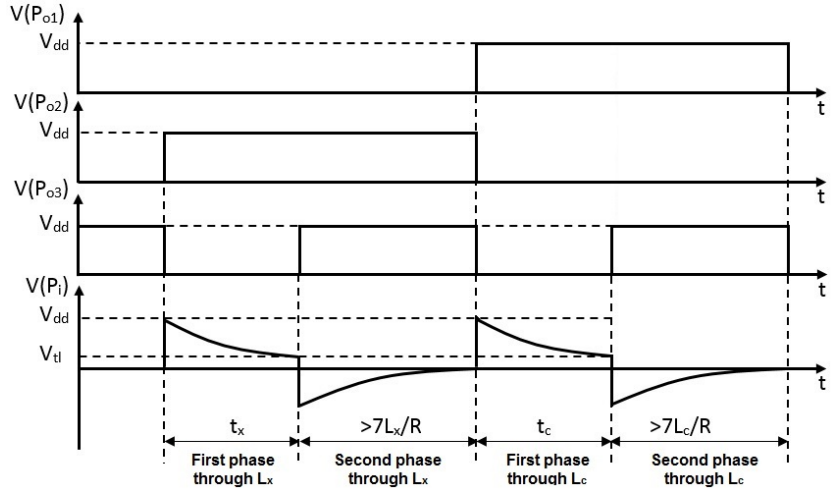

Fig. 6. Voltage waveforms at the microcontroller pins during the measurements

The measurements for each topology were performed once for the minimal sensor inductance (1 mH) and ten times for the maximal inductance (9 mH) to calculate the standard deviation (σ) and the standard deviation of the mean (u_n). Then, the resolution of the time-to-digital conversion and the ENOB were calculated according (3) and (4) respectively. In the calculations, an effective time base (for PIC16F877A) of T0=0.2 μs was used.

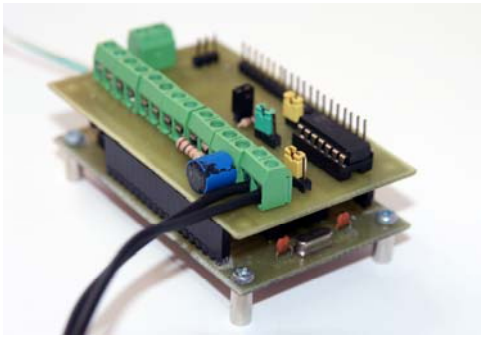

Fig. 7. Setup to test the improved direct interface circuit for inductive sensors

From the results reported in Table 1 it could be seen that the proposed interface circuit has a better measurement resolution. The ENOB increased 0.6 bits comparing to the basic HPF topology and nearly 2.2 bits comparing to the LPF topology. The resolution could be increased even more in cases where the inductive sensor allows higher maximal pulse current. Such results are even more advantageous in cases where the nominal inductance is in the order of microhenries where the basic LPF and HPF topology could be practically inapplicable due to very low resolution performance.

V. CONCLUSION

Direct inductive sensor-to-microcontroller interface is an alternative approach to interface inductive sensors without complex intermediate signal conditioning circuitry and without an analog to digital converter. To achieve this goal, a microcontroller is used to excite and measure the response of a passive RL network. One of the problems of this approach is the low-value time constant when measuring low-inductance sensors due to the limited microcontroller port sink/source current which limits the resolution of the measurements.

This paper proposes a solution to increase the discharging time constant by using external MOSFET transistors. The experimental results show that an improvement of the resolution comparing to the basic configurations can be easily achieved. Such improvement of the basic interface circuits can be very useful, especially when interfacing low-inductance sensors (say, lower than 1 mH).

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Loss of Load Probability in Wireless Sensor Networks using Solar Cells

Mare Srbinovska, Zivko Kokolanski, Cvetan Gavrovski and Vladimir Dimcev

Abstract – **In design and development of Wireless Sensor Networks (WSNs), one of the main challenges is to achieve long lasting battery lifetime. In this paper it is proposed model to estimate the reliability of the photovoltaic system in WSN. Modeling of the Loss of Load Probability (LOLP) parameter defines the system performance per month.**

Keywords – **Reliability, Photovoltaic system, Loss of Load Probability**

I. INTRODUCTION

Wireless sensor networks (WSNs) consist of hundreds or thousands of sensor nodes spread in an environment in order to monitor the specific physical phenomena. These networks have several advantages including easy installation, small size and low power consumption. In recent years, agriculture faces many challenges, so precision agriculture monitoring and remote controlling is rapidly growing [1].

Sensor nodes are small devices that include three basic components: a sensing system for data acquisition from the physical environment, a processing unit for data processing and storage and wireless communication component for measurement data transmission. In recent research, the focus is especially based on low power feature of the sensor nodes because the power consumption is always a challenge for wireless nodes, supplied with batteries [2-4].

So, the main problem in wireless sensor technologies are the constrained energy resources (e. g. Battery, processing capacity), and they should work as long as possible in the environment while collecting and sending data to the central station.

The development of crop production procedures would increase energy efficiency in agriculture and enable sustainable development [2],[3]. Furthermore, the use of renewable technologies on farms is considered as essential, but not single factor to influence modern and energy efficient agriculture [4]. In fact, cleaner production procedures and renewable energy technologies along with reliable real time monitoring systems based on WSNs would contribute in creating the adequate conditions for development of sustainable agriculture [5], [6].

We developed a system for monitoring of crop production which would be tailored to the needs of farmers and therefore, should be easy to build, use, maintain and upgrade, built of low-cost, low powered components and resilient to loss of data.

One of the main advantages of WSNs is their independence of pre-established infrastructure. In most common scenarios, recharging or replacing nodes batteries is not practical due to inaccessibility or huge number of sensor nodes. In order for sensor networks to become a ubiquitous part of the greenhouse environment alternative power sources should be employed. So, if nodes are equipped with energy transducers like, solar cells, the generated energy may increase the autonomy of the sensor nodes significantly.

Techniques to harvest energy via photovoltaic (PV) cells have attracted the interest of the sensor network community [7-9]. Solar energy is certainly one of the most promising energy sources and typical environmental monitoring applications have access to solar energy. Due to the progress in low power design, the energy generated by small solar panels suffices to execute most common data gathering applications. Equipped with photovoltaic cells, perpetual operation becomes possible without frequent recharging and replacement of the batteries.

The demand for the corresponding software control can be seen as one disadvantage compared to the battery operated systems. Also, concerning the hardware the solar panel has to be integrated into the system.

One more additional problem with the solar cells is using them during the night or when the solar radiation is very low (foggy or cloudy days). Thus, a means of storing energy is necessary. The stored energy is used to bridge the gap during the time when the ambient energy supply fades away. There are various means of storing electrical energy: capacitors, primary (non-rechargeable) and secondary (rechargeable) batteries, supercapacitors, etc.

II. METHODS FOR MODELING THE PV SYSTEM

To estimate the solar radiation it can be used statistical method or astronomical method. With a statistical method it is estimating the solar radiation for a given period using the history of solar radiation. With the astronomical model it is estimating the solar radiation using the parameters that affect the angle between the sunlight and the solar panel.

In order to get the statistics, we can use meteorological database, which estimate the solar radiation as the monthly solar radiation Using E_m, we can calculate the peak solar hours (PSH), which is the equivalent solar radiation hours per day assuming that the same amount of solar energy is given at an intensity of $1kW/m^2$. Then, the available energy from a specific solar panel for one day, E_{sol}, can be estimated as the product of PSH and the solar panel output power P_{sol} at $1kW/m^2$ (usually provided by its manufacturer):

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$$E_{sol} = PSH \cdot P_{sol} = \frac{E_m \cdot P_{sol}}{1kW / m^2 \cdot \#days} \qquad (1)$$

According to the metrology weather data base for the incident solar radiation in Skopje, Macedonia (latitude φ = 42,005°N, ψ = 21,41°E), one of the lowest values for the solar radiation is taken for December. This data is an average taken over almost 20 years and represent the best data we were able to find. For the experiment we chose minimum value for the month of December (2.10 kWh/m^2/day). This value represent the amount of energy (measured in kWh) accumulated over 1 square meter in a twenty four hour period.

III. Model of the PV System

To estimate the reliability of the photovoltaic system it is used NSol model. It is a computer assisted design tool that is used in the design and analysis of battery based photovoltaic (PV) power systems. There are three major tasks when designing a PV system using NSol:

- Entering the data;
- Optimizing the array tilt;
- Sizing the system and estimating performance

NSol [10,11] uses a proprietary Loss of Load Probability (LOLP) algorithm. Based on the concept of "Markov Transition Matrices" this algorithm calculates the statistical performance of the solar insolation resource, then applies this to the battery based PV system. The result is Loss of Load Probability, which gives a concise estimate of a system reliability.

To design the photovoltaic system, three solar cells of amorphous silicon with dimensions 3 cm x 3 cm are used with the following characteristics:

$$A' = 0,0009\,m^2 \qquad (2)$$

Where A' is the effective area of the photovoltaic cell

$$\eta_{pv} = 7,2\% \qquad (3)$$

η_{pv} is the photovoltaic efficiency refers to the PV cell's ability to convert light energy to current. For the purpose of this analysis, we will assume 7,2 % efficiency of the PV cells.

$$P'_{pv} = A' \cdot G_{sc} \cdot \eta_{pv} = 0,065W \qquad (4)$$

P'_{pv} is the power generation for one PV module.

$$P_{pv} = 3 \cdot P'_{pv} \qquad (5)$$

Multiplied by three, we calculate the power generation for the three modules (equation 5).

$$W = 0,26Wh / day \qquad (6)$$

To design the PV system we need to multiply the calculated values for the power generation in order to size the PV system using the NSol tool. For the equivalent power generation per day.

$$\overline{P}^e = 7,2W \qquad (7)$$

Skopje , R Macedonia
φ = 42,005°N, ψ = 21,41°E

Minimal solar insolation

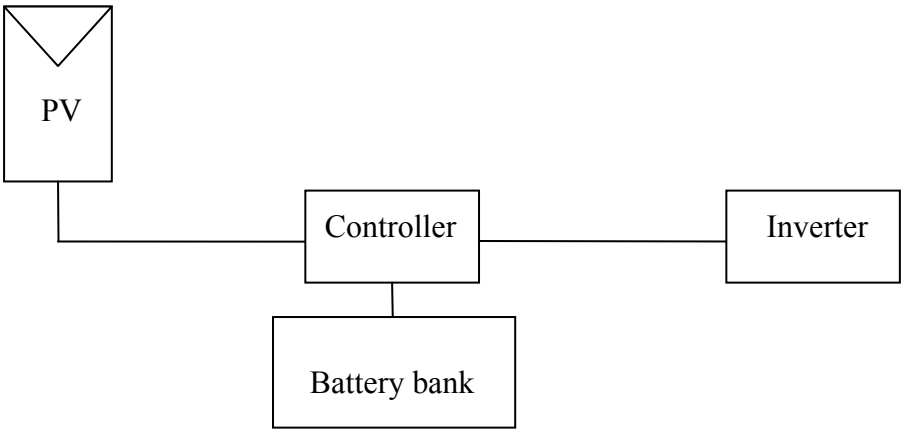

Fig. 1. Model of the PV system

In figure 1 is given the model of the PV system. The model consists of three components: PV, Controller, Inverter and Battery bank. Every component should be properly dimensioned in order to design the system. For example in inverter tab should be defined the VAC operating voltage of the inverter, VDC to DC voltage of battery based inverter, the efficiency and cost of the inverter etc. Battery bank tab defines the model and type of the manufacturer. The controller tab defines the operating voltage of the controller, maximum battery charge amps of controller, while PV tab defines how many PV cells are used in series.

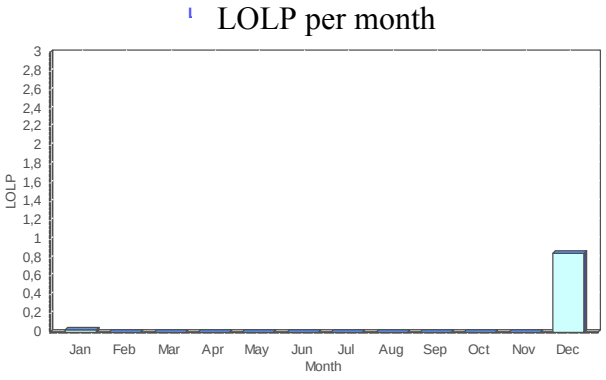

Fig. 2. LOLP per month

On the figure 2 it is presented the Loss of Load Probability factor per months for the designed PV system. According to the calculations the system is very reliable for almost every month. The lowest value for LOLP is calculated for December. LOLP=0,8%, while for January is 0,03%.

TABLE 1. PERFORMANCE PV SYSTEM VALUES FOR SKOPJE

Months	Solar insolation (kWh/m^2/ day)	Battery size (days)	ALR
January	2,32	10,6	1,19
February	3,05	10,7	1,56
March	3,86	10,9	1,97
April	4,43	11,2	2,27
May	4,59	11,4	2,34
June	4,86	11,6	2,49
July	5,08	11,6	2,60
August	5,16	11,6	2,64
September	4,90	11,5	2,50
October	3,91	11,2	2,00
November	2,68	11,0	1,37
December	2,10	10,7	1,07

The Loss of Load Probability (LOLP) is a statistical calculation on whether the array and battery combined can support the load.

A low LOLP (0.3 or lower) indicates that the system is very reliable. An LOLP of 0.3 indicated that the system will lose the load on an average of 0.3 days per month. If the month has 30 days, this is a load disconnect event once every three years.

In the table I are given the parameters that define the performance of the PV system. In the first column it is presented the solar insolation values per month. The lowest value is for December as the worst case. The other parameter is the battery size per days, which defines how long can the system work reliably without loss of load.

The other primary output beside the Loss of Load probability is the Array to Load ratio (ALR). The ALR is simply the energy balance between the average insolation and the average load for the design month. A good system will operate best with an ALR of at least 1,1. The critical value for this parameter is again for December.

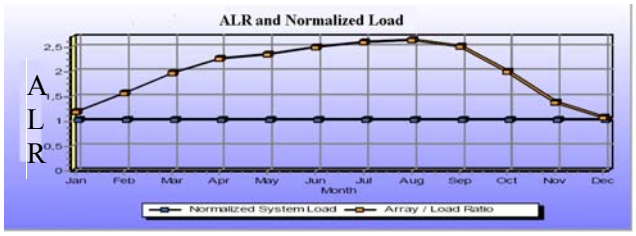

Fig. 3. System performance - ALR per months

In figure 3 it is given the graphical representation of the system performance for the Array to Load ratio (ALR) per months. The highest values are for the summer months, while the lowest values are for January and December.

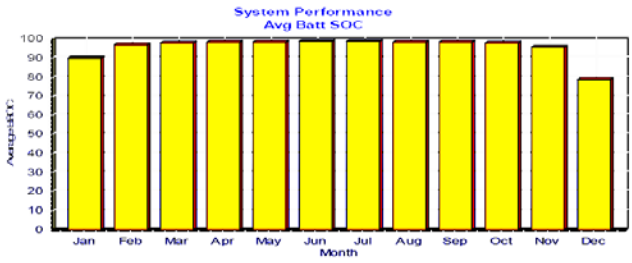

Fig. 4. System performance - BSOC per month

The state of charging of the accumulated battery (Battery State of Charge – BSOC) has typical starting value of 40% SOC, and stop value of 85-95% SOC. Each cycle replaces 45-55% from the capacity of the accumulated battery.

The graphical representation of the BSOC per months is shown on figure 4. This parameter actually defines the efficiency of the system.

The best value is obtained for August, while the worst value is obtained for December.

IV. MEASUREMENT OF SOLAR CELLS VOLTAGE DROP

The solar cells can work during the day and use the accumulated energy during the night. In this experiment the sensor nodes transmit the measurement data twice in one hour and goes to sleep mode to save energy. During of one month measurement, the solar cells voltage drop is shown in fig.5.

As it can be seen from the figure the maximum value of the solar energy voltage is 4.1 V, which is reached during the day when the sun is mostly intensive, while the lowest value is dropping to 2.5 V.

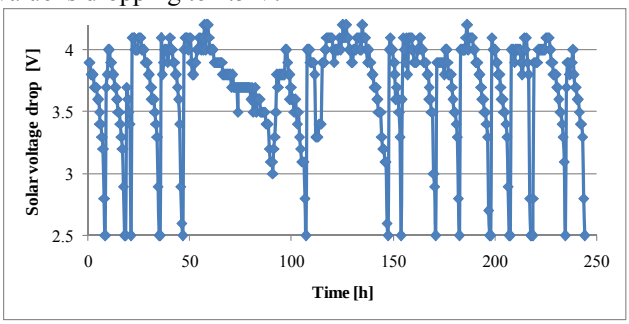

Fig. 5. Solar cells voltage drop taken in August in Skopje, R. Macedonia

This is still operating value for the sensor nodes. The measurements were made in August, 2014 (the best case) and on the figure are presented the measurement results for one week of measurement. It can be seen that the curve is continual without any interruptions during the data transmission. This is because the solar energy is enough to power the nodes the whole time.

V. CONCLUSION

Energy consumption is one of the most constraining requirements for design and implementation of wireless sensor nodes. Analysis of power consumption and reliability of the measurement system are the crucial factors for the design and development process of the sensor networks.

In this paper, a model for estimation of the reliability of the photovoltaic system is presented. Loss of load probability is a statistical calculation parameter that represents the reliability of the system. The low LOLP (0.3 or lower) parameter indicates that the system is very reliable. The best cases are obtained for the sunny months (July and August), while the worst case is obtained for December and January.

The solar cells voltage drop for one month measurement is presented. The system works continually without any interruption during the transmission of data.

Different design, deployment and functional aspects of a reliable WSN are analyzed in this paper. A wireless sensor node reliability model considering the battery voltage level is evaluated.

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Electric Power Transducers with Networking Capabilities

Peter Ivanov Yakimov and Nikolay Todorov Tuliev

Abstract – **Modern energy systems control faces various challenges caused by the introduction of renewable energy sources and rapidly changing loads. To achieve successful and sustainable control big quantities of information have to be transferred and processed. This establishes the need of universal accurate measuring transducers with rich information capabilities. The paper discusses the structure and the operational possibilities of measuring transducers for networking application.**

Keywords – **Electric power system, Smart transducer, Network**

I. INTRODUCTION

Modern energy systems control faces various challenges caused by the introduction of renewable energy sources and rapidly changing loads. This requires the application of innovative approaches in the automation systems aiming energy efficiency increase. Key problems in reaching this goal are intelligent sensor networks development and storage and real time processing of the large amount of data generated by them. Similar to the production technology, production control and monitoring systems have moved away from central operational structures and towards Decentralised Control Systems (DCS) [1]. Industrial processes as well as many modern systems depend on SCADA and DCS systems in order to perform their complex functionality. Typical examples include electric power grids, oil refining plants, pharmaceutical manufacturing, water management systems etc. An advanced trend in the distributed automation systems development for working with great number of sensors and large data arrays is the use of networks and Internet technologies based on Web services (Service Oriented Architectures - SOA) and cloud technology. The building of a smart energy system includes realization of a variety of measuring devices distributed in different locations – at the end customers, at the manufacturers, in the distribution network. These distributed measurements can be done using smart transducers connected in networks which will be able to measure and to process primarily the data but to transmit them to different locations for storage, analysis, accounting and etc. as well. Such networks are from the type IoT (Internet of Things) and WoT (Web of Things). The foundation of Internet of Things (IoT) is the intelligence that embedded processing provides. The IoT is comprised of smart machines interacting and communicating with other machines, objects, environments and infrastructures. As a result, huge volumes of data are being generated, and that data is being processed into useful actions that can "command and control" things to make human lives much easier and safer - and to reduce the human's impact on the environment [2].

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II. SMART TRANSDUCERS OBJECTIVES

Smart Grid is regarded as a system that uses two-way communication and information technologies, and computational intelligence in an integrated fashion across electricity generation, transmission, distribution and consumption to achieve an electric system that is clean, secure, reliable, efficient, and sustainable [3]. The two-way communication, allowing both control and management of the network devices, is becoming even more important.

European Working Group for smart grids defined as intelligent energy networks that can efficiently integrate the behaviour and actions of all connected to them users - producers, consumers and those that do both - in order to ensure economically efficient and sustainable power system with low losses and high quality, security of supply and safety [4].

According to Article 2, paragraph 28 of the Energy Efficiency Directive (2012/27/ES), OJ L 315, 14.11.2012, p1 „smart metering system" or „intelligent metering system" means an electronic system that can measure energy consumption, providing more information than a conventional meter, and can transmit and receive data using a form of electronic communication".

Smart meters and the information they provide are of a great importance for a smart grid to work effectively and efficiently.

Measuring transducers are used everywhere, where measurement of electrical quantities and sending of data or signals to devices is needed for checking and supervising the used energy. They are intended for a permanent monitoring and for conversion of electrical quantities in single and three phase electrical systems. PLCs, PCs, microprocessor control, indicators, alarms units and etc. can be operated by the output signal. The communications interfaces are serial (mostly RS-485) or Ethernet. The analog outputs of the transducers can be used in places where is needed analog output quantities as input into another device [5], [6].

III. SMART TRANSDUCERS STRUCTURE

A smart transducer is the integration of an analog or digital sensor or actuator element, a processing unit, and a communication interface [7]. A smart transducer comprises

a hardware or software device consisting of a small compact unit containing a sensor or actuator element, a microcontroller, a communication controller and the associated software from signal conditioning, calibration, diagnostics and communication [8].

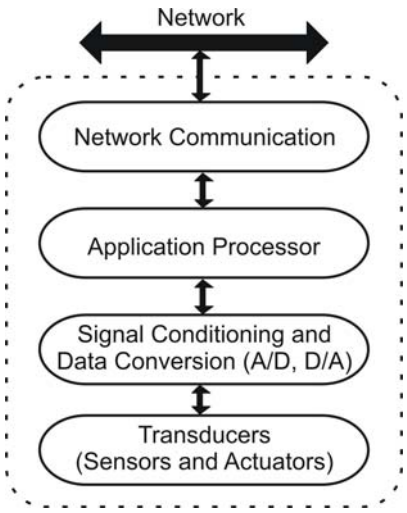

Fig. 1. Smart transducer model

Based on this premise a smart transducer model is shown in Fig. 1. It consists of four parts: transducers (sensors and actuators), signal conditioning and data conversion, application processor, and network communication. The analog output of the sensor is conditioned and scaled (amplified), then converted to a digital format by an A/D converter. The digitized sensor signal is processed by a microprocessor using a digital application control algorithm. The measured or calculated parameters can be passed on the host or monitoring system in a network by means of network communication protocols. In a reverse manner, an actuation command send form a host via the network can be used to control an actuator [9].

IV. Network Connection Possibilities

The International Electrotechnical Commission (IEC) promotes international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, the IEC publishes International Standards. The standard of IEC 60870 applies to telecontrol equipment and systems with coded bit serial data transmission for monitoring and controlling geographically widespread processes. It defines a telecontrol companion standard that enables interoperability among compatible telecontrol equipment. Nowadays the most often used systems for telecontrol are SCADA. As well as standard SCADA data reporting functions, the IEC 60870-5-101 and IEC 60870-5-104 drivers provide slave file transfer functionality to support remote operations. IEC 60870-5-104 protocol operates over IP interfaces. IEC 60870-5-101 protocol provides the same functionality as IEC 60870-5-104, except 60870-5-101 operates over serial lines.

The mentioned above illustrates that a measuring transducer has to provide a digital interface in order to be included in SCADA system, e.g. to be smart. And this interface must give the transducer networking capabilities. So there are two possibilities – serial and Ethernet interface. Depending on the place of the transducer in SCADA at least one of the pointed interfaces is mandatory but generally most of the smart transducers allow as options the both possibilities. While the Ethernet interface has no alternatives the serial one can be organized using different methods. Therefore that using RS-485 the smart transducers can be connected in parallel and thus to build an industrial network this interface is preferred instead of RS-232. So here will be considered some possibilities to provide the transducers with network communication.

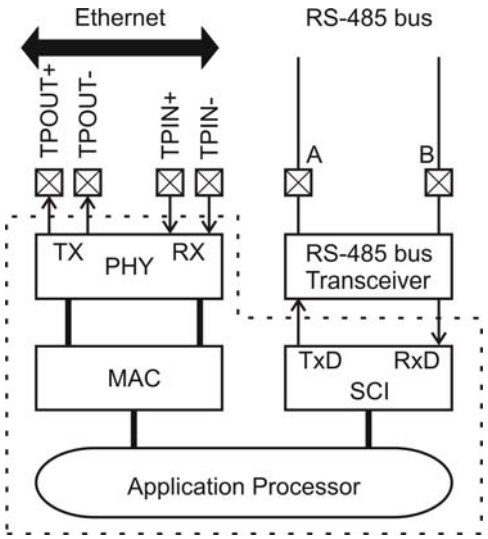

Fig. 2. Smart transducer based on a powerful microcontroller

The first possible model is when the transducer is based on a powerful microcontroller which executes the functions of the application processor and the network communication as it is depicted in Fig. 2. There are various microcontrollers which can be used in this model – for example ARM based microcontrollers LPC1768 of NXP, LM3S6938 of Texas Instruments and etc. They have enough resources to measure the parameters of the power grid – analog-to-digital converters, timer modules, digital inputs and outputs. Also they are supplied with different digital interfaces to maintain the network communications – SPI, I2C, USART and etc. Generically, the USART (Universal Synchronous Asynchronous Receiver Transmitter) is also known as a Serial Communications Interface or SCI. For this example one USART port and an external RS-485 transceiver are used to realize serial communication via RS-485 bus. The Ethernet communication is available too because of the embedded medium access controller (MAC) and physical transceiver (PHY). The system is compact and with low consumption. As disadvantages can be considered difficulties in tasks management which must be had in mind in the software design and also the dependency on only one device which leads to complete failure in case of fault. Nowadays the microcontrollers are reliable enough to minimize the second disadvantage.

Another possible model of a smart transducer is when the structure consists of an application processor based on standard microcontroller which is responsible not only for the signal conditioning, data conversion and parameters

values calculation but for the serial communication as well. An external Ethernet controller is used to maintain the network communication. The block diagram of such model is shown in Fig. 3.

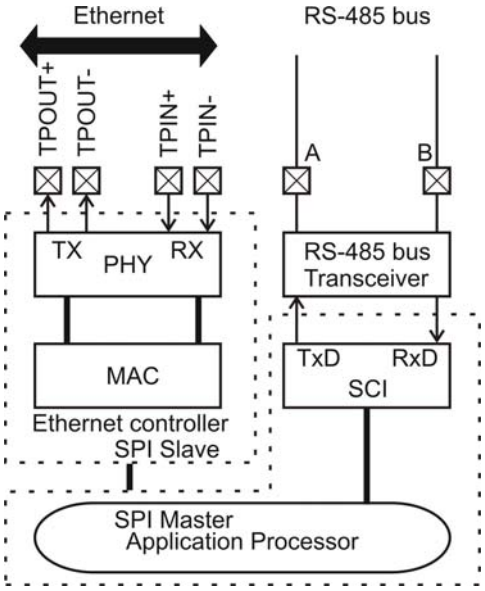

Fig. 3. Smart transducer model using external Ethernet controller

In this example is used external Ethernet controller which transfers information with the application processor using industry standard interfaces – SPI, SCI, I2C. The external controller supports the Ethernet communication. Well known and often used stand-alone Ethernet controllers are ENC28J60 and ENC624J600 of Microchip. Both are IEEE 802.3™ compatible Ethernet controllers fully compatible with 10/100/1000Base-T Networks. They have integrated MAC and 10Base-T physical layer and support one 10Base-T Port with automatic polarity detection and correction. ENC28J60 can communicate with the host microcontroller only via SPI interface with clock speeds up to 20 MHz. It has 8-Kbyte Transmit/Receive packet dual port SRAM. ENC624J600 has 24-Kbyte Transmit/Receive packet buffer SRAM and can communicate with the host microcontroller using 14 Mbit/s SPI interface with enhanced set of opcodes or 8-bit or 16-bit multiplexed or demultiplexed parallel interface. The advantage of the model is that the measurement process and the serial interface are independent from the Ethernet controller. A disadvantage is the delay caused by the communications between the processors. When the data buffer that is transferred is not too big this delay is not significant, especially if the parallel interface is used.

As a new possible model of a smart transducer can be considered the example which is shown in Fig. 4. In this case the application processor deals with the signal conditioning, data conversion, parameters values calculations and the serial communications. It is based on a standard microcontroller with industry standard interfaces – SPI, SCI and etc. The Ethernet communication is assigned to a separate microcontroller with the required capabilities. Representatives of such class microcontrollers are PIC18F97J60 family of Microchip, AX11001/AX11005 of ASIX and etc. The representatives of the PIC18F97J60 family are IEEE 802.3™ compatible Ethernet controllers which are fully compatible with 10/100/1000Base-T Networks. They have 8-Kbyte Transmit/Receive packet buffer SRAM, integrated MAC and 10Base-T physical layer. They support one 10Base-T Port. There are also available SPI, I2C and USART modules. The microcontrollers AX11001/AX11005 are 8-bit pipelined RISC, 100% software compatible with standard 8051/80390. They are fully compatible with 10/100/1000Base-T Networks. 12KB SRAM is dedicated for Ethernet packet buffering. Build in TCP/IP accelerator in hardware improves network transfer throughput. There are SPI, I2C and USART interfaces too. When two microcontrollers work simultaneously the problem with synchronization occurs. One of them must have higher priority and has to initiate the data transfer. As far as the application processor has the leading role in the complex device, it is responsible for the main tasks and is busy more than the communication processor, it has to initiate the data transfer. The advantage is similar like in the previous model. Also the second controller gives more possibilities of the device. The disadvantage caused by the delay needed for the data transfer exists again. It can be overcome using high baud rates in the communications.

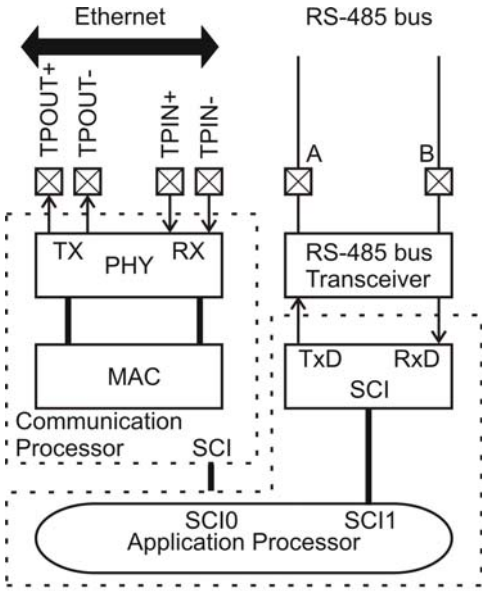

Fig. 4. Smart transducer model using a communication processor

The RS-485 standard is ideal for multi-drop applications and for long-distance interfaces. RS-485 allows up to 32 drivers and 32 receivers to be connected to a data bus, making it an ideal choice for multi-drop applications. Because it is a differential interface, data is virtually immune to noise in the transmission line. That's why it is recommended for energy meter networks, industrial automation and building automation networks. The modern representatives of the RS-485 transceivers are low-power and fast like SP485E of Exar, SN65HVD3082E and etc. of Texas Instruments.

V. SMART TRANSDUCER DEVELOPMENT

On this phase of the project the third model for smart transducer development is chosen and its block diagram is

shown in Fig. 5. Based on the previous experience as application processor is used the microcontroller of Freescale MC9S12A32 [10].

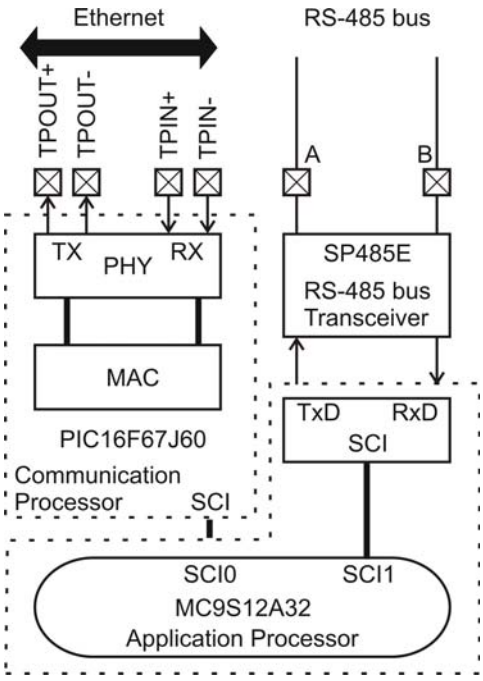

Fig. 5. Smart transducer project development

The communication capabilities are improved by adding a special module which provides standard serial and Ethernet interfaces. As RS-485 transceiver is chosen SP485E and it is connected to one of the available SCI ports. The other one is intended for connection to the communication processor. For this purpose is used PIC18F67J60. Its function is to maintain the Ethernet communications. The serial interfaces operate with 9600 bit/s baud rate. The data buffer which is sent by the application processor is 45 or 55 bytes long according to the concrete purpose of the transducer (Delta or Wye connection).

VI. CONCLUSION

In this paper the objectives, functions and possibilities of the smart transducers are considered. Three models of smart transducer structure are proposed and discussed. For each of them the basic components of the main blocks are proposed. At least two possibilities for choice are presented. On the current phase of the project a smart transducer proposal is developed. Its possibilities are investigated. On the next phase of the project another model might be investigated in order to compare the possibilities of each. The proposed transducers are intended for Internet based SCADA system development.

ACKNOWLEDGEMENTS

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Smart Transducers Network Development Using PLC as a Gateway

Peter Ivanov Yakimov, Atanas Nikolov Iovev and Nikolay Todorov Tuliev

Abstract – **Development a network of smart power transducers is considered in the present paper. The network control is based on PLC as a gateway. The goal is to investigate the communications abilities of standard devices like PLC for use as a gateway in networks of smart power transducers. Thus the application of PLCs in SCADA systems for control power grids will be enlarged.**

Keywords – **Electric power system, PLC, Transducer network**

I. INTRODUCTION

The electric power system (EPS) is a complex which consists of the following subsystems – generation, transmission, distribution and consumption. In every one of them there is a need of transfer specific information. Thus for the generation process like important information is considered the recording key performance and quality of service issues such as scarcity (especially for wind and solar) and generator failures, utilizing the data provided by the market sub-domain to schedule generation and simultaneously provide availability data to the markets and recording the history of device operations and maintenance, and analyze the performance and the life expectancy of devices. The information management part in the transmission subsystem should provide monitoring, information exchange, and control data for operations and control of transmission substations and field devices. This information is generated from widely-deployed measurement and monitoring devices, such as sensors and phasor measurement units [1]. Furthermore, this information should be properly used to manage the operations in the transmission system, including optimizing power flows, improving reliability, and optimizing asset utilization. The task of the distribution subsystem is to deliver the electric energy to the customers. There are performed communications in real time in order to manage the power flows associated with a more dynamic market sub-domain, and hence promptly adjust localized consumption and generation [2]. A large amount of monitoring and control information, including load management and distribution system reliability, should be managed in this subsystem. The consumption is the activity that represents the customers' participation in the electric power system. This is the most important part for which the system is intended. To manage their energy usage, generation, and storage customers need accurate information. It will support the realization of many advanced features, such as remote control, monitoring and control of distributed generation, inhome display of customer usage, automatic reading of meters, and control of new electric devices (e.g. electric vehicles).

To apply a reliable control of all parts of the electric power system new innovative approaches in the automation systems are needed. This will lead to sustainable development of EPS and the energy efficiency increase. Key problem in reaching this goal is intelligent sensor networks development to transfer large amount of data from the system to the dispatch centers for processing and analyzing.

II. NETWORK DEVELOPMENT

One device becomes smart through the integration of embedded processing and the next logical step is remote communication with the smart device [3]. Most of the transducers which are in use in EPS have two types of interface: analog and digital. The output quantities of the analog outputs can be load independent direct current or direct voltage signals. The range of the current outputs may be different - -5mA÷ +5mA, 0mA÷20mA or 4mA÷20mA. Usually the range of the voltage outputs is 0÷10V. The transducers may have several analog outputs. Their number limits the number of the quantities which values can be transmitted. The digital interface gives the transducer the possibility to be included in a network. It is usually serial in order to minimize the number of the wires. The standard is mainly RS-485 or RS-232. There are custom defined interfaces as well. The network can be developed using the well known configurations – star, ring, bus etc. In order to minimize the connections bus topology is suitable and RS-485 has a wide application [4].

The most common used transducers in the electric power system have three phase connection and delta configuration. This system has three wires. The input variables are the line voltages U_{12} and U_{23} and the phase currents I_1 and I_3. This is known as the method with two watt-meters or Aron circuit. The maximal values are 130V and 6A. The data transmitted data buffer contains the values of line voltages (U_{12}, U_{23}), phase currents (I_1, I_3), active power (P), reactive power (Q), frequency (f), ratios of the voltage and current measuring transformers (kU, kI), phase angles of the vectors in relation to U12 (φU_{23}, φI_1, φI_3). The last two bytes contain the checksum (CS) and the value is the sum of the all bytes of the buffer. All quantities except the active and reactive power are transmitted as

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unsigned hexadecimal integer. The length is two bytes and the pattern is 0aaaaaaa, 0bbbbbbb. In this case the values of the quantities have the following accuracy: voltage – 0,1V, current – 0,001A, frequency – 0,01Hz, phase angle – 0,1°. The values of the active and reactive power which have different signs in the four quadrants of the complex plane are transmitted as signed hexadecimal integer. The length is two bytes and the pattern is 0±aaaaaa, 0bbbbbbb. The accuracy is 0,1W or 0,1VAr.

A very important part of the network development is to choose the gateway. This is a circuitry used to interconnect networks by converting the protocols of each network to that used by the other. It enables the connection of different network types within the architecture, or provides a means of transportation of data to different network areas for distribution. For application in EPS it has to be small, rugged, reliable device. Thus the goal of the investigation is to use as a gateway a standard device like PLC. They are reliable devices which have a wide application in automation in the industry and in EPS as well. In addition to their main function to handle analog and digital signals in order to control and monitor different devices from the electric power system their communications capabilities will be used to maintain the smart transducers network. The network organisation is shown in Fig. 1.

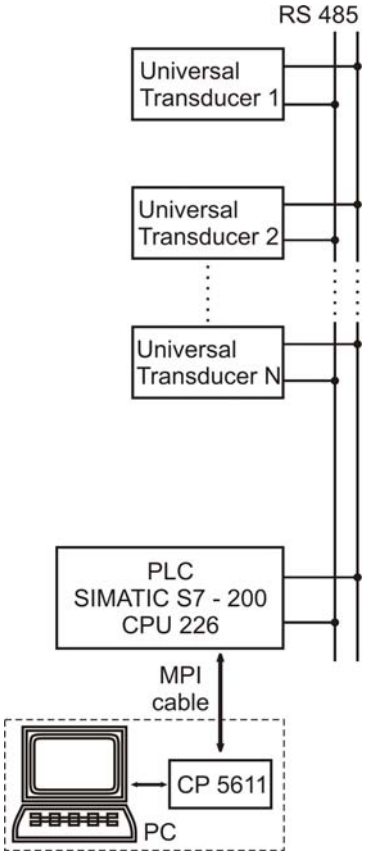

Fig. 1. Smart transducers network organisation

The PLC of Siemens Simatic S7-200 CPU 226 is chosen [5]. It has two ports realizing RS-485 serial interface. Port 0 of Simatic S7-200 CPU 226 is chosen to operate with the transducers network. Port 1 using MPI protocol is intended for connection to the upper level of the SCADA, in this case to a personal computer. It is used as an operator's station in order to observe the information in real time. The collected data can be stored there for post-processing and later visualization. A communication processor module CP 5611 is added to the personal computer which enables it to communicate using MPI protocol.

III. SOFTWARE DESIGN

During the startup initialization the communication parameters for the Port 1 are set: Micro/WIN → CP5611(MPI) interface and 19200 baud rate. This port is provided for programming the controller and receiving the manipulated data from the transducers, which will be displayed on a PC monitor.

The block diagram of a main PLC program is shown in Fig.2.

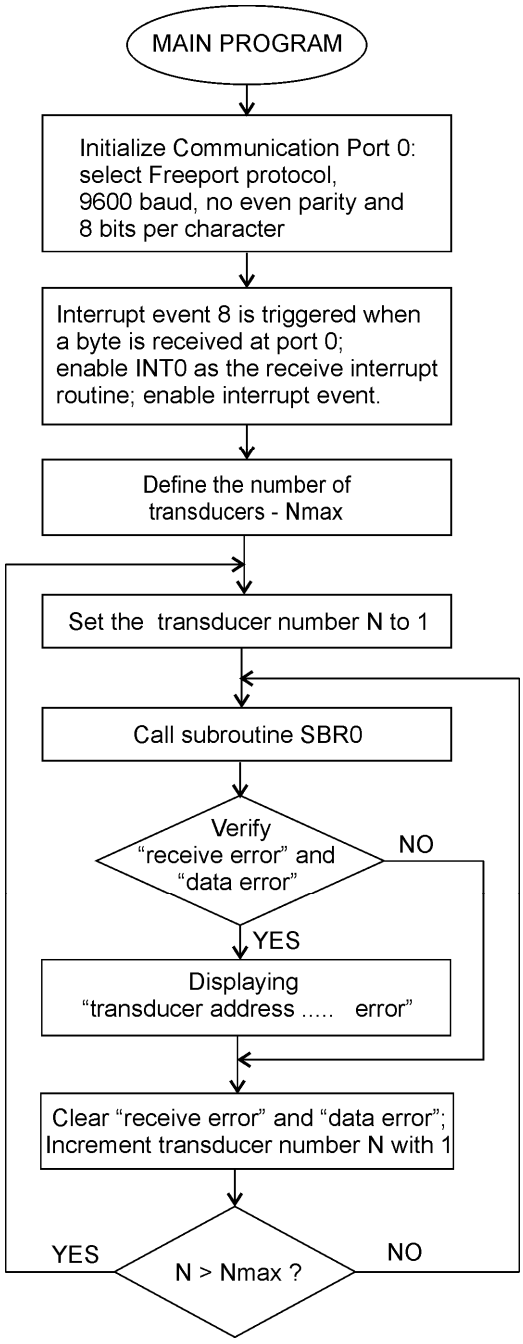

Fig. 2. Block diagram of a main PLC program

For communication port 0 is used Freeport protocol and 9.6 kbaud rate is chosen to correspond to the same value that is used by the transducers.

Interrupt event 8 is attached to interrupt routine INT0 to enable INT0 as the receive interrupt routine. Interrupt event 8 is triggered when a byte is received at port 0. Interrupt events are enabled.

The number of transducers Nmax in the transducers network is defined as the maximum number is 32.

After implementing the subroutine SBR0 are displayed the parameters of the transducers or "error'' signal.

The block diagram of a subroutine SBR0 is shown in Fig.3.

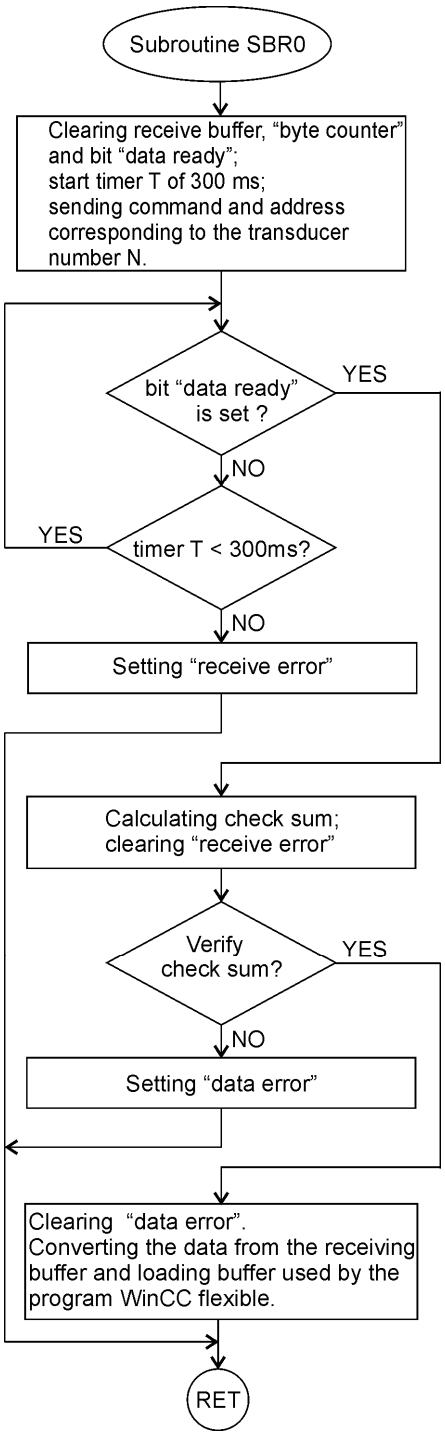

Fig. 3. Block diagram of a subroutine SBR0

In the subroutine is provided a programming timer (On-Delay Timer) representing 300 ms. The timer is starting when command and address corresponding to the transducer with number N are transmitting.

The data are valid if during the time interval from 300 ms the transducer's data are received without "receive error" and "data error".

The measured data except the active and reactive power are received as unsigned hexadecimal integer in two bytes and must be consecutively converted. In order to eliminate unused zeros high byte is multiplied with 256 and low byte is multiplied with 2. Two results are summed and divided by 2.

The equation is:

unsigned integer **K** represented with two bytes

K = ((**high byte**)*256 + (**low byte**)*2) / 2

The values of the active and reactive power which have different signs in the four quadrants of the complex plane are received as signed hexadecimal integer in two bytes.

The equations used to convert data are:

- if the sign is plus:

positive signed integer **K** represented with two bytes

K = (**high byte**)*256 + (**low byte**)*2

- if the sign is minus:

negative signed integer **K** represented with two bytes

K = 16384 - ((**high byte**)*256 + (**low byte**)*2)

Ready data for visualization are stored into a buffer and are intended for the program WinCC flexible.

Interrupt routine INT0 is shown in Fig. 4.

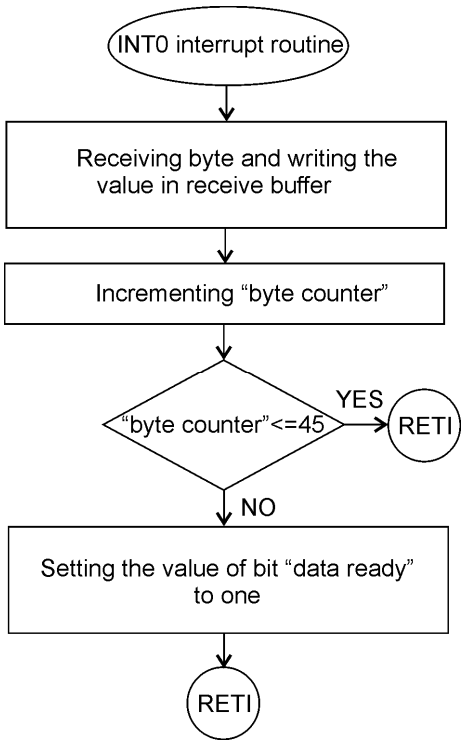

Fig. 4. Block diagram of an interrupt routine.

When a byte is received at port 0, the interrupt routine is executed. Received byte is stored in receive buffer and "byte counter" is incremented by 1. If all of the bytes have been received, the bit "data ready" is set to 1.

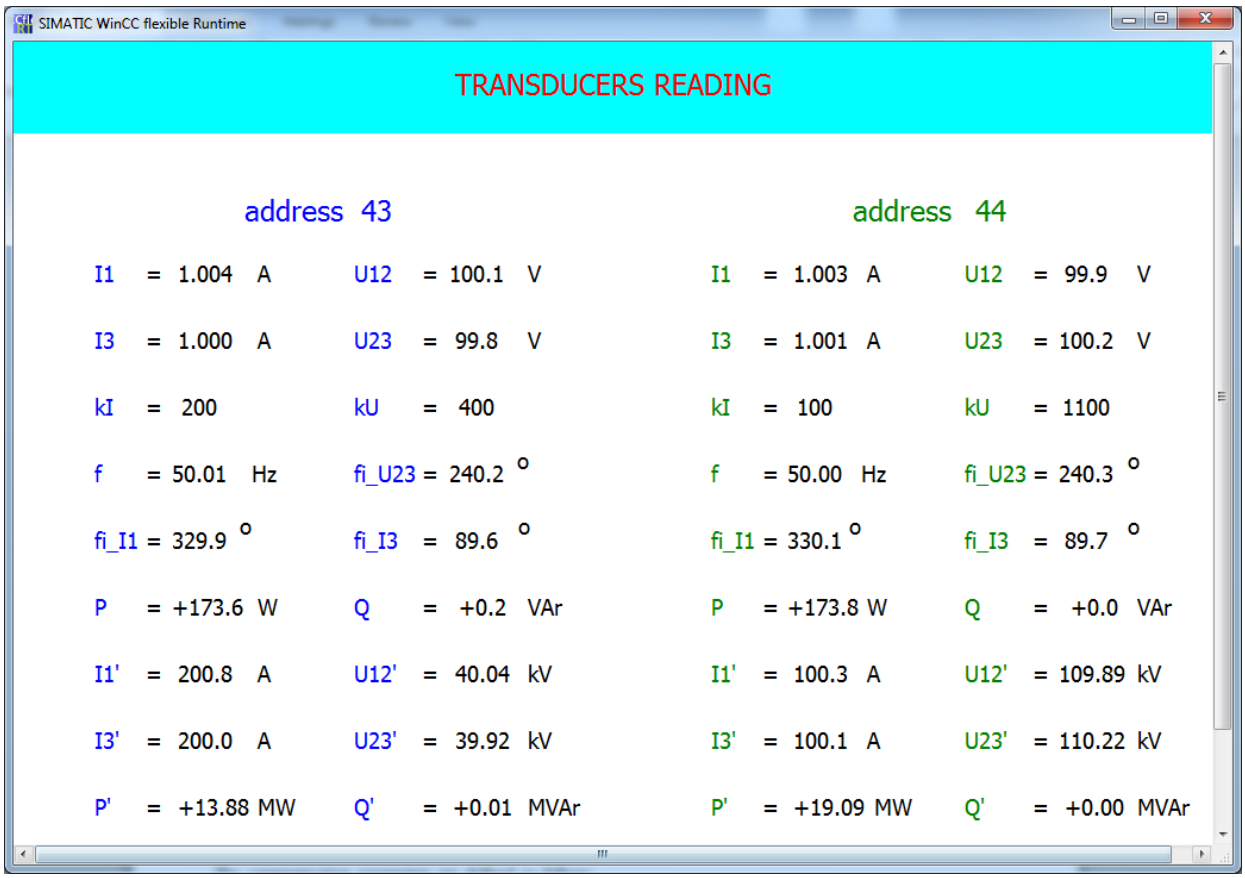

Fig.5. Front panel of two power transducers connected to smart transducers network

The SIMATIC WinCC flexible 2008 programming package is used for visualization of power transducers data. The communication parameters are defined as follows: personal computer as HMI - address 1, interface MPI/DP, baud rate 19200, network profile MPI and communication station SIMATIC S7 200 as a gateway - address 2.

The data of two power transducers with addresses 43 and 44 in transducers network are shown in Fig. 5.

The appropriate tags are developed that give the relationship between the displayed value and the relevant data stored into the buffer for visualization in the PLC memory. The project is starting in runtime mode. The buffer for visualization is updated every second.

IV. Conclusion

A system based on PLC as a gateway in a network of smart power transducers for parameters calculation and monitoring of three-phase power grids is developed and considered in the present paper. The system can capture the signals from the power grid and display the values of active power, reactive power, frequency, voltages and currents, active and reactive energy in four quadrants, phase angles, ratio of transformers and etc. The system can process data of up to 32 power transducers connected via industrial network using standard serial interface RS-485. The functionality of PLCs as components in the automation in EPS is widened. To their main control functions are added the obligations for smart sensors network management. The presented results will be used in further investigation of more complex systems for electric power management.

Acknowledgements

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LabVIEW Based Wireless System for Environmental Monitoring

Georgi Todorov Nikolov, Boyanka Marinova Nikolova
and Elitsa Emilova Gieva

Abstract – **Thanks to miniaturization of the sensors as well as developments in the realm of Wireless Sensor Networks (WSN), the wireless technologies are becoming integral to a number of applications, including environmental monitoring. This paper presents the design and implementation of ZigBee enabled wireless data acquisition system for monitoring of temperature, relative humidity and illuminance. The presented system collects the signals of a number of sensors using the National Instruments' gateway and WSN modules. Finally system interface is designed on the graphical programming software platform.**

Keywords –**Environmental parameters, LabVIEW, WSN.**

I. INTRODUCTION

In the last few years in electronics and wireless communications have progress. The networks are developing and become more inexpensive, with a lower power consumption and the sensors become more multifunctional. These sensors are small in size, with good sensitivity and easy process and transmit data one to another. They communicate typically over an radio frequency channel. Sensor networks are designed to detect and registrate different events or phenomena, to collect and process data and transmit the information to the final consumer or interested users. Main characteristics of the sensor networks are [1]:

- The opportunity to organize themselves;
- Short-range broadcast communication and multihop routing;
- Dense deployment and cooperative effort of sensor nodes;
- Frequently changing topology due to fading and node failures;
- Energy limitations, as well as energy for transmission of information, memory and computing power.

These characteristics, particularly the last three, make sensor networks different from other wireless ad-hoc or mesh networks. Clearly, the idea of mesh networking system is not new; it is assumed for some time for wireless internet access or voice communication. Similarly, small computers and sensors are not innovative per se. However, the combination of small sensors, computers with low power consumption and transmitters makes it possible to create a new technology platform that has many important applications. Research and commercial interest in wireless sensor networks is now growing exponentially, that occurs in many ways [2, 3, 4]. Wireless sensor networks are increasing wide application in different fields and have several advantages over standard sensor networks [4, 5, 6].

In this paper is presented an application of wireless sensor network for environmental monitoring. An introduced wireless system is built with sensor modules from National Instruments and is controlled in LabVIEW programming environment. In LabVIEW are mounted a wide variety of technologies for creating distributed applications. One of this technologies is the shared variable, with which is possible to share data between loops on a single diagram or between applications across the network. To receive data from wireless sensor modules is used just a shared variables. The luck of this technology is necessity of a project open in the Project Explorer window. In this paper is presented different approach to communicate with wireless sensor nodes by using specific application programming interface. With this approach is possible to implement standard programming techniques to create wireless applications.

II. DESIGN CONSIDERATIONS FOR HARDWARE IMPLEMENTATION

A. Ethernet Gateway

The Ethernet Gateway is a pass - through device that coordinates communication between wireless measurement nodes and the host controller [7]. In present work the National Instruments' WSN-9791 Ethernet Gateway is selected. This gateway has a 2.4 GHz, IEEE 802.15.4 radio, based on ZigBee specification and provides connectivity to a Windows via Ethernet port. The gateway can be connected up to 36 measurement nodes and has outdoor range up to 300 m.

B. Wireless Measurement Nodes

There are various type of measurement nodes manufactured by National Instruments. Each measurement node has four analog input channels and up to four digital input/output channels [8]. The analog channels provide direct sensor connectivity while digital channels can be configured for input, sinking output, sourcing output, or

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programmatic control. Block diagram of such wireless node is shown on Fig. 1.

A low-power microprocessor is MSP430 from Texas Instruments. This microprocessor delivers operation and control of the measurement nodes. The nodes are powered with four 1.5 V AA battery for up to three years of operation or can be used external power with a DC supply. Up to eight end nodes for star topology or 36 measurement nodes in a mesh topology can be connected to a gateway.

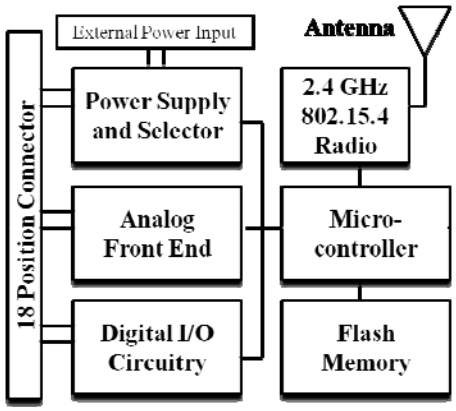


Fig. 1. Block diagram of the wireless sensor node

In order to demonstrate capability of such wireless sensor network in present project are selected two NI WSN 3212 nodes and one NI WNS 3202.

The NI WSN-3212 measurement node provides four thermocouple input channels with 24 bit resolution. It is compatible with all thermocouple types and according selected type can be configured to indicate directly temperature in degrees Celsius.

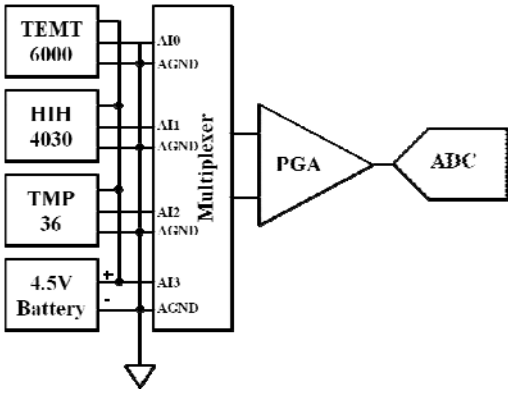


Fig. 2. Sensors connection to the analog circuitry

The NI WSN - 3202 measurement node is a wireless multifunction data acquisition system [8]. This device provides four analog input channels with four selectable nominal input ranges: ±10 V, ±5 V, ±2 V and ±0.5 V. The resolution of analog to digital converter is 16 bit with minimum sample interval of 1 second per channel. Input impedance of each analog channel is greater than 1 GΩ and input bias current is less than 3 nA. Crosstalk between channels is greater than 100 dB.

The connection between voltage signals, generated from sensors and analog inputs of the NI WSN – 3202 is shown in the Fig. 2. Each channel has a terminal for voltage signal and a AGND terminal which is internally connected to the ground reference. The voltage signals are multiplexed, filtered, conditioned and sampled by an analog to digital converter.

C. Sensors for Measuring Environmental Parameters

TEMT6000 Ambient Light Sensor

Measurement of illuminance can be achieved by ambient light sensor TEMT6000 and 10 kΩ load resistor between emitter and ground. TEMT6000 is a phototransistor sensitive to the visible spectrum. Sensor acts like a transistor and its sensitivity is a function of the collector–base junction quantum efficiency and also of the dc current gain of the transistor [9]. Therefore, the greater the incoming light, the higher the analog voltage on the output.

In order to define transfer characteristic of the sensor a number of calibration procedures was done using lux meter. After regression the derived polynomial equation is:

$$l = -46.73V_O^3 + 366.8V_O^2 - 76V_O + 15{,}7\,, \quad (1)$$

where l is luminance in lux, V_O is output voltage from voltage divider between emitter and resistor.

HIH-4030 humidity sensor.

The HIH-4030 is an integrated humidity sensor that measures relative humidity and delivers it as a corresponding analog output voltage [10]. The output of the sensor can be connected directly to an analog to digital converter. The sensor has near linear voltage output, and the voltage is very easy to convert to percentage of relative humidity using the equation:

$$RH = \frac{\frac{Vout}{Vs} - 0.16}{0.0062}. \quad (2)$$

where RH is relative humidity in percentage, V_{out} is output voltage and V_s is supply voltage.

Optimal supply voltage of the sensor is 5 V and a maximum consumption is about 500 μA.

Temperature Sensors TMP36

The precision temperature sensors TMP36 provides a voltage output that is near linearly proportional to the Celsius temperature. The transfer characteristic, derived from [11] is:

$$T = \frac{V_0 - 0.10.16}{0.01} - 10. \quad (3)$$

where T is temperature in degree Celsius, V_0 is the sensor output voltage.

This sensor, without any external calibration provides accuracies of about ±1°C at room temperature. The TMP35 has low voltage supply operation from 2.7 V to 5.5 V. Its supply current is less than 50 μA, that make the sensor very suitable for wireless applications. In addition, its low output impedance and linear output simplify interfacing to analog to digital converter.

III. SOFTWARE DEVELOPMENT

Once configured with wireless network, the measurement nodes are automatically added in the

LabVIEW Project and give immediate access to their Input/Output variables and properties. They uses a particular type of protocol called NI Publish-Subscribe Protocol (NI-PSP). The I/O data can be accessed using static I/O variables from the LabVIEW Project tree or programmatically using DataSocket functions or Shared Variable functions. The Uniform Resource Locator (URL) format is the following:

ni.var.psp://gateway/node/channel,

where gateway is the IP address of the Ethernet Gateway, node is the WSN node name and channel is the I/O variable name. The default node name is NodeX, where X is the number assigned when the node is added to a LabVIEW Project. Default I/O variable names depend on the measurement node type and become active after the project is deployed to the gateway. For NI-3202 Voltage Node default names for analog inputs are AI0, AI1, AI2, AI3, and for digital inputs the default names are DIO0, DIO1, DIO2, DIO3. For NI-3212 Voltage Node the default names for thermocouple inputs are TC0, TC1, TC2 and TC3.

A National Instrument's Wireless Sensor Networks use LabVIEW shared variable engine to get data to and from each sensor node via a Ethernet Gateway. A simple approach can be to use network shared variables on block diagram by drag the I/O variable directly to the block diagram, create an indicator, and click *Run* for execution. This approach, however can cause for a complicated block diagram if there are a large number of I/O points.

In present work a different approach is suggested, where NI WSN IOV Application Programming Interface (API) is used. An API, is a set of functions that interfaces to some set of underlying code that already exists. By using API, a developer can programmatically access existing functionality within their own application. Usually an API includes functions such as Start, Read, Write, Stop, Close etc. In such way, the user does not care about what happens inside of the subVIs, because they complete the function that they want.

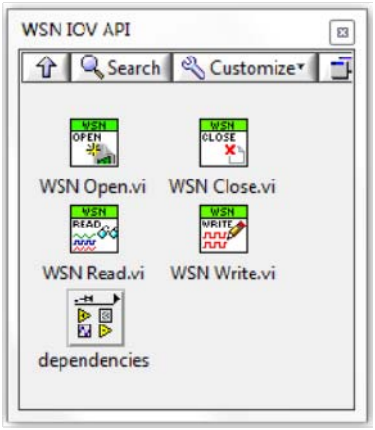


Fig. 3. WSN IOV API function palette

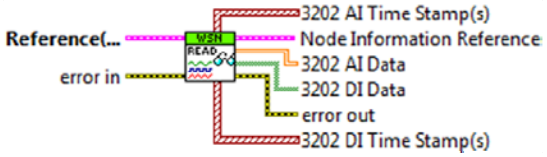
WSN IOV API can be downloaded from [13] and allows users to send and return data from a sensor network without having to use network shared variables on the block diagram. It is possible to pull back data from multiple nodes using an initialize, operate and close type of architecture. This high level application programming interface is built on the shared variable function and WSN Host API and can underhanded discover all nodes and measuring points in the wireless sensor network.

The WSN IOV API palette is installed in the User Libraries function palette and contains only four functions.

1. WSN Open.vi

This function opens a reference to the gateway and references to the analog and digital shared variables for each wireless node. If no nodes are found the function returns an error. Before using the function wireless sensor nodes must be added to a Ethernet Gateway in Measurement and Automation Explorer. The default names for a reference to variables must not be changed.

2. WSN Read.vi



This is polymorphic function that allows users to select what type of nodes (NI WSN 3202 or NI WSN 3212) and data to read. There are the ability to read analog data, digital data or both analog and digital data from all nodes. The function returns one dimensional array of data when configured for one node and two dimensional array of data when configured for multiple nodes. If shared variables have not been deployed or if a corresponding node has dropped off the network the function returns no data.

3. WSN Write.vi

Like the Read function, this function is based on the polymorphic instance of the VI and writes digital data to network published nodes. This VI writes one dimensional Boolean data when configured for one node and two dimensional data when configured for multiple nodes.

4. WSN Close.vi

This function closes references to all open nodes and network published variables. The function will not execute if no nodes are found by function Open.

Using described API functions and a scalable architecture it is easy to expand applications and decrease development efforts when new features is added.

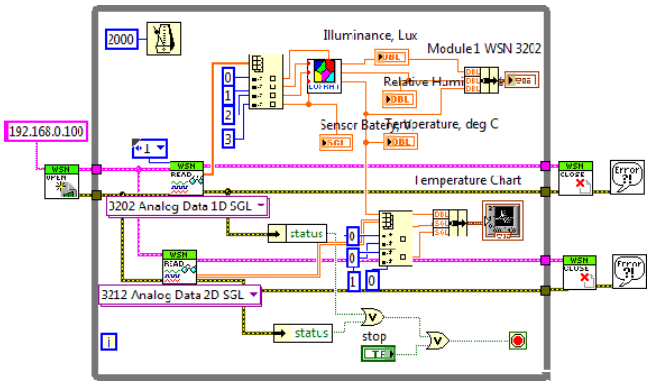


Fig. 4. Block diagram of the developed software.

The presented graphical program code or so called block diagram is shown in Fig. 4. Instead shared variables to be dragged and dropped to the block diagram form a LabVIEW project in the developed graphical code, as can be seen from figure, the data from wireless system is read in usually way. Follow the standard architecture for data acquisition system the first called function is to open a reference to the gateway. The code for reading and data manipulating is written in a while-loop. There are two Read functions. The upper one returns one dimensional data array from NI WSN 3202 with each row corresponding to one of sensors from Fig. 2. Voltage measurement from sensors is converted to illuminance, relative humidity and temperature measurements by equations from (1) to (3). The lower Read function returns 2D arrays of analog data with each row corresponding to one NI WSN 3212 node. These nodes returns data in degree Celsius. For each variable is created corresponding indicators. The last two functions are Close and Simple Error Handler. These functions terminate software connection to the WSN and indicates whether an error occurred.

IV. Experimental Results

In order to illustrate performance of the developed LabVIEW based WSN a number of experiments was done. Front Panel of the system is shown in Fig. 5.

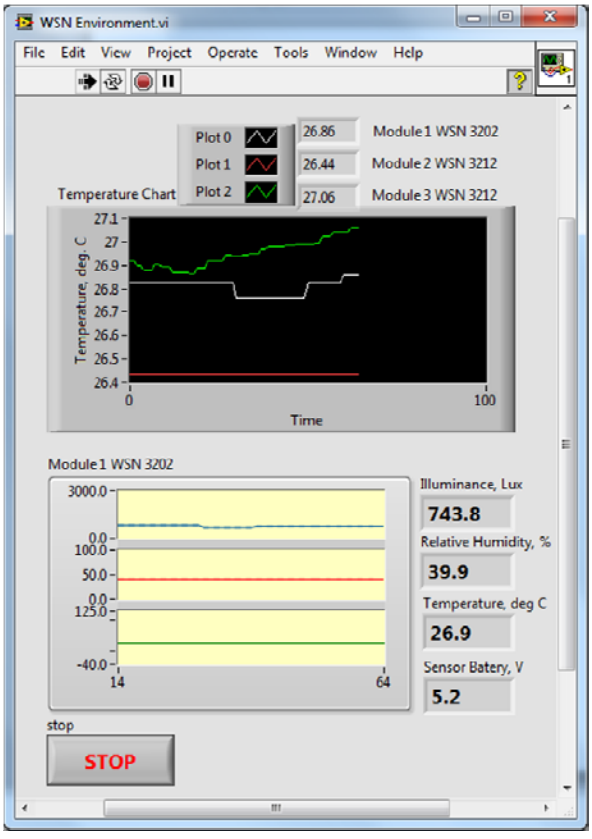


Fig. 5. The Front Panel of the WSN for Environmental Monitoring

There are temperature chart with three plots, that display temperature from three different wireless measurement nodes from three different places. The first one (white plot) displays temperature from TEMT6000 sensor and NI WSN 3202 node. The other two temperature (green and red) are measured by J-type thermocouples from two NI WSN 3212 measurement nodes. In the lower part of the Front Panel are placed indicators for illuminance, relative humidity, temperature and voltage of external battery.

V. Conclusion

In presented work is described design and implementation of a wireless sensor network for environment parameters monitoring, based on LabVIEW graphical system-design platform and measurement nodes from National Instruments. With introduced approach that suggest to use WSN IOV API, wireless system is easy to deploy, configure and get data from different sensors. The advantages of WSN based system according the conventional measurement method is in terms of cost, portability and reliability. In addition the developed ZigBee and LabVIEW based WSN provides mobility and networking capabilities. Graphical user interface and advanced signal processing functions distinctive for LabVIEW contributes for additional benefits.

The presented wireless sensor network for environmental monitoring can be used as for measurement of different environmental factors as for educational purposes.

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Wireless Sensor Network-based Illumination Control

Marin Berov Marinov, Georgi Todorov Nikolov and Borislav Todorov Ganev

Abstract – **In this paper the problem of illumination control in a lighting system with networked lighting devices is examined. The luminaries have fluorescent light sources dimmable by a local controller. The optimal dimming values are calculated according to the user and legal requirements for illuminance of different workspaces and their actual illumination levels are measured by light sensors. A closed-loop lighting device control algorithm is used for obtaining the set illumination values. So a distributed and energy optimised illumination control with the use of daylight can be effectively implemented. The proposed approach is evaluated in lecture rooms and office environments.**

Keywords – **lighting control, daylight adaptive lighting, wireless communication, distributed lighting systems, LabVIEW.**

I. INTRODUCTION

Currently, electricity consumption for lighting in residential, commercial and industrial buildings accounts for about 15% of the total electricity consumption in the European Union. Over the past two decades, the lighting industry has developed new technologies that have greater potential for savings in lighting.

Innovative systems for indoor lighting can work over three times more efficiently than existing ones and with significant amounts of daylight, up to 75% of the electricity can be saved. Studies show that the full potential for energy saving can be realized only with the implementation of complex solutions using not only modern lighting, but intelligent control systems with sensors for light, motion, presence and others [1, 2, 3].

The use of wireless networks in the implementation of intelligent lighting systems is gaining ground as a promising approach. Numerous studies have shown the benefits of wireless sensor networks in the implementation of modern systems for lighting control [4, 5].

In recent years the application of wireless sensor networks for intelligent illumination control is becoming more popular. There are different illumination control approaches discussed in the literature depending on the architecture, connectivity and control strategies. Some of the first applications implemented on the basis of the DALI (Digital Addressable Lighting Interface) bus were presented in 2005 by O'Reilly et al. [6]. Park et al. defined some of the basic user requirements and their impact on energy efficiency [4]. Wen et al. presented an intelligent daylighting system with fuzzy rule-based sensor validation and fusion control [7].

The rest of this text has been organized in the following manner: Section II gives a brief overview of the standards for illumination levels in different workspaces. In Section III we propose a simplified system model and in Section IV the architecture of the intelligent illumination system. In Section V we present some experimental/prototyping results. The paper closes with Section VI, which summarizes the main points and provides an outlook for further work.

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II. STANDARDS FOR INDOOR ILLUMINATION LEVELS

The leading international organization in the field of coordinating the management of lighting standards is CIE (Commission Internationale de l'Eclairage). The CIE has published a lot of recommendations for indoor lighting and contributed to the joint ISO-CIE standard ISO 8995-1 which deals with indoor working places [8]. CIE requirements have been interpreted in a different way in different countries. They are the basis for the current European standard EN 12464-1:2002: Light and lighting. Lighting of work places. Most recommendations in this standard include specifications about:

- Minimum illuminance levels on work planes;
- Minimum illuminance when working on computers;
- Minimum illuminance in the surroundings;
- Luminance ratios near task areas and some other parameters [9].

These specifications are essential and are related to the minimum quantities of light in the rooms and in task areas and surrounding areas, recommendations for glare etc. They are used to define the illumination levels in the different working zones and can be summarised as follows:

- The minimum illuminance levels on work planes for lecture rooms, offices, drawing and conference rooms vary from 200 to 500 lx.
- The recommendations concern the minimum horizontal and vertical illuminance levels, but do not take into account the luminance of computer screens.

III. MODEL OF THE SYSTEM

The proposed system assumes that the information about the presence or absence of users in the different zones and

the illuminance level that have to be achieved there is specified.

For the purpose of this study we use a (model of a) lecture room with N dimmable fluorescent lighting devices arranged in R rows and C columns. An example of such configuration with $N = 12$ lamps arranged in $R = 2$ rows and $C = 6$ columns is shown on Fig. **1**. The workspace plane is parallel to the ceiling and it is assumed that it is divided into the equal number N corresponding zones $z_i,\ i = 1 \dots N$. In each zone a light sensor s_i is mounted.

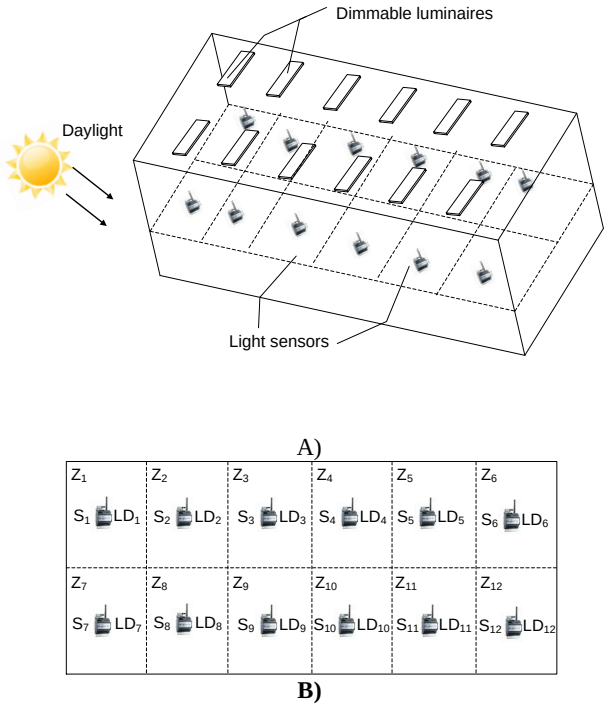


Fig. 1. A) Model of a lecture room environment with networked lighting devices, B) Zoning scheme.

The lighting devices are labelled $LD_i, i = 1 \dots N$. They are networked over a DALI bus and have a fluorescent light source(s) and local dimming controller.

The dimming settings for each local controller are set so that the required illumination level in each zone is reached using gathered information about the illuminance in the corresponding zone and current dimming settings of the local and the neighbouring controllers.

A. Illuminance measurement

The sensors in the system periodically report the measured illuminance. The illuminance sensed by sensor $s_i, i = 1 \dots N$ is marked as $e(s_i)$. It has two basic components: luminance from the lighting devices and daylight.

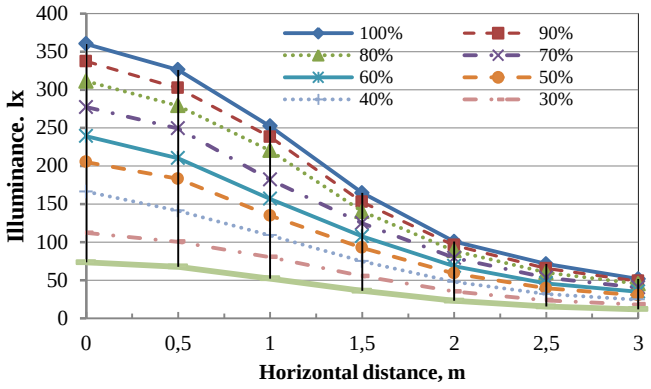
We denote with $e(LD_i)$, the component of the illuminance, contributed by device LD_i.

On the basis of the above notations for the purposes of simplification we can define the following vectors for the measured illumination and for the illuminance contributed by the lighting devices as:

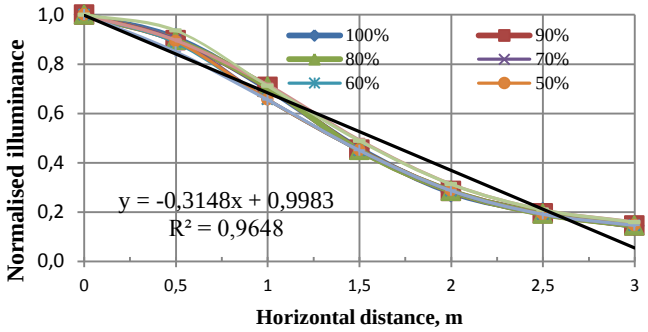
$$E_s = [\, e(s_1), e(s_2), \dots, e(s_N)]^T$$
$$E_{LD} = [\, e(LD_1), e(LD_2), \dots, e(LD_N)]^T \quad (1)$$

B. Computing E_{LD} and the dimming settings for the light sources

The E_{LD} values cannot be determined directly. For estimating them we use an experimental approach proposed by Pan et al [10]. If there is only one lighting device switched on and there is no daylight we can measure the illuminance in the corresponding zone and in the neighbour zones at different distances with fixed sensors and a mobile sensor. It can be seen in Fig. 2.a that the illuminance measured by the sensor in the zone degrades with the distance in a coherent way with the different dimming settings (20 – 100%). Measured results can be normalised with respect to the maximum values for light at a horizontal distance of 0 m. After normalisation it can be seen that the degrading trends are almost the same. The dependence of degradation of the distance from the light source can be determined analytically with sufficient accuracy (using regression - see Fig. 2.b – linear trend line with coefficient of determination $R^2 = 0{,}9648$).



a) Measured illuminance



b) Normalised illuminance

Fig. 2. Experimental evaluation of illuminance degrading with the distance from the light source.

Using this experimental approach, if we assume that the impact factor of the lighting luminaire LD_i on the luminance sensed by the corresponding fixed sensor in the zone $e(s_i)$ is 1 ($w^i_{LD_i}$), the impact factors of LD_i on any other sensor $s_j, j = 1 \dots N$ can be defined as a weighted factor w^i_j, where $(0 \le w^i_j \le 1)$. At the end we can achieve a normalised NxN Matrix W_N with all impact factors:

$$W_N = \begin{bmatrix} w_1^1 & w_1^2 & \cdots & w_1^N \\ w_2^1 & w_2^2 & \cdots & w_2^N \\ \vdots & \vdots & \ddots & \vdots \\ w_N^1 & w_N^2 & \cdots & w_N^N \end{bmatrix}. \quad (2)$$

Illuminance is additive and at a given point it is the sum of the illuminances from every luminaire in the room [11]. So the illuminance measured by the fixed sensor in every zone is the sum of the illuminances from the luminaire in the corresponding LD_i zone, from the neighbouring luminaires and daylight.

The daylight illuminance, measured by the fixed sensors can be written as $Nx1$ column vector E_{Day}. So the illuminance sensed by the fixed sensor can be written in a matrix form:

$$E_S = W_N \cdot E_{LD} + E_{Day}. \quad (3)$$

Equation (3) can be rewritten as

$$E_S - E_{Day} = W_N \cdot E_{LD} \Longrightarrow E_{LD} = W_N^{-1}(E_S - E_{Day}). \quad (4)$$

Here the normalised Matrix W_N with the impact factors can be measured a-priori at the design stage, the E_{Day} vector can be measured after switching all lighting devices off.

The computational complexity is $O = N \times N$ but can be significantly reduced because of the zoning concept used in lighting system design. It specifies that the luminaire significantly influences the illumination in the corresponding zone and a small area around it. As it can be seen in Fig. 1.b the LD_1 luminaire has a larger influence on zone z_1 than on zones z_2, z_7 and z_8. So, on the basis of the established dependence of illuminance degradation on the distance an appropriate threshold can be set and all impact factors bellow this threshold do not have to be calculated.

Finally, the dimming levels for all luminaires can be estimated on the basis of the calculated values for E_{LD}. The dimming levels are set via a set of standard DALI commands.

In the DALI standard the intensity of radiation is set by 8-bit integer. The 0 value means that the source is not switched on, 1 corresponds to 0.1% intensity and the value 254 corresponds to 100% intensity. The dependence of the light intensity of the set numeric value is logarithmic, but because of its specifics the human eye perceives it as linear [12]. It is assumed, that for each lamp a dimming value d is set. So for the j-th lamp the set value is given by d_j, where $0 \leq d_j \leq 254$. In case of N lamps we have a $N \times 1$ dimming vector for the light system given by

$$D = [d_1, d_2, \dots, d_N]^T . \quad (5)$$

IV. Architecture of the Intelligent Illumination System

The system architecture and the main components of the implemented intelligent light control system are shown in Fig. **3**. It can be divided into three main parts: control host, lighting controller with DALI interface and wireless light sensor network.

A. Control host

The control host is implemented in LabVIEW programming environment. It consists of 3 main components:

1) User interface for system parameter configuration and wireless sensor network management and monitoring.

2) Sensor data handler for processing the sensor data and providing them to the control algorithms.

3) Dimmer handler which serves as the interface between the control host and the local dimming controller.

B. Lighting controller with DALI interface

In general, DALI is an industry standard that forms the basis for the unification of components and ensures full interchangeability of products from different manufacturers. In it each actuator has its own address, which receives commands and returns information about its current state. A significant advantage of the DALI system is the ability to obtain feedback about the operation of the light sources. As for the control function, it obtains feedback about: on/off state of the light source, lamp failure, absence of ignition, overheating ballast defects and other faults of the luminaries. Data is transmitted via a dedicated two-wire line with the maximum length between two devices not exceeding 300 m. The interface is bidirectional with a data transfer speed at 1,2 kbps.

A lighting controller is implemented and it is based on programmable logic controller 750-881 of the WAGO company and is equipped with 750-641 DALI / DSI module [13]. Its main tasks are to set the appropriate dimming levels and to obtain feedback about the operation of the light sources.

C. Wireless light sensor network

Our sensor nodes are developed using NI-WSN9791for the wired part of the communication and NI-WSN3202 for the wireless part together with an integrated Ambient Light Sensor TEMT6000 [14].

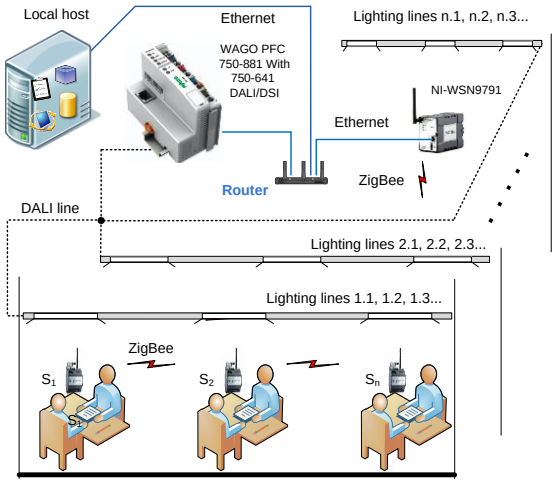


Fig. 3. System architecture.

V. Prototyping Results

In order to illustrate the applicability and capacity of the wireless system presented here, a number of experiments were done.

The LabVIEW block diagram of the software implemented for WSN and illumination control is shown in Fig. 4. In this work the producer/consumer design pattern is selected as base software architecture. This design pattern is a pre-designed solution which separates the two main

components by placing a queue between different loops, which allows the producers and the consumers to execute in different threads. With the producer/consumer design pattern the user can easily handle multiple processes running at different speeds. Communication between the processes is buffered using data queues.

In Fig. 4 the upper loop acts as a producer. In the upper left corner of the Event Structure is positioned a Shared Variable AIO, which communicates with one of the wireless modules. In this Shared Variable is stored the current measured data of illuminance. If the measured illuminance value is greater than desired, the producer loop "enqueued" command and data to the consumer loop to decrease the intensity of radiation of a luminaire and vice versa.

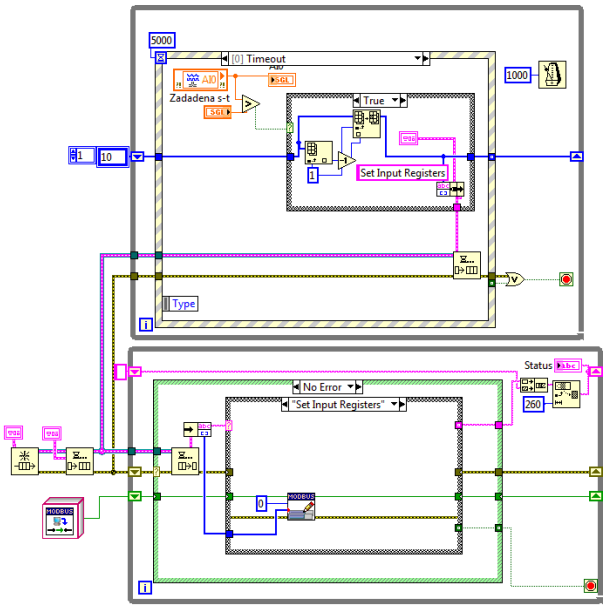


Fig. 4. The LabVIEW block diagram for WSN control and Modbus communication.

The lower loop acts as a consumer and its main function is to provide communication information via the DALI interface. The communication is developed by a set of functions from Modbus Library for LabVIEW programming environment. This library consists of a number of Virtual Instruments that provide communication from any standard Ethernet port, implement тхе Modbus software protocol and offer functionality to both, master and slave. Fig. 5 shows one of these Virtual Instruments that writec тхе data into тхе input registers of a Modbus device.

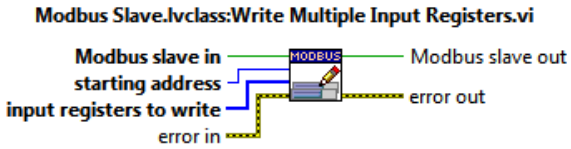


Fig. 5. A Virtual Instrument from Modbus Library for LabVIEW

VI. Conclusion

The combination of optimizing user comfort, meeting illumination levels requirements and employing strategies for energy saving is a task of an enormous economic importance. In this paper we presented a WSN-based illumination control system based on the zoning concept and daylight use. On the basis of the device control and illumination control algorithms presented here the required illumination levels in the different zones can be dynamically controlled and energy consumption optimised. The proposed hardware solutions are verified by real implementation in a lecture hall environment. The experimental results verify the feasibility of the presented approach.

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Alternating Current-Driven Strain-gage Bridge Amplifier System for Brushless Motors Torque Measurement

Nina Jetchkova Djermanova, Marin Berov Marinov and Borislav Todorov Ganev

Abstract – **An alternating current (AC) driven strain gage bridge amplifier system is developed for torque measurement in a brushless motor test bench. AC excitation of the strain gage bridge is applied instead of commonly used DC voltage, and an AC-signal conditioning dual-phase lock-in amplifier is developed using AD630 balanced modulator-demodulator for synchronous detection together with three-pole active Butterworth filter. Thus, lower levels of excitation voltage and lower self-heating of the strain gages are achieved allowing for measurements in very low ranges with high resolution (of about 0.1microstrain/0.05μV/V). The measurement system is controlled in a LabVIEW programming environment through high resolution data acquisition (DAQ) system. Additionally, in the test bench the angular velocity of the mechanical shaft and electrical power data are measured. So the mechanical power data can be compared in real time with the energy consumption and other significant variables. Using this "Power Efficiency" information a number of optimization problems can be solved.**

Keywords – **Brushless motors, Torque measurement, Lock-In amplifier, Power measurement, LabVIEW.**

I. Introduction

The use of mechanical systems driven by electric motors in different production and transportation processes accounts for over two thirds of the electricity consumed by industry [1]. Brushless motors offer several advantages over brushed DC motors, including high torque to weight ratio, more torque per watt (increased efficiency), increased reliability, reduced noise, longer lifetime (no brush and commutator erosion), elimination of ionizing sparks from the commutator, and overall reduction of electromagnetic interference [2]. Because of their high power density, good speed-torque characteristics, high efficiency and wide speed ranges at low maintenance costs brushless motors are widely used in industrial applications where high efficiency in converting electrical into mechanical energy is aimed at. Measuring the torque of these motors is one of the tasks performed on a diagnostics bench when efficiency and power losses have to be evaluated.

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The development of modern industry requires more precise tools for test and measurement. This trend is reinforced by the ever stricter legal requirements for low pollutant emissions. Reliable and reproducible detection of relevant measurement variables is becoming increasingly important. A key part of all these studies and optimizations, particularly in the development of engines and transmissions, is the measure of torque, which together with the rotation speed is a measure of (mechanical) power. The processes are dynamic and the interplay of the units such as the engine and transmission is increasingly becoming the focus of optimization [3].

II. Torque and Mechanical Power Measurement

Torque, being an important factor in the performance of production machines, is measured so that equipment failure is identified and critical situations in important production processes are prevented. A moment is called a torque if its axis corresponds to the axis of rotation defined by the design of the machine concerned. In the case of the moment that results from the action of a single force when the axis of rotation is defined, the computation includes not only the length of the lever arm but also the angle between the lever arm and the force.

For torque measurements, there are numerous applications in the fields of testing technology, operational and process monitoring, automation technology, quality assurance, and research and development. The measurement of true mechanical torque and power on rotating shafts allows users to optimize energy efficiency by first verifying the true power output of the motor(s) and then comparing the energy consumption to motor power output. The precise measurement of torques of rotating parts in particular, is a serious challenge for test equipment manufacturers and users. The current trend is towards looking for opportunities to improve mechanical power and performance by increasing the rotation speed.

There are basically two different approaches of determining the torque: the direct and the indirect method.

A. Direct measurement the torque action

In this method the torque is detected in the rotating strand. Often the term in-line torque measurement is used. Figure 1 shows the principle of action torque measurement. The classic product groups are torque transducers, hubs and flanges [3].

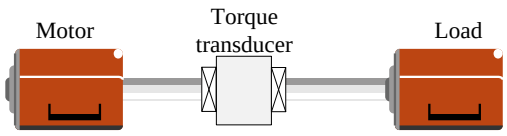

Fig. 1. Measuring the torque action [3].

B. Measuring the reaction force on the lever arm

The method of reaction force measurement, according to the principle action torque is equal reaction torque, is very often used for power determination. The acting at the end of the lever arm force is measured by a load cell. If there is a transmission between the transducer and the point of the powertrain, where the torque is to be actually detected, the transmission ratio must be taken into account by the choice of measuring range and the scaling of the measuring amplifier

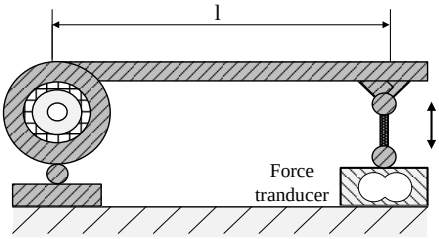

Fig. 2. Measurement of the reaction force with strain gauges (SG).

Today the most common way is to measure the deformation with strain gauges (SG) where their change in resistance is a measure of the strain. Torque sensors consist of main elements spring body with strain gauges and compensation elements, as well as adaptation parts for torque introduction and outtake (Fig. 2) [4, 5].

The techniques widely used for torque measurement apply full Wheatstone strain-gage bridge with an appropriate signal conditioning. Stability, accuracy and high resolution are among the major instrumentation requirements when making motor diagnostics and measurement. Usually a DC voltage is used to power the Wheatstone strain-gage bridge, with a precision instrumentation amplifier connected to the bridge output. High CMRR and low-noise input voltage are must features of the amplifier when striving for high resolution at low strain deviation. Offset drift, 1/f noise, and line noise often impede the measurement of DC signals, hence high precision cannot be achieved [6, 7]. One solution is to use an AC signal to excite the bridge. A bridge amplifier is essentially a simple lock-in, referenced at the AC-bridge frequency (AD 630) [8]. On the other hand, AC methods even though they are not affected by low-frequency noise, drift, and thermal effects, suffer from parasitic reactances – inductive or capacitive [9, 10]. In this paper, a circuit solution is proposed based on the use of a second unloaded (dummy) AC strain-gage bridge, completely identical with the loaded AC bridge. Both strain-gage bridges are mounted closely to each other so that they experience quite equal parasitic effects. The outputs of both amplifiers are subtracted to eliminate the effects of reactances on the result. Thus, at frequencies between 1 kHz and 10 kHz very high sensitivity can be achieved, allowing for measurement of low strain deviations with high resolution.

The power P of a rotating shaft is obtained from the product of torque M_D and angular velocity Ω:

$$P = M_D\,\Omega. \tag{1}$$

Due to different losses such as friction, atmospheric resistance and heating every machine consumes more power than it delivers. The ratio of the output power P_{OUT} to the input power P_{IN} is known as efficiency coefficient η. In the case of the electrical brushless motors P_{OUT} corresponds to the output mechanical power P_{MECH} and P_{IN} to the input electrical power P_{EL}:

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{P_{MECH}}{P_{EL}}. \tag{2}$$

III. Measurement Set-up

An instrumentation system in a LabVIEW programming environment is used to control the measurement with a DAQ module that integrates connectivity and signal conditioning and delivers fast and accurate measurements. AC square-wave voltage with a frequency between 1kHz and 10 kHz is generated by DAQ to supply both strain-gage bridges with an rms value of 1, 2 or 5 Volts. Both bridges are full 4-arm strain-gage with nominal resistance of 350 Ohms. Two equally designed lock-in amplifiers are connected to the AC outputs of the bridges. So the first lock-in measures the loaded AC bridge together with the parasitic components, while the second lock-in measures only the effects of the same parasitic components. Subtracting the respective signals measured from loaded and unloaded (dummy) strain-gage bridges is carried out by DAQ system and the final result is displayed on PC.

The proposed measurement set-up with two AC- strain-gage bridges is shown on Fig. 3.

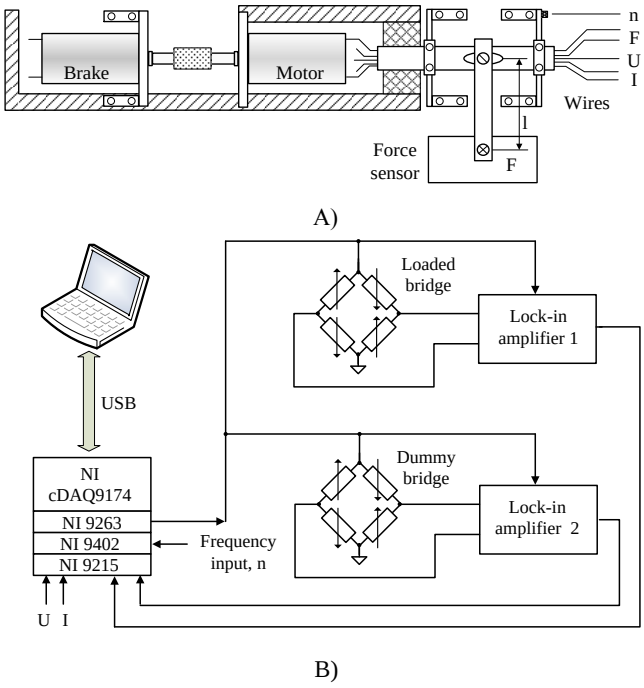

Fig. 3. A) Main components of the test bench.
B) Proposed measurement set-up with two AC- strain-gage bridges in LabVIEW environment.

The NI cDAQ-9174 is a 4-slot NI CompactDAQ USB chassis. It has four 32-bit general-purpose counter/timers built in. Each timer can be accessed through NI 9402. The NI 9402 is a 4-channel bidirectional digital input module.

The NI USB-9215A DAQ module offers four channels of simultaneously sampled voltage inputs with 16-bit accuracy. Two channels are used for the measurement of the output signals of the lock-in amplifiers and the other two for electrical power measurement.

NI 9263 is a 4-channel, high-performance analog output 100 kS/s simultaneously updating analog output module. It is used to generate the needed waveforms.

The current measurement uses a precision of 0,01 Ohm (resistance tolerances of 0,5%) 4 terminal Powertron shunt resistor type FPR 4-3316.

For the rotation speed measurement a Texas Instruments DRV5023 digital-switch Hall sensor is used. The device is a chopper-stabilized Hall sensor with a digital latched output for magnetic sensing applications.

IV. AC-STRAIN-GAGE BRIDGE WITH LOCK-IN AMPLIFIER

The main idea of using the AC excitation of the strain-gage bridge is to employ a lock-In amplifier in order to recover the weak bridge signals from the noise. The lock-in amplifier measures the magnitude of a signal in a very narrow frequency bandwidth, while rejects all the components of the signal that are outside it. The lock-in approach has revealed to be better than a simple filtering operation, thanks to its superior performance. In fact, because of the automatic tracking, lock-in amplifiers can give effective quality factor Q values (a measure of filter selectivity) over 100,000, whereas a normal band-pass filter becomes difficult to use with a Q greater than 50 [11].

Here, a simple dual phase lock-in amplifier solution is presented, designed with two AD630 balanced modulator/demodulator circuits. Considering first the way AD630 works, one should discuss the square-wave form of multiplier switching. Using Fourier's theorem, any input signal, including the noise accompanying it, can be represented as the sum of many sine-waves of different amplitudes, phases and frequencies. Let us suppose for example a 2 volt peak-to-peak square-wave at frequency f, which according to Fourier's theorem can be expressed as:

$$V = \frac{4}{\pi} sin\, \omega t + \frac{4}{3\pi} sin\, 3\omega t + \frac{4}{5\pi} sin\, 5\omega t. \qquad (3)$$

The phase-sensitive detector in the lock-in amplifier multiplies all these components by a signal at the reference frequency [12]. In the case of the square-wave responding Analog Devices chip AD630, an output proportional to the components of the input signal in phase lock with the reference signal and its odd harmonics has to be expected. Using a three-pole Butterworth low-pass filter one can remove the odd harmonics from the output and obtain a DC signal proportional to the desired signal from the bridge with locked first harmonic frequency.

The second consideration when developing the AC bridge amplifier system is to use dual-phase lock-in amplifier – employing two quadrature phase detectors to eliminate the effect of phase shift of the signal due to parasitic stray capacitances and wires [13]. An advantage of the dual-phase unit is that if the signal channel phase changes (but not its amplitude) then although the output – "X" - from one detector will decrease, that from the second –"Y – will increase. It can be shown, however, that the vector magnitude, R, remains constant.

Using DAQ in LabVIEW environment makes the development of dual-phase lock-in amplifier system easy. This DAQ module allows us not only to convert the analog signal into digital, but also to perform mathematical operations over the measured signal. Thus, a simple dual-phase lock-in amplifier has been developed for measuring output from AC strain-gage bridge with two equally performing circuits AD630. The first one multiplies the output signal from the bridge with the reference signal in phase, while the second one multiplies the same signal with the reference signal phase-shifted by 90 degrees. Both AD630 circuits are followed by equally designed three-pole Butterworth filter for eliminating odd harmonics and fed to analog-to digital converter inputs of DAQ. The first output is being referred to as the "X", and the second output as "Y"

Hence, if the lock-in amplifier is set to display R, changes in the signal phase will not affect the reading and the instrument does not require the adjustment of the reference phase-shifter circuit.

$$R = \sqrt{X^2 + Y^2}\,. \qquad (4)$$

Figure 4 illustrates the circuit diagram of the dual-phase lock-in amplifier system for measurement of the AC strain-gage bridge output.

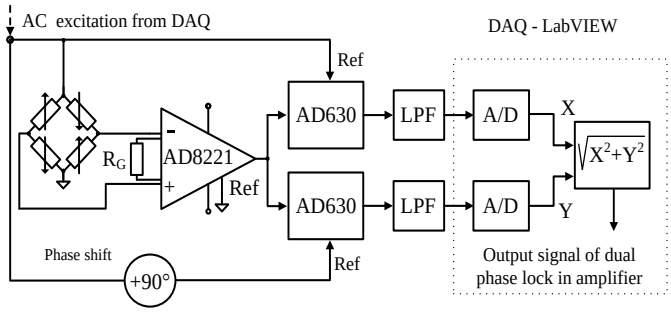

Fig. 4. Dual-phase lock-in amplifier for measuring output from AC strain-gage bridge (AD630)

Here an instrumentation amplifier AD8221 is used directly at bridge output to amplify the weak signals from the strain-gage. The AD8221 is well suited for this application because its high CMRR over frequency ensures that the signal, which is of interest for us and appears as a small difference voltage riding on a large AC common-mode voltage, is picked up and the common-mode signal is rejected. In typical instrumentation amplifiers, CMRR falls off at about 200 Hz. In contrast, the AD8221 continues to reject common-mode signals beyond 10 kHz [14].

V. EXPERIMENTAL RESULTS

TABLE 1 shows the results of the accuracies achieved by DC and AC bridge excitation. For a better comparison of

the results the relative standard deviation (RSD – relation of the standard deviation against the arithmetic mean value in percentage) is used.

TABLE 1. COMPARISON OF THE RELATIVE STANDARD DEVIATION (RSD) BY DC AND AC BRIDE EXCITATION.

	Force, N	RSD, DC excitation, %	RSD, AC excitation, %	Ratio
1	20	0,8412	0,0624	13,48
2	50	0,6855	0,0519	12,81
3	100	0,4164	0,0364	10,68
4	200	0,2757	0,0192	14,36
5	500	0,1939	0,0116	16,74

The results show the superiority of the proposed AC bridge excitation and lock-in amplifier approach.

TABLE 2 displays the experimental results for the comparison of the relative standard deviation (RSD) by AC bride excitation in setups with one and two bridges. It can be seen that the measurement setup with 2 bridges outperforms the one bridge setup by 2 – 3 times.

TABLE 2. COMPARISON OF THE RELATIVE STANDARD DEVIATION (RSD) BY AC BRIDE EXCITATION WITH ONE AND TWO BRIDGES.

	Force, N	RSD, one bridge AC, %	RSD, two bridges AC, %	Ratio
1	20	0,0604	0,0182	3,32
2	50	0,0519	0,0167	3,11
3	100	0,0364	0,0152	2,4
4	200	0,0182	0,0078	2,33
5	500	0,0116	0,0055	2,1

The system displays the values of all parameters, needed for the measurement of electrical and mechanical power and the calculation of the efficiency coefficient in real time. Fig. 5. shows the experimentally obtained dependence between current and efficiency coefficient η.

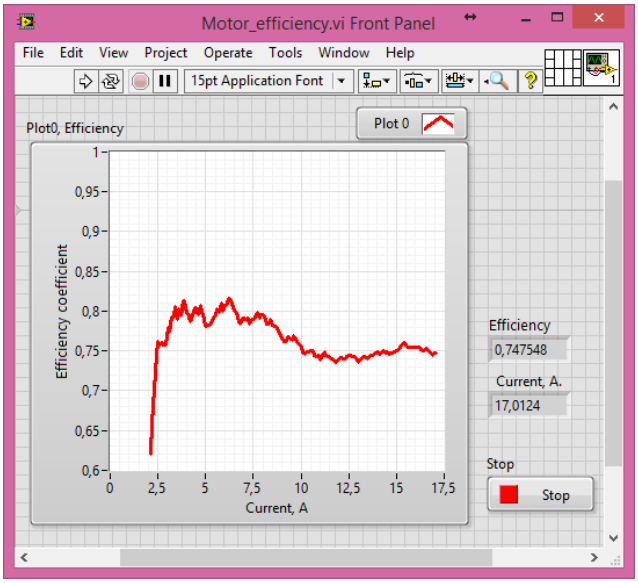

Fig. 5. The experimentally obtained dependence between current and efficiency coefficient η.

VI. CONCLUSION

Torque measurement and control is essential for companies to ensure their product's quality, safety and reliability. This paper presents the implementation of systems for monitoring torque, efficiency and speed of brushless motors. The proposed solution is robust and offers possibilities for significant error reduction. Our framework can easily be augmented by additional sensors if necessary.

The strain gage technique will be the primary solution for torque sensors in the future. As electronics is becoming smaller and electrically more stable, sensors can be designed for higher spring rates which leads to improved dynamics of the measurement. The usage of AC excitation and lock-in amplifier techniques allows the precise amplification of smallest measurement signals. This improved measurement signal conditioning can be successfully used for achieving a higher accuracy of the testing equipment.

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Investigations on Impedance Behaviour of Microwave-Plasma at Atmospheric Pressure

Nina Jetchkova Djermanova, Jivko Gospodinov Kiss'ovski, Vassil Atanasov Vachkov, Yanko Iliev Todorov and Desislav Stilijanov Damyanov

Abstract – **Impedance investigations of microwave plasma at atmospheric pressure are performed using an Arduino-based PC-controlled measurement system. A simple capacitive sensor is designed to monitor the impedance of the discharge at different conditions with impedance converter AD5933 connected via Arduino microcontroller board to PC. An appropriate equivalent circuit is proposed to describe the behavior of plasma impedance. Measurements results are obtained, verifying the equivalent circuit of microwave plasma.**

Keywords – **impedance, microwave-plasma, capacitive sensor, arduino**

I. Introduction

In this study we present a new technique for investigations of a small plasma source at atmospheric pressure. Microwave plasma is produced at low power levels by means of surface wave discharge in a ceramic tube with high permittivity [1-2]. The high thermal conductivity and high working temperature of the discharge ceramic tube allow permanent work of the source cooled only by air and ensure stable plasma parameters independent on the ambient conditions for a long period. Investigations of plasma impedance behavior at different discharge conditions are performed and an appropriate equivalent circuit is verified by measurements results.

Impedance behavior is a versatile tool used to characterize the intrinsic properties of any material and its interface. It is used in many applications such as monitoring electrochemical reactions, testing batteries, geological mapping, testing coatings and many other applications [3-4]. In recent years impedance spectroscopy is especially gaining popularity for biological and medical applications. Impedance tomography as well as impedance pletismography are just two examples of this new technique in medicine. Many integrated circuit suppliers deliver already Systems on a Chip – SoC, intended to measure impedance and to analyse electric network properties. These make the realization of measurement tasks in many cases much more compact, easier and completely realizable under PC control. In this work impedance measurements are used to investigate the miniature source of microwave surface wave discharge plasma at atmospheric pressure. An appropriate capacitive sensor is designed to monitor the impedance of the discharge at different conditions. An Arduino-based PC-controlled measurement system is developed, using the impedance converter AD5933 for measuring the impedance of the capacitive sensor. The capacitive character of plasma impedance with its real and imaginary parts allow for evaluation of plasma parameters – plasma density and temperature.

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II. Arduino-based Microcontroller System with AD5933 Impedance Converter

AD5933 is a high precision impedance converter system solution that combines an on-board frequency generator with a 12-bit, 1 MSPS, analog-to-digital converter (ADC). The frequency generator allows an external complex impedance to be excited with a known frequency. The response signal from the impedance is sampled by the on-board ADC and a discrete Fourier transform (DFT) is processed by an on-board DSP engine. The DFT algorithm returns a real (R) and imaginary (I) data-word at each output frequency. A DFT is calculated for each frequency point in the sweep. The result is stored in two 16-bit registers representing the real and the imaginary components R and I of the result. The data is stored in binary two's complement format. The impedance magnitude and phase are easily calculated using the following equations:

$$\text{Magnitude} = \sqrt{(R^2 + I^2)} \quad (1)$$

$$\text{Phase} = \tan^{-1}(I/R) \quad (2)$$

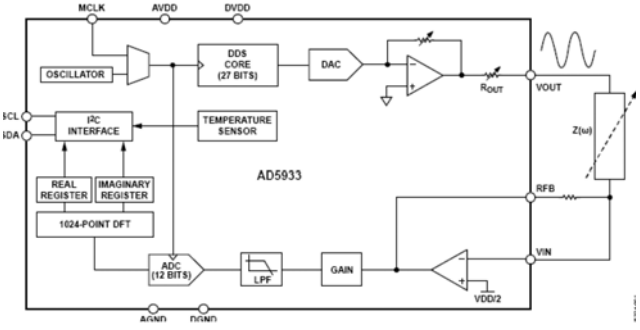

Fig.1. Impedance converter AD5933 (Analog.com)

Once the magnitude of the impedance (|Z|) and the impedance phase angle (ZØ, in radians) are correctly calculated, it is possible to determine the magnitude of the real (resistive) and imaginary (reactive) component of the impedance (ZUNKNOWN) by the vector projection of the impedance magnitude onto the real and imaginary impedance axis using the following formulas: The real component is given by

$$|Z_{REAL}| = |Z| \times \cos(ZØ) \quad (3)$$

The imaginary component is given by

$$|Z_{IMAG}| = |Z| \times \sin(ZØ) \quad (4)$$

The system should be calibrated before measuring the unknown impedance applying known reference resistor at the input of the trans-impedance converter. Once calibrated, the magnitude of the impedance and relative phase of the impedance at each frequency point along the sweep is easily calculated. This is done off chip using the real and imaginary register contents, which can be read from the serial I2C interface.

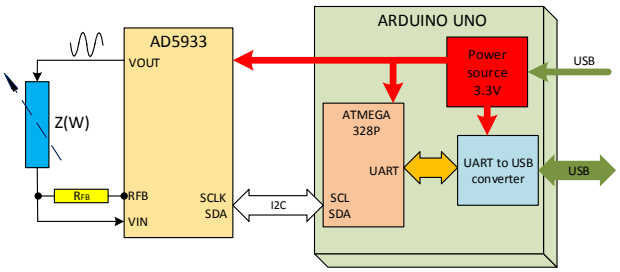

Fig. 2. Connecting Arduino to AD5933 via I2C and to PC via USB

The AD5933 permits the user to perform a frequency sweep with a user-defined start frequency, frequency resolution, and number of points in the sweep. In addition, the device allows the user to program the peak-to-peak value of the output sinusoidal signal as an excitation to the external unknown impedance connected between the VOUT and VIN pins. Control of the AD5933 is carried out via the I2C compliant serial interface protocol. The AD5933 is connected to this bus as a slave device under the control of a master device – the Arduino microcontroller board in this case. Arduino is connected via USB to a Personal Computer using open source coding for control and calculating the results [3]

III. Design of a Capacitive Sensor for Miniature Microwave Plasma Discharge at Atmospheric Pressure

To successfully investigate plasma parameters by means of the impedance converter AD5933, some constructions of an appropriate plasma impedance probe were considered [7-12], most of them based on the capacitive character of the plasma impedance. In this work a convenient capacitive sensor is designed to suite the features of the investigated microwave plasma source.

A. Miniature microwave plasma discharge at atmospheric pressure

The plasma source developed in [1] is operating at low power regime at atmospheric pressure and creates argon plasma in dielectric tube with inner diameter of 1 mm. This tube is an extension of open-ended coaxial structure. Microwave power at frequency 2.45 GHz is coupled into the source applicator at power levels 5-20 W. The plasma source operates as a plasma torch in case of plasma column longer than the dielectric tube length. The source maintains discharges over a wide range of neutral gas flow and works in continuous wave and pulse regimes of the input microwave power. The dielectric of the exciter of the surface waves is a ceramic tube with inner diameter of D= 1mm and outer of 2 mm of alumina ceramic with dielectric constant εd = 9.3, which is also used as a discharge tube. This material reduces significantly the exciter dimensions l1 to the length of 10 mm (l1~ λ0/4 d ε , λ0 – wave length in the free space).

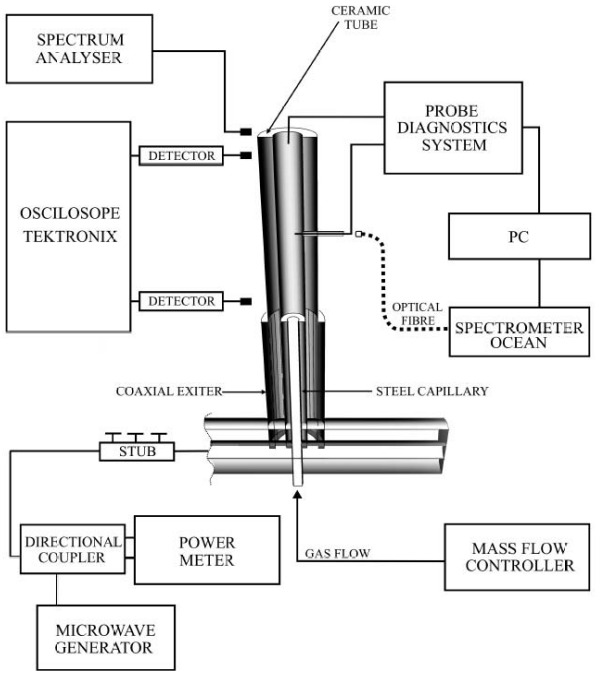

Fig. 2. Experimental set-up of microwave plasma discharge at atmospheric pressure

B. Capacitive sensor design

These small dimensions – length and diameter of the dielectric tube set specific demands on the plasma impedance probe which has to be used in our measurement system. Previously two ideas were discussed – first one about using a coax cable as a small antenna placed in the discharge torch, and second one – about a capacitive sensor built up of two rings slipped on the ceramic discharge tube. Considering the small inner diameter of the tube the usage of a coax as a capacitive sensor is not the best solution. Two thin copper wires with diameter 1mm wrapped around the ceramic tube at a distance of 5mm (fig. 3) are used as two rings of the capacitive sensor. The equivalent circuit of the sensor in absence of plasma discharge is given on

figure 4. The capacitor formed of these two rings is approximately evaluated by the formulae:

$$C_o = \varepsilon\Pi(r_{out}^2 - r_{in}^2)/d, \quad (5)$$

where r_{out} is the outer radius of the ring;
and r_{in} is the inner radius of the ring.

Parallel to this capacitor in absence of plasma a resistance Rd is connected defined by isolation resistance of the dielectric tube. When however plasma discharge is excited inside the ceramic tube, the equivalent circuit is completely changed. Plasma inside the tube acts as a conductor, which is shown in the equivalent circuit in figure 5 by a resistance Rpl, added in parallel to C_o. The effect of plasma presence inside the tube is also indicated through adding of two equal capacitances C_c in series with this small plasma resistance. These capacitances are formed between each ring and the conducting plasma inside, divided not only by the wall of the dielectric tube but also by the pre-sheet at the inner side of the walls. The major change in the equivalent circuit is the emergence of an additional capacitance Cpl between the two copper rings as a result of plasma ignition which causes variation in the dielectric constant in-between the both metal rings of the capacitive sensor over the tube.

C. Equivalent circuit of the capacitive sensor

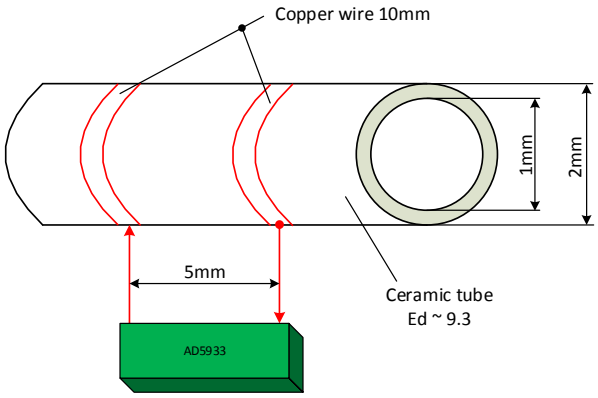

Fig. 3. Capacitive sensor over the discharge tube

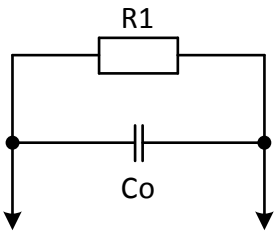

Fig. 4. Equivalent circuit of the sensor in absence of plasma

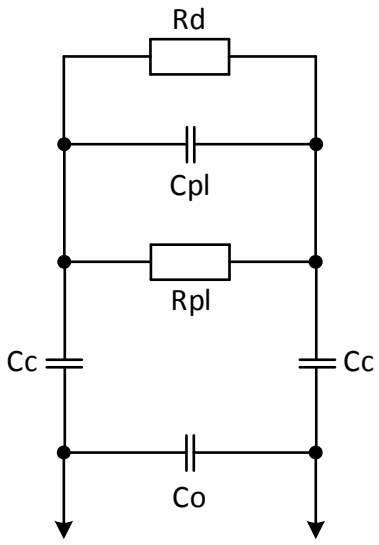

Fig. 5. Equivalent circuit of the capacitive sensor with plasma in the discharge tube

IV. Experimental Results

Microwave plasma discharge at atmospheric pressure was investigated at three different values of discharge-sustaining power. The impedance of the plasma was measured by the impedance converter AD5933 connected to Arduino and PC according to figure 2. The level of exciting voltage was chosen 2V and the frequency set to 30Khz. Results for the |Z|-magnitude, the real and the imaginary part obtained by the measurement are shown in table 1 for 10W, 15W and 20W discharge power.

TABLE1. EXPERIMENTAL RESULTS

Power (W)	|Z| magnitude (Ohm)	Real part (Ohm)	Imaginary part (Ohm)
0 (No plasma)	74592	59673.6	44755.2
10	60988	36592.8	48790.4
15	42446	25467.6	33946.8
20	10123	6073.8	8098.4

Obviously the impedance of the sensor is changed significantly in presence of plasma. Parallel to the initial capacitance Co the series capacitances of the ring-dielectric-plasma-pre-sheet are added together with the parallel combination of plasma capacitance Cpl and plasma resistance Rpl. It is seen that increasing the power leads to significant reducing in the impedance of the plasma with reducing its real as well as its imaginary part.

V. Conclusion

In this work an impedance investigation of a microwave-plasma at atmospheric pressure is performed using an impedance converter AD5933 connected to Arduino platform and to PC. An appropriate equivalent circuit of the microwave plasma is proposed and verified by measurement results. The real and the imaginary part of the

plasma impedance are measured and the effect of the microwave power sustaining the discharge is estimated.

ACKNOWLEDGEMENTS

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Sun Tracking Sensor with Current Loop Output

Todor Stoyanov Djamiykov, Katya Konstantinova Asparuhova and Ivan Slavov Spasov

Abstract –**The paper is presented the technical solution of simultaneous measurement of the angle of the sun elevation and the create radiation. The sensor is based on three photodiodes. The diodes are arranged at different angles, three amplifier circuits and three transmitters for the current loop 4÷20 mA. The relation between the signals from each photodiode depends of the sun altitude. The PSpice simulation results for the amplifier ant the current converter circuit are shown.**

Keywords – **Sun altitude sensor, photodiode, Optoelectronic device, PSpice optoelectronic circuit simulation**

I. INTRODUCTION

The sun light absorbing technologies are among the priorities in the world energetical economy development. Increasing the efficiency of photovoltaic systems is possible, through their continuous panel orientation perpendicular to the solar radiation. Sun-tracking photovoltaic systems provide 40% more energy compared to static ones [1, 2, 6]. For the implementation of such system a sensor measuring sun angular placement is needed. This is the ascent to the horizon, respectively the angle of the solar radiation when the sensor is placed horizontally. Another option is a sensor that generates a signal proportional to the angular deviation between the sun and solar system direction. In this case the sensor can be moved together with the solar system.

The proposed solution is an optoelectronic sensor, used for setting-up on the moving part of the solar system (mirror or photovoltaic) and for generating current proportional to the solar radiation. The sensor consists of three identical channels. Solar radiation measurement is based on the photodiode in a photovoltaic mode. The generated voltage is further gained, filtered and converted into a current loop 4÷20 mA [3].

The algorithm for tracking the sun's angular deviation is implemented in the computing unit by using information about the incident solar radiation. It is calculated according to the voltage generated by the photodiode, which depends logarithmically of the incident solar radiation [4, 5].

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II. PRINCIPLE OF OPERATION

A. Block Diagram

The basic requirements that must be satisfied by the angular sun deviation sensor are: Firstly normal operation in a wide dynamic range of sun light; Secondly changing the luminance of the Earth's surface is in the range 500-150000 Lux or the entire spectral range - irradiance in the range up to 1300 W/m^2; High accuracy of the conversion and measurement of solar radiation; Multiple channels of photosensitive elements availability in order to accurately calculate the angular deviation; Last but not least is the sensor implementation in the minimum size and weight.

To satisfy the variety of requirements we propose that the sensor is composed of three photodiodes, arranged at different angles, three amplifier circuits and three drivers for the current loop 4÷20 mA. A block diagram for one channel is shown on Fig.1 as the other two are identical to the shown one. The generated by photodiodes voltage is amplified by non-inverting amplifier with amplification gain 6. On the input of the voltage to current convertor is fed the maximum value of 4.2 V. This voltage value is selected to be the maximum value and is being converted into 20 mA current. There is a constant voltage of 5V in the driver's current circuit for supplying the analog part. To establish an initial value of radiance transmitted in the circuit, a source is switched on the input of the convertor.

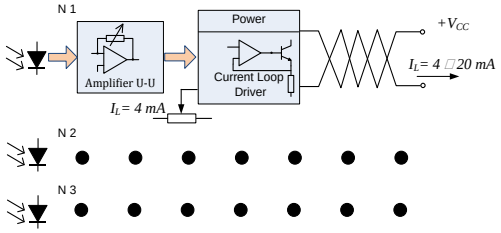

Fig. 1. Sensor Block Diagram

The geometric positioning of the photodiodes is shown on Fig. 2. The first one is mounted horizontally, and the other two photodiodes symmetrically on both sides in a 40 degrees angle. Thanks to such positioning, when the sensor is precisely directed towards the sun, the optical flow falling on the photodiode side will be cos (40 °), or 0.76 of the photodiode Ph1's one.

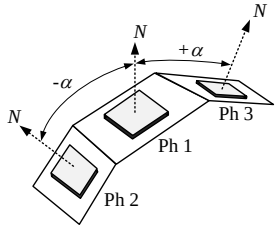

Fig. 2. Geometric positioning of the photodiodes.

Horizontally set-up photodiode is calibrated such that the output current is functionally dependent on the incident solar radiation in units of W/m^2.

B. Relation between the Sun Radiation and the Voltage over the Photodiode

Silicon photodiode type BPW34 is selected for the sensor. BPW34's spectral sensitivity is in the range of 0.4 to 1.1 micrometers, whereas the maximum sensitivity is 0.6 A/W [7, 8]. The luminance created from the sun light is in a range of tens lx to 150 000 lx, or expressed in energy units from approximately zero to 1300 W/m^2. A wide dynamic range of the photodiode-generated voltage according to a logarithmic dependence can only be implemented in photovoltaic mode [4, 9]:

$$V_{OC} = \frac{kT}{q} \ln\left(\frac{E_e A_{ph} . R_{ph}}{I_S} + 1\right), [V] \quad (1)$$

Where: kT / q is the temperature potential equal to 25 mV, I_S is the saturation current in the opposite direction; A_{ph} - the photosensitive area; *Rph* - integral sensitivity of photodiodes according to the source generating irradiance *Ee*, W/m^2 over the photodiode. For the used photodiode the current I_S is equal to 2 nA, which is the dark current from the data sheet, A_{ph} is equal to 7.5 m (from the data sheet). After conversion and calculating the relation of irradiation, created by the sun, is:

$$E_e = \frac{\left(e^{\left(\frac{qV_{OC}}{kT}\right)} - 1\right) . I_S}{A_{ph} . R_{ph}}, \quad (2)$$

The measured voltage is V_{OC}, other variables in the equation are constants. The equation (2) for the sun irradiation includes the integral sensitivity of photodiodes R_{ph}. For its calculation is used mathematical package MATHCAD. On Fig. 3 are shown the spectral characteristics in relative units: curve 1 - the solar radiation; curve 2 – the spectral response of the photodiode; dotted curve 3 - the sensitivity of the human eye and 4 – the product of curve 1 and curve 2. These characteristics are necessary for determining the coefficient of radiant flux from the sun as the source, by the set spectral characteristics of the photo detector.

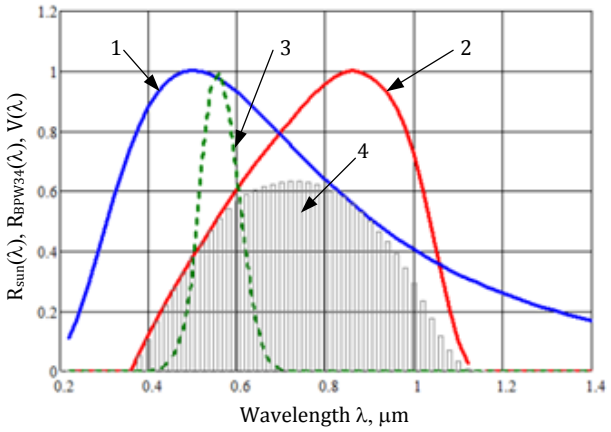

Fig. 3. Spectral characteristics.

After calculating and substituting the numerical values for the sensitivity the transfer characteristic of photodiode's relative to the solar radiation is obtained. This characteristic is, shown on Fig. 4.

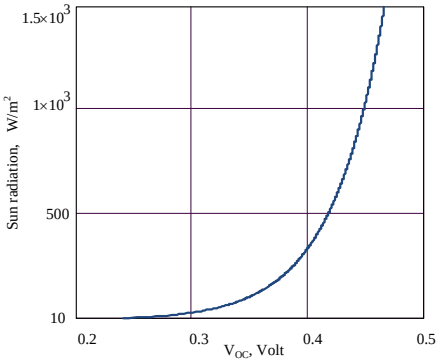

Fig. 4. Transfer characteristic of photodiode's relative to the solar radiation.

III. HARDWARE REALIZATION

The sensor's circuit is functionally composed of two parts. First part is an amplifier for the photodiode voltage and the second is a current-loop transmitter in the range of 4÷20 mA. This part of the circuit can be realized using the precision current output converter XTR117 of TI Inc. [3]. Fig. 5 shows the circuit diagram as the converter is replaced with representative simplified input circuitry enclosed by the solid line because there is no Spice model for this circuit.

In the circuit of the amplifier a capacitor *C3*, which together with the resistor *R7* forms an integrated group and narrows the bandwidth. As the movement of the sun in the sky is a slow process, as well as the movement of clouds, which drastically reduce optical flow reaching the ground, the bandwidth of this amplifier does not need to be wide.

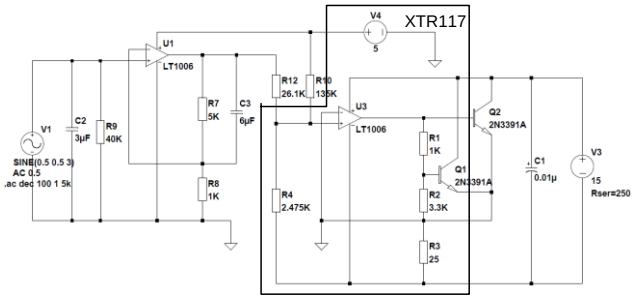

Fig. 5. Circuit diagram.

The precision current output converter designed to transmit analog 4-20mA signals over an industry-standard current loop. It is a two-wire current transmitter. Its input current controls the output current. A portion of the output current flows into the power supply. The remaining current flows in Q2. External input circuitry connected to the XTR117 can be powered from internal voltage regulator. Current drawn from these terminals must be returned to input pin. This pin is a local ground for input circuitry driving the XTR117. The XTR117 is a current-input device

with a gain of 100. A voltage input is converted to an input current with an external input resistor, *R12*, as shown in Fig. 5. Typical full-scale input voltages range from 1V and upward. Full-scale inputs greater than 0.5V are recommend to minimize the effects of offset voltage and drift of amplifier.

The power supply of the circuit diagram is unipolar 5V. The selected operational amplifier is LT1006 [10], which is a precise and with low values of polarized voltages and currents.

IV. Simulation Results

The two part of the circuit are simulated separated in order to test their functionality.

The transfer characteristic of the one channel of the amplifier is simulated in case of input from 0 to 0.7V. The simulation result is shown on Fig.6. The circuit amplifies linearly in the range.

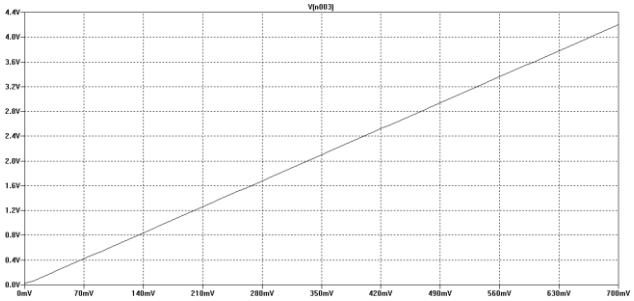

Fig. 6. Transfer characteristic of the amplifier.

The transient analysis of the amplifier is carried out based on a source of sinusoidal voltage with a frequency of 3 Hz. The given amplitude is 0.25V, the average point is also shifted to 0.25 V. The input voltage is only in positive direction. The results of the simulation are shown on Fig. 7.

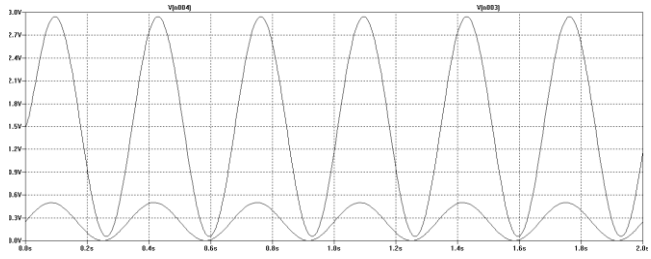

Fig. 7. Simulation results with sinusoidal source.

The results show that the circuit is working normally and without deviations. At the maximum possible input voltage value voltage of 0.5V, the output voltage of the amplifier is approximately 3.0 V. A frequency analysis is made for the amplifying circuit and the results for the gain and the phase are shown on Fig. 8.

The bandwidth is 23 Hz (at -3dB level), which is sufficient for the functions of the sensor.

For the current transmitter the efficiency, transfer characteristics and frequency properties are verified. Fig. 10 shows the results of the transfer characteristics simulation. Since the conversion of solar radiation becomes first in voltage ranging from 0 to 4 V, and the current must be within the range 4÷20 mA, is to be added to the input current by means of resistor *R10*.

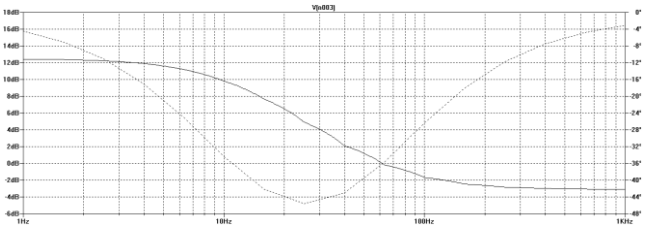

Fig. 8. Frequency response.

The current's value in the output circuit is determined according the following dependence:

$$I_{\text{out}} = \frac{100.\text{V}_{\text{inp}}}{\text{R}},$$

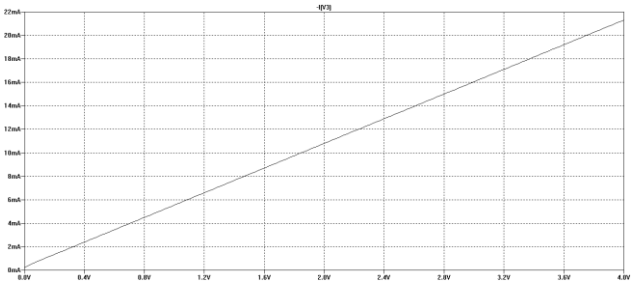

Fig. 10. Result of the transfer characteristic of the converter

Where *R* is the value of the resistor limiting the input current. The resistor *R12* sets the maximum current value in the circuit to 20mA, which must be generated at a maximum output voltage of the amplifier. The value of the resistor *R10*, defines the minimum current value chain - 4mA, when solar radiation is zero.

A frequency analysis is made for the amplifying circuit and the results of the simulations are shown in Fig. 11.

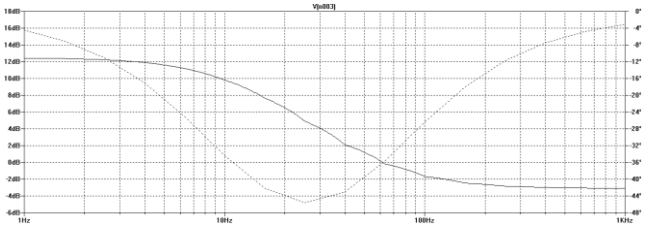

Fig. 11. Frequency analysis of the current output converter.

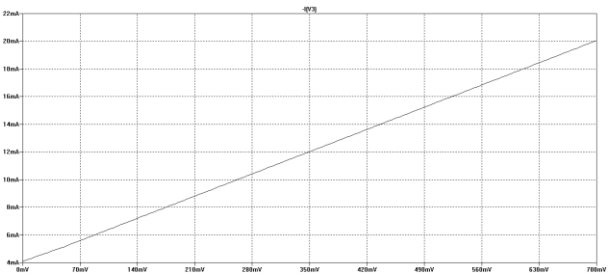

Fig. 12. Simulation results of the transfer characteristic.

The circuits of the amplifier and current output converter are simulated separately, but sensing device transfer characteristic is one. Fig. 12 shows the simulated total transfer characteristic of a measuring channel of the sensor of sun radiation.

V. CONCLUSION

In this paper is proposed a solution of the optoelectronic sensor for simultaneous measurement of the angle of the sun elevation and the create radiation. The theoretical dependencies of the generated voltage value of photodiodes are discussed and the transfer characteristic is represented. The results from the frequency analysis are shown too. Proposed is a block and a circuit diagram of the optoelectronic sensor implemented with minimum components. The circuits are simulated in the PSpice environment. Also the computer simulation results, the performance and the frequency properties of both the amplifier and the current transmitter generating the output current 4÷20 mA, are shown.

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Design of Adaptive Weather Station with Reduced Power Consumption

Dian Milchev Iliev, Vassil Nikolov Gourev and Mityo Georgiev Mitev

Abstract – **This paper describes the initial design of an adaptive weather station. The device relays on an ultra-low power micro architecture, adaptive power distribution mechanism, small form factor, and GPS receiver for time synchronization. The device is dynamically reconfigurable for working in high performance, real time transfer mode with direct operator control; and ultra-low power, fully autonomous, self-monitoring, long-term measurement mode. For convenience the collected data of the environment parameters will be initially analyzed and visualized by specialized software.**

Keywords – **Weather Station, Ultra-Low Power Management, Self-Monitoring, Dynamically Reconfigurable, GPS synchronized, Global Warming**

I. INTRODUCTION

Weather stations are facilities, with instruments and equipment for measuring atmospheric conditions to provide information for weather forecasts and to study the weather and climate.

For studying the climate changes is necessary to analyze the data from long-term measurements of the environment parameters (like temperature, barometric pressure, humidity, etc.). In correspondence with the requirements of the World Meteorological Organization [1], those measurements are done three times a day, with respect of the Sun position per each whether station. The data from the daily measurements are then logged in sets of different time frames (3 months, 6 months, year, etc.) and analyzed to define the tendencies in the climate changes.

The weather stations are often conveniently located in easily accessible locations, and the data could be collected daily. But sometimes scientific interests are remote regions without sustainable access (unattended areas). In this case, it is necessary to use a sophisticated apparatus capable of self-configuring, data logging and performance control, taking into account their power distribution and working conditions of the respective area.

For a number of activities (aviation, shipping, scientific research, etc.) measurements are focused on current weather conditions. In this case is used equipment allowing monitoring of environmental parameters in real time - measurements are done continuously, as a suitable interface is provided for communication with the user. Data from these measurements can be used as reference in order to take into account possible errors in the further processing of data from other measurements taken in parallel or used as input for other systems.

With records since latest 50s of last century showing rise in average temperature of the atmosphere and ocean on Earth, and the predictions for the possible consequences if these trends in climate change preserve, more attention is paid to strict measurement of environment parameters, globally and continuously. But the ground control stations designed for this purpose are often too expensive and highly power consuming to be installed permanently in remote areas. Therefore reporting of climate change on these sites often rely on satellite measurements - primary temperature. However this measurements are not directly comparable to the quoted above, since it is a skin temperature deduced from satellite-measured upwelling radiance, rather than a thermometer-measured temperature of the air 1.5 m above the ground surface.

In order to support a research of Bulgarian Antarctic Expedition was requested to provide systems for environment control in two different bases - measuring environmental parameters in real time as an aid to perform parallel measurements; and securing long term environment measurements in order to log statistical information on climate change during the winter season. These conditions make two contradictory system requirements - first, ensure monitoring of a wide range of parameters, where the high performance of the system is priority; and second - long-term measurements, where the total power consumption should be as low as possible. Last one requires great reduction of the parameter count and data logging rate, which are a priority for the first one.

The optimal solution is to create an adaptive compact system, that ensures all the necessary measurements to support experiments performed in real-time and able to autonomously provide series long-term measurements, by dynamically reconfiguring its working rate.

II. BASIC DESIGN

A. Requirements and Block Diagram

Key factors affecting the development of the system, with the specified requirements, are the working conditions

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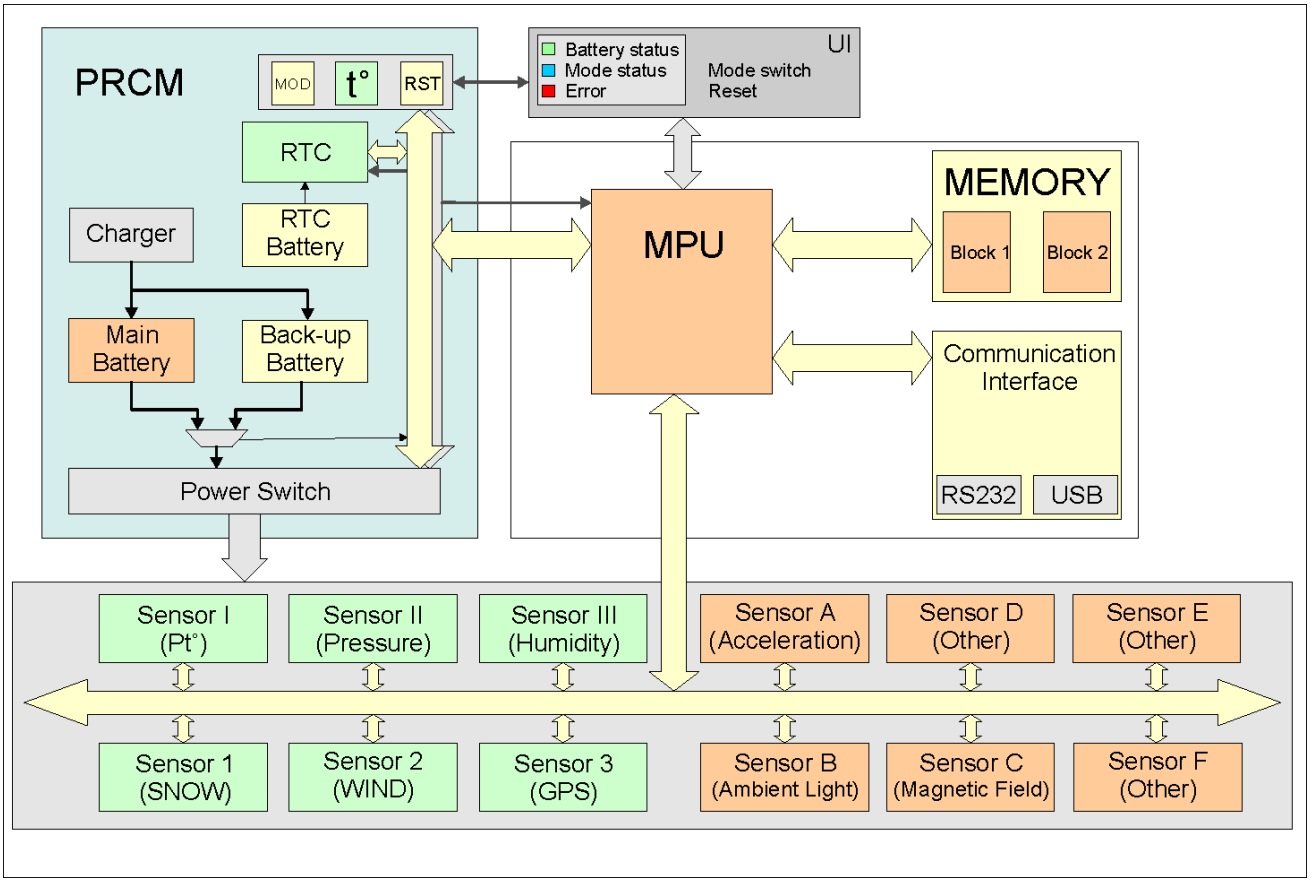

Fig. 1. Block diagram

under which the system operates, power consumption, autonomy and cooperativeness.

The weather station is developed on the base of three main subsystems:

- *Power, Reset, and Clock Manager (PRCM)*
- *Control Subsystem*
- *Sensor Subsystem*

Figure 1 is the conceptual block diagram of the weather station.

A special feature is the combination of high power consumption real-time monitoring system of environmental parameters and minimum power consumption requirements for long-term measurements. For this purpose was developed a specialized power control system (PRCM) that could isolate from the power source all unnecessary subsystems, for the duration of their passive states, and switch them on again when necessary. Management is fully electronic, as the specifics of the working conditions do not allow use of mechanical switches or moving parts.

B. Power, Reset, and Clock Manager

Power, Reset, and Clock Manager includes main and reserve batteries, interface insulator, as well as specialized charger.

Most weather stations for long-term measurements in unattended areas are equipped with various independent power sources - solar panels, wind or water turbines. These sources, however, are practically irrelevant in terms of the polar winter, so the system is designed to use only battery power.

The role of the charger is to provide power to the system in real-time modes and recharging batteries in serviceable stage of the device operation.

It also provides data for battery status to the control system on the base of which the latter may decide to limit the consumption during the period of unattended operation. This can be achieved by the exclusion of certain low-priority sensors.

C. Control Subsystem

The control subsystem is based on a microcontroller and includes a user interface for direct work with the system, interfaces for data transfer with other systems, real-time clock, an additional external watch-dog subsystem, and a data memory.

System management is executed by embedded software, including algorithms for determining the operating modes of the system (autonomous control or subordinate work), powering the sensors, synchronization, error detection, analysis and reconfiguration of the operating modes, the data logging and transmission.

The Device has two command interfaces - RS232 and USB.

RS232 is the system service interface designed for setup and connection with other autonomous systems. This allows the station to be integrated as a module in a larger system, and actively exchange data with it.

USB interface is designed for direct transmission of data to the computer systems, so the operator can monitor real-time measurements.

Real time clock and the additional watch-dog subsystem, though defined as control devices, in fact belong to the PRCM, as they ensure the continuous operation of the station. RTC also provides time stamp required for the synchronization of the measured parameters with a global database.

D. Sensor Subsystem

The sensor subsystem contains all the necessary sensors and peripherals required for the operation of the station. Sensors are prioritized and divided into 3 main groups.

The first group contains the basic sensors for the station - temperature sensors, sensor for pressure and temperature compensated humidity sensor.

The sensors for measuring the temperature of the system are two. The main sensor is built from platinum RTD (Pt100) type B. It is connected by a three-wire circuit to the instrumental amplifier INA827 [2] with offset correction. Analog to Digital conversation is performed by 12-bit ADC ADS7828 [3]. Figure 2 shows connection schematic.

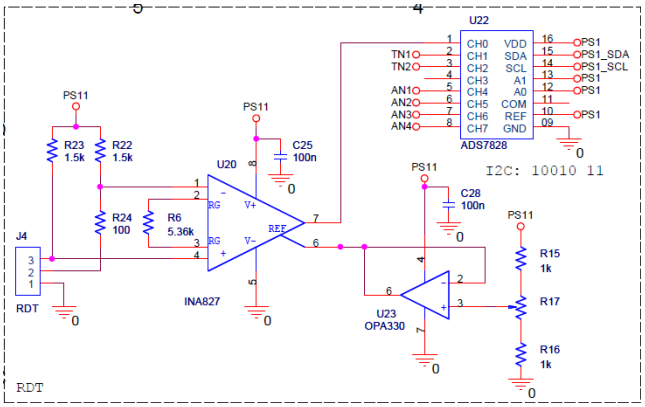

Fig. 2. Primary temperature sensor

In compliance with the requirements of the World Meteorological Organization temperature measurements are made at 1.5 meters above the ground [1].

There is an additional temperature sensor of semiconductor type (TMP112 [4]), whose role is to monitor the internal temperature of the system in the quartz resonator of real-time clock.

The humidity measurement is based on intelligent sensor with internal temperature compensation and a full range relative humidity - HDC1008 [5].

Measurement of barometric pressure is provided by other intelligent sensor - BMP085 [6].

The second group of sensors are used for the purposes of the research. It includes an accelerometer, a light sensor, and a magnetic field sensor.

The third group of sensors are low-priority and high consuming additional and synchronizing systems - GPS, wind sensor and sensor for thickness of the snow cover.

The GPS subsystem is provided as synchronization module for time adjustment. GPS as well as Anemometric module are intended to operate primary in serviceable period with available power supply, as their power consumption is very high.

Sensor module for reporting the snow cover thickness is designed to work during unattended period of the system. Therefore, it is planned to provide data once a day and to work in very short interval of time. If a shortage of energy resources appears - use can be further reduced by the system.

The sensor subsystem includes three expansion interface for adding additional sensor modules. The interfaces are equipped with controllable power supply, two analog inputs, a digital interface for transmission of data and two digital ports with general purpose.

III. PC APPLICATION

A specialized computer application is designed to provide easy control over the station during the real-time operation, and easily retrieve data collected during long-term measurements.

Figure 3 presents the summary diagram of computer application for working with the station.

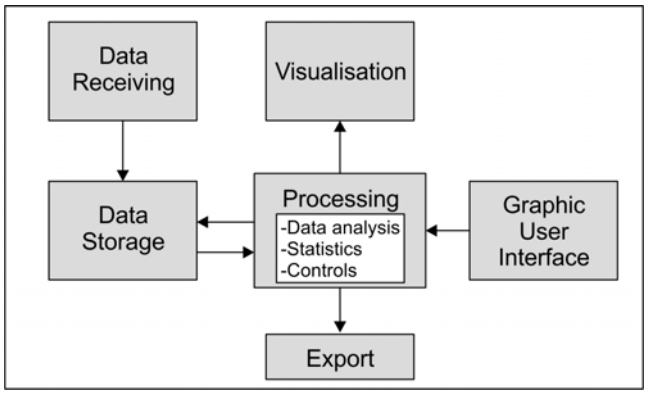

Fig. 3. Block diagram of the PC application

The application enables direct recording and storing data obtained during real-time operation of the station. It can be processed immediately and visualized on the display for direct monitoring and / or exported as a file for further analysis.

The user interface allows to set various parameters – configuring the work of the station and the application itself.

IV. CONCLUSION

Ground-based weather stations are among the most important tools for monitoring climate change and the impact that these changes have on the environment. Of great importance is the collection of as larger amounts of data from all over the world. The main problems in the construction of such a network of ground-based instruments is the size and cost of the stations, and their use is additionally limited by the specific function they are initially designed for.

Building a cheap and adaptive compact stations could significantly ease the process of collecting data in remote areas, and at the same time offers the possibility to use them as reference tools in other studies.

ACKNOWLEDGEMENT

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Measurement of Organic Solar Cell Parameters

Vasil Jivkov Siderov, Petar Georgiev Georgiev, Ivaylo Tzankov Zhivkov, Georgi Hristov Dobrikov, Rumen Stoyanov Yordanov, Martin Vala and Martin Weiter

Abstract – **Computer controlled voltage source operating in the range of 0÷10 V with up to 16 bit resolution was constructed and tested. The device capabilities were tested by measurement of *I-V* characteristics of organic solar cell.**

The tests performed show clearly that the module constructed could be used for testing of solar cells.

Keywords – **Data Acquisition System, Solar Cell Measurements**

I. Introduction

Current-voltage (*I-V*) measurements of semiconductor samples prototypes and devices with nonlinear characteristics - photovoltaic cells, light-emitting diodes, field effect transistors, and sensors play an important role [1, 2, 3].

These devices sometimes contain thin films of wide-gap semiconductors or insulators [4], where both ohmic and injection currents [5] could flow applaying voltages from few milivolts to several volts. From the other side the high precision measurements requires a satisfactory resolution to be achieved.

Especially for low-level signals, more sensitive instruments such as electrometers, picoammeters, and nanovoltmeters must be used. In this case some special precautions should be taken to prevent the noise and the influence of parasitic signals generated from sources with piesoelectrical, triboelectrical or electrochemical origin. In this case applaying galvanic insulation between the different modules could significantly reduce the afforementioned effects.

From other side the long time measurement need an atomatisation to be applied. For the purpose of automatiization virtual instrument are constructed consisting of an industry-standard computer or workstation equipped with powerful application software, cost-effective hardware such as plug-inboards, and driver software, which together perform the functions of traditional instruments.

This paper describes a construction and testing of simplified voltage source operating in the range of 0÷10 V with up to 16 bit resolution. The device has additional advantage of computer control and galvanic insulation which makes it proper for low-current measurements of wide-gap semiconductors and insulators.

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II. Device Description

A. Hardware

The voltage source (Fig. 1.) consists of 16 bit digital-to-analog converter (DAC), analog unit, reference voltage, galvanic insulation, microcontroller (μC) and power supply units.

DAC (1) is the fast, low noise DAC8830 chip (Texas Instruments) connected to the 5V high precise ADR02 voltage reference. The unbuffered DAC output is connected to the buffer (OPA376) which belongs to the analog unit (2). The analog unit includes also two operational amplifiers (OP07) which act as a summer and power amplifier, respectively. The summer converts the unipolar (5V) voltage to a bipolar (±5V) one. The power amplifier provides the full range woltage scale of ±10 V and output current up to 24 mA. The power amplifier could be connected to a second stage amplifier providing higher output voltage and current, which is under development.

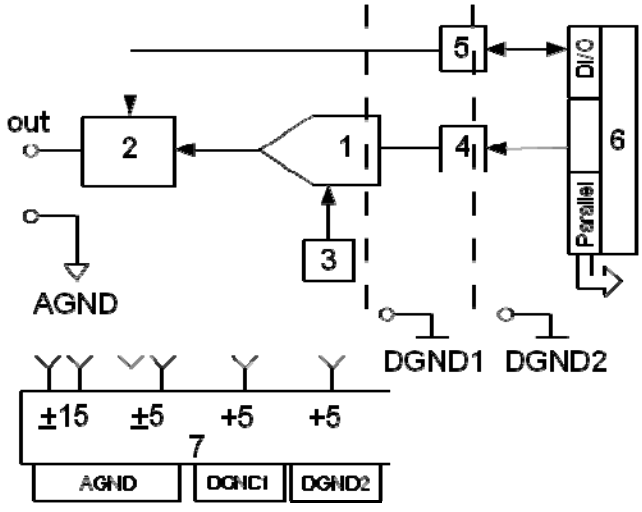

Fig. 1. Block Diagram of the Solar Cell Measurement Setup: 1 – DAC; 2 – Analog Unit; 3 – Voltage Reference; 4, 5 – Galvanic Insulation; 6 – Microcontroller; 7 – Power Supply

The galvanic insulation of the DAC (4) is implemented by the specialised chip ISO7241, which is proper to separate the serial peripheral interface (SPI), while the digital I/Os (5) are separated by conventional optocouplers. SPI interface transmitts the data from the μC to DAC in one direction. Therefore the SPI consists only of two clock and data lines. The additional chip select pin not only servs to select a specific slave devace, but also initiates the

measurement. Galvanic insulation module improves the performance of the device, especially for low current measurements. The microcontroller (μC) (6), controls the voltage source and gets the data from the main processor via parallel 8 bit interface. The parallel interface includes typical "data ready" (DR) and "data acknowledge" (DA) lines which provides the handshaking. The power supply provides three separate grounds (ANGND, DGND1, DGND2), which decreases the noise in the system and prevents the parasitic influence between the modules and external devices.

B. Software

Block-diagram of the μC firmware is presented in Fig. 2. It consists of the main part and the hardware driven interrupt service routine. The main part of the program implements the device initialization and configuration and starts and endless loop which is related to other tasks of the module. Upon an external interrupt request initiated by the main processor (non-presented in the block diagram), the data and commands presented on the 8 bit parallel bus are

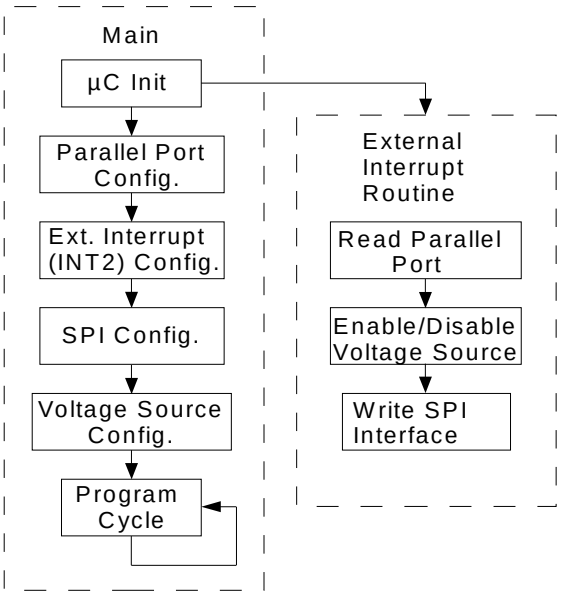

Fig. 2. Block diagram of the μC software

read and delivered to the periphery by the interrupt service routine. The interrupt line stays active during the whole stage of the data transmission and plays a role of DR signal. After the slave device accepted the data it emits the DA signal, which notifies the master device to finishes the measurement. The received through the parallel interface data could either rearrange the digital pins of the μC or sends a 16 bit data trough the SPI interface, The 16-but data are sent trough the interface in two bytes. The device performance was tested by measurement of current-voltage (*I-V*) characteristics of organic solar cell samples.

III. Solar Cell Sample Testing

A. Experimental conditions

The device performance was tested by measurement of *I-V* characteristics of organic solar cell samples.

The samples were prepared in the clean room class C, to prevent the dust and particles from disrupting the thin layer. The clean lab is equipped with MB-200B MBRAUN gloveboxes (M. Braun Inertgas-Systeme GmbH, Garching, Germany). Oxygen sensitive materials were stored and manipulated exclusively in the nitrogen gloveboxes, where also most of device fabrication step took place.

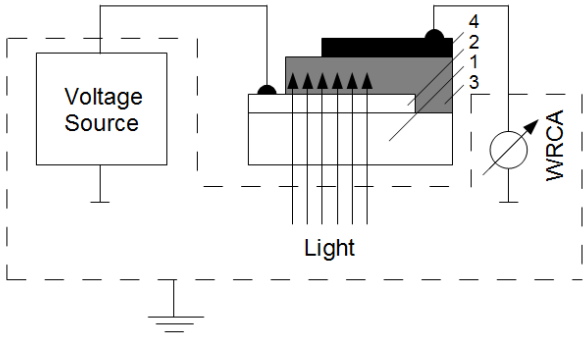

Fig. 3. Block Diagram of the Solar Cell Measurement Setup. Sample Configuration: 1 – Glass Substrate; 2 – Transparent ITO Anode; 3 – Active Organic Film; 4 – Al Cathode

Zinc Phthalocyanine (ZnPc) OF (see Fig. 3) (3) of 100 nm thickness were deposited onto indium tin oxide (ITO) electrode (2) of commercially pre-patterned Ossila substrates in the vacuum system from thermally heated sources at evaporation temperatures of about 500 ºC and deposition rate of 2.0 Å/s through the active area deposition mask. The deposition rate was controlled by quartz crystal microbalance. After deposition of the active composite layer, the samples were taken out in nitrogen atmosphere, the mask was changed and vacuum deposition of aluminum was performed. The aluminum cathode (4) of 150 nm film thickness was thermally evaporated in 1×10^{-6} mbar at a deposition rate of 1 Å/s.

Finally the structures were encapsulated by epoxide resin, which was hardened for 30 minutes under UV lamp irradiation. After that the samples were removed from the glovebox and provided with contacts for electrical measurements.

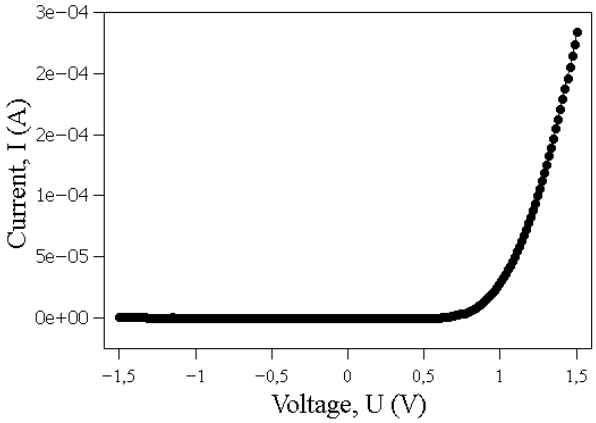

Fig. 4. Typical dark current-voltage solar cell diode

The setup for electrical measurement (Fig. 3) consists of originally developed Wide Range Current Amplifier (WRCA) and the constructed voltage source. Dark *I-V*

characteristics were measured in both directions of the voltage scale. The photoconductivity of the samples was measured under exposure of a standard light produced by solar simulator LS0916 LOT Oriel class AAA. It provides defined light source according to standard AM 1.5. Incident light intensity was about 1000 mW.cm^{-2} and was controlled by calibrated reference silicon cell RR200O from ReRa systems (ReRa Solutions BV; Nijmegen, Netherlands). For the studied samples, the exact irradiation of 953 mW.cm^{-2} was measured.

B. Results and Discussion

In Fig. 4 dark *I-V* characteristic measured with the constructed module from ITO|ZnPc|Al structure is presented. The curve exhibits a clear diode behavior, which is a typical case for organic solar cell. In Fig. 5 the dark *I-V* characteristic is plotted together with curves measured from the same sample under white light illumination. For the sake of clarification and estimation the electrical parameters of the samples, the data are presented in a semilogarithmic scale (the negative values of the current are multiplied by −1).

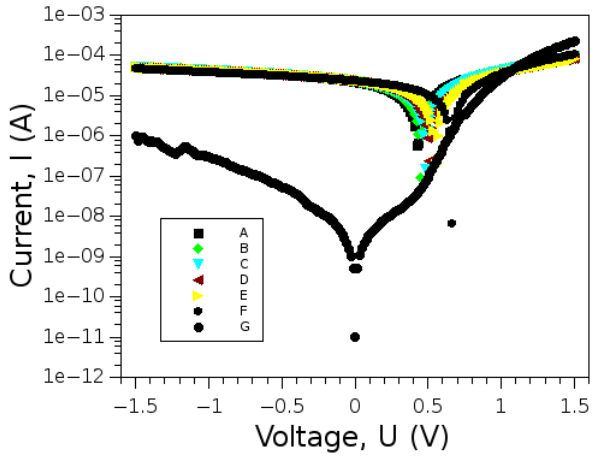

Figure 5. Current-voltage characteristic measured in dark and under light exposure

The dark-current diode curve (Fig. 5, Curve A) shows almost no contact barrier, which demonstrates a good interface contacts between the active OF and the electrodes. The dark curve measured in reverse direction has a tendency of diode saturation about -0.3 V. At higher voltages the measurement differs from the ideal diode which results in an increased curve slope. This effect could be related to the injection current as a result of the dominating bulk sample properties at higher voltages. Nevertheless the increased injection current in reversed direction which worsens the diode behavior a diode rectification ratio of more than two orders of magnitude was obtained. Under light exposure the open circuit voltage of 0.66 V was determined and the photocurrent in the clear diode part of the sample characteristic (0 to -0.3 V) increases almost 4 orders of magnitude comparing with the dark one.

The degradation of the sample reflected in a decrease of the open circuit voltage (Fig. 5, curves B÷F) under oxygen exposure was also investigated by the constructed. The dependence of the U_{OC} on the time of exposure on air is

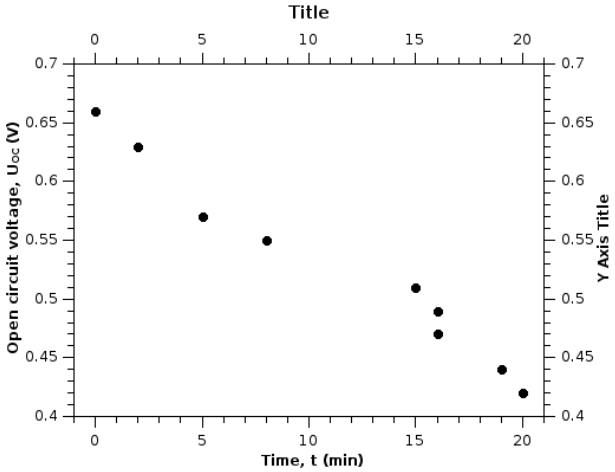

Fig. 6. Kinetics of the open circuit voltage

plotted in Fig. 6. Almost a linear U_{OC} decrease for a period of about 20 min air exposure could be seen.

IV. Conclusion

Computer controlled voltage source operating in the range of 0÷10 V with up to 16 bit resolution was constructed and tested

The device capabilities were tested by measurement of *I-V* characterisgics of organic solar celll.

The datk *I-V* curve taken from te tested solar cell shows clear diode behaviour. Under light exposure the photoconductivity, increases 4 orders of magnitude. The tests performed clearly show that the module constructed could be used for measurement of solar cells.

Acknowledgements

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Design of High-efficiency Dual-ratio Step-down Switched Capacitor Converter with Full Digital Feedback Control

Vazgen Shavarsh Melikyan and Vache Ashot Galstyan

Abstract – **The paper presents a novel adaptive digital control technique for multi-topology step-down switched-capacitor (SC) converter. The control system performs dynamic frequency modulation depending on load current as well as adjusts the conversion ratio to provide the required output voltage level. A novel non-overlap clock generator (NOCG) used in feedback control provides adjustable non-overlap period for switch control signals and enables the implementation of soft charging technique which reduces the output voltage ripple to 5mV. Proposed converter achieves 40ns response time to 60mA load variations and average conversion efficiency of 89% over wide range of load currents. The converter is designed in 28nm CMOS process using the proposed technique.**

Keywords **– CMOS, power converter, pulse frequency modulation, digital control oscillator, non-overlap clock generator, output ripple, conversion efficiency.**

I. INTRODUCTION

SC converters are widely used in up-to-date low power portable electronic systems to provide independent voltage conversion which is required for per module power management [1]. Primary function of DC-DC SC converters is the conversion of DC voltage at the input terminals into another DC voltage at the output terminal [2]. SC converters consist of power stage, which is responsible for voltage conversion and feedback control, which assures overall efficiency, load and line regulation characteristics of the system. The power stage is a dual phase structure which contains flying capacitors, switches and an output capacitor connected in corresponding way to form the required topology [3]. During the charging phase (Ph1), flying capacitors are connected to the battery and charged to the appropriate voltage. During the discharge phase (Ph2), flying capacitors are connected to the output node and discharge into the load through the output capacitor, thus providing the required output voltage. The most popular control technique for SC power converter is the pulse frequency modulation (PFM), where the switching frequency of the switches increases with the increase of the load current. Primary characteristics of SC converters are the voltage-conversion ratio (VCR), and the conversion efficiency (η). VCR is defined as the ratio between output voltage V_{out} and the input voltage V_{in} (Eq. 1), while the efficiency is the ratio of the converter's output power and input power. The efficiency has an upper bound equal to the ratio of the actual VCR and the iVCR: ideal VCR (Eq. 2), which is the maximum possible ratio between the output and input voltages of the conversion block.

$$VCR = \frac{Vout}{Vin} \quad (1)$$

$$\eta_{\max} = \frac{VCR}{iVCR} \quad (2)$$

A certain topology of SC converter corresponds to a specified VCR, which is the main disadvantage of SC converters. In order to increase input/output voltage range a multi-topology configuration is developed. Main challenge for modern SC converter design is to maintain low level of output ripple while providing high conversion efficiency for wide range of loads.

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II. STRUCTURE OF THE POWER CELL

The power stage topology proposed for this application is a dual-ratio, eight switch design shown in Fig. 1. With 1.4V input voltage, nominal output voltages of 0.75, 0.5 can be obtained.

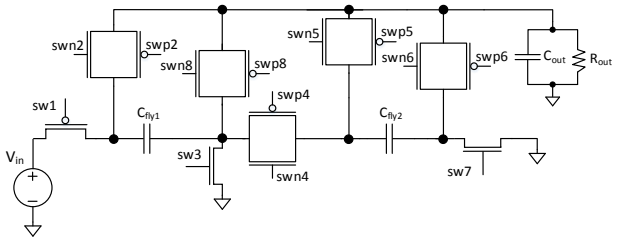

Fig. 1. Structure of the power cell

Switches connecting the input voltage source and flying capacitors were implemented with PMOS transistors which cover the whole operational range of the input voltage, while NMOS transistors where used to connect flying capacitors to the ground, thus lowering the area occupied by the switches. All remaining switches were implemented using transmission gates, i.e. NMOS and PMOS transistors connected in parallel which provided a low equivalent switch resistance. By varying how the switches are clocked, according to the TabSle I, conversion ratios of 1/2 and 1/3 can be obtained [5].

TABLE 1. SWITCH OPERATION FOR EACH PHASE AND MODE

Topology	Phase	Sw1	Sw2	Sw3	Sw4	Sw5	Sw6	Sw7	Sw8
1/2	**Ph1**	**ON**	**OFF**	**OFF**	**OFF**	**OFF**	**OFF**	**OFF**	ON
1/2	Ph2	OFF	ON	ON	OFF	OFF	OFF	OF	OFF
1/3	**Ph1**	**ON**	**OFF**	**OFF**	**ON**	**OFF**	**ON**	**OFF**	**OFF**
1/3	Ph2	OFF	ON	ON	OFF	ON	OFF	ON	OFF

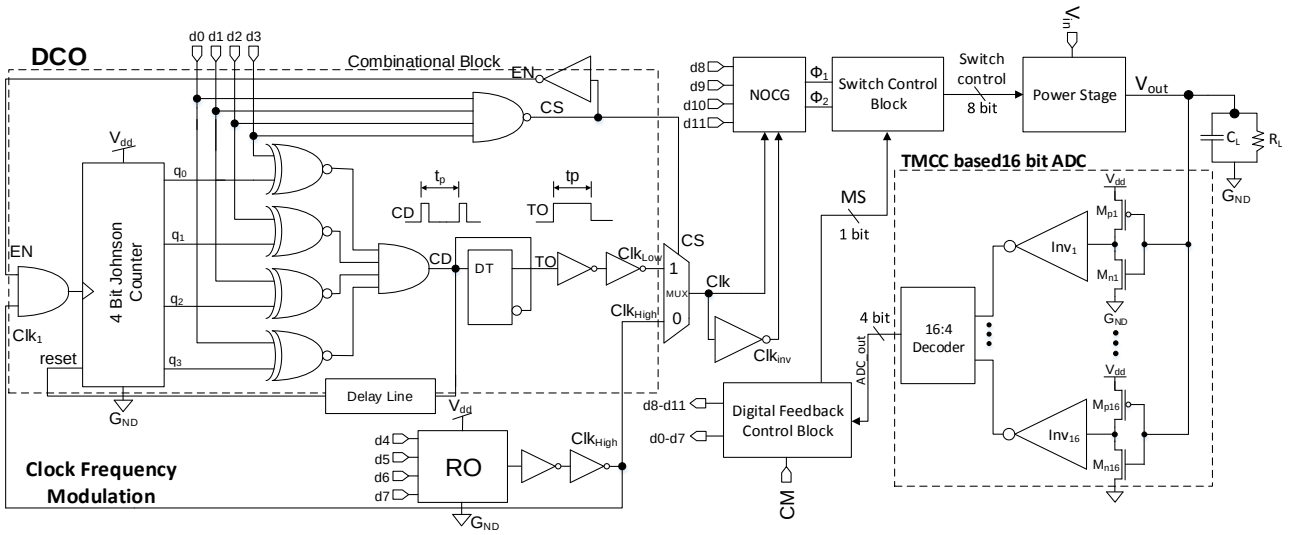

Fig. 2. System Architecture of proposed SC converter

III. System Architecture and Design Strategy

A novel digital control system is proposed which consists of threshold modified comparator circuit (TMCC) based analog-to-digital converter (ADC), digital control oscillator (DCO), NOCG and digital control block which adjusts the feedback system and power stage topology (Fig.2). Main goals for developing the feedback control were to eliminate the usage of reference voltages, as well as to assure fast load regulation response speed. The principle of PFM is shown in Fig. 3, which is the control of output voltage by modifying the switching frequency according to the load.

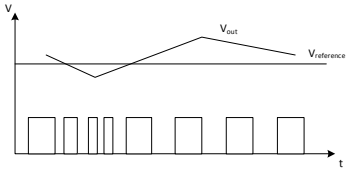

Fig. 3. Principle of frequency modulation

In order to track the output variations, conventional SC converters use a reference voltage and comparator circuit [4]. In proposed design a novel TMCC based 16 bit ADC is implemented which eliminates the usage of reference voltage and reduces the power consumption of the feedback circuit [5]. Unlike traditional Flash ADC, the series combination of resistors is replaced with TMCCs. TMCC is an inverter circuit with modified threshold voltage followed by NOT gate (Fig. 4). According to the required reference voltage, the threshold of corresponding inverter can be modified by modifying the width-length ratio of the MOSFETS (Eq.3).

$$V_{th} = \frac{V_{tn} + \sqrt{\frac{\mu_p W_p}{\mu_n W_n}}(V_{DD} - |V_{tp}|)}{1 + \sqrt{\frac{\mu_p W_p}{\mu_n W_n}}} \quad (3)$$

Then the input of the TMCC is less than the threshold, the output is interpreted as logic '1'. For input voltage higher than threshold, the output will be logic '0'. The extra NOT gates perform the function of logical restoration of inverter outputs. This approach ensures great decrease in power and area consumption as the bulky resistors are replaced by inverters and no constant shut through current is present from VDD to ground. The ADC output is then transferred to 16:4 decoder which is connected to the digital feedback control (DFC) block. DFC is a digital comparator, which performs adjustment of feedback circuitry according to ADC output code.

One bit Mode Select (MS) signal is used for selection between SC topologies with different conversion ratios. The logic '0' and logic '1' values for MS corresponds to 1/3 and 1/2 conversion ratios respectively.

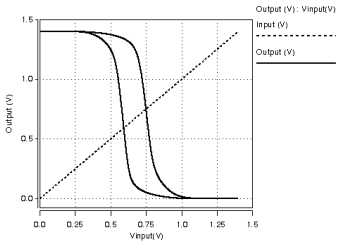

Fig. 4. Inverter threshold modulation

As the switched capacitor converters work with relatively low frequencies, a novel DCO circuit was proposed which consists of a digital control ring oscillator (RO), which generates the high frequency component of clock signal, and of a combinational block (CB) which uses the RO output to generate the low frequency component (Fig, 2).

Proposed RO is a 7 stage structure, where each stage consists of a 3 transistor XOR element and a transmission gate (Fig. 5). The delay of each stage is a summary of XOR and transmission (TG) gate delays which forms the output clock signal frequency. The delay of TG depends on the resistances of NMOS and PMOS transistors (Eq. 4) which are controlled by 4 bit digital code (Eq. 5). By manipulating the digital control, 16 fixed output clock frequencies can be obtained within output frequency range from 1.6GHz to 2.5GHz. The proposed DCO ensures up to 3 times less average power consumption than conventional analog VCOs.

$$t_{delay} = 0.7\ (R_n||R_p)C_{load} \quad (4)$$

$$R_{p,n} = \frac{VDD}{\frac{KP_{p,n}}{2}*\frac{(W_{p,n}+d0*W_{lp,n1}+\ldots+d3*W_{lp,n4})}{L}*(VDD-V_{THp,n})^2} \quad (5)$$

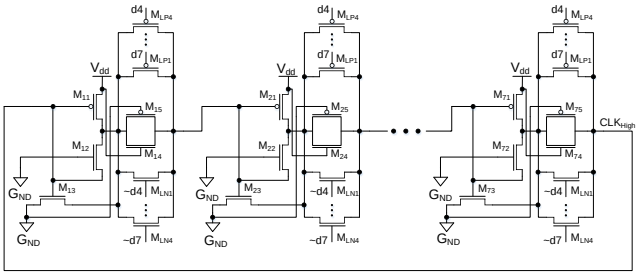

Fig. 5. Structure of Digital Control Ring Oscillator

The CB uses 4 bit Johnson counter and a digital comparator to generate the low-frequency clock signal. The CB output frequency is also controlled by 4 bit digital signal and varies from 120MHz to 1.2GHz. Hence, the output frequency range of proposed DCO is 2.38GHz. To provide similar frequency range with the usage of conventional ring oscillator, 40% more transistors must be used. With 8 bit overall frequency control, the proposed DCO provides acceptable frequency controllability while assuring less power consumption and transistor usage.

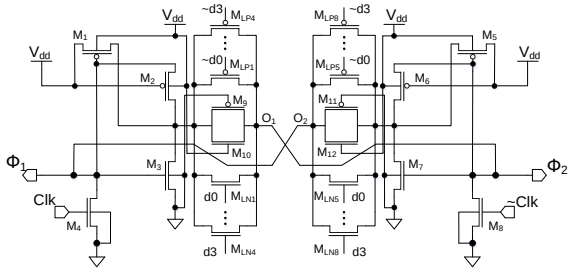

Fig. 6. Proposed non-overlap clock generator

The proposed NOCG (Fig. 6) is a back to back circuit which has similar structure as the RO stage [6]. By means of digital control code, both non-overlap period and rise/fall times of output two phase clock signal are controlled.

One of the major requirements for SC converter is the low output voltage ripple, which is the result of SC construction [7]. The current pulse on the flying capacitances decays gradually by RC time component, where R is the on-resistance of the switches and C is the flying or charge transfer capacitance. The difference between the current pulse and the load current is injected in the output capacitor, thus creating an output ripple (Eq. 6).

$$\Delta V = \frac{Q_{out}}{C_{Load}} \quad (6)$$

For heavy loading conditions with high switching frequency the output voltage ripple is relatively low. In order to have small output ripple for lights loads either the switching frequency must be increased or additional technique must be implemented. The increase of switching frequency will cause unreasonable leap of system power consumption. Hence the soft charging technique of flying capacitances is implemented with the usage of proposed NOCG which suggests opening the switch transistors gradually rather than in a step fashion. In this case the transistors' resistance is modulated such that the generated current on the flying capacitance matches the load current in each switching phase. Therefore no extra charge is injected in the output capacitance and the output ripple is be eliminated.

IV. Simulation Results

Proposed SC converted is designed using CMOS 28nm technology. Simulations where performed for input voltage equal to 1.4V. The clock signal generated by proposed digital control ring oscillator is shown in Fig. 7. The output frequency depends on the digital control code, and the pulse period varies from 392ps to 619ps.

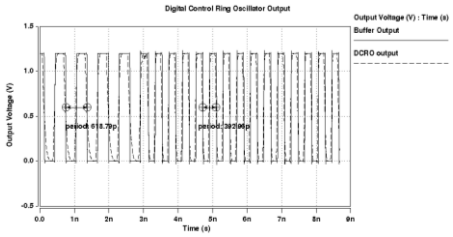

Fig. 7. High frequency output clock signal of RO

As shown in Fig. 8, output ripple at light load varies from 2.8mV to 5mV. At heavy loads converter operates at Fast Switching Limit (FSL) region with high switching frequency, therefore eliminating the output ripple at acceptable level of 5mV. For light loads because of soft charging technique the output ripple varies around 3mV.

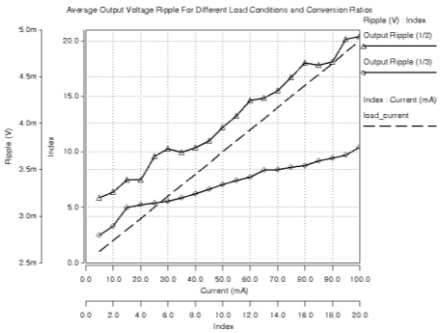

Fig. 8. Output ripple of the SC converter under different loading conditions

Fig. 9 shows the startup transient response of the converter which depends on the current topology of power cell. As it can be seen, the startup time for 1/2 topology is 70ns. Relatively slow startup time is caused by setup time of digital control circuitry of power cell.

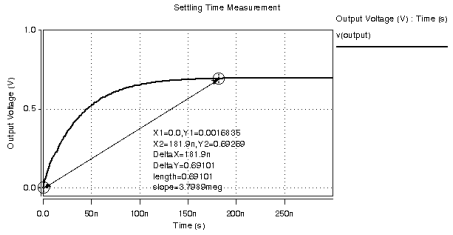

Fig. 9. Startup transient response

The usage of low power components and overall digital based feedback ensures high conversion efficiency over wide range of varying load conditions as shown in Fig.10.

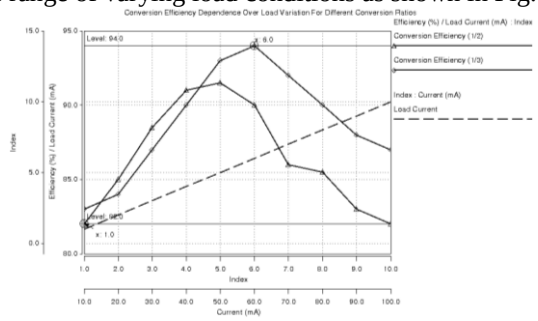

Fig. 10. Efficiency measurements of multi-topology converter at varying load conditions

Fig. 11 shows the transient response of the converter when load current is changed from 50mA to 10mA and the topology is switched from 1/3 to 1/2 and back. As shown in figure, the switching frequency is changed and the output voltage enters the permissible range during 70ns.

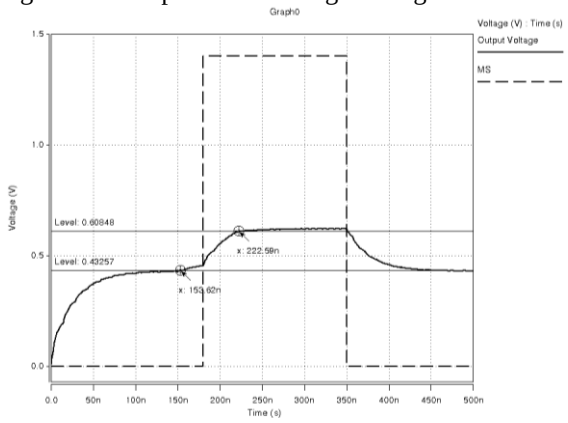

Fig. 11. SC converter transient response to load variation

Table 2 shows the performance comparison of proposed SC converter with similar designs [8] [9]. By means of the novel control methodology, the proposed design demonstrated the highest actual conversion efficiency, better startup and response characteristics as well as lower level of output voltage ripple.

TABLE 2. PERFORMANCE COMPARISON OF THE DESIGNED SC CONVERTER WITH SIMILAR DESIGNS IN THE LITERATURE

Parameter	Proposed Design	[8]	[9]
Voltage Conversion Ratio	1/2, 1/3	2/5	1/2, 1/3
Supply Voltage (V)	1.2 – 2.5	3.3	2.5V
Output Voltage (V)	0.4 – 1.25	1.25V	0.9-1.5
Theoretical max. Conversion Efficiency (%)	98	N/A	100
Average Conversion Efficiency (%)	89	64	50-66.7
Output Ripple (mV)	5	45	110
Cout (nF)	0.25	0.5	440
Cfly (nF)	0.8	3	6.72
Maximum output current (mA)	100	10.3	5
Maximal Switching Frequency (MHz)	200	40	1
Technology (nm CMOS)	28	18	0.35

V. CONCLUSION

A multi-topology SC converter with a novel control technique is proposed and the respective circuit designed. The usage of full digital control with low power components and dual ratio power cell configuration provided higher average conversion efficiency of 89% and lower output voltage ripple of 5mV compared with other designs. The other advantage of proposed circuit is the absence of reference voltage in feedback control circuit, which ensures easy integration and overall simplicity of usage. Main disadvantage of proposed converter is slightly slow start-up time and overall complexity of feedback control circuit.

ACKNOWLEDGMENTS

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Fully Integrated Low Power Temperature Measurement Circuit Design in 28nm Process

Armen Aleksandr Durgaryan, Abraham Henri Balabanyan and Vazgen Shavarsh Melikyan

Abstract – **This paper presents a new on-die temperature detection principle and its circuit implementation in a 28 nm CMOS process. The suggested fully integrated circuit is capable of converting IC temperature to voltage in a range of -40°C to 125°C. Compared to conventional methods of temperature sensing the suggested solution is process and supply voltage independent. The circuit provides means for easy control of output voltage range depending on application specifics, consumes less than 1.4 mW power and requires about an 800 um^2 chip area. The principle theory, circuit implementation, simulation results and their correlation with theoretical values are discussed.**

Keywords – **Temperature measurement, PVT compensation, logarithmic amplifier, on-die temperature, temperature detection**

I. Introduction

Rapidly growing level of integration and data rates result in significant IC core temperature variations and gradients during system operation [1-3]. Temperature variation seriously affects such parameters of modern IC elements as transistor threshold voltage, effective impedance as well as integrated resistor resistance and as a result can significantly degrade circuit performance. This becomes more and more critical as SoC operating frequencies increase resulting in lower timing budget margins and technology processes becoming more susceptible to PVT variations. In I/O circuits the temperature variation degrades output and input impedance affecting signal matching in transmission lines, hence negatively impacting signal integrity and timing parameters [4, 5]. Most modern SoC components employ integrated calibration mechanisms to allow tuning of crucial components back to specified parameters. Examples of such systems are such high speed I/O standards as USB and DDR [4] where output and input impedances are periodically calibrated to minimize PVT variation effects [5, 6]. Some state of the art standards like DDR4 [4] allow for background mode (online) tuning to compensate for temperature changes during circuit operation. The above mentioned reasons as well as number of other applications [2, 3] create demand for SoC compatible temperature sensors. External sensors and thermo-pair based sensors have a number of disadvantages such as measurement error due to temperature difference in IC core and package as well as additional manufacturing/production cost. There are number of solutions for integrated sensors including BJT current measurement and ring oscillator based ones [2, 3], however they usually share such disadvantages as high variability with process and voltage. Namely ring oscillator frequency will drift substantially with process variation, obscuring frequency drift due to temperature, hence making the measurement less correct. The process variation effects cannot be neglected for technologies below 90 nm. This paper suggests a principally new, fully integrated solution based on modified logarithmic amplifier pair output voltage difference amplification. Compared to existing integrated solutions the presented circuit is highly tolerant to technology and supply voltage variations, has comparatively small area and low power consumption. The theory, measurement results and their correlation are presented.

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II. Temperature Detection Suggested Principle

The principle of temperature detection is based on measuring the difference between two logarithmic amplifiers with a shared voltage bias and load resistance parameters, Fig.1.

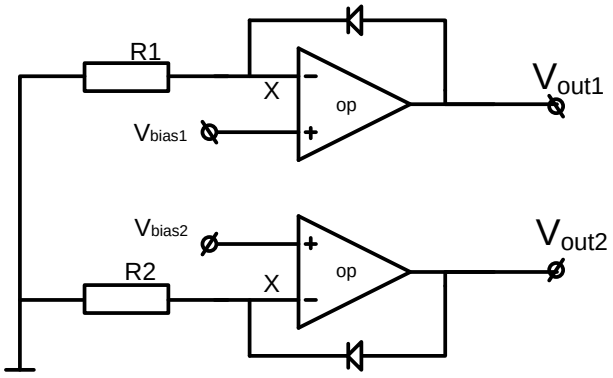

Fig. 1. Detection and sensing circuit principle

The bias voltage is generated internally and can be implemented by a simple resistive divider. The circuit can operate in two modes, when $V_{bias1}=V_{bias2}=V_{bias}$ (common bias mode), and when $V_{bias2}=m_bV_{bias1}$ (scaled bias mode, m_b is the bias scaling factor). Both current branches in Fig.1 have identical, preferably matched diodes. The resistors use identical structures with a different nominal value, achieved by a scaled number of parallel connected fingers. Poly-resistors available in all modern technology processes

can be used. Both branches are required to use the same single ended operational amplifier with shared bias current generators and properly matched critical elements. In common bias mode, the opamp negative inputs will be forced to V_{bias}, hence using diode current expression it can be easily shown that:

$$V_{out1} = V_{bias} + V_T \cdot ln\frac{V_{bias}}{R \cdot I_0} \quad (1)$$

The circuit branches separately behave like classic logarithmic circuits. If $R_2=m_rR_1$ a similar expression for V_{out2}, after simple transformations can be rewritten respectively as follows:

$$V_{out2} = V_{bias} + V_T \cdot \ln\frac{1}{m_r} + V_T \cdot \ln\frac{V_{bias}}{R \cdot I_0} \quad (2)$$

Substituting Eq.1 into Eq.2 for Vout2 and Vout1 voltage difference the following expression can be shown:

$$V_{out2} - V_{out1} = V_T \cdot \ln\frac{1}{m_r} = T \cdot \frac{k}{q} \cdot \ln\frac{1}{m_r} \quad (3)$$

Hence, the output voltage difference after differential amplification by A, (V_{det}) will be described as:

$$V_{det} = A \cdot V_T \cdot \ln\frac{1}{m_r} \quad (4)$$

As it can be seen from Eq.4 the detected voltage is strictly proportional to temperature and has no dependence on other factors such as operating voltage, logarithmic amplifier bias voltage and process corner. The parameters A and m_r serve as detected voltage scaling factors, which can be defined for a specific application. The Eq.1 and Eq.2 suggest that the same principle can be realized with a slightly different modification of the presented circuit, using the same load resistor value for both branches but different bias voltage values ($V_{bias2}=m_bV_{bias1}=m_bV_{bias}$) in Fig.1. For this case the expression (3) will be rewritten the following way:

$$V_{out2} - V_{out1} = (m_b - 1) \cdot V_{bias} + T \cdot \frac{k}{q} \cdot \ln(m_b) \quad (6)$$

The resistor scaling can be used along with bias voltage scaling in order to increase the detected voltage range:

$$V_{out2} - V_{out1} = (m_b - 1) \cdot V_{bias} + T \cdot \frac{k}{q} \ln(\frac{m_b}{m_r}) \quad (7)$$

The introduction of bias voltage scaling can be used to center the detected voltage range around a specific DC offset value.

III. Temperature Detection Circuit Description

The temperature detection system consists of the logarithmic amplification pair with sensing diodes, controlled gain differential to single amplifier, bias generation and control blocks, Fig.2. The control block implements basic digital logic and performs signal conditioning to control the bias generator operation mode, dual to single amplifier gain and allows to put the circuit into power down when detection is not required. The logarithmic amplification pair functions as a main temperature sensing block. It is implemented by the principle described in previous chapter, and consists of two identical operation amplifiers, two sensing diodes and a pair of resistors, Fig.1. The sensing diodes in this paper were implemented as forward biased drain-bulk diodes of PMOS devices. This solution can be preferred to conventional diodes or BJT devices for its considerably smaller area and better layout matching.

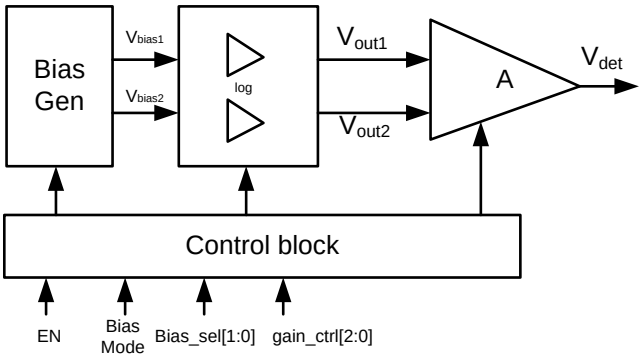

Fig. 2. Detection circuit block diagram

The behavior of the detection block is described by Eq.7. It can operate both in common and scaled bias voltage modes. In common bias mode the coefficient m_b equals to one hence the circuit outputs being described by expression (3). Different values of the aforementioned coefficient determine the detection voltage DC offset and range. The bias generator block (Fig.3) allows choosing between four m_b values, including the common bias mode.

It is activated by the control signal "ENn" and put into power down when the latter is de-asserted. In power down both the bias voltages are 0. The bias generator uses resistive dividers to generate bias voltage values. Vbias1 is controlled by the "bias_sel[1:0]" signal, and connects it to the respective output of the resistive divider through analog multiplexor. When bias_sel[1:0]=2b'0 and/or bias_mode=1 V_{bias2} and V_{bias1} voltages are shunted together through the multiplexor and additional pass-gate putting the circuit into common bias voltage mode. The control block logic is implemented in a way that when bias_mode=1 then bias_sel[1:0] is asserted 0, so the circuit is forced to common bias mode, table 1.

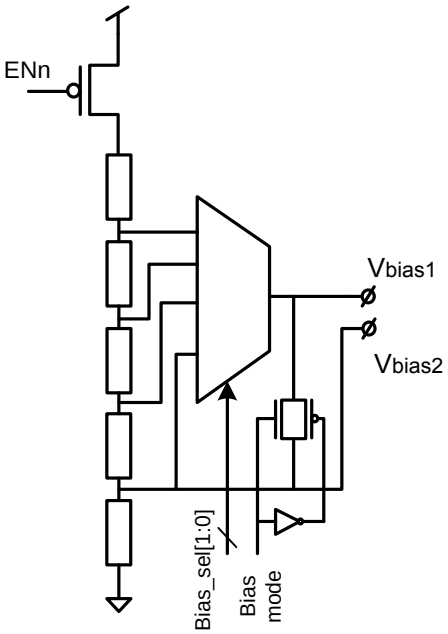

Fig. 3. Bias generation block

TABLE 1. BIAS GENERATOR MODES

ENn	Bias_mode	Bias_sel[1:0]	m_b
1	-	-	Power-down
0	0	0	1
0	0	1	2
0	0	2	3
0	0	3	4
0	1	-	1

The dual to single amplifier (Fig.4) is a modified instrumentation amplifier. The choice of this topology in this paper is attributed to the fact that these amplifiers are known for low offset and robustness.

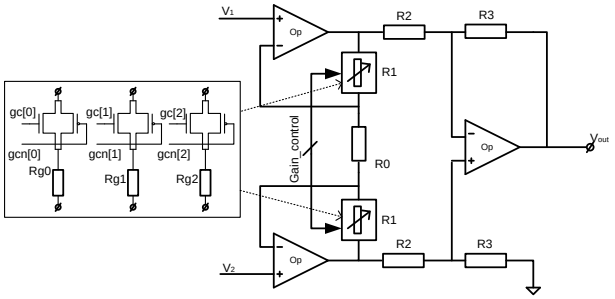

Fig. 4. Dual to single modified instrumentation amplifier

The amplifier gain is known to be described by following relationship:

$$A = (1 + \frac{2 \cdot R1}{R0}) \cdot \frac{R3}{R2} \quad (8)$$

The effective detected voltage for general and common bias modes will be described respectively as:

$$V_{det} = A \cdot (m_b - 1) \cdot V_{bias} + A \cdot T \cdot \frac{k}{q} \ln(\frac{m_b}{m_r}) \quad (9)$$

$$V_{det} = A \cdot T \cdot \frac{k}{q} \ln(\frac{1}{m_r}) \quad (10)$$

In this paper the conventional amplifier was modified to obtain gain control allowing for detected voltage range additional control. On the circuit level this is achieved using controlled impedance matrices for the R1 resistor, Fig. 4. The pass gate input signals are related to control block gain_ctrl[2:0] inputs with simple digital logic. The pass gate transistors are sized to have significantly less impedance than the resistors Rg0, Rg1 and Rg2, which eventually determine the gain. The designed amplifier has gain options equal to 1, 3 and 5. The nominal gain as well as controlled gain value number can be modified depending on specific design requirements.

IV. DESIGN AND SIMULATION SETUP

The proposed system was designed and implemented for a 28 nm CMOS process, with 0.9 V core device and 1.8 V thick-gate nominal voltages.

The schematic/physical design has been performed using the Synopsys Custom Designer tool. Global corner and Monte-Carlo simulations [7] were performed using Synopsys Hspice[7] and Finesim analog simulators. For graph plotting and numerical measurements Synopsys Cosmosscope tool was used.

V. SIMULATION RESULTS AND DISCUSSION

For global corner simulations the following cases were considered SS, TT, FF, FS and SF, with ±10 % of nominal supply voltage variations. The temperature detection circuit was simulated for -40°C to 125°C temperature range. Fig.5 shows DC sweep simulation results for the common bias operation mode. The considered circuit had the resistor scaling factor m_r=1/12 and dual to single amplifier gain was set to 3. The mentioned plot shows detector circuit voltage dependence on temperature in range of -40°C to125°C for SS minimal voltage, TT typical voltage and FF maximal voltage PVT corners. The dashed line corresponds to ideal dependence following from expression (10). The simulated voltage values show less than 3 mV deviation from theoretical value. As the formula (10) suggests the detected voltage is expected to have no dependence in supply voltage or process corner. This behavior is confirmed by simulations. The zoomed segment on Fig.5 suggests that detected voltage difference between slow and fast corners is less than 0.1 mV. The detected voltage is 196.6 mV at room temperature with range of 152 mV to 260 mV for -40°C to 125°C temperature range. The detected voltage can be stored or processed after analog to digital conversion. A 6 bit digital conversion will yield ~2.5°C per bit temperature detection resolution.

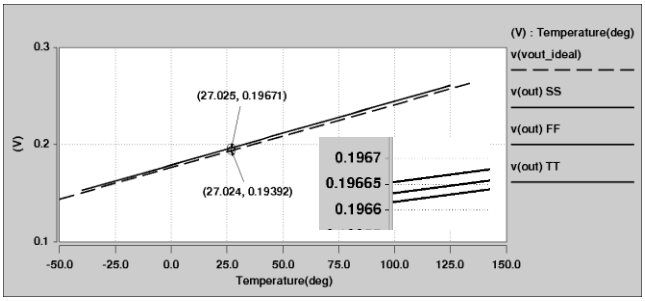

Fig. 5. Detector output voltage dependence on temperature, common bias mode

In some cases it may be preferred to have wider control over detection range and detected voltage DC offset, then scaled bias detection mode can be used. The voltage offset will be determined by m_b bias voltage scaling factor, as follows from (9). Fig.6 simulation plot shows detection voltage for 3 PVT corners when m_r=1/4, m_b=3 and A=3. As the theoretical expression and simulation results suggest the circuit output voltage offset will be dependent on supply variations. This can be useful when the analog to digital convertor is connected to the same supply, cancelling the detected value degradation due to ADC supply variations. The detected voltage at room temperature for slow, typical and fast cases is respectively 790 mV, 856 mV and 922 mV. Detection range is identical to the previous case. The presented circuit has practically no dependence on process corner and in case of common bias mode on supply voltage as well. Due to its symmetrical and fully differential structure the offsets of detection pair operational amplifiers cancel each other thus having no effect on detected voltage value. The sensing diodes can introduce detection error if not properly

matched. Fig.7 shows 3σ, 100 run Monte-Carlo simulation results for the common bias mode at typical simulation corner. The statistical simulation has shown 3σ = 2.2 mV for the detected voltage, which in case of 6 bit conversion is less than 1 bit error. The proposed circuit consumes 1.37 mW maximal power in fast PVT corner and requires around 800 um^2 silicon area with PMOS devices used for sensing diodes.

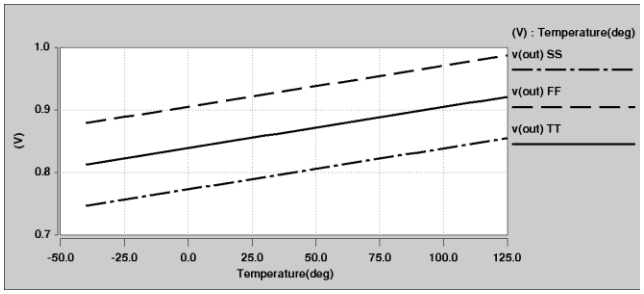

Fig. 6. Detector output voltage dependence on temperature, scaled bias mode

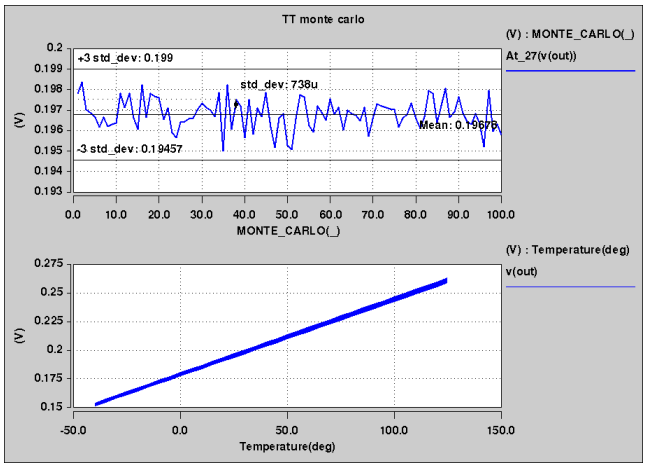

Fig. 7. Statistical simulation results in common bias mode

The summary for the simulation results is presented in the table 2.

TABLE 2. TEMPERATURE DETECTOR SUMMARY RESULTS

	Common bias mode			**Scaled Bias mode**		
	-40^{0}C	**25^{0}C**	**125^{0}C**	**-40^{0}C**	**25^{0}C**	**125^{0}C**
V_{det}; SS min. voltage **(mV)**	152.8	196.59	260.09	746	790	855
V_{det}; TT nom. voltage **(mV)**	152.81	196.6	260.1	812	856	920
V_{det}; FF max. voltage **(mV)**	152.82	196.62	260.12	878	922	0.99
Theore-tical target value	150.4	194	257	-	-	-
Output voltage range (mV)	108			107		
Monte carlo **σV_{det} (mV)**	0.738			0.788		
Max power; FF max. voltage **(mW)**	1.31			1.37		

As demonstrated in the simulation results, the detected voltage in common bias mode has very high tolerance to process and voltage conditions yielding stable absolute voltage. The scaled bias mode allows the output voltage to drift in line with supply voltage, which can be practical in cases when analog to digital conversion is performed from the same supply. The detected voltage values and range can be easily tuned for a specific application since the detection circuit simulation values are in precise correlation (less than 2% deviation) with presented theoretical expressions.

VI. CONCLUSION

A principally new temperature detention method and its circuit implementation in 28 nm CMOS technology are presented. The principle is based on differential amplification of logarithmic amplifier outputs under scaled bias conditions. The designed circuit is fully integrated, uses no external components and requires about 800 um^2 of on-die area and less than 1.4 mW maximal power consumption. The theory of the suggested method is presented and compared to simulation results. Simulations of temperature detection voltage have shown very good correlation with theoretically expected values for temperature range of -40°C to 125°C and practically no dependence on process and supply variation. The design allows for output voltage range and DC offset values to be easily adjusted for a specific application.

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Green Fluorescent Protein Hydrogen Bonds Compared to Microelectronic Devices

Rostislav Pavlov Rusev, George Vasilev Angelov, Elitsa Emilova Gieva, Boris Petkov Atanasov and Marin Hristov Hristov

Abstract – **Green Fluorescent Protein hydrogen bonding network in ground state is investigated. The network consists of chromophore, water molecule, and protein residues around the chromophore that participate in the photocycle. Proton transfer characteristics for each hydrogen bond are obtained. It is found that the proton transfer parameter depends on donor and acceptor electrostatic potentials, cooperative effects, and the sum of protein electrostatic potentials. The shapes of proton transfer parameters versus donor and acceptor electrostatic potentials are similar to *I-V* characteristics of 2- or 3-terminal devices. In addition, there are characteristics that are similar to reverse diode characteristic, output characteristic of field effect transistor, current source. The chromophore and glutamine acid residuum in hydrogen bonding networks have functions similar to microelectronic multiplexer.**

Keywords – **Hydrogen bonding networks, green fluorescent protein, proton transfer characteristics.**

I. Introduction

Green fluorescent protein (GFP) is one of the most wide spread proteins. It has application to biology and medicine as a biological marker, in bioelectronics – for biosensors [1], for photodiodes [2]. Its chromophore and fluorescence properties are the basis for GFP applications. During the photocycle, in ground state A the chromophore is neutral and can be photoexcited at 397 nm to state *A**. State *A** evolves very rapidly to an intermediate state *I** with decay times on the order of a few picoseconds. State *I** can either decay to the ground state *I* (and later revert back to *A*) or it can further evolve to state *B**, eventually relaxing to *B* [3]. The chromophore is bonded to a hydrogen bonding network (HBN). The HBN plays crucial role in the overall photocycle and in chromophore stabilization.

In the present paper we will investigate the proton transfer via hydrogen bonds formed around and with the chromophore. We will also examine how the proton transfer depends on donor-acceptor potentials, and surrounding residues. We will compare the proton transfer characteristics to the characteristics of known microelectronic devices to find its potential applications in bioelectronics.

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II. Materials and Methods

We will use a wild type green fluorescent protein in A state (neutral chromophores). The high-resolution crystallographic structure of GFP (2wur) is taken from Protein Data Bank [4]. It is made by X-ray diffraction at resolution of 0.9 Å. The chromophore-atom HBN is visualized by Vega ZZ [5]. The distances between hydrogen bond donors and acceptors are measure by Vega ZZ.

The pH-dependent electrostatic potentials $\Phi_{el,i}$ and the *pKa* of ionizable groups are calculated by PHEI server [6] using the followoing equations:

$$\Phi_{el,i}(pH) = 2.3RT\sum_{j\neq i}\{Q_j(pH)W_{ij}[1-(SA_i+SA_j)/2]\} \quad (1)$$

where $Q_j(pH)$ is defined by degree of dissociation or statistical mechanical proton population of given H+-binding site; W_{ij} is pair-wise interaction; *SA* is solvent area.

The pKa is calculated by

$$pKa_i(pH) = pKa_{\text{int}i} + \\ +\frac{1}{2.3RT}\sum_{j\neq i}\{Q_j(pH)(W_{ij}-C)[1-(SA_i+SA_j)/2]\} \quad (2)$$

where R – gas constant, T – temperature in Kelvins, pKa_{int} is the *pKa* of the *i*-th site according to model compounds.

In this way we calculate the electrostatic potential of each participant in the HBN. Using the calculated *pKa*-s we can also calculate the bottom of potential wells of each donor and acceptor; these bottom potential wells are needed of the calculation of proton transfer *K*.

For the calculation of proton transfer *K*, we have developed a custom code that is based on Marcus parameterization [7]. In this parameterization, the cooperative effects and surrounding residue electrostatic effects are taken into account. The *K* parameter is calculated by:

$$K = \frac{k_B T}{2\pi} \exp(-\frac{Eb - h\omega/2}{k_B T}) \quad (1)$$

where: K – proton transfer parameter, k_B – Boltzmann constant, Eb – energy barrier, h – Planck constant, ω – frequency, T – temperature [°K].

The energy barrier is calculated by:

$$Eb = (s_A(R(DA) - t_A)^2 + v_A) + s_B E_{12} + \\ + (s_C \exp(-t_C(R(DA) - 2)) + v_C)(E_{12})^2 \quad (2)$$

where $R(DA)$ — distance between the donating and accepting atoms, E_{12} — energetic difference between bottom potential wells donating and accepting atoms; the values of other parameters are taken from [7]. The proton transfer parameter is measured in [J/mol] and the proton current is proportional to K.

It should be noted that the higher the K parameter, the easier the positive charge (proton) transfer is. Therefore, with higher K we obtain larger current.

III. Results and Discussion

Green fluorescent protein hydrogen bonding network with a chromophore is shown in Fig. 1. The distances between each donor and acceptor of hydrogen bonds are given in Table 1.

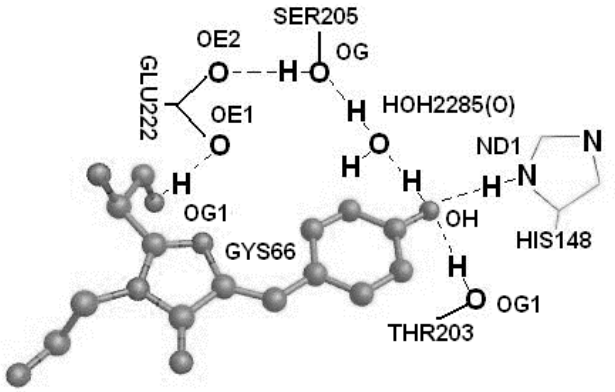

Fig. 1. Hydrogen bonding network : OH and OG1 – oxygen atoms of chromophore GYS66, ND1 – nitrogen atom of Histidine residue HIS148, OG1 – oxygen atoms of Threonine residue THR203, O – oxygen atoms of water molecule HOH2285, OG – oxygen atoms of Serine residue SER205, OE1 and OE2 – oxygen atoms of Glutamic acid residue GLU222.

Table 1. Distance between donor and acceptor of hydrogen bonds

Hydrogen Bond	Distance [Å]
HIS148(ND1)…(OH)66GYS	2,79
THR203(OG1)…(OH)66GYS	2,69
GYS66(OH)…(O)2285HOH	2,66
HOH2285(O)…(OG)205SER	2,63
SER205(OG)…(OE2)222GLU	2,59
GYS66(OG1)…(OE1)222GLU	2,78

In Fig. 1, the chromophore atom (OH)66GYS is proton donor of caged water molecule HOH2285. From the other hand, it is a proton acceptor in the hydrogen bonds with (ND1)148HIS and (OG1)203THR. The water molecule is also proton donor of SER205 which is on its turn a proton donor of the strong proton acceptor GLU222. Note that in addition GLU222 is acceptor of the chromophore atom (OG1)66GYS.

For the purposes of our paper we will investigate only this part of the HBN (close to the chromophore) although the HBNB is branched till the periphery of the protein including tens of residues (not showed in Fig. 1).

After determination of the participants of the HBN around the GFP chromophore and their donor/acceptor role, we start to investigate the characteristics of the hydrogen bonds. For this reason we vary the pH of the environment around the entire protein. The pH variation initiates polarization and ionization of the groups. Immediately, the charges of the system of protein residues, chromophore and water molecules are redistributed and the potentials of all atoms are changed (including investigated donor and acceptor atoms from target HBN). Subsequently, changing the charges result in change of the proton transfer conditions. The proton transfer parameters (K) versus electrostatic potentials (El. pot.) of hydrogen bonding donors and acceptors are shown in Fig. 2 to Fig. 4.

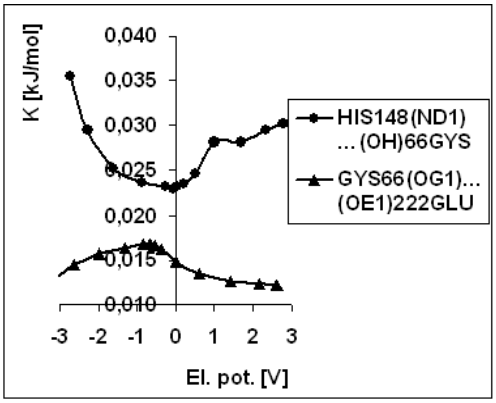

Fig. 2. Proton transfer parameter (K) vs. electrostatic potentials (El. pot.) curve of HIS148(ND1)…(OH)66GYS and GYS66(OG1)…(OE1)222GLU hydrogen bonds.

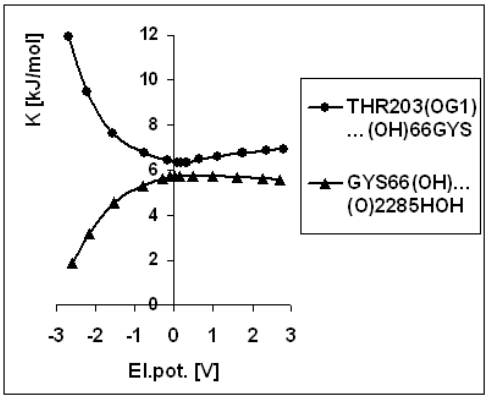

Fig. 3. Proton transfer parameter (K) vs. electrostatic potentials (El. pot.) curve of THR203(OG1)…(OH)66GYS and GYS66(OH)…(O)2285HOH hydrogen bonds.

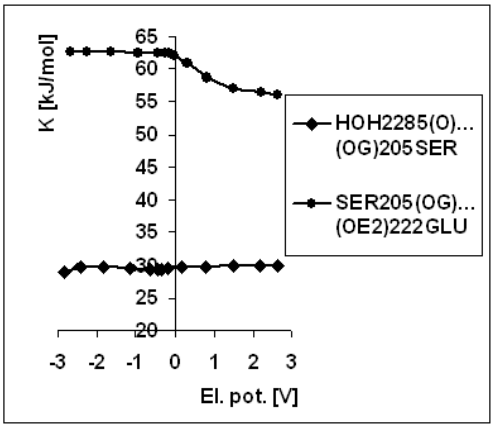

Fig. 4. Proton transfer parameter (K) vs. electrostatic potentials (El. pot.) curve of HOH2285(O)…(OG)205SER and SER205(OG)…(OE2)222GLU hydrogen bonds.

Figures 2-4 show that the electrostatic potential interval is between –3 to +3 [V]. The *K*-range is large (between 10^{-3} to 10^{2}). The reason of this phenomenon are donor-acceptor atom distances, which change between 2.59 Å to 2.79 Å. The value of K exponentially increases with donor-acceptor distance decrease. There are various shapes in Fig. 2-4 : linear, parabolic, S-shaped curves. The shapes are determine by the type of donor and acceptor atoms and the number of hydrogen bonds in which a single donor/acceptor atom forms (bifurcate hydrogen bonds). For example (OH)66GYS participate in three hydrogen bonds.

From bioelectronics point of view, the *K* vs. (El.pot.) characteristics of THR203(OG1) ….(OH)66GYS hydrogen bond is similar to reverse diode (with inverted *I-V* characteristic of a diode). The characteristic of the hydrogen bond formed by the chromophore and the water molecule GYS66(OH) is similar to the output characteristic of a filed effect transistor. On the other hand, there is no change observed in the hydrogen bond between HOH2285(O)….(OG)205SER when varying (El.pot.) in the *K* vs. (El.pot.) characteristics; hence, this hydrogen bond behaves similarly to a current source. Similar characteristics are obtained for hydrogen bonding network from β-lactamase protein [8].

The characteristics of the other hydrogen bonds – parabolic and S-shaped – no direct analogy to conventional microelectronic devices can be found. The characteristics are non-linear which implies amplifying properties.

In general, the hydrogen bonds might be compared to microelectronic devices; the proton donor and proton acceptor can be presented as drain and source electrodes. The sum of electrostatic potential (function of pH) in a given hydrogen bond can be presented as a gate electrode. In the investigations of the hydrogen bonding network, the chromophore atom GYS66(OH) can sum signals from different donors similar to microelectronic multiplexer. The hypothesis applies to GLU222 residue. The oxygen atoms OE1 and OE2 have strong proton acceptor properties. They take part in two separate hydrogen bonds. But due to the redistribution of electronic density between the two atoms, the proton transfers in the two bonds will influence onto each other.

If we consider the entire hydrogen bonding network as a single device, we find that the characteristics of its inputs at the acceptor GYS66(OH) are mirrored to the characteristics of its output at the donor GYS66(OG1) (cf. Fig. 2); both characteristics are parabolic, mirrored to each other with inflex point at approx. –0.5 V. Hence, the entire HBN will behave as an inverter.

IV. CONCLUSION

The study of proton transfer in hydrogen bonds with the chromophore of wild type green fluorescent protein shows that the proton transfer parameter depends on donor and acceptor electrostatic potentials, and the sum of protein electrostatic potential. The obtained curves of proton transfer parameters versus donor and acceptor electrostatic potentials are similar to *I-V* characteristics of 2- or 3-terminal devices. In addition, some of the characteristics are similar to the *I-V* characteristics of a reverse diode (a diode with an inverted characteristic), field effect transistor, current source. The chromophore and glutamine acid residues in the hydrogen bonding networks exhibit functions similar to microelectronic multiplexers.

ACKNOWLEDGMENT

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Impact of Energy Band Structure on CNTFET Output Characteristics

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Abstract – **The electronic band structure of the nanotube is a main factor controlling the device performance of Carbon Nanotube Field Effect Transistors (CNTFETs). In this paper four different calculation models of the band structure of a zig zag carbon nanotube are used to demonstrate the influence of the electronic band structure on device characteristics. The results of calculation of the energy band structure by the different methods are then analyzed.**

Keywords – **Graphene, nanoribbon, zigzag**, **carbon nanotube (CNT), CNTFET, energy band structure**

I. INTRODUCTION

The semiconductor device down scaling, that follows the Moore's law, has been the main driver of technology and performance advancements in the last decades [1]. Present day conventional CMOS technologies reached the 14-nm technology node and very soon will go down to 10 nm, 7 nm and 5 nm nodes [2]. Device scaling has faced critical limitations related to fabrication technology and device performances – leakage of carriers through the thin gate oxides and leakage from source to drain, and from drain to body all due to quantum mechanical tunneling, control of dopant atoms density and location in the transistor channel as well as the source drain region, the finite sub-threshold slope and a plethora of other short-channel and narrow channel effects.

Different principal directions for finding solutions to overcome these limitations are proposed. Some of them focus on modification of existing structures and technologies to extend their scalability. Other involve the use of novel materials and technologies to replace the existing bulk silicon CMOS technology.

Despite all the limitations and challenges related to deice scaling, silicon based semiconductor technology will continue to scale down. Alternatives to conventional bulk silicon transistors such as FinFETs, that allow for fabrication of nanoscaled devices, are already present in the mainstream CMOS technologies. Other modifications of the conventional technology are focused towards implementation of novel materials and structures in the transistor channel, viz. carbon nanotubes (CNTs), to obtain higher mobility in the channel.

Graphene is a promising candidate for implementation in the future electronic devices in order to significantly boost their performance [3]. Concerning its structure, the graphene is a hexagonal monolayer sheet carbon atoms that form a 2D hexagonal lattice similar to a honeycomb. A graphene nanoribbon is called any strip that is cut out of the graphene sheet (Fig. 1). Alternatively, a nanoribbon can be thought of as an unzipped carbon nanotube (which in fact is one of the ways of nanotube fabrication).

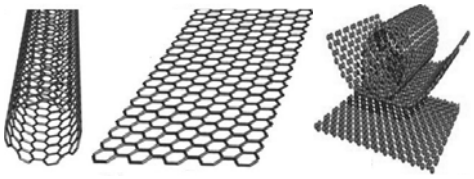

Fig. 1. Structure of single-walled CNT (*left*) and monolayer graphene nanoribbon (*middle*), and its formation (*right*).

Graphene nanoribbons are obtained by patterning a graphene sheet into strips. The boundaries of the strip (nanoribbon) can have either zigzag, or armchair, or chiral (irregular) shape [4], [5] (Fig. 2).

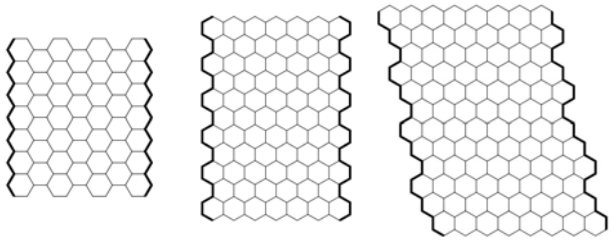

Fig. 2. Structure of a zigzag (*left*), armchair (*middle*), and chiral (*right*) graphene nanoribbon.

From energy band structure point of view, graphene is a semiconductor with zero band-gap. This is not suitable for electronic devices because in order to operate they need a band gap. For this reason, nanoribbons attract special interest as they allow to have a band gap. Combinations of monolayer and bilayer junctions are assumed to be used as switches by applying a gate voltage.

In this paper we examine four different models of band structure of 3 zigzag nanotubes: semiconducting (19,0), metallic (15,0) and semiconducting (13,0) nanotubes.

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II. CARBON NANOTUBE FETS

Carbon Nanotube Field Effect Transistor (CNTFET) implements a carbon nanotube (CNT) in the transistor channel. A single-wall CNT (SWCNT) consists of single-layer nanoribbon rolled up in as a cylinder. The relatively straightforward implementation of manufacturing process to the state-of-the-art CMOS technology makes CNTFETs a very promising alternative to conventional MOSFETs for channel lengths sizes under 10 nm [6].

An SWCNT behaves as either a conductor or a semiconductor, depending on the particular atom arrangement when forming the nanotube cylinder. The arrangement is described and defined by the chirality vector (*n, m*). Chirality of is a crucial parameter in calculation of the CNT band structure [7]. The chirality and the energy bang structure determine whether a CNT is metallic or semiconducting. There is an empirical rule to determine CNT conductivity: if $n = m$ or $n - m = 3j$, where j is an integer, the nanotube is metallic; otherwise, the nanotube is semiconducting [8]. In Table 1 we list some chiralities of different zigzag CNTs with some parameters calculated in Matlab.

TABLE 1. PARAMETERS AND CONDUCTIVITY OF ZIGZAG TYPE CNTS

Ch	Dt [nm]	Channel [nm]	Num	E_g [eV]	Conduc-tivity
(5,0)	0.391	1.23	10	2.3	semic.
(7,0)	0.548	1.72	14	1.7	semic.
(9,0)	0.704	2.21	18	1.3	metal
(10,0)	0.783	2.46	20	1.1	semic.
(13,0)	0.101	3.19	26	0.84	semic.
(15,0)	1.174	3.69	30	0.60	metal
(19,0)	1.487	4.67	38	0.58	semiv.
(26,0)	2.035	6.396	52	0.44	semic.

Although there are several types of CNTFET structure, the most common one is shown in Fig. 3. The CNTFET *I–V* characteristics are similar to the characteristics of the conventional MOSFET.

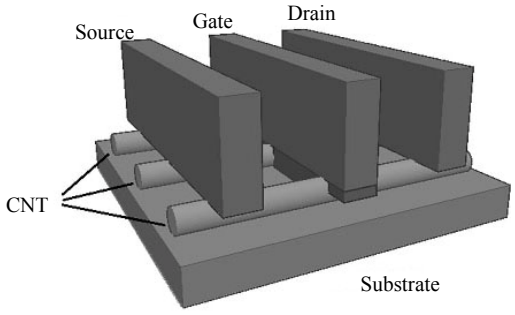

Fig. 3. Typical structure of a CNTEFT.

Two of the leading research groups on CNTFETs are at Stanford University and at IBM. The Stanford group created a carbon nanotube processor consisting of some 178 transistors. Each of them has carbon nanotubes with length between 10 to 200 nm [9], [10], [11]. The IBM Systems and Technology Group has demonstrated individual carbon nanotube transistors with channels smaller than 10 nm with better performance (faster, more energy efficient) than the silicon MOSFETs [6].

III. ENERGY BAND CALCULATION APPROACHES

The one and only complete behavioral compact model of CNTFET so far is the Stanford University CNTFET model [12], [13]. The model was released in 2008 and since then it is constantly updated by adding or refining different features [8]. The latest version of the Stanford model is Virtual-Source Carbon Nanotube FET (VS-CNFET) [14], [15]. It describes semi-empirically the *I-V* characteristics in a short-channel FET. The difference between the original Stanford CNFET model and the VS-CNFET model is in the approach of modeling the carrier transport.

There are different methods for calculation of the energy band structure (the *E-k* dispersion). The Density Functional Theory (DFT) that is based on Hohenberg-Kohn theorems [16] and the Kohn-Sham equations [17] is most frequently used. However, it requires a lot of computational resources due to its complex equations.

Tight-binding (TB) approaches for calculations of band structure are also popular for energy band calculation due to their computational efficiency and the atomistic nature of the treatment [18], [19]; in particular the orthogonal p_z tight-binding (OTB) approach has been widely used for CNTs structures calculations [20]. Slater–Koster tight-binding scheme is also employed sometimes [21].

For CNTs diameters less than 1 nm, the approach based on the Extended Hückel Theory (EHT) is usually applied [22], [23]. The main difference between a common OTB approach and EHT is that the orbital basis functions are nonorthogonal in the latter. In contrast to OTB, the EHT-basis functions are formulated explicitly which allows for easier calculation of Hamiltonian matrix elements.

We use the original Stanford CNFET model [12], [13] coded in Verilog-A to perform simulations in Cadence Spectre circuit simulator. We do several simulations, each time using a different Verilog-A code for calculation of the *E-k* dispersion relationship, and in particular we modify the perpendicular component of the energy subband in accordance with the above described different approaches for energy band structure calculation.

Afterwards, we simulate the *E-k* dispersion relationship in Matlab using the numerical approach described in [24] that is also used in the original Stanford CNFET model. In the Stanford model the Born-Karman boundary conditions on both the circumferential and axial direction are used [12].

Next we do simulations in VirtualNanoLab [25] using the above calculation approaches in order to compare the results with the results of Verilog-A and Matlab calculations.

Finally, we input back in the original Verilog-A code the results obtained by the simulations in VirtualNanoLab and Matlab. In this way, we calibrate the initial Verilog-A model.

IV. BAND STRUCTURE MODELS

The band structure of CNTs can be computed by substituting the allowed wavevectors into the energy

dispersion. NNTB energy *E-k* dispersion relation of graphene is described in Eq. (1).

$$E(k) = \pm\gamma\sqrt{1+4\cos\left(\frac{\sqrt{3}a}{2}k_x\right)\cos\left(\frac{a}{2}k_y\right)+4\cos^2\left(\frac{a}{2}k_y\right)} \quad (1)$$

where the plus and minus signs denote the conduction and valence band respectively. *Kx* and *Ky* are the vector components describing the geometry and chirality of the CNT; they are described with Eq. (2) and Eq. (3).

$$Kx = \frac{2\pi\sqrt{3}aj(n+m)Ch + a^3k(n^3-m^3)}{2Ch^3} \quad (2)$$

$$Ky = \frac{\sqrt{3}ak(n+m)Ch + 2\pi aj(n-m)}{2Ch^2} \quad (3)$$

$$k = \frac{2\pi}{NucT}l, l = 0,1,...., Nuc-l, \quad (4)$$

where *Ch* is the chiral vector, *l* is determined by the unique solution of *K*, restricted to the first Brillouin zone. *K* determines the wavevectors within the Brillouin zone that lead to the Bloch wave function. The wave vector *q* describes CNT along the circumferential direction Eq. (5).

$$q = \frac{2\pi}{Ch}j, j = 0,1,...j_{\max} \quad (5)$$

The band structure of the zigzag semiconducting (19,0) nanotube is calculated using the numerical approach described in [18]. The zigzag CNT is an attractive type of nanotube because of its high symmetry. It leads to a simple analytical expression of many solid-states properties. The energy dispersion for zigzag CNTs can be obtained from the Brillouin zone wavevector (Eq. 6) [24].

$$E(j,k) = \pm\gamma\sqrt{1+4\cos\left(\frac{\sqrt{3}ka}{2}\right)\cos\left(\frac{j\pi}{n}\right)+4\cos^2\left(\frac{j\pi}{n}\right)} \quad (6)$$

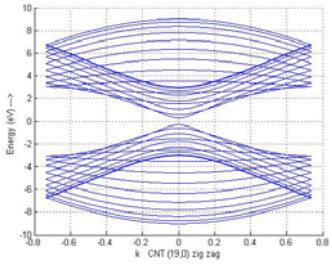

Fig. 4. Band structure of (19,0) zigzag nanotube containing 38 1D-subbands in the conducting and valence bands

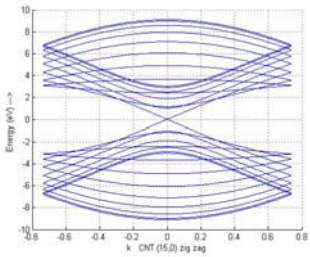

Fig. 5. Band structure of (15,0) zigzag nanotube containing 30 1D-subbands in the conducting and valence bands

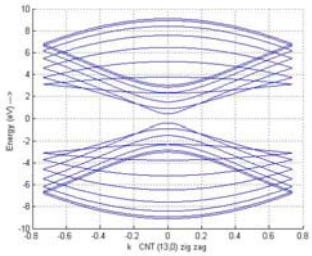

Fig. 6. Band structure of (13,0) zigzag nanotube containing 26 1D-subbands in the conducting and valence bands

In Fig. 4, 5 and 6 we show the band structure for semiconducting (19,0), metal (15,0) and semiconducting (13,0) nanotubes calculated in Matlab using the numerical approach described in [24]. The CNT diameters are 1.487 nm, 1.174 nm, and 0.101 nm respectively. In Fig. 5 the metallic CNT shows a band degeneracy at 0 eV and $k = \pm\pi/(\sqrt{3}a)$. The semiconducting (19,0) CNT has a bandgap of 0.58 eV.

Fig. 7, 8 and 9 plot the band structure of semiconducting (19,0), metal (15,0) and semiconducting (13,0) nanotubes calculated using VirtualNanoLab [25] with its band structure calculators using DFT, extended Hückel and Slater-Koster approaches.

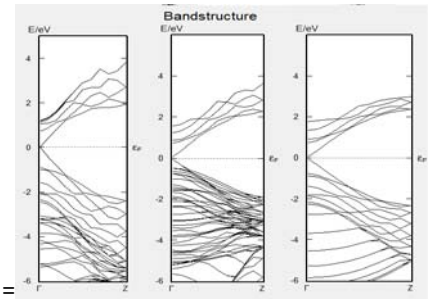

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Fig. 7. Calculation using a) DFT, b) Hückel and c) Slater-Koster calculator in the semiconducting zigzag (15,0) CNT

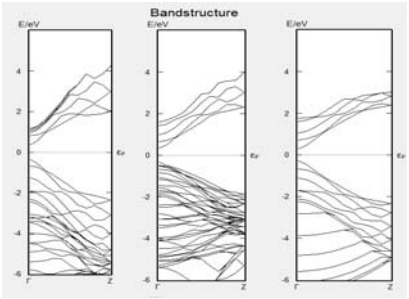

Fig. 8. Calculation using (a) DFT, (b) Hückel, and (c) Slater-Koster calculator in the semiconducting zig zag (13,0) CNT

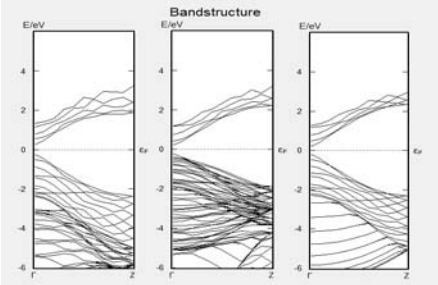

Fig. 9. Calculation using (a) DFT, (b) Hückel and (c) Slater-Koster calculator in the semiconducting zig zag (19,0) CNT

V. SIMULATION RESULTS

Simulation results show a change in the energy of the first conduction zone varying between 0.2001 to 0.2236 eV. In order to estimate the impact of the first energy band on the output *I-V* characteristics of the CNTFET the simulated output characteristics are shown in Fig. 7.

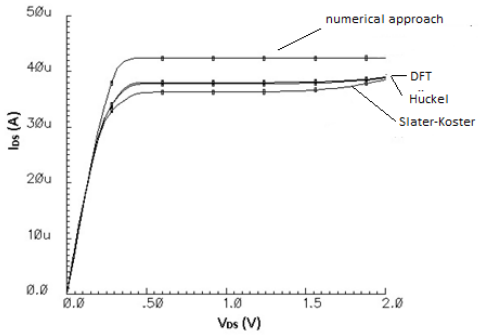

Fig. 7. I_{DS} (V_{DS}) at V_{GS} = 0.9 V results for the (19,0) CNTFET using numerical approach, DFT, Hückel and Slater-Koster calculator in CNTFET

The drain current value calculated by the numerical method is IDS = 0.42 μA. When applying the methods of DFT, extended Hückel, and Slater-Koster the drain current is IDS = 0.38 μA, 0.382 μA, and 0.3782 μA respectively.

VI. CONCLUSION

In this paper four different calculation models of the band structure of a zigzag (19,0) carbon nanotube has been studied using numerical, DFT, Slater-Koster and Hückel calculation approaches. We compared the results from the above mentioned approaches in Matlab and input them back in the original Verilog-A code. In result the impact of electronic band structure on device output characteristics has been demonstrated.

ACKNOWLEDGMENT

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Investigation of Colpitts VCO Designed on 0.35 µm Technology

Tihomir Sashev Brusev

Abstract – **In this paper is presented Colpitts voltage controlled oscillator (VCO) designed with Cadence on AMS SiGe BiCMOS 0.35 µm technology. The frequency of oscillation f_o of VCO is equal to 2.5 GHz, while the supply voltage V_{DD} of the investigated circuits is equal to 2.5 V. The obtained result shows that phase noise of Colpitts VCO is -103 dBc/Hz at a 100kHz offset and -115.6 dBc/Hz at a 400kHz offset. The f_o of Colpitts VCO can be adjusted from 2.2 GHz to 2.5 GHz, when control voltage is changed in the range between 2.5 V and 0 V.**

Keywords – **Collpits VCO, Integrated circuits (IC), SiGe BiCMOS 0.35 µm technology, Cadence.**

I. INTRODUCTION

The wireless communication standard fourth generation Long-Term Evolution (4G LTE) allows transfer of large date packages in the real time, because orthogonal frequency division multiplexing (OFDM) modulation is used. The signal is transferred by several sub-carrier frequencies. Thus the spectrum is used very efficiently [1]. One of main requirements in 4G LTE standard is VCO to have low phase noise [2]. In Fig. 1 is presented the block diagram of wireless transceiver, where PA is power amplifier and LNA is low-noise amplifier [3].

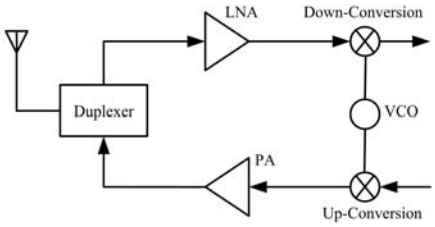

Fig. 1. Block circuit of the wireless transceiver.

The main goal of this paper is to be designed VCO with low phase noise. Cross-coupled LC VCO architectures are widely proposed in the literature as good choice for low phase noise oscillator circuits [4], [5]. The obtained results from this investigation show that Colpitts VCO is an alternative as oscillator with low phase noise performance [5]. Differential Colpitts VCO architecture should be used in the block diagram shown in Fig. 1, when up and down conversion is needed. In this paper is investigated single-ended Colpitts VCO architecture in order to evaluate the feasibility of this circuit.

In Section II*A* of this paper are presented the single-ended Colpitts VCO core and buffer designed on AMS process. For the purpose of this investigation from SiGe BiCMOS 0.35 µm technology are used MOS transistors, capacitors, varicaps and one of the available integrated inductors. The phase noise and frequency tuning characteristic of the Colpitts VCO are presented in Section II*B*.

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II. INVESTIGATION OF COLPITTS VCO

The block circuit of investigated Colpitts VCO is shown in Fig. 2. It consists of VCO and buffer. The load resistor R_L is equal to 50 Ω, while the supply voltage V_{DD} is 2.5 V.

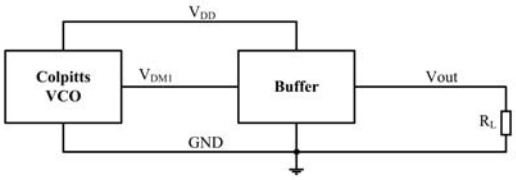

Fig. 2. Block circuit of Colpitts VCO.

A. Colpitts VCO core and buffer

The schematic of the designed Colpitts VCO core is presented in Fig. 3.

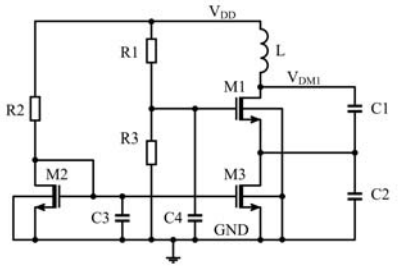

Fig. 3. Schematic of Colpitts VCO.

The frequency of oscillation of the VCO is determined by [6]:

$$f_o = \frac{1}{2\pi\sqrt{L_t C_t}}, \quad (1)$$

where L_t is total tank inductance and C_t is the total tank capacitance. The spiral integrated inductor SP011S200T is chosen for L. Simulated characteristic of inductor's Q-factor as a function of frequency is shown in Fig. 4. The maximum Q-factor obtained at 5.01 GHz is equal to 11.56, while Q-factor at 2.5 GHz is equal to 9.5.

The values of: inductor L; feedback capacitors *C1* and *C2*; the sizes of core transistor *M1* of the Colpitts VCO are given in Table 1. The capacitance of *C1* and *C2* respectively is formed by: 18 and 16 "*cpolyrf*" capacitors with values of 330 fF, which are connected in parallel.

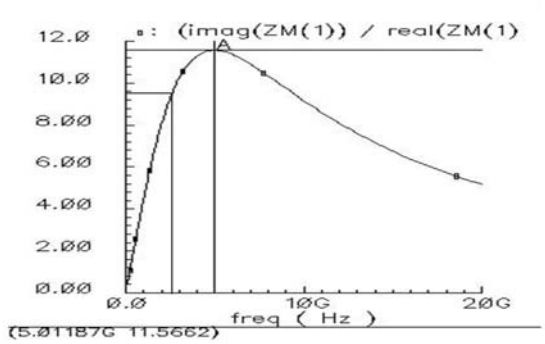

Fig. 4. Q factor as a function of frequency of inductor SP011S200T.

Colpitts VCO's core transistor *M1* is represented by 4 parallel connected "*modnrf*" NMOS transistors. The capacitance of *C3* and *C4* is formed by 16 parallel connected "*cpolyrf*" capacitors with values equal to 1 pF.

TABLE 1. THE VALUES OF INDUCTOR, FEEDBACK CAPACITORS, AND CORE TRANSISTOR SIZE OF COLPITTS VCO CORE

VCO core	L [nH]	C1 [fF]	C2 [fF]	C3=C4 [pF]	M1-W/L [μm]
	1.1	18x330	16x330	16x1	4x(200/0.35)

The schematic of buffer topology is shown in Fig. 5. The output of Colpitts VCO is the drain voltage of transistor *M1* (V_{DM1}), which is connected to input (*Buffer_in*) of the buffer stage. Block circuit of Colpitts VCO and buffer simulated with Cadence is shown in Fig. 6.

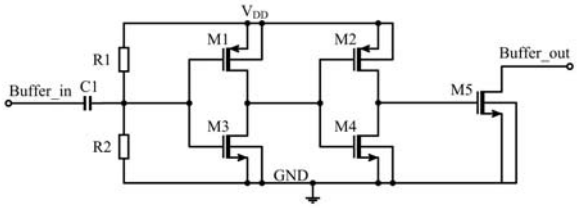

Fig. 5. Schematic of buffer.

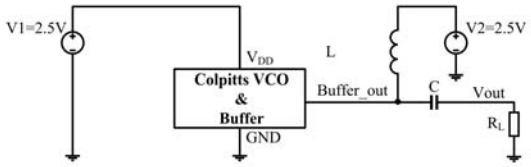

Fig. 6. Simulated Colpitts VCO and buffer block circuit.

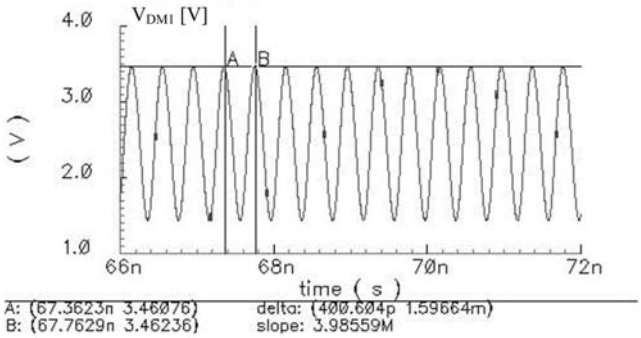

Fig. 7. Drain voltage waveform of transistor M1 V_{DM1}.

The value of load resistor R_L, of the block circuit shown in Fig. 6, is equal to 50 Ω. Simulated waveforms of output voltage of Colpitts VCO (V_{DM1}) are presented in Fig. 7 and Fig. 8.

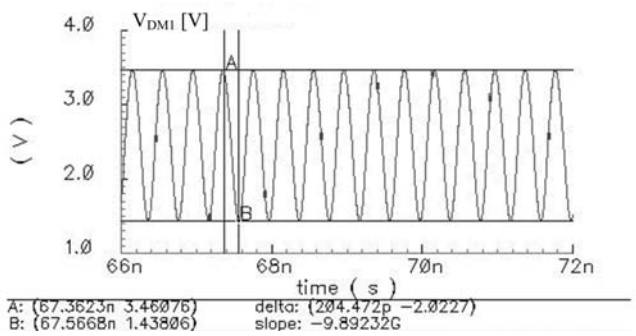

Fig. 8. The peak-to-peak voltage of V_{DM1}.

As can be seen from Fig. 7 the frequency of Colpitts VCO core's output voltage is equal 2.5 GHz. The peak-to-peak voltage of $V_{DM1(p-p)}$ equal to 2.02 V could be seen in Fig. 8. The simulated waveforms of output voltage V_{out} of designed Colpitts VCO and buffer block circuit, shown in Fig. 6, are presented in Fig. 9 and Fig. 10.

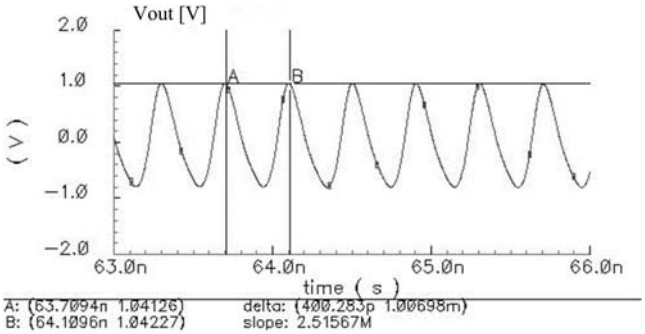

Fig. 9. The simulated waveform of output voltage V_{out}.

As can be seen respectively from Fig. 9 and Fig. 10 frequency of oscillation f_o of Colpitts VCO is equal to 2.5 GHz, while output peak-to-peak voltage $V_{out(p-p)}$ is equal to 1.83 V.

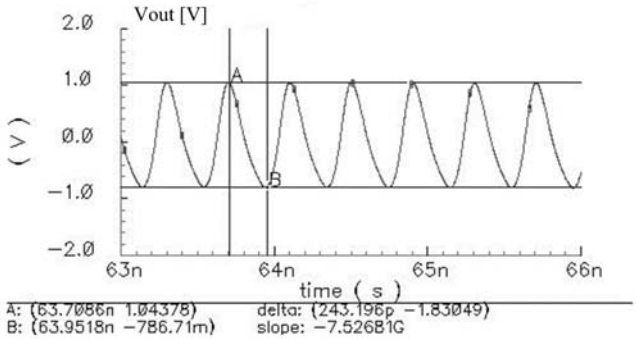

Fig. 10. The peak-to-peak voltage of V_{out}.

The drain current waveform of core transistor *M1* (I_{DM1}) is shown in Fig. 11.

TABLE 2. THE MAIN PARAMETERS OF COLPITTS VCO

Colpitts VCO	f_o [GHz]	$V_{DM1(p-p)}$ [V]	$V_{out(p-p)}$ [V]	$I_{DM1(p-p)}$ [mA]
	2.5	2.02	1.83	45.23

The value of peak-to-peak current $I_{DM1(p-p)}$ is equal to 45.23 mA. The main obtained parameters of the designed Colpitts VCO are summarized in Table. 2.

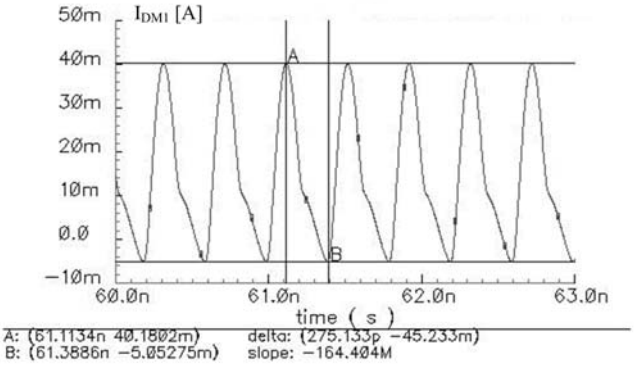

Fig. 11. The waveform of drain current of transistor M1 (I_{DM1}).

B. Phase noise and frequency tuning of designed Colpitts VCO

The phase noise of the oscillators degrades the dynamic range of the receivers [7]. If voltage controlled oscillators have low phase noise, the signal-to-noise ratio of the desired signal can be improved. According to the theory the phase noise can be expressed by [7]:

$$L_{total}\{\Delta\omega\} = 10.\log\left[\frac{P_{sideband}(\omega_0 + \Delta\omega, 1Hz)}{P_{carrier}}\right], \qquad (2)$$

where $P_{sidebanh}$ is the single sideband power at the frequency offset $\Delta\omega$ from the carrier with a measurement bandwidth of 1 Hz. $P_{carrier}$ is the total power under power spectrum. The obtained phase noise characteristic of the Colpitts VCO is shown in Fig. 12.

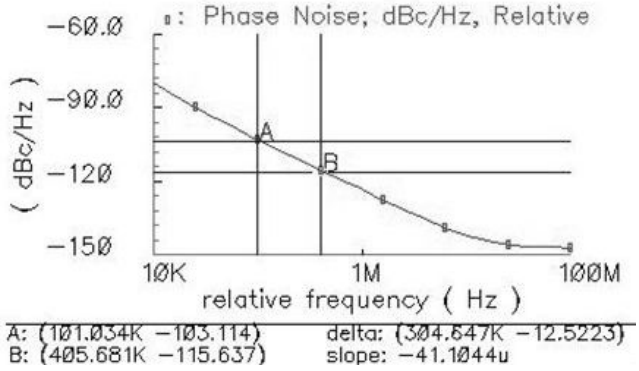

Fig. 12. Phase noise characteristic of designed Colpitts VCO.

The simulated phase noise is equal to -103 dBc/Hz at a 100 kHz offset from 2.5 GHz carrier when Colpitts VCO drawing 20 mA current from a 2.5 V power supply.

TABLE 3. PHASE NOISE OF COLPITTS VCO

Colpitts VCO	Phase Noise @ 100kHz [dBc/Hz]	Phase Noise @ 400kHz [dBc/Hz]
	-103	-115.6

The phase noise at a 400 kHz offset from 2.5 GHz carrier is equal to -115.6 dBc/Hz. The obtained phase noise results of the designed Colpitts VCO are summarized in Table. 3.

The frequency tuning of the investigated Colpitts VCO is performed using MOS varicap "*cvar*", available in the library *PRIMLIB* of the AMS 0.35 µm technology. This voltage controlled capacitance component is connected in parallel with capacitor *C1* of the VCO core shown in Fig. 3. The schematic of Colpitts VCO core with varicap is illustrated in Fig. 13.

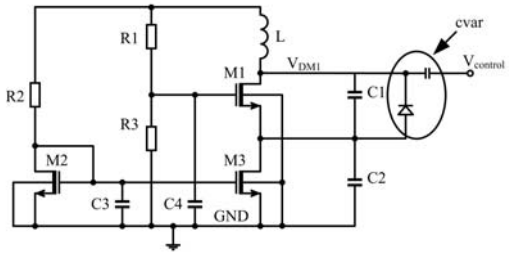

Fig. 13. Schematic of Colpitts VCO core with varicap.

The frequency of oscillation f_o of the investigated Colpitts VCO as function of control voltage $V_{control}$ applied to varicap "cvar" is investigated. The obtained results are presented in Table 4.

TABLE 4. FREQUENCY OF OSCILLATION OF COLPITTS VCO AS FUNCTION VCONTROL

$V_{control}$ [V]	Colpitts VCO f_o [GHz]
0	2.5
0.5	2.4
1	2.35
1.5	2.34
2	2.31
2.5	2.2

The dependence of f_o as function of control voltage $V_{control}$ is graphically presented in Fig. 14.

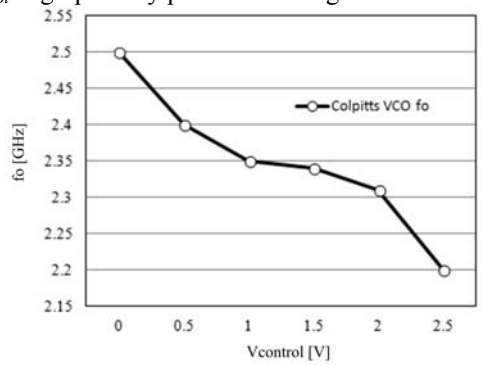

Fig. 14. Frequency of oscillation f_o of Colpitts VCO as function of control voltage $V_{control}$.

The received simulation results show that f_o of Colpitts VCO can be adjusted from 2.5 GHz to 2.2 GHz, when the control voltage $V_{control}$ is changed from 0 V to 2.5 V. The simulated waveform of the voltage V_{DM1}, when $V_{control}$ is equal to 2.5 V, is presented in Fig. 15. In this particular

case frequency of oscillation f_o of Colpitts VCO is equal to 2.2 V.

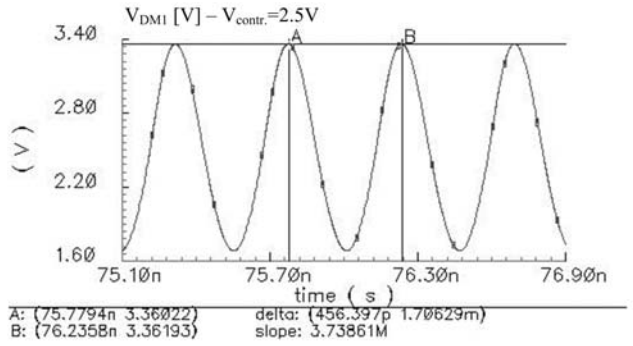

Fig. 15. The waveform of V_{DM1} when $V_{control}$ is equal to 2.5 V.

The layout of Colpitts VCO, designed on AMS SiGe BiCMOS 0.35 µm technology, is presented on Fig. 16.

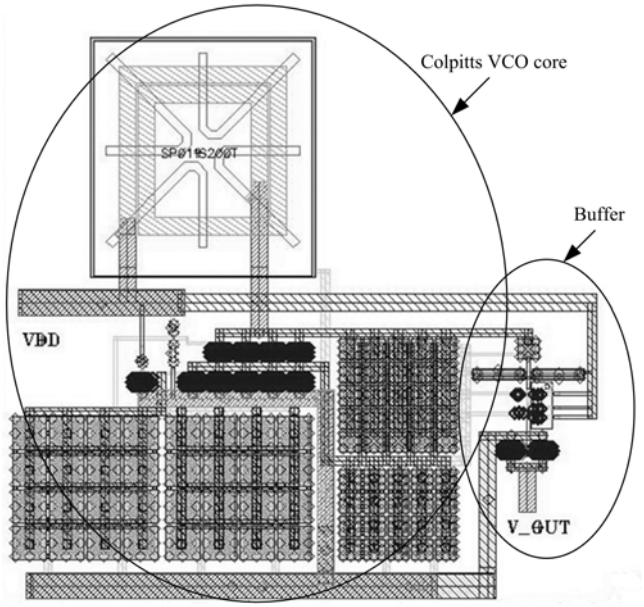

Fig. 16. The layout of Colpitts VCO designed on SiGe BiCMOS 0.35 µm technology.

The occupied silicon area of Colpitts VCO and buffer designed on AMS SiGe BiCMOS 0.35 µm technology is 0.73x0.69 mm^2.

III. CONCLUSION

In this paper is presented Colpiits VCO designed on 0.35 µm technology. The phase noise of the investigated circuit is equal to -103 dBc/Hz at a 100 kHz offset and -115.6 dBc/Hz at a 400 kHz offset from 2.5 GHz carrier frequency. The frequency of oscillation f_o of Colpitts VCO can be adjusted from 2.2 GHz to 2.5 GHz, when the control voltage $V_{control}$ is changed in the range between 2.5 V and 0 V. The obtained results show that Colpitts VCO can be used for wireless communication applications.

ACKNOWLEDGEMENT

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Layout Design of Switching-mode Amplifier for LTE Applications

Tihomir Sashev Brusev and Rossen Ivanov Radonov

Abstract – **The layout design of hysteresis controlled switching-mode amplifier for fourth generation Long-Term Evolution (4G LTE) applications is presented in this paper. Those circuits are used in envelope amplifiers (EAs) architectures, which supply voltage to the transmitter's power amplifier (PA). The proper layout design can help to improve the overall efficiency of EA, because most of the energy delivered to PAs is supplied by a switching-mode amplifier. The design is made with Cadence using AMS CMOS 4-metal 0.35 µm technology. The investigation and comparison between efficiency results from the simulation of schematic and layout with extracted parasitic devices is performed.**

Keywords – **Switching-mode amplifiers, CMOS 0.35 µm 4-metal technology, Layout, Efficiency, Cadence**

I. INTRODUCTION

The new wireless communication standard 4G LTE allows transfer of large date packages in real time. The reason is that in LTE orthogonal frequency division multiplexing (OFDM) modulation is used. Information is transferred by several sub-carrier frequencies, which are summed at the output of the system. As a result the transmitted signal has big variation of the amplitude [1]. Therefore linearity of transmitter's PA is very important characteristic, because it helps to avoid interference with nearby users. The disadvantage of linear PAs is that they indicate low efficiency results. One of the most useful methods for efficiency improving of PA is envelope tracking method [2], [3]. Envelope amplifier in this technique, supply dynamically changeable voltage to drain or collector of PA's RF transistor as a function of envelope signal [4].

Efficiency of envelope tracking power amplifier (ETPA) system, consisted by envelope amplifier and PA, is determined by [2]:

$$\eta_{ET\,PA} = \eta_{EA} . \eta_{PA}, \quad (1)$$

where η_{EA} is the efficiency of the envelope amplifier; η_{PA} is respectively the efficiency of the PA. The formula above shows that efficiency of envelope amplifier is a key for improving $\eta_{EA\,PA}$, taking into account low efficiency of linear power amplifiers. The most popular EA's architectures, presented in the literature, are combination between linear amplifier and switching-mode amplifier [5], [6]. Advantages of fast linear amplifier stage and high efficiency switching-mode stage are used in those hybrid circuits. Transmitter's PA in LTE applications work with high peak to average power ratio (PAPR). In most of the time these circuits have to work in the back-off mode of operation. Switching-mode amplifier in hybrid EA architectures is used to deliver low frequency and dc voltages, while linear amplifier has to supply high frequency voltages to PA. The efficiency of envelope amplifier depends strongly on switching-mode amplifier's efficiency, because this stage delivers about 80% of the total output power to the PA [4].

The signals in LTE standard have bandwidths up to 40 MHz with a trend of further increase. The disadvantage of pulse-width modulation (PWM) controlled switching-mode amplifiers is that they are low bandwidth circuits. Their switching frequency f_s have to be about ten times higher than the bandwidth of the LTE signal, which leads to unacceptable efficiency degradation [7]. On the other hand hysteresis control allows increasing of switching converter's bandwidth up to switching frequency f_s [7]. Therefore this method ensures LTE bandwidths to be covered using lower f_s, increasing efficiency of switching-mode amplifier.

An integrated circuit (IC) layout of hysteresis controlled switching-mode amplifier designed with Cadence is presented in Section II of this paper. The investigation efficiency results from the simulations of schematic and layout with extracted parasitic devices are presented in Section III.

II. LAYOUT DESIGN OF HYSTERESIS CONTROLLED SWITCHING-MODE AMPLIFIER

Hysteresis control allows switching-mode amplifier to operate with lower switching frequency f_s compared to PWM control covering the equal bandwidths of LTE signals. Thus power losses in the building blocks and power transistors are decreasing. In Fig. 1 is shown a block circuit of hysteresis controlled switching-mode amplifier, which is designed using AMS CMOS 0.35 µm process.

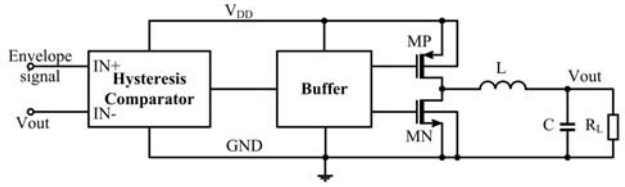

Fig. 1. Block circuit of hysteresis controlled switching-mode amplifier designed CMOS 0.35 µm process.

Wireless portable electronic devices, like mobile phones and tablets, use lithium-ion batteries. For that reason power supply voltage V_{DD} of the designed circuit is chosen to be

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equal to 3.6 V, which is standard output voltage of this type of batteries. The inductance value of filter inductor L is equal to 250 nH, while capacitance of the output filter capacitor C is equal to 5 pF, which is equivalent capacitance value of parallel combination between power transistor of linear amplifier. The resistor's value R_L represents the current load of RF power amplifier. The schematic of comparator with hysteresis is illustrated in Fig. 2. A LTE envelope signal is applied to the input "IN+". A signal sinusoidal waveform with frequency equal to 20 MHz is used as a test signal. This signal doesn't represent the real waveform of LTE signal. Nevertheless using this test fast changing LTE envelope signal could be emulated.

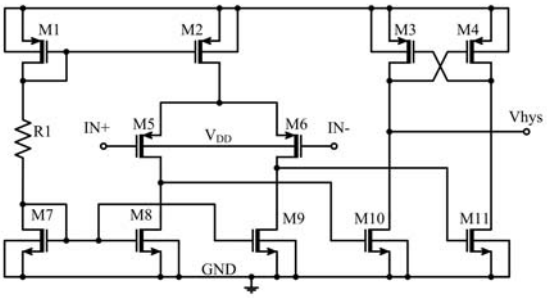

Fig. 2. Schematic of comparator with hysteresis.

The layout of the comparator with hysteresis is designed using Virtuoso layout tool of Cadence IC package and AMS CMOS 0.35 μm 4-metal technology. The layout is shown in Fig. 3.

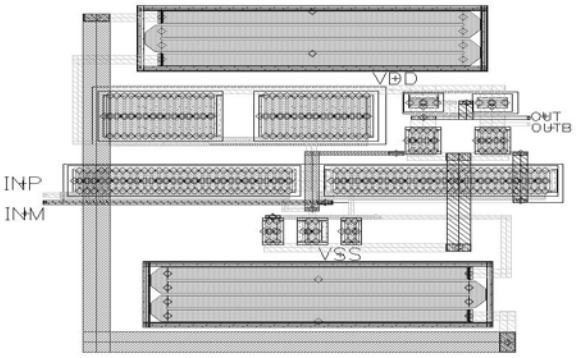

Fig. 3. Layout of comparator with hysteresis.

The circuit's topology of the buffer stage used in the hysteresis controlled switching-mode amplifier is presented in Fig. 4 [8].

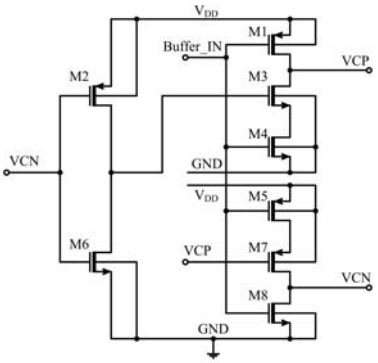

Fig. 4. Buffer circuit's topology.

The buffer's topology ensures short time when NMOS and PMOS transistors in the power stage are both switched-off. Thus power stage is prevented from short-circuit losses when both power MOS transistors are switched-on simultaneously. The layout of buffer stage is presented in Fig. 5.

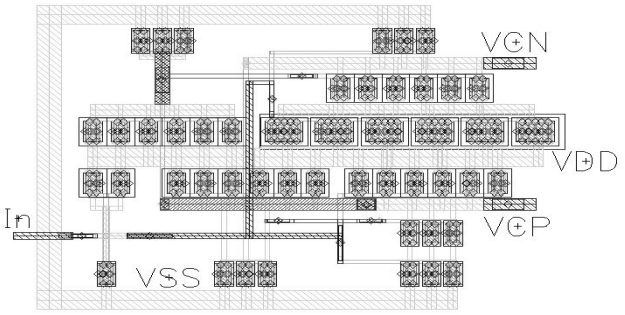

Fig. 5. Layout of Buffer.

The layout of the hysteresis controlled switching-mode amplifier designed on AMS CMOS 0.35 μm 4-metal technology is presented on Fig. 6.

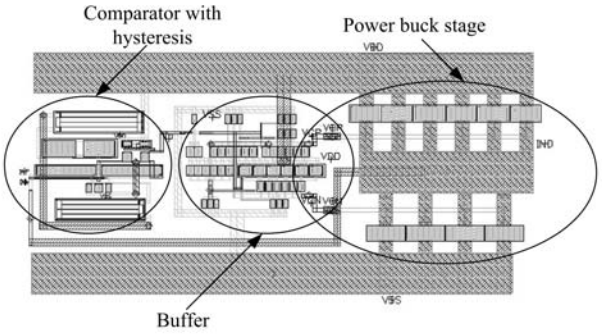

Fig. 6. Layout of hysteresis controlled switching-mode amplifier.

In order to verify the proper work of the designed switching-mode amplifier, a re-simulation of the layout design with extracted parasitic devices is performed. The results are compared with the simulation results of the designed circuit at the schematic level. The verification is made at different dc levels of the sinusoidal envelope signal.

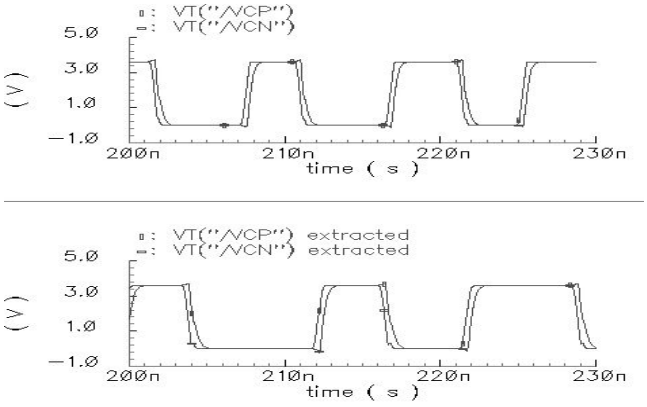

Fig. 7. Buffer's output control signals VCP and VCN of schematic and layout with extracted parasitics, when envelope sinusoidal signal has dc voltage equal to 1.2 V and amplitude equal to 500 mV.

In Fig. 7 are presented buffer's output control signals VCP and VCN, which regulate the state of power MOS

transistor, of schematic and layout with extracted parasitics, when envelope sinusoidal signal has dc voltage equal to 1.2 V and amplitude equal to 500 mV. As can be seen from the picture short gap time is ensured when both NMOS and PMOS output transistors of buck converter are switched-off. Also the control pulses obtained after re-simulation of layout with extracted parasitics are slightly larger and phase shifted compared to those obtained after schematic simulation. This is due to the parasitic capacitors formed by the inevitable overlapping of the metal layers. The same signals at different time range are shown in Fig.8. Larger time range helps to compare VCP and VCN signals at different dc voltage levels of sinusoidal envelope signal. On the other hand at larger time range short gap time cannot be seen when power MOS transistors are both switched-off.

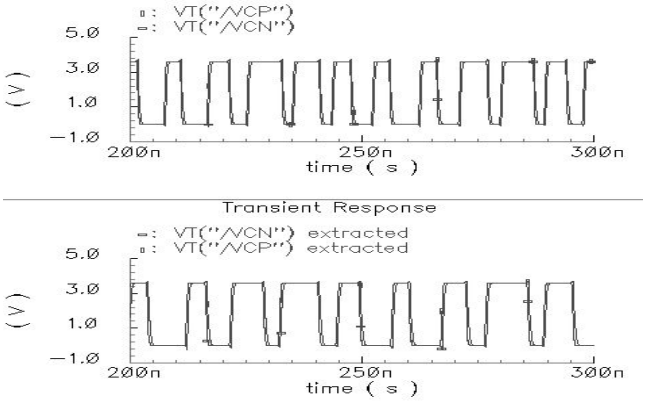

Fig. 8. VCP and VCN when envelope sinusoidal signal has dc voltage equal to 1.2 V and amplitude equal to 500 mV.

The signals VCP and VCN are shown in Fig. 9 when envelope sinusoidal signal has dc voltage equal to 1.8 V and amplitude equal to 500 mV.

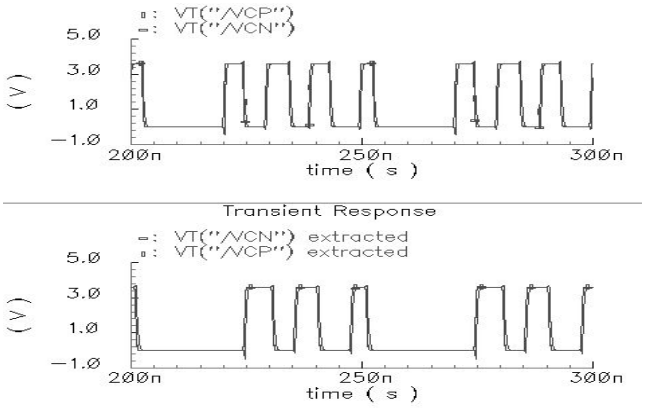

Fig. 9. VCP and VCN when envelope sinusoidal signal has dc voltage equal to 1.8 V and amplitude equal to 500 mV.

The reaction of the system can be seen in Fig. 8 and Fig. 9 when different envelope signals are applied to hysteresis comparator. The small number of pulses generated from the re-simulation of the layout with extracted parasitics, compare to those generated from simulation of the schematic are due to their greater pulse width. This fact proves that after layout design the hysteresis controlled switching-mode amplifier works properly.

III. Efficiency Investigation of the Designed Switching-mode Amplifier

The efficiency of the switching-mode amplifier is calculated by formula:

$$\eta = \frac{P_{out,avg}}{P_{in,avg}}, \tag{2}$$

where $P_{in,avg}$ and $P_{out,avg}$ are the respective average input and output power of the circuit. In the Table 1 are presented the simulation results of the efficiency as a function of R_L, when the average output voltage $V_{out,avg}$ of the switching-mode amplifier is equal to 1.2 V. The values of the R_L are changed between 10 Ω and 30 Ω, because those numbers represent the practical equivalent value of PA used as a load [6].

TABLE 1. EFFICIENCY S A FUNCTION OF RL AT $V_{OUT,AVG}$=1.2 V

	R_L=10 [Ω]	R_L=15 [Ω]	R_L=20 [Ω]	R_L=25 [Ω]	R_L=30 [Ω]
Eff. [%]	47.71	55.45	59.24	61.17	61.54
Eff. [%] - layout	45.34	53.03	57.22	58.98	59.57

In Table 2 the efficiency results are given obtained after simulation respectively of schematic and layout with extracted parasitics as function of R_L, when $V_{out,avg}$=1.5 V.

TABLE 2. EFFICIENCY AS A FUNCTION OF RL AT $V_{OUT,AVG}$=1.5 V

	R_L=10 [Ω]	R_L=15 [Ω]	R_L=20 [Ω]	R_L=25 [Ω]	R_L=30 [Ω]
Eff. [%]	49.15	57.14	61.19	63.86	64.58
Eff. [%] - layout	46.45	54.74	59.81	61.67	63.47

In Table 3 are presented efficiency results as function of R_L, when $V_{out,avg}$=1.8 V.

TABLE 3. EFFICIENCY AS A FUNCTION OF RL AT $V_{OUT,AVG}$=1.8 V

	R_L=10 [Ω]	R_L=15 [Ω]	R_L=20 [Ω]	R_L=25 [Ω]	R_L=30 [Ω]
Eff. [%]	50.15	58.36	63.33	66.28	68.05
Eff. [%] - layout	46.48	56.29	61.23	64.6	66.58

It can be seen from the results presented in Table 1, Table 2 and Table 3, that the efficiency of the switching-mode amplifier obtained after re-simulation of the layout design with extracted parasitic devices is smaller in comparison to the results after simulation of the schematic. This is due to the parasitics formed after layout design of the circuit. They lead to extra power losses, which are not included in efficiency results in schematic simulations. The results given in Table 3 when $V_{out,avg}$=1.8 V, are graphically presented in Fig. 10.

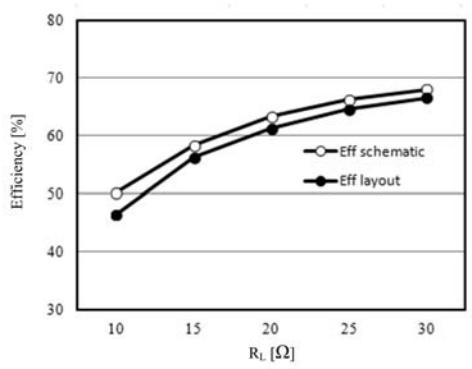

Fig. 10. Efficiency of the switching-mode amplifier as a function of the load R_L, *when* $V_{out,avg}$*=1.8 V.*

The total estimated parasitic capacitance formed by overlapping of the metal layers is equal to 1 pF. The main contributor is power buck stage. In this stage four metal layers in parallel are used in the layout design, to ensure the highest output current of the switching-mode amplifier.

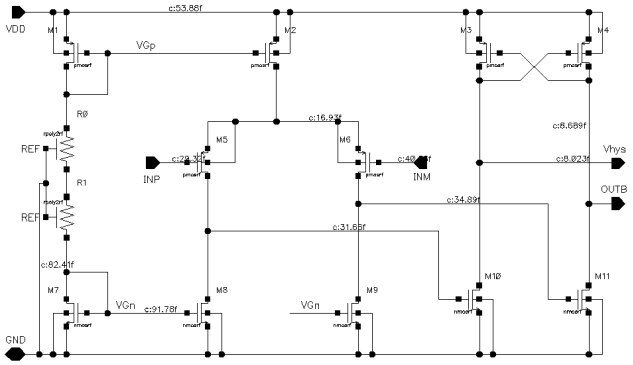

Fig. 11. Schematic of net's capacitive load of comparator with hysteresis.

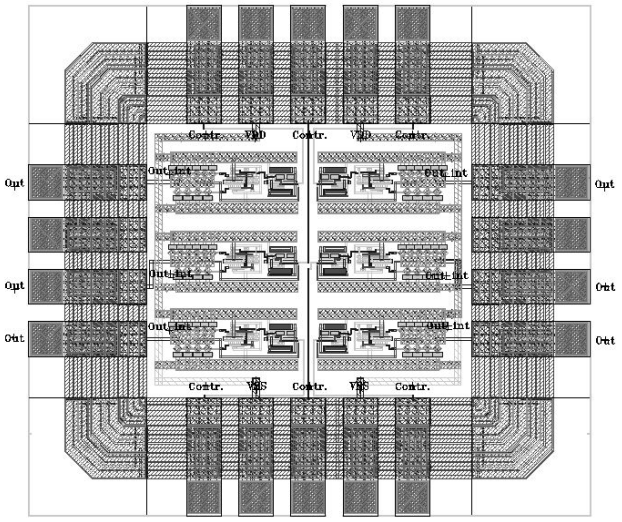

Fig. 12. Layout top view of switching-mode amplifier system.

The parasitic capacitance can be reduced by using fewer metal layers, but then occupied silicon will be larger. The parasitic capacitance formed in the power buck stage is 85% of total parasitic capacitance. Nevertheless, the simulation results show that the designed circuit works properly after layout design. The schematic of net's capacitive load of comparator with hysteresis is shown in Fig. 11. The layout including pad rings of the designed hysteresis controlled switching-mode amplifier is presented in Fig. 12.

IV. CONCLUSION

In this paper the layout design of hysteresis controlled switching-mode amplifier for wireless communication applications is presented, performed with Cadence on AMS CMOS 4-metal 0.35 μm technology. The re-simulation of the layout with extracted parasitics proves the proper work of the circuit. The parasitics decrease the overall efficiency of the system between 1.2 % and 3.5 %.

ACKNOWLEDGEMENT

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Automotive Industry Trends and Effects over Analog Circuit Design

Vesselina Atanasova Barzinska

Abstract – **This paper presents the current tendency in automotive industry, analyses the influence into the Integrated Circuit (IC) design, and proposing project and process transferable solutions for overcoming some of the common problems.**

Keywords – **Automotive, simulation based design, EMC, High Voltage, design procedures**

I. INTRODUCTION

The automotive market with its constant grow is very interesting for IC (Integrated Circuits) components design companies. According the market researches, electrical and electronics parts account for 20% to 25% of the cost of an average vehicle, while in hybrid vehicles those parts account for 50% of the cost [1]. In area with constant and growing competition, new developing markets, companies need to constantly improve their strategy to survive in these hard days. The IC shall be cost effective, while managing with the constantly increasing functionality, power efficiency requirements, temperature range, and the specific for the industry high Electromagnetic Compatibility (EMC), reliability and functional safety requirements [1], [2]. At same time companies are following other trends: customers are giving more value of personalized solutions, connectivity to mobile devices, internet, cars-to-cars and infrastructure.

Even in this changing environment, from the practice it can be seen that no small part of circuits and design problems are repetitive. This could be seen as same small blocks architectures, sizing task, simulation test approach, High Voltage (HV) design, or big IC development tasks related to Functional Safety, EMC and power management, which are usually part of Automotive IC requirements.

Another growing task for decreasing project risk is to perform more and more simulations instead on relying on expensive prototype evaluation, and to decrease risk of design re-spin. As the performed simulations have different targets and simulation environment, the best suitable models are build depending on specific verification targets.

In chapter A. is given example of automated design sizing based on simulations of a very popular current bias source.

Chapter B. discuss tendency in modeling, in respect of development stage of product life.

Chapter C briefly comment Functional Safety.

In chapter D. discuss EMC simulation for IC.

Chapter E. is focused on HV design.

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A. Design reuse by Soft IPs

In electronic design a semiconductor intellectual property core, IP core, or IP block is a reusable unit of logic, cell, or chip layout design that is the intellectual property of one party [9]. The IP are hard core IP, including fixed layout format, and soft core IP which are offered as synthesizable RTL.

The most of analog IP can be categorized in the follow circuit type:

- AFE (Gain amplifiers, active filters, ADC, DAC)
- Timing IP (clock circuits line PLL and DLL)
- PVT monitoring IP (temperature, battery, power, performance sensing)
- Power IP(LDO low-drop out regulators)
- Peripheral/Interface IP
- Memory IPs

There are many pros and cons about the use of analog IPs. Benefits of reusing silicon proven Analog Hard IPs are project risk decrease about:

- Schematic/design development time
- Physical layout representation
- Complete documentation
- Models, supporting verification at different design development step
- Silicon proven electrical parameters, including qualification
- Easy connection to other IPs from same IP provider.

Negative aspects of analog IPs start with ASIC requirements diversity. It can be needed very small circuit adaptation, but will cause changes starting from schematics and going through components of IP package. Another disadvantage is that analog IP is linked to specific FAB technology node and it revision.

Those are the main reason most of the analog IPs to be a complex blocks, like ADCs, PLLs, Interfacing circuits and etc., where risk of design iteration is very high. Although big part of analog blocks designs are custom, consuming significant part of project resources.

Analog design process is far behind Digital design regarding design automation, formal verification, transferability from one technology node to another, and “open design source” for implementing design adaptation. To overcome those negative aspects, can be reused some of design approaches from digital design and expand existing practices like:

- Creation of libraries basic blocks, a technology independent schematics, with some of most popular block architectures;
- Verification IPs: test benches, simulation setups, post-simulation parameters extraction and reporting;

- Tools, linking design to new or existing design sizing and design optimization software products;
- Enhance use of verification tools, using package of checks, based on experience. Some of this tools use netlist, where are recognized specific structures. This provides very fast rules violation check.
- Developed automated design procedures linked to specific structures. The literature provide significant amount of design procedures, which automation will increase significantly the quality of new designs.

The listed above can be part of Analog Soft IP, or synthesizable version of analog circuit, making it manufacture process, size, parameters process independent. All given examples above have the common characteristics that they step on design experience, which can give short development time and predictable final results.

One of the key factors for success of automation design task is proper circuit selection. A current CMOS bias source, working in week inversion for example is a popular architecture, suitable for implementation in Low Voltage (LV), as well possible to extend for High Voltage (HV) CMOS process [3]. The typical characteristics achieved with this architecture are:

- Reference current from few 100 nA to 100uA. The achieved current consumption is in the same range.
- Wide supply voltage operating range: from 2 transistors threshold voltage (Vth) in LV systems and one more Vth for the HV systems, up to maximum supply for the system, which for HV automotive systems can be up to 25V for 12V battery system or even 50V for 42V systems.
- Precision mainly defined by used resistors process variation.
- Linear behavior in wide range, which is good base for applying optimization algorithms for automated design sizing.

B. Modeling during product development

To cover all functional, parametric, EMC, ESD, temperature profiles, quality and safety targets, with every electronic component are performed significant experiments and measurement, sometimes with negative results.

As many of characteristics cannot be evaluated without the components to be integrated in the system, automotive industry invest more and more efforts in SoC modeling. The models vary on abstraction level, simulation environment, the used description language. From practice can be distinguished the follow models categories, with some example from automotive electronic circuit design industry:

- Depending of product or project hierarchy, by used model languages can be grouped to(but not limited to – system (SystemC, SystemVerilog, MATLAB Simulink), Printed Circuit Board (PCB) (IBIS, transmition lines, 3D chip (VerilogAMS), block(Verilog, Spectre)
- Depending project stage could be requirements definition oriented and circuit synthesis (Verilog, VHDL, Simulink), or verification oriented (SystemC, SystemVerilog, VerilogAMS).
- Depending to what precision level the model replicate the electronic circuit they could be include single case mathematical or behavior representation, or they could include process or temperature parameters dependency.

The simulations in microelectronics are extensively used from few decades. The OEMs companies are integrating electronic components from different companies, which are produced at different technologies, developed with different software tools, integrating the same with sensors using physical simulators, and possibility for software development and evaluation ate early stage. The OEM companies respectively demand these models to be provided by electronic components producing companies. Those models have to cover the main function, error conditions detection and/or limitation, process variation etc. By these models are secured not only the actual system performance, but also is provided possibility to be simulated the system in case of change – due to new functionality, environment requirements change, or even in case of changed supplier of electronic components [4].

C. Functional Safety

ISO 26262 is one of most cited standard by automotive company in the last years. Published 2011, it is an adaptation of Functional Safety standard IEC 61508 for electrical and electronic (E/E) systems, adapted for automotive industry. In ISO 26262 the risk of hazardous operational situations is qualitatively assessed and safety measures are defined to avoid or control systematic failures and to detect or control random hardware failures, or mitigate their effects. It covers Quality Management (QM), engineering and testing requirements. It is guideline based on many years' experience of OEMs and ECU suppliers.

From design point of view is important to be understood that meeting all parametric and functional requirements in product specification, to be compliant with EMC standards, does not guarantee product safety, although this are base topics that shall be met. It is also encouraged to be reused existing, proven in practice technical solutions and methods.

D. EMC simulations for IC

Electromagnetic Interference (EMI), Compatibility (EMC) and Environmental Effects (E3) are important considerations in any electronics product development and critical for systems integration. Legally, products must comply with international EMC standards which have been developed to control conducted and radiated emissions from electrical and electronics systems [7], [9]. Early prediction by simulation of the IC EMC problems and same time meeting the all IC requirements presents major challenges to engineers. Not passing the EMC tests with first prototypes have to be solved in new prototype design iteration or adding filtering components.

Compared to embedded system domain, tools for EMC simulations in IC are very few. The IC-EMC software [8] is one, where is a demonstrated handling the modeling, simulations and comparison with real measurement data of emission of integrated circuits.

Modeling of complex circuit is non-trivial task regarding finding the minimum needed precision of the model for the simulation. Another aspect is non-linear effects of active components as diodes and transistors. Based on that use of simplified schematic or block extract of main influencing/influenced components verified with known, existing design methods and tools from the embedded system domain could give the needed tradeoff of precision and design efforts [6].

E. HV design

HV design is part of almost all automotive IC. This is due to the battery supply range, automotive communication interfaces, specific sensors operating range or EMC requirements. The international and government regulations for decreasing CO2 emissions busted the development of 24V and 48V automotive systems, high efficient DC converters, LED drivers.

In the 24V and 48V systems, big part of new designs can step and reuse significant part of existing 12V systems schematics, mainly by replacing the HV devices. HV transistors have usually worst dynamic characteristics, higher threshold voltage and low area density, compared to basic process LV transistors. Due to that the typical uses of HV transistors in analog circuits are:

- HV switch, used in switching application.
- Cascoding switch, protecting the LV transistors from Drain-Source and Drain-Bulk brake-down. This cascoding is used in current source, active loads in amplifier, levelshifters, and serial switch.
- Voltage reference: the threshold voltage of HV transistors is usually higher than the same of the LV transistors from same process option. The transistor is used in diode connection.
- Reverse voltage protection: HV switch can be used as serial reverse voltage protection diode, where the used process is not offering HV diode or HV schottky diode with the required characteristic. The HV transistor drain and source position is swapped. When transistor is off, it acts as serial forward connected diode. When transistor is turned on, it is as switch, with much lower voltage drop than usual HV diode can have.
- Active voltage clamp (zenner): in that transistor application the gate of HV transistor is connected to static reference level, the source is connected to the net that voltage level has to be limited. When the voltage on the source change that HV transistor gate-source voltage is higher than HV transistor Vth, transistor is turned on and pass through it the unwonted current.

The first two listed use of HV devices cover about 90% of HV transistors application in HV circuits, which is providing good reference for new ASICs design partial reuse. Next listed examples are more process specific dependent, but can provide recognizable advantage for the circuit.

Looking on high efficiency on DC convertors, developed for LED drivers, it shouldn't be underestimated the cost of required external components, also electromagnetic missions due to switching. Depending on specific circuit application and requirements, it could be found power, cost and EMC compatible HV solution, which to use continuous biasing and driving, using floating HV-switches, sill having an efficient solution [5].

HV design is often suffering from incorrect or missing gate-source and/or drain source protection. Simulation of Safe Operating Area cases with transient simulations is one of most popular approach for identifying that something is unprotected or in risk but is highly dependent from skills of designers. To decrease risk of failure in new silicones, ASIC companies still relay on internal or external experts, to provide best practice recommendations and to review design regarding mistakes. To cover this verification challenge, companies attempt to develop tools, verifying analog circuit design based on experience and best practices.

II. CONCLUSION

Automotive Industry is requesting from microelectronic manufactures safer, energy efficient, and environment robust design. Together with cost pressure, high dependent of first time right design, analog microelectronic design need to change it design methodologies. Key success factors are selection and reuse of stable solutions, which are easy applicable in many of the projects, technologies, reuse design methodologies and practices from OEMs, invest on development of analog Soft-IPs and design best-practice verification tools.

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Implementation of DOE in the Heat Sink Design for LED Application

Nikolay Vakrilov Vakrilov and Anna Vladova Stoynova

Abstract – **In this article there is analyzed the influence of various design parameters of the heat sink and their influence on the junction temperature of the LED system. Tests are performed by thermal simulations and by the use of technology for design of experiments (DOE) to find the optimal design of the heat sink. The results from the thermal modeling and simulations have been validated experimentally and they show good matching results.**

Keywords – **Heat sink Design, Heat Transfer, Design of Experiment**

I. INTRODUCTION

The development of LED technology has led to the emergence of more compact and more powerful LED devices, which, despite their higher efficiency dissipate a lot of heat. Heat negatively affects the performance of LED devices and must be dissipated effectively because it can cause damage and reduce reliability. Therefore, proper thermal management is essential for the good design of each LED device or system [1], [2].

Management problems in heat exchange of LED systems are analyzed and studied by many scientists. A number of studies focus on improving the heat transfer through MCPCB (Metal Core Printed Circuit Board), IMS (Insulated Metal Substrate) and various ceramic materials where powerful LEDs are usually mounted on [2], [3], [4].

Regardless of the type of the circuit board to dissipate heat from the more powerful LED modules heat sinks of different materials and in different sizes are typically used. The effectiveness of the heat sink does not depend only on the size and the material from which it is made, and is determined by its structure. Different design requirements are put at various LED applications according to the working conditions and installation, which require the development of customized solutions for cooling design of the final product.

The problems associated with the design of heat sinks are discussed by many researchers. H. Fengze and Y. Daoguo and others in [5] studied the thermal behavior of designed by them LED array and a heat sink with flat fins and fins pin type. Using a 3D model created in ANSYS and simulations there are investigated temperature distribution of a LED system taking into account the impact of the construction of the heat sink. Analyses show that the transition temperature of LEDs in the array is the lowest when the structure of the heat sink has fins pin type and are arranged so that the fins alternate every other fin. P. Huang, Kailin Pan and others in [6] apply thermal modeling and simulations to optimize the entire design of multi-chip LED lighting module. To optimize the LED structure there are used statistical analysis and thermal simulations by ANSYS software to evaluate the factors influencing productivity as - output of chips, layout of chips, the size of MCPCB and heat sink.

T. Kobayashi, S. Ishikawa, R. Hashimoto and others in [7] study the thermal effects of a heat sink with a round base and flat fins designed for LED bulb. In the analysis of heat transfer they use FEM (Finite Element Method) and are in the model report thermal convection and radiation. By applying the design of experiments (DOE) there are set out the parameters of the heat sink affecting the temperature of the heat sink and is evaluated the best and worst construction. Results from the simulation model of the heat sink are validated by measurements with thermocouples and thermal camera.

A. Mahalle and M. Shende in [8] numerically analyze the heat flow of a star heat sink with a round base and flat fins in natural convection. Research is done in three geometric parameters of the heat sink for finding the optimal structure. The effects of changing the geometric dimensions and the effects of heat flow on the heat resistance and the coefficient of heat exchange are analyzed. The results show that with an increase in the geometric dimensions of the heat sink, the heat resistance and the coefficient of heat transfer are usually reduced.

Although there are studies that examine different structures of the heat sinks, there are still enough challenges in their design. A good heat sink must maintain low transition temperature of the LED devices at different operating conditions; it must be compact and with an easy installation.

This article presents a study of a passive heat sink for a powerful LED module. For optimization of the geometric dimensions of the heat sink, a design of experiments is used. To assess the thermal efficiency of the optimized structure the temperature of junction of the LED source is monitorred.

II. HEAT SINK DESIGN METHODOLOGY

A. Choice of structure

The basic structure of the heat sink has a square horizontal base and circular fins pin type arranged in line. This type of construction allows different orientation of the heat sink and allows more flexible installation and use. As

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a heat sink material aluminum alloy is used, because of its low price, good thermal conductivity and a heat sink with enough complex geometric shape can be easily molded. The structure of the heat sink and the geometry of the fins are shown in Fig. 1.

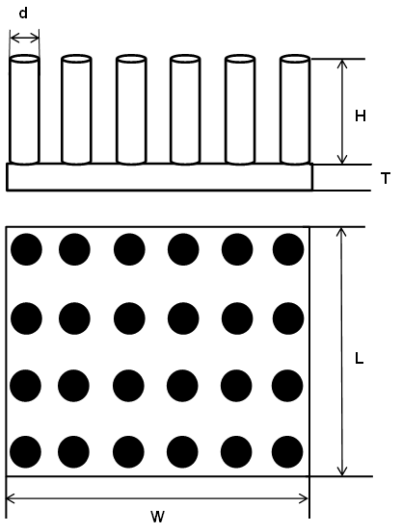

Fig. 1. Heat sink construction

B. Thermal modeling

For the design and testing of the thermal behavior of the heat sink structure CFD software Flotherm is used. Fig. 2 shows the heat-modeled structure of the heat sink fitted with LED module, situated in the center, which thermal power to be dissipated.

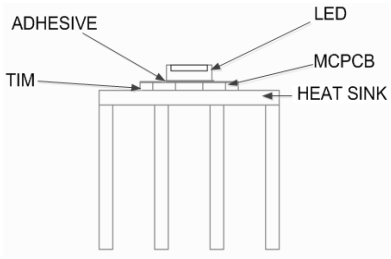

Fig. 2. LED system - made up of LED, MCPCB and a heat sink

The maximum heat power set to the thermal modeling of 3W LED (at maximum operating voltage U_f = 4.1V, maximum current I_f = 700mA and a coefficient of conversion of electrical energy into heat H = 75%) is calculated as follows [8]:

$$P_{th} = U_f I_f H = 4{,}1V \cdot 0{,}7A \cdot 0{,}75 \approx 2{,}15W \qquad (1)$$

Table 1 shows the physical characteristics of the materials constituting the LED system.

TABLE 1. PHYSICAL CHARACTERISTICS OF THE MATERIALS

Material	Conductivity [W/m·K]
Heat Sink – Aluminum 6061	180
GaN Chip	130
SnAgCu Solder	58
FR4 – Dielectric Layer	0.2
Top Layer Copper	385
MCPCB – Aluminum Plate	150
TIM – Silver grease	3

When creating a geometric model of the different variants of heat sinks, the length L, width W and the thickness of the base of the heat sink T do not change with thermal modeling and simulations, because of the specific requirements of LED application.

The heat sink is modeled with a length L = 40mm, width W = 40mm and thickness of the base T = 3 mm.

In order to optimize the parameters of the fin - the height of the fin, the fin diameter and the number of fins in the design of the heat sink, a design of experiments (DOE) is used.

C. Use of DOE in the heat sink design

To obtain optimum thermal characteristics in the design of the heat sink there must be identified the factors having the greatest impact on improving the capacity for heat dissipation.

The geometrical factors of the structure of the heat sink, which are selected as design parameters, are the height of the fins (A), the fin diameter (B) and the number of fins (C) of the heat sink.

Full Factorial Experiment for three factors for each one on two levels is used as a tool for the realization of DOE. Table 2 shows the three design parameters, whose influence is analyzed.

TABLE 2. PARAMETERS AND LEVELS OF EXPERIMENT

Factor	Factor Latter	Level	
		Low	High
Height of Fins, [mm]	A	15	30
Diameter of the Fin, [mm]	B	3	4
Number of Fins, [mm]	C	24	42

In Table 3 there are shown the eight possible experiments and the different configurations of the design parameters.

TABLE 3. COMBINATION OF DESIGN PARAMETERS

Experi-ment №	Height of Fins [mm]	Diameter of the Fin [mm]	Number of Fins
1	15	3	24
2	15	3	42
3	15	4	24
4	15	4	42
5	30	3	24
6	30	3	42
7	30	4	24
8	30	4	42

In Full Factorial Experiment there can be estimated all main effects and interactions, since the method has full resolution.

III. ANALYSIS AND DISCUSSION OF RESULTS

All thermal simulations are conducted at specified ambient temperature of 25^0C.

Fig. 3 shows the distribution of heat and the maximum temperature of the LED system at the first design configuration (with a height of the fins 15mm, diameter of the fin 3mm and 24 fins), and the Fig. 4 of the latter

configuration (with a height of the fin 30 mm, a diameter 4 mm, and the number of the fins - 42) of Table 3.

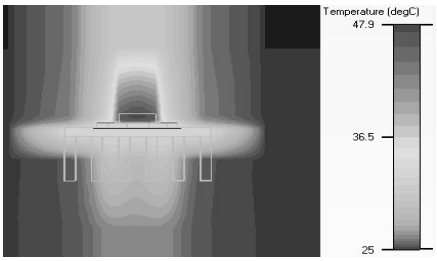

Fig. 3. Temperature distribution in the design configuration of the fins with a height of 15mm, a diameter of 3mm and 24 fins

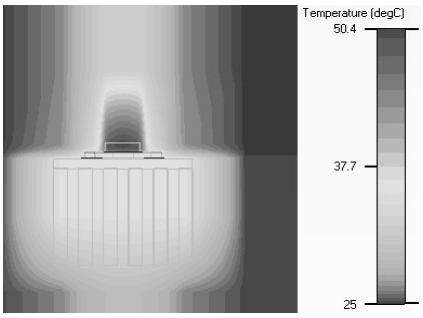

Fig. 4. Temperature distribution in the design configuration of the fins with a height of 30mm, a diameter of 4mm and 42 fins

The effects of various configurations of heat sink design parameters on the maximum temperature of the LED system simulations are shown in Table 4.

TABLE 4. THERMAL SIMULATIONS RESULTS

№	Height of Fins	Diameter of the Fin	Number of Fins	Max. Temp. [^{0}C]
1	15	3	24	47,9
2	15	3	42	47,1
3	15	4	24	49
4	15	4	42	51,9
5	30	3	24	45,4
6	30	3	42	45,7
7	30	4	24	46,1
8	30	4	42	50,4

After analyzing the results of the simulations the factor of influence of each parameter of the heat sink on the maximum temperature of the LED system is represented graphicall in Fig. 5.

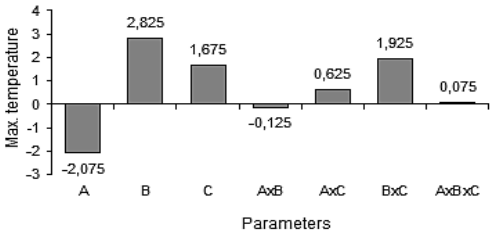

Fig. 5. Factor of influence of each parameter on the maximum temperature

From the graph above it is clear that the effects of A (the height of the fins) and AxB (the interaction between the height of the fins and the diameter of the fins) are the most important parameters of the heat sink to lower the temperature.

On Fig. 6a, b and c there are presented plots of the interaction between each of the parameters on the basis of the processed data from the simulations.

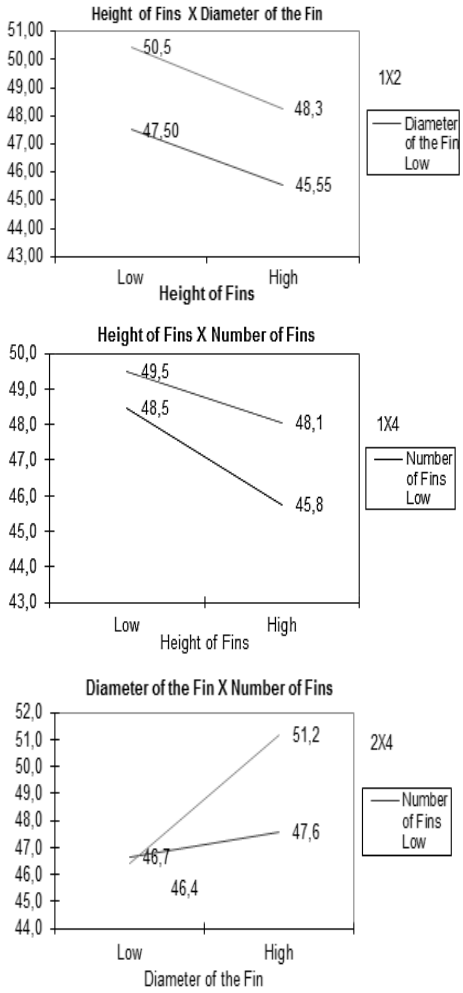

Fig. 6. Graph of interaction between: a) the height of the fins X the diameter of the fins; b) the height of the fins X the number of fins; c) the diameter of the fins X number of fins

It can be seen that the greatest interaction between the parameters is observed in Fig. 6c, where the two lines intersect. From there we can determine that the small value of the diameter (3mm) and the small number of fins (24 fins) provide optimal project results and lead to lowering the temperature of the LED system.

The studies carried out show that the optimal design parameters of the heat sink are - height of the heat sink 30mm, diameter of the fin 3mm and 24 fins. At these values of design parameters the temperature of the LED system is the lowest - 45,4^{0}C. Very low temperature 45,7^{0}C has the heat sink with a fin height of 30mm, fin diameter of 3mm and 42 fins, but it is more expensive to be made. Worst heat sink design parameters are - height of the fin 15mm, diameter of the fin 4mm and 42 fins, then the temperature of the LED system is the highest - 51,9^{0}C.

IV. VALIDATING OF RESULTS

To validate the results of thermal simulations there is used a prototype of the heat sink, which is made with the optimal parameters and has a mounted a LED module on it

supplied by 3,6V DC voltage. Temperature measurement using K-type thermocouple, which is connected to the data acquisition system (UNI-T UT804) and fully dedicated computer with software for data processing are performed. Fig. 7 shows the place of the thermocouple on the LED structure during the measurements.

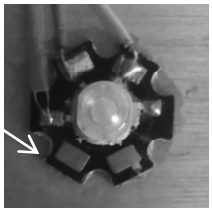

Fig. 7. The place of the thermocouple for measuring the temperature of the module

During the measurements, the ambient temperature is 24^0C and the LED works without interruption for 30min. By substituting the measured temperature at the solder T_S and other thermal parameters of the LED package, for the transition temperature Tj we get:

$$T_j = T_s + \left(R_{j-s}\right)P_d = 33^0C + \left(8^0C/W \cdot 1{,}89W\right) = 48{,}12^0C \quad (2)$$

The resulting temperature of the LED junction of $48{,}12^0$C is very similar to that obtained by the thermal simulations - $45{,}4^0$C. The relative error between the simulated and measured temperature is about 5.6%, which demonstrates accordance of the results.

V. CONCLUSION

Analyses show that the heat sink design with circular fins pin type the larger number of fins is not a factor of influence to increase the cooling capacity.

To increase the heat exchange capacity of the heat sink a major role plays the height of the fin and the interaction between the fin height and diameter of the fin.

For obtaining a better evacuation of heat flow from the heat sink structure the diameter of the fins must not be large, but the number of fins must be carefully selected so as not to hinder the movement of the hot air to the environment.

ACKNOWLEDGEMENT

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Coincidence of the Electron and Ion Beams at Auger Profiling in Microelectronics

Georgi Spasov Spasov

Abstract – **The article presents and discusses the methods for coincidence of the spots of electron and ion guns. The problem has great practical value for precise depth profiling. The Auger profiling gives information for the vertical die architecture and for the layers in the researched technological experiment. This is the main AES preference and a cause for its widespread use in microelectronics. The applicability and performance of the methods are discussed.**

Keywords – **Auger electron spectroscopy, microelectronics, ion beam, electron beam, profiling**

I. INTRODUCTION

Auger electron spectroscopy (AES) is the first method for surface analysis, used in microelectronics (ME). The literature sources point out hundreds applications. This is the case, because its analytical capabilities combine element analysis (for almost the whole periodic table) with informational depth only several atomic layers. At utmost importance especially for ME are the additional possibilities for easy quantification and depth profiling. The last gives information for the vertical die architecture and for the layers in the technological development experiment. Profiling was used: I. For process characterization [1, 2] (passivation, photolithography, chemical and plasma etching, metallization, layers' deposition, oxidation – as technological process or harmful phenomenon, diffusion and ion implantation, and packaging); II. For quality control and as a failure analysis tool [3]. The profiling importance increases persistently [4], because ME requires at present the exactitude of the element composition to be combined with depth separation at atomic order.

As in other analytical methods, the standard profiling in AES combines Auger spectral analyses with ion sputtering. The spectrum gives information for the element composition in the analyzed spot from the surface. The in depth composition of the specimen is traced by alternating consecutively analytical and etching steps (or performing analytical steps during the continuous sputtering). On the other hand, the precise depth profiling (without decreasing of depth resolution) requires exact matching of the analyzed and the sputter areas (a problem alias in the literature "coincidence of the electron and ion guns" and "overlapping of the electron and ion spots").

The purpose of the current work is to present and discuss methods for this coincidence. Despite its upmost importance for the practice, the literature data for the topic is scarce, because it seems this is regarded as a daily round question that has acceptable solution for each laboratory. Most of the presented data below is obtained during conversation with colleagues-analysts. But the work is not only addressed to the Auger analysts, but mainly for the engineer-developers of devices and technologies as the clients, participating in the die development.

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II. EXPERIMENTAL

The experimental setting comprises of an electron gun, an electron spectrometer, an ion gun and a sample stage, Figure 1, as everything is well known and standardized [5, 6].

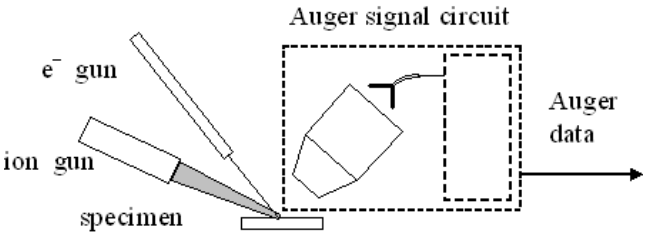

Fig. 1. Block circuit of a classical Auger experiment

Considering the discussed topic we can separate the ion guns used for Auger profiling into 3 groups:

A. Simple ion guns using static beam;

B. Ion guns with x-y beam deflection;

C. Ion guns focusing spot with dimensions a few μm.

The group A guns are rarely used nowadays and are not a subject of our discussion (they require an initial mechanical tuning of the middle of the etching spot in the analyzed spot from the sample). The group B guns are simple electrostatic devices. Their widespread application is due to their low cost and possibility to be added to already existing apparatus. Their ion beam can be focused and shifted (generally – and scanned) on the surface (the sample). Without focusing the ion current density distribution is a Gaussian (Figures 2 and 3 are for a mono-focus ion gun). The focusing forms distribution with greater centralized "homogenized" areas. We will note that with type B guns, a scan with size of the order of the intense central area can be performed, which provides an area with a significant homogeneous current without significantly decreasing the sputtering rate. The group C guns are usually more complex devices. They work in scanning mode, ensuring homogeneous density of the current in the scan area. The larger scan slows down the sputtering rate (in inverse proportion to the square of the characteristic size of the scanned area).

III. RESULTS AND COMMENTS

A. Specifying the details for the presented problem

We assume that the **e-G**un focus is brought in coincidence with the electron **A**nalyzer **F**ocus on the

desired analyzed surface (EGAF point). Also the middle of the focused ion spot has to be put in the EGAF-point. The methods for coincidence the etching and analyzed spot will be covered in subsection *B.*

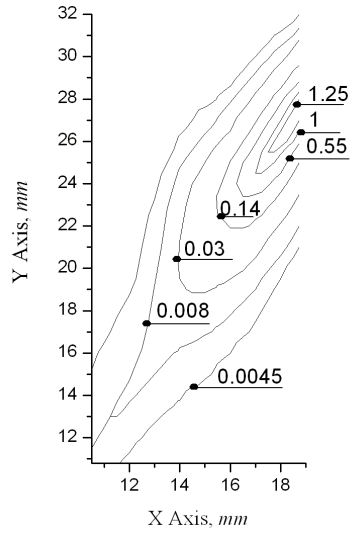

Fig. 2. The ion current density distribution (for ion gun mod. CI-40 /Riber/) is taken in the sample' plane with Faraday cup with an aperture diameter 25 μm. Gaussian' axis represent the spatial position of the ensemble "guns-spectrometer-sample". (Due to the symmetry only half spot is presented.)

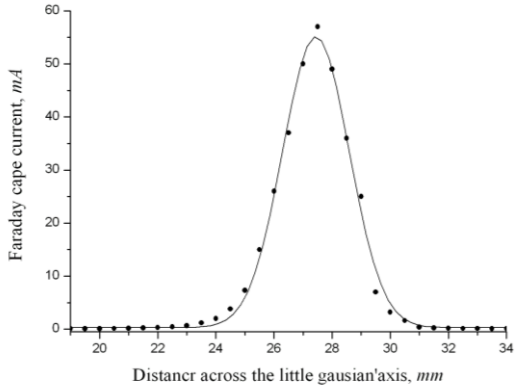

Fig. 3. The ion current density distribution (from Fig. 2) across the little Gaussian' axis.

B. Methods for coincidence the etching and the analyzed spot

a) By etching of thin insulator layer. The ion sputtering of the insulator' layer (e.g. 30-50nm SiO_2/Si) is performed until the etched spot appeared on the surface' layer. The etched spot (result of the local removal of SiO_2 by the ion sputtering) appears where the ion current density is highest (the medium of the ion beam, the Gaussian' center). The etched spot is observed by its different contrast in the electron induced current (EBIC) image. EBIC is the current flowing to ground due to the fall of the beam on the sample. It is dominated by the local conductivity of the layer (of the local volume under the electron beam) – so the absence of a dielectric layer (eliminated by etching) is clearly visible. EBIC-image is electron microscopy mode, wherein the image brightness is modulated by the current (rather than the secondary electrons). The sample is previously put in the EGAF-point, which is therefore the center of the EBIC image. The displacement of the etching spot of this center gives the un-coincidence of electron and ion beam. The coincidence requires several steps, at each of which is etched a new sample to bottom. At each step the ion gun' deviation plates voltage is changed while the spot came in the center of the screen. Therefore this method is one of the slowest and most labour-consuming. We should also add to its shortcomings the lack of direct indication for the focusing of the ion beam (for the focusing could be concluded by the sputtering time of the layer at each step). However we will note that this is the only method giving the sputtering rate.

b) By the trace from the beam in the EBIC image from thin insulator layer (put in the EGAF-point). As initial setup this method doesn't differ from the previous one. On the other hand here the result from the etching is not waited for, but the ion spot indication (its image – obtained by the EBIC contrast) is used directly. Since the obtained image reflects the ion current density distribution, this method allows a focusing of the ion beam. The coincidence is done again by changing the voltage on the ion gun' deviation plates. Coordination between the thickness and the conductivity of the insulator layer might be necessary for the specimen.

c) By Faraday' cup, [7]. The method consists of optimization of the ion current, registered by the cup, Figure 4. The center of the cup hole is fit in the EGAF-point; the ion gun' axis should be normal towards the aperture plain). The controlling gun voltages change. The aperture diameter should be a few times (and even better an order) smaller than the characteristic size of the ion spot. A few quick current checks at positions close to the center position can provide additional information for the ion beam focusing.

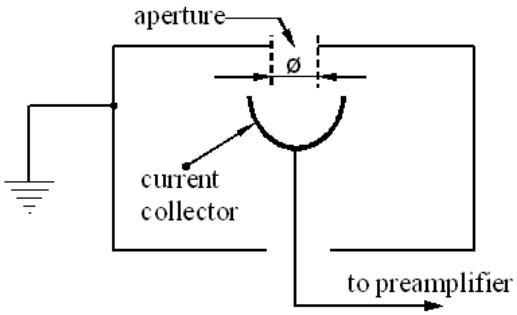

Fig. 4. Faraday' cup principle wiring diagram

d) By the electrons, induced by the ion gun. The ion beam produces electron emission. The peak of the induced by the ion bombardment "elastic" electrons in the spectrum is monitored (we should remind that the analyzer is focused on the analyzed surface). The peak is most intense, symmetrical and narrow if the ion beam is focused precisely and its focus is on the EGAF-point. It is most convenient the peak to be in differential mode while being observed in fast mode through oscilloscope (such practice is a daily routine for the Auger analysis when one brings the electron gun focus in coincidence with that of the analyzer). Additionally, at precise tuning, the energy position of this peak in the spectrum (at an average of the

position of the positive and the negative wing in the differential spectrum) should be at the ion gun energy. This setting should be done on a surface made by material with high ion-electron emission.

e) By the ion-induced Auger peak of the aluminum from the Al probe. This method uses the high ion-induced Auger electron emission of the aluminum. The probe is an Al disk with diameter around 1 mm, prepared on the surface (or also in depth) of the specimen, Figure 5. The tuning is achieved, by maximizing the intensity of the low-energy Al Auger peak. It is convenient to fix the energy of the analyzer at the minimum of the differential LVV peak, which is around 52 eV for ion-electron emission. This method can prove to be perfect and most universal. Therefore some companies producing surface analytic apparatus add a build-in Al probe in their highly specialized sample' manipulators. This is justified since the probe can be used several thousand times.

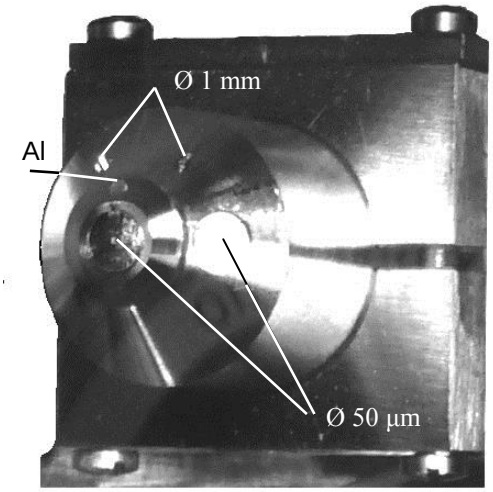

Fig. 5. Commercial coincidence tool (aluminum probe and Faraday cup with 4 different space-oriented diaphragms

f) By combining the ion and the electron image. This method is only applicable for guns with narrow enough beam, allowing the obtaining of the scanning image by ion beam induced electron. The focusing for such beam on the analyzed surface is not a problem (it is performed as in SEM but in fact isn't critical for the profiling, which in this case is done by a scanning of the ion beam). The coincidence of the ion image with the classical SEM image (obtained by the e-gun) is done by the ion gun's deviation plates. We should note that for sharp-focusing ion guns (with a spot' dimension less than 10 μm), this method appears to be the only applicable.

g) By scanning of the ion beam. Introducing this item is somewhat conditional and it is rather presented to underline that the necessity of coincidence (of the electron and the ion beams in Auger profiling) depends on the assigned analytical task. The optimally focused ion beam leads to the maximum gun's sputtering rate. If the last is required for the particular analysis, the focusing is absolutely necessary. However if the analysis requires profiling at speed a few times or even one-two orders lower, the focusing requirements decrease. The simplest way to achieve this decrease is by scanning of the ion beam. The received "blur" of the ion spot equalizes the ion current density distribution. At large enough scanning it might turn out that there is no need to center the ion spot. It is enough to increase the scanning until reaching the necessary (for the analysis) ion current density, measured by the Faraday' cup put at the sample's place.

For better clarity and easier comparison we introduce all of the described methods in TABLE 1.

C. Comments for the application of the methods for the coincidence and the profiling in the analytical practice

Dominant for the setup is the analytical task being solved, which determines the profiling. For example, precise sputtering with speed close to the nominal for the used gun (thick layers) requires careful tuning (mandatory including a focusing). On the contrary, at slow sputtering speed towards the nominal, the precise sputtering can be achieved with appropriate scanning (The ion milling used at some spectral AES analyses should also add here.). Therefore, which coincidence method will be used, the most important is the apparatus base, particularly the type of the ion gun and the availability of tuning options (or the possibility such ones to be additionally upgraded).

Important factor for the discussed tuning is the apparatus mistuning. Where the last is not essential a single precise tuning over long period of time is performed. During this period only tuning tests are made or partial sub-tunings.

TABLE 1. MAIN CHARACTERISTICS OF THE DISCUSSED IN THE ARTICLE METHODS FOR COINCIDENCE THE ELECTRON AND THE ION BEAMS. LEGEND: **A –** BY ETCHING OF THIN INSULATOR LAYER; **B –** BY THE TRACE OF THE BEAM IN THE EBIC IMAGE ON THIN INSULATOR LAYER; **C –** BY FARADAY' CUP; **D –** BY THE ELECTRONS, INDUCED BY THE ION GUN; **E –** BY THE ION-INDUCED AUGER PEAK OF THE AL PROBE; **F –** BY COINCIDENCE THE ION AND THE ELECTRON IMAGE; **G –** BY SCANNING OF THE ION BEAM.

2

Method	Precision	Speed	Focussing	Samples	Notice
A	Very well	slow	yes	yes	It's the only one useful for ion guns using static beam. Additionally it provides sputtering speed.
B	Well	fast	Not very well	yes	The image doesn't correspond linear to the ion current density.
C	Very well	fast	yes	-	FC is required.
D	Very well	fast	yes	-	
E	Very well	fast	yes	*	Al-probe is required (sample or option).
F	Very well	fast	yes	-	
G	Well	fast	no	-	In order to decrease the ion current density. Significant area can be covered.

The situation is significantly different for apparatus, where daily optimization of the analytical electron gun's parameters is made. It is obvious that this disrupts – at least partially – the previously made setup of the whole group/ensemble. Before starting the coincidence of the ion gun towards the new position, it is good the check the lateral displacement of both spots towards the new situation. If it is of no significant, it can be compensated by additional weak scan of the ion beam (without significantly lowering the sputtering rate). In general such scan (with amplitude 20-30% from the size of the central intense area from the ion spot) is useful approach during profiling.

IV. CONCLUSION

Auger spectroscopic profiling gives information for the vertical die architecture and for the layers in the technological research experiment.

The increased importance for profiling is a tendency in the application of Auger analyses in microelectronics.

The precise profiling in AES requires a coincidence the electron and the ion beams.

We introduce methods for coincidence of the electron and the ion beams, as their practical application and performances are discussed.

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Electron Probe Microanalyses in Auger Electron Spectroscopy

Georgi Spasov Spasov

Abstract – **The electron probe micro analysis (EPMA) is examined as calibrating method for quantitative Auger electron spectroscopy (AES). It is used in AES profile analysis for finding the averaged Auger elemental sensitivity factors, leading to the quantification of the profile.**

EPMA can be also used for evaluating some parameters of the layer (thickness, weight content of component, etc.) if there is other available data for it. The performed Auger analyses of volumetric or layered samples with known composition prove the applicability of the method.

Keywords – **Auger electron spectroscopy, AES, electron probe micro analysis, EPMA, quantification**

I. INTRODUCTION

Micro- and nano-electronics are the main fields of application of Auger analyses. The reason is the unique possibility for element analysis of the surface, expanded with depth profiling. Usually the analysis is required to be quantitative, which is easy and always feasible if being "semi quantitative" is enough while it is traditionally hard – if accuracy is pursued.

The binary alloys' Auger quantification theory [1] states the content (the relative fraction), c_A, of the element A from the sample should be changed proportionally to its spectral intensity I_A:

$$c_A = (I_A / I_{0A}) / \sum_i (I_i / F_{Ai} I_{0i}) \qquad (1)$$

The introduced relative Auger elemental sensitivity factor (RAESF) I_0 is the spectral intensity from the pure (100%) element (so called elemental standard), normalized according to that of an arbitrarily fixed element. The correction factor F aims to equalize differences in the intensities for the sample and the standards, which are not connected proportionally to the concentration. (If a correction is not introduced, F=1). In classic matrix corrections those are due to the different atomic density, N, electron back-scattering factor, R and attenuation depth, λ (differences due to other reasons are also liable to correction).

We should note that ion sputtering is almost always used during the layer analysis. The occurring selective removal of the lighter and less bound component decreases its content in the outermost atom layer [2]. It is important for our presentation that in this case the real concentrations can be found by additional correcting. I.e. the sputtering is taken into account by additional multiplayer in the correction F.

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There are different methods for practical application of (1). The most accurate are the using standard specimens. In literature the electron probe micro analysis (EPMA) is indicated as standardizing analytical method. It has ~5% inaccuracy [3] – better than the desired for AES. But the considerable difference between Auger and EPMA information depth (some monolayers versus some microns) requires special care: EPMA result shows the integral composition of the analyzed layer. Meanwhile we didn't find anything concrete on the matter. Therefore – despite the risk to speak for something referred as obvious – we will share our experience from the last 15 years.

In the current article we will discuss the use of the electron micro analysis (EMPA) for calibrating the quantitative Auger layer-analyses. We will also adduce a few concrete applications.

II. EXPERIMENTAL

The Auger microprobe used has an energy resolution $\Delta E/E$ ~ 0.3 % and a beam energy E_p up to 10 keV. The analytic regime was E_p 3 keV and a modulation voltage V_{mod} 4 V_{pp}. The spectra are monitored in differential mode.

Electron Probe Micro Analyses (EPMA) were performed on ESEM XL30 FEI Co, allowing the light elements detection, at the beam voltage of 3.0 kV.

III. RESULTS AND COMMENTS

Let's assume we have performed Auger profiling of the analyzed layer through ion sputtering, obtaining the result as graphic "Auger intensity *vs* etching time".

A. EPMA calibration at homogeneous massive sample or layer

Despite this case is analytically trivial, we dwell on it due to its importance. If the sample is rendered standard (homogeneous and with known content) the EMPA result can be directly used for calibrating the Auger analysis. Otherwise if an unknown layer is analyzed and the Auger profiling shows its homogeneity, the EMPA result can be related to the layer (without performing Auger quantification). (In such case the layer shouldn't contain the same elements as the substratum). Example for this type of analysis is shown on Figure 1.

B. EPMA calibration in sample with concentration gradient

At constant sputtering rate in depth of the layer, the relation between the measured by EMPA content of the i-th element in the whole layer X_i (in atomic parts) and the determined by AES local concentration in the layer is:

$$X_i = k\int c_i(x)dx \quad (2)$$

where k is numeric multiplayer.

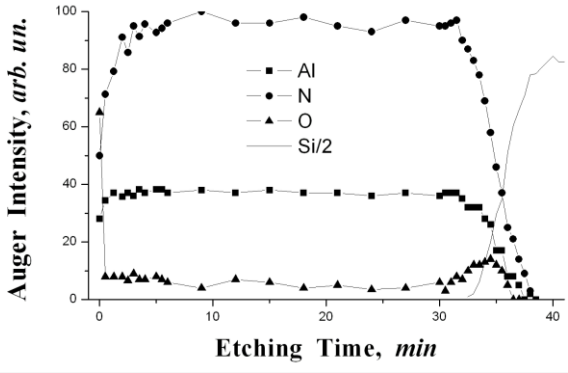

Figure 1. Auger profile of the AlN_x layer. EPMA measurement gives $x = 0.70$ and $c_O = 2.65$ at.%.

If the sum in the denominator of (1) is constant over the layer (mainly, if there are no unrelated to the concentration changes in the intensities), [2] is:

$$X_i = (kI_{oj}'^{-1}\Sigma^{-1})\int I_i(x)dx = kI_{oj}'^{-1}\Sigma^{-1}.S_i \quad (3)$$

where I_{oj}' is the corrected elemental sensitivity factor (including the correction for a selective etching), averaged for the layer. S_i is the integral from the intensity i along the layer (the area under the i-th curve, Figure 2). Dividing the expressions (3) for the i-th and j-th element, we get

$$I_{oi}'/I_{oj}' = (S_i/S_j)(X_j/X_i) \quad (4)$$

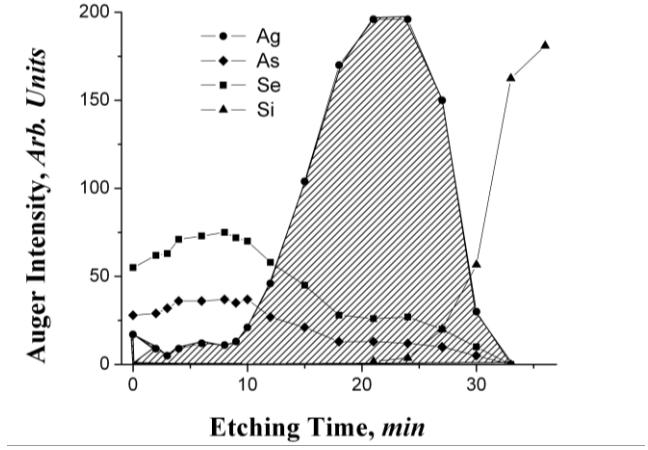

Figure 2. Auger profile of a sample (As_2Se_3 + Ag). The hatched area is for the silver.

(4) gives a linear system of (N-1) equations for the N unknowns I_{oi}', which solution is trivial (to an accuracy of a multiplier) – for example, assuming $I_{ok}' = 1$. Having RAESF, by (1) we can convert the y-axis of the profile into concentrations, Figure 3.

Evaluation of the inaccuracy of the method is done by the following experiment. Well known compositions – in the current case (As_2S_3 + Ag), (As_2Se_3 + Ag) and ([As, S, Se] + Ag) - are deposed on the silicon wafer by vacuum evaporation. A process of temperature annealing is conducted, leading to diffusion of the Ag in the layers (without evaporation of components). The first two samples are used as base and from their Auger profiles by EMPA calibration the RAESF for As, S, Se and Ag are found. With these RAESF the third profile is quantified. Integrating along the layer, the full content of its elements is found. The comparison with the real one (determined by EPMA) is shown in Table 1.

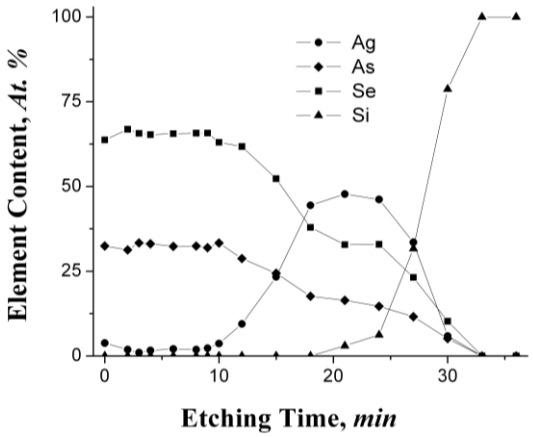

Figure 3. Quantification of the sample from Figure 2.

TABLE 1. ELEMENT CONCENTRATIONS (AT. %) AND THEIR ERRORS.

Ag	As	Se	S	Analysis
25.92	18.58	19.78	35.71	EPMA
26.0	19.2	20.2	34.6	AES
0.08	0.62	0.42	-1.11	Δc
0.3	3.3	2.1	-3.1	Δc/c, %

C. Determination of integral layer parameters using both EPMA and AES

The approach from chapter *III.B.* can be applied for calculating integral parameters of the layers too (i.e. parameters, obtained from integrating concentration-dependent quantities in depth of the layer). This is done as described above; of course additional data for the layer elements/compounds are required. Typical problem is finding the full mass of an element of the layer. We underline, that the state of the component in the layer has to be known, which will define reliable model for the calculations. The most simplistic case is an alloy from the layer components. If the components have weight parts W_i and densities ρ_i, the layer density ρ_l is $\Sigma^{-1}(W_i/\rho_i)$, which allows determination of the mass of the element in the layer if the layer thickness is known. This is demonstrated in Figure 4 and 5 for layer systems (Ag, Cu, As_2S_3, Cr) from a study for ion-selective membranes. In Table 2 the basic steps for checking the accuracy of the method are shown. Here, the first sample is used as a standard for EPMA calibration of RAESF of the elements. Via the determined RAESF the second sample (with known layers) is quantified. The sought integral quantity in the case is the layer thickness, which would contain the full amount of an element from the layer. This quantity is compared with the thickness of the initially deposed elemental layer.

D. Discussion

In the first place stands the issue, to what extend the assumptions, made for deducing (4) are valid. The first – constant sputtering speed along the layer – is assumed correct mostly for easing the presentation. The change in the sputtering speed as a result from the change in the content is a known problem for the ion sputtering (known in Auger profiling as "calibration of the depth scale").

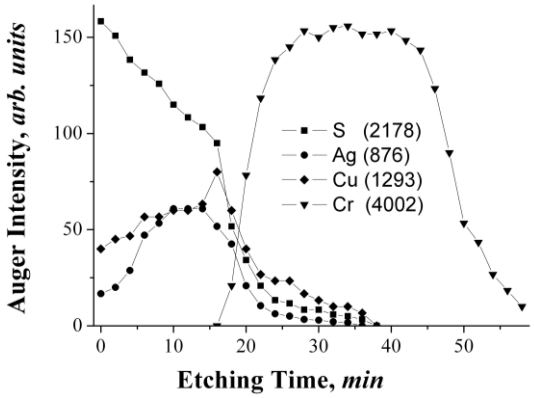

Figure 4. Auger profile of the standard (As_2S_3, Cu, Ag, Cr).

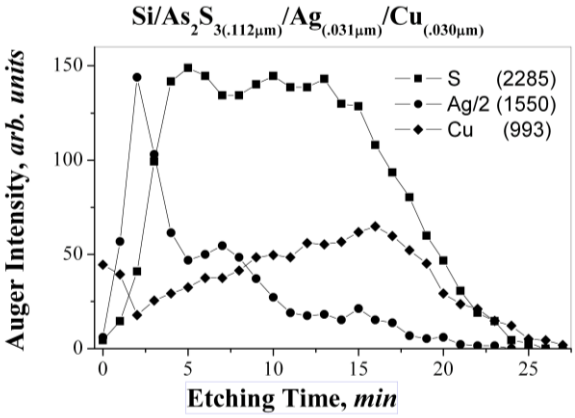

Figure 5. Auger profile of the specimen (Cu, Ag, As_2S_3)/Si. (Silicon intensity is not represented).

The situation is more serious for the factored out the integral sum in (3). This is an approximation and the introduced inaccuracy is smaller, the smaller is the area, related to the analyzed system towards that of the concentration figure (triangle, square, etc.) for the participating elements. In the case the close compositions and their smooth "transfusion" should ensure the lack of both unconnected to the concentration changes in the intensities (there are no metallurgical junctions), and small concentration-dependent corrections, connected to the matrix (close concentrations). This is the situation for several important for the practice cases. For example, in case of ternary or quaternary quasi-binary $A^{III}B^{V}$ solid solutions (Auger analyzed), the concentration of one (or two) of the elements is constant while it is remaining in limited ranges for the rest.

The essence of the suggested method for RAESF determination is finding average ones for the range, which the system is analyzed in. I.e. the found RAESF are local and valid for the concrete analysis (the concentration zone of the system). For some elements from the composition they should be increased (slightly) while for others decreased (slightly), leaving the analysis in the range of acceptable inaccuracy, Figure 6. (The determination of the value of the averaged RAESF is done by calibration with the EMPA data.)

TABLE 2. BASIC STEPS FOR CHECKING THE ACCURACY OF THE METHOD (PROFILE AES + EPMA) AT A DETERMINING THE THICKNESS OF EVAPORATED LAYERS.

Ag	Cu	As_2S_3	Cr	Notice
Standard				
0.070	0.105	0.289	0.536	*at.*% (EPMA)
584	431	1452	2668	Area, *arb. units*
8392	4106	5021	4976	Area (100%)
1.000	0.489	0.598	0.593	RAESF
Specimen				
1550	992.5	2285	-	Area, *arb. units*
1550	2028	3819		Area/RAESF
21.0	27.4	51.6		*at.*% (AES)
32.3	29.5	111.2		d, *nm* *
31	30	112		d experiment, *nm*
4	-2	-1		Δd/d, %

* The measured total layer depth is 173 *nm*.

The question, why the described procedure should be used for obtaining the integral parameters of the layer, instead of directly using the (integral) EMPA data, might arise. The reason is the higher accuracy. Auger profile gives the depth composition in detail, permitting the usage of parameters for the exact compositions (for example, density for Al and Al_2O_3 in different areas of the profile (instead of the averaged for the AlO_x). Also it has EMPA-detectors, which do not register the light elements, not allowing the exact determination of the composition in this case.

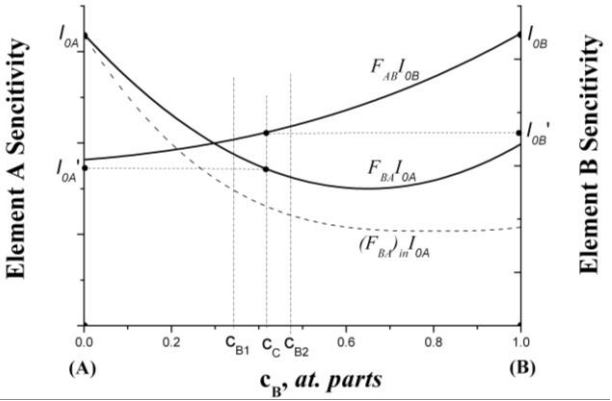

Figure 6. Binary composition of the elements A and B (The concentration figure is a leg). The true sensitivities (after "total correction" F_{ij}) are plotted with solid curves (The dash curve depicts the result of an incomplete correcting). The EPMA result at c_c averages the sensitivity in the profiling range (c_{B1}, c_{B2}).

Evaluation of the inaccuracy of the discussed methods – as usually for the Auger problems – is done by quantitative analysis of standards. Two standards are prepared. In the case, well-known compositions are vacuum evaporated

(metal layers with known thickness). A process of temperature annealing is conducted (without component evaporation). Via the suggested method RAESF are found from one of the standards, through which are determined the integral quantities from the second standard (for example masses of the evaporated metals). The obtained results are compared with the known. During such tests we get match within 10%. Therefore we assume that the incorrectness of the discussed methods is 10%. (Actually it can be lower, since some decrease in the thickness of the evaporated layer occurs during its annealing to a metal; for example for aluminum we have determined the decrease to be 5-10%).

To use the procedure, the occurring processes have to be known in order to use adequate model for describing the integral quantity. (For example, the used above formula for alloys might not be valid if any chemical reactions in the layer have occurred; at temperature processes it is mandatory that there is no evaporation of elements/components from the layer etc.).

Our discussion has been for determining masses, but it is also possible to determine other integral quantities for the layer. Additionally, depending on the experiment or the concrete necessity, the input/output data can be presented according to the need. For example, the evaporated component can be submitted as mass or thickness of the evaporated layer. Overall, in mass measuring, the relation between the mass m, density ρ and the layer geometry (thickness d, area S) – applied to the output and final layers – makes it possible to look for any of the quantities involved:

$$m = \rho dS \tag{5}$$

We have used the suggested quantification method for about 15 years, but it is the first time we publish its reasoning. We have applied it in 4 works for ion-selective membranes (most Auger orientated is [4]); 4 works for deposition and studying AlN (most Auger orientated is [5]); 5 works for humidity and ethanol sensors (most Auger orientated is [6]); 5 works for applications in micro-electronics and others (most Auger orientated is [7]).

IV. CONCLUSION

1. In the current article we discuss the use of the electron probe micro analysis (EPMA) for calibration in quantitative Auger layer analyses.

2. We suggest a method in which averaged Auger elemental sensitivity factors are determined by EMPA data and Auger profiles. Its essence is calibration through the EMPA data of the integral content of an element in the layer (proportional to the result from the numeric integration of the respectful Auger intensity along the profile).

3. The method is base for determination of the concentration-dependent integral parameters of the layer.

4. The applicability and accuracy of the methods is demonstrated through profile Auger experiments. In one of them the full content of the elements in the layer is determined, while in the other – the thicknesses of the deposed layers (related with their mass).

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Studying of Converter for Charging and Management of Energy Flows in Photovoltaic System

Ivan Ivanov Nedyalkov, Dimitar Damyanov Arnaudov and Nikolay Lyuboslavov Hinov

Abstract – **In the following article a converter, providing management of the energy flow from the photovoltaic system (PV) to the elements for energy storage – supercapacitors, has been studied. The proposed converter provides charging and voltage balancing across series connected elements (supercapacitor cells). Simulation and experimental studies of the proposed circuit, from the PV system, has been made. Characteristics of the tested converter were made**

Keywords – **Supercapacitor charging, Resonant converter, PV system**

I. INTRODUCTION

For extending the operational life of a battery, used in a photovoltaic system, a mutual work between battery and supercapacitor is applied [1, 2, 3, 4, 5, 6]. The purpose of the supercapacitor is to provide high power to the load, for a short period of time, without using the battery and so to reduce the discharging/charging cycles of the battery. A typical example for such kind of load, requiring a lot of power for short period of time, is the telecommunication equipment, transmitting data at certain intervals of time. For studying the management algorithms of energy flows, via PV, battery and supercapacitor, a test bench of a PV system has been created [1].

In the proposed system the bi – directional converter, providing the energy transfer to/from the supercapacitor, is made of two unidirectional converters. The block diagram of the proposed system is shown on figure 1.

II. MANAGEMENT ALGORITHM FOR ENERGY FLOW

To create a converter for charging supercapacitors and reservation of the energy, a circuit, proposed from the authors, is used. The proposed circuit is based on Resonant Converter with Voltage Limitation Over the Commutating Capacitor (RIVLOCC). The circuit of the charging converter is shown on figure 2. Figure 1 shows the block diagram of the proposed system.

The management algorithm is the following: When the PV system generates instantaneous power, bigger than the consumed power in the load, the difference between generated and consumed power is priority accumulated in the supercapacitor. When load demands higher power, the DC/DC2 converter provides the desired power, by the control system.

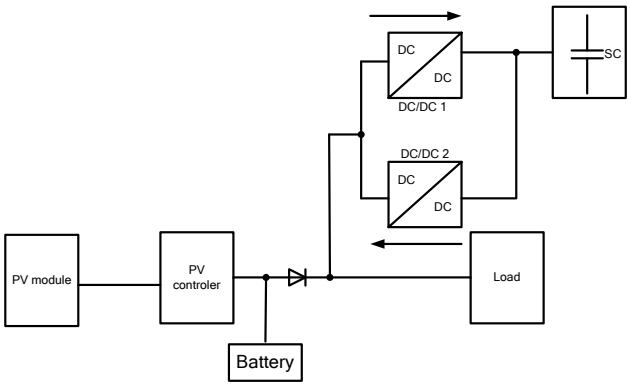

Fig.1. Block diagram of the proposed system

Because of the factory tolerances of the capacitors capacity, they discharges to a different voltage, since the consumed current, from the series connected capacitors, building the supercapacitor pack, is the same. When the voltage over one cell reaches zero, the consumptions must stop. In the following charge, it is necessary first to charge the cell, with the lowest voltage level. The circuit, providing these working regimes, is RIVLOCC. In the diagonal of it a double – phase, half – wave rectifiers are connected, by using an inverter transformers, which are used for charging of the supercapacitors.

There are other applications of supercapacitors in hybrid systems [7].

III. STUDYING OF THE CONVERTER FOR CHARGING AND VOLTAGE BALANCING OVER SERIES CONNECTED SUPERCAPACITORS CELLS

The working principal of the circuit from figure 2 is similar like the working principal of RIVLOCC. When the voltage across C_k reaches the value of $\pm U_d/2$, the limitation diodes (D_{d1} or D_{d2}) turns on and starts to conduct, where U_d is the power supplying voltage of the converter.

At the working process of the circuit, during charging of the supercapacitor cells, there is a moment when the limitation diodes D_{d1} and D_{d2} does not turn on. This is achieved when the voltage over C_k is always lower then $\pm U_d/2$. In this case the circuit works like Resonant Inverter with Reverse Diodes - RIRD.

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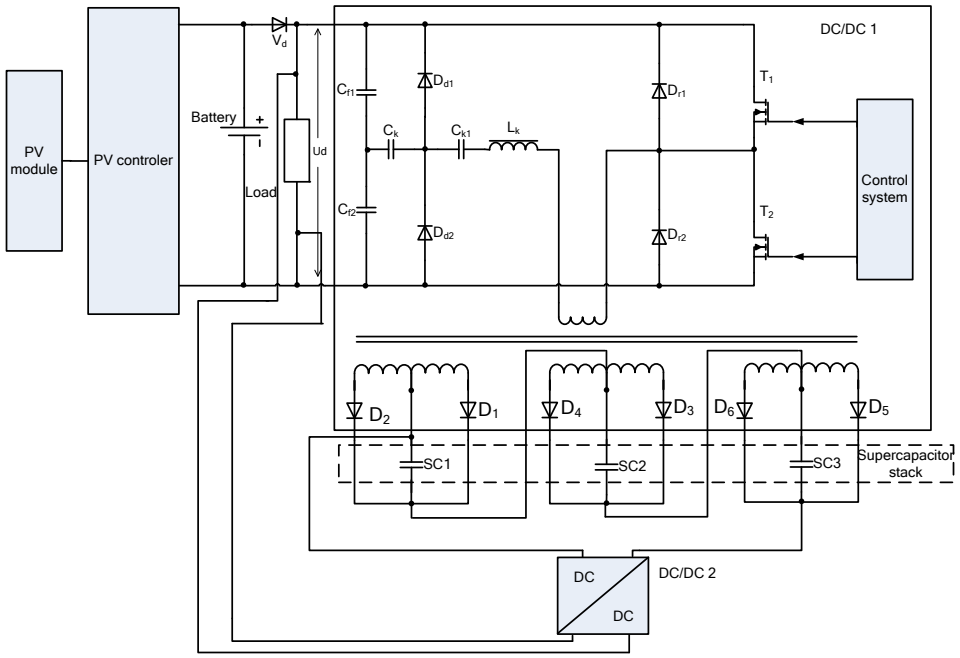

Fig.2. Proposed circuit for charging and balancing

Simulation and experimental studies of DC/DC 1 converter, from figure 2, has been made. The studies havebeen made on three supercapacitor cells. The capacity of cell 1 is 20% lower than cell 2. The capacity of cell 3 is 20% bigger than cell 2.

A simulation model, based on the circuit from figure 2 has been made, using LTSpice. The used transistors in the model are with low R_{DS}. The supercapacitors are presented with their equivalent model, made of series connected resistor and capacitor. For more precise simulation studies the supercapacitor models from [7] can be used.

For the simulation studies the capacity of the cells are significantly reduced, than the real, to assess the quality of the circuit, for less simulation time.

Figure 3 shows the waveforms of the charging currents through the supercapacitor cells – I(Csc1), I(Csc2), I(Csc3), and the voltage over the cells .

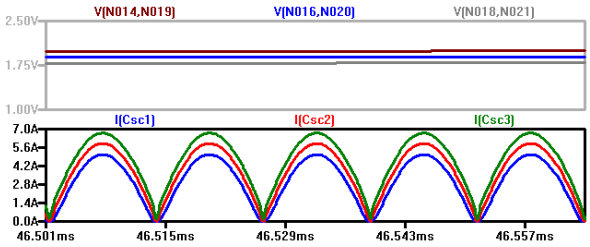

Fig.3. Charging currents and voltages over the cells

I(Csc1) is the charging current through cell 1, I(Csc2) is the charging current through cell 2 and I(Csc3) is the charging current through cell 3.

V(N014, N019) is the voltage over cell 1, V(N016, N020) is the voltage over cell 2 and V(N018, N021) is the voltage over cell 3.

As we can see from the waveforms, the difference in the voltages, between the cells is almost the same.

Figure 4 shows waveforms of the current through the transistor and its reverse diode – Id(T1), the current through the limitation diode – I(Dd1) and the voltage across the transistor – V(N002, N010). As we can see from the waveforms the transistor turns on, on zero current and turns off, on zero voltage (ZCS and ZVS).

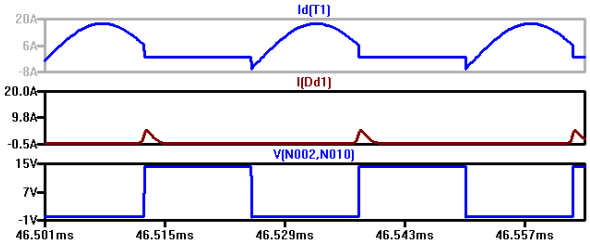

Fig.4. Current through transistor, reverse diode, limitation diode and voltage over the transistor

IV. Studying of Converter for Charging and Voltage Balancing over Series Connected Supercapacitor Cells, by Using CL – filter on the Rectifiers

To charge the supercapacitor cells with constant current, instead charging with pulse current, the circuit on figure 5 is proposed. The outputs of the rectifiers are connected to CL – filters (Cff1 and Lff1).

Figure 6 shows the waveforms in the begging of the charging process. The shown waveforms are: current through one of the transistors and through its reverse diode – Id(T1), voltage over it – V(N002, N010), current through two of the rectifying diodes – I(Diz1), I(Diz2), current trough supercapacitor 1 – I(Csc1), and voltages over the three supercapacitor cells – V(N019, N021).

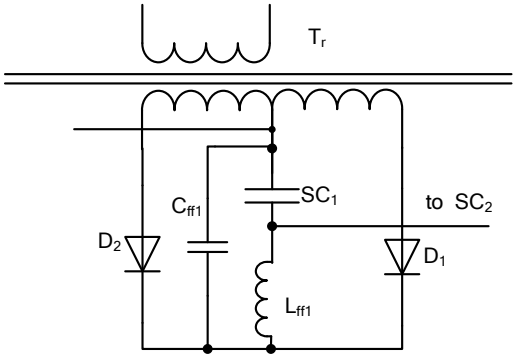

Fig.5. Using CL – filter on the rectifiers

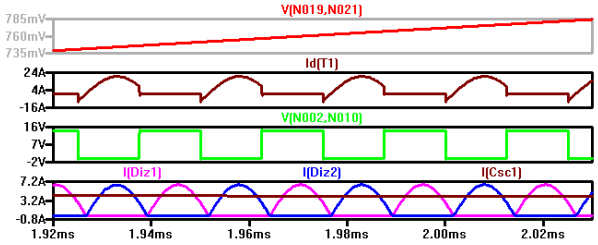

Fig.6. Currents and voltages in the begging of the charge

Figure 7 shows the following waveforms: current through one of the filter capacitors – I(Cff1), Currents through rectifying diodes – I(Diz1) and I(Diz2), voltage across diode D1 – V(N013,N014), the and current through one of the supercapacitors – I(Csc1).

As we can see, the maximum value of the charging current flows through the filter capacitor. Through the charged supercapacitors cell flows the average value of the charging current.

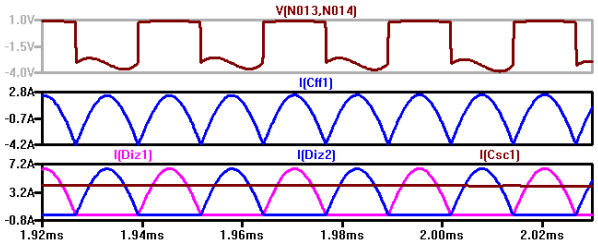

Fig.7. Currents and voltages in the load circuit

V. EXPERIMENTAL STUDIES

For conducting of the experimental studies of the circuit from figure 2, a test circuit has been developed. For management of the converters and testing different management algorithms of the energy flows, a virtual instrument has been developed, by using the software for graphical programming – LabView. The virtual instrument is described in [1]. Experimental studies for evaluation of the parameters of supercapacitors can be find in [8].

Figure 8 shows the current through one of the transistors and voltage over it, obtained from the experimental studies. As we can see the transistor turns at zero current and zero voltage, which confirms the simulation results.

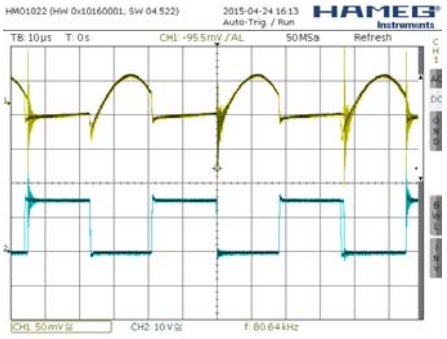

Fig.8. Current and voltage of one of the transistors

The characteristics from figures 9 to 13 are made from the carried out simulation studies. These characteristics show the change of the corresponding parameter, by changing the voltage across the charging supercapacitor cell – SC1. The characteristics are built up in relative units to the value of the corresponding parameter - beginning of the charge, when Usc = 0V

Figure 9 shows the change in the average value of the charging current through SC1.

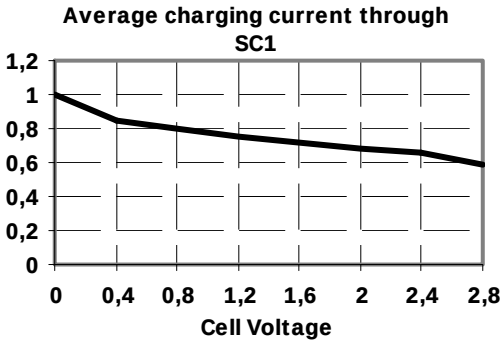

Fig.9. Average charging current characteristic

Figure 10 shows the consumed current by RIVLOCC in relative units. From the chart we can see that the consumed current is approximately constant.

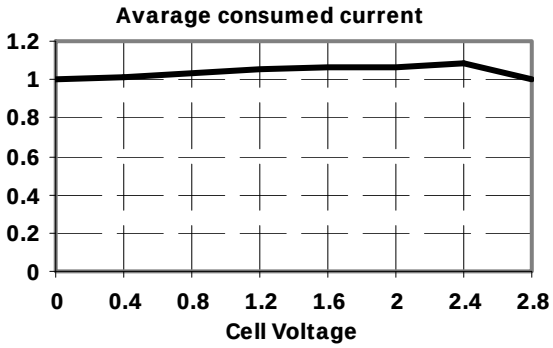

Fig.10. Average consumed current characteristic

The circuit is so designed that by reaching the value of 2,6V across the supercapacitor cell, the limitation diodes D_{d1} or D_{d2} stops working.

Figure 11 shows the change of the maximum value of the current through one of the transistors, during charging.

Figure 12 shows the characteristic of the maximum current through the reverse diode during the charging process.

Figure 13 shows the change in the maximum value of the current through the limitation diodes. From the chart we can see that, when the voltage across the supercapacitor cell is 2.6V, limitation diodes are turned off.

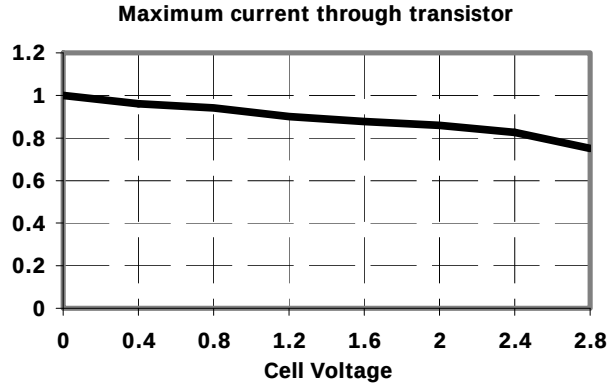

Fig.11. Maximum current through transistor characteristic

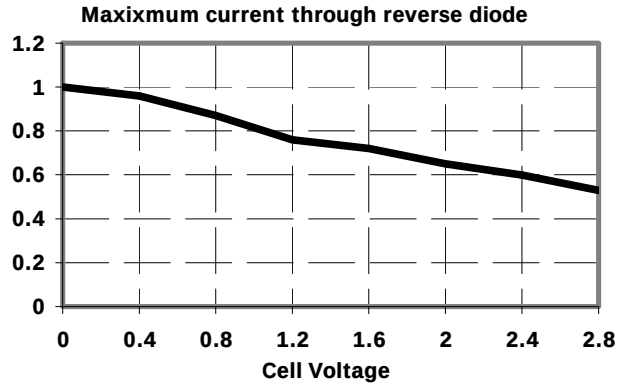

Fig.12. Maximum current through reverse diode characteristic

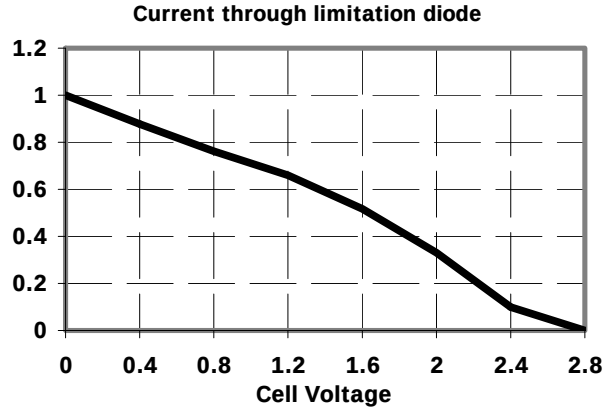

Fig.13. Maximum current through limitation diode characteristic

VI. CONCLUSION

1. Circuit of a converter for management of the energy flows at charging, of series connected supercapacitor cells, is developed. The circuit provides charge initially to the supercapacitor cell with the lowest voltage over it. The developed model allows examining the characteristics of the converter for management of the energy flows and charging of series connected elements for energy storage. By using the obtained characteristics, different algorithms for management of the energy flows in a PV system, can be developed.

2. Using a CL – filter (fig.6) in the circuit from figure 2, provides charging with constant current instead with pulse current.

3. The obtained characteristics of the maximum value of the currents through the elements, allows the capability of evaluating the qualities of the proposed circuit and selection of some basic rations at designing the circuit.

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Control of Induction Heating Power Converter for Ferromagnetic Materials Melting

Dimitar Nikolov Penev, Nikolay Lyuboslavov Hinov and Tzvety Hristov Hranov

Abstract – **The paper discusses the electronic control of Induction heater power converter for ferromagnetic materials melting working in independent excitation. The system of power electronic converters is composed by a controlled three-phase rectifier and parallel current source inverter. Analysis of regime with fixed current from the DC supply source has been made. This guarantees working with maximum power and respectively short meting process time.**

Keywords – **Frequency converters, Current source inverter Simulation, Controllers, Induction melting, Robust control, Power Electronics.**

I. INTRODUCTION

The control of electronic converters for supplying power for induction heating is important part of the technological process in the electrothermical devices. It is expected to provide normal operation of the converters, keeping the electrical regime of the electronic devices optimal and achieve best electrical properties [1-4, 6, 7, 9].

On the other side for the normal operation of the system of power electronic energy converters in the devices for induction heating it is necessary to achieve the following conditions [1, 4, 6, 7]:

• The consumed current from the supply unit I_d must not exceed the boundary value $I_{d\,adm}$;

• The inverted voltage and also the voltage over all circuit's elements must not exceed their maximum ratings;

• When using thyristor circuits (common practice in the ferromagnetic materials melting), the commutated turn-off time t_{qc} must be greater than the datasheet specified t_q for the elements.

For the utilization of such systems two methods of automated regulation of the electrical regime are possible for the converters [1, 7]:

• Stabilization of the inverted voltage U_T. This regime finds application in the devices for surface metal hardening and heaters with methodical operation, where it is necessary repetitiveness of the process of heating in periodical change of the molds;

• Stabilization of the consumed current I_d of fixed value. This is used in the devices for melting, because it guarantees working with maximum active power and respectively fastest melting of the metal.

In the operation of the induction heating system in each of these regimes, it is observed change in the equivalent resistance of the load [1, 6, 7]. Because of that during the technological process it is possible disruption of the normal operation of the electronic converters.

The emphasis of the work is the control of a thyristor frequency converter, composed of three-phase rectifier and parallel current source inverter with active-inductive load.

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II. CONVERTER MODEL

The schematic of a parallel current source thyristor inverter is shown on Fig. 1. By the synthesis of the mathematical model are made the following assumptions:

• The pulsations from the DC source are not considered;

• The thyristors are simulated as ideal switches, the capacitors and inductors have no losses;

• The magnetic components are linear;

• The current commutation between the thyristor pairs is instantaneous.

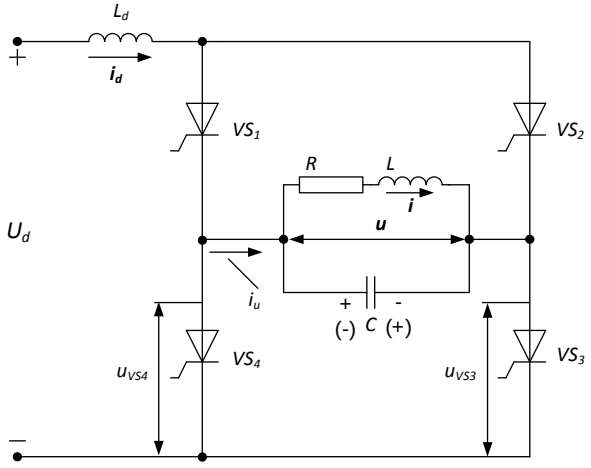

Fig. 1. Full Bridge parallel current source thyristor inverter with active-inductive load circuit.

The workings of the power circuit is discussed in [1, 7, 9]. In the mathematical representation of the inverter can be distinguished two structures [13]:

The first is when thyristors VS_1 and VS_3 are conducting and is assumed that this is through the positive half-waves of the inverted current n = 1, 3, 5... (n is the number of the half-wave);

and the second – when VS_2 and VS_4 are conducting through the negative half-waves n = 2, 4, 6... In order to illustrate these commutations a coefficient is defined:

$$k = \begin{cases} 1, & npu\ i + C\dfrac{du}{dt} > 0 \\ -1, & npu\ i + C\dfrac{du}{dt} < 0 \end{cases} \quad (1)$$

This approach allows unifying the differential equation system describing the two half-waves. A state vector is defined as:

$$x = \begin{vmatrix} u \\ i_d \\ i \end{vmatrix},$$

where:

u - the voltage of the capacitor;

i_d - input current;

i - load current.

If for the examined circuit is applied first and second Kirchhoff's laws and write down:

$$\dot{x} = Ax + bU_d, \quad (2)$$

where:

U_d - supply voltage and A and b matrices are:

$$A = \begin{vmatrix} 0 & \frac{k}{C} & -\frac{1}{C} \\ -\frac{k}{L_d} & 0 & 0 \\ \frac{1}{L} & 0 & -\frac{R}{L} \end{vmatrix} \qquad b = \begin{vmatrix} 0 \\ \frac{1}{Ld} \\ 0 \end{vmatrix} \quad (3)$$

The shown model is realized in Matlab software environment. When the DC–AC converter is working in melting regime, the changes of the load must be considered, which are described in detail in [1, 16] and shown on Fig. 2.

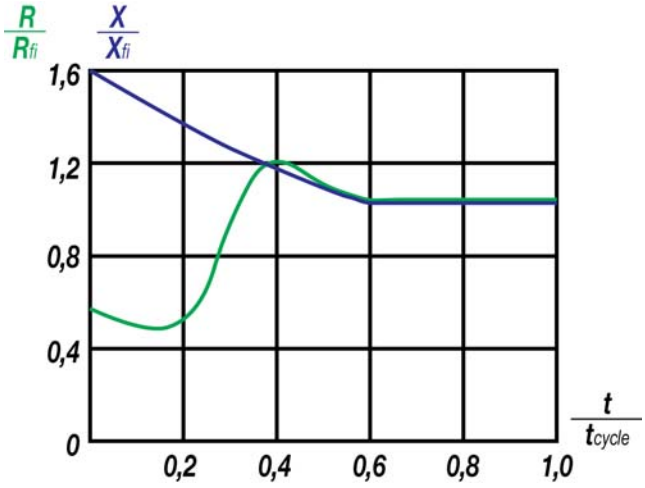

Fig. 2. Change of load paramaters during the melting

When melting ferromagnetic materials the technological process sets the following restrictions:

• input current - $I_D \le I_{Dmax}$; (4)

• output voltage of the converter - $U \le U_{max}$; (5)

• recovery time of the thyristors - $t_{qcmin} \le t_{qc} \le t_{qcmax}$; (6)

• minimum operating frequency in order the converter to work above resonance. (7)

The task is to operate the input current of the converter in the different regimes – warming (from cold) and melting (from hot). The control is done through varying the converter operating frequency

III. Control Algorithm

The control algorithm must allow effective operation at start-up of the system, working in warming regime, melting and processing disturbances in the input supply voltage channel.

Developing the control algorithm requires the following:

• Considering the restrictions (4) to (7);

• Comply with the settled current values, which are different for warming, transition and melting (Fig. 2)

• Choosing and setting up a regulator, that is robust in relation to changes of circuit's parameters.

The arrangement shown on Fig. 5 consists from four intervals:

• for the interval $t \in [0;0.1]$ the current is rising linear for a soft start;

• for the interval $t \in [0.1;0.6]$ has constant value 80 A, according to the warm-up regime;

• for the interval $t \in [0.6;1]$ is arranged linear change of load parameters with respect for transition from warm-up to melting regime;

• for the interval $t \in [1.0;1.6]$ the current is constant at 200 A according to the melting regime.

In the moment t = 1.2 the supply voltage is lowered with 20% (Fig. 7).

The block diagram of the controller is shown on Fig. 3 [12]. This structure provides saturation of the integrator output (anti-windup) and saturation of the regulator output. This allows for restriction of the input current (4). The other restrictions (5) to (7) are satisfied with a rational arrangement of the inverter circuit's elements [6, 7].

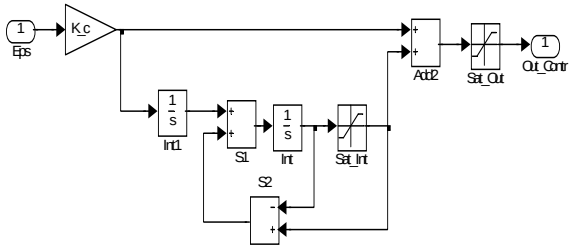

Fig. 3. Block diagram of the controller

IV. Modeling Results

The model block diagram is shown on Fig. 4. It is composed of the following elements – reference block (Reference), controller (Controller), converter controller to frequency (Converter contr to frequency), current FET converter (Current FET Converter), block supply voltage reference (Ref U), reference block loading coil (Ref L) and block assignment active resistance (Ref R).

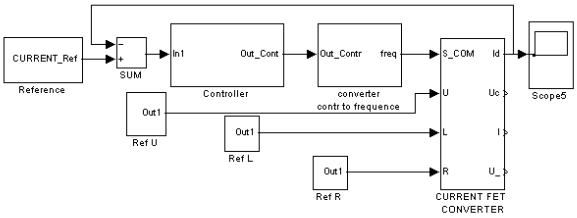

Fig. 4. Model block diagram of the technological device for metal melting

A current-source parallel inverter is designed according to [7, 8] with the following parameters in melting regime:

• active output power P_T = 100 kW;

• working frequency at the end of the process – f = 2.4 kHz;

• Power factor in the load cos(φ_T) = 0.1;

• Output voltage in the load U_T = 700 VAC;

• Input voltage U_d = 500 VDC;

In warm-up regime is referenced input current I_d = 80 A, and in melting regime I_d = 200 A (Fig. 5).

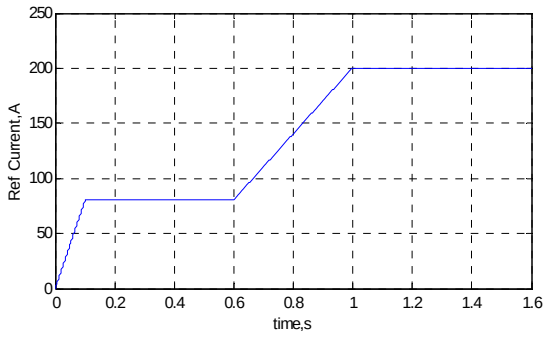

Fig. 5. Current reference

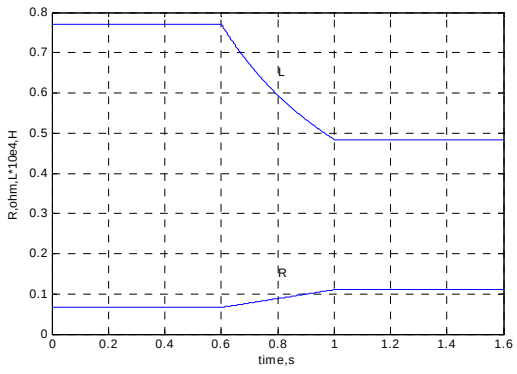

Fig. 6. Change of load parameters

The controller reference data must be set so, that the load parameters R and L (Fig. 6) doesn't affect the stability and quality of the processes in the technological device, that is to guarantee robust stability and quality [12] of the processes in the melting system.

Because of the thermal time constants are much greater from the electrical time constants in the inverter the main requirement is bound with the stability of the system, without having requirements to the transient processes in the converter. In the case it's inappropriate to use differential component mainly because of the presence of higher frequencies in the output (current) of the inverter.

The control has significant reserve with respect to the rate of change of the load parameters R and L. In this paper is the entire time for the changing values of R and L is considered 0.4 seconds. In reality this time is several magnitudes higher.

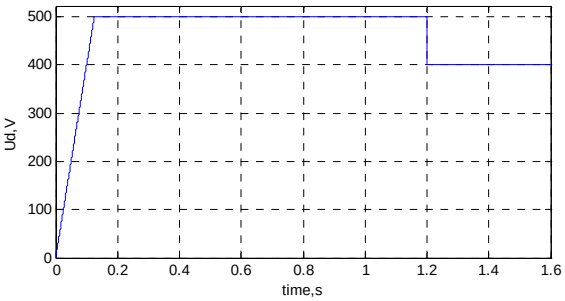

Fig. 7. Supply voltage change

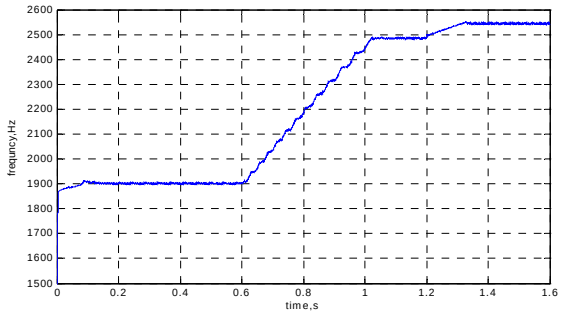

Fig. 8. Inverter operating frequency change

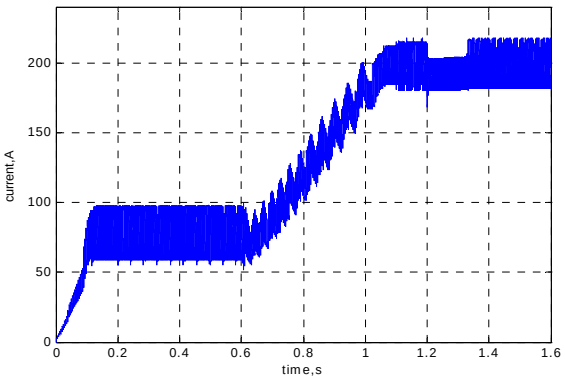

Fig. 9. Input current

In spite of the significant change in the resonant frequency of the parallel load circuit at the change of load parameters, the operating frequency (Fig. 8) is changing in the settled boundaries. This allows the operation of the system at high energy efficiency. At all regimes the inverter frequency is greater than the minimum allowed 1816 Hz.

From Fig. 7 and Fig. 9 is visible that the processing of a disturbance at the input supply voltage with the chosen controller is effective and with enough speed performance.

When comparing the results shown on (Fig. 5) and (Fig. 9) is determined that the processing of the parameters in all regimes is with enough accuracy.

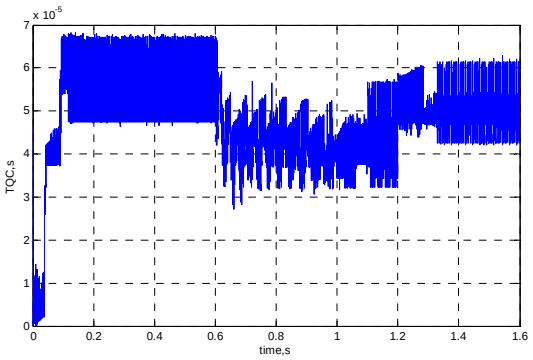

Fig. 10. Circuit's commutated turn-off time of the thyristors

V. CONCLUSION

As a result to the laid out above is determined that the system is designed correctly and is appropriate with the requirements of the technological process. A good control with guaranteed quality and high energy efficiencies is achieved.

The performance of the converter is proven to the changing parameters of the parallel load circuit with respect of the restrictions, set by the switching elements, at working frequencies maximum close to the resonant.

The realized method for control allows for the process to be controlled without regulation of the supply voltage. This rises the power factor and lowers the consumption of reactive power.

The system is with reserve for robustness, because the change of the parameters in the real process are significantly slower than these assumed in our research.

The use of classical tools for control simplifies the technological realization and rises the safety of the system.

From another point of view the system is unsusceptible to great changes in the supply voltage (up to 20%) which is the main disturbance at the work of these types of thermical devices in real production conditions.

The analysis of (Fig. 10) shows that the commutated turn-off time is in the boundaries defined by the data sheets. It is found out also that independently of the change of the supply voltage and the current reference to the controller, in the initial moment the circuit's commutated turn-off time for the thyristors is insufficient for the safe operation of the device. In this relation it is necessary to correct the control system with emphasis on eliminating this flaw or usage of another starting procedure [1, 7].

A future research on the system operation including the effect of the non-linearity of the inductive elements is considered useful alongside the expansion for other technological objects like the induction heating, welding and rectifier converters and others.

At higher quality requirements and speed performance at fixed robustness is possible and effective use of advanced control methods, in particular the model predictive control [15, 16].

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LabVIEW Virtual Instrument for Modeling and Control of Three-Phase BUCK Rectifier with Sinusoidal PWM

Stoyan Aleksandrov Vuchev, Georgi Tzvetanov Kunov and Dimitar Damyanov Arnaudov

Abstract – **The present paper considers a developed by the means of the LabVIEW software virtual instrument for modeling and control of three-phase BUCK rectifier with sinusoidal PWM. It generates control pulse sequences which can be used to control a rectifier via proper hardware and driver stages. The structure of the virtual instrument is presented. Results from its operation are obtained and compared to the ones from a simulation of the device via MATLAB Simulink. Apart from the control capabilities, this virtual instrument can be used for simulation of the operation of three-phase rectifiers with sinusoidal PWM as well.**

Keywords – **Virtual Instrument, LabVIEW, Three-Phase Rectifier, Sinusoidal PWM, Power Factor Correction.**

I. INTRODUCTION

Three-phase rectifiers with sinusoidal PWM are used in order to improve the power factor of the devices. There are different power circuits for realization of three-phase rectifiers using combinations of transistors and diodes as power switches [1, 2, 3, 4, 5].

Circuit of the considered rectifier is presented in fig. 1. It is realized by a conventional three-phase bridge with six unidirectional switches (*VD1*, *VS1* ÷ *VD6*, *VS6*). Its control unit consists of driver stages, CDAQ frame with TTL input-output module and the developed virtual instrument.

Different control algorithms for three-phase rectifiers are known. One of them is illustrated in [6]. By analogy to this algorithm, a MATLAB Simulink model of the investigated rectifier and its control unit is designed [7].

According to the algorithm characteristics, PWM sequences are obtained for each transistor via comparison between a sinusoid and a high-frequency saw-tooth signal. When one of the grid phase voltages is the most positive or negative compared to the other two, the corresponding switch conducts according to its own pulse sequence. Otherwise, its gate is controlled by the sequences for the prior and the next to conduct switches. Equations (1) and (2) illustrate this for the gate signals *G1* and *G4* of transistors *VS1* and *VS4*:

$$G1 = R\_MAX.R\_POS \cup pwmSp.pwmTn.S\_MIN.RLp \cup pwmTp.pwmSn.T\_MIN.RLp \quad (1)$$

$$G4 = R\_MIN.R\_NEG \cup pwmSp.pwmTn.S\_MAX.RLn \cup pwmTp.pwmSn.T\_MAX.RLn \quad (2)$$

where *pwmXp* and *pwmXn* are the PWM sequences for the positive and negative side switches of the corresponding phase, *X_MAX* and *X_MIN* determine the most positive and negative phase voltage, and *X_POS* and *X_NEG* indicate the sign of these voltages.

$$RLp = \overline{R\_MAX}.R\_POS \quad (3)$$

$$RLn = \overline{R\_MIN}.R\_NEG \quad (4)$$

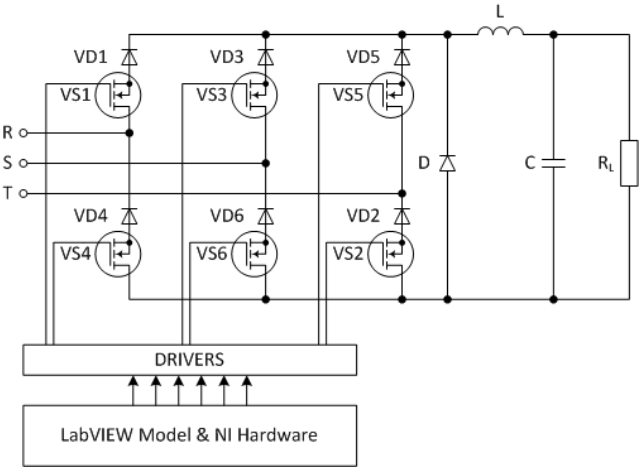

Fig. 1. Circuit of the considered rectifier.

By the means of the operation algorithm, a power factor correction can be obtained without using additional PFC circuits. When the output voltage of the considered rectifier varies from 0 to the maximum value, unlike with the conventional circuits of controllable rectifiers with thyristors, its power factor high values are maintained.

On the basis of the analysis in [7], a virtual instrument realizing the illustrated control algorithm is developed. It consists of two main parts – a Front Panel and a Block Diagram. The influence of the input filter on the circuit operation is not an object of the present analysis for both the MATLAB Simulink model and the developed virtual instrument.

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II. VIRTUAL INSTRUMENT FOR MODELING AND CONTROL OF THREE-PHASE BUCK RECTIFIER WITH SINUSOIDAL PWM

A. Front Panel of the Virtual Instrument

Fig. 2. illustrates the Front Panel of the virtual instrument.

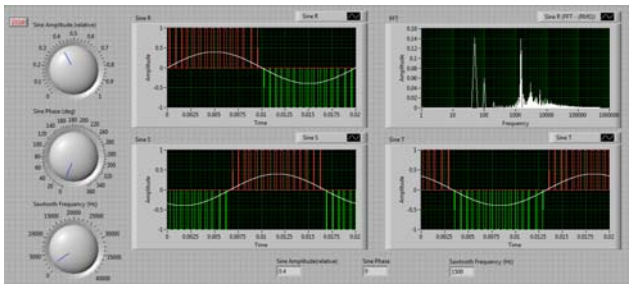

Fig. 2. Front Panel of the Virtual Instrument.

Graphical knobs are adjusted to the Front Panel in order to set the required depth of modulation (the sinusoid magnitude in relative values from 0 to 1), the saw-tooth frequency and the phase shift of the primary grid voltage (phase R). The values of these three parameters are displayed via numeric indicators at the bottom of the panel.

Graphical indicators are put as well for visualization of the shape of the control sequences required for the corresponding transistors for the positive and negative half period. These indicators allow visual perception of the controllable rectifier operation.

Another indicator illustrating the spectral composition of the generated PWM signals is also adjusted to the Front Panel. The displayed results allow determination of the input current spectral composition, which helps evaluating the rectifier power factor.

B. Block Diagram of the Virtual Instrument

The Block Diagram of the virtual instrument is presented in fig. 3. As it is a three-phase circuit, there are repetitive elements which are realized as subunits (*subVI*). The Block Diagram consists of seven different units:

- *Unit 1 (subVI 1)* – this is the Signal Generation Block. Its main features are related to determination of the most positive and most negative phase voltage, indication of the sign of each phase voltage, as well as, generation of the primary PWM sequences for each of the rectifier transistors. Each of the three main functions is realized by a separate subunit as it is shown in fig. 4.
- *Unit 2 (subVI 2)* – this is the Signal Distribution Block. It realizes the logic responsible for the formation of the gate PWM sequences for each switch. This block consists of six identical subunits each of them corresponding to one of the power circuit transistors. The inner logic of the subunits is shown in fig. 5. The structure of the Signal Distribution Block is presented in fig. 6.
- *Unit 3* – this unit consists of three identical sine wave generators, as well as, a saw-tooth one. The frequency of the three sinusoids is fixed to the value of the grid frequency (50 Hz). The sinusoid labeled with R is admitted to be the primary one. Its phase can be set from the front panel. The other two (respectively S and T) are shifted at 120 degrees prior and next to R.
- *Unit 4* – it contains the three graphical knobs used to set the main operating parameters of the virtual instrument. The numeric indicators with their values are not marked as part of it but may be considered so.
- *Unit 5* – this unit consists of the three graphical indicators and the corresponding logic used to display the three sinusoids and the generated gate PWM sequences for the six transistors. The control signals for the even numbered switches (respectively for the negative half periods of the three phase voltages) are displayed inverted.
- *Unit 6* – it consists of the graphical indicator and the corresponding logic for spectral composition analysis of the generated PWM sequences.
- *Unit 7* – it contains the blocks realizing the connection between the virtual instrument and the hardware used to connect it to the rectifier power circuit.

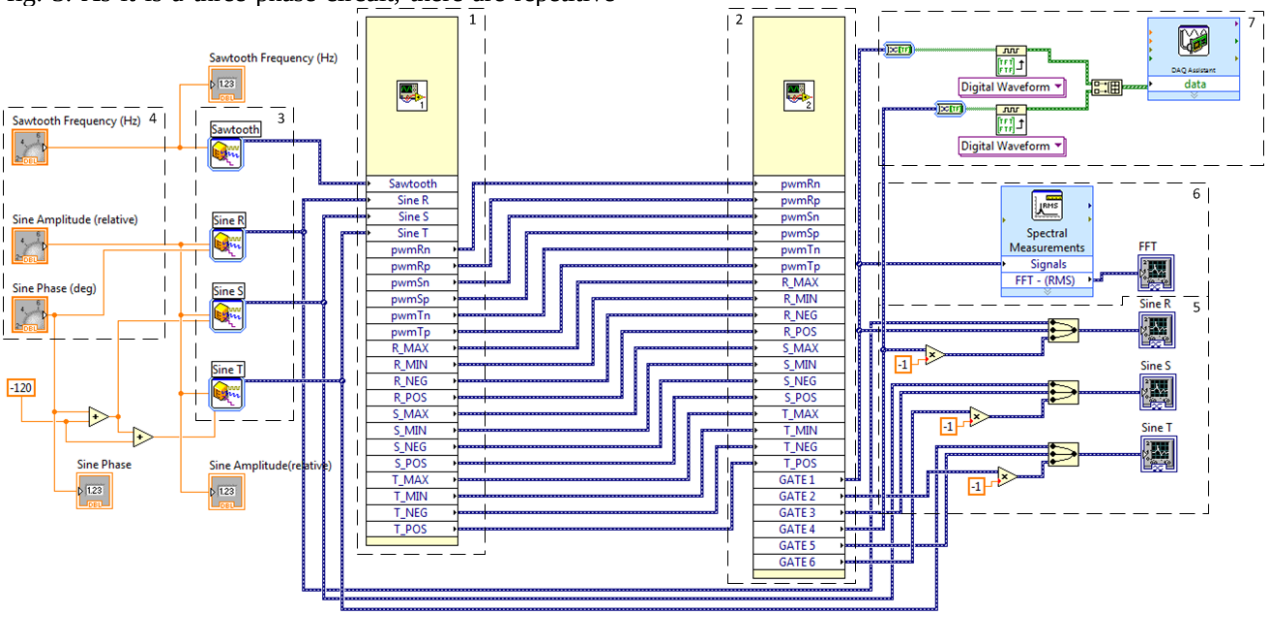

Fig. 3. Block Diagram of the Virtual Instrument.

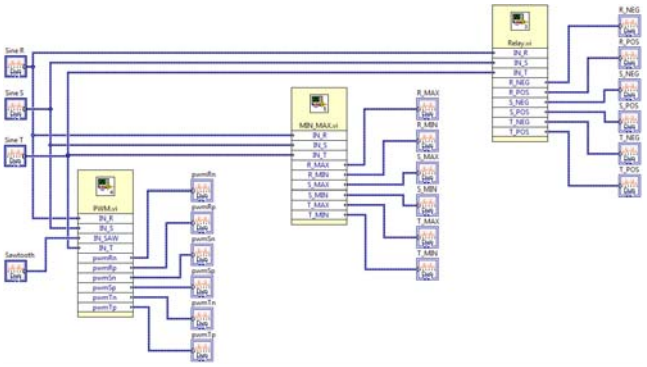

Fig. 4. Structure of the signal generation block.

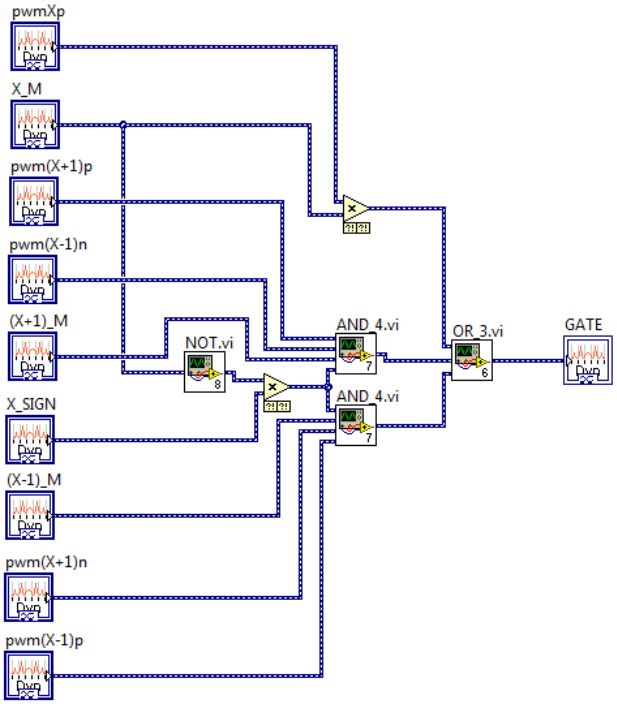

Fig. 5. Logic forming the gate PWM control sequences.

III. Experimental Results

Experimental examinations of the developed virtual instrument are conducted using CDAQ frame NI9178 and programmable TTL input-output module NI9401. The control PWM sequences generated by the virtual instrument are observed with oscilloscope. They can be applied to a controllable rectifier via appropriate driver stages.

Fig. 7 and fig. 8 present the experimentally obtained waveforms of the gate signals *G1* and *G4*, respectively for transistors *VS1* and *VS4*. These waveforms prove one of the main advantages of the control algorithm – the switches operate during the whole time interval of the half period, which leads to consumption of currents in phase with the grid voltages.

IV. Comparison in Operation Between the LabVIEW and the MATLAB Simulink Model of the Rectifier

A comparative analysis of the two software models of the three-phase BUCK rectifier with sinusoidal PWM shows identical operation results for both of the models, which confirms the correctness of the developed LabVIEW instrument. The Front Panel of the virtual instrument can be supplemented with additional graphical indicators illustrating typical parts of the control algorithm and information analogical to the one presented in [7], which may enable the use of the virtual instrument for investigation and teaching purposes.

An advantage of the developed virtual instrument compared to the MATLAB Simulink model of the rectifier and its control unit is the ability to vary some of the operating parameters in real time via the graphical knobs from the Front Panel.

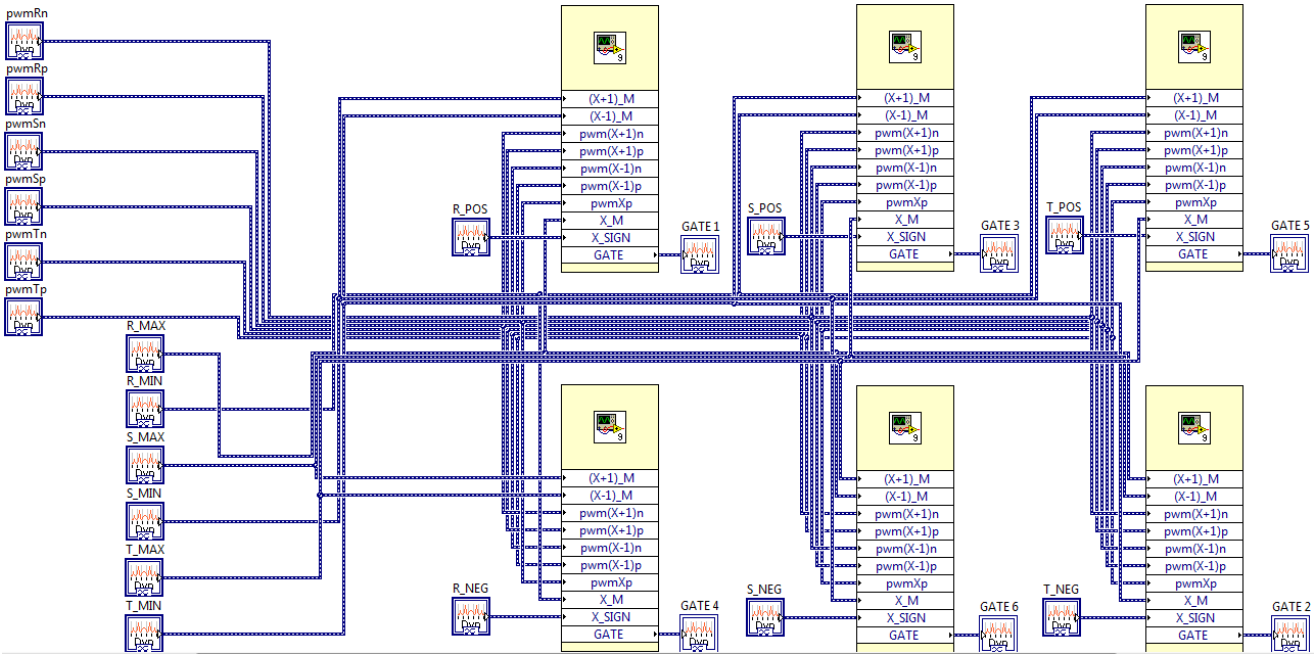

Fig. 6. Structure of the signal distribution block.

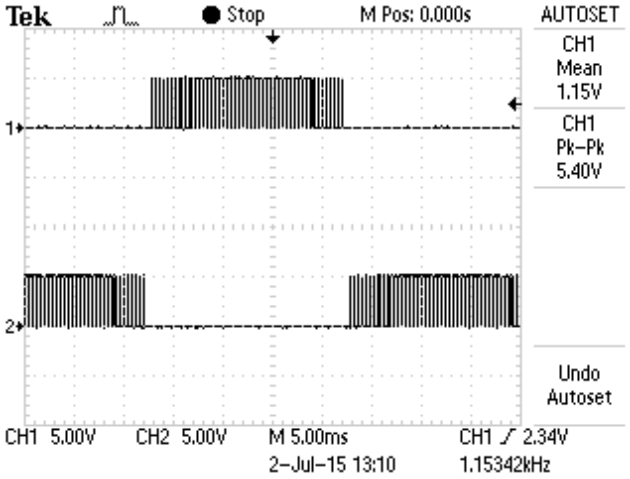

Fig. 7. Waveforms of the gate signals *G1* and *G4*.

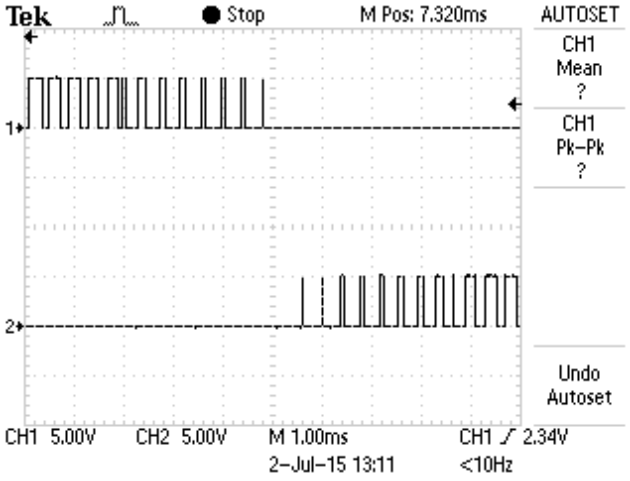

Fig. 8. Waveforms of the gate signals *G1* and *G4*.

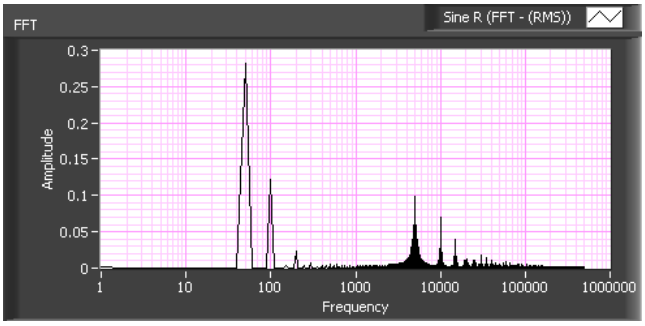

Fig. 9. Results from FFT analysis of signal *G1* (LabVIEW).

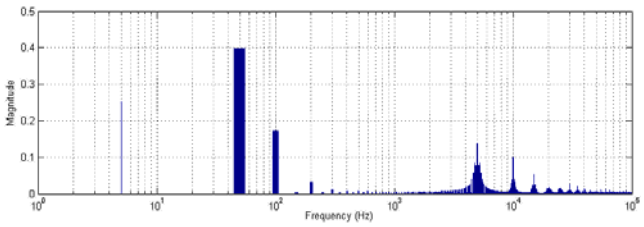

Fig. 10. Results from FFT analysis of signal *G1* (MATLAB).

Fig. 9 and fig. 10 illustrate the spectral composition of the gate PWM sequence generated for transistor VS1 (G1), respectively in the LabVIEW virtual instrument and in the MATLAB Simulink model. The results obtained from the operation of the developed in LabVIEW virtual instrument match those obtained from the MATLAB Simulink model. The spectral compositions of the rectifier input currents differ from the results of the FFT analysis as the control PWM sequences are unipolar signals, which results in presence of even numbered harmonic components in their compositions.

V. CONCLUSION

The developed virtual instrument can be used for control and examination of the characteristics of three-phase bridge rectifiers with sinusoidal PWM. It can be used for realization of asynchronous rectifier control unit. The virtual instrument consists of modules realized as separate functional subunits (*subVI*). This allows variations in the operation principles of the virtual instrument and, thus, realization of different modifications of the control algorithm.

As a result from the operation of the virtual instrument, the Front Panel displays the waveforms of the grid voltages and the gate signals in an appropriate way for illustration of the input currents. These waveforms and the results from the FFT analysis of the gate signals provide the PFC features of the circuit with the presented control algorithm to be well comprehended.

The conducted analyses confirmed the limitations for the values of maximum allowed modulation depth and step of output voltage control imported by the parameters of the used hardware.

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An Analysis of a Bidirectional Series Resonant DC/DC Converter

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Abstract – **A bidirectional series resonant DC/DC converter operating at frequencies higher than the resonant frequency is examined. It consists of two identical bridge commutation circuits whereby a phase-shift control is achieved. An analysis of the processes in the converter with the impact of only the first harmonic is carried out. The condition that defines the border between the two typical operating modes is established. As a result of the analysis, expressions for basic parameters of the converter are obtained and both output and control characteristics are drawn.**

Keywords – **Series Resonant DC/DC Converter, Controlled Rectifier**

I. Introduction

For years, series resonant DC/DC converters operating at frequencies higher than the resonant frequency have been widely used for the realization of different power supply devices. This is due to their inherent advantages, the most significant of which are small size and weight, natural short circuit protection and so on. Last but not least, these converters operate at low switching losses due to the real opportunity the power switches to commutate when the voltage applied on them has a value of zero (ZVS – Zero Voltage Switching).

In order to control the output power of the series resonant converters, two groups of methods are applied [1] – at variable and at constant frequency. Most of these methods are realized by the means of the inverter, which assumes uncontrolled rectifiers to be put in the converter structure.

Such a decision, however, does not support energy return to the power supply, which is indispensable for a number of applications. A solution to the problem is the use of controlled rectifier [1] – [3]. Such circuits for phase-shift control of series resonant DC/DC converters have long been known and investigated [4] – [6]. With these circuits, the output power varies practically from zero to the maximum value. In this case, however, the used rectifier is asymmetric, which does not provide energy return back to the power supply source.

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For investigation of series resonant DC/DC converters, a number of authors [5, 6] apply harmonic analysis taking into consideration only the influence of the first harmonic. The results obtained by this method are to a significant extent appropriate for engineering calculations.

A purpose of the present work is the examination of a bidirectional series resonant DC/DC converter with harmonic analysis with the impact of only the first harmonic. As a result of the analysis, expressions for basic parameters of the converter must be obtained and both its output and control characteristics must be drawn.

II. Principle of the Converter Operation

The scheme of the examined bidirectional converter is presented in fig.1. It consists of two similar bridge switching circuits, a resonant tank circuit (L, C), matching transformer Tr, capacitive input and output filters (C_F and C_0) and load resistor (R_0). Likewise the conventional series resonant DC/DC converter, the first switching circuit (transistors $Q_1 – Q_4$ with reverse diodes $D_1 – D_4$) interprets the function of an inverter, and the second one (transistors $Q_5 – Q_8$ with reverse diodes $D_5 – D_8$) respectively – the function of a rectifier. In the scheme, the required for ZVS mode snubber capacitors are not shown.

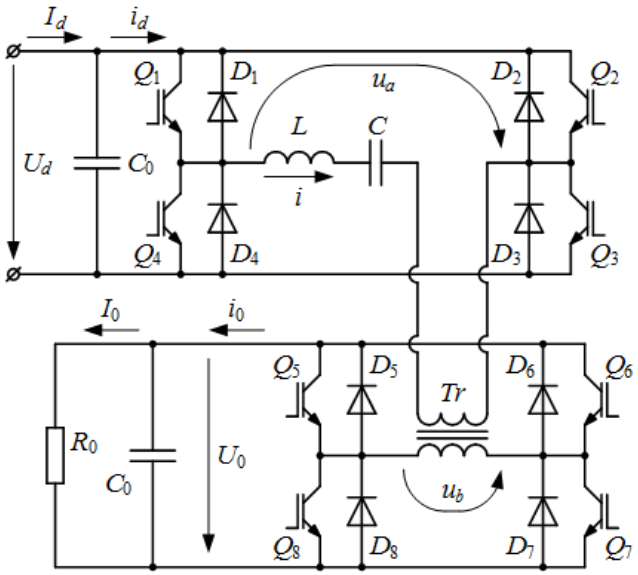


Fig. 1. Scheme of the bidirectional resonant DC/DC converter

The operation of the converter is illustrated by the waveforms, presented in fig.2. In this case, however, in order to control the output power, a different from the suggested in [4] – [6] strategy is applied.

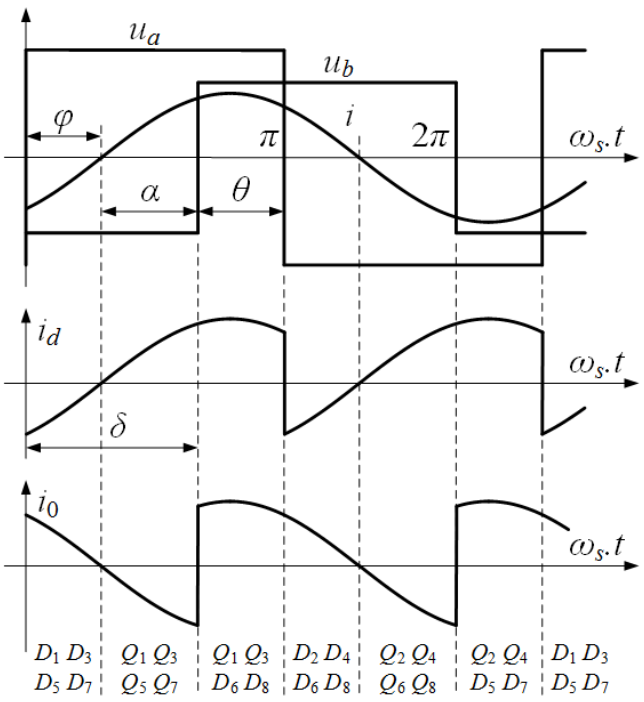


Fig. 2. Waveforms of the basic voltages and currents

The converter operates at constant frequency higher than that of the resonant circuit. Therefore, the inverter transistor couples (Q_1, Q_3 or Q_2, Q_4) switch at ZVS. They are controlled in a way that the voltage u_a at the inverter output has almost rectangular shape. The resonant current i falls behind the voltage u_a at angle φ. The rectifier transistors operate at ZVS also. Therefore, with the current i pass by zero, the respective couple (Q_5, Q_7 or Q_6, Q_8) starts to conduct. This couple is switched off after time corresponding to the angle δ after the turn-off of the inverter conducting transistors for the same half period. The voltage u_b at the input of the rectifier, the shape of which is similar to the one of u_a, changes its direction when the rectifier transistors are switched off. In this way, the control of the output power is obtained by the variation of the angle δ.

III. Analysis of the Converter Operation

The examination of the converter is carried out with harmonic analysis with the impact of only the first harmonic taken into account. The obtained results are suitable for engineering calculations.

For the purposes of the analysis, the following assumptions are made: the matching transformer is ideal with a transformation ratio k, all the circuit elements are ideal, the influence of the snubber capacitors and the pulsation of the supply voltage U_d and the output voltage U_0 are neglected, i.e. the voltages u_a and u_b have rectangular shape.

The analysis of the waveforms in fig.2 shows the possible energy transfer modes – from the power supply source to the load and back.

In accordance with the assumptions made, when the conduction time of the inverter reverse diodes D_1, D_3 (respectively D_2, D_4) is more than that of the transistors Q_1, Q_3 (respectively Q_2, Q_4), the energy transferred back to the power supply source is more than the consumed one, so that the average value of the current I_d is negative. This happens when $\varphi > \pi/2$.

Because of the rectifier diodes operation, the output voltage U0 cannot change its sign. Therefore, the energy transferred back from the load is more than the consumed for the rectifier when $\alpha > \pi/2$ or when the average value of the current I_0 becomes negative. This means that the rectifier transistors Q_5, Q_7 (respectively Q_6, Q_8) must conduct longer than its diodes D_5, D_7 (respectively D_6, D_8).

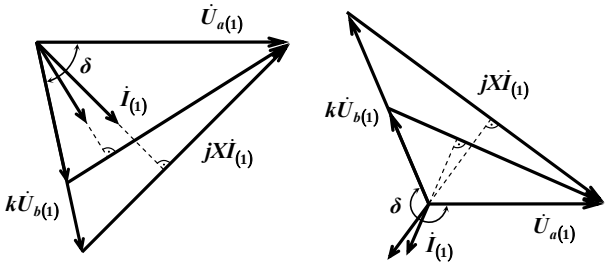
Considering the above mentioned and taking into consideration that $\delta = \alpha + \varphi$, energy transfer back to the supply source is possible when $\delta > \pi$.

On the basis of the assumptions made, the following symbols are introduced:

$\omega_0 = 1/\sqrt{LC}$ and $\rho_0 = \sqrt{L/C}$ – resonant frequency and characteristic impedance of the resonant tank circuit (L, C);

$\nu = \omega_s/\omega_0$ – frequency detuning of the resonant circuit, where ω_s is the inverter operating frequency.

In accordance with the chosen method of analysis, it is assumed that only the first harmonics of the current i and the voltages u_a and u_b have impact in the examined circuit. This gives the opportunity the processes in the converter to be illustrated with vector charts. The first operation mode when $0 \le \delta \le \pi$ and the energy is transferred to the load is illustrated in fig.3a. The second mode when $\pi \le \delta \le 2\pi$ and the energy is transferred back from the load is illustrated with the vector chart in fig.3b.



a) b)

Fig. 3. Vector diagrams of the basic voltages and currents

The following equation is valid for the examined circuit in standing mode:

$$\dot{U}_{a(1)} = k\dot{U}_{b(1)} + jX\dot{I}_{(1)} \tag{1}$$

where $\dot{U}_{a(1)}$, $\dot{U}_{b(1)}$ and $\dot{I}_{(1)}$ are the first harmonic complexes of u_a, u_b and i, and

$$X = \omega_S L - \frac{1}{\omega_S C} = \left(\nu - \frac{1}{\nu}\right)\rho_0$$

According to the assumptions made, the average value of the output current is defined as:

$$I_0 = \frac{1}{\pi}\int_0^{\pi} \sqrt{2} k I_{(1)} \sin(\omega t + \alpha) d\omega t = \\ = \frac{2\sqrt{2}}{\pi} k I_{(1)} \cos\alpha \tag{2}$$

from where for the effective value of the first harmonic of the resonant current is derived that:

$$I_{(1)} = \frac{\pi}{2\sqrt{2}} \cdot \frac{I_0}{k\cos\alpha} \tag{3}$$

In the first case when $0 \le \alpha \le \pi/2$, the following expressions are valid for the complex values $\dot{U}_{a(1)}$, $\dot{U}_{b(1)}$ and $jX\dot{I}_{(1)}$:

$$\begin{aligned} \dot{U}_{a(1)} &= \frac{2\sqrt{2}}{\pi} U_d \\ \dot{U}_{b(1)} &= \frac{2\sqrt{2}}{\pi} U_0 \cdot e^{-j\delta} \\ jX\dot{I}_{(1)} &= \frac{\pi}{2\sqrt{2}} \cdot \frac{I_0}{k\cos\alpha} \cdot \frac{\nu^2 - 1}{\nu/\rho_0} \cdot e^{j(\pi/2-\varphi)} \end{aligned} \tag{4}$$

In the second case when $\pi/2 \le \alpha \le \pi$, the expressions for the complex values $\dot{U}_{a(1)}$, $\dot{U}_{b(1)}$ and $jX\dot{I}_{(1)}$:

$$\begin{aligned} \dot{U}_{a(1)} &= \frac{2\sqrt{2}}{\pi} U_d \\ \dot{U}_{b(1)} &= \frac{2\sqrt{2}}{\pi} U_0 \cdot e^{j(2\pi-\delta)} = \frac{2\sqrt{2}}{\pi} U_0 \cdot e^{-j\delta} \\ jX\dot{I}_{(1)} &= \frac{\pi}{2\sqrt{2}} \cdot \frac{I_0}{k\cos\alpha} \cdot \frac{\nu^2 - 1}{\nu/\rho_0} \cdot e^{j(\pi/2-\varphi)} \end{aligned} \tag{5}$$

From expressions (4) and (5) it is observed that independently from the interval of variation of the control angle δ, equation (1) assumes the same description:

$$\begin{aligned} &\frac{2\sqrt{2}}{\pi} U_d = \frac{2\sqrt{2}}{\pi} k U_0 \cdot e^{-j\delta} + \\ &+ \frac{\pi}{2\sqrt{2}} \cdot \frac{I_0}{k\cos\alpha} \cdot \frac{\nu^2 - 1}{\nu/\rho_0} \cdot e^{j(\pi/2-\varphi)} \end{aligned} \tag{6}$$

In order to obtain generalized results, the magnitudes output voltage U_0' and output current I_0' are introduced in relative units:

$$U_0' = kU_0/U_d \text{ and } I_0' = \frac{I_0/k}{U_d/\rho_0} \tag{7}$$

Then from equation (6) the following normalized expression is obtained:

$$\begin{aligned} &1 = U_0'\cos\delta - jU_0'\sin\delta + \\ &+ \frac{\pi^2}{8} \cdot \frac{\nu^2 - 1}{\nu} \cdot \frac{I_0'}{\cos\alpha} \cdot \cos(\pi/2 - \varphi) + \\ &+ j\frac{\pi^2}{8} \cdot \frac{\nu^2 - 1}{\nu} \cdot \frac{I_0'}{\cos\alpha} \cdot \sin(\pi/2 - \varphi) \end{aligned} \tag{8}$$

As the imaginary part of the above expression equals zero, it is obtained that:

$$U_0'\sin\delta = \frac{\pi^2(\nu^2 - 1)}{8\nu} \cdot \frac{I_0'}{\cos\alpha} \cdot \cos\varphi \tag{9}$$

From the vector charts presented in fig.3 it is observed that:

$$U_{a(1)}\cos\varphi = kU_{b(1)}\cos\alpha \tag{10}$$

and therefore:

$$\cos\varphi = U_0'\cos\alpha \tag{11}$$

On the basis of the expressions (9) и (11), the final expression is obtained as follows:

$$I_0' = \frac{\sin\delta}{c} \tag{12}$$

where: $c = \frac{\pi^2}{8}(\nu - 1/\nu)$

From the real part of equation (8) and taking (12) into consideration, it is derived that:

$$U_0' = \frac{1 - \frac{\sin\varphi}{\sin\alpha}\sin\delta}{\cos\delta} \tag{14}$$

The above expression allows the boundaries of the ZVS operating mode to be obtained for the transistors of the inverter (at $\varphi = 0$ and $\varphi = \pi$) and the rectifier (at $\alpha = 0$ and $\alpha = \pi$) respectively.

It is easy to seed that these boundaries are meaningful at two cases when control angle is changing in range $0 \le \delta \le \pi/2$ or $3\pi/2 \le \delta \le 2\pi$ respectively. For $\pi/2 \le \delta \le 3\pi/2$ the transistors in both the rectifier and the inverter operate at ZVS.

IV. Output and Control Characteristics

A full enough picture of the examined series resonant DC/DC converter features can be obtained via analysis of its graphically illustrated normalized characteristics drawn for a value of the transformation ratio equal to one ($k = 1$).

Thus, on the basis of equation (12), the normalized dependencies of the output voltage U_0 from the output current I_0 are obtained when the converter operates at a constant frequency ($\nu = 1{,}15$). As mentioned above, according to the control angle are two possible cases. For first one at δ = -π/2; -2π/5; -3π/10; -π/5; -π/10; π/10; π/5; 3π/10; 4π/5; π/2 such dependencies are presented on fig.4.

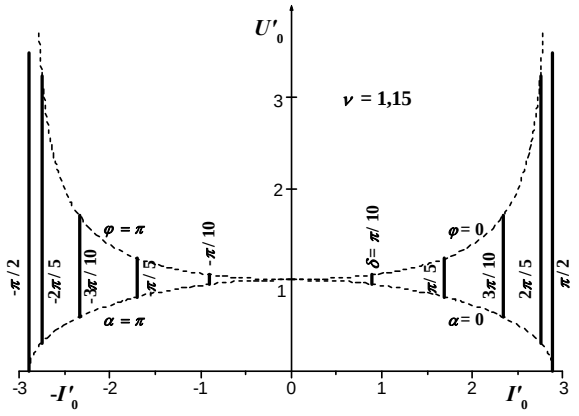


Fig. 4. Output characteristics at -$\pi/2 \le \delta \le \pi/2$

The output characteristics are presented with thick lines. The ones situated in the first quadrant for $0 \le \delta \le \pi/2$ correspond to the mode of energy transfer to the load, and the others in the second quadrant for $-\pi/2 \le \delta \le 0$ – to the mode of energy return back to the power source respectively. In the area of the output characteristics, the boundaries of ZVS mode are shown with dotted line for inverter's transistors (at $\varphi = 0$ and $\varphi = \pi$) and for rectifier's transistors (at $\alpha = 0$ and $\alpha = \pi$) respectively. The analysis of the dependencies presented in fig.4 shows that in this case the converter operation is very limited and practically no-load mode is not possible.

For control angle $\delta = \pi/2; 3\pi/5; 7\pi/10; 4\pi/5; 9\pi/10; \pi; 11\pi/10; 6\pi/5; 13\pi/10; 7\pi/5; 3\pi/2$ normalized dependencies of the output voltage U_0 from the output current I_0 are shown in fig.5.

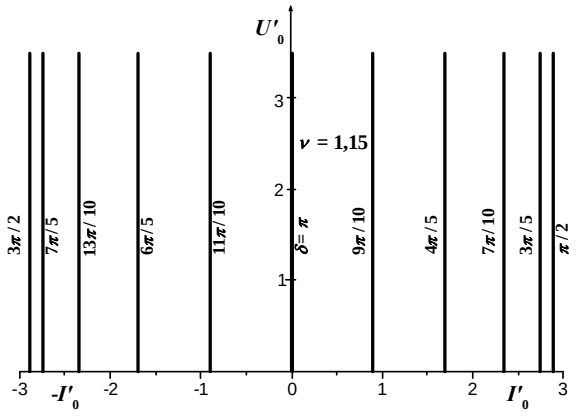


Fig. 5. Output characteristics at $\pi/2 \le \delta \le 3\pi/2$

The output characteristics are presented with thick lines again. The ones situated in the first quadrant for $\pi/2 \le \delta \le \pi$ correspond to the mode of energy transfer to the load, and the others in the second quadrant for $\pi \le \delta \le 3\pi/2$ – to the mode of energy return back to the power source respectively. The ordinate appears to be the boundary between the two modes. Referring to it, the characteristics for the equally distanced from π control angles are situated symmetrically.

The analysis of the output characteristics shows that independently from the control angle value the converter behaves such as an ideal current source.

Normalized control characteristics for the output current I_0 as a function of the control angle δ are presented in fig.6. They are drawn on the basis of equation (12) when the converter operates at several different values of the frequency detuning $\nu = 1{,}08; 1{,}10; 1{,}15; 1{,}20; 1{,}30$.

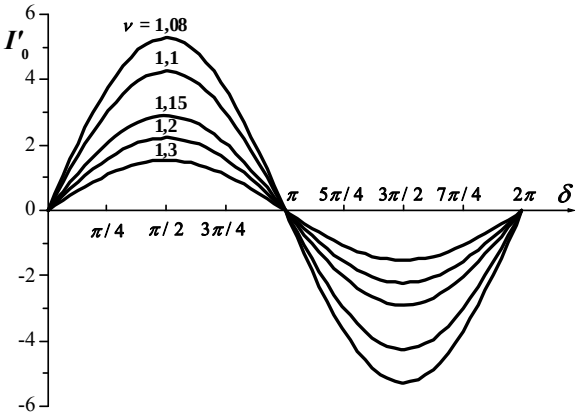


Fig. 6. Control characteristics of the converter

In this case, the abscissa appears to be the boundary between the two modes of energy transfer.

Fig. 6 shows that independently from the value of the operating frequency these characteristics have two extreme values. The output current gains same values for these points.

Obviously, from the point of view of the converter output power control, the most appropriate interval of variation of the angle δ is the one limited by the two extreme values. Moreover, the control characteristics can be assumed as linear for a comparatively wide range.

V. CONCLUSION

A bidirectional resonant DC/DC converter operating over the resonant frequency with phase-shift control of the output power is examined. A theoretical examination of the converter is carried out on the basis of harmonic analysis with taking into consideration only the impact of the first harmonic. As a result, dependencies for the basic parameters of the converter are obtained and its output and control characteristics are drawn. The control intervals are determined for the two energy transfer modes – to the load and back to the power supply source. The boundary conditions for the power switch area of commutation at zero voltage are defined. Several specialties in the converter output power control are discussed. The most suitable interval of variation of the control angle is pointed.

The presented output and control characteristics show that the examined resonant DC/DC converter is bidirectional only by means of current as its output voltage cannot change its sign. Furthermore, the change of the energy transfer direction is unambiguously determined by the control angle. Moreover, the converter behaves such as an ideal current source for both modes.

The obtained analytical results can be used for design of this and similar resonant DC-DC converters.

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Buck ZVS DC-DC Quasi-Resonant Converter: Design, Modeling, Simulation and Experimentation

Nikolay Lyuboslavov Hinov and Nikolay Rangelov Rangelov

Abstract – **In the paper work a experimental study has been made with practical trend, of a Buck DC – DC quasi resonant converter, working with ZVS (Zero Voltage Switching). In the work a mathematical expressions, for the parameters, which describe the work of the power part of the circuit, has been made. With their help a method for designing of a Buck ZVS DC – DC quasi resonant converter has been proposed. The advantage of this method is the use of simple expressions, which facilitate the designing, but in the same time an acceptable error of 10 % is kept, commensurate with the tolerance of the values of the reactive elements (capacitor and inductor). The verification of these expressions has been made with modeling (Matlab/Simulink), computer simulations (LTSpice) and experimental measurements on a laboratory stand.**

Keywords – **Zero voltage switching, DC-DC power converters, Soft-switching, Modeling, Simulation.**

I. INTRODUCTION

One of the main methods for increasing the efficiency of converters of electrical energy is the decreasing of the switching loses in the power semiconductor elements [9, 10, 11]. Therefore a widely used method for achieving this is the using of a soft switching – shift switching of the power elements on zero voltage or zero current. For some converters this is achieved by virtue of circuit features (for example resonant inverters), and for others by using of a additional elements (capacitor or inductor), which are connected parallel or serial to the semiconductor switch. [2, 4, 5]. Thus parallel or serial resonant circuits can be made. These circuits are well known in the literature with the name quasi resonant converters. In this paper work a study of a Buck ZVS quasi resonant converter has been made. The analysis of these converters are in [4, 5, 13], but there are some inaccuracies and incorrectly identified values, and in addition these analyses are not useable for designing, which is one of the purposes of this work.

II. DESIGN-ORIENTED ANALYSIS OF BUCK ZVS QUASI-RESONANT CONVERTER

On figure 1 is shown the circuit of a Buck ZVS quasi resonant DC-DC converter. The circuit consist of transistor SW, diode D, filter elements L and C, Load R_L resonant elements L_r и C_r, which provide the zero voltage switching.

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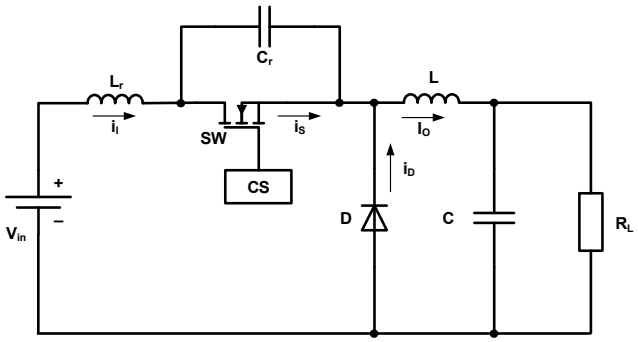

Fig. 1. Circuit of a Buck ZVS converter

The analyze is made under steady state and assumption that all element are perfect. The circuit is working in continuous conduction mode with negligible ripples through the filter inductor. Due to the resonant circuit C_r-L_r for the analysis of the converter some specific ratios are used [4, 5, 9]:

- Resonant frequency of the serial L_r-C_r circuit for ideal elements:

$$\omega_0 = \frac{1}{\sqrt{L_r C_r}} \tag{1}$$

- Ratio between control frequency and the frequency of the resonant circuit:

$$\nu = \frac{f_s}{f_0} \tag{2}$$

- Characteristic impedance of the resonant circle:

$$Z_0 = \sqrt{\frac{L_r}{C_r}} = \omega_0 L_r = \frac{1}{\omega_0 C_r} \tag{3}$$

- Normalized load resistance:

$$R' = \frac{R_L}{Z_0} = \frac{R_L}{\omega_0 L_r} = \omega_0 C_r R_L = \frac{\nu R_L}{\omega_S L_r} = \frac{\omega_S C_r R_L}{\nu} \tag{4}$$

- Ratio between output and input voltage of the converter (DC voltage transfer function):

$$M_{VDC} = \frac{V_O}{V_I} \tag{5}$$

- Normalized initial resonant inductor and switch current when the switch turns on:

$$h = \frac{i_{L_r}(0)}{I_O} = \frac{i_{L_r}(0)}{I_O} \tag{6}$$

- Duty ratio:

$$D = \frac{t_{on}}{T} \tag{7}$$

The work of the studied circuit is shown by the waveforms on figure 2 (when the value of h=0). During one period we can see four different working stages:

Stage 1 ($0 < T \le t_1$) – The resonant inductor accumulate energy. The switch and the diode are turned on. During this

stage currents and voltages have the following conditions: $V_S = 0$, $I_L = 0$, $I_C = 0$, $V_{LR} = V_I$, and the current through the switching inductor is:

$$i_{L_r} = \frac{1}{\omega_S L_r}\int_0^{\omega_S t} V_{L_r} d(\omega_S t) + i_{L_r}(0) = \frac{V_I}{\omega_S L_r}\omega_S t + i_S(0) \quad (8)$$

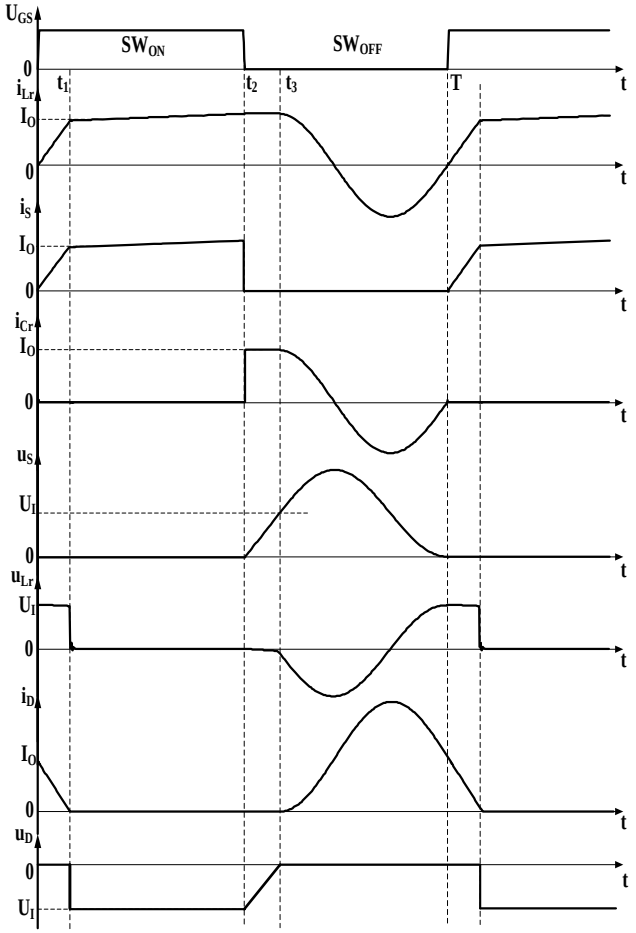

Fig. 2. Time waveforms when the converter is working.

For the purpose of the study it is conveniently to obtain expressions in relative units, using the expressions mentioned above in the paper work. Thus the current through the inductor L_r is:

$$\frac{i_{L_r}(\omega_s t)}{I_O} = \frac{i_s(\omega_s t)}{I_O} = \frac{R'}{\nu M_{VDC}}\omega_s t + h \quad (9)$$

The relationship between the current through the diode i_D, and the current through the switch i_S in the circuit is:

$$i_D = I_O - i_S = I_O\,(1 - i_s/I_O) \quad (10)$$

So for the current through the diode, in relative units:

$$\frac{i_D(\omega_s t)}{I_O} = 1 - \frac{R'}{\nu M_{VDC}}\omega_S t - h \quad (11)$$

This stage ends when the current trough the diode becomes zero.

Stage 2 ($t_1 < t \le t_2$) – the diode is turned off. During this stage the following terms are executed: $V_S = 0$, $I_{CR} = 0$, $I_D = 0$, $i_S = i_{LR} = I_O$, $V_{LR} = 0$, и $V_D = V_I$. This stage ends in the moment when the transistor turns off from the control system.

Stage 3 ($t_2 < T \le t_3$) – charging of the resonant capacitor and both diode and the transistor are turned off. During this stage the following terms are in effect: $i_S = 0$, $I_D = 0$, $I_{LR} = I_{CR} = I_O$, $V_{LR} = 0$. The voltage over the capacitor is determined with the following expression:

$$v_S = v_{C_r} = \frac{1}{\omega_S C_r}\int_{2\pi D}^{\omega_S t} i_{C_r} d(\omega_S t) + v_{C_r}(\omega_S t_2) = \quad (12)$$

$$= \frac{I_O}{\omega_S C_r}(\omega_S t - 2\pi D) = \frac{V_0}{\omega_S C_r R_L}(\omega_S t - 2\pi D)$$

Where $V_{C_r}(\omega_s t_2) = 0$.

After transformation for the voltage over the transistor and the diode, in relative units is:

$$\frac{v_S}{V_I} = \frac{M_{VDC}}{\nu R'}(\omega_S t - 2\pi D)$$
$$\frac{v_D}{V_I} = \frac{M_{VDC}}{\nu R'}(\omega_S t - 2\pi D) - 1 \quad (13)$$

This ends when the voltage over the diode becomes zero - $v_D(\omega st_3) = 0$. From this term we get the expression:

$$\omega_S t_3 = 2\pi D + \frac{\nu R'}{M_{VDC}} \quad (14)$$

Stage 4 ($t_3 < t \le T$) – in its beginning the diode turns on. By the made assumptions for perfect elements in the circuit starts a serial resonant process with the following initial conditions: $I_{LR}(\omega_s t_3) = I_O$ и $v_{Cr}(\omega_s t_3) = V_S(\omega_s t_3) = V_I$.

Determine the current in the resonant circuit can be made with different methods [4, 5, 9, 13], and in relative units it is:

$$\frac{i_{L_r}}{I_O} = \frac{i_{C_r}}{I_O} = \cos\frac{\omega_S t - \omega_S t_3}{A} \quad (15)$$

From (15) and (10) the relative current through the diode is:

$$\frac{i_D}{I_O} = 1 - \cos\frac{\omega_S t - \omega_S t_3}{\nu} \quad (16)$$

At working in steady mode the following condition is executed:

$$i_{L_r}(2\pi) = i_{L_r}(0) = hI_O \quad (17)$$

From it is applying in (15) and by using of (14) we determine:

$$cos\left[\frac{2\pi(1-D)}{\nu} - \frac{R'}{M_{VDC}}\right] = h \quad (18)$$

The voltage over the resonant inductor, during stage 3 is:

$$V_{L_r} = \omega_S L_r \frac{di_{L_r}}{d(\omega_S t)} = -\frac{M_{VDC} V_I}{R'} sin\frac{\omega_S t - \omega_S t_3}{\nu} \quad (19)$$

The voltage over the switch is:

$$V_S = V_{C_r} = \frac{1}{\omega_S C_r}\int_{\omega_S t_3}^{\omega_S t} i_{C_r} d(\omega_S t) + v_{C_r}(\omega_S t_3) = \quad (20)$$

$$= \frac{V_I M_{VDC}}{R'} sin\frac{\omega_S t - \omega_S t_3}{\nu} + V_I$$

In relative units is:

$$\frac{v_S}{V_I} = \frac{M_{VDC}}{R'} sin\frac{\omega_S t - \omega_S t_3}{\nu} + 1 \quad (21)$$

For achieving ZVS mode, the following condition must be fulfilled: $v_S(2\pi) = v_S(0) = 0$.

So the relation between the used factors is:

$$sin\left[\frac{2\pi(1-D)}{\nu} - \frac{R'}{M_{VDC}}\right] = -\frac{R'}{M_{VDC}} \quad (22)$$

After trigonometric transformations of (18) and (22) gets:

$$\frac{R'}{M_{VDC}} = \sqrt{1-h^2} \tag{23}$$

For the duty ration we get:

$$D = \frac{t_2}{T} = 1 - \frac{\nu}{2\pi}\left[2\pi + \sqrt{1-h^2} - arccosh\right] \tag{24}$$

For the purposes of the design it is necessary to determine the relation between duty ratio and the voltage transfer function at constant current. Initially the average value of the input current is determined:

$$I_I = \frac{1}{2\pi}\int_0^{2\pi D} i_s d(\omega_s t) = I_O\left[D - \frac{\nu(1-h)^2}{4\pi\sqrt{1-h^2}}\right] \tag{25}$$

By assuming for perfect elements and lack of losses in the circuit elements the following relation is in effect: $V_O I_O = V_I I_I$. From the definition for the voltage transfer function gets:

$$M_{VDC} = \frac{V_O}{V_I} = \frac{I_I}{I_O} = D - \frac{\nu(1-h)^2}{4\pi\sqrt{1-h^2}} \tag{26}$$

In [4, 5, 6, 9, 10] are examined and analyzed the impact of the initial conditions for current over the work of the converter, and the scope of the load resistance for ZVS work.

For simplification of the calculations it is recommended to choose the value h = 0. Moreover this mode is best from the point of view for the stress and use of the circuit elements [4, 5, 13].

III. Methodology for Designing

The main data necessary for designing a Buck ZVS converter are:

- Input voltage V_I;
- Output voltage V_O;
- Output current I_O;
- Ripple factor for output voltage and current;
- Control frequency f_S.

From the necessary data mentioned above we can see that these are the necessary values for calculating random converters (independently from its working mode – is it with zero switching or no). For first step it begins with calculating of the converter without resonant circuit (C_r - L_r, shown on figure 1) – standard Buck converter with hard switching. After that the values of the resonant elements must be determine. Because the main purpose is to suggest a simple and easy method for designing, a value of h=0 has been chosen. In this case a simplified kind of the expressions is received (23) (24) and (26):

$$R' = M_{VDC} \tag{28}$$

$$D = 1 - \frac{3\pi+2}{4\pi}\left(\frac{f_S}{f_O}\right) \approx 1 - 0.9092\left(\frac{f_S}{f_O}\right) \tag{29}$$

$$M_{VDC} = 1 - \frac{3\pi+3}{4\pi}\left(\frac{f_S}{f_O}\right) \approx 1 - 0.9887\left(\frac{f_S}{f_O}\right) \tag{30}$$

Except the reactive components a suitable semiconductor elements must be chosen. This is accomplishing by using the expressions for their maximum current and voltage stress. From the presented analyze the values for maximum current and voltage across the transistor is determined by:

$$I_{SM} = I_O \tag{31}$$

$$V_{SM} = \left(\frac{M_{VDC}}{R'} + 1\right)V_I \tag{32}$$

For the diode the maximum current and voltage stress are:

$$I_{DM} = 2I_O \tag{33}$$

$$V_{DM} = V_I \tag{34}$$

Of course the frequency parameters of the elements must be determined too during the design and the practical realization, because these circuits are working for high frequency. [4, 9, 10, 12].

IV. Example

The necessary data for designing is:

V_i = 30V; V_O=15V; I_O=200mA; f_S=100kHz and we choose to work with h = 0.

A conventional Buck DC – DC converter with hard switching is calculated, by one of the well-known design methods, like the ones in [1, 8, 9, 10]. From the designing we get the following results for the values of the elements: L = 200μH, C = 5μF и R_L=75Ω. An inductor with L = 250μH and a capacitor with C = 5.7μF are chosen. The values of these filter elements are determine so they can provide a work in continuous mode and set values for the output current and output voltage ripple.

After that the calculation of the resonant elements begins. From expression (28) follows that, M_{VDC}=R′=0.5. Z_0 is determine by (4) and its value is Z_0=75/0.5=150.

From (30) after we replace the determined till now parameters, the value for the resonant frequency of the serial resonant circuit is – f_0=197775Hz;

With the determined resonant frequency the value of the duty ratio D from (29) is 54.02%;

After that the resonant inductor must be determine from (4), its value is: L_r = 120.73μH;

The resonant capacitor C_r is calculated from (4) and it is: C_r=5.3656nF.

From the determined values we can see that the inductor and the capacitor, in the resonant circuit, are not with standard values. Because of the specificity of the offered elements (their values are in standard order), a using of a elements with standard values is required.

There are two possible methods for settle this task, like we can see from expression (29) and (30). If the values of the resonant capacitor and inductor are changed, the duty ratio must be changed too or the control frequency. So the values of the elements pointed out in the assignment are kept.

The easies way is to change the duty ratio (so the working frequency is kept, which lead to suppression of the electromagnetic interference). In this case a standard values for the resonant elements are set and with their new values, the frequency of the resonant circuit must be calculated again. So an inductor with L_r = 110μH and capacitor with C_r=6.8nF are chosen. After standard values are been used of L_r and C_r, they are replaced in (4), the new value of the resonant frequency is - f_0'= 186530Hz. Recalculation of the duty ratio must be done and the new value is - D'= 51.26%.

With these data and certain values the values of the

transistor should be bigger than U_{SM}=60V and I_{SM}=0.2A, and for the diode - U_{DM}=30V и I_{DM}=0.4A. Of course the elements should work with frequency bigger than 100 kHz.

V. Simulation Studies and Modeling

By the so determined values of the converter elements, simulation researches and modeling have been made with Matlab/Simulink and LTSpice.

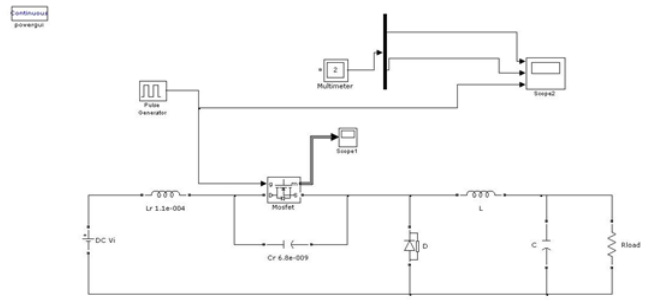

Fig. 3. Matlab/Simulink model of a BUCK ZVS quasi resonant DC-DC converter.

The purpose of the research is checking of the design method. On figure 3 is shown the model of the converter in Matlab/Simulink. On figure 4 the results of the modeling are shown (from up to down are current trough the transistor; voltage over the transistor and the control signal for the transistor).

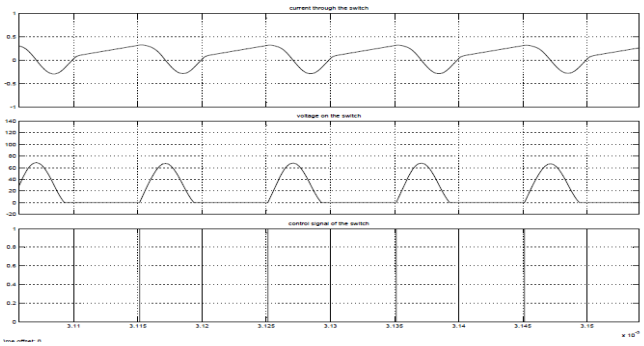

Fig. 4. Results from modeling a BUCK ZVS quasi resonant DC-DC converter with Matlab/Simulink.

On figure 5 is shown the circuit of the studied converter, which will be simulated in LTSpice. On figure 6 are shown the results of the simulation (from up to down are current through the resonant inductor; current through the transistor; voltage over the transistor and control signal for the transistor).

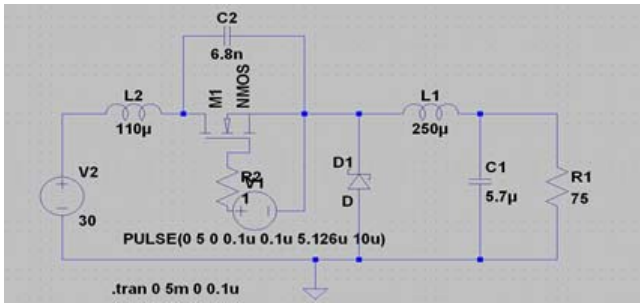

Fig. 5. Simulation model of a BUCK ZVS quasi resonant DC-DC converter in LTSpise

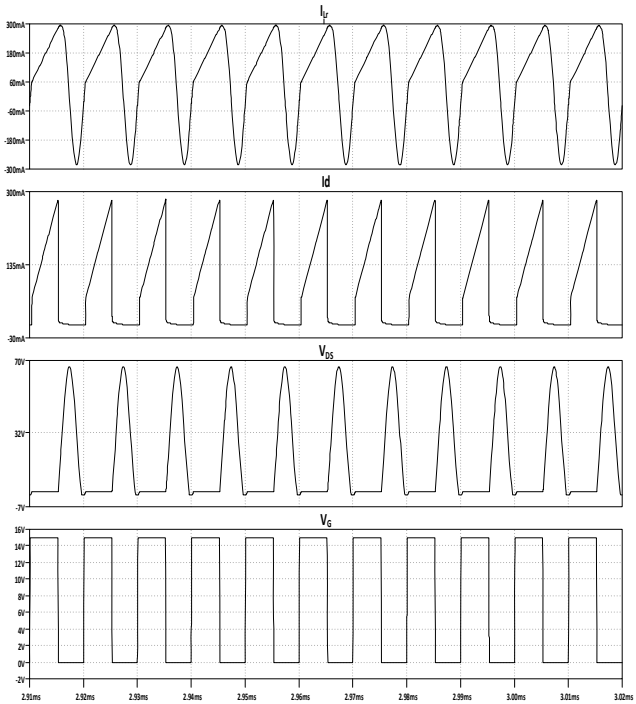

Fig. 6. Results from the simulation of a BUCK ZVS quasi resonant DC-DC converter with LTSpise.

From the two simulation studies we can see that the theoretical calculation and the correction, related to the change of the duty ratio, due to using switching elements with standard values, are confirmed. It is important to mention that the conditions for zero voltage switching are fulfilled.

VI. Experimental Researches

The experiments are made on an experimental stand, shown on figure 7. The software part of the control system is implemented with the software for visual programming LabView, and for the hardware part of the control system a chassis CompactDAQ is used with the connected modules to it NI9122 – 8 input ADC and NI9104 - 8 programmable TTL inputs/outputs.

This approach and allows us to achieve maximum flexibility in the testing of the DC-DC converter, in different operating modes.

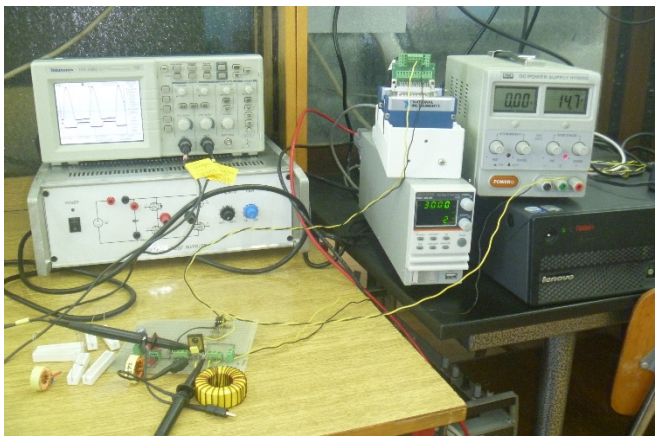

Fig. 7. Experimental stand

By LabView we can achieve a wide range of variations of the control frequency and the duty ratio, which is very comfortably for experimental studies. On figure 8 is shown the block diagram of the pulse generator.

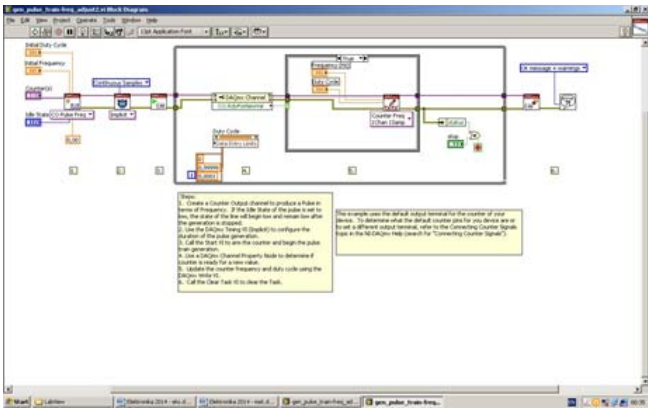

Fig. 8. Block diagram of the pulse generator

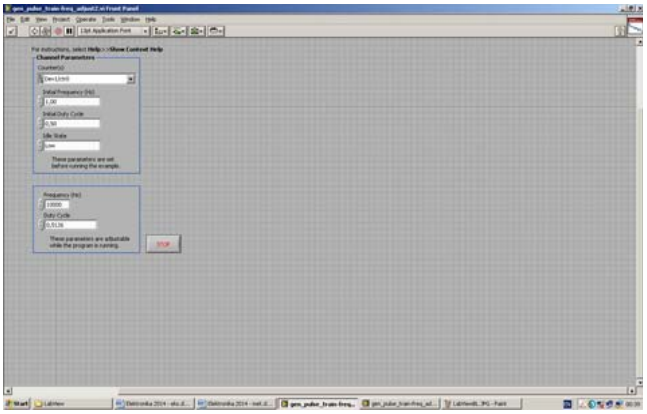

Fig. 9. Front panel of the pulse generator

On figure 9 is shown the front panel, from this panel we can change the frequency and the duty ratio of the virtual instrument. As we can see from the front panel it is very comfortable to set the parameters of the control pulse for the transistor and so we can achieve different working regimes of the converter.

For the realization of the power circuit the following elements are used: one MOSFET transistor model 6R165, high frequency diode model 60APU04, driver HCPL3120 with integrated optocoupler, resonant inductor with the following value of 110μH, resonant capacitor with the following value of 6.8nF, filter inductor with the following value of 250μH, filter capacitor with the following value of 5.7μF and load resistor with the following value of 75Ω. The circuit of the experimental stand of a ZVS Busk DC-DC converter is shown on figure 10.

The measurements are done with oscilloscope model Tektronix TDS1002. The voltages are measured with voltage scope with scale 10:1. The currents are measured with current scope.

On the following figures are shown the results from the measurements with the oscilloscope. On figure 11 are shown the voltage over the transistor and the control pulses. From the graphical results we can see that the zero voltage switching is achieved.

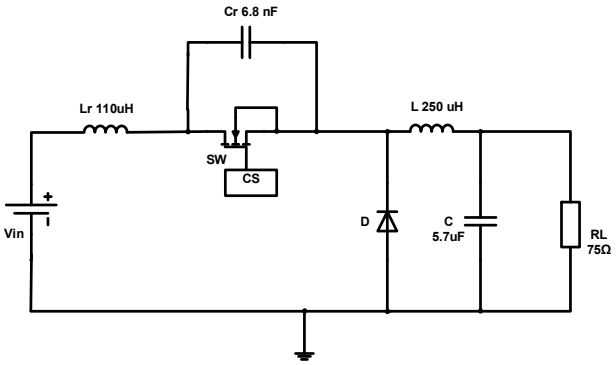

Fig. 10. Power circuit of the experimental stand.

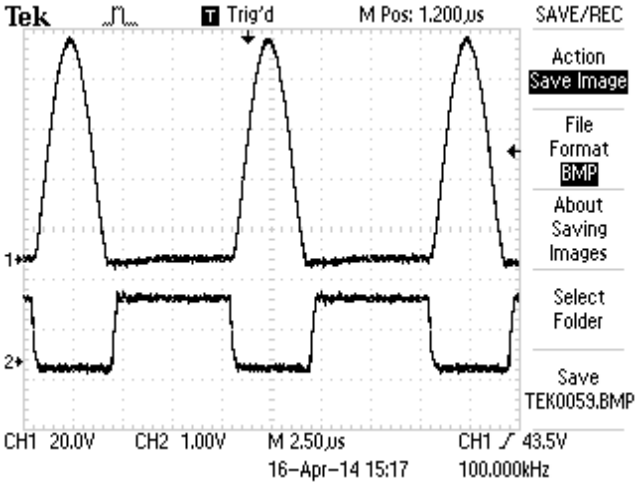

Fig. 11. Voltage across the transistor and control pulses.

On figure 12 are shown the current through the transistor and the voltage over it. As we can see when the transistor turns on we have zero voltage and current switching. These results show that the proposed method for designing is correct, because in the calculations we have accepted zero initial condition for the current. On figure 13 are shown the voltage over the switch and the current through the resonant inductor and on figure 14 the output voltage ripples. When working with control frequency of 100 kHz allows us the achieving of small ripples (196mV), when the output filter capacitor is with small value – 5,7μF [3, 12].

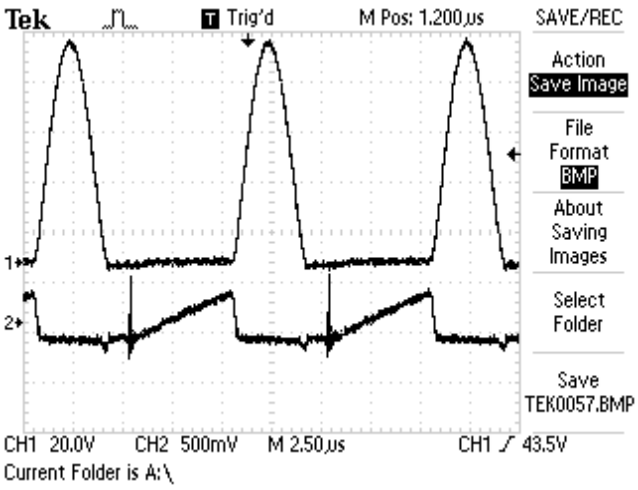

Fig. 12. Voltage over the transistor and the current through it.

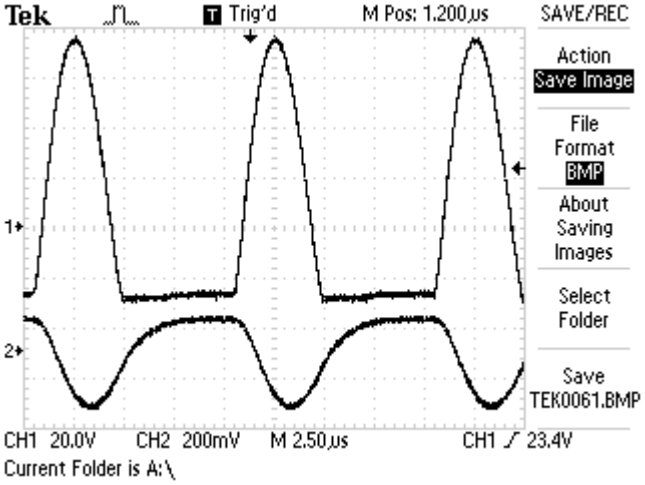

Fig. 13. Voltage over the transistor and over the resonant inductor.

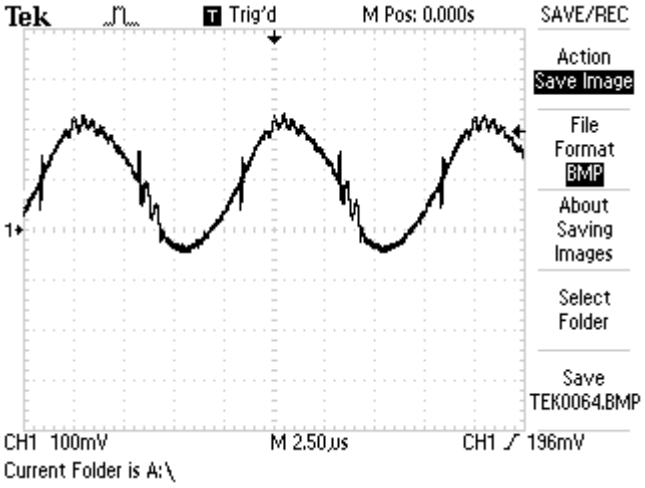

Fig. 14.Output voltage ripples.

VII. CONCLUSIONS

The made simulation and experimental researches of the Buck ZVS DC – DC converter check and confirmed the proposed, from the authors, design method. The main purpose in the article is finding a comfortable and easy expression for simple designing of converters, without using complicated calculations. In table 1 a comparison between calculations results, simulations, mathematical modeling and experiments is shown. As we can see there is a very good coincidence between them (difference between them no more than 10%), despite the assumptions and simplifications.

TABLE I. COMPARING OF THE RESULTS.

Parameters	LTSpice	Simulink	Experiments	Calculated/ Set
V_O (V)	14.65	14.85	14.78	15
I_O (mA)	198.98	198	197	200
ΔV_O (mV)	188	175.5	192	187.5
V_{SM} (V)	60.10	65.5	65	60
I_{DM} (mA)	409	396	394	400

On the other side it would be interesting achieving zero voltage switching with possible low value of the voltage over the transistor. The feature studies of the authors are directed in further optimizations of the design method, which will lead to easier way of choosing the elements of the resonant circuit. All this will lead to a little voltage stress of the power transistor.

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Driving System for Electric Vehicles: Modelling and Simulation

Vladimir Vladimirov Dimitrov and Peter Trifonov Goranov

Abstract – **The paper presents a system level overview of an electric vehicle power train. After a brief review of the available power train architectures, a particular one is constructed along with its control circuit, using popular simulation software. Finally, the results for typical driving cycles are plotted.**

Keywords – **Electric Vehicles, Bidirectional power converters, EV system level simulation**

I. Introduction

The ongoing strive for sustained transportation requires an increasing electrification in all its current technologies. This so called Transportation 2.0 parading, calls for continuously increasing investment in electrified transport [1]. However, to achieve such goals the design engineers must have a broader understanding of the key enabling technologies involved. To gain a better understanding of the factors involved to achieve the ever stringent design specification the designer must seek a system level overview of the whole vehicle.

The system level construction of pure electrical vehicle, which is the ultimate goal in a fully electrified transportation, allows the designer to look at different confronting issues that need to be addressed to achieve an optimum working design. The first step in such an endeavor usually involves the construction of a full system model with varying levels of detail for the different components. The results obtained for the system behavior allows the identification of some of the possible optimizations and design faults in the different subsystems, which than can be independently solved during their detailed design. The system level simulation of a pure electric vehicle is the primary topic in this paper.

The paper is organized as follows: section 2 presents a brief literature overview and comparison of the available power train architectures, concentrating on the ones that can support a hybrid energy source. Then, in section 3 a full system block diagram for the investigated design is given, with description of the separate subsystems involved. In section 4 the full system is simulated for a typical driving cycle involving acceleration and braking and the different waveforms are given. Finally, in section 5 a brief overview of the work is presented, along with some possible future iteration.

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II. EV Topology Overview

The design of a pure electric vehicle with a hybrid energy storage system consisting of a supercapacitor (SC) and battery is investigated in this paper. The great diversity of possible power train architectures does not allow for their full comparison, but the most popular types are shown in Fig. 1 [2], [5]. Their advantages and disadvantages are summarized in Table 1. In the particular realization a cascade configuration is chosen.

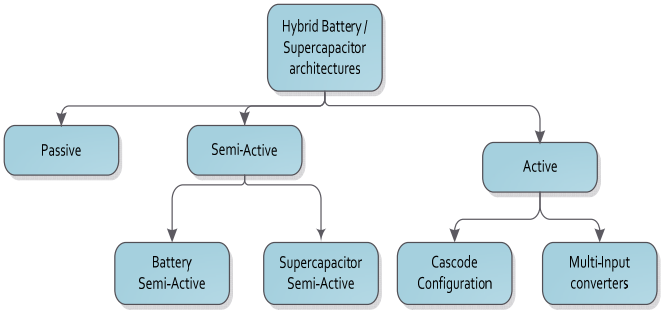

Fig. 1. Battery/Supercapacitor power train architectures

Table 1. EV power train architectures comparison

Type	Advantages	Disadvantages
Passive	Simple realization and control	Equal battery and SC voltage, Similar current profile for SC and battery
Battery Semi-Active	Requires only one additional power converter, adds a degree of freedom in choosing battery voltage and control its current profile	The supercapacitor needs to be at the same voltage as the motor
SC Semi-Active	Requires only one additional power converter, adds a degree of freedom in choosing the SC voltage	Braking energy absorbed by the battery is not directly controlled
Cascode configuration	Relatively simple control for active configuration, independent control of battery charge/discharge profile	Increased losses for the battery power flow path, also requires separate control of two additional converters
Multi-Input Converters	Minimizes the total amount of power switches or filter elements for the same degrees of freedom in power control	Increased control system complexity

III. System Level Description

To simulate an electric vehicle on the system level the designer must at least model the power source, electric motor, the vehicle dynamics and the power converters with their control circuits that manage the conversation between the energy source and the motor. A full system level

overview of an EV is shown in Fig. 2, where the black blocks are minimum requirements for a full system simulation. For this reason their implementation will now be separately explained.

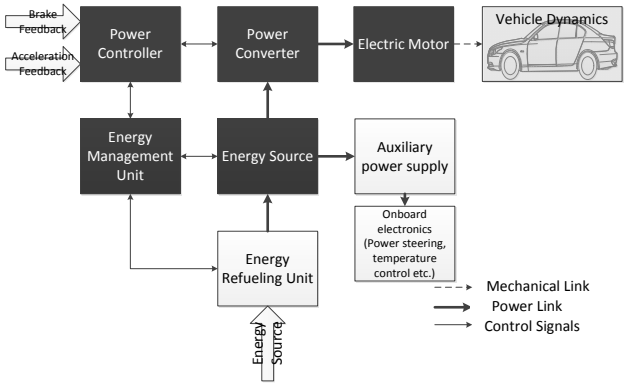

Fig. 2. System level overview of a EV

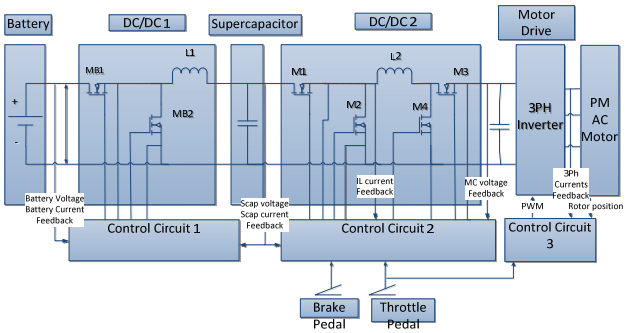

Fig. 3. Power train topology

A.Power Electronics

The power electronics in such an implementation consist of the main converters connected between the energy source (hybrid in this case consisting of a supercapacitor and battery) and the motor, along with its control systems that ensure proper energy management of the whole vehicle.

As noted in Section II the model in question will use a cascade configuration, which is shown in Fig. 3. The first converter with the accompanying control system are responsible control the voltage of the supercapacitor as a function of the vehicle speed in order it to be able to capture the kinetic energy in case the vehicle needs to slow down. The used two-quadrant converter allows the current to reverse direction boosting the voltage between the SC and the battery for a possible battery charging, if the voltage on the SC is higher than needed. The block diagram of the control circuit is shown in Fig. 4, and the Stateflow realization in Fig. 5.

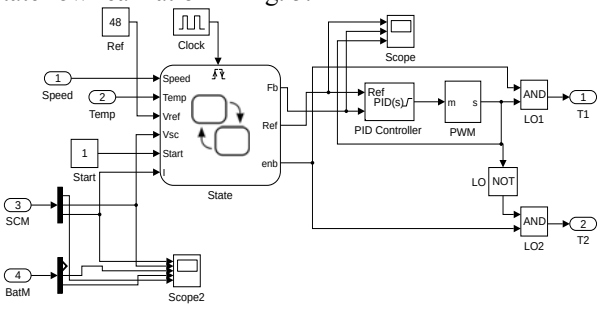

Fig. 4. Control circuit 1

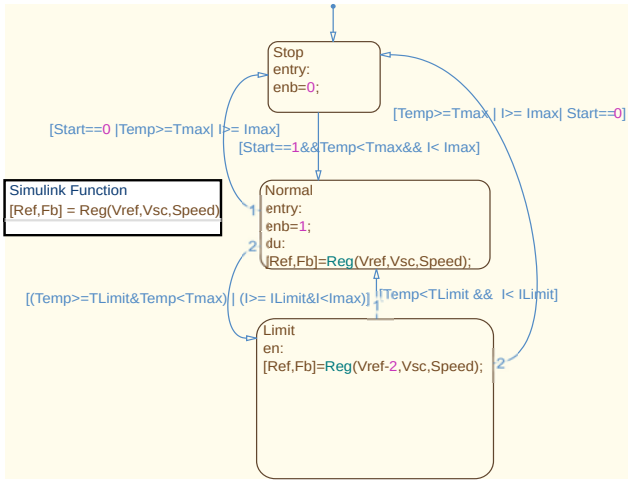

Fig. 5. Control circuit 1 state diagram

The second converter connected between the SC and the inverter is a noninverting buck-boost converter [3],[4]. When the vehicle is accelerating energy must be supplied to the motor from the hybrid energy source, and when the vehicle is braking energy is supplied from the generator.

In the first case the voltage at the input of the motor controller must be used as a setpoint, and the converter allows either buck or boost operation. The control system uses a current peak control algorithm to stabilize the voltage. In this case the output of the voltage control loop (PID2) is multiplied by the current, that is needed to achieve the desired torque (Iref) and this is the current reference used by the peak current controller.

During regenerative braking the control circuit uses the motor current as the setpoint in order to achieve constant braking torque. The control system then uses a hysteresis controller (Relay 2).

The block diagram is shown in Fig. 6, while Stateflow realization due to its size will not be shown. However, the main idea behind its realization is to set one of the possible operation modes of the power converter under consideration (shown in TABLE 2), the possibility of the a third operating regime where part of the cycle the converter is used as a boost and the rest as a buck is not investigated.

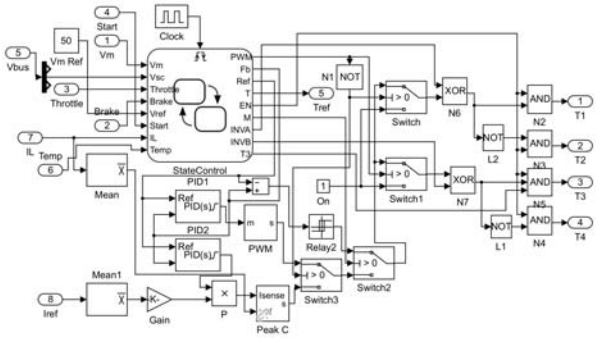

Fig. 6. Control circuit 2

TABLE 2. TRANSISTOR OPERATION IN DIFFERENT MODES OF OPERATION

Function \ Mode	Acceleration	Regenerative Braking
Boost	M1-On, M2-Off M3,M4- PWM	M1,M2-PWM M3- On,M4-Off
Buck	M1,M2-PWM M3- On,M4-Off	M1-On, M2-Off M3,M4- PWM

B. Power Source

The topology under investigation uses a hybrid energy source consisting of a battery and supercapacitor. The battery is optimized for long-term energy balance, so its dynamics can be neglected for the short term acceleration or braking times that will be considered. This motivates the decision to model it as a perfect voltage source, and lump its internal resistance with the resistance of the power converter that connects it to the supercapacitor.

The supercapacitor is modeled in its simplest form as a voltage dependent capacitor and an equivalent series resistance.

C. Motor

The motor used is a permanent magnet AC machine, due to the reduced driving requirements. The machine along with its inverter is control in the dq frame with torque setpoint given form the acceleration pedal. After the currents corresponding the torque are transferred back to abc domain, a hysteresis controller is used to track them. The control system is shown in Fig. 7.

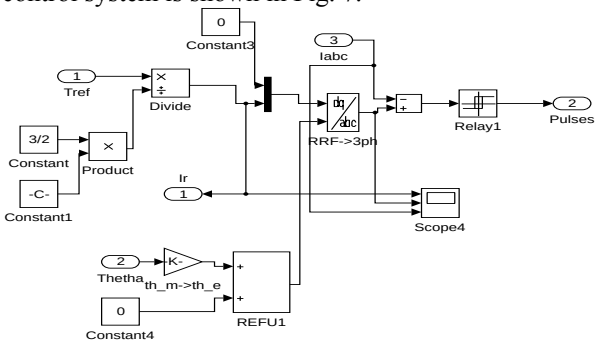

Fig. 7. Control circuit 3

A. Vehicle Dynamics

To simplify the full model the vehicle subsystem only considers a two dimensional model in which the second Newton law of motion is used to calculate the vehicle acceleration, while accounting only for the rolling resistance force, aerodynamic drag force and the grading resistance force, which are being subtracted from the traction force [5].

IV. Simulation Results

The full simulation diagram is shown in Fig. 8, while the power circuit in Fig. 8. Due to the large number of simulated elements and the large difference in the time constants in the mechanical and electrical subsystem the simulation step needs to be small to account for the PWM control of the power transistors, but the simulation time must be long to appreciate the vehicle speed changes.

This leads to very long simulation time of the whole system and the inability to achieve solution for long periods of time on a normal desktop computer. For this reason some simulation parameters are scaled allowing an minimization of the simulation time, and proper use of initial condition of the vehicle speed and supercapacitor voltage are implemented in order to obtain mechanical responses and test the validly of the overall control system.

The overall system behavior in case of full throttle from standstill to 100km/h and then a braking cycle is shown in Fig. 10.

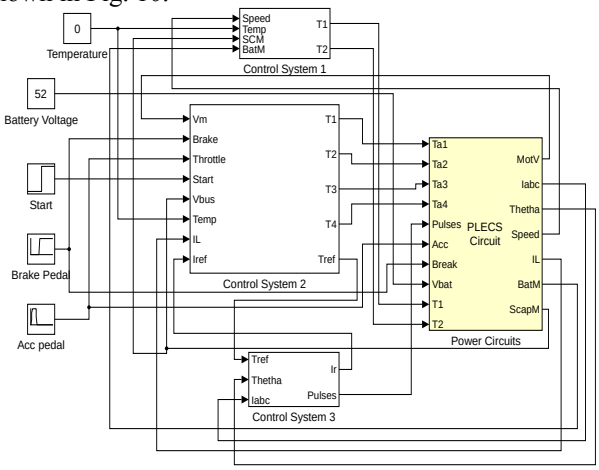

Fig. 8. Simulated circuit overview

V. Conclusion

The system level design and simulation of an electric vehicle with a hybrid energy source was the primary goal of this paper. To achieve this goal the various power train topologies were compared for achieving the goal set. After choosing an appropriate topology the system level overview of the control system were shown, together with the accompanying state level design. The complete system was than implemented using a popular software package that allows system level simulation. Finally, the various waveforms obtained for rapid acceleration and braking were shown for some parameters that allowed computation in a limited time due to the very time consuming simulation on a typical computer.

Acknowledgments

This work was supported in part by Technical University- Sofia through project 152ПД0010-03.

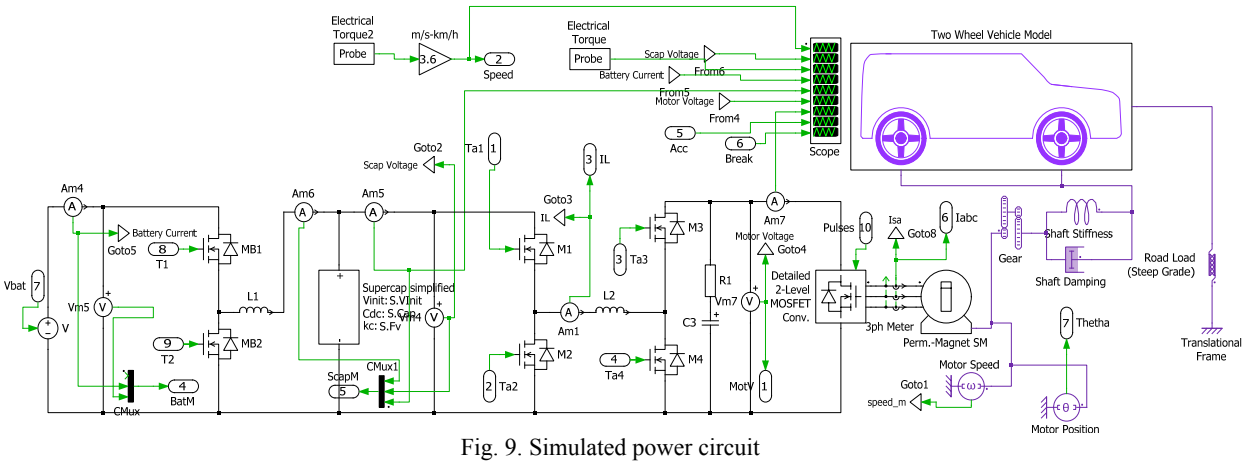

Fig. 9. Simulated power circuit

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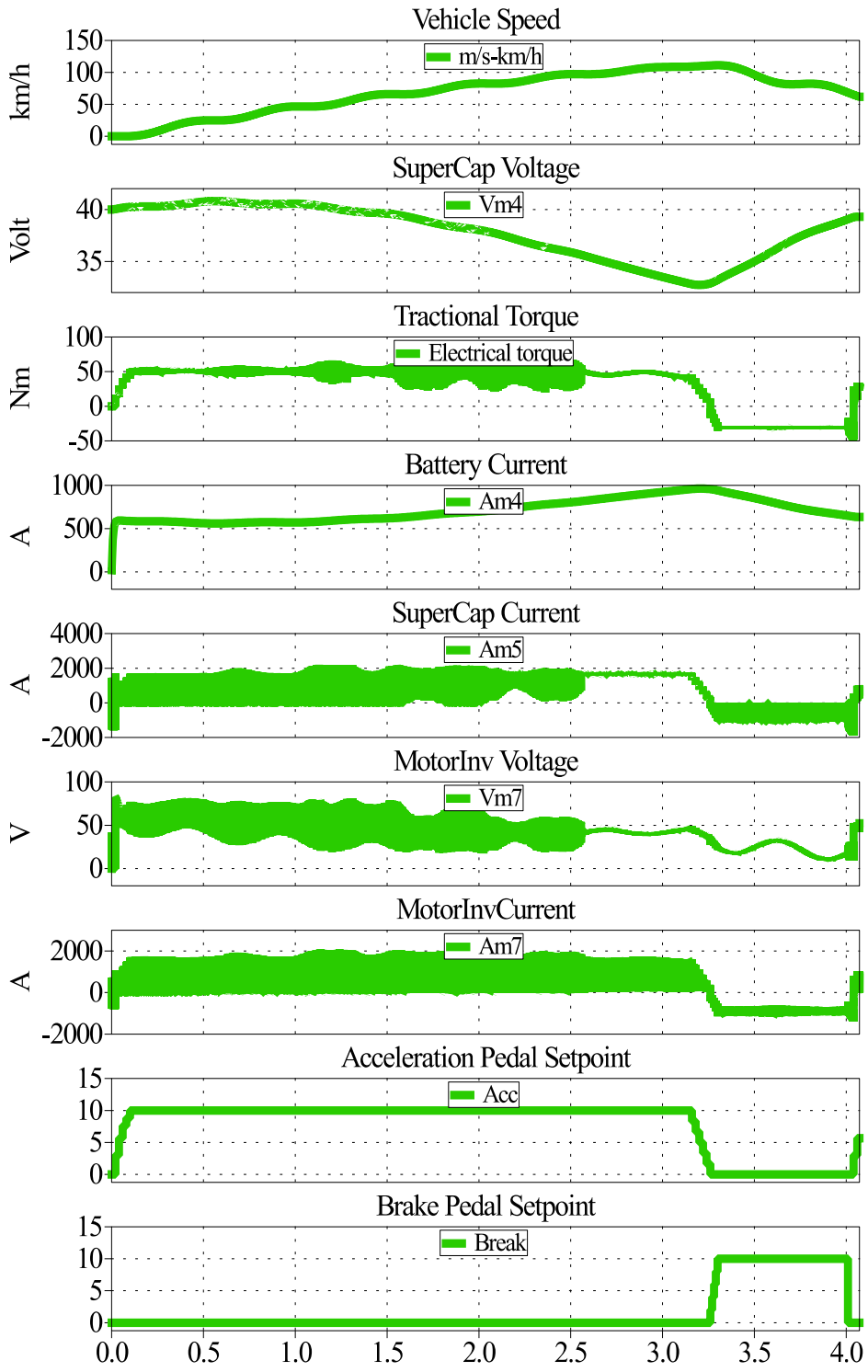

Fig. 10. Electric vehicle waveforms for an acceleration and braking cycle

Analysis and Design of the Parallel Quasi Resonant DC Link Converter for Induction Motor Drive Application

Dimitar Stoilov Spirov and Nikolay Georgiev Komitov

Abstract – **A parallel quasi resonant DC link converter for induction motor drive application is analyzed and designed. The proposed soft-switching inverter is formed from the traditional pulse-width modulated (PWM) inverter by simply augmenting with auxiliary resonant circuits, and the soft switching is achieved through applying PWM switching control signals with suitable delays for the switches. The designed soft-switching inverter is used for powering an induction motor drive which is connected to drive the constant nominal load. The converter is designed to achieve the maximum voltage gradient and simultaneously to have low peak current and voltage stresses on the devices and thereby to reduce the losses.**

Keywords – **Induction Motor Drive, Parallel Quasi Resonant DC Link Converter**

I. INTRODUCTION

Variable speed drives using induction machines require power electronic circuits that are capable of producing sinusoidal voltages of varying frequency and magnitude [1]. The control of adjustable speed drives is done by the power converters. In hard-switched power converters switching losses limit the applicable switching frequency. Switching with large du/dt reduces the switching losses. Bigger voltage gradients combined with long feeders lead to high frequency parasitic effects, like over voltages at motor terminals, high common mode ground current, bearing currents, etc. In addition, electromagnetic interference increases and efficiency decreases. To overcome these problems, the application of soft switching techniques is essential [1-5].

The resonant DC-link inverter is the most commonly used one for induction motor drives, owing to its simplicity, but it possesses the disadvantage of having a high resonant link voltage, which is equal to or greater than twice the supply voltage [2].

Quasi-resonant (QR) inverters offer several advantages compared with resonant DC-link inverters with regard to resonant link design and control, device rating requirements and use of pulse width modulation (PWM) [3]. The QR inverter schemes generate zero-voltage instants in the DC link at controllable instants that can be synchronised with any PWM transition command, thus ensuring a zero-voltage switching condition of inverter devices. As a result, these inverters can be operated at high switching frequencies with high efficiency [3].

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A number of discontinuously resonant link circuits employing a parallel resonant link arrangement in conjunction with additional switches have been reported in the literature [1-7]. These have in common that the resonant link is only active when the bus voltage has to be reduced to zero in order to commutate the inverter switches. Two distinct advantages can be identified. The voltage across the dc link is resonated from supply voltage level down to zero, hence, the voltage stress for the inverter devices never exceeds the supply voltage. A resonant cycle can be initiated at any time which enables inverter switching at any desired instant.

These inverters can be designed not only for the soft switching but also for the voltage gradient reduction. In addition to switching loss reduction, the resonant circuit undertakes the filter's task of reducing voltage overshoot at motor terminals. It is important to minimize the peak value of the resonant current in order to reduce the stress on circuit devices.

The object of this work is to analysis and design a parallel quasi resonant DC link converter for a three-phase induction motor drive soft-switching inverter. The passive component values must be selected to meet specific design criteria, to reduce the level of the common mode voltage and to minimize the peak value of the resonant current.

A. Mathematical model

The parallel quasi-resonant dc link converter is presented in [5-7] (Fig. 1). The six switches of the bridge are represented by a single switch S_{inv} for the purpose of the analysis [5]. The proposed converter shown in Fig. 2 consist of an ideal current source I_o, equivalent switch S_{inv}, diode D_{inv} and resonant circuit. To turn on the equivalent switch S_{inv} means to turn on both the switches in one of the inverter legs simultaneously. The diode D_{inv} is conducting means both the diodes in one of the inverter legs are conducting.

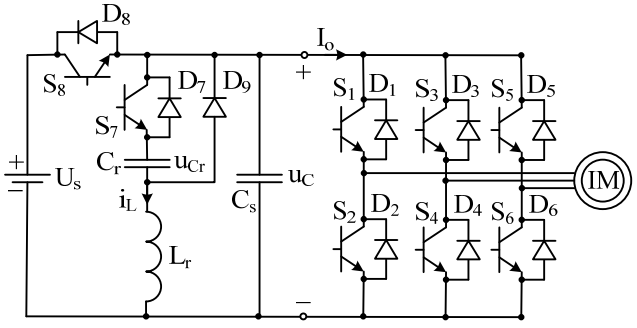

Fig. 1. Parallel quasi-resonant dc link converter

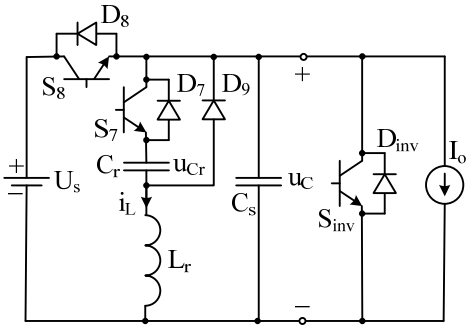

Fig. 2. Simplified circuit of the parallel quasi-resonant dc link converter

To simplify the analysis, all the components are assumed ideal. I_o is suddenly altered when the state of the inverter switches changes.

In Fig. 3, the main operational waveforms of the resonant circuit are shown.

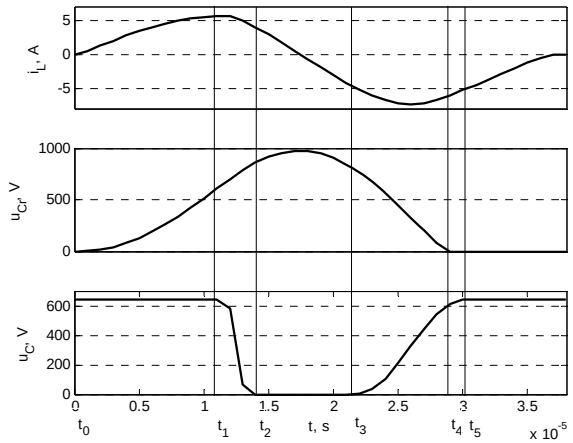

Fig. 3. Operational waveforms of the resonant circuit

The following notations will be used in the subsequent equations: $C_{rs}=C_r+C_s$; $C_e=C_rC_s/C_{rs}$; $k_s=C_r/C_{rs}$; $k_r=C_s/C_{rs}$; $\omega_r=1/\sqrt{(L_rC_r)}$; $\omega_s=1/\sqrt{(L_rC_s)}$; $\omega_e=1/\sqrt{(L_rC_e)}$; $Z_r=\sqrt{(L_r/C_r)}$; $Z_s=\sqrt{(L_r/C_s)}$; $X_{Cr}=1/(\omega_eC_r)$; $X_{Cs}=1/(\omega_eC_s)$; $X_{Ce}=1/(\omega_eC_e)$; $X_{Lr}=\omega_eL_r$.

In the steady state, the resonant tank energy is zero, S_8 is closed and S_7 is open.

$$\begin{aligned} &i_L(t)=0;\\ &u_{Cr}(t)=0;\\ &u_C(t)=U_s. \end{aligned} \tag{1}$$

An **energy storage interval** (t_0-t_1) is needed in order to store resonant energy in the resonant inductor L_r to ensure that the resonant link voltage does decrease down to zero, during the ramp down interval. The energy storage interval starts with turn-on of the resonant link transistor S_7 [5-7].

$$\begin{aligned} &\theta_0=\omega_r(t-t_0);\\ &i_L(t)=\frac{U_s}{Z_r}\sin\theta_0;\\ &u_{Cr}(t)=U_s(1-\cos\theta_0);\\ &u_C(t)=U_s. \end{aligned} \tag{2}$$

The energy storage interval is finished when the inductor current reaches the trip current $i_L(t_1)$.

$$i_L(t_1)=\frac{U_s}{Z_r}=i_L(t)_{\max}. \tag{3}$$

The duration of the energy storage interval is equal to

$$\Delta t_1=\frac{\pi}{2\omega_r}. \tag{4}$$

The **resonant link voltage ramp down interval**, (t_1-t_2) is initiated by turning off the resonant link series transistor S_8, forcing a discharge of the resonant link capacitor C_s [5-7].

$$\begin{aligned} &\theta_1=\omega_e(t-t_1);\\ &i_L(t)=(k_sI_o+i_L(t_1))\cos\theta_1+\\ &+\frac{U_s-u_{Cr}(t_1)}{X_{L_r}}\sin\theta_1-k_sI_o;\\ &u_{Cr}(t)=k_r(u_{Cr}(t_1)-U_s)\cos\theta_1+\\ &+X_{C_r}(k_sI_o+i_L(t_1))\sin\theta_1+\\ &+k_rU_s+k_su_{Cr}(t_1)-\frac{I_o(t-t_1)}{C_{rs}};\\ &u_C(t)=k_s(U_s-u_{Cr}(t_1))\cos\theta_1-\\ &-X_{C_s}(k_sI_o+i_L(t_1))\sin\theta_1+\\ &+k_rU_s+k_su_{Cr}(t_1)-\frac{I_o(t-t_1)}{C_{rs}}. \end{aligned} \tag{5}$$

The ramp down interval is finished when the resonant link voltage reaches zero.

During the **zero voltage interval** (t_2-t_3) the resonant link voltage is clamped to zero, first by the converter freewheeling diodes and then by the converter transistors [5-7].

$$\begin{aligned} &\theta_2=\omega_r(t-t_2);\\ &i_L(t)=i_{Lr}(t_2)\cos\theta_2-\frac{u_{Cr}(t_2)}{Z_r}\sin\theta_2;\\ &u_{Cr}(t)=u_{Cr}(t_2)\cos\theta_2+\\ &+Z_ri_{Lr}(t_2)\sin\theta_2;\\ &u_C(t)=0;\\ &i_{Dinv}(t)=i_L(t)+I_o. \end{aligned} \tag{6}$$

The zero voltage interval is finished when the diode current i_{Dinv} reaches zero. The duration of the zero voltage interval is equal to

$$\Delta t_3=\frac{1}{\omega_r}\arctan\left(\frac{X_{C_s}i_L(t_2)}{u_{Cr}(t_2)}\right) \tag{7}$$

The equations valid for the **resonant link voltage ramp up interval** (t_3-t_4) are given below [5-7].

$$\begin{aligned}
&\theta_3 = \omega_e(t-t_3);\\
&i_L(t) = (k_s I_o + i_L(t_3))\cos\theta_3 -\\
&+\frac{u_{Cr}(t_3)}{X_{L_r}}\sin\theta_3 - k_s I_o;
\end{aligned} \tag{8}$$

$$\begin{aligned}
&u_{Cr}(t) = k_r u_{Cr}(t_3)\cos\theta_3 +\\
&+X_{C_r}(k_s I_o + i_L(t_3))\sin\theta_3 +\\
&+k_s u_{Cr}(t_3) - \frac{I_o(t-t_3)}{C_{rs}};\\
&u_C(t) = k_s u_{Cr}(t_3)(1-\cos\theta_3) -\\
&-X_{C_s}(k_s I_o + i_L(t_3))\sin\theta_3 -\\
&-\frac{I_o(t-t_3)}{C_{rs}}.
\end{aligned} \tag{9}$$

The resonant link voltage ramp up interval is finished when u_{Cr} reaches zero. The duration of this interval is equal to

$$\Delta t_4 = \frac{1}{\omega_e}\arcsin\left(\frac{X_{C_s} I_o}{u_{Cr}(t_3)}\right) \tag{10}$$

During the **resonant energy recovery interval**, (t_4-t_5) the excess energy stored in the resonant inductor L_r is transferred back to the DC link voltage sources U_s via the resonant link series diode D_8. Furthermore, this also implies that the resonant link voltage is clamped to the DC link voltage level. During the energy recovery interval the resonant link series transistor S_8 is turned on, to be able support the current fed to the converter during the off resonance period. The equation valid for this mode is thus written [5-7]

$$\begin{aligned}
&\theta_4 = \omega_s(t-t_4);\\
&i_L(t) = (i_L(t_4) + I_o)\cos\theta_4 +\\
&+\frac{u_{Cr}(t_4)}{Z_s}\sin\theta_4 - I_o;\\
&u_{Cr}(t) = 0;\\
&u_C(t) = u_{Cr}(t_1)\cos\theta_4 -\\
&-Z_s(I_o + i_L(t_4))\sin\theta_4.
\end{aligned} \tag{11}$$

The resonant energy recovery interval is finished when u_C reaches U_s.

The inductor current i_L goes back to zero from a negative value. The equation valid for this mode is thus written [5-7]

$$\begin{aligned}
&i_L(t) = i_L(t_5) + \frac{U_s}{L_r}(t-t_5);\\
&u_{Cr}(t) = 0;\\
&u_C(t) = U_s.
\end{aligned} \tag{12}$$

The duration of this interval is equal to

$$\Delta t_5 = -L_r\frac{i_L(t_5)}{U_s} \tag{13}$$

B. Design Considerations

A good design of the resonant elements is important in order to reduce the peak voltage stress and the peak current stress on the devices [5]. The specifications to design the quasi resonant dc link inverter circuit parameters are as follows [5, 6]:

- The inverter input voltage must be pulled down to zero for zero voltage switching (ZVS) and again boosted to the DC link source voltage;
- The trip currents should be as small as possible in order to reduce the circuit power loss;
- It is important to minimize the peak values of the resonant voltage and the resonant current in order to reduce the stress on circuit devices;
- The rising and falling slope of the inverter output voltage must be low for long cable drives;
- The resonant transition interval must be designed to be much shorter than inverter's switching frequency cycle time.

The peak resonant voltage $u_{Cr}(t_{ucr.max})$, peak inductor current $i_L(t_{ir.max})$, falling time of the voltage u_C - Δt_f and resonant transition interval T_s are to be obtained from the equations, derived for different modes.

$$t_{ucr.\max} = \frac{1}{\omega_r}\arctan\left(\frac{Z_r i_L(t_2)}{u_{Cr}(t_2)}\right) + t_2 \tag{14}$$

$$t_{ir.\max} = \frac{-1}{\omega_e}\arctan\left(\frac{u_{Cr}(t_3)}{X_{Lr}(i_L(t_3) + k_s I_o)}\right) + t_3 \tag{15}$$

It is difficult to obtain an analytical solution for the falling time of the voltage u_C - Δt_f and resonant transition interval T_s due to complex modes. The "root" function of the software product Mathcad is used to determine these functions [8]. The result is obtained in the form: *root(f(var1, var2, ...),var1, [a, b])*. The "root" function returns the value of *var1* lying between *a* and *b* at which the function *f* equal to zero. Fig. 4 shows the variation in peak resonant voltage $u_{Cr}(t_{ucr.max})$ for different values of the L_r^*, C_r^* and C_s^*. The quantities shown in Fig. 3 are normalized, where the L_r, C_r and C_s base values are the optimal values L_{rb}=L_{ro}=800μH, C_{rb}=C_{ro}=60nF, C_{sb}=C_{so}=20nF.

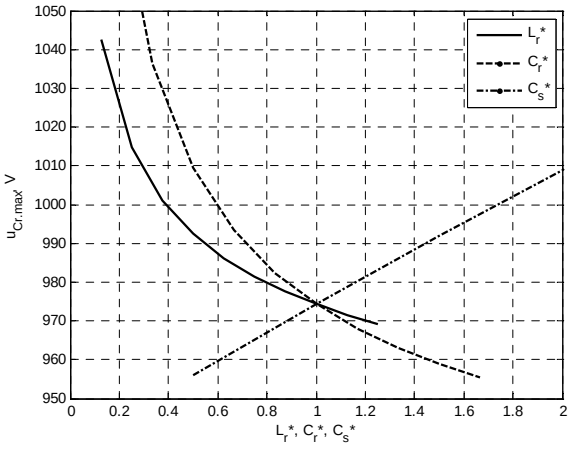

Fig. 4. Dependences $u_{Cr.max}$=f(L_r^*), $u_{Cr.max}$=f(C_r^*), $u_{Cr.max}$=f(C_s^*)

Fig. 5 shows the variation in peak inductor current $i_L(t_{ir.max})$ for different values of the L_r^*, C_r^* and C_s^*.

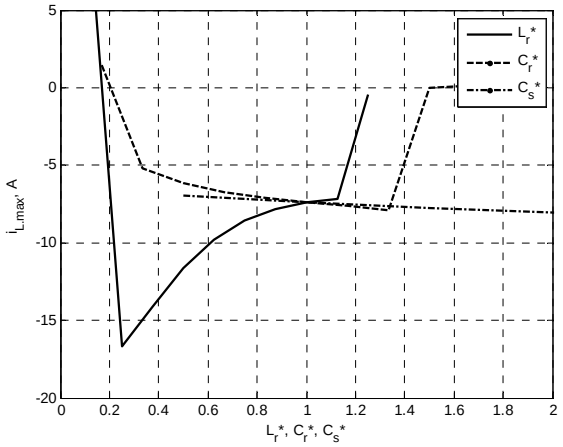

Fig. 5. Dependences $i_{Lr.max}$=f(L_r^*), $i_{Lr.max}$=f(C_r^*), $i_{Lr.max}$=f(C_s^*)

Fig. 6 shows the variation in falling time of the voltage u_C - Δt_f for different values of the L_r^*, C_r^* and C_s^*.

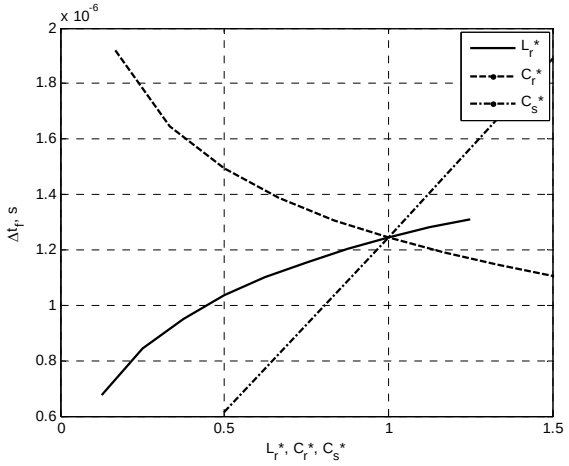

Fig. 6. Dependences Δt_f=f(L_r^*), Δt_f=f(C_r^*), Δt_f=f(C_s^*)

Fig. 7 shows the variation in resonant transition interval T_s for different values of the L_r^*, C_r^* and C_s^*.

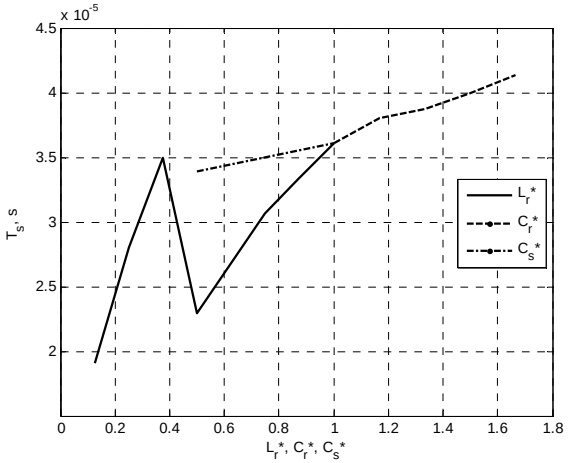

Fig. 7. Dependences T_s =f(L_r^*), T_s =f(C_r^*), T_s =f(C_s^*)

The converter is designed to achieve the maximum voltage gradient and at the same to have low peak current and voltage stresses on the devices and thereby to reduce losses. The selected parameters for this resonant converter were summarized in Table 1.

TABLE 1. THE SELECTED PARAMETERS FOR THE RESONANT CONVERTER

Resonant Inductor L_r	800μH
Resonant Capacitor C_r	60nF
Parallel Capacitor C_s	20nF

The basic circuit of the proposed scheme consists of a three phase induction motor type AO-90S-4 having ratings as 1,1kW, 380V, 50 Hz which is connected to drive the constant nominal load. The parameters used in the simulation were U_s=640V, I_o=5A. The Mathcad model of proposed soft-switching converter for powering of the three phase induction motor drive has been developed.

The peak resonant voltage, peak inductor current, falling time and resonant transition interval for the selected parameters were summarized in Table 2.

TABLE 2. PEAK VALUES, THE FALLING AND RESONANT INTERVAL TIME

Peak resonant voltage $u_{Cr.max}$, V	974,27
Peak inductor current $i_{Lr.max}$, A	-7,371
Falling time of the voltage u_C - Δt_f, μs	1,24
Resonant transition interval T_s, μs	36,13

II. CONCLUSION

A parallel quasi resonant DC link converter for induction motor drive application is analyzed and designed. Link waveforms and operation modes are analyzed to reveal various soft switching characteristics. The converter is designed to achieve the maximum voltage gradient and simultaneously to have low peak current and voltage stresses on the devices and thereby to reduce the losses.

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Evaluation of the Used PWM Techniques in the Control of Brushless DC Motors

Ivan Petrov Maradzhiev and Dilyana Marinova Ognyanova

Abstract – **At present the brushless DC motors find increasingly wider application, thus different methods for their control are developed. The paper presents varieties of pulse-width modulation applied in control of these types of motors. It is researched, analyzed and evaluated the energy exchange between motor and power source using the unipolar modulation of upper and lower transistors of voltage invertor, PWM_PWM and PWM_ON modulation. The load characteristics in each of examined PWM technics are researched, as well.**

Keywords – **Motor control, brushless motor, power electronics, modulations**

I. INTRODUCTION

In the dynamic life of modern society time and its optimal use is of great importance. It becomes possible by increasing the degree of automation of the surrounding environment. Automation helps in solving both specific and global problems, regarding the control of various mechanisms. The trend observed in modern automatic is the increase of share of brushless DC motors, such as low-power actuators, at the expense of AC motors. There are various power schemes and methods for power control. However, the requirement for modern automated systems is connected with higher efficiency and smaller electromagnetic interference. Brushless motor technology allows achieving it. These machines combine high reliability with high efficiency at lower price compared to brush DC motors in spite of the identical characteristics [1].

A specific feature of brushless DC motors is the requirement for invertor powering of their phase windings and feedback of the rotor position (Fig. 1). This is all needed to determine the moments of invertor commutation. Determination of rotor's position can be done with Hall sensors which are installed on the motor or without sensors by measuring back electromotive force (emf) generated in the stator windings during rotation of the rotor [1][2].

A three-phase brushless motor is powered by three-phase voltage system, in which voltages are shifted by 120° from each other. The voltage applied to the phase windings of the motor can be expressed by Eq.1:

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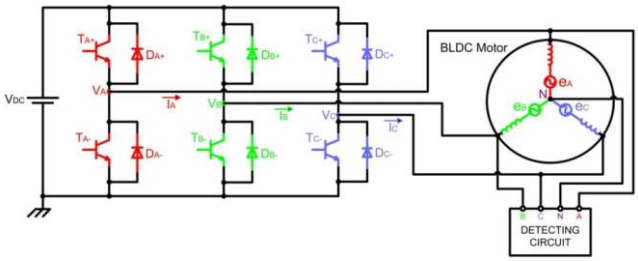

Fig. 1

$$\begin{aligned} V_a &= Ri_a + L\frac{di_a}{dt} + e_a \\ V_b &= Ri_b + L\frac{di_b}{dt} + e_b \\ V_c &= Ri_c + L\frac{di_c}{dt} + e_c \end{aligned} \qquad (1)$$

where: R - active resistance of the windings; i - current flowing through the windings; **e** - the generated back emf in the motor windings. That back emf can be expressed by Eq.2:

$$\begin{aligned} e_a &= K_e + \phi(\Theta)\omega(t) \\ e_b &= K_e + \phi\left(\Theta - \left(\frac{2\pi}{3}\right)\right)\omega(t) \\ e_c &= K_e + \phi\left(\Theta + \left(\frac{2\pi}{3}\right)\right)\omega(t) \end{aligned} \qquad (2)$$

where: K_e - voltage constant of the motor; ω - speed of rotation; ϕ - magnetic flux; Θ - position of the rotor [4][5].

Eq. 1 and Eq.2 shows that the speed of rotation of the motor depends on the value of the applied voltage to the motor windings [1]. So the adjustment of the rotational speed of the motor requires regulation of its voltage. Therefore for the control of brushless machines various PWM technics are developed, which adjust the average value of the applied voltage. This present report examines the most common modulations - unipolar modulation of upper and lower transistors of the voltage invertor, PWP-PWM modulation and PWM-ON modulation. In the research is used development system DRV8312-C2, which includes microcontroller and TMS30F28035 and DRV8312 Three-Phase PWM Motor Driver.

TMS320F28035 are part of the family of C2000 microcontrollers, which enable cost-effective design of intelligent motor controllers by reducing the system components and increasing efficiency. The DRV8312 is high performance, integrated three-phase motor driver with an advanced protection system [6][7]. Fig. 2 shows a block diagram of the system.

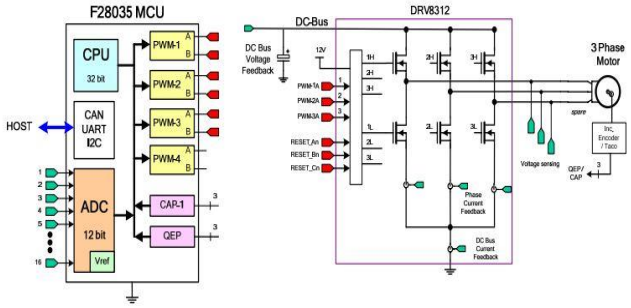

Fig. 2.

II. Types of Modulations Used for Control of Brushless DC Motors

A. Unipolar modulation of upper and lower transistors of the three-phase voltage inverter

Unipolar PWM is one of the most widely used modulation for electric drives. Its feature is that in the three-phase voltage inverter only the lower transistors of the inverter are modulated but the upper are permanently switched on (at a lower unipolar transistors, it's opposite for upper unipolar modulation). Time-diagram of this type of modulation, and the synchronization with the sensors of position for one cycle of the algorithm of the phase shifting coils is shown at Fig. 3. In comparison with bipolar PWM in unipolar PWM the voltage pulsations are reduced by half. Unipolar PWM is also called "soft" switching modulation [3].

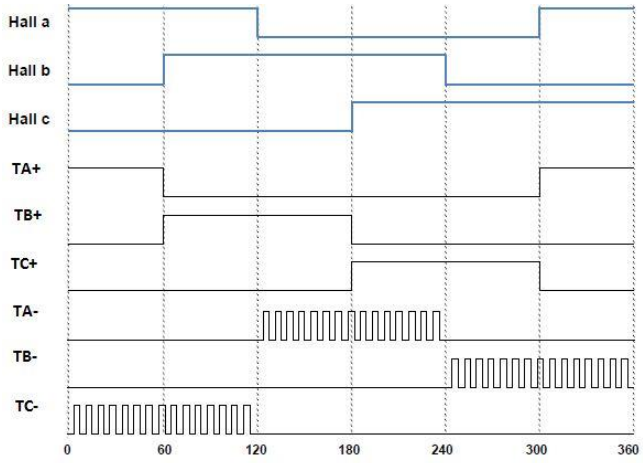

Fig. 3.

B. PWM-PWM modulation

This type of modulation is shown in FIG. 4. In its essence it is a symmetric PWM (PWM-PWM), at which complementary phased modulation is performed, phase A-transistors TA + and TA-; Phase B - TB + and TB-, and for phase C - TC + and TC- Fig. 1. The duration of modulation is 2 steps [2].

This technique of modulation is used in the low voltage power systems, and is characterized by small switching losses.

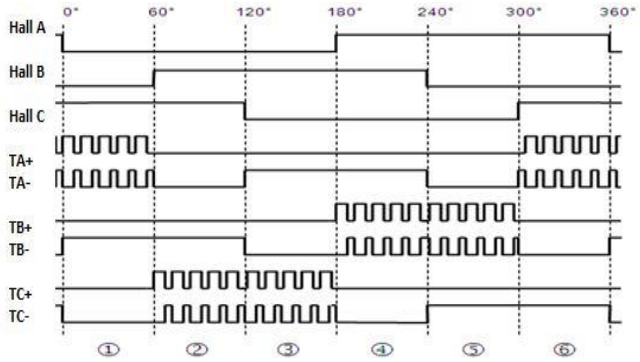

Fig. 4.

C. PWM-ON modulation

Mixed PWM (PWM-ON) is shown in Fig.5. When there is complementary, phased modulation for phase A- TA + and TA-; Phase B - TB + and TB-, and for phase C - TC + and TC-. The duration of the phased modulation is one step. Additional second step is uncontrolled (hard switching) [2].

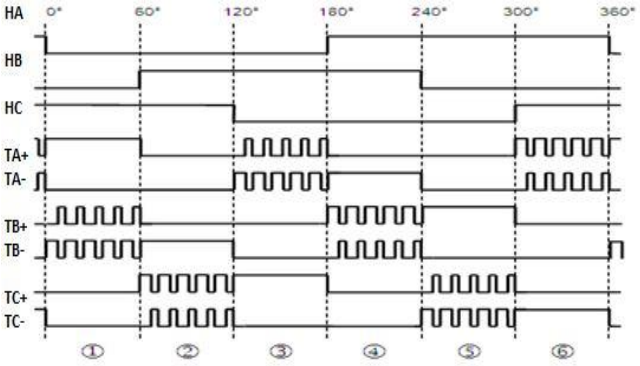

Fig. 5.

The high side power device is chopped in 1/6 fundamental period and duty ratio is derived from the speed reference. Similar control signal is applied to the low-side power device with 180º shift. These control signals are applied to the other two phases with 120° shift. As the high-side device is with chop control, the associated low-side power device is triggered by the inverse signal of chop control.

It is used in low powerful electric drives, in order to reduce commutation losses and therefore thermal losses, and electromagnetic noise, as well.

III. Experimental Results

The experimental results are made by the DRV8312-C2 evaluation board and brushless DC motor type DT4260-24-055-04 (24V, 55W). The speed of the motor is set to 1500rpm. The frequency of the PWM signals is 20 kHz. The control signals are fed to the PWM_X and RESET_X inputs of the DRV8312 chip [6][7]. By using the principle of operation of the three-phase driver, modulation techniques described above are realized and tested.

A. Waveforms of the supply current for different types of PWM

On Fig. 6 are shown waveforms of the current consumed from the supply source and a PWM signal to one of the RESET inputs of the driver. These waveforms are for unipolar modulation of upper transistors.

A specific feature is the appearance of negative peaks of the current consumed by the power source on each 120 electric degrees.

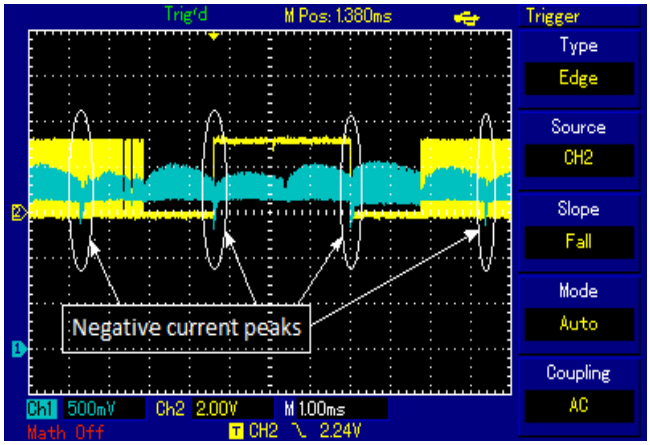

Fig. 6. Supply current (trace1), RESET_B signal (trace2) for unipolar upper transistors modulation

These negative peaks are caused by stored energy in motor windings inductance Eq. 3. They appear when two lower transistors of the inverter change their conditions.

$$W_L = \frac{I^2 L}{2} \qquad (3)$$

From the moment of switching off a bottom transistor until the moment of switching on the other bottom transistor, the energy in the phase inductance changes its polarity. The energy that is stored in inductance becomes negative and returns to the power source, using the built-in reverse diodes of the MOSFET transistors in the three-phase voltage inverter.This process is illustrated in Fig. 7.

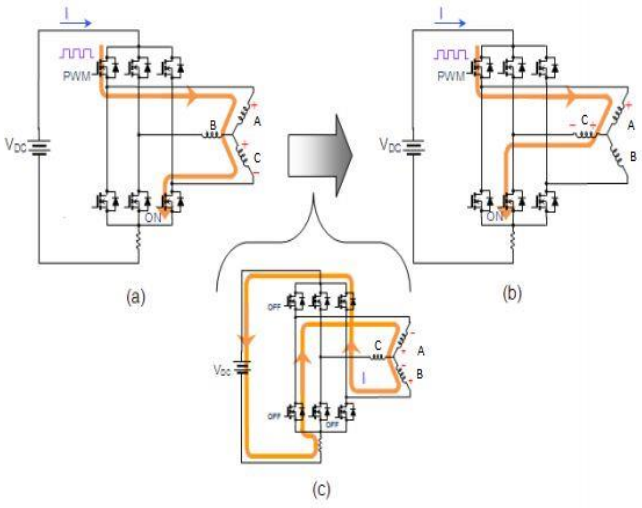

Fig. 7.

On Fig. 8 are shown waveforms of the current consumed from the supply source and a PWM signal to one of the RESET inputs of the driver. These waveforms are for unipolar modulation of lower transistors.

Again, there are negative peaks in the form of the total current. The cause is the same as described above with the difference that occurs when commutation between two upper transistors happen.

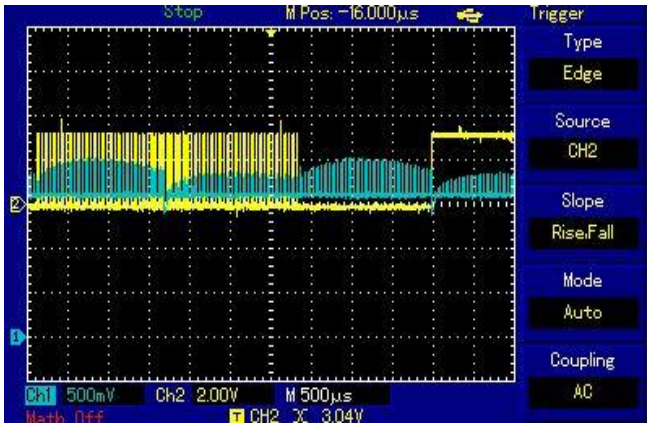

Fig. 8. Supply current (trace1), RESET_B signal (trace2) for unipolar lower transistors modulation

On Fig. 9 are shown waveforms of the current consumed from the supply source and a PWM signal to one of the RESET inputs of the driver when PWM-PWM modulation is tested. With this type of modulation of the transistors, the negative peaks of the total current are seven times greater than its peaks in unipolar modulation. The process of generation of these peaks is identical like in unipolar modulation of top transistors. These peaks are main cause of generation of electromagnetic noise. Also, when the battery power supply is used such negative peaks are not conducive to the battery.

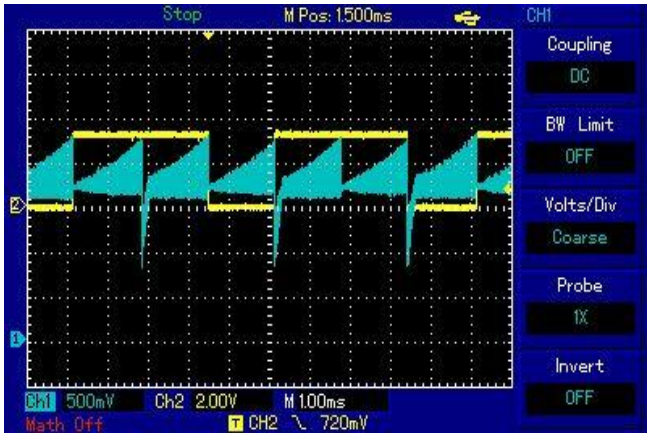

Fig. 9. Supply current (trace1), RESET_B signal (trace2) for PWM-PWM modulation

On Fig. 10 are shown waveforms of the current consumed from the supply source and a PWM signal to one of the PWM inputs of the driver when PWM-ON modulation is tested. At this type of modulation of the transistors, it's clearly seen that there are no negative peaks in the form of the current consumed from the power source.

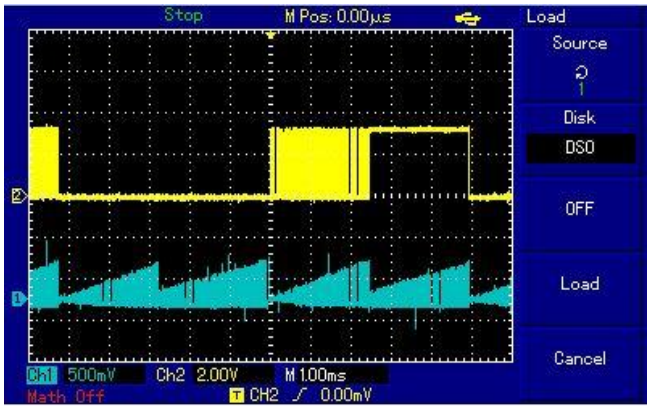

Fig. 10. Supply current (trace1), PWM_B signal (trace2) for PWM-ON modulation

This leads to less-electromagnetic noise. This modulation is suitable for use with battery power supply.

B. Load characteristics

Load characteristics of the motor are made with the modulation techniques described above. For that purpose, brushless motor is connected to another DC motor type NISCA MM5475B, who works in generator mode and serves as a load. The speed of the brushless motor without load is set to 1500 rpm. Torque-speed characteristics are shown on Fig. 11.

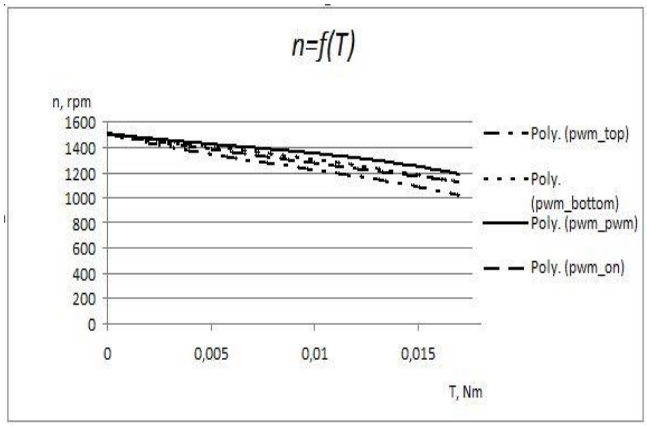

Fig. 11. Torque-speed characteristics of four types of modulations

It is noticeable, that the load characteristic by using PWM-PWM modulation is hardest. For this method of modulation when the load is 17mNm the speed of the motor drops by 310rpm. The softest load characteristic is obtained by using unipolar modulation of top transistors. In this case with the same load the speed drops by 500 rpm. The load characteristics by using unipolar modulation of lower transistors and PWM-ON modulation are identical.

C. Evaluation of current consumption from the power source

Along with the load characteristics for four types of modulation the current consumption from the power supply is measured. The change of the current by increasing the load of the motor is shown in Fig. 12.

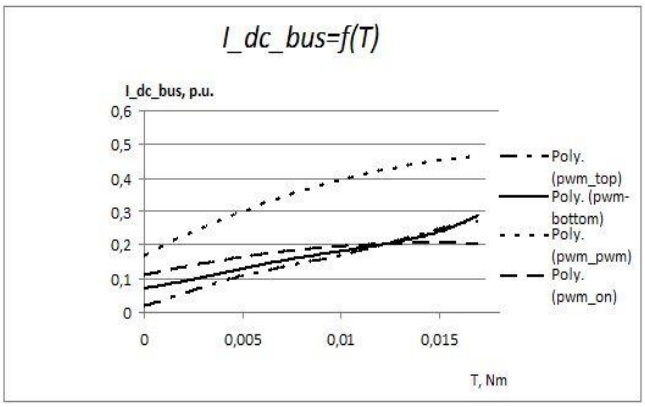

Fig. 12.

The value of current is given in relative units compared to the maximum motor current. It is noticeable that the PWM-PWM modulation consumes approximately twice as large current compared to the PWM-ON modulation. This is the reason for the hard load characteristic of the PWM-PWM modulation.

IV. CONCLUSION

The presented four types of modulation techniques used in control of brushless DC motors demonstrate different behavior in terms of current consumed from the power source. The experiments show that the unipolar modulation of upper or lower transistors leads to generation of negative peaks on the total current on every 120 electric degrees. These negative peaks are especially large in PWM-PWM modulation. This is the main disadvantage of these types of modulation, because negative current peaks are source of electromagnetic noise. In contrast, PWM-ON modulation has no such negative current peaks. Furthermore the research proved that the PWM-PWM modulation is suitable for use in bigger loads at the expense of the current consumed from the power supply, while PWM-ON modulation is suitable for use in battery-powered electric drive and also in environments where there are increased requirements in terms of electromagnetic noise.

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Enhanced Read-Out System for RADFET Dosimeters Research

Georgi Mitev Mitev, Snejana Sarieva-Jordanova and Mityo Georgiev Mitev

Abstract –**This paper proposes a novel system for RADFET read-out, which allows measuring its threhold voltage at varied current levels. The system has the distinctive ability to change the direction of the readout current. That way the characteristics of the reverse diode between the drain and the silicon base can be measured and the FET temperature can be determined. Te paper also presents experimental data from pMOSFET ZVP4424 dynamic characteristics measurements.**

Keywords – **RADFET, Read-Out System**

I. INTRODUCTION

The first research on the effects of ionizing radiation on semiconductor devices started at the beginning of the 60s of the last century. Initially the limits when the semiconductor circuits stop working properly due to irreversible damage were studied. Later a variety of efficient and highly sensitive semiconductor radiation detectors were developed. In the mid-70s was proposed the idea 0 to use the accumulated defects in semiconductors to estimate the total absorbed ionizing radiation dose.

A. Application of pMOSFET as dosimetry sensors

When a semiconductor is exposed to ionizing radiation electron-hole pairs are produced. The holes in the gate area of a MOSFET are trapped in the SiO_2 layer above the channel. That creates a slight positive charge at the gate which in turn increases the threshold voltage of the p-channel MOSFETs. This effect is used to determine the dose the semiconductor device has absorbed.

Usually the dose absorbed in the pMOSFET is determined by the change in the threshold voltage *ΔVth* 0,0,0, at a predefined point on the $I_D=f(V_{GS})$ characteristic. The dose is calculated empirically using (1):

$$\Delta V_{th} = A.D^n \qquad (1)$$

where for a given MOSFET *A* is a coefficient of proportionality and *n* accounts for the nonlinearity.

Sometimes the absorbed dose is determined by the change of the slope of the I-V characteristics. This poses the requirement to measure more than one point on the characteristic $I_D=f(V_{GS})$. The absorbed dose is determined using 0 the equation (2):

$$\Delta D = a.\left(S_{D2} - S_{D1}\right) = a.\Delta S \qquad (2)$$

where *ΔS* is the change of the slope of the I-V characteristic and *a* is a coefficient of proportionality. The slope is defined as (3):

$$S = \frac{dV_{GS}}{d(Log(I_D))} \qquad (3)$$

It should be noted that the relation between the dose and the slope change *ΔS* is much more linear than between the dose and the threshold voltage *ΔVth*.

Because of their small size, ease of use (dose can be accumulated without power and/or external circuitry) and relatively simple measurement circuit pMOSFET are becoming a popular dose measurement solution in radiotherapy, for dosimetry control in industry and nuclear facilities and for radiation exposure monitoring in space ships.

B. Problems, research and solutions

Nowadays special transistors have been created, popular as RADFET, designed specifically for dosimetry 0. Their parameters are highly repeatable and have been thoroughly studied. The DDGAA RADFET 0 can be used as an example. They are distinguished for their unique design and excellent linearity over a wide dynamic range but their price is very high which prevents their widespread use. This is a motivation for many research teams to study the possibility to use cheap, widespread general purpose p-channel MOSFETs for the same purpose.

Some of the most commonly studied transistors are BS250F, ZVP3306 and ZVP4525 0,0. The ZVP3306 for example have shown excellent sensitivity and very good linearity. In 0 the possibility to use the pMOS inside CD4007 has been studied. They have achieved very good results – high sensitivity and easy temperature compensation due to the Zero Temperature Coefficient (ZTC) region occurring at low drain current - I_D value of about 140 μA.

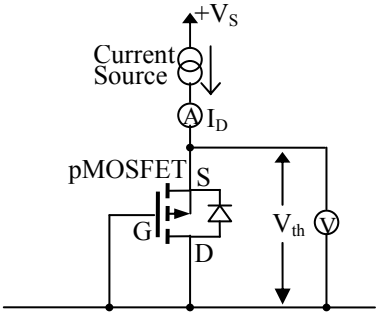

Fig. 1

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Various circuit solutions have been used 0, 0 to measure the threshold voltage V_{th}. The gate of the pMOS is connected to the drain and a current source is applied at the source (fig. 1). The drain-source voltage and the source current are measured to determine the threshold voltage or the transfer function. This circuit has positive output voltage and is compatible with practically every existing ADC, either stand-alone or integrated in a microcontroller.

The temperature dependence of the pMOSFET parameters may pose a serious problem when determining V_{th} or S. Its value may be of the same magnitude or even greater than the change caused by the absorbed dose. The most elegant solution when measuring V_{th} in only one point is to choose is so it coincides with I_{ZTC} (zero-temperature coefficient drain current). Unfortunately this can't be done for power MOSFETs as I_{ZTC} can be as high as a few amperes. For those cases a temperature sensor is used (usually a thermistor) which measures the MOSFET temperature. After making the measurements the data is corrected for the temperature dependence.

C. Reasoning behind the read-out system research

The need to determine the suitability of a growing number of general purpose pMOSFETs to be used as absorbed dose sensors is increasing. Their sensitivity and temperature instability have to be determined. As a side task the limits for stable operation of the devices when exposed to ionizing radiation can be determined.

The compensation of the thermal instability is an especially important topic. We believe the change, due to the absorbed dose, of the I-V characteristics of the reverse diode between the drain and the silicon base haven't been thoroughly studied. In case this change is sufficiently small the reverse diode can be used to measure the temperature of the semiconductor. That would allow for precise compensation of the thermal effects in the MOSFET and eventually allow for more precise measurement of the dose.

D. Research tasks

The main task of the research is to create an enhanced read-out system for measurement of the characteristics (V_{th} and S) of pMOSFET transistors after they have been exposed to ionizing radiation. It should also be able to measure the I-V characteristics of the reverse diode between the drain and the silicon base. The read-out system must support measurements at varied values of the current through the MOSFET. It must also be able to reverse the current direction in order to measure the diode characteristics.

II. System Design

A system has been developed that allows performing the measurements required for the research tasks. It measures the initial values of the threshold voltage V_{th} of the chosen pMOSFETs as well as the *I-V* characteristics of the transistors and their reverse diodes at different preset temperatures. The system also allows offline measurement of the parameters after the MOSFET has been irradiated.

A. Experimental setup

Figure 2 shows the experimental setup. It contains a thermostat that allows keeping the pMOSFET at a predefined temperature for the duration of the measurement. The temperature can be varied in the range 20 to 65 ^{o}C with an accuracy of at least ±0.5 ^{o}C. The temperature value is measured by the DAQ system.

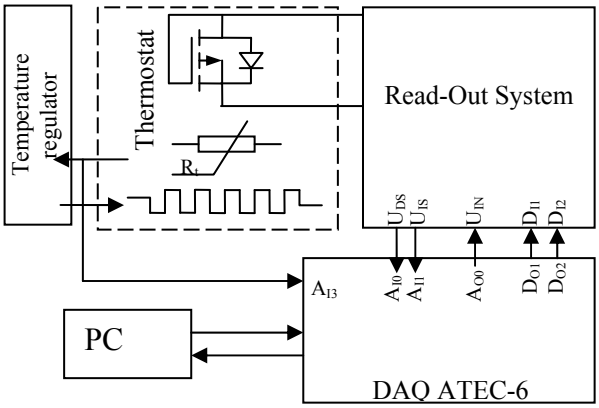

Fig. 2

The specially developed read-out system allows measuring the forward and reverse *I-V* characteristics of the pMOSFET. The output of the read-out system is a positive voltage for both forward and reverse currents, which allows easy coupling to the data acquisition system DAQ. The DAQ used is a 6 channel mixed signal system ATEC-6+1 0. It links to a PC by an RS232 serial interface.

B. Structural diagram of the read-out system

At the heart of the system is a bipolar voltage-to-current convertor that is connected to the pMOSFET (Fig. 3). The measurement point (current) is setup by the DAQ. A series

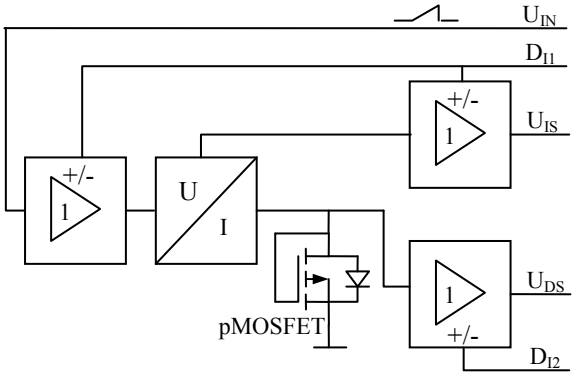

Fig.3

of successive settings allows scanning the *I-V* characteristic of the device.

A digitally controlled inverting amplifier allows inverting the setting. That way the current direction can be reversed and allows measuring the reverse diode characteristic. That would output negative voltages to the DAQ (U_{DS} and U_{IS}), that's why the output digitally controlled inverting amplifiers are used to change the sign of the output. The U_{DS} voltage equals the voltage of the

reverse diode or the V_{th} of the MOSFET. The U_{IS} voltage is proportional to the current through the device.

C. Read-out system schematic

Figure 4 shows the read-out system schematic. The operational amplifier U1B and the analogue switch S1A make up the setting input digitally controlled inverting amplifier. When the switch is open it repeats the U_{IN} voltage from the DAQ. When the switch is closed the amplifier has an amplification coefficient of -1 and inverts the voltage. Its output voltage controls the voltage-to-current convertor.

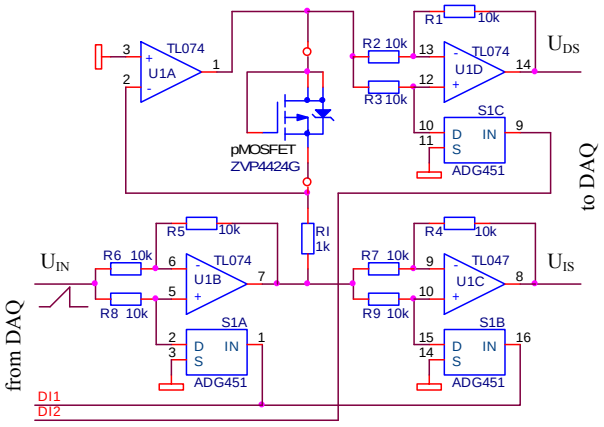

Fig.4

The bipolar voltage-to-current convertor consists of the *U1A* operational amplifier and the R_I resistor. The source is always connected to a virtual ground. The drain is driven by the op-amp in an opposite polarity to the setting voltage. The current is proportional to the voltage across R_I.

The output digitally controlled inverting amplifiers consist of *U1C* and *U1D* and the *S1B* and *S1C* analogue switches respectively. They use the same schematic as the input amplifier. The U_{DS} voltage equals the voltage of the reverse diode or the V_{th} of the MOSFET. The U_{IS} voltage is proportional to the current through the device.

The readout system allows a unipolar DAQ to make bipolar measurements of pMOSFET (or other) devices.

D. Measurement sequence

In order to measure the p-channel MOSFET a positive voltage has to be applied to R_I. The DAQ sets logical "1" on *DI1* which configures *U1B* and *U1C* as repeaters. The drain voltage is negative. The *U1D* is configured as an inverting amplifier by setting *DI2* to logical "0".

The DAQ then applies a range of setting voltages from 0V to 5V which corresponds to current values from 0 to 5mA. Both output voltages U_{DS} and U_{IS} are measured for each current setting. The data is used to determine the *I-V* characteristic of the pMOSFET.

To determine the characteristic of the reverse diode the current direction has to be reversed. *U1B* и *U1C* are configured as inverting amplifiers by setting *DI1* to logical "0". The anode voltage is positive so *U1D* is configured as a repeater by setting *DI2* to logical "1". The characteristic is measured the same way as for the MOSFET.

III. Results and Discussion

A series of experiments have been carried out with the Enhanced Read-Out System. The characteristics of

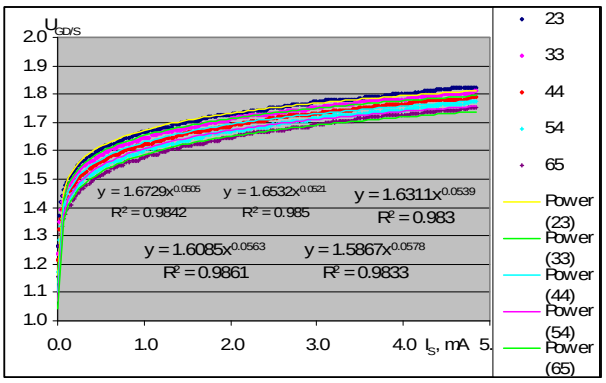

Fig.5

pMOSFET ZVP4424 as well as those of the reverse diode have been measured at different temperatures.

Figure 5 shows the pMOSFET ZVP4424 characteristics at different temperatures. Their change with temperature can be seen easily. In the measured range of currents no zero-temperature coefficient drain current has been observed.

Taking this into account:

a) the measurements should be carried out in multiple points of the characteristic;
b) the transistor temperature should be measured;
c) the compensation of the thermal shift should be carried out using digital processing.

Figure 6 shows the characteristics of the reverse diode at different temperatures. Again their temperature dependence can be clearly seen.

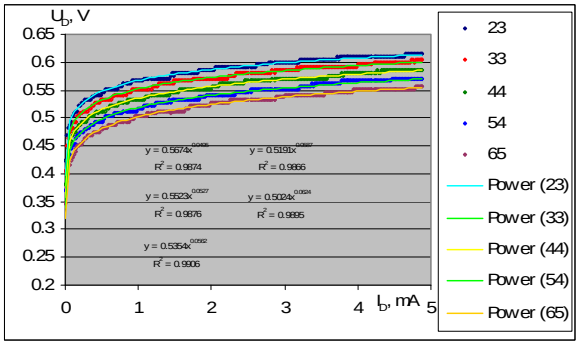

Fig. 6

IV. Conclusion

As a result of the analyses of the measurement conditions when measuring p-channel MOSFETs to determine their absorbed dose a special Enhanced Read-Out System has been developed and studied. It allows measuring the pMOSFET temperature using the reverse diode as well as multi-point measurements. That allows

making measurements with pMOSFETs whose zero temperature coefficient is well outside the system's current range. The ability to reverse the current polarity allows for a wide range of studies that would be inaccessible otherwise.

ACKNOWLEDGEMENT

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Light Extraction Improvement of LED Packages

Berkant Seydali Gyoch

Abstract – **The area of research relates to efficiency improvement of LED packages. The purpose of this work is to present a method for increasing of light extraction from LEDs. Light extraction is the ratio of photons emitted from the semiconductor chip into the encapsulant to the total number of photons generated in the active region. Decreasing of emitted photons is the effect of light reflection back into the chip caused by the refractive indices differences of intermediate media. Reduction of optical losses may be achieved by wide-band antireflection (AR) coatings for the intermediate elements of LED packages, with the first stage - wide-band AR coatings design.**

Keywords – **power LED, antireflection coatings**

I. Introduction

Over the past few years an improvement in the technological characteristics of power LEDs can `be seen. According to Directive 2005/32/EC of the European Parliament and to the Council of the European Union of 06.07.2005, the energy efficiency is a major evaluation of the work for each well designed system. The accepted goal by the European Commission in 2007: strategy 20-20-20 is related to 20% reduction of energy consumption by 2020 (20% increase of energy efficiency, 20% reduction of CO_2 emissions, and 20% renewables by 2020).

Also in a multiyear program plan of the US government (Solid - State Lighting Program featuring Building Technologies Office, Office of Energy Efficiency and Renewable Energy, US Department of Energy) 2011, 2012, 2013, 2014 [1] trends in the booming LED lighting equipment are presented. The losses in LED packages achieved efficiency and expected improvements in efficiency until 2020 (green colored ones) are presented in Fig. 1.

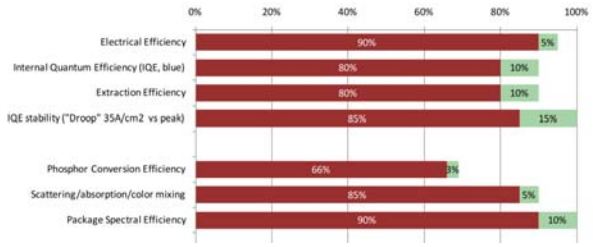

Fig. 1. LED package and luminaire loss channels and efficiencies [1].

Light extraction losses from LEDs are considerable (up to 20%) and according to multiyear program plan of the US government should be improved to 2020, see Fig. 1. Light reflection losses from each optical boundary in LED, due to refractive indices differences, may be reduced essentially. Between the semiconductor active region and environment some subsidiary media are located – chip (GaAs, Si, InGaN, GaN), fluorescent material, silicone resin (encapsulation layer), lenses. In Fig. 2 section view of a LED is presented. It can be seen that the number of optical boundaries in a LED is quite big. The media have refractive indices **n** from 1.8 to 3 and refractive index of air is n = 1. LED chip is usually made from semiconductor with refractive index n ≈ 2.5 [1- 5].

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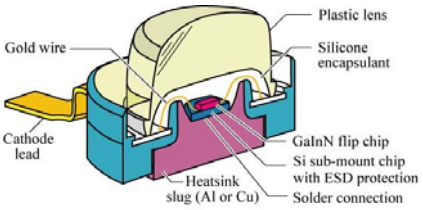

Fig. 2. LED power section view.

Reducing reflection losses can increase the efficiency of LED light extractions. Optical losses only from LED chip at normal incidence of a boundary without antireflection (AR) coatings are over than 18% [2-5]. If we add reflections in the optical elements (n = 1,5 ÷ 1,8), the total optical losses are expected to be more than 25 – 30 %. The usage of AR coatings can reduce them.

II. Design of Antireflection Coatings

Several approaches for design of wide-band antireflection coatings are known [2]. The simplest AR coating is a single layer with optical thickness nd = λ/4, 3λ/4, 5λ/4 ... and refractive index $n = n_S^{1/2}$ (n_S is the substrate refractive index) which acts properly only at one wavelength [2]. Appropriate methods for multilayer coating design in wide spectral region are based on numerical optimization [2, 3]. In those methods the structure of a multilayer coating (number of layers, their refractive indices and thicknesses) is a result of numerical optimization of a proper function.

When refractive indices and thicknesses of all initial structures are calculated, their AR properties can be compared. In our case it is performed by average reflectance, which will be called as factor *Q*. It is calculated according to the following equation:

$$Q = \sqrt{1/N \sum_{i=1}^{N} R^2(\lambda_i)_{CALCULATED}}, \quad (1)$$

where λ_i is N discrete equidistant wavelength values in investigated spectral region 0.38 – 0.78 μm, $R(\lambda_i)_{CALCULATED}$ – calculated reflectance as function of λ_i. The structures with lower value of *Q* have better AR properties.

In our work structures two materials for layers are used because they are much more convenient and easy for deposition. As a rule those structures consist of layers of low- and high-refractive index materials which are usually denoted with *L* and *H* [2, 3].

For semiconductor substrates with refractive index n≈2.5 4620 initial antireflection structures are designed and after optimizing several of them are proposed.

For appreciation of AR properties of the coating, average reflectance *Q* in research spectral region is used. It is called *Q*-factor, *Qin* - for initial structures or *Qopt* - for optimized structures, their values are given in percentages. *Q* corresponds to the average value of the reflectance in the whole selected spectral range.

All designed initial structures are 4620 number; below see some of them with better AR properties:

✓ Bilayer AR structures with different initial optical thicknesses *Din* have an average reflection: for *Din* = λ/4 *Qin* = 5,58%, for *Din* = 3λ/4 *Qin* = 10.65% and for *Din* = 5λ/4 *Qin* = 12.09%.

✓ Four layers structures with initial optical thickness: *Din* = λ/4 *Qin* = 3.12%; *Din* = 3λ/4 *Qin* = 21.93%; *Din* = 5λ/4 *Qin* = 17.71%.

✓ Six layers structures with initial optical thickness: *Din* = 3λ/4 *Qin* = 21.06%; *Din* = 5λ/4 *Qin* = 40.43%.

✓ Others worse multilayer structures.

The final thicknesses of all layers are found as a result of numerical minimization of *Q*, equation (1). The optimization procedure consists of steps which number is equal to the number of optimized thicknesses. Each step is one-dimensional minimization carried out by means of the golden section method [2,3]. In many cases thickness of a layer in a given k-layer initial structure becomes negligible after minimization procedure and the corresponding optimized structures are considered as (k-1)-layer.

Obtained structures are large number and a lot of them do not improve enough AR properties of substrate that is appropriate to be deposited. Therefore several conditions for assessing the quality of the multi-layer AR structures are accepted: 1) the usage of fewer materials in terms of manufacture and durability of the multilayer coating are preferable; 2) fewer layers are technologically and economically more advantageous for deposition; 3) the average reflection *Q* should be low, *Qopt* <1%; 4) changes in values of layers' refractive indices n_H and n_L and their thicknesses remains *Qopt* less than 1%.

III. Results and Discussion

Analysis of optimized multilayer structures in accordance with the above mentioned conditions for quality assessment shows that the best AR properties have three types of structures (two-layer, four-layer and six-layer):

✓ **2-layer** structure is obtained with refractive indices of layers n_H = 2.05 and n_L = 1.35 (air/LH/n_S) *Qopt* = 0.33%, reflection spectrum is presented in Fig. 3. In the figure reduction of reflection losses comparing with those from uncoated substrate is shown. The initial structure significantly reduces reflection from substrate, but at a higher wavelengths reflection increase to $R_{(\lambda = 780nm)}$ = 10%. Compared with the initial structure, optimized two-layer structure has better AR properties for entire spectral range. The maximum values of reflectance R for double-layer structure at one wavelength is less than 2% and the values reached at $R_{(\lambda=380nm)}$ to 1,43%, at $R_{(\lambda=516nm)}$=0,66% and $R_{(\lambda = 660nm)}$ = 0,64%. Total physical thickness of the **2-layer** coating is 150 nm.

✓ After optimization of the initial **4-layer** structures of air/LHLH/n_S type *Qopt* = 0.14% for n_H = 2.4 and n_L = 1.3 is obtained, see Fig. 2. The initial structure has the best AR properties for wavelengthes λ = 450 - 500 nm. After optimization of *Q* **4-layer** structure has a maximum value of reflectance $R_{(\lambda = 380nm)}$ = 0.32%, $R_{(\lambda = 500nm)}$ = 0.16% and $R_{(\lambda = 780nm)}$ = 0.30%. **4-layer** structure is better than two-layer structure. The maximum value of the reflectance R is lower than *Qopt* of structures with **2-layer**. In comparison with **2-layer** the total physical thickness of the **4-layer** coating is increased to 210 nm.

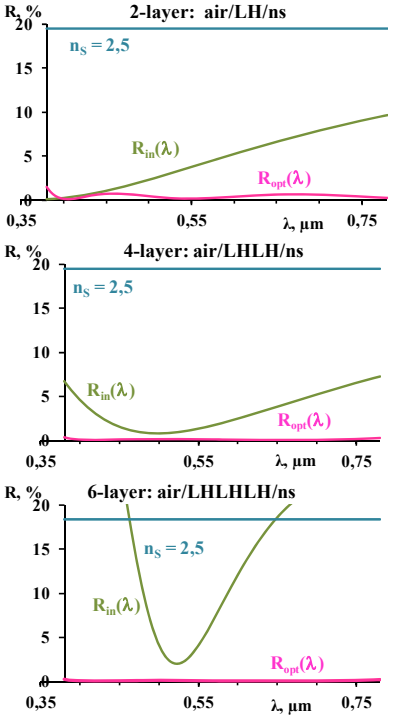

Fig. 3. Reflectance spectra of uncoated substrate n_S of refractive index 2.5 (blue line); of initial structure *Rin(λ)*(green line) and of optimized antireflection coatings R_{opt} *(λ)*(pink line).

✓ After optimization of the initial **6-layer** structures of type air/LHLHLH/n_S the lowest average reflection of *Qopt* = 0.12% at n_H = 2.6 and n_L = 1.3 is obtained, see Fig. 2. The maximum values of reflectance R are for $R_{(\lambda = 380nm)}$ = 0.2%, $R_{(\lambda = 500nm)}$ = 0.15% and $R_{(\lambda = 780nm)}$ = 0.23%, they are at the same wavelengths as the **4-layer**. Compared to other structures total thickness of the **6-layer** coating is increased two - three times (410 nm).

In order to find a better AR properties average reflection as a function of the parameters of low- and high-refractive indices for the three structures are investigated. This study is carried out when for each combination of the changes of refractive indices values layer thicknesses have been optimized. Average reflection as a function of the refractive indices n_H and n_L of three AP structures is presented in Fig. 3. The areas with the average reflection *Qopt* < 0.5% are colored in blue and *Qopt* with <1% - red.

Average reflection of **2-layer** structure stays *Qopt* <1% for n_H = 1.9 ÷ 2.25 and n_L = 1.3 ÷ 1.5. For comparison, **4-** and **6-layer** keep good AR properties for values of n_H and n_L in a much wider range.

The results obtained in the study of changes in the refractive indices can identify areas of values n_L and n_H for selecting and using materials in the coating before deposition (manufacturing), as the average reflection remain below 1%.

To manufacturing **2-layer** AR coatings materials with refractive indices n_L = 1.3 ÷ 1.45 and n_H of 1.9 ÷ 2.2 are suitable. It is seen (Fig.4) that the number of possible combinations of materials n_L and n_H is not large.

For **4-layer** AR coating may be used for layer's materials n_L = 1.3 to 1.55 and n_H = 2.1 to 3.5 values. Their number are the greatest in comparison with the other two structures.

6-layer AR coating required materials with n_L = 1.45 to 1.5 and n_H= 2.0 to 2.55 refractive indices. For low refractive index can be used n_L = 1.5 (a material with such a refractive index in a visible spectral region is silica, a material with very good density of the coating and mechanical strength, which makes it preferable for the outer layer of the multilayer AR coatings [2, 4, 5]) but n_H should be in the range of 2.1 to 2.5.

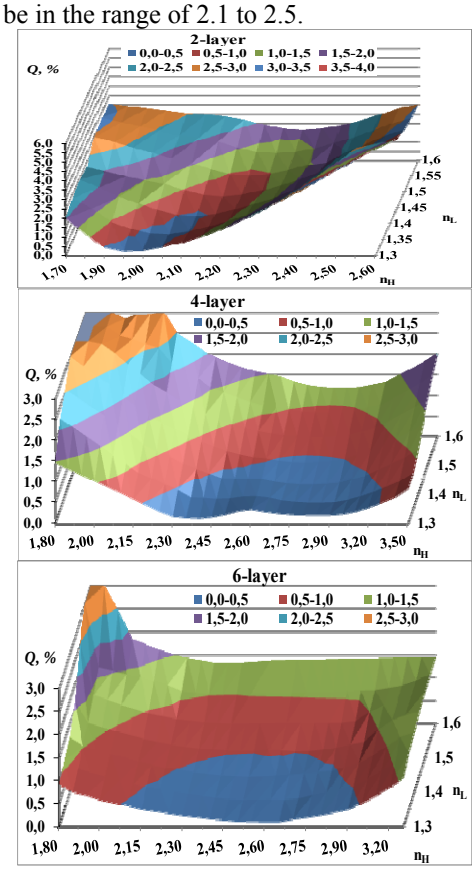

Fig. 4. Average reflectance Q as a function of refractive indices n_L (1,3 ÷ 1,6) and n_H (1.8 ÷ 3.5) for 2-layer, 4-layer, 6-layer structure on substrate n_S=2.5 for the visible spectral region.

From the presented above we can see that the number of possibilities to use various materials in n_L and n_H of coating layers is the largest for **4-layer** AR structure (according to condition that *Qopt* < 1%) and the lowest – for **2-layer**. Changes in the values of n_H at **4-layer** and at **6-layer** affect less to coatign AR properties than n_L.

The phase thickness deviations' influence on the properties of AR coatings for designed three multilayer structures on substrate with n_S = 2.5 is analyzed, too. Phase thickness is a parameter, which depends on wavelength λ, thickness d and refractive index n of antireflective coating's layers. The investigation is performed in three stages. Those three steps have been described in detail in our previous work [6].

The investigation was performed as layers materials for 2-, 4- and 6-layer structures substituted with values of the refractive indices of real materials. Materials with high refractive index are usually used: n_H=2.05 (ZrO_2, Si_3N_4), n_H=2.35 (TiO_2) and material of low refractive index n_L = 1.38 (MgF_2) [3 - 6]. Magnesium fluoride is characterized by good resistance to external influences, which makes it convenient to use as a outer layer of the coating. With this substitution values of Q is obtained:

- ✓ 2-layer structure of *Air/LH/n$_S$* – type, where are used n_L = 1.38 and n_H = 2.05 Q_{OPT}= 0.39 %. In this case total thickness of coating is obtained 156 nm.
- ✓ 4-layer structure of *Air/LHLH/Substrate* – type, where are used n_L = 1.38 and n_H = 2.05 Q_{OPT} = 0.34 %. Total thickness of coating is obtained 174 nm.
- ✓ **6-layer** structure of *Air/LHLHLH/Substrate* – type, where are used n_L = 1.38 and n_H = 2.05 Q_{OPT} = 0.43 %. Total thickness of coating is obtained 326 nm.

First stage.

Dependences of average reflectance Q of the substrate with AR coating as a function of refractive indices n_L (from 1.3 to 1.5) and n_H (from 1.9 to 2.7) at **constant thicknesses of separate layers** are investigated.

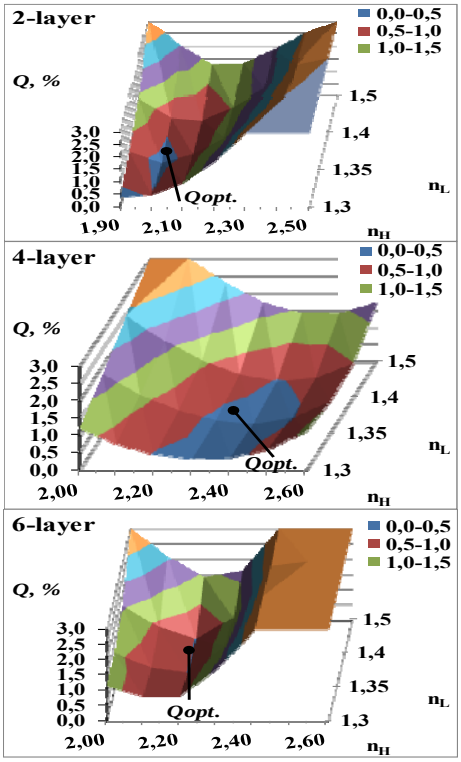

Fig. 5. Averaged reflectance Q as function of refraction indices n_L (from 1.3 to 1.5) and n_H (from 1.9 to 2.7) for AR structures on substrate n_S=2.5 at constant thicknesses of separate layers for the visible spectral region. *Qopt* - point where chosen multilayer structures have best AR properties.

2-layer structure is more sensitive to deviations of refractive indices $\mathbf{n_H}$ and $\mathbf{n_L}$ of layers which have coating.

It can be seen in Fig.5, that the change of n_H mostly affect the **2-layer** AR properties, therefore n_H should be in the range from 1.9 to 2.1, and n_L can be changed from 1.3 to 1.45. AR properties of **6-layer** influenced mostly from deviations of refractive indices. **4-layer** structure has a better resistance to changes in the refractive indices of the layers than other investigated multilayer AR structures. Even with large changes in refractive indices n_H and n_L within the interval $n_L = 1.3 \div 1.5$ and $n_H = 2.7 \div 3.4$, Q factor remains below 1%.

Therefore the most resistant to deviations of refractive indices $\mathbf{n_H}$ and $\mathbf{n_L}$ is **4-layer**.

Furthermore by comparison of Fig. 4 and Fig. 5 can be seen the complex relationship between the thicknesses of the separate layers and their refractive indices for the respective AR coating.

Second stage.

Optical properties of **2-layer, 4-layer and 6-layer** AR structures are evaluated by modeling at: thickness' variations of each layer by ± 5 nm at constant values of layer's refractive indices n_H and n_L.

For all investigated AR structures the most influenced is the increase in the total thickness of the coating on AR properties, so it is important to do not increase the thickness of designed optimum values. At least influenced change thicknesses (d_H) of layers with high refractive indices minus 5 nm, and d_L unchanged.

Thickness' deviations impact minimal on **2-layer** with $Qopt$ = 0.39%, $n_L = 1.38$, $n_H = 2.05$. For this structure, the number of combinations of thickness' deviations are greatest and average reflectance stays - Q <1%. Compared with **6-layer** and **4-layer** it is more resistant to changes in the thickness of the layers. The biggest impact in **4-layer** has change of d_L layers +5 nm and d_H layers minus 5 nm simultaneously, at which the value of Q deteriorates only to 1.06%. Therefore it can be argued that **4-layer** also has good resistance to thickness' deviations of separate layers.

Third stage.

Dependencies of average reflectance Q for substrate with AR coating to deviations of substrate refractive index n_S (from 2 to 3) at constant n_L and n_H and at constant thicknesses of separate layers are investigated. In Fig.6 it is shown for **2-layer**, **4-layer** and **6-layer** AR structures.

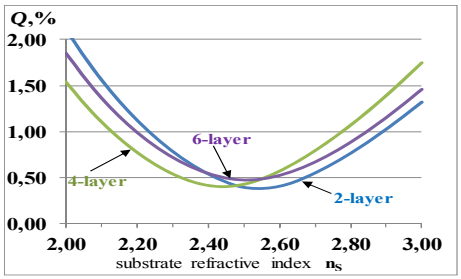

Fig. 6. Averaged reflectance Q as a function of substrate refractive index n_S at constant thicknesses and refractive indices of separate layers for the visible spectral region.

The analysis of all multi-layer structures with deviations in the value of the refractive index of the substrate n_S, to predict deterioration on properties of multilayer antireflection coatings after deposition of coating is carried out. Moreover possibility of the use of these coatings for substrates with different values of the refractive index is investigated, because refractive indices of the various optical elements in LED are not made from the same materials. Light emitting diodes (GaAs, Si, InGaN, GaN), lenses, the fluorescent material, silicone resin (encapsulation layer) and the surrounding air. They have refractive indices (n or n_S) with values from about 2 to 3 [1-5].

The differences between the three structures are minimal. For values of 2.4 <n_S <2.65 **2-layer** has the lowest average reflection (Q < 0.5%), and for values 2.32 <n_S <2.55 - **4-layer**.

2-layer can be used on n_S in the range of 2.45 to 3.0, and in this range the Q factor preserves lower than the 4-layers and 6-layers Q factors.

4-layer can be used for n_S in the range of 2.0 to 2.45, and in this range the Q factor preserves lower than the 2-layers and 6-layers Q factors.

For values of $n_S = 2 \div 2.45$ it is appropriate to use **4-layer** coating, and $n_S = 2.45 \div 3.0$ - **2-layer**.

IV. Conclusion

From the analysis of the results in this research can be concluded that universal one is not designed yet, but the designed coatings can be selected to satisfy different needs and substrates. Best resistance to the influence of external factors to AR properties is performed at three stages. First place is assigned to 4-layer and 2-layer lags behind only in changes of n_L and n_H. Taking into account a lower number of coating layers it can be considered that **2-layer** mostly appropriate AR structure for values of $n_S = 2.45 \div 3.0$ and for $n_S = 2 \div 2.45$ it is appropriate to use **4-layer** coating.

Acknowledgement

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LED Lamp for Application in Horticulture

Petko Hristov Mashkov, Berkant Seydali Gyoch, Katya Konstantinova Asparuhova, Hristo Ivanov Beloev and Rostislav Yuriev Kandilarov

Abstract – **In this paper the results related to the construction and testing a LED lamp with special spectral characteristics and radiant flux, suitable for industrial applications in horticulture are presented. By selection of different types of LEDs and control of their operation the desired spectral distribution of lamp's luminous flux is achieved. Thermal management analysis and experimental investigations in thermal chamber are made. Safety operation conditions for LEDs are determined in dependence of LEDs' operation regimes and ambient conditions.**

Keywords – **LEDs' thermal management, greenhouse lighting, power LEDs**

I. INTRODUCTION

Nowadays replacing current light sources with new LEDs becomes hot topic. Latest LEDs have luminary efficacy even higher than 100 lm/W in contrast to the best fluorescent lamps that reach 60-65 lm/W [1, 2]. Considering the light loss in the case being times lower in LEDs, the overall energy efficiency is twice as much as those reached by the fluorescent lamps and even more efficient in comparison with other conventional light sources. Other overcoming property of the LEDs are the typically five to fifty times longer life and there are no sudden drops of functionality during the exploitation time. When properly designed and operated for tens of thousands of hours (over 50,000 hours) LED reduces the output light by about 30% (typical parameter of lighting equipment of this type - L_{70}) [1,2]. LED's luminous flux can be adjusted easily within a wide range (dimming) which is a great convenience for operation.

Important advantage of LEDs lighting sources is the ability to obtain desired spectral characteristics of the luminous flux by combination of different types of LEDs. Thus one can produce light sources with a desirable correlated color temperature, color rendering index, and optimal spectral characteristics for various industrial applications - as lighting for growing different species of animals, greenhouses, etc. [1 ÷ 10].

It should be noted that the main advantages of LED lighting can be realized only if proper design is made and proper operation during lifetime is ensured. About 75% of electricity energy consumed by the LEDs is dissipated in the form of heat [1, 2]. This heat must be removed from the area of the p-n junction where it is generated and must be dissipated in environment. The successful resolution of this problem is the main condition for ensuring reliability and long life of lighting equipment. Increase in the temperature of the p-n junction leads to decrease in luminous efficacy of LEDs and reduction of their life (L_{70}). The above data on the life and light efficiency of LED lighting can be realized only if the temperature of p - n junction during operation doesn't exceed 80°C. The aim of this work is to design and test energy efficient light source with spectral characteristics suitable for use in illumination of various types of greenhouses.

II. PROBLEM STATEMENT

Photosynthesis is a complex process that includes more than 30 types of chemical reactions. Photosynthesis pigments play major role as the primary photons acceptors and support further conversion of chemical energy. All pigments can be divided into 4 types: chlorophylls, carotenoids, phycobilins, anthocyanins.

Chlorophyll is green pigments found in leaves in 1818 by Peletier and Kaventon. It takes a crucial part in photosynthesis - absorbs sunlight and converts it in energy of the chemical bonds in the organic compounds which are synthesized in the process. There are 5 types of chlorophyll: chlorophyll A (with cyan); Chlorophyll B (green-yellow); Chlorophyll C and chlorophyll D - in red and brown algae; bacteriochlorophyll - in sulfur, nonsulfur, purple and green bacteria. Chlorophyll absorbs light selectively - spectral characteristics are shown in Figure 1 [3-9].

The most intensive photosynthesis takes place in the red and violet-blue region of the spectrum - Fig. 1 [3 ÷ 10]. In the process of evolution plants have adapted to absorb those rays of the spectrum whose energy is the most effective in photosynthesis. The intensity of each photochemical reaction is determined not by the amount of energy absorbed but by the number of ingested quanta.

Carotenoids - yellow or orange colored pigments, that constitute 98% of the yellow pigments in the photosynthetic apparatus of higher plants. They also have selective absorption spectral characteristics (Fig. 1a). Phycobilins - contained in the sea red cryptophyta algae (phycoerythrin), cyanobacterias and some blue-green algae (phycocyanin). They transmit absorbed light quanta to chlorophyll in yellow-green spectrum, so seaweeds can absorb light energy far deep in the ocean. Anthocyanins -

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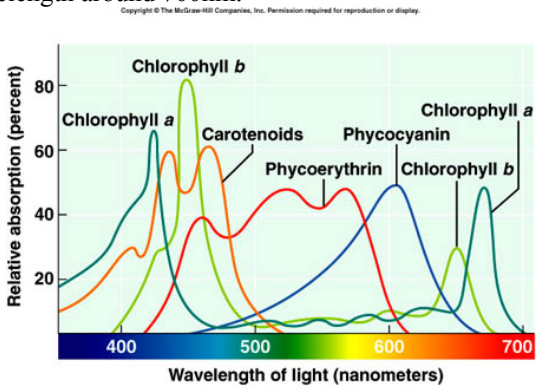
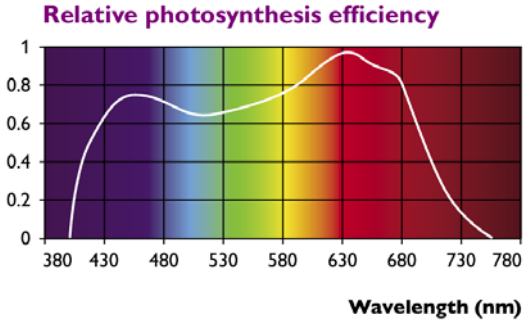
water-soluble pigments located in the cytoplasm. They stained plant parts in purple, red, brown in autumn and at low temperatures.

Energy quanta in the red region of the spectrum is lower, so the same amount of energy absorbed by the red rays is produced by greater number of quanta compared with blue-violet rays. There may be a quantum with so little energy that it is not sufficient for inducing chemical effect. This means that when photochemical reactions there is a threshold limit of quantum energy in which responses are impossible i.e. there is an upper limit to the length wavelength around 700nm.



a)



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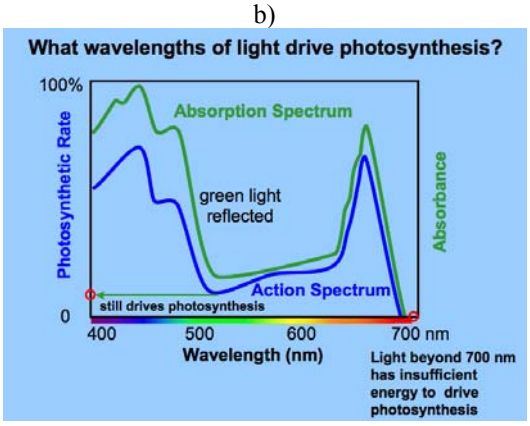

c)

Fig. 1. Spectral characteristics: a) plant pigments, b) and c)-photochemical efficiency [8, 9, 10].

The efficiency of energy conversion of light into chemical energy in plants is estimated between 3 and 6%. The actual efficiency of the photosynthesis (between 0.1 and 8% [3 ÷ 10]) varies considerably with changes in light spectrum, light intensity, temperature and carbon dioxide concentration.

As can be seen from Fig. 1b, and Fig. 1c various authors present a somewhat different characteristics for the effectiveness of the process of photosynthesis; the most effective is radiation in the blue and the red part of the spectrum.

The main goal of this work is design of energy effective LED lamp module with spectral power distribution (SPD) of the radiant flux corresponding to the spectral photosynthesis efficiency.

III. EXPERIMENTAL

Used LEDs are XLamp XPC series produced by CREE Inc. There are several reasons for this choice: they have good exploitation properties [2]; in this series white LEDs are available with color temperatures in a wide range - from 2600K to 10000K; a range of colored LEDs required to achieve the objectives set are also available. All LEDs can operate with the same power supply that is essential advantage. In current study all LEDs are powered by a constant current source. White LEDs operate at currents of 350 mA; for colored LEDs forward current is changed from 100 mA to 350 mA.

The spectral characteristics of LEDs being used are determined experimentally with spectrophotometer of the company StellarNet-Inc and are presented in Fig. 2 and Fig. 3.

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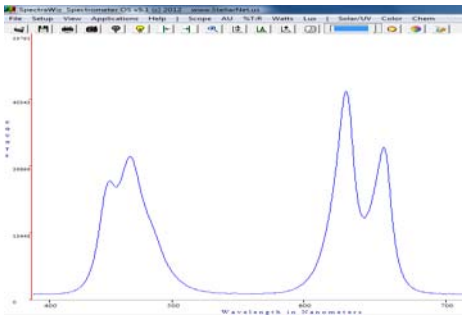

Fig. 2. LEDs' spectral characteristics (from left to right): royal blue (XPCROY), blue (XPCBLU), red (XPCRED) and deep red (HPL).

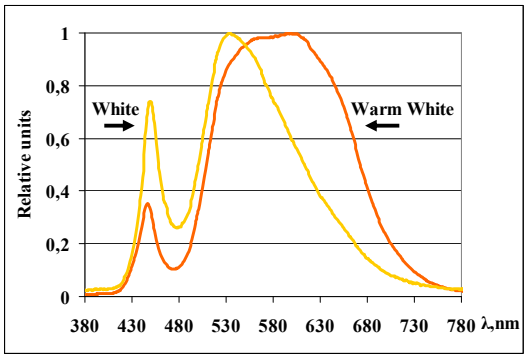

Fig. 3. LEDs' spectral characteristics (from left to right): neutral white (XPC) and warm white (XPC).

During experimental investigations three warm white LEDs (XPC), three neutral white LEDs (XPC), one blue LEDs (XPCBLU); one royal blue LED (XPCROY), one red LED (XPCRED), and one deep red LED (HPL) are used. All LEDs are soldered to circuit boards with metal

core (MCPCB) and mounted on aluminum heatsink with thermal resistance between the heat sink and the ambient environment $R_{th\ hs\text{-}a}$ = 1ºC/W.

In Fig. 4 a photo of the LED module is presented.

Fig. 4. Realized lamp module with one warm white, three neutral white; one blue, one royal blue one red and one deep red LEDs.

IV. Experimental Study on Spectral Characteristics

At the first stage of experimental investigations (module 1) all white LEDs operate at 350 mA current and the current of colored LEDs is changed between 100 mA and 350 mA. Spectral characteristic of the module's 1 luminous flux is shown in Fig.5.

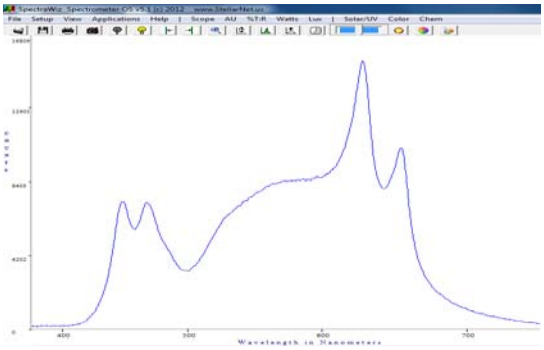

Fig. 5. LEDs' spectral characteristics: three warm white LEDs at 350mA; royal blue (XPCROY), blue (XPCBLU), red (XPCRED) and deep red (HPL) at 200mA.

The nominal drive current for color LEDs is 350 milliamps; when they operate at low current are not fully exploited; the energy efficacy of the LED module is decreased. Therefore, during further investigations all LEDs are connected in series and operate at 350 mA current. The number of warm and neutral white LEDs and their ratio is changed to achieve the desired spectral power distribution.

During experiments the following combinations are used:

- Always one blue, one royal blue, one red and one deep red LEDs;
- Three warm white LEDs; - three warm white and one neutral white LEDs; two warm white and two neutral white LEDs; one warm white and three neutral white LEDs; three neutral white LEDs. Some of spectral characteristics of different LED modules are shown in Fig. 6 and Fig.7.

The decisive criterion for the successful implementation of our objective is the appropriate spectral characteristics of the luminaire - similar to those shown in – Fig. 1 [8 ÷ 10].

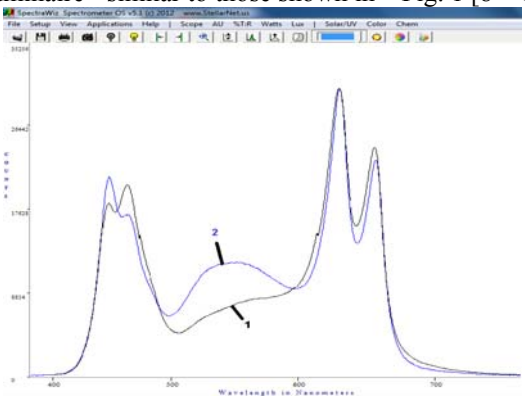

Fig. 6. Comparison between SPD of two variants of the LED module: 1 - three warm white, one blue, one royal blue, one red and one deep red LEDs; 2 - three neutral white, one blue, one royal blue, one red and one deep red LEDs.

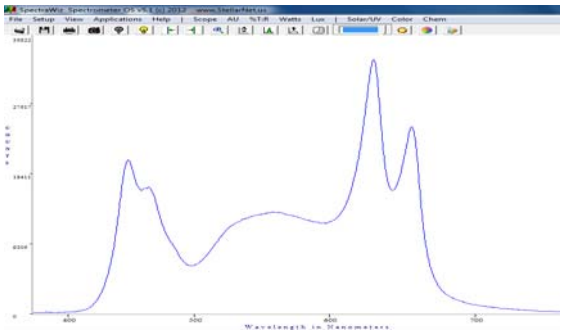

Fig. 7. Spectral characteristics of the LED module: two neutral white, two warm white, one blue, one royal blue, one red and one deep red LEDs.

Comparison between spectral power distribution of luminous flux of LED module (three neutral white, one blue, one royal blue, one red and one deep red LEDs), and the desired SPD [8] is shown in Fig. 8. The result clearly shows that spectral characteristics of the constructed lamps are suitable for its use in the process of photosynthesis for plants of various kinds.

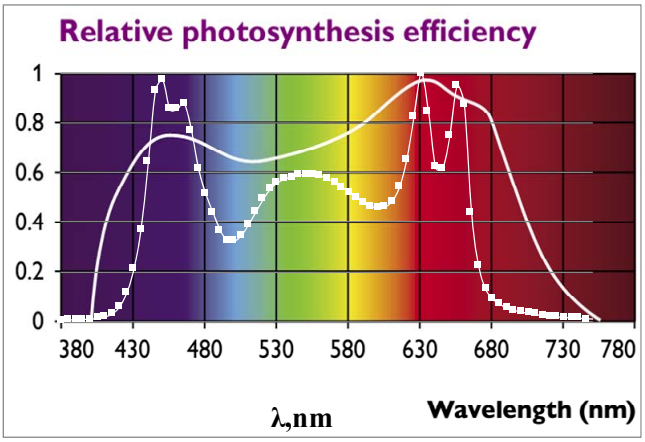

Fig. 8. SPD of LED module (three neutral white, one blue, one royal blue, one red and one deep red LEDs, which spectrum is shown in Fig. 6, curve 2), compared to the relative photosynthesis efficiency [8].

V. THERMAL MANAGEMENT

For the evaluation of thermal loads at different environmental conditions the LED modules are placed in a thermal chamber. The temperature in the chamber is gradually changed from 20°C to 45°C. Studies were carried out at constant current through the LEDs 350 mA.

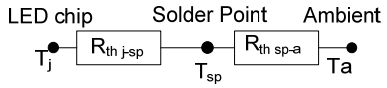

Fig. 9. Schematic diagram of the thermal resistances in the heat flow path from the p-n junction to the ambient environment; Temperature notations are as follows: Tj – temperature of p-n junction; Tsp - temperature of solder point; Ta - ambient temperature; Rth j-sp and Rth sp-a - thermal resistance between the p-n junction and solder point and between the solder point and the ambient.

The temperature distribution of the different LEDs under different operating conditions was assessed by measurement using thermocouples installed in accordance with the producer recommendations [1]. Most convenient way for investigating the temperature regimes for all the LEDs is the infrared thermography. Fig. 10 shows infrared image of the LED lamp (shown in Fig. 4) in the heating chamber, using thermography measurements taken with an infrared camera ThermaCam E300 - FLIR-Systems.

Using obtained experimental data for the temperature of the solder point (T_{sp}) the thermal loading of the LEDs is estimated by calculating the temperature of the p-n junction T_j using (1).

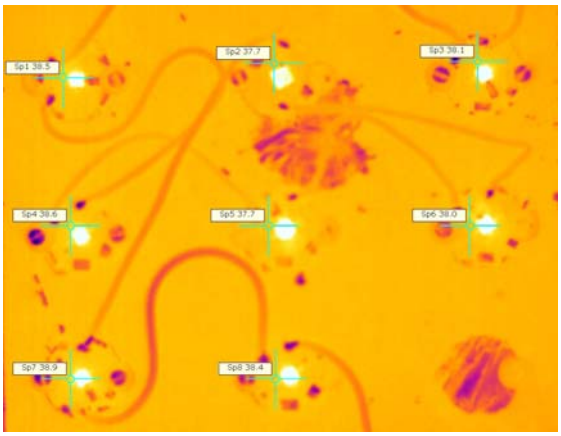

Fig. 10. A study of temperature distributions on LEDs cases using infrared thermography; ambient temperature is 35 ° C.

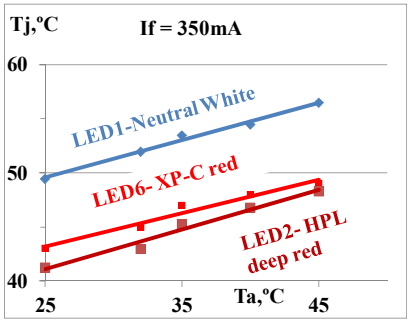

Fig. 11. XPC – White, blue, red and deep red LEDs' p-n junction temperature (**Tj**) in dependance of the ambient temperature (**Ta**).

$$T_j = T_{sp} + R_{th\ j\text{-}sp} * P_{LED} \quad (1)$$

The thermal resistance between the p-n junction and solder point $R_{th\ j\text{-}sp}$ is given by the manufacturer: for XLamp XPC – White and blue, $R_{th\ j\text{-}sp}$ = 12 K/W; for red LEDs $R_{th\ j\text{-}sp}$ = 10 K/W; for deep red LEDs $R_{th\ j\text{-}sp}$ = 5 K/W.

In Fig. 11 the calculated junctions' temperatures of LEDs during operation at different ambient temperatures are shown.

The results show that the operating modes of the LEDs in designed modules are far from the dangerous temperatures of the p-n junction (over 85°C). This ensures smooth operation and long life of the lamp. From the other hand it allows an industrial production LEDs to be soldered on a common circuit board and to reduce the size of the cooling radiator.

VI. CONCLUSION

LED modules for industrial applications in horticulture are designed and tested. Performed experimental studies show that the spectral features are suitable for the cultivation of a wide class of plants. The operating temperatures of the LEDs ensure smooth operation and long life of the developed equipment. Used light sources and their power supply can provide very good energy efficiency at relatively low cost of lighting equipment.

ACKNOWLEDGEMENT

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Energy Effective LED Module for Poultry Lighting

Petko Hristov Mashkov, Berkant Seydali Gyoch, Tamara Grigorievna Pencheva, Hristo Ivanov Beloev and Rostislav Yuriev Kandilarov

Abstract – **The aim of this work is design and thermal management of energy effective LED module for poultry lighting. The spectral sensitivity of fowls differs significantly from that of humans and primary objective of this work is to match as close as possible the spectral power distribution of artificial light source to the spectral characteristics of the poultry vision. In different stages of growth of poultry adequate illumination of premises varies very widely. Therefore essential requirement to luminaires for such purposes is the possibility of their luminous flux to be dimming over a wide range while retaining its spectral distribution. These tasks have been successfully resolved in the designed module by selecting the appropriate LEDs and management regimes. Proper thermal management ensures safety regimes of operation of the LED module even at heaviest ambient conditions (temperatures up to 45ºC).**

Keywords – **LEDs' thermal management, poultry lighting, power LEDs**

I. INTRODUCTION

Current trends in the design of lighting equipment are related with making sources with continuous spectrum, similar to that of the sun. This is appropriate when it comes to humans needs lighting, natural circadian rhythm maintaining and true color reproduction [1-7]. For a number of industrial applications the use of specialized light sources, whose spectral and power characteristics are consistent with the characteristics of the illuminating object, is much more efficient. It is known [1, 2] that the poultry eye's spectral sensitivity differs significantly from the human one – Fig. 1.

Spectral characteristics of the most popular light sources in the recent past (incandescent and fluorescent) differ significantly from the optimal for chicken farms, as it can be seen in Fig. 2 and Fig. 3 [4].

Dimming these light sources is problematic and further reduces their energy efficiency. In contrast dimming of LED light sources is easy to implement and allows the management of their luminous flux widely with minor decrease of luminous efficacy.

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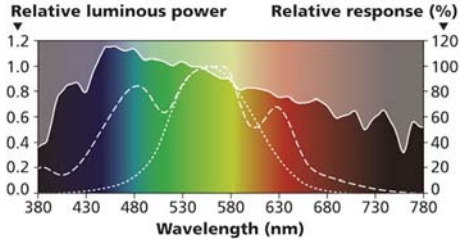

Fig. 1. Fowl (dashed) and human (dotted) spectral sensitivity, compared to sunlight spectrum (solid line) at noon [4].

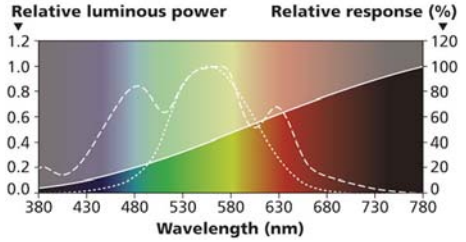

Fig. 2. Fowl (dashed) and human (dotted) spectral sensitivity, compared to incandescent spectrum (solid line).

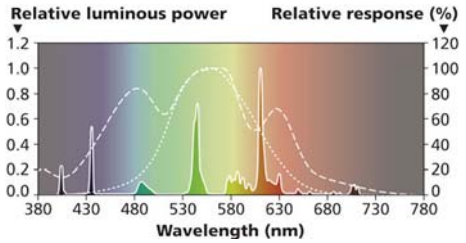

Fig. 3. Fowl (dashed) and human (dotted) spectral sensitivity, compared to fluorescent spectrum (solid line).

Application of LEDs with appropriate spectral and power characteristics enables the creation of light sources with characteristics very close to optimum. Advantages of LED lighting equipment allows solving very important problems in poultry farming because illumination affects directly poultry growth, amount of feed being consumed, maturation, reproduction, sexual activity, behavior, egg production, aggression, feather picking, etc [4 - 7].

II. PROBLEM STATEMENT

LEDs' properties allow creation of light sources with optimal characteristics considering variety of luminarie features appropriate spectral distribution of the radiation, resistant to external influences, long operational life, possibility of dimming light flux over a wide range, etc.

Domestic fowl have enhanced sensitivity to green (peak at 550 nm), reds (peak at 640 nm), blues (peak at 450 nm) and ultraviolet (peak at 385 nm) light Fig. 1.

The major task in the creation of light sources for poultry is the selection of LEDs with appropriate spectral and power characteristics. There is not a single solution; the criteria for selection may diverse.

In the literature some solutions are known – [4, 5, 6], without mentioning what type and how many LEDs are being used – Fig. 4a, 4b.

A significant problem in the use of these light sources is connected with the control of their luminous flux. In various stages of development birds need different levels of illumination, and the differences are big.

As it can be seen from Fig. 4a and Fig.4b some problems can occur at dimming – spectral characteristics of lamp's luminous flux are changed and move away from the optimal spectral distribution.

That's why the other important task is to choose the proper power source for LED lamp and the manner of dimming.

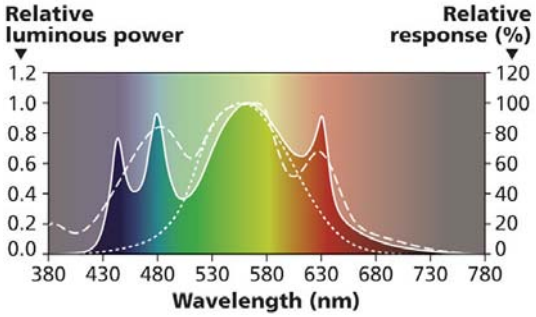

Fig. 4a. LED lamps' characteristics compared to desirable spectral characteristics for poultry housing [6].

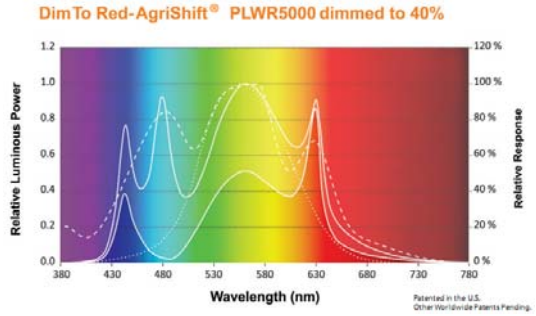

Fig. 4b. LED lamps' characteristics compared to desirable spectral characteristics for poultry housing [6].

As housing for poultry are not air-conditioned another important stage in the design is connected with the correct thermal management of the LED lamp. It is necessary ensuring trouble free operation and long life at ambient temperatures up to 50°C.

III. Experimental Results

3.1. Selection of LEDs with suitable characteristics to achieve the goals of development.

Analysis of the possibility of obtaining the desired spectral composition (suitable as a solution to the goals set above) by combining different types of LEDs based on the data specified by the manufacturer is done. A combination of LEDs suitable for achieving the desired SPD (spectral power distribution) is chosen - LEDs XLamp XTE, XPC and XPE family, CREE Inc. There are several advantages in the selection of LEDs of one type - electrical characteristics are similar, thermal resistance and the thermal loads during operation are close, dimming and thermal management are easier. The combinations of warm white, neutral white, blue and red LEDs are used for design of the experimental module.

Some of electrical and thermal characteristics of used LEDs are presented below:

- Thermal resistance between junction and solder point $R_{th\ j\text{-}sp}$:

for white LEDs $R_{th\ j\text{-}sp} = 12°C/W$; blue LEDs $R_{th\ j\text{-}sp} = 12°C/W$; for red LEDs $R_{th\ j\text{-}sp} = 10°C/W$ [1].

- Forward voltage at nominal current:

$U_F = 2.2V$ for red LEDs; $U_F = 3.3V$ for blue LEDs; $U_F = 3.2V$ for white LEDs [1].

All LEDs are powered by a constant current source.

All of LEDs are soldered on MCPCBs with thermal resistance solder point – heat sink $R_{th\ sp\text{-}h} = 1°C/W$ [1].

Experimental equipment for spectral measurement of Stellar Net Inc is used.

3.2. Experimental results - spectral power distribution (SPD) of the LED modules.

Some experimental LED modules for poultry housing are realized and tested. Proper spectral characteristics are achieved for these modules:

1 - The first module contains three warm white (XTE), two neutral white (XPC), two blue (XPE), and one red (XPC) LEDs; all LEDs are connected in series and operate at 350 mA constant current. Spectral power distribution (SPD) of the luminous flux of this module is shown in Fig. 5.

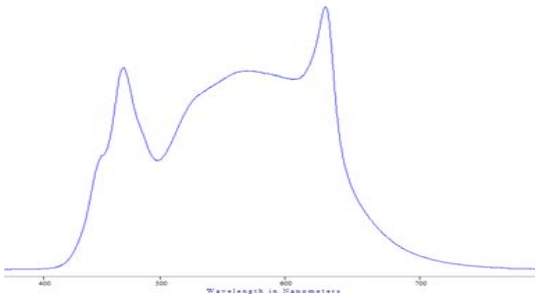

Fig. 5. SPD of the first LED module's luminous flux for poultry housing.

2 - The second module contains two warm white (XTE), three neutral white (XPC), two blue (XPE), and one red (XPC) LEDs; all LEDs are connected in series and operate at 350 mA constant current.

Fig. 6. Photo of the second LED module for poultry housing.

Spectral power distribution (SPD) of the luminous flux of this module is shown in Fig. 7.

In Fig. 6 a photo of the LED module is presented.

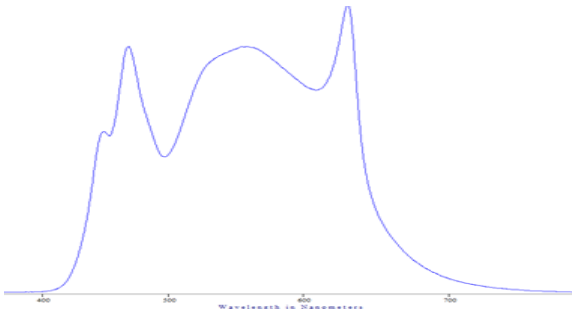

Fig. 7. SPD of the second LED module's luminous flux for poultry housing.

SPD of the second module's luminous flux, compared to the desirable SPD for poultry housing [6, 7] is shown in the Fig. 8.

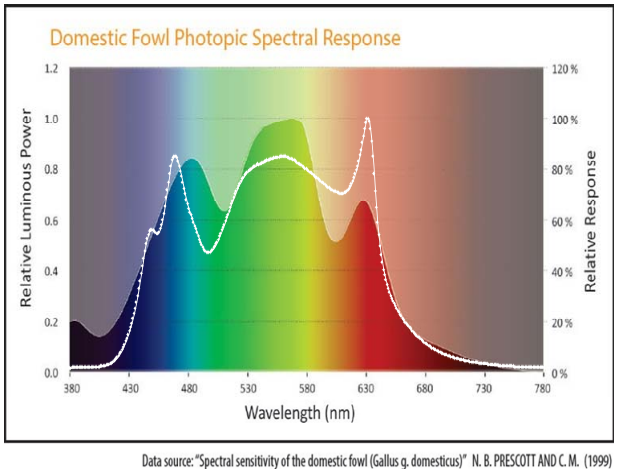

Fig. 8. Spectral power distribution of the second module's luminous flux (white line), compared to the desirable SPD for poultry housing [6, 7].

As it can be seen SPD of the LED module's luminous flux is very close to the desired SPD.

Adequate illumination of premises varies widely in dependence of the stage of poultry growth. Therefore essential requirement to luminaires for such purposes is the possibility for their luminous flux to be dimmable over a wide range while retaining its spectral distribution. As it can be seen in Fig. 4b, it may be potential problems at dimming - spectral characteristics of luminous flux can change.

The essential advantage of driving LEDs by constant current supply is possibility to dim luminous flux widely at unchanged form of the SPD.

As it can be seen in Fig. 9 at dimming to 80%, 60%, 40% and 30% the SPD of luminous flux of the second module remains unchanged.

As can be seen from Fig. 8 and Fig. 9 the achieved spectral characteristics are suitable and are very close to optimal for poultry lighting. The shape of the spectral characteristics is not altered by dimming, which is a significant advantage for adjusting the desirable value of illuminance in the poultry housing.

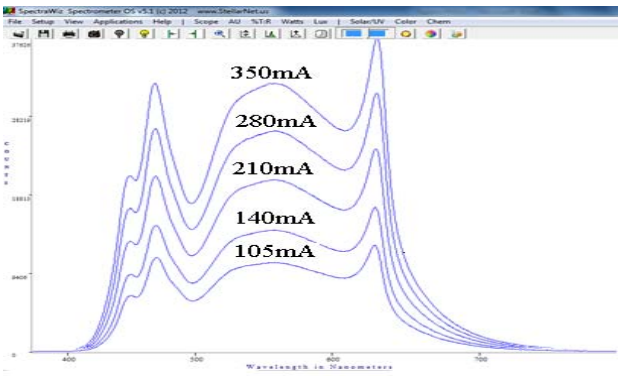

Fig. 9. Spectral power distribution of the second module at dimming to 80% (280mA), 60% (210mA), 40% (140mA) and 30% (105mA).

3.3. Thermal management.

Thermal resistance model, described in [1], is used, Fig. 10.

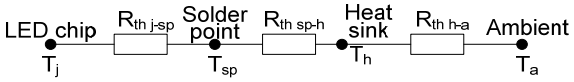

Fig. 10. Thermal resistance model [1]:
$R_{th\ j\text{-}sp}$- thermal resistance from junction to solder point;
$R_{th\ sp\text{-}h}$- thermal resistance solder point - heat sink;
$R_{th\ h\text{-}a}$- thermal resistance heat sink - ambient; T_j, and T_{sp}, - junction and solder point temperatures.

Experimental investigations of solder points' temperature distributions at different operating currents and different ambient conditions are achieved using an infrared camera, ThermaCam E300 – FLIR Systems and corresponding junction temperatures are calculated, equation (1) [1]:

$$T_j = T_{sp} + R_{th\ j\text{-}sp} * P_{LED} \quad (1)$$

P_{LED} is the power of one LED chip:

$$P_{LED} = I_F * U_F; \quad (2)$$

The heat sink with thermal resistance about 1.5°C/W is used. The choice was made because of the shape of the cooling radiator, which serves as the body of the lamp and ensure hermetic isolation of LEDs from the environment.

Experimental investigations of LEDs' thermal loading.

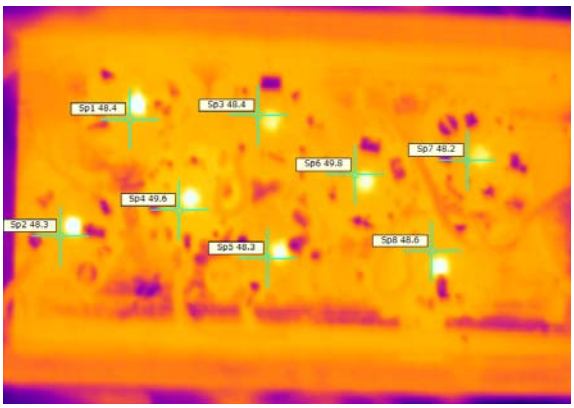

Fig. 11. IR photo of the LED module; solder points' temperatures distributions.

The main results for different type of LEDs at maximum operating currents are presented below – Fig. 12 – Fig. 14.

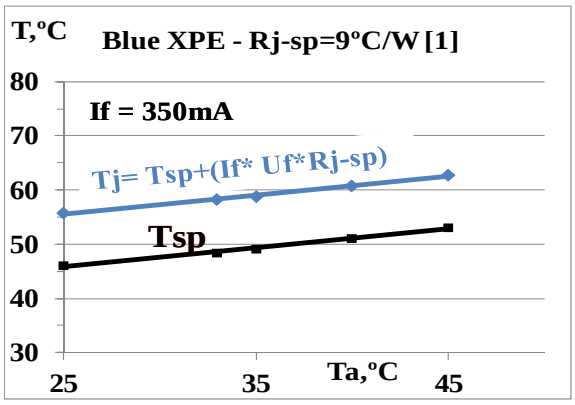

Fig. 12. Solder point's temperature Tsp (measured) and junction temperature Tj (calculated) dependences on temperature of the ambient air Ta for the blue XPE LED.

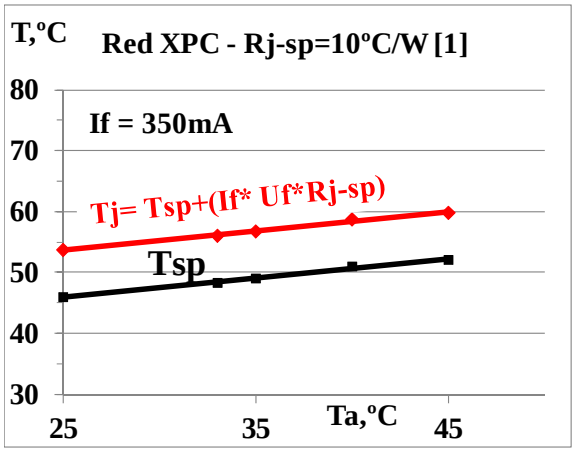

Fig. 13. Solder point's temperature T_{sp} (measured) and junction temperature T_j (calculated) dependences on temperature of the ambient air T_a for the red XPC LED.

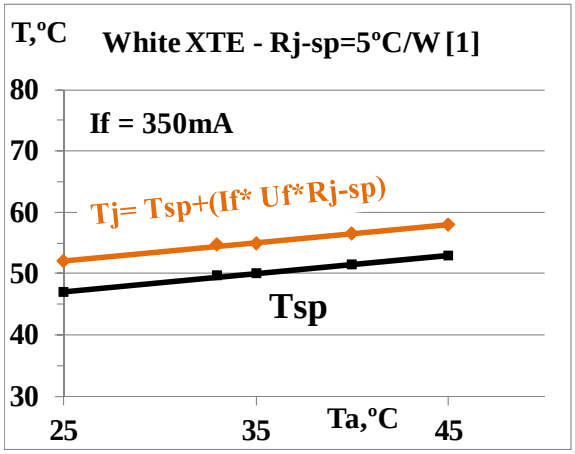

Fig. 14. Solder point's temperature T_{sp} (measured) and junction temperature T_j (calculated) dependences on temperature of the ambient air T_a for the white XTE LED.

The results presented in Fig. 12 – Fig. 14 shows that the operating temperatures of the LEDs are far from dangerous which provides reliable operation and long life of the developed lighting equipment.

IV. Conclusion

LED module for illumination of poultry houses is designed and produced. A particular combination of LEDs is selected in order to achieve a close match between the spectral distribution of the lamp and the eye sensitivity of different types of domestic fowl. Spectral power distribution of the designed luminaire is very close to the optimal spectrum, recommended in literature. Proper choice of LEDs ensures good energy efficiency of the luminaire and allows easy dimming.

Acknowledgement

The National Science Fund, Ministry of Education and Science of Bulgaria, is gratefully acknowledged for the financial support of research project DFNI – B02/2 12.12.2014 (Int. № FNI B 02/75).

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Dependencies between Basic Timing Parameters in Image Processing System

Tsvetomir Nikolov Lazarov

Abstract – **This paper presents the dependencies between the basic timing parameters that define the processing of a pixel from image generated by a matrix image sensor. The ratio between pixel clock frequency and the time required for one pixel processing determine system parameters like frame rate, system clock frequency, the choice of processing algorithms, achievable accuracy. Here are presented several configurations of image processing system and opportunities through which it is possible to relax the timing requirements to the system and to make its design process more flexible.**

Keywords – **image processing system, frame rate, clock frequency, processing cycles, parallel processing.**

I. INTRODUCTION

The main component of image processing system is the processing block. It contains a set of elements that implement different operations over the individual pixels, groups of them or over the entire frame. The type of these elements and the connections between them depend on the current application and the utilized hardware-software platform. The frames generated by the image sensor are transferred serially to the processing block. This fact allows implementation of conveyor processing of the pixel data flow (Fig.1). Each processing element (PE) executes one certain function over a portion of the input data and than sends the result to the next PE. All elements of the processing block are synchronized to the main system clock frequency F_{SYS}.

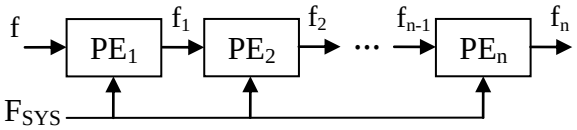

Fig.1. Data flow processed by conveyor

The conveyor type of data processing structure requires nonstop data execution and guarantied lack of data loss. In order to satisfy this requirement, every PE should complete the processing of the current portion of data before the arrival of the next one. Duration of the time interval that every PE requires for execution of its specific function varies upon the different functions and it is in direct relation to the PE clock frequency.

In the following paper, several possible configurations of image processing system are presented and for every one of them the dependencies of the basic timing parameters are defined.

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II. TIMING PARAMETERS DEPENDENCIES

At fig.2 a single PE is presented with its main connections. The data that is to be processed (f) comes from the image sensor or from the previous PE. The result (f_{PE}) is transferred to the next PE when the function is completed. The clock frequency of the PE (F_{PE}) is derivative of the system clock frequency FSYS, but it is not obligatory that all PE work with same F_{PE} – if it is possible to adjust the individual F_{PE} of every PE, the designer gets a great flexibility during the system design and configuration.

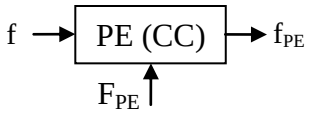

Fig.2. Processing element

Time duration for one pixel processing (T_{PP}) is proportional to the period of the PE clock signal and the total number of clock cycles (CC) needed for completion of the certain function:

$$T_{PP} = CC \times T_{PE} = \frac{CC}{F_{PE}} \quad (1)$$

Formula (1) is basic point that manifests the opportunities to gain additional flexibility during the design and the configuration of the image processing system. If one of the product components or both of them are changed, some main topics could be settled:

- Pixel processing duration T_{PP} could be reduced through decreasing of CC by implementing simpler and/or shorter algorithm with eventually less accurate final result;
- In order to get certain required better precision, the implementation of more complex and/or more accurate algorithm will increase T_{PP} along with CC;
- T_{PP} could be changed through increasing or decreasing of clock frequency (F_{PE}) of the PE. Due to the fact that F_{PE} is directly related to the energy consumption, T_{PP} value could be designed with taking this fact into consideration;
- Certain amount of CC increase, caused by algorithm complexity or increased accuracy, could be compensated by proportional increase of F_{PE} and by this keeping T_{PP} constant;
- If simpler and/or shorter algorithm is implemented, the reduced value of CC will allow corresponding reduction of F_{PE} and thus lower energy consumption.

Parameter T_{PP} is in direct dependence on pixel clock signal and the chosen frame processing configuration. Three possible configurations are analyzed and parallel processing of data flow with multiple PE is presented as a forth case.

A. One-Pixel processing configuration

At this configuration the pixels are processed at the time of their arrival. Duration of one pixel processing T_{PP} should be less or equal to the time of next pixel arrival, which is indeed the period of the clock signal that gets the pixel from the image sensor:

$$T_{PP}^{P} \leq T_p = \frac{1}{F_p} \quad (2)$$

From formulas (1) and (2) follows

$$T_{PE}^{P} \leq \frac{T_p}{CC} \quad (3.1)$$
$$F_{PE}^{P} \geq CC \times F_p \quad (3.2)$$

which means that the clock frequency of the processing element should be at least CC-times greater than the frequency pixel arrivals at that element. If this is not true, there have to be some buffering for the pixels that leads to the next configuration.

B. One-Row processing configuration

This configuration take advantage of the fact that at every transferred row there is additional time period (Horizontal Blanking, T_{HB}) after the last pixel of that row. The total amount of time needed for processing of all the pixels (M) from one row at certain PE should be no greater than T_{ROW}:

$$M \times T_{PP}^{L} \leq T_{ROW} = M \times T_p + T_{HB} = (M + P_{HB}) \times T_p \quad (4)$$

Time for one pixel processing in this configuration is

$$T_{PP}^{L} \leq \frac{T_{ROW}}{M} = \frac{M+P_{HB}}{M} * T_p = \frac{T_p}{\alpha} = \frac{1}{\alpha \times F_p} \quad (5)$$

where $$\alpha = \alpha_N = \frac{M}{P_R} = \frac{M}{M+P_{HB}} < 1 \quad (6)$$

The coefficient α represents that part of T_{ROW} during which the current row pixels are received at PE. It is analogue of the digital signal parameter "duty cycle".
From formulas (1) and (5) follows

$$T_{PE}^{L} \leq \frac{T_p}{\alpha \times CC} \quad (7.1)$$
$$F_{PE}^{L} \geq \alpha \times CC \times F_p \quad (7.2)$$

Formulas (7.1) and (7.2) show that due to the addition of the horizontal blanking period to the whole row processing duration (α<1) the requirements to the PE are relaxed in comparison to One-Pixel processing configuration. This is advantage that could be used in one of the following cases:

- Increasing CC (allows utilizing function that requires more clock cycle for completion) while keeping T_{PE} and T_p the same;
- Decreasing PE clock frequency F_{PE};
- Increasing pixel frequency F_p , hence increasing frame rate (if image sensor is capable of this);
- Some combination of previously mentioned actions on condition that (7.1) and (7.2) are not violated.

This configuration (T_p<T_{PP}<T_{ROW}/N) requires FIFO buffer to store the arriving row pixels while they are waiting their turn for processing (fig.3). Its volume should be large enough to prevent data loss, but adequate memory usage is also a factor that determines the size of the buffer. Having these into consideration, calculation of B_{ROW} is made in order to find the minimal value that is enough to hold the maximum possible number of row pixels.

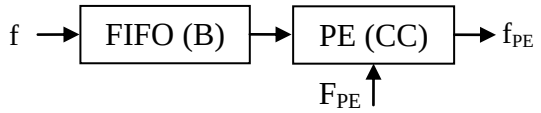

Fig.3. Processing element with FIFO buffer

The buffer should be emptied at the beginning of the next row and if this is not the case, there will be accumulation of waiting pixels that increases with every row. When the frame includes many rows the queue becomes enormous and requires buffer with significant size. This situation is described in the next system configuration. Pixel accumulation starts with the first pixel of the current row and continues until the last one from this row is received. At the same time goes extraction of elements in the head of the FIFO buffer and their processing by PE and by this feeing space for new pixels. The size of the buffer is determined by the number of pixels that could be processed during the horizontal blanking – time interval in which extraction from FIFO continuous and no new pixels are added. All the other elements should be processed before the start of T_{HB}. Total duration of processing the remaining pixels in the FIFO during horizontal blanking is

$$T_{BUF} = T_{PP}^{L} \times B_{ROW} \leq T_{HB} \quad (8)$$

From the limitation (8) and formula (5) follows

$$B_{ROW} \leq \frac{T_{HB}}{T_{PP}^{L}} = \frac{P_{HB} \times T_p}{\frac{T_p}{\alpha}} = \alpha \times P_{HB} \quad (9)$$

C. One-Frame processing configuration

When PE is not capable of processing the entire row during the T_{ROW} period, system configuration with larger FIFO buffer should be used. It uses the additional time slot in the frame (Vertical Blanking, T_{VB}) to deal with the remaining content of this buffer. All pixels from one frame of N rows and M columns (total number of NxM pixels) should be processed for the total time less than T_{FRAME} :

$$N \times M \times T_{PP}^{F} \leq T_{FRAME} = R_F \times T_{ROW} = R_F \times P_R \times T_p \quad (10)$$

where R_F (Rows-pr-Frame) is the duration of the frame in rows and P_R (Pixels-per-Row) is the duration of one row in pixels. Time duration of one pixel processing is

$$T_{PP}^{F} \leq \frac{T_{FRAME}}{N \times M} = \frac{R_F \times P_R}{N \times M} * T_p = \frac{T_p}{\alpha_N \times \alpha_M} = \frac{T_p}{\beta} = \frac{1}{\beta \times F_p} \quad (11)$$

where $\alpha_N = \frac{N}{R_F} < 1$ (12)

$\beta = \alpha_M \times \alpha_N < \alpha$ (13)

The coefficient β is the frame "duty cycle", i.e. it represents that part of T_{FRAME} during which the frame pixels are received. From formulas (1) and (11) follows

$T_{PE}^F \le \frac{T_p}{\beta \times CC}$ (14.1)

$F_{PE}^F \ge \beta \times CC \times F_p$ (14.2)

Formulas (14.1) and (14.2) show that the time requirements to the PE are relaxed in comparison to the other two processing configurations, because β<α<1. Parameters CC, F_{PE} and F_p could be managed to the desired direction in a greater degree compared to the previous configuration.
The size of the FIFO buffer that contains the waiting frame pixels, is defined by the maximum number of pixels that could be processed during the time of frame blanking T_{FrB} (from the moment in which the last frame pixel is received in the FIFO to the arrival of the first pixel from the next frame). Time duration of processing the pixels remaining in the FIFO buffer should be

$T_{BUF} = T_{PP}^F \times B_{FRAME} \le T_{FrB}$ (15)

From the limitation (15) and formula (11) follows

$B_{FRAME} \le \frac{T_{FrB}}{T_{PP}^F} = \frac{P_{FrB} \times T_p}{\frac{T_p}{\beta}} = \beta \times P_{FrB}$ (16)

D. Parallel processing configuration

All the thee configurations, described by now use single PE to dial with the entire data flow. If parallel processing structure with multiple (K) PE is implemented, the timing requirements will be significantly enhanced. Every PE will process 1/K part of the data flow and correspondingly the time slot granted to him will be K-times bigger and the required minimum PE clock frequency will be reduced also K-times:

$T_{PE}^{PP} \le \frac{K}{CC} \times T_P$ (17.1)

$F_{PE}^{PP} \ge \frac{CC}{K} \times F_p$ (17.2)

$T_{PE}^{PL} \le \frac{K}{\alpha \times CC} \times T_P$ (17.3)

$F_{PE}^{PL} \ge \alpha \times \frac{CC}{K} \times F_p$ (17.4)

$T_{PE}^{PF} \le \frac{K}{\beta \times CC} \times T_P$ (17.5)

$F_{PE}^{PF} \ge \beta \times \frac{CC}{K} \times F_p$ (17.6)

In case of configuration with FIFO buffers, the total volume is equal to the value defined for a single PE (K=1) case. There could be two different implementations of the FIFO buffer. The first one is presented on fig.4 – one common buffer stores the row (frame) pixel and the distribution to the PE is done after the element extraction from the head of the buffer. The other case makes the separation of the data flow to the individual PE FIFO buffers and the size of each of them is

$B_{ROW}^P \le \frac{T_{HB}}{T_{PP}^{PL}} = \frac{P_{HB} \times T_p}{\frac{K \times T_p}{\alpha}} = \frac{\alpha}{K} \times P_{HB}$ (18.1)

$B_{FRAME}^P \le \frac{T_{FrB}}{T_{PP}^{PF}} = \frac{P_{FrB} \times T_p}{\frac{K \times T_p}{\beta}} = \frac{\beta}{K} \times P_{FrB}$ (18.2)

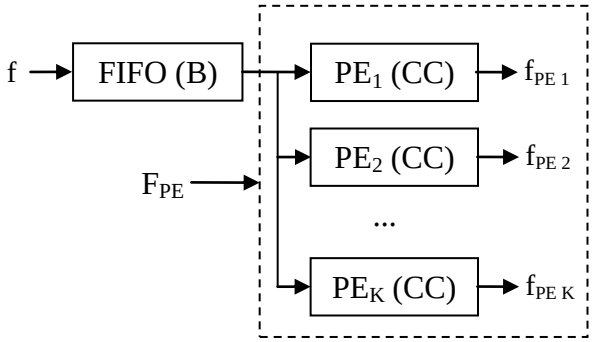

Fig.4. Parallel processing with common FIFO buffer

E. Example

As a example of described configurations a image sensor OV2640 of OmniVision Technologie is analyzed. Fig.5 presents timing diagram of one frame and Table1 includes the basic parameters of the image sensor frame and calculated values of coefficients and buffers sizes for different frame formats.

Table1.Basic parameters of a image sensor frame

Frame format		UXGA	SVGA	CIF
Rows	**N**	1600	800	400
Colums	**M**	1200	600	300
$\mathbf{T_{FRAME}}$	$\mathbf{R_F * T_{ROW}}$	1248	672	336
$\mathbf{T_{ROW}}$	$\mathbf{P_R * T_p}$	1922	1190	595
$\mathbf{T_{HB}}$	$\mathbf{P_{HB} * T_p}$	322	390	195
$\mathbf{T_{VB}}$	$\mathbf{P_{VB} * T_p}$	84890	81310	14398
$\mathbf{T_{FB}}$	$\mathbf{P_{FB} * T_p}$	27193	7415	3707,5
$\mathbf{T_{BB}}$	$\mathbf{P_{BB} * T_p}$	57697	73895	17907,5
$\mathbf{T_{FrB}}$	$\mathbf{P_{FrB} * T_p}$	92578	86070	16778
$\boldsymbol{\alpha=\alpha_M}$	$\mathbf{M/P_R}$	0,8325	0,6723	0,6723
$\boldsymbol{\alpha_N}$	$\mathbf{N/F_R}$	0,9615	0,8955	0,8955
β	$\boldsymbol{\alpha_N * \alpha_N}$	0,8	0,6	0,6
$\mathbf{B_{ROW}}$		269	263	132
$\mathbf{B_{FRAME}}$		74063	51643	14398

III. DISCUSSION

From formulas (3.1), (7.1) and (14.1) it is possible to determine the ratios of the parameter T_{PE} (maximum acceptable time duration for processing one pixel in certain PE) for the different configurations:

$\boldsymbol{T_{PE}^P : T_{PE}^L : T_{PE}^F = 1 : \frac{1}{\alpha} : \frac{1}{\beta}}$ (19)

Formula (19) shows that the available time for one pixel processing is increasing, but additional memory should be allocated for the FIFO buffers. In One-Row configuration their sizes are relatively small, but in One-Frame case they are significant. Despite of this, they are many times smaller than the memory required for a whole frame.

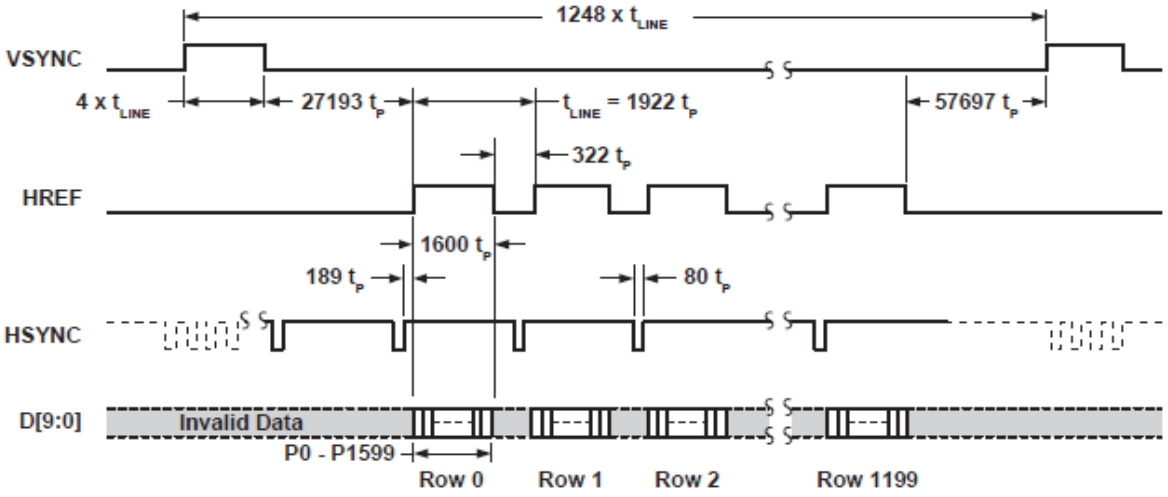

Fig.5 Timing diagram of one frame of OV2640 image sensor

From formulas (3.2), (7.2) and (14.2) it is possible to determine the ratios of the parameter F_{PE} (minimum acceptable clock frequency for a certain PE) for the different configurations:

$$\boldsymbol{F_{PE}^{P} : F_{PE}^{L} : F_{PE}^{F} = 1 : \alpha : \beta} \qquad (20)$$

Formula (19) shows that the required minimum PE clock frequency decreases. This is relaxation of the requirement to the image processing system. Other possible decision is to keep higher F_{PE} and to implement other version of the function that requires more clock cycles for execution, but produces better results.

If One-Frame configuration is implemented, the parameters should be calculated with some safety margin, because after the end of the frame processing, some of the following operations could take place:

- Evaluation of the result from the whole frame processing – some functions, for example statistical functions, consider the information from all frame pixels;
- Evaluation and/or additional processing of the information extracted from the frame
- Image sensor configuration adjustments for the next frames.

Presented analysis is build on the assumption that the PE can deal with only one pixel at any given time. If the processing function allows some form of decomposition and rearrangements toward conveyor-type structure that could handle more than one pixel at a time, than the calculations for this PE should be adjusted to the new structure.

Other important assumption was that the pixel data flow is transferred from the image sensor in TV standard frames. A possible example of different data transfer is the usage of the internal output buffer of the image sensor – in this case the pixels are outputted at regular intervals and there are not horizontal and vertical blanking periods. Another case is when data it transferred through some high speed serial interface. If the real image processing system does not work with TV-type frames, only One-Pixel configuration should be considered in single PE or multiple-parallel PE versions.

IV. Conclusion

Presented dependencies of the basic timing parameters allow quick and easy evaluation of the PE of a image processing system and detection of potential possibilities for system adjustment and enhancement. By individual configuration of the different PE it is possible to achieve a good balance between the system requirements – energy consumption, frame rate, result accuracy.

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New Two-wavelength, Transversally Laser- pumped Laser with Improved Spatial Structure

Margarita Angelova Deneva

***Abstract* – We propose a new solution of transversal, one-side laser pumped two-wavelength laser. The proposed laser solution has as main and essential advantage the assurance of natural intensity symmetry in generated beam cross section and the facilitation of strong low-transversal mode emission – for the case of strongly non-homogeneous pumping. We present the principle, the theoretically treatment with computer analysis and also carry out basic experimental tests of our proposal.**

***Keywords* –** two-wavelength laser, side pumped, radial homogeneous generated beams

I. INTRODUCTION

Laser light with two independently tunable wavelengths is basis for many practical methods and devices. The most important of them are: the differential absorption spectral technique for study the presence and concentration of a given substance in complex mixtures; in nonlinear mixing of two wavelengths to produce their sum and difference wavelengths; in metrology; in holography. Essential practical application is the LIDAR technique for remote sensing and control of atmospheric components, especially of the undesired pollutants such as NO_2, SO_2 [1]. The intuitive way to obtain the two wavelength laser light is to superimpose or to use in different manner the emission of two separated lasers. However, the essential drawback is that such realization needs two lasers – optics, mechanics, pumping and involves the usage of complex systems for synchronization of two nanosecond emissions. The output power P_{out}, being generally proportional to the difference between the maximum P_{pump} and the threshold P_{th} pumping power respectively [3], will decrease if such division is used (following the ratio $P_{out} \sim (P_{out}/P_{th})$-1, e.g. for operation at pumping power three times exceeding the threshold, the decrease of the output power is 2 times).

A well established, cheaper and effective way to obtain laser light at two wavelengths is to use a single laser in regime of generation of two (or more) output beams at different wavelengths, the so called two–wavelength laser [1,2]. The most suitable for this proposal are the wide gain lasers such as Dye, Titan-Sapphire, F-Color Center lasers with laser pumping carried out by additional laser. Typical important practical case of two-wavelength generation is the one-side transversally laser pumped lasers. A well-established examples are the Dye lasers, pumped most frequently by the harmonics of Q-switched Nd:YAG or Ruby lasers [4]. As a rule, the two wavelengths are generated in superimposed or closely disposed, parallel to the axes parts of two spectral-selective resonators. The common linear parts are also parallel to the input wall for the pump light. Thus, for the generation process the pumped volume is used in optimal manner. However, there are also essential drowbacks, related to the progressive decreasing of the pump light intensity in the depth of the pumped region. This leads to strong non-homogeneous amplification distribution in cross section of the generation and respectively to strong transversal non-homogeneity of the laser output beam. Some problems can be partially solved using low-absorption dye solution and by decreasing strongly the beam diameter (~ 0.1-0.2 mm). The latter leads to a very ineffective use of the pump radiation.

In this work we propose a new solution of transversal, one-side laser pumped two-wavelength laser. The consideration is on the example of laser pumped dye laser [4]. The main and essential advantage of the proposed laser solution is to naturally assure the homogeneous radial pumping of the generated beam resulting in natural intensity symmetry in beam cross section. It also strongly facilitates the low-transversal mode emission. We present the principle, the theoretical treatment with computer analysis and carry out basic experimental tests of our proposal.

II. PRINCIPLE OF THE PROPOSAL – DISCUSSION, WHAT ARE THE ADVANTAGES. EXPERIMENTAL AND THEORETICAL TREATMENT.

For simplicity and for clarity of the solution, the case of Rhodamine 6G (Rh6G) dye solution laser, pumped by the second harmonic (0.53 μm) of the Nd:YAG laser was used. The standard arrangement [5] of such laser was utilized - quartz cell with length of 10 mm filled with the Rh6G dye solution ($6x10^{-4}$ mol/l in ethanol). The pump light (~5 mJ/40 ns; 0.5 Hz rep. rate) was focused on the front cell wall with a 5 cm cylindrical lens. The focalization forms the beam in horizontal rectangular form with dimension 0.7 cm x 0.04 cm. Practically, the entire energy (~90 %) was absorbed in parallelepiped-form volume of the solution with approximate dimensions of 0.7 x 0.04 x 0.04 cm.

Following our experimental results, we have noticed a drawback concerning the spatial beam profiles when the traditional solution with the parallel propagation of the two channel axis in the pumped layer is used. That is why in our previous work [5] we have realized Rh6G two-wavelength laser, using an arrangement in which the channels of the two selective resonators are separated, one being parallel and close to the cell wall and the other – passing the active layer under a small angle (~ 10^o) using the internal

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reflection by the input cell wall. By investigating the transversal profile of the generated beams we have noted the strong difference to the common scheme and the advantage to use the declined resonator axis.

Here we will use our observation and in order to propose and develop a two wavelength laser of the described type with essentially improved beam profiles. The basic idea is to use the internal total reflection for the laser operation with conveniently declined axes of the two spectral selective resonators. Thus, as we will show, the two beams are naturally obtained with very good radial symmetry, in contrast to the parallel axes propagation is used.

As a first experimental point in the work we show the two beam profiles in the realization of the laser of the considered new type (with kinked axis). The results and the corresponding curves after computer treatment of the photographed spots are illustrated on the photograph on Fig.1. The bottom spots on Fig.1(a) and the corresponding graph on Fig.1(c) are for the generation in the channel with axis parallel to the input window (that passes through the pumped zone). The top spot and the corresponding curve in Fig.1 (b) are for the resonator with the axis using the total reflection to pass in grazing angle through the pumped volume. The improved beam profile for the second case is evident.

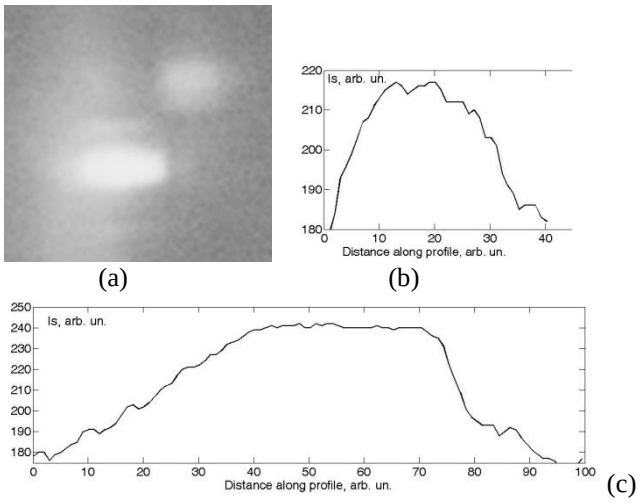


Fig.1. The actual photograph of the beam profiles (a) for generation with resonator axis parallel of the input window (bottom spot) and for grazing axis using total reflection in the wall (angle ~ 10^o , top spot), (b) and (c) gives the corresponding computer treatment - of the top spot (b) and the bottom spot (c). The natural improvement of the profile for the grazing propagation is evident.-

Based on this our two-wavelength laser realization using a grazing trajectory for one of the axes, leads us to the idea to develop the laser of the discussed type with the two axes, both kinked using the total internal reflection was considered. If the axes pass at very small angle (grazing incidence ~ 10^o) by respect to the input wall plane, the used length of the pumped region will be slightly shorter with respect to the full length and the losses will be negligible. However, the beam profiles will be with strongly improved quality. The natural principle of the beam profiles improvement for the grazing axes disposition is clarified by Fig.2.

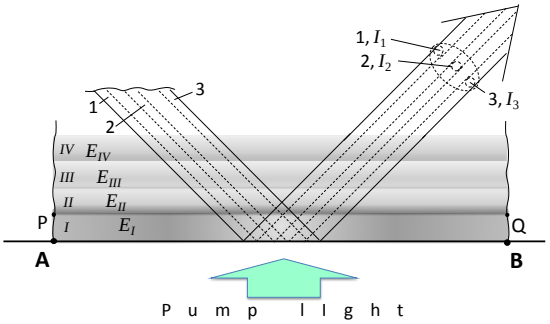


Fig.2 . To the explanation of the beam profile improvement for the grazing axis propagation using the total internal reflection.

The active medium (pumped dye solution) is presented as sequences of zones (I-IV) with different amplifications due to the pump light energy (E*i*) decreasing, due to its absorption in the active medium ($E_1 > E_2 > E_3 > E_4$). The detailed consideration of the picture shows that the arbitrary ray of any part of the formed laser beam (for example 3 rays are shown – (1), (2), (3)) passes exactly the same path. The averaged pumping conditions contribute to the equal amplification through the active medium. Thus we obtain propagation of the beam as in the homogeneously pumped active medium that is completely different in comparison with wall-parallel propagation. The given observation and the physical discussion lead to the proposal of the two wavelength laser with two grazing angle propagation axes in the active laser volume (and formed laser beams). The scheme of such laser solution, based on grazing beam propagation in the active volume, obtained by total internal reflection of the input wall, is shown in Fig.3. The concave mirror M_0 and the end mirrors M_1, M_2 are with parameters, disposition and adjustment suitable to form two optical resonators [3]. The axis of each resonator propagates in kinked manner in the active medium, using the total reflection of the glass laser cell wall (the incident angles are of order of 75^o-80^o). The Interference Wedges $IW_{1,2}$ are used as spectral selectors [6,7] in the cavities, $D_{1,2}$ are diaphragms.

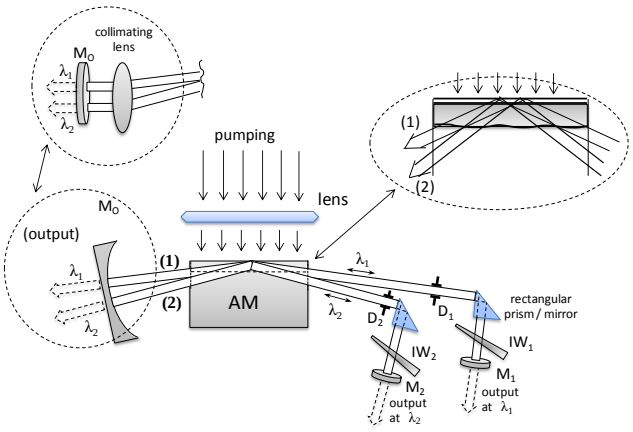


Fig. 3. The scheme of the proposed two-wavelength laser solution. AM is the Active Medium - quartz cell with dye solution. In the left inset - the formation of the output in parallel beams using the lens and a flat mirror and in the right - scheme for the explanation of the laser action.

On Fig.4 are given schematically the parts of the resonator axes and the formed beams around the places of the incident central part of the input wall of the dye cell. The axis and the formed beam are noted as (1) and (2).

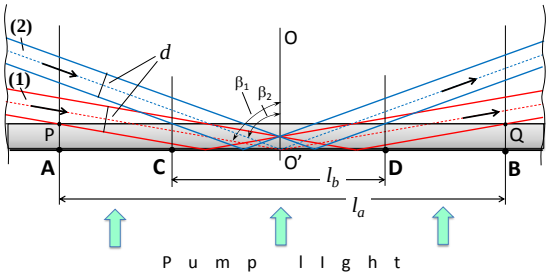


Fig. 4. Scheme of resonator axis and formed beam propagation in the zone of amplification.

On Fig.4. AB is the pumped length in the cell, CD is the zone of beam superposition. The incident angles are β_1= 83.16° and β_2=74.36° for the beams (1) and (2), respectively. The lengths of AB and of CD are 1 cm and 0.28 respectively. The depth of the pumped region d is calculated to be 0.04 cm - for used 6.10^{-4} mol/l Rh6G ethanol solution as an active medium.

Using the scheme from Fig. 4 we have estimated the path of each beam outside the competition zone (practically outside the zone CD) and the part with superposition (competition) of the beams – zone CD. We have theoretically investigated the beams behavior - especially tunability, described with two differential equation systems – one for the non-competing parts and second for the superposition and competition of the two beams. Practically, the system that describes the generation in the competition zone is based on the conveniently adapted rate differential equations [4]:

$$\frac{dN_2}{dt} = R_p(t) - \left[B_1 \cdot q_1(t) + B_2 \cdot q_2(t)\right] \cdot N_2(t) - \frac{N_2(t)}{\tau}$$

$$\frac{dq_1}{dt} = B_1 \cdot q_1(t) \cdot V_{a1} \cdot N_2(t) - \frac{q_1(t)}{\tau_{c1}}$$

$$\frac{dq_2}{dt} = B_2 \cdot q_2(t) \cdot V_{a2} \cdot N_2(t) - \frac{q_2(t)}{\tau_{c2}}$$

with $P_{out}^{1,2} = \left(\gamma_{out}^{(1,2)} . c/2L'\right) . h\nu^{(1,2)} . q_{1,2}(t)$ where the output powers are P_{out}^1 and P_{out}^2, the generated photons in the two channels are denoted as q_1 and q_2 for the two selected wavelengths λ_1 and λ_2. N_2 is the inverse population in the pumped active volume; $B_{1,2} = \sigma_e^{(1,2)} . l_{1,2} . c/(V_{a1,2} . L')$ is calculated in s^{-1}; σ_e^1 is the emission cross-section for λ_1 in the channel (1) (variable); $\sigma_e^2 = 1.8x10^{-16}$ m^2 is the emission cross-section for λ_2 = 562 nm (fixed at the maximum of the gain curve of the Rh6G [4]); l_1 = 0.34 cm and l_2 = 0.3 cm – lengths of the active medium, corresponding to (1) and (2) channels respectively in overlapped part; c = $3x10^{10}$ cm/s is the light velocity; V_{a1} = $4.22x10^{-4}$ cm^3 and V_{a2} = $3.73x10^{-4}$ cm^3 is the active volumes for the two wavelengths; L' = 6 cm is the optical length of the resonator for both channels. The lifetime of the upper laser level is τ = 3 ns. The term in $h\nu^{(1,2)}$ is the energy of the generated photons for the corresponding wavelength, measured in [J]. The dumping time of the photon in the resonator is $\tau_{c1,2} = L'/c.\gamma^{(1,2)}$, where $\gamma^{(1,2)}$ describes the loss in the corresponding channel resonator, following Ref. [Svelto 2010]. The total number of active dye molecules used in the calculations is $3.61x10^{17}$ cm^{-3} that corresponds to a solution concentration of $6 \cdot 10^{-4}$ mol/l. The term $R_p(t) = P_p(t)/(h\nu_p . V_{a1})$ is the pump rate. $R_p(t)$ is related to the temporal shape of pump energy for our oscilloscope observation trapezoid shape with a rise time of 10 ns, near-plateau part of 10 ns and fall time of 20 ns. For the considered case the pump energy is 5 mJ. The concave mirror was taken to be with 99% reflection and the mirrors M_1 and M_2 with reflections of 0.1 and 0.6, respectively; the transitivity of IW_1 is 50 % and of IW_2 – 90 %. For this conditions, we obtain for two selected wavelengths λ_1 = 563 nm and λ_2 = 562 nm for the two beams near equal outputs of 2 mJ and 1.9 mJ respectively.

For the computing of the generation outside the zone of competition CD we take the same system with initial conditions $N_2 = 0$ and $q_1 = 1$ and $q_2 = 0$ (the last acceptance reduces the system to describe the generation only for q_1. Here and below, we take as a pump energy the part of the full pump energy, proportional to the relative length of the considered active medium length. After solving the reduced system we obtain the new value for q_1. We solve again the full system for the range CD taking as initial condition the obtained value of q_1. For q_2 the value 1 is used. As a third step we solve the system for the third zone, taking as initial condition the obtained value for q_2 from the solution for the zone of competition and now we accept $q_1 = 0$. From the solution of the system, we obtain q_2 as a photon number in the beam (2) and take for the beam (1) q_1 to be equal of the photons number, obtained by solution of the system for zone CD. From obtained photon number for each output beams, we obtain correspondingly the generated output energy for each beam [5].

Using this scheme of calculation with a fixed wavelength λ_2 in the channel (2) at 562 nm and tuning the wavelength λ_1 in the first channel, we obtain the tuning curve of the laser. The last is given in Fig. 5.

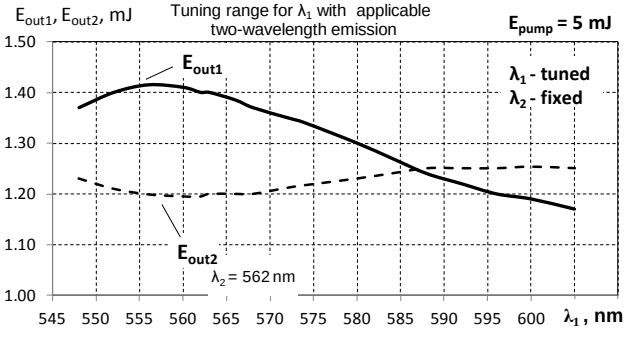
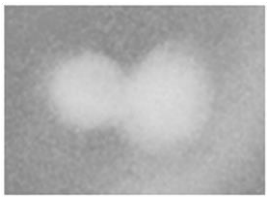


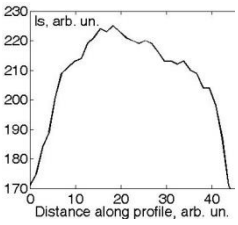
Fig.5. The calculated tuning curve for the output energy of the proposed laser. The wavelength in the second channel (2) is fixed at λ_2=562 nm and the wavelength λ_1 in the first channel (1) is tuned.

If we compare this tuning curve with the two-wavelength laser for which one of the channel is close and parallel disposed to the input wall and the second one is with grazing propagation [5] it can be seen that in the new laser the tuning curve is essentially broadened. This can be expected, taken into account that the competition zone here is quite shortened. This is one of the advantages of the proposed laser.

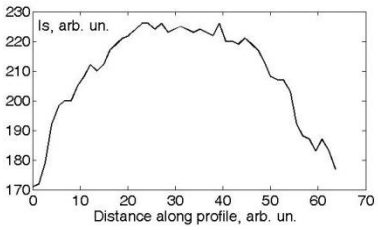
However, the main and essential advantage is, as we have discussed already, the generation in the scheme of pumping the two beams with radial symmetry in the cross section. We have already presented the physical argumentation of such phenomena.

In our preliminary test-experiment we have utilized such laser with discussed construction parameters and have obtained the expected results – the two beams with naturally obtained radial symmetric beam profiles. The actual photograph and the computer treatment to obtain the beam profiles are given in Fig.6. It is clearly seen that the spot profiles are with radial symmetry. Our consideration shows that the spots profiles are nearly composed by superposition of two radial symmetric modes each – of the modes TEM_{00} and TEM_{01*} [7].


(a)



(b)



(c)

Fig. 6. The actual photograph of the beam profiles (a) for generation in the proposed two wavelength laser with grazing resonator axis and beam propagation (incident angles of ~ 70 ^{o}, left spot (b) and ~ 80 ^{o} right spot (c). The obtained natural radial symmetric profile can be seen.

III. CONCLUSION

In this work we have proposed a new solution of transversal, one-side laser pumped two-wavelength laser. The consideration is for the example of laser pumped dye laser. The proposed laser solution has as main and essential advantage to assure naturally the homogeneous radial pumping of the generated beam. The natural intensity symmetry in beam cross section is assured. Additionally, the strong low-transversal mode emission is facilitated. We have presented the principle of this solution together with the carried out theoretical treatment, computer analysis and basic experimental tests.

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Features of Electro-magnetic Methods for Evaluating Sizes of Surface Cracks in Metals

Dorian Asenov Minkov

Abstract – **Two methods are described for evaluating sizes of surface cracks in metals. In the first method, induced leakage magnetic field around a surface crack, measurement and calculation of Hall voltage from Hall element, and minimization of the deviation between such voltages for several locations of the Hall element are used. In the second method, induced AC current on the metal surface, and loop antenna with output voltage, depending on the amplitude of the magnetic field within the crack are used.**

Keywords – **Electro-magnetic methods, evaluating depths of surface cracks in metals, Hall element, loop antenna**

I. Introduction

Presence of surface cracks in materials can lead to their mechanical breakdown, especially under heavy load or in hostile environment. Evaluating the depths of surface cracks is difficult, because the small crack width often hinders the applicability of direct visualization techniques. Development of methods for evaluating sizes (also called 'sizing') of cracks on metal surfaces is important, because they are needed for prediction and prevention of failure of equipment for the pipeline, railway and aircraft industries.

In this paper, two electro-magnetic methods for non-destructive sizing of surface cracks in metals are outlined. These methods were developed, with my active participation, during my five years work at the Fracture Research Institute in Sendai, Japan.

II. Method Using Measurements by a Hall Element

A. Description of the method

In this method, a magnetic metal is magnetized, by a static magnetic field, parallel to its flat surface. The magnetic field redistributes around a surface crack, and its part called 'leakage magnetic field' (LMF) spreads out of the specimen, in the vicinity of the crack. Hall voltage is measured by a Hall element, and is proportional to LMF.

LMF is also estimated using the 'dipole model of a crack' (DMC). In DMC, the crack is considered to be filled with magnetic dipoles oriented parallel to the magnetizing field, the opposite poles being located on the two opposite walls of the crack. Integrating the contributions of all of these magnetic dipoles, gives LMF in a given point outside the specimen. Hall voltage is calculated by summing its constituents over the active region of the Hall element.

Sizes of the crack are evaluated by minimizing the RMS deviation between the set of measured Hall voltages and a set of calculated Hall voltages, in the vicinity of the crack.

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We investigated only cracks with constant widths. The magnetizing field was always directed perpendicular to the long axis *y* of the crack, at the metal surface. The density of the magnetic dipoles was assumed to increase linearly with the depth of the crack. The Hall voltages were measured along scanning lines parallel to the magnetizing field.

B. Formulation of the method

Let us consider the simplest possible surface crack representing a right angle parallelepiped, with length *2l* along the *y*-axis, width 2*a* and depth *d*. The (*x0y*) plane of the coordinate system is at the flat metal surface, the point 0 is at the geometrical center of the crack in this plane, and the z-axis is directed away from the metal. In case of magnetizing the metal parallel to its crack containing surface, magnetic field lines in the vicinity of such a crack, and a representation of LMF by only one magnetic dipole in the DMC framework are illustrated in Fig. 1.

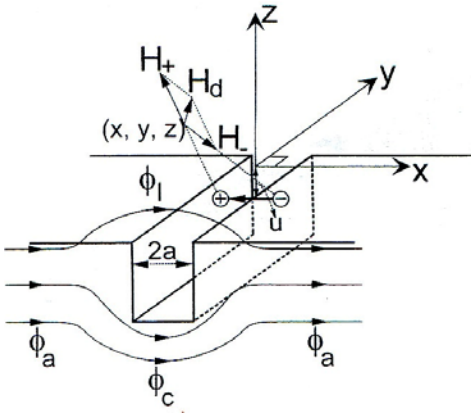

Fig. 1. LMF H_d for only one magnetic dipole has two components H_+ and H_-. u is distance between this dipole and the metal surface

The z-component of the intensity of the leakage magnetic field (ZILMF) of this crack is represented by integrating the ZILMF of all of the dipoles filling the crack:

$$H_{rz}(x,y,z)=\int_{-l-y}^{l-y}\int_{0}^{d}\frac{m(u)}{4\pi\mu_0}\left\{\frac{(z+u)(du)(dy)}{\left[(x+a)^2+y^2+(z+u)^2\right]^{\frac{3}{2}}}-\frac{(z+u)(du)(dy)}{\left[(x-a)^2+y^2+(z+u)^2\right]^{\frac{3}{2}}}\right\} \quad (1)$$

where *m(u)* is the surface density of magnetic dipoles at the crack walls. It is assumed that:

$$m(u)|_{u\subset[0,d]}=m(v)|_{v=u/d\subset[0,1]}=m_1+m_2v \quad (2)$$

where m_1 and m_2 are constants. At the crack mouth $m(0)=m_1$, and the crack bottom $m(d)=m_2$ [1].

Performing the integration in (1) gives:

$$H_{rz}(x,y,z)=\frac{m_2}{4\pi\mu_0 d}\times\left\{\begin{array}{l}\left(\frac{m_1 d}{m_2}-z\right)\left[\begin{array}{l}A_1(l-y,x+a)+A_1(l+y,x+a)\\-A_1(l-y,x-a)-A_1(l+y,x-a)\end{array}\right]\\+\left[\begin{array}{l}-(x+a)A_2(l-y,x+a)-(x+a)A_2(l+y,x+a)\\+(x-a)A_2(l-y,x-a)+(x-a)A_2(l+y,x-a)\end{array}\right]\\+\left[\begin{array}{l}(l-y)A_3(l-y,x+a)+(l+y)A_3(l+y,x+a)\\-(l-y)A_3(l-y,x-a)-(l+y)A_3(l+y,x-a)\end{array}\right]\end{array}\right\}$$

$$A_1(l-y,x-a)=\ln\left[\sqrt{\frac{(x-a)^2+(z+d)^2}{(x-a)^2+z^2}}\times\frac{(l-y)+\sqrt{(x-a)^2+(l-y)^2+z^2}}{(l-y)+\sqrt{(x-a)^2+(l-y)^2+(z+d)^2}}\right],$$

$$A_2(l-y,x-a)=\tan^{-1}[A_{21}(l-y,x-a)],$$

$$A_{21}(l-y,x-a)=\frac{(l-y)(x-a)\left[(z+d)\sqrt{(x-a)^2+(l-y)^2+z^2}-z\sqrt{(x-a)^2+(l-y)^2+(z+d)^2}\right]}{(x-a)^2\sqrt{(x-a)^2+(l-y)^2+z^2}\times\sqrt{(x-a)^2+(l-y)^2+(z+d)^2+(l-y)^2 z(z+d)}},$$

$$A_3(l-y,x-a)=\ln\left[\frac{\sqrt{(x-a)^2+(l-y)^2+(z+d)^2}+z+d}{\sqrt{(x-a)^2+(l-y)^2+z^2}+z}\right], \quad (3)$$

where μ_0 is vacuum permeability, $A_j(l\text{-}y,x\text{+}a)$, $A_j(l\text{+}y,x\text{-}a)$ and $A_j(l\text{+}y,x\text{+}a)$ for j=1,2,3 are obtained by replacing respectively x-a by x+a, l-y by l+y and both l-y by l+y and x-a by x+a in the above expressions for $A_j(l\text{-}y,x\text{-}a)$.

For a crack with a length $2l_0$ and an arbitrary depth profile, along the long axis of the crack, according to DMC, ZILMF for such a crack is:

$$H_z(x,y,z)=\sum_{i=1}^{N_1N_2}H_{rz}(x,y_i,z)=\sum_{i=1}^{N_1N_2}H_{rz}(x,y-l_i,z) \quad (4)$$

where i is the number of a constituent sub-crack, and $l_i=-l_0[1-(2i-1)/(N_1N_2)]$.

A Hall element is positioned on the flat metal surface. Its Hall voltage is formulated, by integrating ZILMF over the active region of the element, as follows:

$$V_H(x,y,z)=\frac{\mu_0 I}{qnd_a}\frac{\sum_{i_1=1}^{n_1}\sum_{i_2=1}^{n_1}\sum_{i_3=1}^{n_2}H_z(x_{i_1},y_{i_2},z_{i_3})}{n_1^2 n_2}=\left(\frac{\mu_0 I}{qnd_a}H_a\right)=cH_a \quad (5)$$

where I is the electric current supplied between two opposite contacts of the Hall element, $V_H(x,y,z)$ is the Hall voltage induced between the other two opposite contacts, d_a is the thickness of the active layer of the chip of the Hall element, q is the absolute value of the electron charge, n is the electron concentration in the active layer which is assumed to be n-type and to have square-shaped top surface of its active region, the volume of the active region is represented as a sum of $n_1^2n_2$ parallelepipeds, n_1 and n_2 are the numbers of these parallelepipeds along the length and the thickness of the active region, $H_z(x_{i1},y_{i2},z_{i3})$ is the z-component of the intensity of the leakage magnetic field of the investigated crack with an arbitrary depth profile in the center of the parallelepiped with number (i_1,i_2,i_3), H_a is the average value of ZILMF over the volume of the active region of the Hall element, and $c=\mu_0 I/(qnd_a)$ is constant.

During measurement, the top planar surface of the Hall element is positioned onto the metal surface. The Hall voltage is measured at several locations, close to the crack, which are usually aligned along a scanning line parallel to the magnetizing field [2].

The Hall voltage is also calculated for each of the measurement locations by using Eqns. 1 to 5. The unknown depth profile of the crack, the width of the crack and the depth distribution of m can be computed by minimizing the RMS deviation $\sqrt{\left\{\sum_{i=1}^{N}\left[V_H^m(i)-V_H^c(i)\right]^2\right\}/N}$ between the set $V_H^m(i)$ of measured Hall voltages, and its respective set $V_H^c(i)$ of calculated Hall voltages, where N is the number of measurement points. This technique is a 'crack inversion'.

C. Results

In the discussed experiments were used right angle parallelepiped specimens of ferromagnetic steel SS400 with dimensions 200x100x5 mm. One surface crack with a constant width of $2a$ = 0.9 mm is cut mechanically at the surface of each specimen, and the crack length is $2l_0$ = 10 mm. One crack has a right angle parallelepiped shape, and is designated by a first symbol "r" in the case symbol, which describes the measurement conditions. The other crack has an isosceles triangular depth profile, and is designated by a first symbol "t" in the case symbol.

The Hall voltage is measured by a Toshiba THS124 GaAs Hall element, supplied with DC current I = 5 mA, which leads to $c = 2.096\text{x}10^{-6}$ Ω.m in Eq. 5. The size of the active region of the chip is 125x125x6 μm, and the distance between the center of this active region and the metal surface is z_m = 0.54 mm.

One set of measured Hall voltages is obtained along a scanning line passing through 0, and is designated by a second symbol "c" in the case symbol. Other set of measured Hall voltages is obtained along a scanning line at a distance of $2l_0/3$ = 3.33 mm from the first scanning line, and is designated by a second symbol "s" in the case symbol. A second symbol "b" means that both "c" and "s" sets of measurements are used. All of the Hall voltage measurements are taken on the same side with respect to the long axis of the crack, and the number of measurement points along each of the scanning lines is N = 10.

Two types of crack inversions are performed. In the first type, the crack is assumed to have a right angle parallelepiped shape, and N_1N_2 = 1. The inversions give the parameters d, a, m_1, m_2. The depth d for the triangular depth profile crack is expressed by the depth d_e of a crack with a semi-ellipsoidal depth profile and the same area below its long axis whereat $d_e = 4d/\pi$, which represents similarly the maximum depth $d_m = d_{tr}$ (true depth) of the investigated crack. The inversion results are shown in Table 1.

The second type of crack inversions is performed for the triangular depth profile crack only. It is assumed that the depth profile of the crack is unknown but symmetrical with respect to the central axis, as well as that the crack width is measured independently. Both the true and the computed depth profiles for N_1 = 4 and N_2 = 7 are illustrated in Fig. 2.

TABLE 1. RESULTS FROM FIRST TYPE CRACK INVERSIONS

Case Sym-bol	m_1 $\left[\frac{H.A}{m^2}\right]$	m_2 $\left[\frac{H.A}{m^2}\right]$	d [mm]	a [mm]	$\frac{\lvert d-d_{tr}\rvert}{d_{tr}}$ [%]	$\frac{\lvert a-a_{tr}\rvert}{a_{tr}}$ [%]
rc2	0.45	0.99	2.690	0.480	10.33	6.67
rs2	0.61	0.99	3.184	0.395	9.20	12.22
rb2	0.42	0.83	2.810	0.477	10.73	11.00
tc2	0.42	0.26	2.802	0.405	6.60	10.00
ts2	0.42	0.26	2.889	0.407	3.70	9.56
tb2	0.42	0.26	2.799	0.407	6.70	10.56

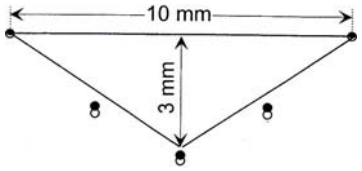

Fig. 2. True and computed depth profiles for the crack with triangular depth profile. $N_1 = 4$, $N_2 = 7$, and a is known

III. METHOD USING MEASUREMENTS BY A LOOP ANTENNA

A. Description of the method

In this method, an alternating current I_s with a frequency f is supplied to a conductive wire, positioned close to the flat surface of a metal, generates an induced alternating current I_i, with the same frequency, which spreads beneath the surface of the metal. This induced current has a direction opposite to the direction of the supplied current at every moment, its density decreases away from the wire, and its penetration depth beneath the surface of the metal is $\delta = 1/(\pi\mu f\sigma)^{0.5}$, where μ is the magnetic permeability of the metal and σ is its conductivity. Both the supplied current and the induced current generate magnetic fields directed perpendicular to the wire, which could be detected by a loop antenna, positioned as close as possible to the surface of the metal, whose loop is perpendicular to the metal surface and parallel to the wire [3].

The largest contribution to the magnetic field generated by the induced current within the antenna loop, and correspondingly to the voltage measured by the antenna, comes from the induced current path located closest to the antenna, because the magnetic field intensity is inversely proportional to square of the distance between the generation source and the measurement point. This path is named the 'dominant induced current path' (DICP), and in the case of a flat metal surface is parallel to the conductive wire, and located at the metal surface right below the antenna – Fig. 3.

For an alternating current with a frequency $f > 100$ MHz, the induced current spreads within a penetration depth of $\delta < 0.05$ mm beneath the metal surface. Furthermore, the amplitude of the voltage measured by the antenna for a metal surface without cracks can be expressed as follows:

$$|U| \propto |-B_s + B_i| \tag{6}$$

where the two components of the amplitude of the magnetic induction $B_s > 0$ and $B_i > 0$ are generated respectively by the supplied and the induced currents in the region below the antenna loop and have opposite directions at every moment.

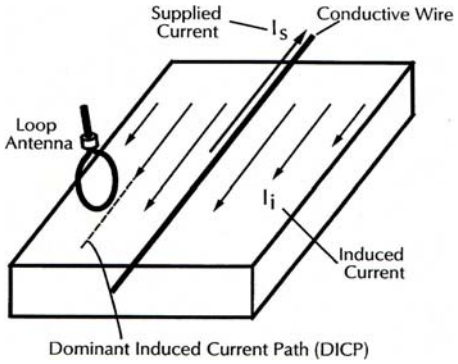

Fig. 3. Geometry, distribution and positioning of the supplied current, the induced current, and the measuring loop antenna

Correspondingly, for a metal surface with cracks, the amplitude of the measured potential drop along the loop of the antenna in the vicinity of a crack is:

$$|U| \propto |-B_s + B_i + B_c| \tag{7}$$

The 'leakage magnetic induction' $B_c > 0$ has the same direction as B_i and is a result of two effects: firstly, a part of the magnetic field generated by the supplied current penetrates into the surface crack. This leads to a decrease of the amplitude of that field within the antenna loop, with respect to a metal surface without cracks, and therefore to a decrease of B_s. Secondly, in the vicinity of the crack, the induced current flows within the penetration depth δ from the crack walls, i.e. it follows the crack geometry closely. The development of such a current bending around the crack leads to reinforcing the magnetic field generated by the induced current, and to increasing B_i – Fig. 4 [4].

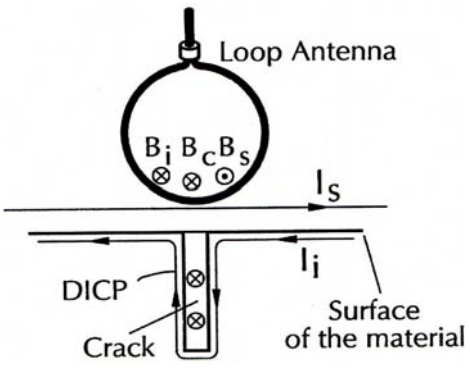

Fig. 4. Illustration of the components of the magnetic induction, with amplitude values B_s , B_i , and B_s within the antenna loop

For a metal surface without cracks, $B_c = 0$. For a metal surface with cracks, B_c has a larger value for larger cracks, in accordance with the above comments about the meaning of B_c. Correspondingly, an analysis of the leakage magnetic induction B_c can provide information about the crack sizes.

B. Results

The experiments were performed on a specimen of paramagnetic steel 316. This specimen contained three mechanically cut cracks, having a right angle parallelepiped shape, lengths of 10 mm, widths of 0.15 mm, and depths of correspondingly d = 0.5 mm, 1 mm, and 2 mm, whereat the long axes of these cracks were parallel to each other. Cu conductive wire, with a rectangular cross section of 2x0.035 mm, was fixed at a distance of 0.1 mm from the surface of the metal by an insulating plastic foil filling the gap between the specimen and the wire. The long axis (x=0,y) of the wire was perpendicular to the long axes of the three cracks, and it passed above their geometrical centers. The loop antenna contained a coaxial line with a Cu inner conductor and a Cu shield, as well as a loop with a diameter D which was closed by a solid Cu conductor. The solid Cu conductor was soldered at its two ends correspondingly to the inner conductor of the coaxial line, and to its shield.

The frequency of the supplied sinusoidal voltage was chosen to be f = 300 MHz. A network analyzer was measuring the ratio R(dB)=|U|/|U$_s$| between the amplitudes of the voltage at the antenna output and the supplied sinusoidal voltage. The ratio R measured, by a loop antenna with D = 7 mm, along scanning lines (x=const,y) parallel to the Cu wire, over a surface area of the specimen which contains the cracks, is represented in Fig. 5 for distances x = [2-6] mm from the long axis of the wire. It is seen that, in most cases, the dependences R(x=const,y) undergo changes in the vicinity of the cracks, which are most significant at the centers of the cracks, i.e. at y = - 60 mm, 0 mm, and 60 mm. The difference $C = R(x=x_1, y=y_1) - R_f(x=x_1, y=y_1)$, which depends on the crack depth d, is named a 'crack response of the ratio R' where R and R_f are measured over the same surface area of the specimen when it contains a crack and does not contain a crack, correspondingly. The results shown in Fig. 5 can be explained by an analysis of the behavior of the components of the magnetic inductions in Eq. 7.

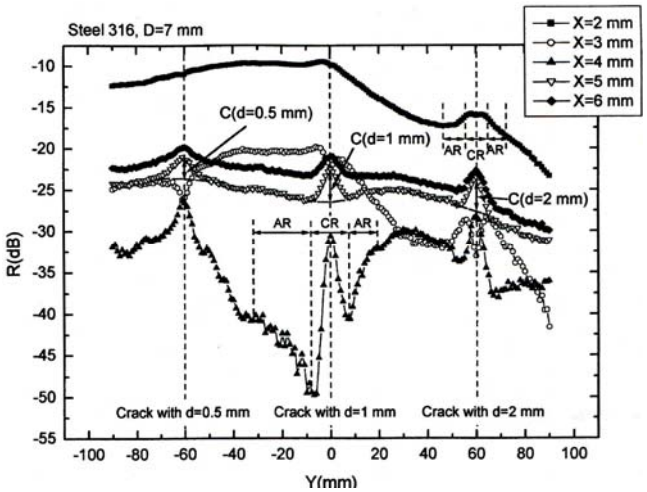

Fig. 5. Ratio R measured by the antenna with D = 7 mm along scanning lines (x=const,y) over area containing the three cracks

The dependencies of the crack response C measured outside the crack at x = 6 mm on the crack depth d are illustrated in Fig. 6, for loop antennas with 3 different diameters. It is seen that largest C is obtained for the antenna with a diameter D = 7 mm, while best linearity of the dependence $C(d)$ is obtained for diameter D = 10 mm.

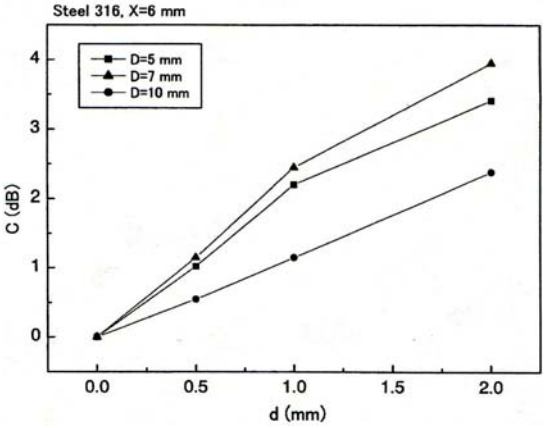

Fig. 6. Dependencies of the crack response C at x = 6 mm on the crack depth d, for loop antennas with 3 different diameters

IV. CONCLUSION

The obtained results indicate that the method using a Hall element allows simultaneous determination of both the average depth and thickness of a crack. In case that the crack width is measured independently, this method leads to obtaining at least a simplified depth profile. The method using a loop antenna can also provide the average depth of the crack.

The principle of the method using a Hall element has some similarity to that of ultrasonic methods using Rayleigh wave [5], in the sense that the paths of both the magnetic field close to the surface and the Rayleigh wave are influenced by the cracks, which leads to a change in the output signal. The Hall element method though allows extracting information about the width and the shape of the crack, unlike the method from [5].

The method using a loop antenna has some similarity to resonant methods using scanning waveguides [6], because all of these methods employ a scanning probe operated at microwave frequency. These methods can detect cracks with sub-mm depths, but the loop antenna method uses frequency of only 300 MHz, while the method from [6] uses frequency of above 8 GHz and inconvenient filling the cracks with dielectric material.

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Approaches to Increasing the Quality and Reliability in the Field of Design Patterns

Dimitrichka Zheleva Nikolaeva and Violeta Todorova Bozhikova

Abstract – **The report presents two techniques in software development based on Design Patterns: programming, providing reliable functioning of the programming systems (PPRF) and reuse of software production (RSP). These are the findings of an analysis made in the field of Design Patterns. The report explores six indicators: the actuality of the topic, analysis of the approaches and methods for the development of Design Patterns, determining the advantages and disadvantages of implementing Design Patterns, study of Design Patterns according to their use and according to the purpose of software development, analysis of the programming languages used to develop Software Templates. They are important for the development of Software Based on Software Templates. In conclusion the advantages of using Design Patterns are summarized and an application is made for future projects.**

Keywords – **Software Design Patterns, Software Re-Use, Software Quality**

I. INTRODUCTION

Over the past 80 years, information technologies have been developing rapidly. Programming systems and products have become increasingly complex and this is a prerequisite for creating of new efficient technologies for development. In the seventies of the last century the development of software based on templates arise. [20] They have a concept for solving common problems in the field of object-oriented modeling. They are designed to provide standardized and efficient solutions for architectural and conceptual problems in computer programming.

The report consists of four parts. The second provides analysis, which includes a study of six indicators: the actuality of the topic, analysis of the approaches and methods for the development of Design Patterns, determining the advantages and disadvantages of implementing Design Patterns, study of Design Patterns according to their use and according to the purpose of software development, analysis of the programming languages used to develop Software Templates. The results are summarized graphically and tabularly. The third part discusses the techniques used in software development based on Software Template. The conclusion supports the need to study and implement approaches in the field of Design Patterns for improving the quality and reliability of software systems and products.

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II. ANALYSIS OF THE LITERATURE LINKED TO THE SOFTWARE PATTERNS DESIGN.

The report presents the results of ongoing research of the first author in the field of "Software development using design patterns." Until now, 107 literature sources have been analyzed, the most important of which are cited in this publication. The large number of publications on the subject clearly demonstrates the topicality of the subject (Fig.1. Grouping of literature and Fig.2 Literature issued/ published in the period 1993-2014 in field of Design Patterns).

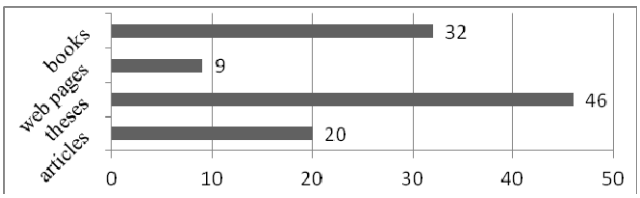

Fig.1. Grouping of literature

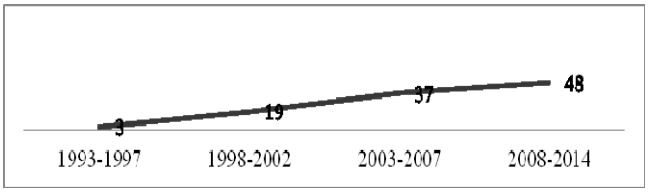

Fig.2. Literature issued/ published in the period 1993-2014 in field of Design Patterns

Apart from, confirming the actuality of the topic, the indicators subject of research aim to:

1) Analysis of approaches and methods for the development of Design Patterns;
2) Determining the advantages and disadvantages of implementing Design Patterns;
3) Study of Design Patterns according to their use;
4) Study of Design Patterns according to the purpose of software development;
5) Analysis of the programming languages used to develop Software Templates.

The conclusions made are important for the development of Software Based on Software Templates. The results of the analysis are presented in table and graphically as follows:

TABLE 1.SUMMARY ANALYSIS OF DESIGN PATTERNS

1) Analysis of approaches and methods for the development of Design Pattern

- Strategies for tolerating software errors.
- A structural approach to the assessment of the design of model-oriented and object-oriented projects [1]
- Parametric Approach and approach check
- Creating a methodology for reuse, storage and application of code
- Development of components for reuse (componentization) [2]
- Development of libraries for re-use and easy configuration [10]
- Methodology for building dynamic binding of components [16]
- An approach for modeling complex business domains [5]
- An approach for detecting design patterns to support reverse engineering [4], [6], [9]
- A method of creating software models, leading to repeatedly used and cost-efficient software, the basis for this process are the so called mind maps
- An approach to develop Detector clones as a prefix to the Eclipse IDE

2) Determining the advantages and disadvantages of implementing Design Patterns

Advantages

- Lead to automating applications[1]
- Create and maintain complex, large-scale, flexible systems [17]
- Lead to re-use and develop components and libraries for re-use
- Simplify design and optimize code
- Develop a high structural level
- Increase the level of conceptual thinking [19]
- Lead to better decisions
- Create a common basis for comparison and detection of Design Patterns [11]
- Applicable (give a quick access to the database, help to develop games, etc.).
- Used for exchange of experience (help programmers, designers, architects and analysts for the successful use of Design Patterns in combination with a wide range of programming languages)
- Lead to the integration of the Object-Oriented, Event-Based and Aspect-Oriented Programming

Disadvantages

- The architectures of some models are not optimal
- It is not clear which model should be applied in which situations
- Novice designers err in their application
- The documentation describing the patterns is not accurate, leading to different interpretations by the designers who use it
- Lack adequate functionality, which limits the use of design patterns within a session
- Similar code segments that appear in the source code, increase both the productivity and the probability of error propagation

3) Study of the Design Patterns according to their application (covering all literary sources):
A. total (for all Design Patterns) and
B. in groups according to the purpose that the relevant Design Patterns
(**B.1.** total and **B.2.** in percent)

3)A.

Design Patterns (DP)	Use of DP	DP according to purpose
Memento	23	Behavioral patterns
Flyweight	24	Structural patterns
Iterator	28	Behavioral patterns
Chain of Responsibility	29	Behavioral patterns
Interpreter	29	Behavioral patterns
Builder	31	Creational patterns
Visitor	32	Behavioral patterns
Prototype	33	Creational patterns
Bridge	35	Structural patterns
Decorator	35	Structural patterns
Mediator	35	Behavioral patterns
Façade	36	Structural patterns
State	38	Behavioral patterns
Command	40	Behavioral patterns
Template method	40	Behavioral patterns
Composite	42	Structural patterns
Adapter	43	Structural patterns
Proxy	43	Structural patterns
Abstract Factory	46	Creational patterns
Observer	47	Behavioral patterns
Singleton	48	Creational patterns
Factory method	49	Creational patterns
Strategy	49	Behavioral patterns

DP according to the purpose	**3) B.1.**	**3) B.2.**
Behavioral patterns	390	46 %
Structural patterns	258	30 %
Creational patterns	207	24 %

4) Study of the Design Patterns according to the purpose of software development (only theses discussed):
A. Delivering reliable operation; [7], [14], [16]
B. Achieving quality; [8], [11], [12]
C. Reuse of software production; [3]
D. Evaluation of the final software [19]

5) Analysis of programming languages for the development of Software Templates:
A. (Java);
B. (C++);
C. (C#);
D. (Xml);
E. (Other)

Design Patterns	**4)**				**5)**				
	A	B	C	D	A	B	C	D	E
Abstract Factory	1	1	6	2	26	13	21	5	3
Factory method	2	1	7	1	27	9	22	9	7
Builder	1	0	4	3	18	7	14	4	4
Prototype	1	1	3	1	16	7	15	5	1
Singleton	1	2	8	2	23	12	19	9	7
Adapter	2	1	7	1	23	13	19	6	6
Bridge	1	2	4	1	16	11	17	6	2
Composite	2	1	6	2	25	11	21	7	4
Decorator	1	1	5	1	22	11	19	4	2
Façade	1	1	6	1	20	10	17	6	4
Flyweight	0	1	4	1	13	8	12	5	2
Proxy	1	1	6	1	23	11	17	6	5
Chain of Responsibility	0	1	4	1	18	10	15	3	1
Command	2	1	7	2	25	13	15	6	5
Interpreter	1	1	3	1	17	6	13	4	2
Iterator	0	0	5	1	15	8	12	3	2
Mediator	0	2	5	2	22	11	15	6	3
Memento	1	1	3	1	13	7	11	3	1
Observer	1	1	6	3	27	13	21	7	3
State	1	1	7	1	20	10	15	5	2
Strategy	2	2	6	2	26	15	24	10	4
Template method	1	1	7	1	24	10	17	5	3
Visitor	0	2	4	1	16	11	15	5	1

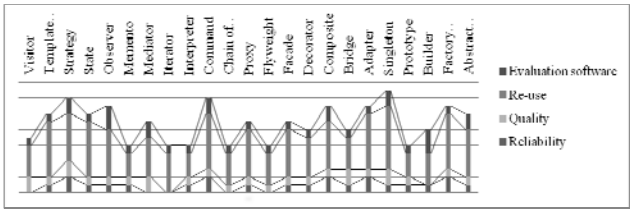

Fig.3. Use according to the purpose of the software development

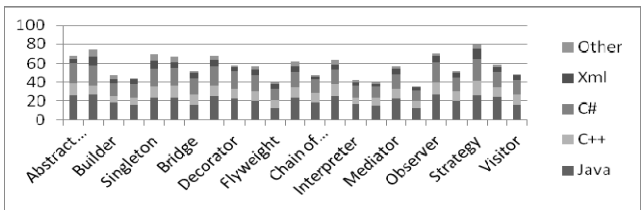

Fig.4. Use of programming languages

The results are important for the development of an approach based on the Design Patterns. After summarizing the data several conclusions can be made:

1) The issue of software templates is up to date, due to the increased interest in recent years.

2) Software Based on Software Templates is practically-oriented and despite its shortcomings, the software templates are preferred to create reliability and quality software. [10]

3) Software Templates allow for re-use, reducing the time and money to develop. Through software programming templates automate labor.

4) The most used by Software Templates: Strategy, Factory method and Singleton, but at least are: Memento, Flyweight and Iterator. The most used group of Design Patterns: Behavioral patterns - 46%, followed by Structural patterns - 30%, and the smallest is the percentage of Creational patterns - 24%.

5) Java is the most used programming language for creating Factory method and Observer. Programming languages: C++, C # and Xml are most often used to create Strategy. The language most used to create applications with Design Patterns in Java, followed by C # and C ++, the least used is Xml.

From the conclusions in 2) and 3) we can conclude that there are two main techniques for developing software-based software templates: programming, providing reliable functioning of the programming systems (PPRF) [1], [4], [6], [9] and re-use in the software production (RSP) [2], [5], [10], [16].

III. Techniques Used in Software Development Base Design Patterns

The development of quality software is associated with construction and validation processes. Construction processes are linked to Fault avoidance (prevention): avoid defects and Fault tolerance: software development with an acceptable level of error. The validation processes are related to the validation of software created and accordingly to: Fault removal: detection and elimination of errors and Fault / failure forecasting giving a forecast. Such processes also take place in the creation a Software Based on Software Templates.

The technique PPRF, used for developing software-based Software Templates is associated with an assessment of: Reliability - frequency of system failures; the collapse of the system - working situation unusual response software; defect - a programming error in the input data leading to collapse. PPRF affects three modern approaches to develop Software Templates (Fig.5):

- ✓ Development of software to minimize the defects in it (Fault avoidance);
- ✓ Software development with an acceptable level of error (Fault tolerance);
- ✓ Defensive programming.

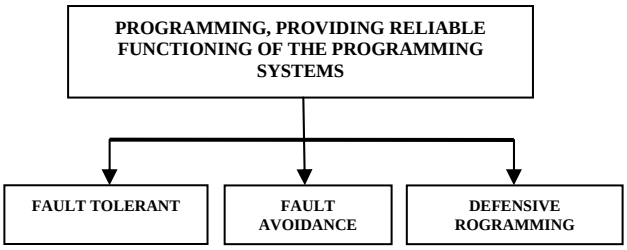

Fig.5. Approaches used in the technique PPRF

The essence of the first approach (Fault avoidance) is to reduce errors in software development. Fault tolerance is software that is designed to keep working even if there are errors. Protective programming (Defensive programming) is an approach that incorporates mechanisms to detect, assess and eliminate potential errors. Validation processes: Fault / failure forecasting and Fault removal are features of Fault tolerance, while Fault removal is a function of Defensive programming, due to the specifics in the design of software. Fault tolerance principles are: Reliable operation - the principle of repetition of elements; a different number of components can be applied for the same activity each one of them performing certain functions, the results are compared and the program continues with the frequent result. The principle is also known as N-version programming in software results; Recovery Blocks - software units comprising an alternative to re-code execution failover; Exception handlers - components for handling exceptions /a message to suspend the process. Features Fault tolerance: Forecast and detect defects (Fault / failure forecasting and Fault removal); Assess the damage after a system crash; Disaster recovery; Locate and remove defects causing the collapse of the system. Principles of Fault-free software are: Create precise specifications; Use of a design allowing the encapsulation of the information; Mechanisms for assuring quality software; Planning and system testing.

The second technique RSP is a combination of planned and systematic activities aimed at using existing software components. Their practical implementation would be successful if they met certain requirements: program components must be designed so that they are readily adjustable to consider the cloning process to regulate the mechanism for (establishing the variable) compiling the names of the change to prevent errors, components should be portable. As a result of the analysis in Table 1.Summary

analysis of Design Patterns we can conclude that in the second RSP technology to develop software based on the Software Templates (reuse) four groups of trends have be registered:

- ✓ Design of libraries of components for re-use;
- ✓ Create reusable components;
- ✓ Establishment of standards for integrated library usage of the elements for reuse;
- ✓ Create models for the process of re-use and appropriate software tools that support the development of and / or reuse.

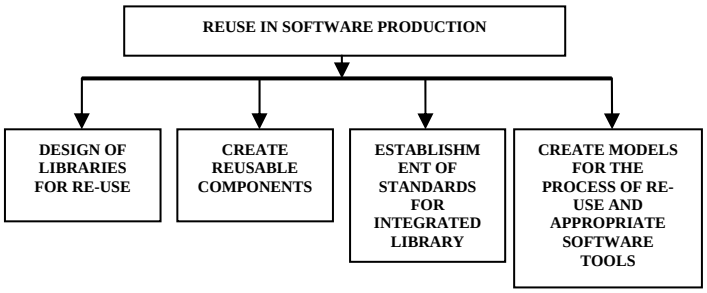

Fig.6. Trends used in RSP technique

The reuse of existing software components has several advantages: increasing the productivity of programmers work to improve the quality of the developed software, quickly create new products as it reduces development time. The success of this approach is due to the techniques of storing and retrieving components. Search mechanisms, are usually associated with a keyword search, text descriptions of natural language faceted technique by drawing descriptions from a different perspective. The principle of operation of the techniques is different, but what unites them is the ability to improve the quality and reliability of software. In PPRF technique this is achieved through different approaches to reduce software errors, while in RSP technique re-use of software components is implemented whose properties are already checked. The choice of approach depends on the application domain and the specific requirements for the created software.

IV. Conclusion and Future Progress

The report summarizes the techniques for developing software based on Design Patterns (PPRF and RSP). For this purpose, a large amount of literature in the field of Software Design Patterns has been examined. Multi criteria analysis has been conducted and results interesting for further study have been received and presented. It must be emphasized that the use of Software Design Patterns on the one hand saves time and resources for development, increasing productivity of programmer's work and on the other it leads to minimizing programming errors both resulting in quality and reliability of the developed software. Our research in the field of Design Patterns continues. The idea is to explore and develop an approach to software development based on a hybrid software template. The creation of such an approach is related to solving a number of research problems, both methodological and practical.

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A Low-power CMOS Pull-up Circuit

Reza Taherkhani, Ali Heidary, Guijie Wang and Gerard C. M. Meijer

Abstract – **In this paper, a low-power internal pull-up circuit is *presented*. For power management, many chips are implemented with a power-down (PD) pin. This paper describes a nonlinear circuit which can pull-up the PD pin through a low-ohmic path, which in default circumstances drives the pin voltage into the ON state with a high immunity for the effects of interference. This opens the option to control the PD pin externally or to use it floating. In both cases the circuit consumes only very little current. The circuit is implemented in 0.7µm CMOS technology with our smart temperature sensor. The simulation results which is in close agreement with our measurement results, shows that for the supply range of 2.7V to 5.5V in the temperature range of -45ºC to 130ºC and for all different corners of technology, the current consumption in power-down mode is less than 2µA, while the pull-up impedance is less than 50 kΩ. The measured power down current in room temperature, which is in very close agreement with simulation results is less than 1µA for all range of supply voltage. Also the measured pull up resistor for 3.3V supply at room temperature is about 26kΩ.**

Keywords –**Low power, Power management, Power down**

I. INTRODUCTION

For power management, many chips have a power-down (PD) pin, which is externally controlled. For instance, with a HIGH voltage the chip functions properly, while for a LOW voltage is in the PD mode. For a specific group of chip users, which don't need the PD option, but prefer to have a minimum number of pins, it would be desirable that in case of a floating PD pin the chip is automatically driven into the ON state. This can be achieved with an internal pull-up resistor. For immunity for interference, it will be required that the impedance of such a resistor is sufficiently low, which has the drawback that it significantly increases the current consumption for users who do use the PD option of the same chip. To solve this problem, we designed a nonlinear power-up circuit which drives a floating pin into the HIGH state and yet has a low input impedance, while in the HIGH, or FLOATING state consume no current, its current in LOW state is also very low. This circuit is applied in a smart temperature sensor [1] that optionally can be used in packages with three pins only (same as existing chip [2]), without PD option. With such an internal pull up circuit, the power down pin can left unwired. While in other applications, the same chip can be used in packages with four pins, including a PD pin.

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II. PROPOSED CIRCUIT

A very common, but not power-efficient, pull-up circuit consists of just a pull-up resistor *R* (Fig.1 (a)). With a 5V supply, limitation of the current in the power-down mode to, for instance, 5µA would require that *R*> 1MΩ. Such a high resistance would make the input circuit rather sensitive for interference. This shows that for low-power application it would be desirable to use a non-linear pull-up resistor, which offers a low resistance in the power-up state with floating PD pin, and a low current consumption in an externally-controlled PD state. This concept shows some similarity to that of open-drain signal busses using pull-up resistor (Fig.1 (b)). Selection of the resistor value poses the problem that with a small resistor the pull-down current is large, while with a large resistor the rise time will be large. One solution to this problem is to make a nonlinear resistor by switching [3] or in a more advanced way [4].

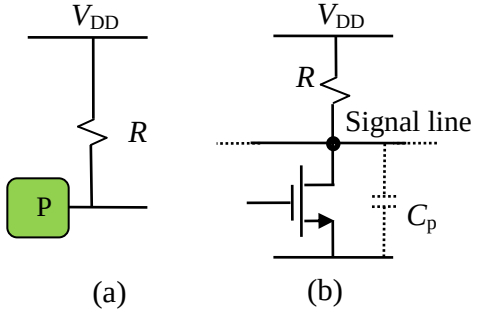

Fig. 1. (a) Resistor power-up circuit; (b) Resistor pull-up circuit for open collector signal line.

Figure 2 shows the proposed low-current power-up circuit for the PD pin. Node PD_i is a chip pin which may be connected to a package pin or can be left floating. In principal this node can also be used to power-down the chip circuitry. However, in that case the parasitic capacitor at node PD_i will be larger. As will be described below, this makes power up slower. Instead, we use the output of node PD_o, which has the same logic level as node PD_i, as power-down control signal.

To understand the behavior of the circuit depicted in Fig. 2, we first suppose that input pin PD_i is floating (not connected) and the power supply is just turned on. Furthermore, we suppose that the parasitic capacitor C_p at node PD_i has no charge and that the voltage V_{PDi} at this node is zero. Then, transistor M2 is conductive, so that the voltages at nodes A and PD_o are V_{dd} and *'0'*, respectively. With this condition, transistor M_3 is turned OFF, and the

only current that charges parasitic capacitor C_p is the drain current I_{d6} of transistors M_6.

In the LOW state of node PD_o, as long as the voltage V_{PDi} is lower than the PMOS threshold voltage $|V_{TP}|$, transistor M_6 is in saturation. When transistors M_6 and M_7 have the same size, and when we ignore the body effect, then it can be shown that the charging current of C_p amounts to about:

$$I_{d6} = \frac{\mu_p C_{ox} W_7}{2L_7}\left(V_{dd}/2 - |V_{Tp}|\right)^2, \qquad (1)$$

where, μ_p, C_{ox}, W and L represent the mobility of holes in the channel, the gate-oxide capacitance per unit area, channel width, and channel length, respectively.

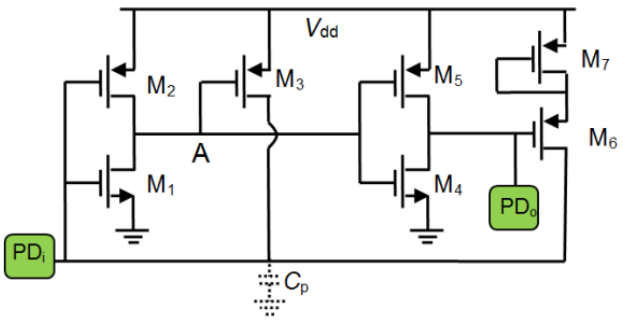

Fig. 2. Proposed power-up circuit

The first inverter M_1 and M_2 has been designed in such a way that, before the voltage at node PD_i, reaches the value $|V_{TP}|$ (before M_6 goes into ohmic region), its output switch to low state and turns on the transistor M_3. This can be set by selecting $W_1/L_1 >> W_2/L_2$. After this transition, the voltage at node PD_o goes to the HIGH state and turns off transistors M_6 and M_7, which are not needed anymore, while transistor M_3 completes charging of C_p, with a much larger current. When V_{PDi} approaches V_{dd}, transistor M_3 is driven into its ohmic region. Its channel resistor R_{DS} equals the input resistance R_{PDiH} for the HIGH state of input pin PD_i, and amounts to:

$$R_{PDiH}{}^{-1} = \frac{\mu_p C_{ox} W_3}{L_3}\left(V_{dd} - |V_{Tp}|\right), \qquad (3)$$

By appropriate selection of W_3/L_3, the required equivalent pull-up resistor for HIGH state R_{PDiH} can be set.

As can be realized, the equivalent pull-up resistor for HIGH state is set by M_3, while the current consumption in PD mode (LOW state) is set by M_6 and M_7 which can make the design of this circuit very flexible: Using small transistor for M_6 and M_7 will guarantee that the current in the (externally-controlled) PD mode is low. While the use of a larger transistor for M_3 guarantees that with a floating PD_i pin and as soon as the voltage is pulled up to the HIGH state, this pin is connected with a low-impedance R_{PDiH} to V_{dd}.

III. Simulation and Measurement Results

The proposed circuit was implemented in 0.7µm standards CMOS technology. As mentioned before, this circuit is used in smart temperature sensors, which should work with supply voltages ranging from 2.7V to 5.5V (with a typical value of 3.3V), and a temperature range of -45ºC to 130ºC. We designed the pull-up circuit to have a current consumption of less than 1µA for whole range of supply and an equivalent pull-up resistor of about 25 kΩ for V_{dd} =3.3V, T=300ºK. Another point of interest was the minimum available current for charging parasitic capacitor C_p. In case of a floating condition of the PD_i pin, this current should be large enough to guarantee a rapid ramp up of V_{PDi}.

To meet our specification the sizes of the transistors have been selected as:

$$\frac{W_6}{L_6} = \frac{W_7}{L_7} = \frac{2\mu m}{40\mu m} \;\&\; \frac{W_3}{L_3} = \frac{2\mu m}{2\mu m}\&$$

$$\frac{W_1}{L_1} = \frac{30\mu m}{0.7\mu m} \;\&\; \frac{W_2}{L_2} = \frac{2\mu m}{2\mu m} \;\&\; \frac{W_4}{L_4} = \frac{2\mu m}{0.7\mu m} \;\&\; \frac{W_5}{L_5} = \frac{6\mu m}{0.7\mu m}.$$

Figure 3 shows the simulated and also measured quasi static I-V characteristic of the input PD_i for V_{DD}=3.3V at room temperature. The simulations has been performed in Cadence software with typical transistor parameters along with worse case corners. It should be mentioned that the two inverters (Fig. 2) only consume some current during the transition of the voltage V_{PDi} during powering up. As can be realized the measured value is in very close agreement with predicted value in the simulator. With external control of pin PD_i, when V_{PDi} is LOW, the measured current has a very low value of about 80nA. With a floating pin PD_i, in the steady-state condition, this pin is strongly connected to V_{DD}. The equivalent resistor in this state is equals to the slope of the curve in Fig. 3 for V_{PDi}= 3.3V and its measured value amounts to about 26 kΩ.

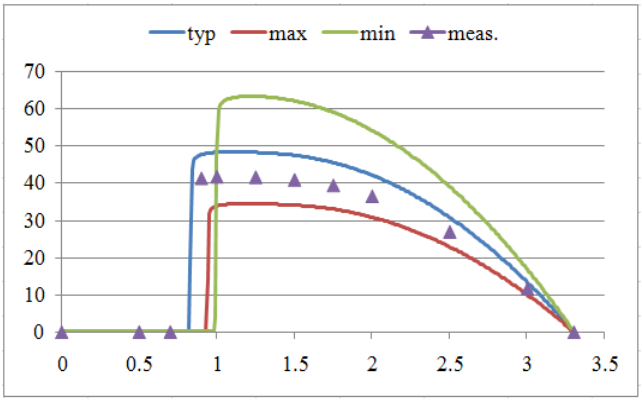

Fig. 3. The simulated and measured I-V characteristic at pin PDi for VDD=3.3V and T=300ºK.

Figure 4 shows the measured and simulated supply current in low state (PD state) versus supply voltage at room temperature. The simulation result is for typical transistor parameter and also for worse case corners. The maximum simulated current is about 1.6µA and the minimum is about 2 nA. The minimum current is much larger than any possible leakage current at node PD_i and will charge the parasitic capacitance at this node with sufficient speed. The measured results in this case are also very close to simulation results. It should be mentioned here that, our temperature sensor consume about 60µA. Therefore the power down current of about 1µA is small enough.

To find the range of charging current in low state and also the maximum pull-up resistance in the HIGH state R_{PDiH} we need to consider all corner including supply and temperature range. The minimum charging current will happen at minimum supply voltage, 2.7V at -45C and amounts to 0.2nA. While the maximum pull down current is less than 2A which happens at maximum supply voltage, 2.7V at -45C .Also the maximum pull up resistance will occur for the smallest supply voltage of 2.7V at 130C which amounts to about 50kΩ.

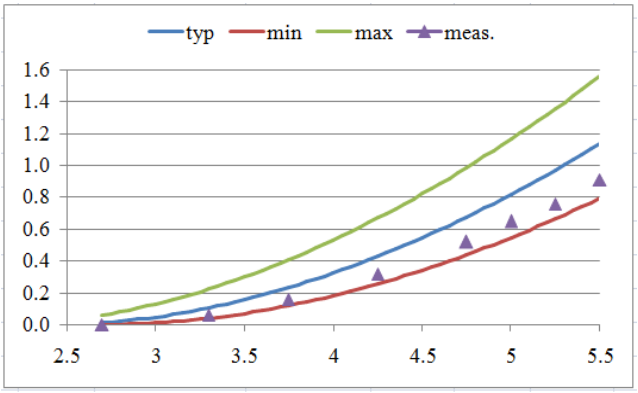

Fig. 4. Supply current versus supply voltage for different corners of technology at room temperature for LOW state (VPDi= 0) along with measured value for the same condition.

IV. CONCLUSION

A nonlinear pull-up circuit for power down pin (PD) is designed that for floating input conditions connects the PD pin to the high voltage through low-ohmic path with a resistance of about 25 kΩ for V_{DD} = 3.3 V. However, when PD pin is externally connected to ground, the power-up circuit consumes less than 0.1μA.

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