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CONTENTS

Biomedical Engineering

Circuits and Systems

Education and Learning Technologies

Embedded Systems

Instrumentation and Measurement

Microelectronics

Nanoelectronics and Technologies in Electronics

Power Electronics

Quantum, Nuclear and Optoelectronics

Testing, Quality and Reliability

Automatic Current Driven Electrode-amplifier Impedance Balance with SPLL Synchronization

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Abstract – **Power-line interference (PLI) is a common disturbing factor in almost all groundfree biosignal acquisition applications. The main cause of interference is the body to amplifier Wheatstone bridge imbalance. The bridge is formed from electrode impedances and the amplifier common mode input impedances. Because the electrode impedances vary with time, the Wheatstone bridge tends to be imbalanced and produces differential PLI which is amplified together with the useful signal. The interference can be canceled only when the bridge is kept continuously in balanced conditions. It was shown how the Wheatstone bridge can be adjusted to maintain balanced conditions by means of Voltage-Controlled-Current-Sources (VCCSs) and synchronous detection. For proper demodulation, an accurate synchronization with PLI is needed. Recently, dedicated software PLL (SPLL) for PLI synchronization was developed implemented and tested. This paper presents a complete, VCCS based, impedance balancing approach wherein synchronization to PLI is done with the designed SPLL. The stability of the whole system is proven by Matlab mixed signal simulations. The presented approach is applicable in various two-electrode applications, such as Holter monitors, external defibrillators, ECG monitors and other heart beat sensing biomedical devices.**

Keywords – **Wheatstone bridge, Power-line interference, Lock-in demodulator, VCCS, Software PLL**

I. Introduction

In ground-free biosignal amplifications (e. g. two-electrode) the common mode interference current must flow via the same electrodes used for the signal sensing. The electrode impedances Z_e and the amplifier common mode impedances Z_{cm} form a Wheatstone bridge, see *Fig. 1* [1].

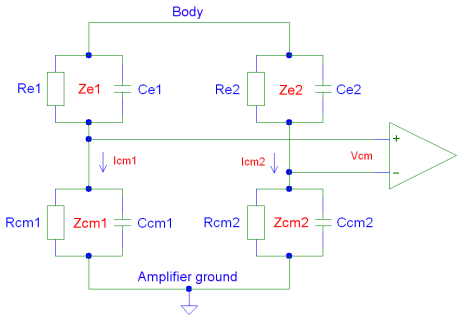

Fig. 1 Body-amplifier interface

Only when the two shoulders Z_{e1}, Z_{cm1} and Z_{e2}, Z_{cm2} of the formed Wheatstone bridge are balanced, the Power-line interference (PLI) is not converted into a differential voltage. The electrode-skin impedances Z_{e1} and Z_{e2}, by their nature, are not set at a precise value and will change from individual to individual, with electrode location and with time on the same person. Their voltage drop can be equalized only when the input currents I_{cm1} and I_{cm2} are continuously adjusted to track the electrode impedance variations with time, to fulfill Eq. (1):

$$Z_{e1}I_{cm1} = Z_{e2}I_{cm2} \qquad (1)$$

Using common mode voltage controlled current sources (VCCSs) to generate I_{cm1} and I_{cm2}, the amplifier common mode impedances Z_{cm1}, and Z_{cm2} can be synthesized [2, 3]. Moreover, if the amplitude of one current is changed or is delayed towards the other, the impedance balance can be achieved automatically [1]. A digital approach for Wheatstone bridge impedance balance was developed [4]. It is based on two digital lock-in demodulators detecting the real and imaginary parts of PLI. Two digital control loops are used for automatically adjusting the real and imaginary components of the amplifier common mode input impedances in order to fulfill Eq. (1). For proper demodulation, the approach needs accurate synchronization with PLI.

Recently, dedicated software PLL was developed [5, 6, 7]. It generates sinusoidal and rectangular waveforms, synchronous with the fundamental harmonic of PLI, and tolerates large variations of PLI amplitude. The SPLL is intended to be used for synchronization in groundfree biosignal acquisition. This paper presents a complete current driven impedance balancing system wherein synchronization to PLI is done with the designed SPLL. The stability of the whole system is proven by mixed signal Matlab simulations with real ECG signal. The presented method is applicable in almost all grounfree biosignal applications.

II. Impedance Balance Concept

Simplified current driven impedance balancing concept is shown in *Fig. 2*. Z_{e1} and Z_{e2} are the electrode impedances represented by two parallel RC networks with R_e=10k and C_e=100nF. The amplifier input impedances Z_{cm1} and Z_{cm2} are synthesized by *VCCS1* and *VCCS2* generating the input common mode currents I_{cm1} and I_{cm2}. The VCCSs are built on Howland scheme, analyzed in [2]. The dfferential signal is amplified 200 times at node V_{ecg}, common mode signal 2

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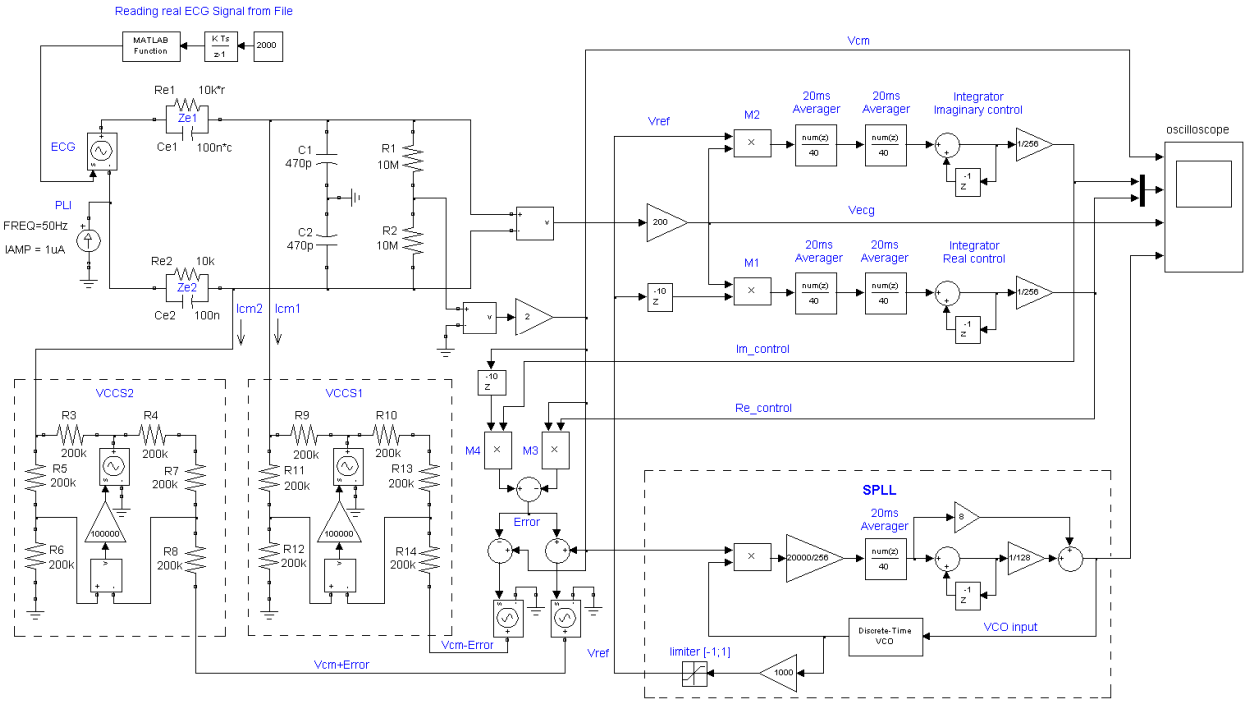


Fig. 2 Current driven electrode-amplifier impedance balance schematic for simulation in Matlab Simulink environment

times at node V_{cm}. If VCCSs transconductance is *gm*, the synthesized common mode resistance per input, when *Error* signal is zero is:

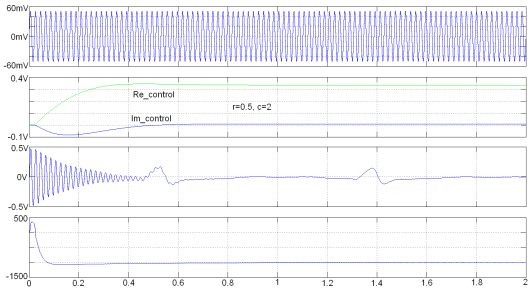
$$R_{cm} = \frac{1}{2gm} \qquad (2)$$

Let's assume that the common mode signal V_{cm} consists of only the fundamental harmonic of the PLI, i. e. it is a pure 50Hz sine wave. The first mixer *M1* detects the presence of real part of PLI in the V_{ecg}. The second mixer *M2* is controlled by 5ms ($\pi/2$ for PLI) delayed reference, and detects the presence of imaginary part of PLI in the V_{ecg}. The outputs of the two mixers are low-pass filtered by two cascaded 1PL period moving-average filters. Note that 1PL period moving-average filter is a comb filter, and rejects all harmonics of PLI. The filter outputs are integrated and scaled with a gain coefficient k=1/256, and are enclosed in two negative feedback loops. The control loops are used to generate real and imaginary error signals. The error signals are added at *VCCS2* input, and subtracted at *VCCS1* input from the common mode voltage V_{cm} controlled the VCCSs. It should be noted that the two VCVS's are controlled from the common mode voltage, thus the differential input impedance is uninfluenced, and only the common mode input impedance is changed due to circuit operation. In steady-state conditions the integrator outputs *Re_control* and *Im_control* settles at voltages, at which the mixers *M1* and *M2* will detect the absence of in-phase (real part) and quadrature-phase (imaginary part) of PLI in the ECG signal. The two negative feedback control loops automatically equalize the electrode voltage drops, due to changed amplitude and delay between *Icm1* and *Icm2*, and cancel the PLI.

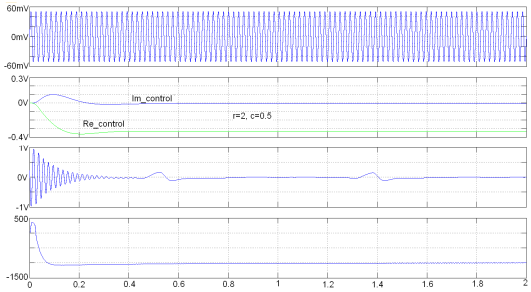
It is important to note that for proper demodulation the mixers *M1* and *M2* should operate synchronously with the PLI. A few samples phase shift is tolerable, but if the phase difference becomes larger, it will cause instability problems and lack of convergence (the sign of the two feedbacks could be changed from negative to positive). That is why, dedicated software PLL was designed and implemented [5, 6, 7]. For easy operation, the two mixers *M1* and *M2* are switching type, and operate with rectangular ±1LSBs references.

III. Simulation Results with SPLL

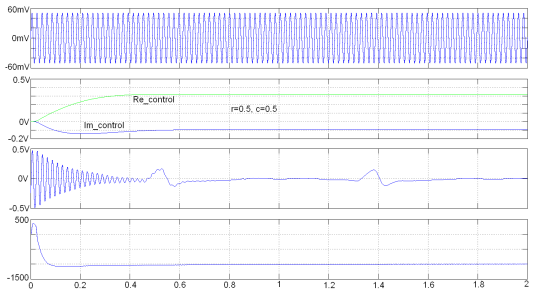
Matlab Simulink simulations of the circuit from *Fig. 2* for PLI frequencies 49Hz, 50Hz and 51Hz are shown in *Fig. 3*, *Fig. 4* and *Fig. 5*. A real ECG signal is read from a file by a Matlab function, and is used in the simulations. Five cases of electrode imbalance are simulated by parameters *r* and *c*. The shown signals are as follows. V_{cm} is shown on the first trace. The second trace shows control signals *Re_control* and *Im_control*. The third trace shows V_{ecg}. The forth trace is the VCO input of the SPLL. It can be seen that the Wheatstone bridge goes automatically in balanced condition, and the PLI is canceled. *Re_control* and *Im_control* signals have stable response in all variations of PLI frequency and simulated mismatch. VCO sensitivity is 1mHz/LSB. When PLI frequency varies ±1Hz, VCO input is settled to about ±1000LSBs. VCO input is settled several times faster than *Re_control* and *Im_control*.



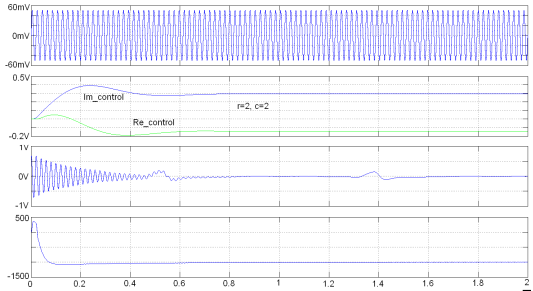
a) f_{PLI}=49Hz, r=0.5, c=2



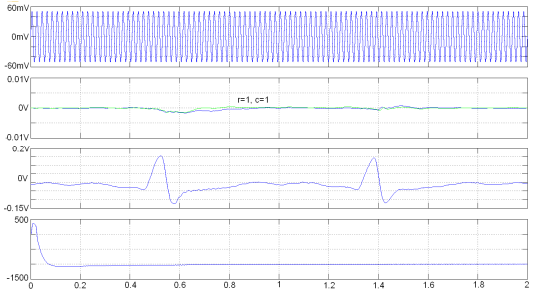
b) f_{PLI}=49Hz, r=2, c=0.5



c) f_{PLI}=49Hz, r=0.5, c=0.5

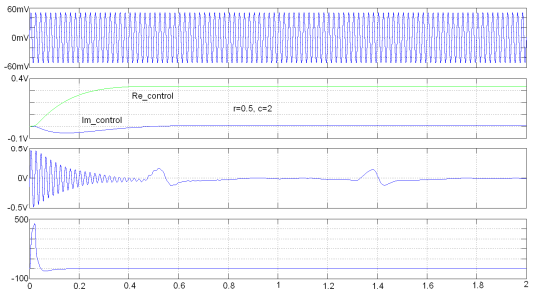


d) f_{PLI}=49Hz, r=2, c=2

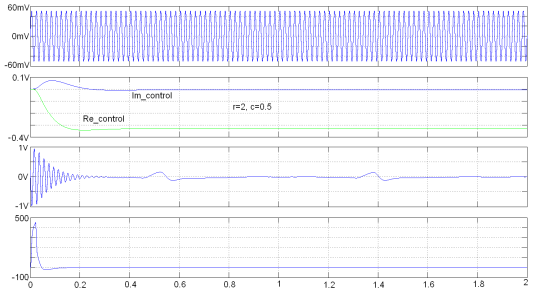


e) f_{PLI}=49Hz, r=1, c=1

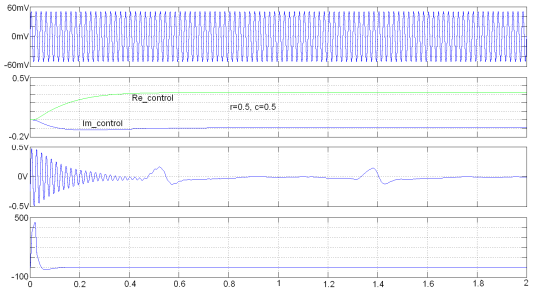
Fig. 3 Matlab simulation results with five cases of different electrode imbalance. f_{PLI}=49Hz, I trace: V_{cm}, II traces: Re_control (green) and Im_control (blue), III trace: V_{ecg}, IV trace: SPLL VCO input



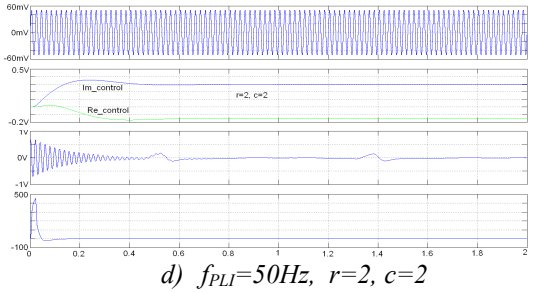
a) f_{PLI}=50Hz, r=0.5, c=2



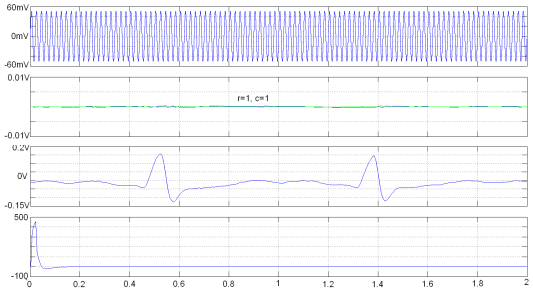
b) f_{PLI}=50Hz, r=2, c=0.5



c) f_{PLI}=50Hz, r=0.5, c=0.5

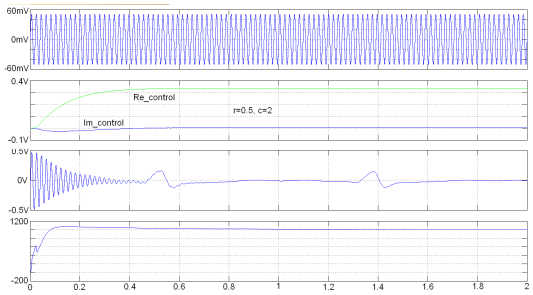


d) f_{PLI}=50Hz, r=2, c=2

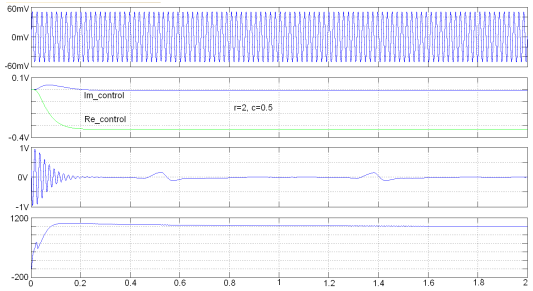


e) f_{PLI}=50Hz, r=1, c=1

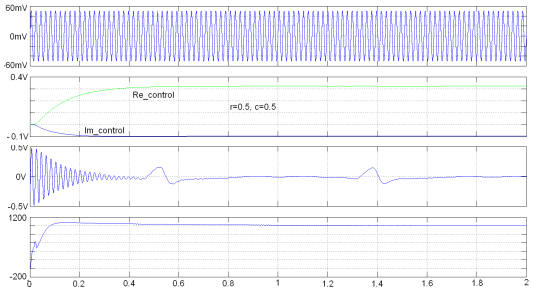
Fig. 4 Matlab simulation results with five cases of different electrode imbalance. f_{PLI}=50Hz, I trace: V_{cm}, II traces: Re_control (green) and Im_control (blue), III trace: V_{ecg}, IV trace: SPLL VCO input



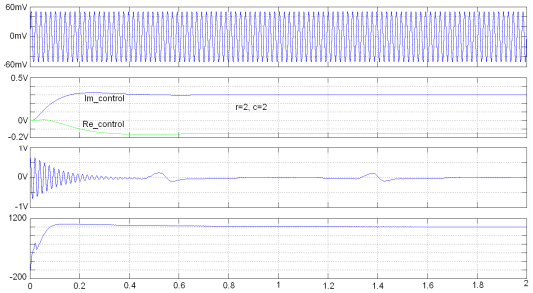
a) f_{PLI}=51Hz, r=0.5, c=2



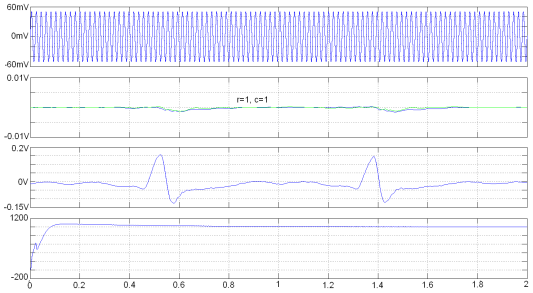
b) f_{PLI}=51Hz, r=2, c=0.5



c) f_{PLI}=51Hz, r=0.5, c=0.5



d) f_{PLI}=51Hz, r=2, c=2



e) f_{PLI}=51Hz, r=1, c=1

Fig. 5 Matlab simulation results with five cases of different electrode imbalance. f_{PLI}=51Hz, I trace: V_{cm}, II traces: Re_control (green) and Im_control (blue), III trace: V_{ecg}, IV trace: SPLL VCO input

IV. Conclusion

The presented impedance balancing approach breaks the gap between two and three-electrode amplification techniques in regards the quality of achieved signals. The PLI is cancelled on a hardware level - wherein it is generated, without affecting the spectrum of the useful signal. In comparison with impedance balancing approach [12], the usage of current sources is a flexible and easier way for modeling the amplifier common mode input impedances. At the same time, the differential input impedance preserves its high value.

Finally, it should be noted that due to the first order impedance synthesis in some cases the impedance balance could not be perfect. Popular PLI removing algorithms could be used in addition, such as subtraction procedure [8], lock-in techniques [9] and high-Q comb IIR or FIR filters [10, 11].

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Automatic Common Mode Electrode-amplifier Impedance Balance with SPLL Synchronization

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Abstract – **Power-line interference (PLI) is a major disturbing factor in almost all groundfree biosignal acquisition applications. The main cause of interference is body to amplifier Wheatstone bridge imbalance. The bridge is formed from electrode impedances and the amplifier common mode input impedances. Because the electrode impedances vary with time, the Wheatstone bridge tends to be imbalanced, and produces differential PLI which is amplified together with the useful signal. The interference can be canceled only when the bridge is kept continuously in balanced conditions. It was shown how the Wheatstone bridge can be adjusted to maintain balanced conditions by means of two digital synchronous demodulators. For proper demodulation, an accurate synchronization with PLI is needed. Recently, dedicated software PLL (SPLL) for PLI synchronization was developed implemented and tested. This paper presents a complete impedance balancing approach wherein synchronization to PLI is done with the designed SPLL. The stability of the whole system is proven by Matlab mixed signal simulations. The presented approach is applicable in various two-electrode applications, such as Holter monitors, external defibrillators, ECG monitors and other heart beat sensing biomedical devices.**

Keywords – **Wheatstone bridge, Power-line interference, Lock-in demodulator, Synchronous detection, Software PLL**

I. Introduction

In two-electrode biosignal amplifications the common mode interference current must flow via the same electrodes used for the signal sensing. The electrode impedances (Z_e) and the amplifier common mode impedances (Z_{cm}) form a Wheatstone bridge, see *Fig. 1* [1].

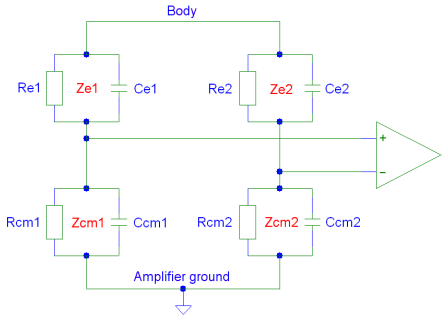

Fig. 1 Body-amplifier interface

Only when the two shoulders Z_{e1}, Z_{cm1} and Z_{e2}, Z_{cm2} of the formed Wheatstone bridge are balanced the PLI is not converted into a differential voltage. But the electrode-skin impedances, by their nature, are not set at a precise value, and will change from individual to individual, with electrode location, and with time on the same person. This means that, it is impossible to match one thing with a fixed value, like amplifier common mode input impedances, to another with a different nature (ion transfer by sustained chemical reactions) and variable values, like electrode impedances. Matching is possible only when the amplifier common mode impedances are continuously adjusted to track the electrode impedance variations with time [1].

A digital approach for Wheatstone bridge impedance balance was developed [2]. It is based on two digital lock-in demodulators detecting the real and imaginary parts of PLI. Two digital control loops automatically adjust the resistive and capacitive components of the amplifier common mode input impedances in order to balance the Wheatstone bridge, and to maintain it in balanced conditions. For proper demodulation, the approach needs accurate synchronization with PLI.

Recently, dedicated software PLL was developed [3, 4, 5]. It generates sinusoidal and rectangular waveforms, synchronous with the fundamental harmonic of PLI, and tolerates large variations of PLI amplitude. The SPLL is intended to be used for synchronization in ground-free biosignal acquisition with input impedance balance. This paper presents a complete impedance balancing system wherein synchronization with PLI is done with the designed SPLL. The stability of the whole system is proven by mixed signal Matlab simulations with real ECG signal. The presented method is applicable in almost all ground-free biosignal applications.

II. Impedance Balance Concept

Simplified impedance balancing concept is shown in *Fig.2*. Z_{e1} and Z_{e2} are the electrode impedances represented by two parallel RC networks with R_e=10k and C_e=100nF. Z_{cm1} and Z_{cm2} are the amplifier input impedances. They are also parallel RC networks, and have values R_{cm}=2MΩ and C_{cm}=2nF. Differential signal is amplified 200 times at node V_{ecg}, common mode signal 2 times at node V_{cm}. Driving R_{cm} and C_{cm} with appropriate part of V_{cm}, the R_{cm} and C_{cm} values, for common mode signals, can be increased or decreased in a way to cancel the differential PLI.

The operation of the circuit shown in *Fig. 2* is as follows. Let us assume that the common mode signal V_{cm} consists of only the fundamental harmonic of the PLI, i.e. it is a pure 50Hz sine wave. The first mixer *M1* detects the

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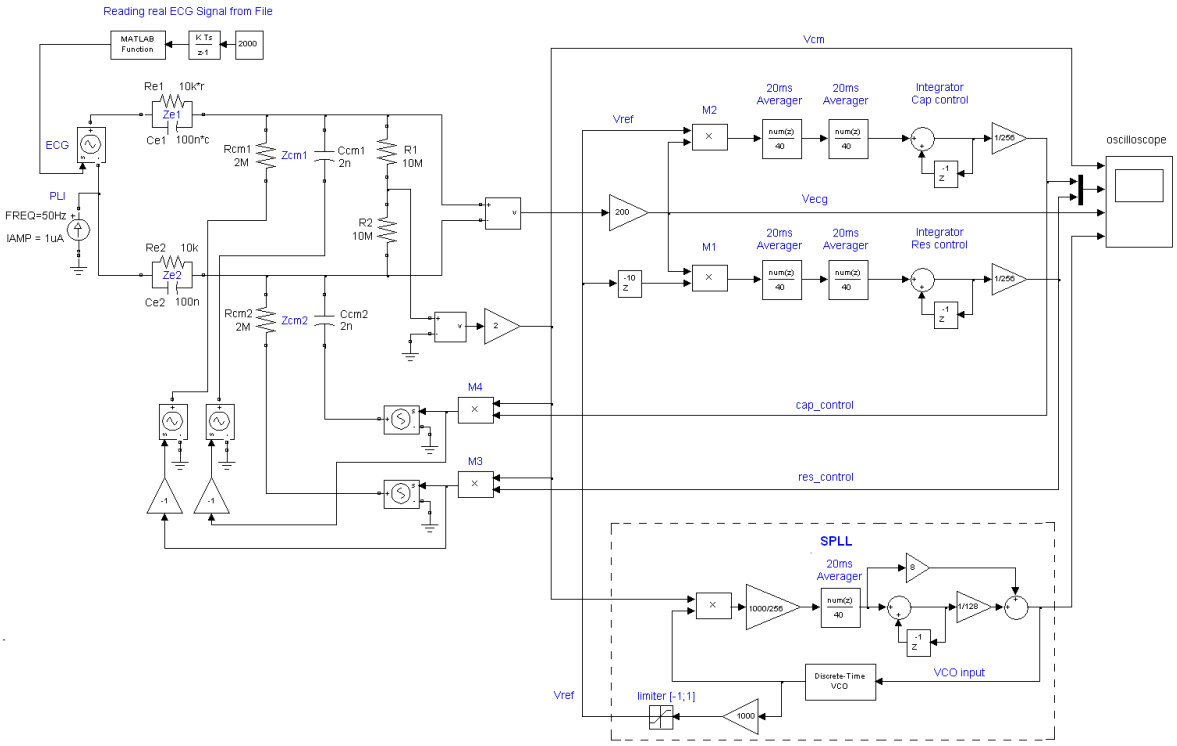


Fig. 2 Common mode electrode-amplifier impedance balance schematic for simulation in Matlab Simulink environment

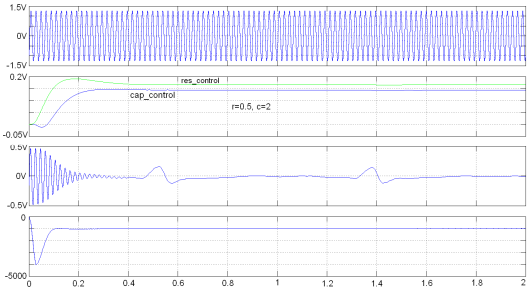
presence of in-phase PLI in the V_{ecg}. The second mixer *M2* is controlled by a $\pi/2$ (or 5ms) delayed reference and detects the presence of quadrature-phase PLI in the V_{ecg}. The outputs of the two mixers are low-pass filtered by two cascaded 1PL period moving-average filters. Note that 1PL period moving-average filter is a comb filter and rejects all harmonic of PLI. The filter outputs are integrated and scaled with a gain coefficient k=1/256, and are enclosed in two negative feedback loops. The loops are used to control the resistive and capacitive components of the amplifier input impedances. Thus, two control loops are organized, one for in-phase resistive control, and the other for quadrature-phase capacitive control. The two averagers introduce a group delay of 20ms. The sampling rate is F_s=2kHz and corresponds to an integration time constant τ_i=1/F_s=0.5ms or to an integrator unity gain frequency f_i=1/(2$\pi\tau_i$)=318Hz. To filter out the PLI fundamental harmonic, and to ensure stable operation, the integrator time constant must be increased to overcome the introduced 20ms group delay of the two averagers. Dividing the integrator outputs e. g. by 256, or introducing a gain k=1/256, the integrator time constant is increased to τ_i=128ms, corresponding to the loop bandwidth of about 1Hz, and ensures stable operation.

At steady-state condition the integrator outputs *res_control* and *cap_control* settle at voltages, for which the mixers *M1* and *M2* will detect the absence of in-phase and quadrature-phase PLI in the ECG signal. Thus, the two negative feedback control loops automatically balance the body to amplifier Wheatstone bridge, and cancel the PLI. It should be noted that the mixers *M3* and *M4* are controlled from the common mode voltage V_{cm}, thus the differential input impedance is uninfluenced, and only the common mode input impedance is changed due to circuit operation. For higher differential input impedance, R_{cm} can be bootstrapped [6]. In practice, the mixers *M3* and *M4* can be replaced by digital potentiometers [1, 2].

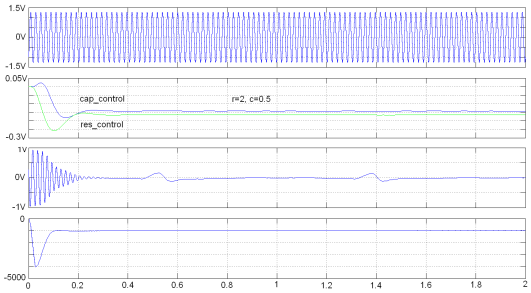
It is important to note that for proper demodulation the mixers *M1* and *M2* should operate synchronously with the PLI. A few samples phase shift is tolerable, but if the phase difference becomes larger, it will cause instability problems and lack of convergence (the sign of the two feedbacks could be changed from negative to positive). That is why, dedicated software PLL was designed and implemented [3, 4, 5]. For easy operation, the two mixers *M1* and *M2* are switching type, and operate with rectangular ±1LSBs in-phase and quadrature-phase references.

III. Simulation results with SPLL

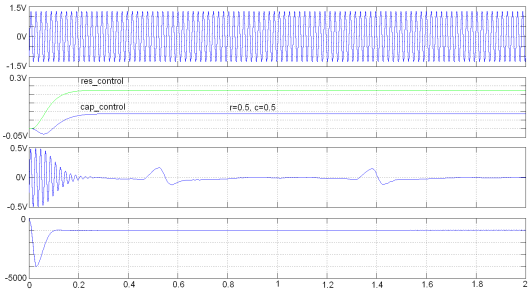
Matlab Simulink simulations of the circuit from *Fig. 2* for PLI frequencies 49Hz, 50Hz and 51Hz are shown in *Fig. 3*, *Fig. 4* and *Fig. 5*. A real ECG signal is read from a file by a Matlab function, and is used in the simulations. Five cases of electrode imbalance are simulated by parameters r and c. The shown signals are as follows. V_{cm} is shown on the first trace. The second trace shows control signals *res_control* and *cap_control*. The third trace shows V_{ecg}. The forth trace is the VCO input of the SPLL. It can be seen that the Wheatstone bridge goes in balanced condition, and the PLI is canceled. *Res_control* and *cap_control* signals have stable response in all variations of PLI frequency and simulated mismatch. VCO sensitivity is 1mHz /LSB. When PLI frequency varies ±1Hz, VCO input is settled to about ±1000LSBs. VCO input is settled several times faster than *res_control* and *cap_control*.



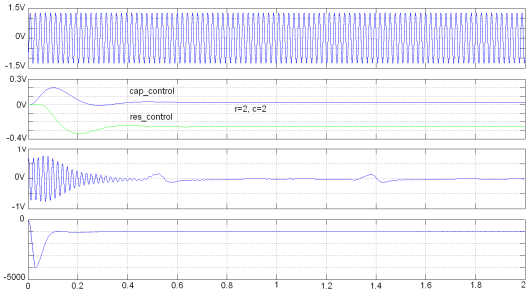
a) f_{PLI}=49Hz, r=0.5, c=2



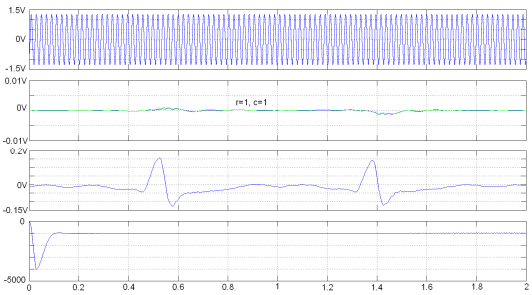
b) f_{PLI}=49Hz, r=2, c=0.5



c) f_{PLI}=49Hz, r=0.5, c=0.5

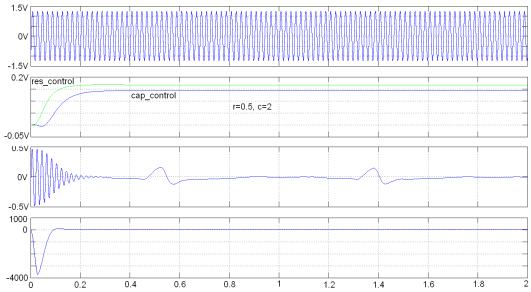


d) f_{PLI}=49Hz, r=2, c=2

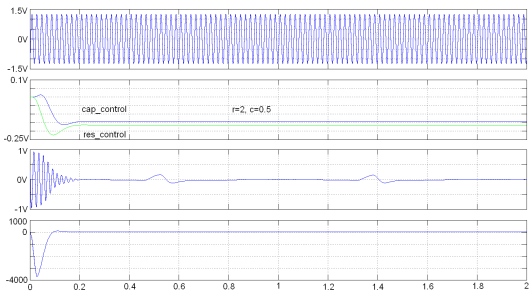


e) f_{PLI}=49Hz, r=1, c=1

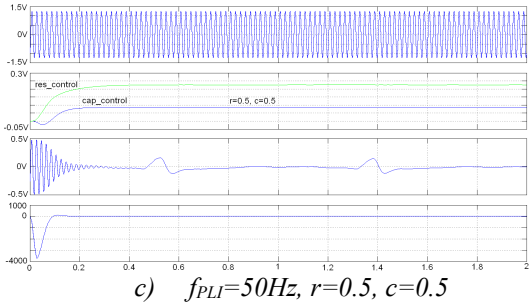
Fig. 3 Matlab simulation results with five cases of different electrode imbalance. f_{PLI}=49Hz, I trace: V_{cm}, II traces: res_control (green) and cap_control (blue), III trace: V_{ecg}, IV trace: SPLL VCO input



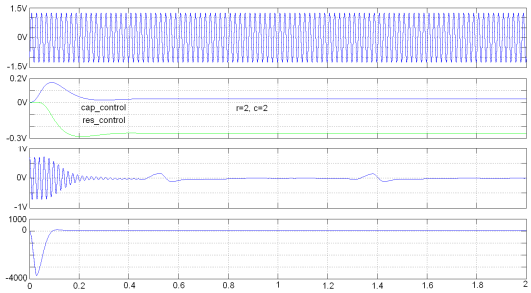
a) f_{PLI}=50Hz, r=0.5, c=2



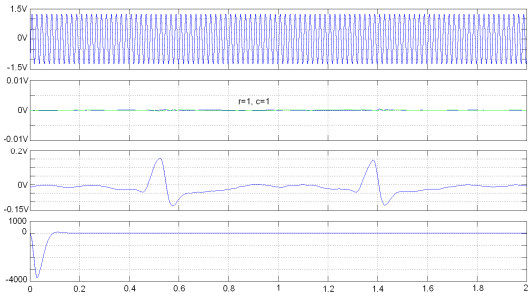
b) f_{PLI}=50Hz, r=2, c=0.5



c) f_{PLI}=50Hz, r=0.5, c=0.5

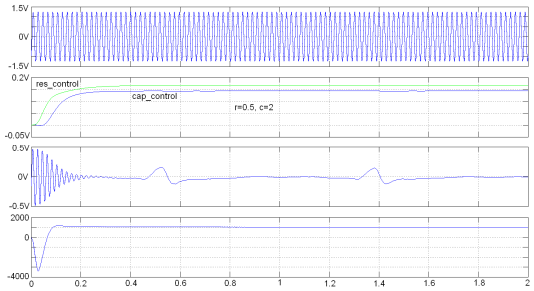


d) f_{PLI}=50Hz, r=2, c=2

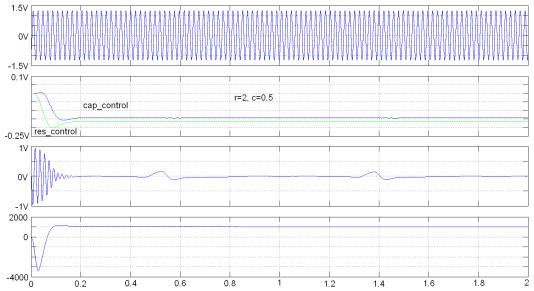


e) f_{PLI}=50Hz, r=1, c=1

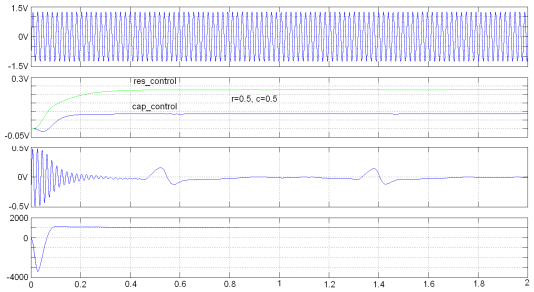
Fig. 4 Matlab simulation results with five cases of different electrode imbalance. f_{PLI}=50Hz, I trace: V_{cm}, II traces: res_control (green) and cap_control (blue), III trace: V_{ecg}, IV trace: SPLL VCO input



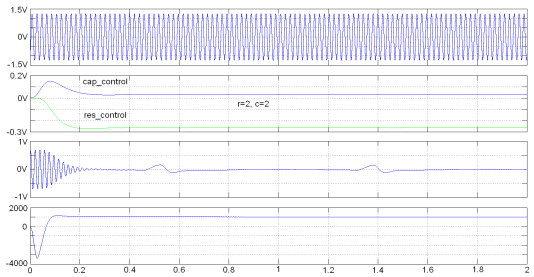
a) f_{PLI}=51Hz, r=0.5, c=2



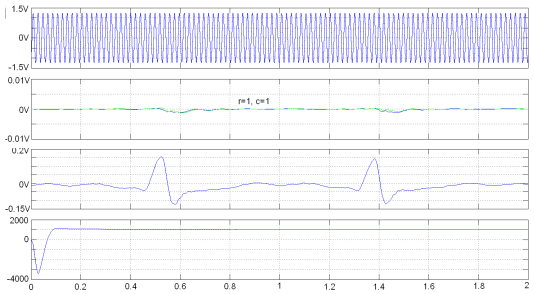
b) f_{PLI}=51Hz, r=2, c=0.5



c) f_{PLI}=51Hz, r=0.5, c=0.5



d) f_{PLI}=51Hz, r=2, c=2



e) f_{PLI}=51Hz, r=1, c=1

Fig. 5 Matlab simulation results with five cases of different electrode imbalance. f_{PLI}=51Hz, I trace: V_{cm}, II traces: res_control (green) and cap_control (blue), III trace: V_{ecg}, IV trace: SPLL VCO input

IV. Conclusion

The presented impedance balancing approach breaks the gap between two and three-electrode amplification techniques in regards the quality of achieved signals. The PLI is cancelled on a hardware level - wherein it is generated, without affecting the spectrum of the useful signal.

The presented approach is suitable for low-cost microcontrollers. It is a software approach, so it has no production cost. Moreover, flexible algorithms could make the impedance balancing process faster and insensitive to the level of interference, e. g. V_{cm} Automatic Gain Control (AGC), changing the loop bandwidth during operation, etc.

Finally, it should be noted that due to the first order impedance synthesis in some cases the impedance balance could not be perfect. Popular PLI removing algorithms could be used in addition, such as subtraction procedure [7, 8, 9], lock-in techniques [10] and high-Q IIR or FIR comb filters [11, 12].

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LabVIEW Based ECG Signal Acquisition and Analysis

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Abstract – **This paper presents a LabVIEW based system of acquisition, processing and analysis of ECG (electro-cardiogram) signals. Biomedical signal acquisition has made great advances in recent years due to the introduction of modern hardware and software technologies. Computer based signal processing systems are becoming an efficient approach for acquisition and analyzing of such signals. In our implementation an AD8232 integrated signal conditioning front end of Analog Devices is used for measurement and pre-processing of the ECG signals. Battery powered data acquisition system, which avoids 50Hz noise and allows for safety measurement without additional isolation is employed. LabVIEW Biomedical Toolkit time-domain analysis is applied to study heart rate variability together with additional parameters.**

Keywords – **ECG signal time-domain analysis, battery powered LabVIEW DAQ, heart rate variability**

I. INTRODUCTION

Health monitoring is now becoming part of everyday life. Today's healthcare industry aims to provide better health services to people in an efficient and patient friendly manner.

Electrocardiogram (ECG) devices measure the electrical activity of the heart muscle in order to determine heart conditions. ECG signal quality is a key factor in diagnosing diseases of the heart. The electrocardiogram is a diagnostic tool that measures and records the electrical activity of the heart in detail. An exact interpretation allows diagnosing of a wide range of heart conditions. These conditions can vary from minor to life threatening [1]. An ECG is generated by a nerve impulse stimulus to the heart. The current is diffused around the body surface and builds on a voltage drop. This drop is in range (an interval of a couple) of μV to mV and is with a wide impulse variation, which requires significant and precise amplification [2].

LabVIEW based ECG acquisition and analysis is shown to provide a robust and efficient environment for successful estimation of heart activity problems [3]. This article presents an ECG signal Time-Domain Analysis assisted by LabVIEW Biomedical Toolkit. Modern software toolkits provide efficient removal of baseline wandering, noise cancellation, as well as QRS complexes and heart rate detection [4].

A portable heart rate monitor is developed using AD8232 integrated Analogue Front End (AFE) of Analog Devices [5]. Typically, pre-processing of the bio-potential signals is needed, to insure proper measurement of ECG data. Pre-processing of ECG signals is usually performed by AFEs, which provide amplification, filtering and noise removal from the acquired signals. To prevent ECG measurements contamination by power line interference, a battery powering of measurement equipment is often preferred, but there are still other noise sources [4]. The baseline wandering and other wideband noises are not easy to be suppressed by hardware devices. Instead, the use of software is a more powerful and feasible means for ECG signal processing.

In our study we applied the Time-Domain Analysis of LabVIEW Biomedical toolkit to resolve statistical and geometric measures of Heart Rate Variability in ECG data. HRV has the potential to provide valuable insight into physiological and pathological conditions [6]. Our contribution aims to explore the possibility of implementing portable heart rate monitors by means of modern software tools.

II. HEART RATE VARIABILITY

A normal one-cycle ECG signal consists of several waves, as shown in Fig. 1. The wave with the highest amplitude is the R wave. An RR interval is the time elapsed between two successive R waves. The waves with the lower amplitudes are the P wave, the T wave, and the U wave. RR intervals show the variation between consecutive heartbeats. Heart rate variability (HRV) measurements analyze how these RR intervals change over time.

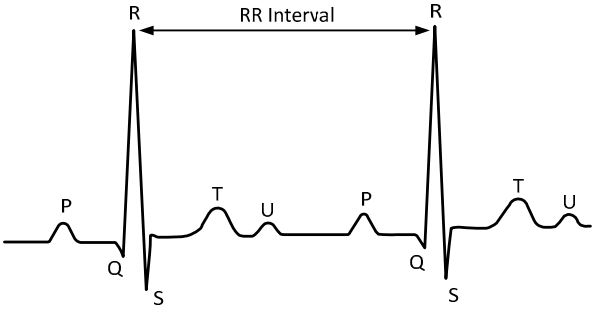

Fig. 1. R Peaks and RR Intervals of an ECG Signal **[7]**.

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A. Acquiring RR Intervals

To analyze heart rate variability (HRV), the RR intervals must first be acquired and pre-processed by AD8232 Analogue Front End. Fig. 2 shows the process of acquiring RR intervals.

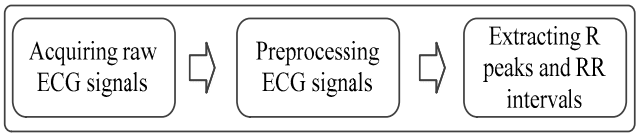

Fig. 2. RR Interval Acquisition Process [7].

B. Extracting RR Intervals from ECG Signals

The extraction process usually involves a preprocessing step and a peak detection step. It is necessary to preprocess the raw ECG signals if they have noise corruption and a significant baseline trend. You can then detect the R peaks by thresholding or by using the wavelet-based peak detection method to compute the RR intervals.

The Biomedical Toolkit also contains a Heart Rate Variability Analyzer application for convenient HRV analysis.

III. HARDWARE

A. ECG Analog Front AD8232

A number of analog front ends for ECG applications are available on the market. The main characteristics of some of the tested chips are shown in Table 1.

TABLE 1. ANALOG FRONT ENDS FOR ECG.

Parameter	AFE			
	AD8232	*ADS1293*	*ADS1191*	*HM301D*
Company	AD	TI	TI	STM
Gain	100 V/V	12 V/V	12 V/V	64 V/V
Input Impedance	10 GΩ	500 MΩ	100 MΩ	50 MΩ
CMRR	80 dB	100dB	95 dB	100 dB
Features	Rail to rail output	Low noise PGA	Low noise PGA	3-channel ECG

After testing in different configurations and with different DAQs, the AFE AD8232 from Analog Devices has been chosen for our implementation due to its gain and input impedance [2]. AD8232 is an integrated signal conditioning block for ECG and other biopotential measurement applications. The main components of this Analog-Front-End (AFE) are shown in Fig. 3.

This AFE provides not only signal conditioning in terms of amplification and filtering, but also fast recovery of ECG signal after lead off condition. The built-in current-feedback instrumentation amplifier, with two well-matched transconductance amplifiers guarantees high common mode rejection and removes half-cell electrode potential. Filtering of the data measured is done by low-pass and high-pass filters. The cut off frequency of the two-pole high pass filter can be optimally selected to remove motion artifacts and the electrode half-cell potential. Additional noise is removed by three-pole low-pass filter built around AD8232 with external components.

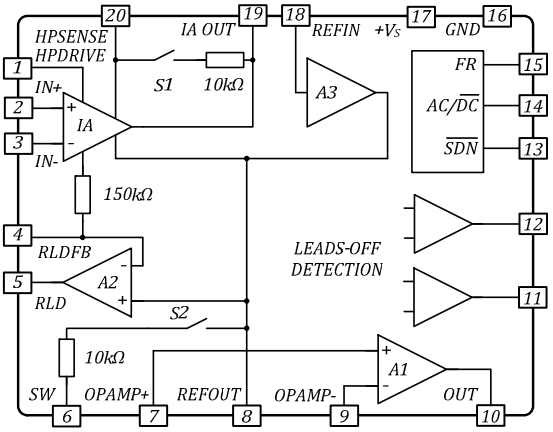

Fig. 3. AD8232 integrated signal conditioning block [2].

B. Preprocessing ECG signals

Pre-processing of ECG signals helps to removing ”contaminants” from the ECG signals efficiently. Broadly speaking, the main ECG contaminants can be classified into the following categories:

- power line interference,
- electrode pop or contact noise,
- patient–electrode motion artifacts,
- electromyographic (EMG) noise,
- baseline wandering [8].

Baseline wander is a low-frequency component present in the ECG system and it is due mainly to offset voltages in the electrodes, respiration, and body movement. This can cause problems in the analysis of the ECG waveform. The offset also limits the maximum value of gain which can be obtained from the instrumentation amplifier. At higher gains, the signal can saturate. This noise can be removed by:

- Implementing a high-pass filter using hardware. The cut-off frequency should be such that the ECG is undistorted while the baseline wander have to be removed. A typical value of the cut-off frequency is 0.05Hz. Since this cut-off frequency is very low, this method requires bulky capacitors.
- Implementing a high-pass filter in software.

The main problem in high-pass filtering distortions is the QRS complex, especially when it is monopolar, of high amplitude and great duration. Partial differentiation of such QRS complexes often occurs and results in an aftereffect component superimposed on the initial part of the ST segment, thus changing its shape [2]. This effect is stronger with higher cutoff frequencies of the high-pass filters. Time-constants in the range 0.3 -1.5s are often used in bedside monitors and Holter devices [9].

C. Data Acquisition System

The analog signals are further processed with the NI-USB DAQ6211. The NI USB-6211 is a USB-powered multifunction Data Acquisition (DAQ) module from National Instruments [10]. It is used to digitize the amplified, filtered ECG signal. The NI USB-6212 card has 8 differential analog input channels with 16-bit analog-to-

digital converter running at a sampling frequency which can be increased up to 250 kHz. This fully satisfies the requirements for digitalization of the ECG signal.

IV. LabVIEW Biomedical Toolkit Time-Domain Analysis of Heart Rate Variability

For the purpose of diagnosis various features from the preprocessed ECG data have to be extracted, including QRS intervals, QRS amplitudes, PR intervals, QT intervals, etc. These features provide information about the heart rate, the conduction velocity, the condition of tissues within the heart as well as various abnormalities. LabVIEW Biomedical Toolkit provides an ECG Feature Extractor VI, and one can select whether to detect QRS only or to detect all supported ECG features, including R position, R amplitude, iso level, QRS onset, QRS offset, P onset, P offset, T onset and T offset. Some of the Statistical and Geometric Measurements are summarized in Table 2 [7].

TABLE 2. STATISTICAL AND GEOMETRIC MEASUREMENTS.

Variable	Unit	Description
Statistical Measurements		
RR Mean & Std	s	Mean and standard deviation of all RR intervals.
HR Mean & Std	1/min	Mean and standard deviation of all heart rates.
RMSSD	ms	Square root of the mean of the sum of squares of differences between adjacent RR intervals.
NN50 Count	N/A	Number of pairs of adjacent RR intervals differing by more than 50 ms in all the measurements.
pNN50	%	NN50 count divided by the total number of all RR intervals.
Geometric Measurements		
HRV Triangular Index	N/A	Total number of all RR intervals divided by the height of the histogram of all RR intervals.
TINN	ms	Baseline width of the minimum square difference triangular interpolation of the highest peak of the histogram of all RR intervals measured on a discrete scale with bins of 7.8125 ms (1/128 s).

- No currently recognized HRV measure provides better prognostic information than the time–domain HRV measures assessing the overall HRV (e.g. SDNN or HRV triangular index).
- We used Heart Rate Variability Analyzer application to acquire these measurements [7].

V. Experimental Results

A LabVIEW application is designed consisting of two virtual instruments (VI). The first one records the signal in a file with a sampling frequency 250 Hz (for environments with network frequencies 50Hz). 16 bit NI-USB DAQ6211 connected to a notebook is used to acquire the signal data with galvanic isolation.

Signal processing is performed in the second VI where data is read from the file, filtered with the *TSA Moving Average.vi* and after low-pass- and band-pass- filtering is forwarded to the inputs of the *ECG Feature Extractor* VI.

Fig. 4 shows the real ECG signal and Extracted Features after power line interference filtering true moving averaging over five data readings, followed by low-pass and band-pass filtering. This results to some T-wave depression, but is not critical for the heart rhythm analysis.

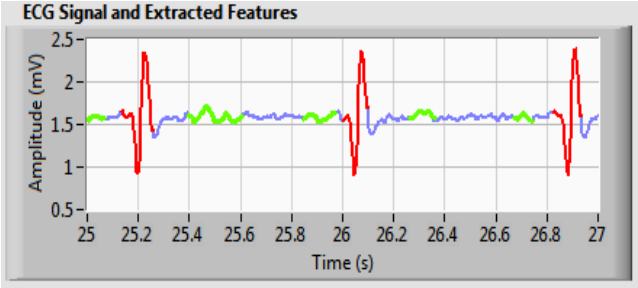

Fig. 4. ECG Signal and Extracted Features (coded with different colors).

As a result of the statistical data analysis with the *ECG feature Stats.vi* a cluster of 12 elements is obtained with basic parameters of the ECG signal. Parallel to these calculations, in a separate array the time between each two samples is stored. After these treatments, by *Show ECG Waves.vi* and *Calculate ECG Feature Stats.vi*, they may be visualized as shown in Fig. 5. In addition, the average parameter values and their standard deviations can be monitored during the whole signal recording.

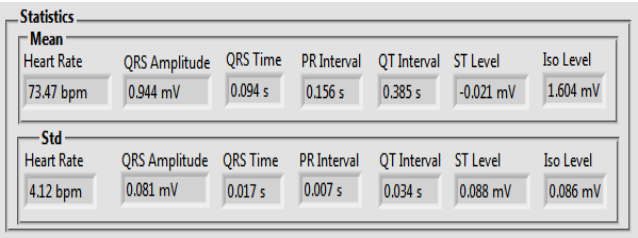

Fig. 5. Statistical data after *ECG feature Stats.vi*.

The next signal processing step is determination of the RR interval. From the cluster an array with R elements is separated and a new array is created containing the difference between each two consecutive R elements. Depending on the subsequent processing a *histogram*, *Autoregressive (AR) spectrum* or *Poincare plot* can be generated.

When attention is focused on HR rhythmic fluctuations, AR methods are suitable because of their ability to identify the central frequency of the oscillation in an analytic way. The AR approach is especially appropriate when the available number of samples for the analysis is relatively low, as the frequency resolution of the AR-derived spectrum is not as dependent as the FFT method on the length of the recording.

The Poincare plot analysis is a nonlinear geometrical method to assess the dynamics of HRV. In this diagram each R-R interval is plotted as a function of the previous R-

R interval. Poincare plots have been evaluated in a qualitative way using their visual pattern whereby the shape of the plot is categorized into functional classes that indicate the degree of heart failure. The plots can also be evaluated quantitatively based on the computation of the SD indexes of the plot [11].

Such output data are shown in Fig. 6, 7 and 8 after processing the ECG recording of a real patient with duration of 740 seconds.

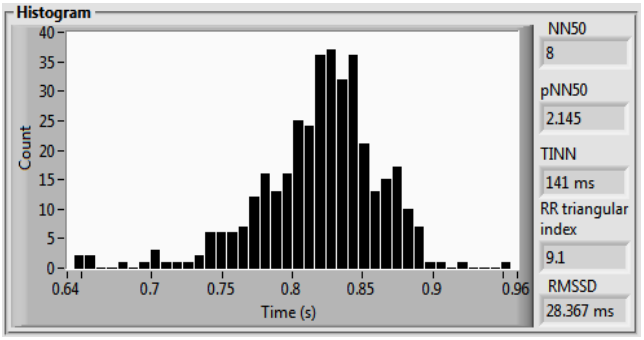

Fig. 6. Histogram with ECG signal parameters.

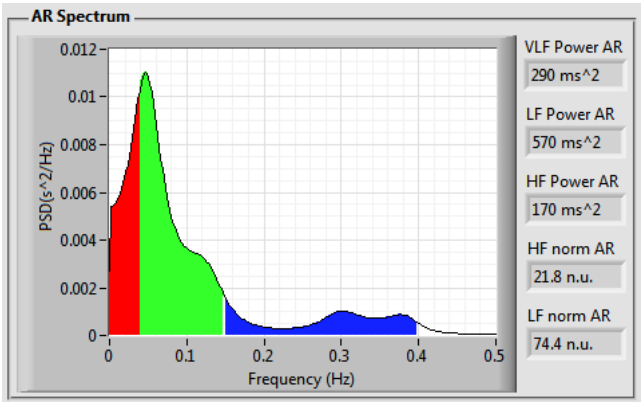

Fig. 7. AR Spectrum.

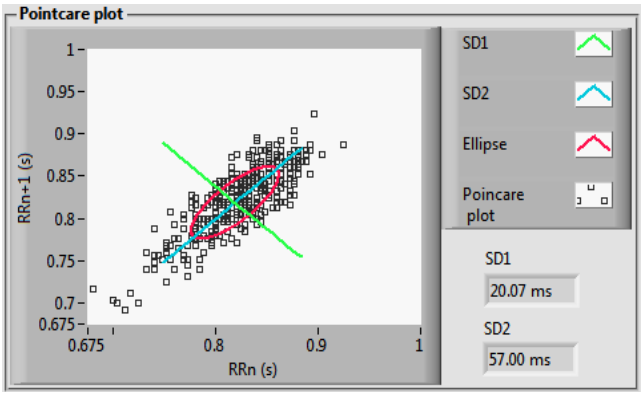

Fig. 8. RR Poincare plot.

VI. Conclusion

The approach for ECG signal acquisition and data analysis presented in this paper shows that a computer based data acquisition system together with the LabVIEW graphical programming environment can be an efficient alternative to the conventional stand-alone systems currently in use. The LabVIEW assisted Time-Domain Analysis of heart rate variability was shown to be successfully implemented using analogue front end AD8232. The results of ECG heart rate variability analysis are comparable to those of a standard clinical ECG device. This is an encouraging study for further development of portable heart rate monitors for home-healthcare and Holter-devices.

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Brain-computer Interface as Internet of Things Device

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Abstract – **Electroencephalography nowadays is used for diagnosing and monitoring patients, suffering from variety of mental disorders, deceases and other conditions. This challenges technology to provide fast connection with minimum data losses. This paper examines the required network parameters for ensuring all measured brain waves to arrive to the doctors' computer in real-time.**

Keywords – **Emotiv EPOC, IoT**

I. Introduction

A continuous monitoring of vital signs of patients can be lifesaving in various number of cases. With the advantage of devices representing Internet-of-Things (IoT), such monitoring can be done remotely. This allows the creation of computational infrastructures, like cloud computing, which simultaneously collect information from a large number of patients (from hospitals, cities, countries or globally) to conduct data analysis and to enable faster diagnosis of diseases in the presence of correlated indicators of different patients.

Gathering information from different types of sensors and rapidly changing measurement values represent a challenge for throughputs of any network infrastructure, which will pass through this stream of data.

II. Background

A representative of that type complex electronic sensor is encephalograph (EEG) - it allows simultaneous collection of data from multiple electrodes that are attached to certain places on the patient's head. Each of the electrodes measured bioelectric activity of the brain of these places. Small fluctuations in the signals are known as alpha, beta, theta, gamma and delta waves. In Figure 1 are shown time diagrams of these five types of brain activity. They are responsible for the relevant waves: gamma – active thinking, beta – work and alert, alpha – peace and relaxation, delta – dreaming and theta – meditation.

Monitoring these parameters assists in the diagnosis of epilepsy, brain tumors, stroke, head trauma, inflammatory, cerebrovascular trauma, memory disturbances, prolonged headache, migraine and etc.

Mainly, this type of monitoring is performed in the direct presence of the doctor. The system design and development of such complete system ready for use is complex task

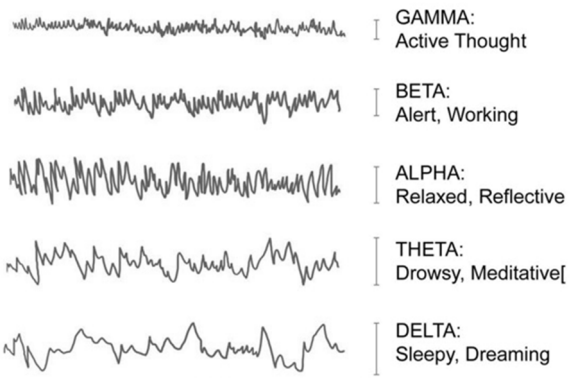

Figure 1: Example of brain waves

which is a subject of many researches and prototypes. The aim of this article is to create embedded system based on existing complete EEG preprocessor, existing universal Linux-based embedded board connected via custom RF USB receiver. The output data from EEG preprocessor is sending to PC using standard Wi-Fi network protocols.

A. Emotiv EPOC EEG Preprocessor

Figure 2: Emotiv EPOC

Emotiv EPOC (shown in Figure 2) is brain-computer interface, providing high resolution and full spatial resolution [1]. It is a 14 channel wireless EEG, designed for contextualized research and advanced brain computer interface (BCI) applications. There are two ways for reading data from the device:

- Collecting the raw data of the bioelectrical signals, which in combination represent activation of concrete brain lobs and show presence or absence of a certain emotion;

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- Development kit, provided by Emotiv, which is a software package with the following tools: Expressiv Suite Panel Display, Sensitivity Adjustment Panel, Training Panel, Affectiv Suite Panel, Affectiv Panel Display, Affectiv Suite Detection Details, Cognitiv Suite, Cognitiv Panel Display.

Raw data is collected by the 14 electrodes attached to the patient head, which places are exact and shown in Figure.3.

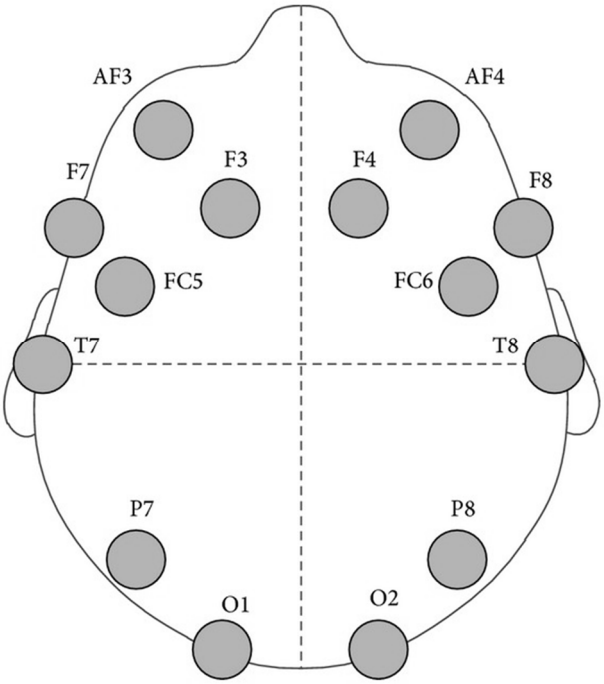

Figure 3: Electrodes' exact positions on the human head

These channels are represented by integer variables, which could be read by a computer program. They have values at around 4000 points (one point represents one microvolt of DC level of each sensor). Regarding the channels there are three values that also can be read in raw condition:

- Timestamp – date and time of the computer running the system. It could be used to synchronize the data with other inputs.
- GyroX – information about what is the momentum acceleration in the X axis of the head. When the head is still this value is close to zero.
- GyroY – information about what is the momentum acceleration in the Y axis of the head.

The GyroX and GyroY values indicate the position of the head and the doctor can determine if the patient is shaking uncontrollably his head.

The connectivity to this preprocessor is wireless RF communication using custom USB dongle for the computer side receiver. The range is limited up to 2 meters which is insufficient when it has to be used for continuous period of time.

B. Linux Embedded System as IoT device

To extend connectivity and capabilities for collecting and analyzing data, the preprocessor needs to be connected to a computer system with an operating system which is supporting development for Emotiv Epoc. Such operating systems are:

- Microsoft Windows - allowing support of Emotiv SDK [2]
- Apple OSX - allowing support of Emotiv Community SDK [3]
- Linux based system - working with EmoKit SDK [4]

From above presented, the development environment for Linux allows to be read in real-time raw data, and finished code can be deployed to an embedded system dedicated to collecting and sending information to a remote peer.

III. EXPERIMENTAL SET

The experimental set is divided into two sets – hardware and software set. The first describes the devices and the connectivity between them, the second describes the software architecture of the system.

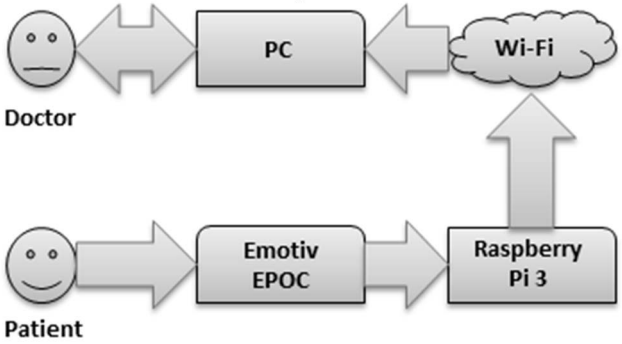

Figure 4: Experimental set diagram

A. Hardware and connectivity

The system is divided into two parts. The first part is the patient device - an embedded system for collecting data from the preprocessor and sending it to doctor's device.

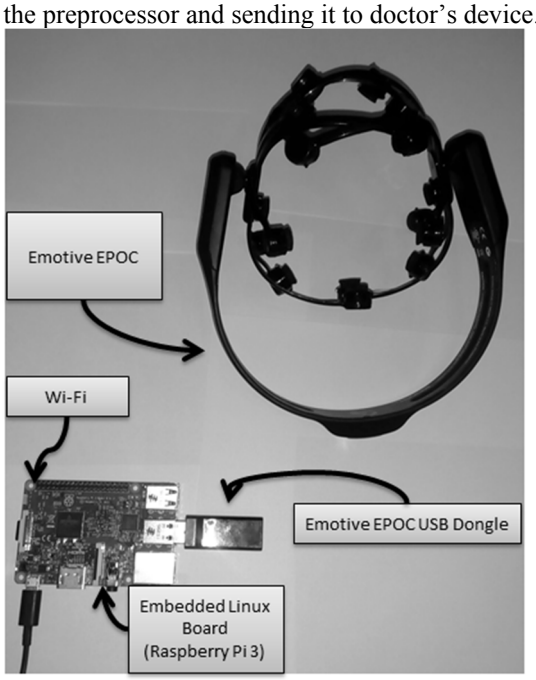

Figure 5: Components of the experimental set

The experimental board for patient's device is Raspberry Pi 3 [5] with 64bit ARM v8 MPU, 1GB RAM and embedded IEEE802.11n Wireless LAN. It provides a computational power and USB support to connect to the headset. The board is using Debian Linux as Operating system.

The second side for this experimental set, the doctor's side, is a personal computer with Microsoft Windows operating system. It can be changed to different mobile devices like tablet or mobile phone.

B. Software architecture

Debian Linux side

The software running on the Linux device is daemon process broadcasting the data using UDP datagrams every time when a reading from Emotiv Epoc occurs. The format of the data is "comma-separated values" (CSV). The content of the datagram contains the value of every electrode (AF3, AF4, F3, F4, F7, F8, FC5, FC6, T7, T8, P7, P8, O1, O2) and the values of the gyroscope (GyroX, GyroY).

Desktop side

The software of the doctor's personal computer is designed with three layer software architecture Model-View-ViewModel (MVVM) and it is a Windows Presentation Foundation (WPF) application.

The MVVM separates the Model structure (class describing a single measurement), the business logic of the program and the user interface (UI). WPF is the necessary tool for binding the data collection of the received datagrams and visual graphic controls on the user's main window of the application.

C. Experiments

To measure the refresh rate that can be got from the desktop side, there are experiments that should be conducted:

- Experiment 1: It is going to check if it is possible to get the data and convert it successfully to a collection of measurements. For this purpose the send data should be shown as a list of objects.
- Experiment 2: This experiment is going to determine the min/average/max time between two generated datagrams. The time is going to be measured in milliseconds when sending and receiving.
- Experiment 3: the experiment has to determine what is the throughput of the sending device in bits per second and to compare it to a regular throughput of a wireless infrastructure with packages with fixed length of 100 bytes.

IV. RESULTS AND DISCUSSION

A. Experiment 1

Figure 6 shows screenshots of the current data which is sending to the desktop side and the receiving part is shown in Figure 7. It can be seen that the parsing of the datagrams is successful and the data can be used for further analysis.

B. Experiment 2

In Figure 8 are shown screenshots of the time between the sending of two datagrams from the Linux side. The current data, which was sent to the desktop side, is received with time, shown in Figure 9. The results show that the average time between sending and receiving the data is between 7.22 and 7.40 ms for more than 9000 sent packages. The greater data in the receiving part is due to some package lost.

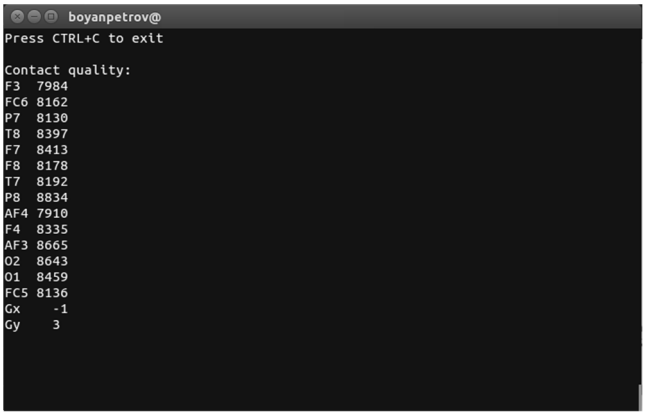

Figure 6: Collected raw data

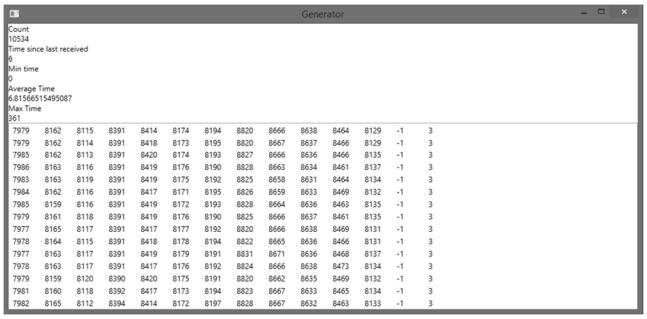

Figure 7: Received raw data

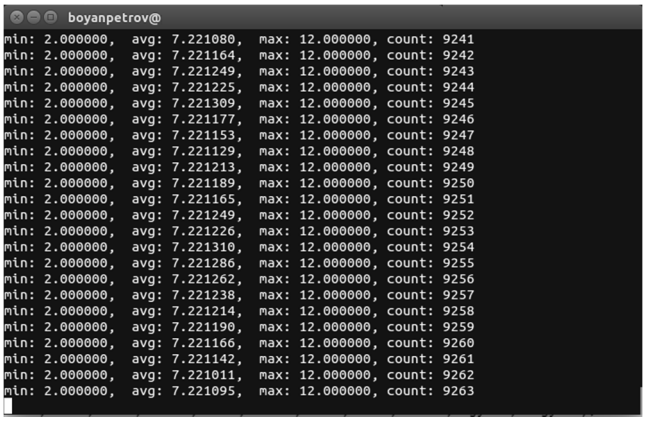

Figure 8: Time between the sending of two diagrams

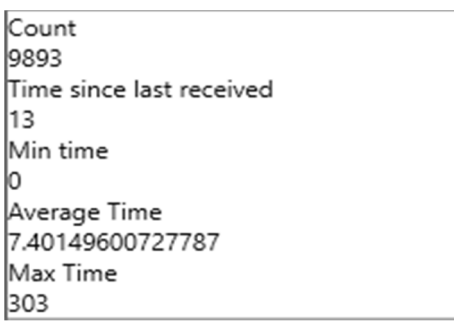

Figure 9: Time between receiving two diagrams

C. *Experiment 3*

The throughput of the network which is needed form the system to stream data is calculated by dividing the amount of bytes per each datagram by the average time between the packages.

Throughput = 100Bytes/7.4 ms = 13 513 Bytes/sec = 108108 bits/sec. (108,1 Kbps)

So the average wireless network with 54Mbits throughput can handle the streaming of more than one patient's device.

V. CONCLUSION

The result speed of the payload data is not high and the described data path can be realized as embedded device accessible, according to Internet-of-Things methods without using any PC with operating system.

Because of the speed of the data it is possible to be used different wireless media for data transmission like ZigBee or 2G/3G mobile network.

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Spatio-temporal EEG Signal Descriptors for Recognition of Negative Emotional States

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Abstract: **In the following paper we present a study on novel signal descriptors for the purposes of automated recognition of negative emotional states from EEG signals – namely, the decorrelated values of the energy of the spatio-temporal distribution of EEG activity. Using the extracted features person-specific SVM models are created. The experimental setups are based on data taken from the DEAP database. The classification accuracy of the proposed features is evaluated using two experimental setups: valence detection and like/dislike detection. Recognition accuracy of 77.5% and 78.0%, respectfully, was achieved.**

Keywords – **EEG, Negative emotion detection, spatial features**

I. INTRODUCTION

Emotions play a key role in human reasoning and behavior, and are among the basic drivers for social interaction. This explains the significant research interest in automated detection of human emotions and affective states. In order to achieve this goal various approaches have been developed – analysis of facial features from videos, classification of voice recordings, use of combinations of physiological signals and modalities, etc [1].

Overall, a relatively small number of studies focus on the detection of emotions and affective states solely from EEG signals. This is mainly due to the lack of a well-defined and universally accepted neural emotional model [1]. Furthermore, the task is additionally complicated by the high dimensionality of the EEG signal, the multitude of information, superimposed in one signal, the high noise to signal ratio and the relative complexity of the signal acquisition process.

The most challenging problem in any task involving classification from EEG signals is the aforementioned superimposition of information. The EEG signal is a measurement of the overall activity of the brain and the information regarding different specific processes and occurrences needs to be identified and extracted. This fact easily highlights the importance of studying, creating and evaluating features for EEG signals.

A number of different approaches for the estimation of EEG signal descriptors exist. The two most widely used methods include statistical features of the EEG, extracted in the time domain [2-4] and extracting and using specific frequency bands in the frequency domain of the EEG signal [5,6]. Another widely used approach is to combine additional features extracted from different physiological signals (ECG, skin resistance and others) and combine them with the EEG features [5].

Other, more specific approaches to the problem also exist. They involve the use of feature extraction techniques, traditionally employed in other fields. In [7] Othman et. al propose an automated system for recognition of four emotional states from EEG signals based on the Mel Frequency Cepstral coefficients (MFCC). They report that the proposed technique can be used to recognize emotions from EEG signals with accuracy up to 90% and conclude that the MFCC-MLP approach shows potential for detection of basic emotions.

Another example of a more specific type of features is given by Huang et. al [8]. Their approach is focused on a binary classification of two types of brain activities, observed in the EEG signals. These activities are characterized by the activation and deactivation of different areas of the brains depending of the experienced emotion. The authors propose an algorithm, which maximizes the asymmetry in the activation levels between the two sources by utilizing pair of spatial filters, for the different areas. The performance of the feature is evaluated on two emotion detection problems: arousal detection and valence detection, where it achieves an average of 82.46% and 66.05% classification accuracy.

In the present study we consider the use of features extracted from a spatio-temporal representation of the EEG signal. The reasoning behind this approach is rooted in the well-established paradigm that different emotions manifest in specific areas of the brain.

The rest of the paper is organized as follows. In Section II, we outline the applied preprocessing procedures and the extraction of the EEG descriptors. In Section III, we describe the common experimental setup used in the evaluation study. In Section IV, we provide details on the estimation of person-specific thresholds for the recognizer of negative emotional states. The experimental results are reported in Section V and in Section VI, we offer a summary and concluding remarks.

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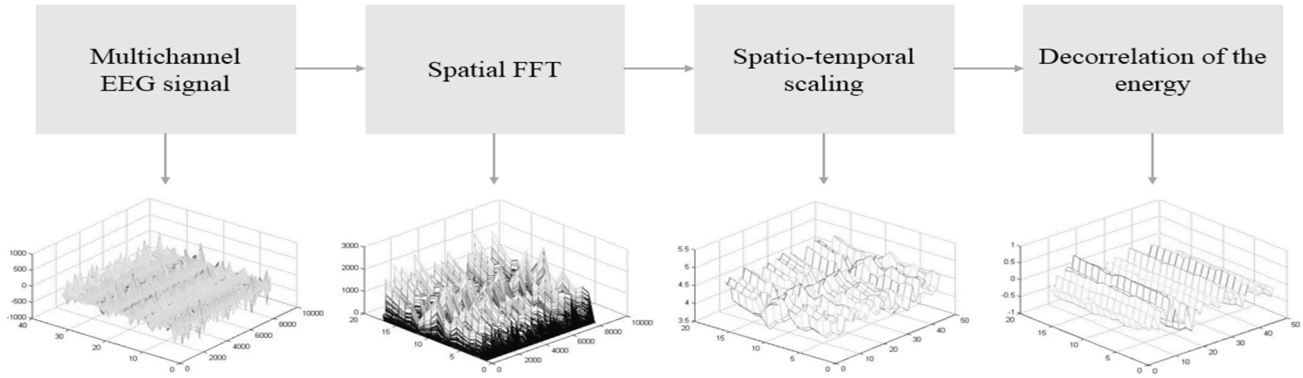

Figure 1: Block diagram of the different extraction steps of the spatio-temporal features.

II. FEATURE EXTRACTION

The goal of the conducted research is to study the qualities of descriptors of negative emotional states, calculated from spatio-temporal representations of EEG signals. The performance of the studied descriptor is evaluated on a binary classification task. In particular the features that we focus on are the decorrelated values of the energy of the spatio-temporal distribution of EEG activity. The features are extracted from a scaled spatio-temporal representation of the EEG signal, created by combining spatial Fast Fourier Transform (FFT) and triangular window functions.

The processing steps, used to extract the features from the EEG signal are given in Figure 1.

The first step of the feature extraction process is the conversion of the standard EEG data into a spatio-temporal representation of the signal. This is done through the application of Fast Fourier Transform (FFT) on the spatial dimension of the EEG recording. More specifically the FFT is performed on the data, recorded simultaneously by the EEG electrodes in one sampling period. In this way we obtain a spatial representation of the brain activity for a given moment. Due to the nature of the FFT, part of the obtained spatial activity spectrum contains mirrored elements which are removed. In the presented case this leads to a reduction of the spatial resolution, as we are left with 16 points of spatial data, down from 32.

The second step of the feature extraction process is the scaling of the obtained spectrogram. This is done through the use of a set of triangular window functions with 50% overlap between subsequent windows, which are applied to the signal. All window function cover an equal number of data samples. The windows are defined as:

$$H_i(k) = \begin{cases} 0 & \text{for } k < n_{b_{i-1}} \\ \dfrac{(k - n_{b_{i-1}})}{(n_{b_i} - n_{b_{i-1}})} & \text{for } n_{b_{i-1}} \le k \le n_{b_i} \\ \dfrac{(n_{b_{i+1}} - k)}{(n_{b_{i+1}} - n_{b_i})} & \text{for } n_{b_i} \le k \le n_{b_{i+1}} \\ 0 & \text{for } k > n_{b_{i+1}} \end{cases} \quad (1)$$

where, the index i stands for the i-th window function, n_{bi} are the boundary points of the windows, expressed in samples, and k = 1,2,… N corresponds to the k-th coefficient of the N-point. We use the outputs, generated by the window functions to calculate the logarithmic energy of the spatial activity for the selected time periods of the EEG signal.

$$S_i = \log_{10}\left(\sum_{k=0}^{N-1} |\mathrm{S}(k)|^2 .H_i(k)\right),\ i = 1,2,...,M \quad (2)$$

where S_i is the output of the i-th filter, $|S(k)|^2$ is the power spectrum, and N is the total number of samples. By taking the calculated spatio-temporal energy for all windows we generate a temporally scaled representation of the spectrogram (Fig.1). The temporal distance between the calculated spatial energy values is constant. The number of used windows determines the temporal resolution of the scaled representation of the EEG signal.

As a final step we apply discrete cosine transform (3) to the obtained scaled representation of the signal. In this way we decorrelate the energy, calculated for the different temporal windows and we obtain the Decorrelated Spatio-Temporal Coefficients (DSTC):

$$DSTC(r) = \sum_{i=1}^{M} S_i \cos\left(\frac{r(i-0.5)\pi}{B}\right), r = 0,1,...R-1 \quad (3)$$

where r is the DSTC index, and R ≤ M is the total number of unique DSTC that can be computed. The number of unique coefficients depends on the number of used window functions.

Statistical standardization of the calculated descriptors is performed, so that their distributions are normalized to zero mean value and unit standard deviation:

$$Z = \frac{D_p - \mu_p}{\sigma_p} \quad (4)$$

where μ_p and σ_p are extracted from the training data of the participant, who's data is currently processed.

III. EXPERIMENTAL PROTOCOL

3.1 Dataset

The evaluation of the DSTC's descriptive performance is carried out following a common experimental protocol, based on the Database for Emotion Analysis using Physiological signals (DEAP) [9]. The DEAP database consists of recordings from thirty-two participants with a total of 40 recordings per participant. Each recording, made while the participants were watching musical video-clips, consists of 40 channels. These include 32 channel EEG, electrocardiographic (ECG), electromyographic (EMG) and other physiological signals, all taken from different parts of the head and the body. The dataset includes pre-processed recordings from these forty channels. Frontal face videos and detailed metadata for the participants are also included in the database. All EEG recordings were self-annotated by the subjects participating in the data collection.

The EEG recordings of 10 participants were taken for our experiments, based on the provided annotations. We aimed at balance between the numbers of songs tagged as negative and positive for each participant. Each participant's data was split into two sets. The first set contained data, separated on the base of the given like-dislike ratings. The second set was created based on the given valence ratings. Both sets were further split in three parts – training, development, and testing dataset, which consist of 20%, 20%, and 60% of the available recordings. However, depending on the distribution of song ratings for each participant, these percentages varied up to 5%.

For both sets the split of recordings into these three subsets was performed in the following way: The datasets of each participant were split into two groups – *negative* and *non-negative* – depending on the like/dislike rating of the recording for the first set and the valence ratings for the second. Each rating provided in the database indicates the personal preferences of the participant. Both the like/dislike ratings and the valance ratings range from 1 to 9, where 1 corresponds to the lowest rating (*disliked/low valence*) and 9 is the highest rating – *liked/high valence*. For the data separation based on the given *like/dislike* ratings, recordings which had rating of 4 or lower were tagged as *negative*, while recordings with ratings higher than 4 were tagged as *non-negative*. In few cases when the number of definitely tagged recordings was not sufficient a 5% tolerance was applied to the separation threshold. For the creation of the second group of data sets, separated based on the valence ratings, recordings with valence rating lower than 4.5 were tagged as *negative*, while recordings with rating higher than 4.5 were tagged as *positive*. In both cases, all EEG recordings for the selected participants were used during the experiments, which totals to 400 EEG recordings.

3.2 Detector

The comparative evaluation of EEG signal descriptors was conducted through the use of a detector of negative emotional states [1], which is based on the following principle:

The training data set, composed of the most indicative examples of negative and non-negative recordings, was used to train a person-specific SVM classifier with radial basis function kernel. In order to find out the optimal training parameters for every emotion classifier, a series of grid searches were implemented on the development dataset. Grid searches for the adjustable parameters of the SVM were carried out for each of the individual descriptors, for each participant. The optimal values found during the grid search were used for the evaluation of each detector.

The model, generated this way, was then tuned on the development dataset, so that a person-specific decision threshold *Tr* can be computed:

$$Tr = \frac{\frac{1}{n}\sum_{f=1}^{n} D_{neg,f} + \frac{1}{m}\sum_{l=1}^{m} D_{pos,l}}{2}, \qquad (5)$$

where D_{neg} and D_{pos} are the portions of development data consisting of n recordings with negative tags and m with non-negative tags (neutral or positive).

During the evaluation of each classifier, the threshold (5) was used for making a decision for each recoding. The person-specific recognition accuracy of the descriptors is evaluated in terms of percentage correct detections:

$$correct = \frac{H}{N_{rec}} \times 100, [\%] \qquad (6)$$

IV. RESULTS

Based on the experimental protocol described in Section III we carried out an evaluation of the proposed EEG signal descriptors, extracted using different number of window functions. Specifically, the descriptive qualities of the spatio-temporal DSTC were evaluated in two different experiments. In the first one, the EEG dataset was split based on the *like/dislike* ratings, provided in the metadata by the participants. In the second one, the data split was performed in accordance with the *valance* ratings for each recording. In both cases, the experiments were carried out 8 times using different number of window functions: 8, 16, 24, 32, 48, 64, 128 and 256.

The corresponding experimental results are provided in Tables 1 and 2, respectively. In both tables, we report the individual detection accuracy achieved for each participant's dataset and the average recognition accuracy.

In Table 1, we present results for the like/dislike ratings based separation. The experimental results show that the recognition accuracy for the individual participants varied from 72.2% to 77.5%. The lowest accuracy (72.2%) was obtained with a filter bank of 16 filters, and the highest with 256 filters. Based on the results presented in Table 1, we can conclude that increasing the number of filters affects the classification accuracy for each participant differently. This does not allow conclusive determination of the most appropriate number of filters.

In Table 2, we present results for the valance ratings based separation of EEG recordings. Here the individual recognition accuracy varied in the range between 70.8% and 78.0%. The lowest recognition accuracy (70.8%) was obtained with 16 filters, while the highest (78.0%) with 48 filters. For a larger number of filters the mean classification accuracy is slightly lower and remains practically the same.

Table 1: *Accuracy achieved using data separation based on the reported like\dislike ratings*

№ of filters:	*P№ 02*	*P№11*	*P№17*	*P№21*	*P№22*	*P№24*	*P№28*	*P№29*	*P№30*	*P№32*	*Mean Acc.*
8 filters	75.0%	81.8%	77.3%	86.9%	77.3%	72.7%	83.3%	60.9%	69.6%	81.8%	76.7 ± 7.6%
16 filters	66.7%	72.7%	63.6%	78.3%	77.3%	77.3%	75.0%	73.9%	69.6%	68.2%	72.2 ± 5.0%
24 filters	75.0%	77.3%	77.3%	69.6%	72.7%	72.7%	79.2%	78.3%	73.9%	72.7%	74.9 ± 3.1%
32 filters	87.5%	81.8%	81.8%	73.9%	63.6%	72.7%	66.7%	91.3%	69.6%	72.7%	76.2 ± 9.1%
48 filters	87.5%	77.3%	81.8%	82.6%	72.7%	75.0%	78.3%	78.3%	78.3%	68.2%	77.0 ± 5.4%
64 filters	75.0%	81.8%	77.3%	69.6%	63.6%	68.2%	91.7%	78.3%	82.6%	81.8%	77.0 ± 8.2%
128 filters	83.3%	72.7%	72.7%	73.9%	63.6%	72.7%	75.0%	78.3%	82.6%	68.2%	74.3 ± 6.0%
256 filters	75.0%	77.3%	81.8$	78.3%	81.8%	63.6%	79.2%	78.3%	78.3%	81.8%	77.5 ± 5.4%

Table 2: *Accuracy achieved using data separation based on the reported valance ratings.*

№ of filters:	*P№ 02*	*P№11*	*P№17*	*P№21*	*P№22*	*P№24*	*P№28*	*P№29*	*P№30*	*P№32*	*Mean Acc.*
8 filters	79.2%	75.0%	75.0%	65.2%	72.0%	58.3%	66.7%	70.8%	79.2%	75.0%	71.6 ± 6.6%
16 filters	66.7%	66.7%	62.5%	69.6%	72.0%	75.0%	70.8%	75.0%	79.2%	70.8%	70.8 ± 4.8%
24 filters	75.0%	66.7%	66.7%	65.2%	72.0%	79.2%	70.8%	83.3%	87.5%	70.8%	73.7 ± 7.5%
32 filters	70.8%	70.8%	79.2%	73.9%	76.0%	66.7%	75.0%	79.2%	83.3%	79.2%	75.4 ± 5.0%
48 filters	75.0%	87.5%	75.0%	82.6%	72.0%	70.8%	70.8%	83.3%	83.3%	79.2%	78.0 ± 6.0%
64 filters	79.2%	83.3%	83.3%	73.9%	72.0%	66.7%	70.8%	75.0%	83.3%	75.0%	76.2 ± 5.8%
128 filters	79.2%	79.2%	75.0%	69.6%	84.0%	70.8%	70.8%	83.3%	79.2%	83.3%	77.4 ± 5.5%
256 filters	87.5%	87.5%	70.8%	78.3%	80.0%	79.2%	70.8%	75.0%	70.8%	75.0%	77.5 ± 6.3%

In addition, from the provided standard deviation values it can be seen that in most cases the results achieved for different participant using one feature vary significantly. This result is consistent with the widely accepted notion that EEG recordings are highly specific for every different individual

V. Conclusion

In the following work we presented a study on the qualities of the decorrelated values of the energy of the spatio-temporal distribution of EEG activity, computed from spatio-temporal representations of EEG signals, as a descriptor for the purposes of classification of negative emotional states.

The experimental results confirm that DSTC extracted from a spatio-temporal representation of the EEG signals can be used as descriptors for classification of negative emotional states. The classification accuracy achieved using DSTC is similar to other widely used features for emotion detection.

Compared to other methods DSTC have a series of advantages. The fact that they are calculated from the entire EEG recording results in small feature vectors which leads to significant reduction in computational time, due to faster feature extraction and model creation. Additionally, the number of applied window functions directly affects the time required for classification. It is important to point out that high classification accuracies can be achieved with a relatively low number of filters.

Furthermore, the extraction of DSTC features is accompanied by a number of different parameters that can be changed or modified. This allows for the creation of finely tuned, person specific models with very high classification accuracy.

Future research will be focused on the further study of the possibilities for spatio-temporal representation of EEG signals. The focus will be on the design of features based on the differences in spatial EEG activity, the descriptive qualities of EEG activity in different areas of the brain and their relation to human affective states.

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Comparative Evaluation of Probability Density Estimators for the Probabilistic Neural Network

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Abstract – **Hardware implementation of machine learning methods is often considered challenging, however, it brings major benefits, such as speed of operation and energy efficiency. Having in mind these benefits, we evaluate the performance and complexity of four probability density estimators (PDE) that we consider interesting for hardware implementation of the probabilistic neural network (PNN). We report results of a comparative evaluation of these PDEs for three different sizes of the PNN, evaluated in a common experimental protocol that makes use of the SPECT dataset. We conclude that two of the estimators are more appropriate for hardware implementation in FPGA.**

Keywords – **probabilistic neural network, probability density function**

I. Introduction

Neural networks undoubtedly improve the automatization and reduce the time needed for repetitive tasks in various fields. In the medical field, such tasks span from analyzing biomedical samples, biomedical signals, etc., to the analysis of different types of medical imagery. These algorithms do not aim to substitute a trained medical doctor but to provide tools in support of diagnostics of diseases.

The mathematical methods behind the structures of artificial neural networks however, are usually computationally expensive and require substantial amount of time and resources to either train a model or compute the output for unlabeled input.

One way to reduce these demands is by making use of Field Programmable Gate Arrays (FPGAs) and implementing a machine-learning algorithm partially or entirely as hardware. Although, this solves issues related to energy consumption and computational speed other problems such as limitation of the size and complexity of the machine learning algorithm become prominent due to the physical constrains of the FPGA chip itself [1,2,3].

In the current study we investigate opportunities for a suitable balance between the aforementioned issues. More specifically, we tackle these problems on a set of binary SPECT images [4]. Diverse studies on the same dataset reported recognition accuracy in the range between 71.70 ± 6.56% to 84%, throughout different approaches [5,6]. However, the training of the algorithms in the abovementioned studies could be referred as rather computationally expensive.

In our case, we make use of the robust statistical classification method employed in the probabilistic neural network (PNN) that deals well with outliers and offers a good discriminative power as soon as a few representative training samples are available for each class. Moreover, the training is very straightforward and the original PNN introduced by Specht has one adjustable parameter, making the PNN suitable for hardware implementation [7,8,9].

However, the commonly used probability density function (PDF) of the PNN can be expensive and complicated to implement in hardware due to its exponential nature. One regularly used way to deal with such situations is implementing the exponential part fully or partially as a LookUp Table (LUT) [1,10]. Nevertheless, choosing the appropriate size and resolution can be a challenge by itself [11,12]. A different approach to the problem is the possibility of using another PDF [7,13] and more precisely such that is less expensive in terms of hardware. Here we investigate the latter option by comparing the performance of four different probability density functions implemented as software in order to choose the most appropriate one for hardware implementation.

The remaining of the paper is organized as follows. In Section II we briefly outline the PNN and the considered probability density functions; in Section III we describe the experimental protocol used in the comparative evaluation; in Section IV a discussion on the experimental results is presented. Finally, in Section V we conclude this study.

II. Probabilistic Neural Network

The structure of the PNN generally consists of four layers with the input layer included. The second and third layers are responsible for the estimation of the probability density function (PDF) for each class. Most often, the PDF is estimated by employing a sum of spherical Gaussian functions that are centered at each training vector:

$$p_i(\mathbf{x} \mid k_i) = \frac{1}{(2\pi)^{d/2}\sigma_i^{\,d}} \cdot \frac{1}{M_i} \cdot \sum_{j=1}^{M_i} \exp\left(-\frac{1}{2\sigma_i^{\,2}} (\mathbf{x}-\mathbf{x}_{ij})^T (\mathbf{x}-\mathbf{x}_{ij}) \right) \quad (1)$$

with $i = 1,2,\ldots,K$ and $j = 1,2,\ldots,M$, σ is the standard deviation, and is also known as spread or smoothing factor, which regulates the receptive field of the kernel. The smoothing factor can be either homoscedastic or heteroscedastic. Here we consider the homoscedastic version, where σ has a common value for all classes.

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Finally, the classification decision of the PNN is made in accordance with the Bayes' strategy for decision rules:

$$D(\mathbf{x}) = \arg\max_i \left\{ P(k_i)\, p_i(\mathbf{x} \mid k_i) \right\},\ i = 1, ..., K \tag{2}$$

where $P(k_i)$ is the *a priori* probability for class k_i. Besides the decision, the PNN also provides a probability and reliability measure of each classification.

Apart from the above described standard Parzen-Cacoullos model, multiple other alternatives exist regarding the estimation of the probability density function for a certain decision class [7]. Here we have chosen three of these alternative estimators:

$$f(\mathbf{x}) = \frac{1}{m(2\lambda)^p} \cdot \sum_{j=1}^{m} 1,\ \textit{when all}\ \left| x_i - x_{ij} \right| \le \lambda,\ i = 1, 2, ..., p,\ j = 1, 2, ..., m; \tag{3}$$

$$f(\mathbf{x}) = \frac{1}{m\lambda^p} \cdot \sum_{j=1}^{m} \prod_{i=1}^{p} \left[1 - \frac{\left| x_i - x_{ij} \right|}{\lambda} \right],\ \textit{when all}\ \left| x_i - x_{ij} \right| \le \lambda,\ i = 1, 2, ..., p,\ j = 1, 2, ..., m; \tag{4}$$

$$f(\mathbf{x}) = \frac{1}{m(\pi\lambda)^p} \cdot \sum_{j=1}^{m} \prod_{i=1}^{p} \left[1 + \frac{\left(x_i - x_{ij} \right)^2}{\lambda^2} \right]^{-1} \tag{5}$$

The selected estimators can be regarded as hardware friendly due to the fact that they are limited to operations such as multiplication, division, and subtraction and adding. In the rest of this paper the different implementations of the PNN with equations (1), (3), (4) or (5) will be referred to as F-1, F-2, F-3 and F-4, respectively.

III. Experimental setup

In order to evaluate the performance of the four probability density functions of the PNN we have considered the publically available dataset of binary images, known as the cardiac Single Proton Emission Computed Tomography (SPECT) dataset [4]. The dataset contains 267 image sets processed to extract summarizing features of the original SPECT images. Each of the 267 images is tagged in two categories: normal or abnormal. Each of the images was further processed resulting in 22 binary feature patterns.

Three cases with different number of neurons of the PNN were investigated for each of the PDF estimators. The default experimental protocol with 80 training vectors was considered as well as cases with subsets of 50 and 20 training vectors. The lower number of training vectors reduces the hardware design as FPGA chip size influences the price and the overall energy consumption.

The lesser number of training vectors was obtained after a uniform random sampling of the 80 training vectors. We started with the default 80 training vectors specified in the SPECT dataset, and randomly selected 50 vectors. This was repeated ten times and the experimental results were averaged. The same protocol was used for the case with 20 training vectors.

IV. Results

The experiments were performed for 100 different values of sigma and lambda, ranging from 0.1 to 10 and changing with a step of 0.1. Furthermore, for each test the value of sigma corresponds to the value of lambda. Summarized results are presented in Figs. 1, 2 and 3 for the cases of 80, 50, and 20 training vectors, respectively. The horizontal axis shows the sigma/lambda values from 0.1 to 10 with a step of 0.1. The vertical axis shows the accuracy in percentages and in the case of Fig. 2 and Fig. 3 the average accuracy in percentages.

In Fig. 1 we present the classification accuracy for the default split of the SPECT dataset with 80 training vectors. As the figure shows, the experimental results for implementations F-3 and F-4 are similar to the commonly used F-1. This behavior is also true for the cases shown on Fig. 2 and Fig. 3.

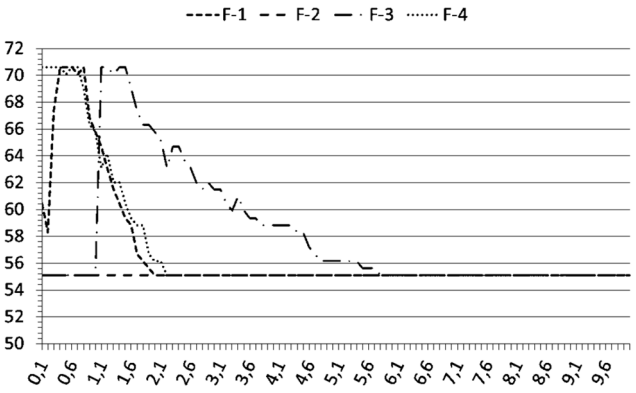

Fig. 1. PNNs with 80 neurons in the pattern layer

In Fig. 2 and Fig. 3 we observe an expected decline in the overall accuracy when the number of training vectors is decreased for the different PDF estimators of the PNN. The decline in accuracy for 50 training vectors compared to 80 training vectors is around four percent for the best achieved results. While the accuracy for the best achieved results in the case of 20 training vectors compared to 50 training vectors declines in the range of five percent.

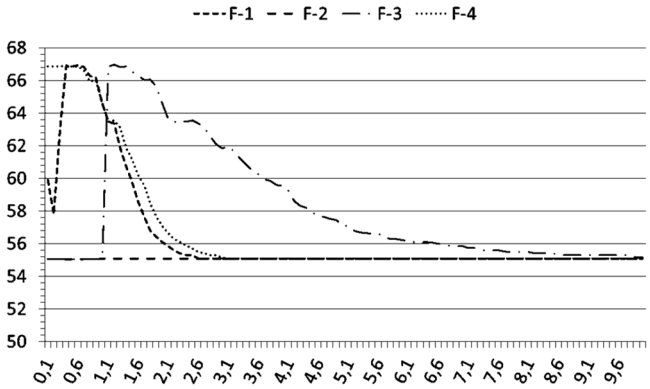

Fig. 2. PNNs with 50 neurons in the pattern layer

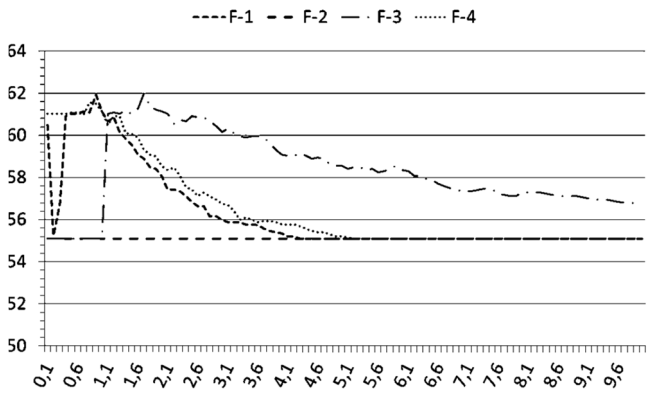

Fig. 3. PNNs with 20 neurons in the pattern layer

In Fig. 1, Fig. 2, and Fig. 3 we see that the region of interest in all cases can be pin pointed to the values of sigma and lambda in the range between 0.1 and 2. There we observe dynamic changes in the overall accuracy as well as the highest achieved accuracies for the different setups. While for values of lambda and sigma in the region beyond 2 the accuracy steadily declines.

In Tables 1, 2 and 3 we summarize the dynamics of the classification accuracy due to changes of the training parameters sigma and lambda for the range of values between 0.1 and 2. In each of these cases, we considered the four PNN implementations – F-1, F-2, F-3 and F-4.

Specifically, in Table 1 we present the experimental results with 80 training vectors. In the case of F-1, the best accuracy is 70.59% for several values of sigma. The same accuracy of 70.59% was observed for F-3 and F-4 as well for several values of lambda.

TABLE 1. PERCENTAGE ACCURACY FOR THE PNNS WITH 80 TRAINING VECTORS

σ/λ	F-1	F-2	F-3	F-4
0,1	60,43	55,08	55,08	70,59
0,2	58,29	55,08	55,08	70,59
0,3	67,38	55,08	55,08	70,59
0,4	70,59	55,08	55,08	70,59
0,5	70,59	55,08	55,08	70,05
0,6	70,59	55,08	55,08	70,59
0,7	70,05	55,08	55,08	70,59
0,8	70,59	55,08	55,08	68,98
0,9	66,84	55,08	55,08	66,31
1	65,78	55,08	55,08	65,78
1,1	64,71	55,08	70,59	63,10
1,2	63,10	55,08	70,59	64,17
1,3	61,50	55,08	70,05	62,03
1,4	60,43	55,08	70,59	62,03
1,5	59,36	55,08	70,59	60,43
1,6	58,82	55,08	68,98	59,36
1,7	56,68	55,08	67,38	58,82
1,8	56,15	55,08	66,31	58,82
1,9	55,61	55,08	66,31	56,68
2	55,08	55,08	65,78	56,15

However, the achieved results were not obtained for identical values of lambda and sigma in the four PNN implementations. Especially for F-3, higher accuracy is achieved for lambda bigger than 1, while for F-1 and F-4 this is true for values of sigma and lambda which are less than 1. Nonetheless, for F-1 and F-4 there is some overlapping of the values of the training parameters at which the best accuracies are observed. Here, F-2 did not perform well and the accuracy is only 55.08%. This result does not change for the different values of lambda.

For Table 2 and Table 3 we see the average accuracy as well as the standard deviation for the different setups. This is imperative due to the approach, by which the training data is obtained for these two cases of training vectors, described in Section III.

For 50 training vectors in Table 2 F-1 achieves accuracy of 66.90% ± 0.04% for σ = 0.6. The same accuracy of 66.90% ± 0.04% is reached for F-4 as well, but for λ = 0.4. For F-3 we have accuracy of 66.95% ± 0.04% for λ = 1.2. Again as in Table 1, F-2 fails to reach values higher than 55.08% in terms of accuracy.

TABLE 2. AVERAGE ± STANDARD DEVIATION OF PERCENTAGE ACCURACY FOR THE PNNS WITH 50 TRAINING VECTORS

σ/λ	F-1	F-2	F-3	F-4
0,1	59,89±0,02	55,03±0,00	55,03±0,00	66,84±0,04
0,2	57,81±0,02	55,03±0,00	55,03±0,00	66,84±0,04
0,3	63,16±0,04	55,03±0,00	55,03±0,00	66,84±0,04
0,4	66,84±0,04	55,03±0,00	55,03±0,00	66,90±0,04
0,5	66,84±0,04	55,03±0,00	55,03±0,00	66,84±0,04
0,6	66,90±0,04	55,03±0,00	55,03±0,00	66,84±0,03
0,7	66,79±0,03	55,03±0,00	55,03±0,00	66,58±0,03
0,8	66,26±0,03	55,03±0,00	55,03±0,00	65,94±0,03
0,9	66,15±0,03	55,03±0,00	55,03±0,00	65,99±0,03
1	64,55±0,03	55,08±0,00	55,03±0,00	64,60±0,03
1,1	63,48±0,03	55,08±0,00	66,84±0,04	63,48±0,02
1,2	63,37±0,03	55,08±0,00	66,95±0,04	63,53±0,03
1,3	61,87±0,03	55,08±0,00	66,79±0,03	63,10±0,03
1,4	60,75±0,03	55,08±0,00	66,84±0,03	61,87±0,03
1,5	59,79±0,02	55,08±0,00	66,52±0,03	61,18±0,03
1,6	58,61±0,02	55,08±0,00	66,31±0,03	60,21±0,03
1,7	57,59±0,02	55,08±0,00	65,99±0,03	59,52±0,02
1,8	56,79±0,01	55,08±0,00	66,04±0,03	58,45±0,02
1,9	56,42±0,01	55,08±0,00	65,61±0,03	57,65±0,02
2	56,10±0,01	55,08±0,00	64,60±0,03	57,06±0,01

In Table 3, where we have the lowest number of training vectors – 20, the lowest accuracy for most of the probability density functions are observed as well. Yet again F-2 has a constant accuracy of 55.08% through all of the different values of lambda. However, F-1, F-3 and F-4 experience some noticeable decline in accuracy, though remaining above 60% accuracy. More specifically, F-1 reaches 61.93% ± 0.04% accuracy for σ = 0.9. While F-3 manages to obtain accuracy of 61.98% ± 0.04% for λ = 1.7 and F-4 declines to accuracy of 61.55% ± 0.04% for λ = 0.8.

It is obvious that in the case of F-2 there is no change in the accuracy or it is changing in such small values that it can be overlooked as in the case of Table 2. This is a result from the type of data being processed by the PNN, which in our case is in binary form, and the internal works of F-2. If we look closer at Equation (3) (F-2) we see that there will always be summation from 1 to m when lambda reaches 1 and beyond. While for lambda less than 1 there can be cases where summation for all values from 1 to m will not occur. This comes from the fact that the result from $|x_i - x_{ij}|$ will always be zero or one. This can be clearly

observed in Table 2 where the accuracy for lambda from 0.1 to 0.9 is 55.03% and from lambda – 1 the accuracy changes to 55.08% and remains as such.

TABLE 3. AVERAGE ± STANDARD DEVIATION OF PERCENTAGE ACCURACY FOR THE PNNS WITH 20 TRAINING VECTORS

σ/λ	F-1	F-2	F-3	F-4
0,1	60,48±0,03	55,08±0,00	55,08±0,00	61,02±0,05
0,2	55,24±0,01	55,08±0,00	55,08±0,00	61,02±0,05
0,3	56,74±0,04	55,08±0,00	55,08±0,00	61,02±0,05
0,4	60,91±0,05	55,08±0,00	55,08±0,00	61,02±0,05
0,5	61,02±0,05	55,08±0,00	55,08±0,00	61,07±0,05
0,6	61,02±0,05	55,08±0,00	55,08±0,00	61,07±0,05
0,7	61,12±0,05	55,08±0,00	55,08±0,00	60,96±0,04
0,8	61,07±0,04	55,08±0,00	55,08±0,00	61,55±0,04
0,9	61,93±0,04	55,08±0,00	55,08±0,00	61,50±0,04
1	61,12±0,04	55,08±0,00	55,08±0,00	61,12±0,04
1,1	60,64±0,03	55,08±0,00	61,02±0,05	60,48±0,03
1,2	60,86±0,03	55,08±0,00	61,07±0,05	60,91±0,03
1,3	60,16±0,03	55,08±0,00	61,02±0,05	60,91±0,03
1,4	59,84±0,04	55,08±0,00	61,18±0,05	61,18±0,03
1,5	59,57±0,03	55,08±0,00	61,02±0,04	60,05±0,03
1,6	59,09±0,03	55,08±0,00	61,28±0,04	59,89±0,03
1,7	58,88±0,03	55,08±0,00	61,98±0,04	59,30±0,03
1,8	58,50±0,04	55,08±0,00	61,39±0,04	59,09±0,03
1,9	58,40±0,04	55,08±0,00	61,23±0,04	58,98±0,03
2	58,07±0,04	55,08±0,00	61,12±0,04	58,56±0,03

Fortunately, F-3 and F-4 behave much better compared to F-2 in the current task. The cases of F-3 and F-4 show similar results compared to the commonly used F-1. Although, not for the same values of sigma and lambda. In the cases of Table 2 and Table 3, F-3 even shows advantage in the accuracy over the other three probability density functions. However, if we look at the best results the difference between F-3 and F-1 and F-4 is in the hundreds or at most in the tenths after the decimal point for the three cases of training vectors.

V. CONCLUSION

The probabilistic neural network studied here did not reach accuracy of 84% reported in previous studies on the SPECT dataset. Specifically for the case with 80 training vectors PNN demonstrated an accuracy of 71% for three of the four tested probability density estimators. However, it must be kept in mind that although accuracy is an important part, the complexity or rather the simplicity of the used classification algorithm is the primary concern in the present study.

The trade-off between accuracy and complexity for the cases of F-3 and F-4 is perceived as satisfactory (on the current classification problem). Further studies regarding their implementation and performance in hardware will be carried out after implementation in a specific FPGA chip.

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Organochlorine Screening Using Food in Fresh an Electronic Nose

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Abstract – **In this work is carried out an investigation of the behavior of the volatile that emit the fruits contaminated in relation to those that are totally organic through an electronic nose, the aim is to achieve a qualitative classification into two classes, presence of pesticide and organic food, this which allows is to reduce the rates of diseases because of the excessive contamination of the food and create a new methodology through a low-cost electronic equipment that is a tool for small and medium-sized farmers.**

Keywords – **Multisensorial system, organochlorine, neural network**

I. Introduction

Food production in Colombia, both plants and animals, are affected by the indiscriminate use of chemicals. Since its introduction around 1950 pesticide use of organic origin has led to better quality and higher yields compared to when only inorganic origin pesticides were used; however, organic products are more difficult to eliminate foods that inorganic salts and therefore have created the potential waste of highly toxic pesticides to humans and the environment problem. High demand in the use of pesticides generates consequences that affect ecosystems generating imbalances; it affects not only farmers but also consumers; this is due to the residual generated in food [1]. This problem at the country level has hampered access to international markets, where standards are highly restrictive with respect to the presence of traces of organochlorides, organophosphates and carbamates in fresh or processed.

This has meant that necessary studies to detect the presence of these compounds in various foods, especially fruits, but because analytical methods are costly and delayed the industry requires alternative methods, indirectly, but in a short time can identify these compounds before the product reaches the consumer.

The use of pesticides coincides with the "era chemical" which has transformed society since the 1950s in areas where intensive monoculture is practiced, pesticides are the usual method of pest control. Colombian pesticide industry began in 1962 with the formulation of products, in 1964, the synthesis of some active ingredients such as Mancozeb and Cymoxanil fungicide began, herbicides diuron and propanil and disinfectant Metam soil sodium. Consumption in 2003 was nearly five times higher than in 1980 and 3 times higher than in 1995.

The research is to propose an alternative or method for detecting pesticides family of organochlorides, organophosphates in fresh foods especially fruits using electronic noses or multisensory systems.

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II. Theoretical Framework

A. Electronic nose

The multisensory systems are a research and data about 30 years but has boomed in recent years developing new products and finding applications at another time would not be possible to perform them. A multisensory system is based on sensors, which may try to imitate the behavior of the human senses, smell and taste. [2]

During the 80s the researchers focused on a scent machine that would be called electronic nose, a compound of an array of sensors that allowed recognize some odors or physical compounds, a variety of sensors instrument has been developed on the basis of three materials widely used, metal-oxide polymers and enzymatic sensors. These systems constantly being compared with spectrometers or chromatographs, as these instruments once the information we can call data is acquired, this is analyzed and processed by different techniques:

- Principal Component Analysis
- PLS
- Analysis of functional discrimination
- Cluster Analysis
- Diffuse logic
- Neural Networks

Overall the electronic nose is a device composed of four functional stages and it's represented in the figure 1. [3]

- Concentration of volatile
- Capture volatile
- Electronic Control
- Processing information

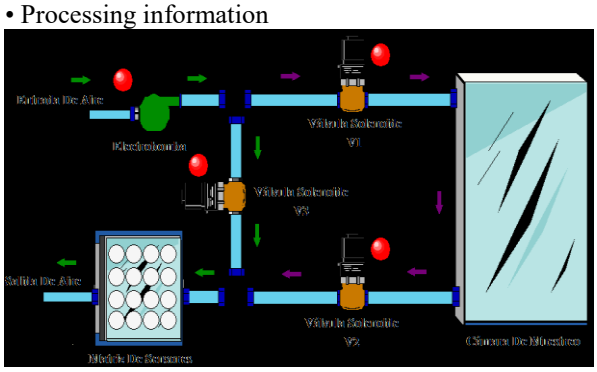

Fig.1. E-Nose general scheme [3]

The concept of electronic nose is born an idea to recreate one of the most complex senses that human, smell, where the olfactory bulb works hand in hand with the brain to easily identify odors, and part chemical concentration, this parallel can be seen in figure 2 along with parts of an electronic nose that starts from sampling the concentration must pass through an array of sensors, that information is captured by a system of data acquisition and then be processed a computer or device and having an output that can be, quantitative or qualitative depending on the amount of information obtained can determine what type of volatile is being examined, a qualitative analysis [4], or extrer full information what concentration where it is expressed in a quantitative analysis, the latter goes hand in hand with the ability of the sensors that are installed in the electronic system [5], because if its maximum detection threshold is a 3ppm example, it would be impossible quantifying concentrations are in the order of ppb, or ppt.

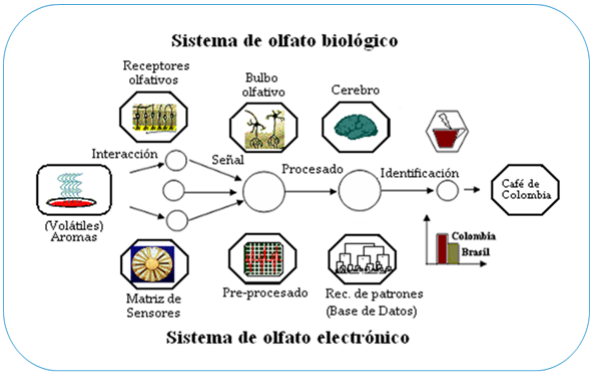

Fig.2. Comparison between electronic nose and olfactory system [6]

Pesticides in fruits and detection

Many years ago before they enter the market pesticides, farmers had to struggle with diseases in their crops that often they represented total loss of their investment by finding the completely damaged product. research developed chemicals that attack the disease directly helping to control their growth and drastically reducing the losses felt this sector of the economy [6], but its benefits have their counterpart and a large number of projects has shown that the use irresponsible of these chemicals have consequences in some cases fatal or carcinogenic to human health.

Because of this precedent many countries to enable food consumption from other countries are looking quite strong controls levels of insecticides or pesticides in food is minimal and has no major impact on health[7].

The most commonly used insecticide and pesticides in general are organophosphates and organochlorides, they can generate a very strong imbalance in ecosystems and directly affect the health of farmers and consumers. Currently the analytical methods to determine the concentration of these substances in food is very complex and in many cases with a fairly high economic component [8][9], the industry needs alternative methods to detect these components in a fast before the product reaches the market or place of shipment.

III. PHYSIC-CHEMICAL ANALYSIS SENSORS AND RESPONE

The first step of the project was to conduct a physical-chemical analysis of fruit with performing the tests should be ensured that the sensors can react to the volatile emitted each food, and can be easily classifiable, if the sensors are not in ability to detect these volatile should choose another type of sensor.

The methodology takes as its starting point the electronic nose B-nose with which account the research group GISM, one of the results of the project is to create a new multi-sensory system, but from this to that have developed a great number of projects, seeking to leverage their strengths and reduce their weaknesses.

A. Try strawberry, blackberry and Uchuva

To try this food a kilo of each fruit is achieved in the marketplace, it is subjected to different conditions and times concentration to determine the ideal for detecting volatile in the multisensory system Thus, in Figure 3 observes the quality of food. It is determined to start 5 minutes concentration time, 2.5 minutes to capture time and 2 minutes for cleaning time on the device, they are going to make 4 samples per test.

Fig.3 Fruits images under study

B. Analysis of results classification fruits

With the data obtained previously will determine whether fruit if they have a different pattern each or is an overlap that prevents proper study and research. Each sample was carried out a pre-processing with reference to the maximum conductance least the minimum conductance divided into the maximum conductance, this is one of the common patterns that work in this system. Once they have done processing the data is loaded and statistical analysis is performed PCA components. The result was very good, because although some samples were alone, most are grouped, which indicates that the sensors respond very good way to fruits studied. Individual PCA are also performed to see the behavior of the samples and determine what may be the best way to perform the sampling.

Figure 4 shows the results of performing the principal component analysis of all samples taken are, although we found a couple of samples a bit scattered, the vast majority behave towards one place, this indicates that the nose is in the ability to discriminate the type of fruit taking as its starting point the samples collected.

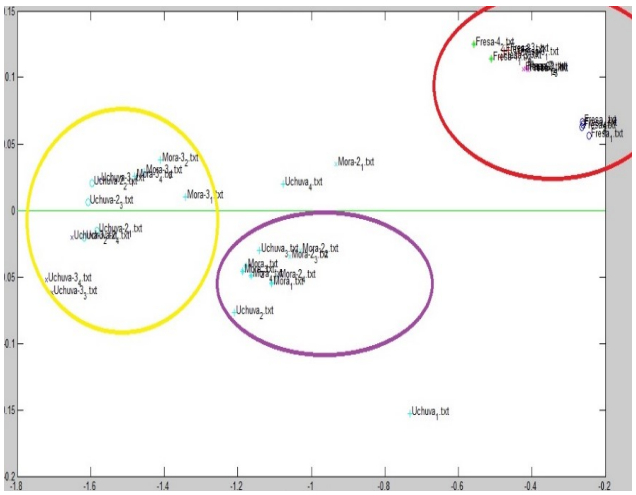

Fig.4. Principal components analysis Strawberry, Mora and Uchuva

A very important aspect in this first research part apart from determining that the MOS sensors with which we at the University of Pamplona were Useful in the rest of the project, also it wanted to check whether affected somehow have the complete, or cut fruit into pieces, in order to determine this factor analysis of main components running on samples of strawberry, blackberry and Uchuva , based on these results the next part of the research, where pesticides and tends to detect and classify against completely organic fruit was designed.

In Figure 5 are 3 of the most widely used crops typical of the region of Norte de Santander, which is prepared is the Pirestar 38 EC fruit pesticides, the idea is to achieve a concentration of 3 parts per million. Although it is quite small, it means a great damage to human health and the environment, the challenge in this first practice is that the sensors are designed to detect substances from 5 parts per million, so the results of this practice will as a result two very important items, the first approval to proceed with construction of a new instrument E-Nose 2.0, with the same MOS sensors seen, and the second most important statement that you can believe a new methodology from the electronic nose for detecting pesticides in fruit. The work schedule is very concise and can be explained as follows:

1. Preparation of the sample with a concentration of 3 ppm
2. The utilization organic fruit (without pesticides) classified by maturity stage 1, 2 and 3
3. Displays with the electronic nose of the pesticide only 100 ml
4. Sample with organic strawberry electronic nose (no pesticide)
5. Sample with strawberry electronic nose with maturity index 1 immersed in the composition of pesticide
6. sample with strawberry electronic nose with maturity index 2 immersed in the composition of pesticide
7. Sample with strawberry electronic nose with maturity index 3 immersed in the composition of pesticide
8. Processing of all results, statistical analysis and neural network to classify 5 classes

Fig.5 Pesticide testing

Due to the same restrictions expressed a paragraph back delay time in achieving acquire the 30 samples necessary to perform processing all the information and have concrete results.

C. Data Processing PCA and neural networks

In the lower left of Figure 6 part are the 3 samples that were loaded strawberry alone without any contaminant, and in the upper right of the group of the other samples corresponding to the remaining four classes is observed, pesticide alone, and strawberry on three levels dipped maturity in the pesticide, this information can be inferred that the response of the sensor allows sorting information of the samples, but the most important thing if you want to make a qualitative analysis nose is completely able to differentiate organic fruit of the contaminated fruit.

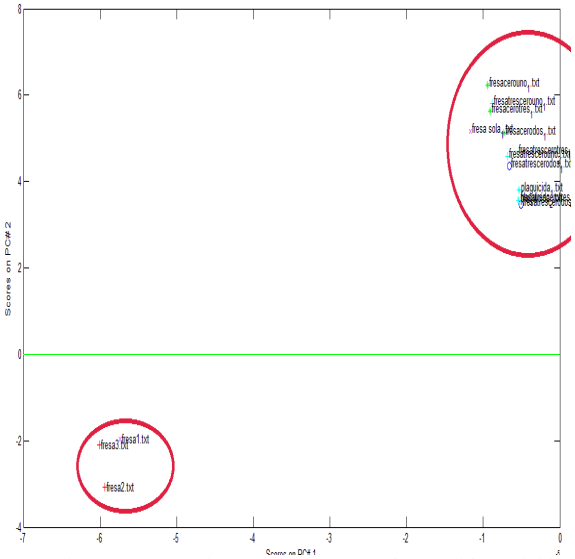

Fig.6. PCA organic strawberry vs strawberry with pesticide

The next step is training a neural network MLP classifier for data, but that are different from those used in the PCA, the method of training the neural network will be in parts, where he trains with data, and it is validated with quite another to test the robustness of the algorithm obtained, defined as a first item five neurons in the hidden and 1 neuron layer in the output layer with activation functions tansig in the hidden and purelin layer in the layer output, the number of iterations scheduled before returning to run the algorithm without finding a good parameter is 100. Once a user-defined order is given start calculating MLP, once completed training results are the following:

TABLE 1. MLP NEURAL NETWORK

Clases	Numero de muestras de entrenamiento	Numero de muestras de validación	Resultado de clasificacion
A	3	3	A-A-A
B	3	3	B-B-B
C	3	3	C-C-C
D	3	2	D-D
E	3	1	E

According to the information in this table and the procedure concludes that the electronic nose could determine the presence or absence of pesticide, and classified into 5 different types depending on the ripeness of the fruit, the pesticide alone and completely organic fruit with these results to the next part of the project where a prototype is built based on the existing B nose is continued, and finally new tests to validate all these results but with the new electronic nose run.

IV. RESULTS

This pesticide is prepared and placed in beakers classifying his concentration, despite being a fairly low concentration the toxic level is quite high so you must use protective equipment required to handle the samples.

Process results of this test can be observed in Figures 10, in a first step the sampling factors are located, then in a glass container 3 strawberry samples are located, then deposited in the fully airtight container and finally you can observe the response of the sensors, which when activated the air flow from the concentration chamber to the gas chamber noticeable changes in the voltage of the FIGARO sensors.

Once completes acquisition of all samples scheduled in Table 4 Class 2, the data acquisition module is closed, and passed to the processing of information, this is done in the processing module of the E- Nose in this regard is made to simple processing.

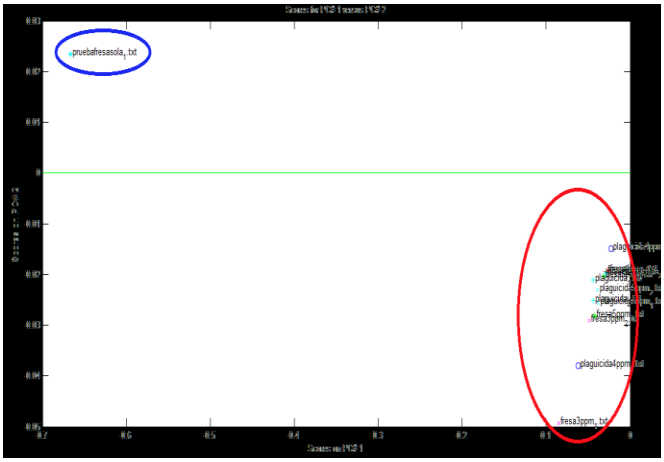

Fig.10. PCA new validation methodology

Similarly trains in the same program a neural analysis parties, where 12 samples train with 6 and confirm with six organizing our samples into two classes, the presence of pesticide or organic fruit, the results are written in Table 2 and shows us that the information embodied in the principal component analysis is true because it gives an error of 0% and a perfect classification of samples tested.

TABLE 2. VALIDATION NEURAL NETWORK

Sample	Neural result validation	Error
Organic fruit	Class 1(Organic fruit)	No
Organic fruit	Class 1(Organic fruit)	No
Plaguicide 3 ppm	Class 2(Plaguicide)	No
Strawberry with 4 ppm	Class 2(Plaguicide)	No
Strawberry with 3 ppm	Class 2 (Plaguicide)	No
Plaguicide with 4 ppm	Class 2 (Plaguicide)	No

V. CONCLUSIONS

A new analysis methodology was developed to detect the presence of pesticides in different from those currently used such as gas chromatography and mass spectrometry, these methods are expensive and are not accessible to small farmers, food analysis with An electronic nose is very economical as we take as reference the equipment cost no more than US $ 500.

The results of the last test show that it is entirely possible to continue this line of research, based on a qualitative analysis is accomplished successfully determine the presence of pesticide in fruit to take the next step in finding a patent in which the nose this electronic able to also sort by concentrations of pesticide, this project may be a little longer for the characterization of all the different types of measures, but with the benefits of the new electronic nose can achieve good results.

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Characterization of CMOS Transistors by Using Transfer Function Analysis

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Abstract – **The paper presents a simulation approach for characterization of integrated CMOS transistors to the needs of analog circuit design. To this aim the main design variables and the key performance indicators of the CMOS transistors are pointed out. A test-circuit for simulation and graphical representation of the relationships between the design variables and the performance indicators is described. It is based on the transfer function analysis mode of the LTspice simulator. The presented approach is examined by using transistors from 22nm bulk CMOS technology.**

Keywords – **CMOS, Design Variable, Performance Indicator, LTSpice, Transfer Function Analysis**

I. INTRODUCTION

The goal of the design of CMOS analog integrated circuits is to determine the operating point and the sizes of the transistors [1, 2, 3]. The operating point can be set by using appropriate gate-source biasing voltage V_{GS} or quiescent current I_D [4, 5]. The channel length L is usually defined by considerations of optimal gain and bandwidth of the circuit [6, 7]. The channel width W is sized according to the parameters of the operating point and the chosen value of L [8]. The gate-source biasing voltage V_{GS}, the quiescent current I_D, the channel length L and the channel width W are design variables of the transistor. They determine the transconductance g_m, the output conductance g_{ds}, as well as the intrinsic gain A_u, which all characterize the performance of the transistors. The intrinsic gain A_u is a key performance parameter, which presents the maximum possible low-frequency small signal voltage gain that a transistor with specified dimensions and biasing can provide in saturation [2]. Despite its value cannot be practically achieved the intrinsic gain A_u gives an useful assessment of the amplifying property of the explored transistor.

The transconductance g_m, and the output conductance g_{ds} can be obtained directly as derivatives of the drain current by using DC Sweep Analysis [2, 6, 7]. The classical test- circuit for evaluation of the intrinsic gain A_u of the MOS transistors by using AC simulations is presented in [2]. The circuit represents a common source amplifier with a transistor in saturation. To avoid some drawbacks of this circuit, a new improved test-circuit is developed in [9]. It allows testing of the intrinsic gain for different values of channel length L at a fixed value of the biasing gate-source voltage V_{GS}. The drawback of the circuit is the need to perform a large number of successive simulations in order to obtain results in the whole range of the biasing gate-source voltage V_{GS}. Another drawback is that the circuit cannot ensure direct determination and visualization of the intrinsic gain A_u as a function of the quiescent current I_D.

An elegant way to simulate the small signal parameters of CMOS transistors by using LTspice simulator is submitted in [10]. To this aim Transfer Function Analysis is proposed to be used. This approach allows to identify the key performance indicators of the examined CMOS transistors avoiding the above described disadvantages of the circuits, presented in [2] and [9].

The paper summarizes and expands the possibilities for characterization of integrated CMOS transistors by using Transfer Function Analysis. To this aim a modified test-circuit and procedures for simulation and graphical representation of the relationships between the small signal performance indicators and the design variables of the transistors are developed. The test-circuit is verified by examination and visualization of the basic small signal characteristics of 22nm bulk CMOS transistors.

II. TEST-CIRCUIT AND METHOD OF INVESTIGATION

Fig. 1 shows the test-circuit for investigation of the key performance characteristics of CMOS transistors. The circuit is based on the test-circuit described in [10]. The examined transistor is presented by two identical transistors Mn1 and Mn. The first one ensures the investigation of the input characteristic. The second transistor Mn ensures the obtaining of the parameters of the output characteristic. The gain of the voltage controlled voltage source V1-E1 have to be high (e.g. 100). This sets the drain-source voltage *VD1* equal to the value of the voltage source V1 for the whole range of the input signal. In this way, the operation of the two transistors in saturation is ensured. The current controlled current source E1-B1 assures identical operating conditions (equal drain currents) for both transistors.

Two type input signals are provided in the circuit. The first source is V2, which allows plotting the small signal parameters in terms of the gate-source voltage V_{GS}. The second source I1 gives possibility to obtain the small signal parameters in terms of the quiescent current I_D.

The circuit includes two 'step' commands, which are executed in the same sequence like they are inserted in the schematic. Consequently, for the test-circuit from Fig. 1 the voltage {VD}(or the current {ID}) determines the x-axis, while the step parameter {v} sets the different values of the sizes of the transistor.

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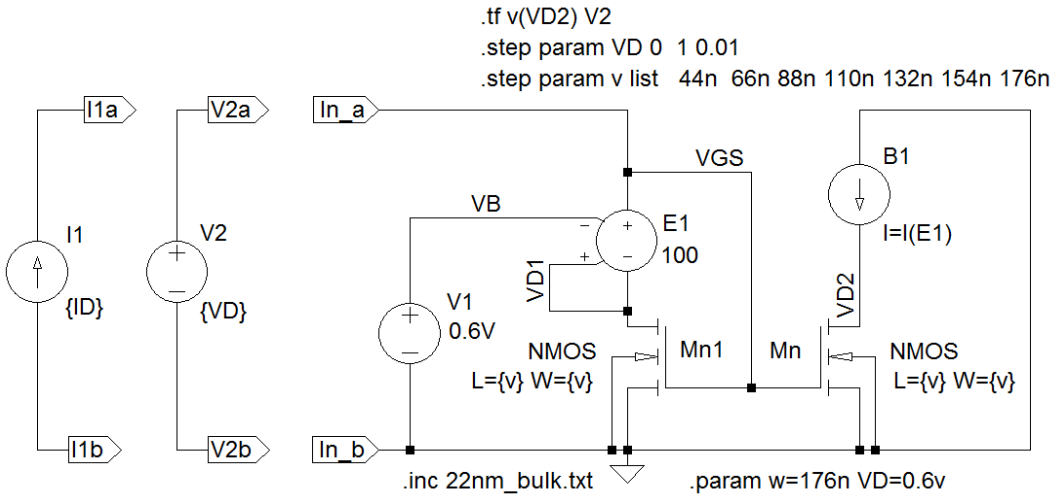

Fig.1. Modified test-circuit for investigation of small-signal parameters of the transistor.

The Transfer Function Analysis gives as results the input impedance r_i of transistor Mn1 and the output impedance r_o of the transistor Mn. Out of them can be determined the transconductance g_m and the output conductance g_{ds}. The formulas are as follow:

$$g_{ds} = \frac{1}{r_o}, \tag{1}$$

$$g_m + g_{ds} = \frac{1}{r_i}, \tag{2}$$

$$g_m = \frac{1}{r_i} - \frac{1}{r_o}. \tag{3}$$

The intrinsic gain A_u can be determined as a ratio of the transconductance g_m and the output conductance g_{ds}:

$$A_u = \frac{g_m}{g_{ds}} = \frac{1/r_i - 1/r_o}{1/r_o} = \frac{r_o}{r_i} - 1. \tag{4}$$

The presented circuit is developed for nMOS transistors. With minor changes in the polarity of the sources, it can be used for investigation of pMOS transistors.

III. Examination of the Test-circuit

The verification of the circuit is carried out by using the transistors from 22nm bulk CMOS technology. This technology is presented in Predictive Technology model site developed by the Nanoscale Integration and Modeling (NIMO) Group at Arizona State University [11]. The simulations are executed by using LTspice program [12].

A. Examination of the performance indicators in terms of the biasing gate-source voltage V_{GS}

Fig. 2 shows the results from investigation of the transconductance g_m, the output conductance g_{ds} and the intrinsic gain A_u of the transistors with channel length L=(2, 4, 6, and 8)L_{min}, W/L=1 and $VD1=VD2$=0.6V at biasing gate-source voltages V_{GS} from 0V to 1V. To this aim the output ports V2a and V2b are connected to the input ports In_a and In_b respectively.

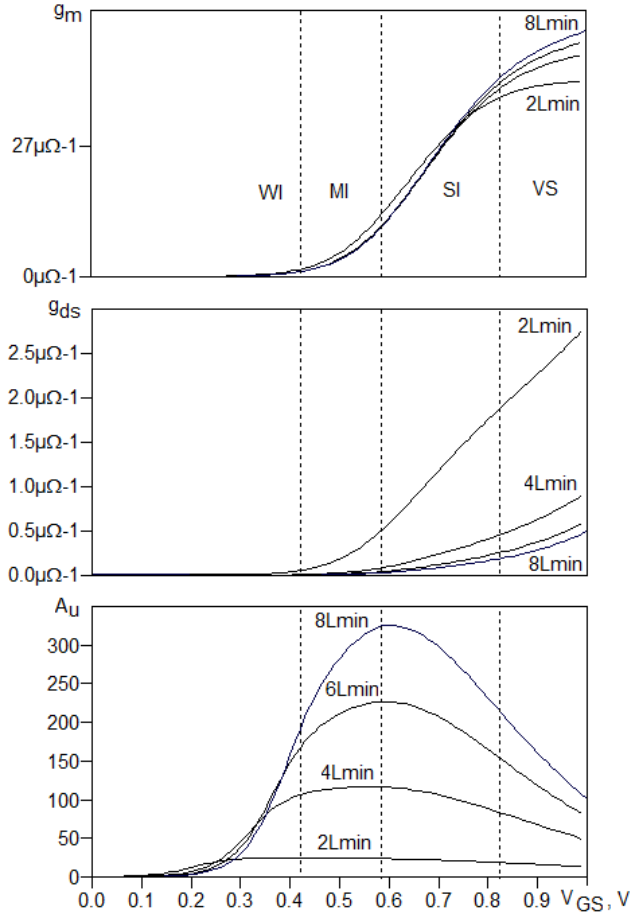

Fig. 2. Results from the simulations by using the modified test-circuit in Fig. 1: a) the transconductance g_m (top plot); b) the output conductance g_{ds} (middle plot) and c) the intrinsic gain A_u (lower plot) vs the biasing voltage V_{GS}.

The type of the obtained transconductance characteristic (the top plot) is typical for the deep-submicron technologies [2, 3, 6, 7]. The four regions of operation are clearly identified – weak inversion (WI), moderate inversion (MI);

strong inversion (SI) and velocity saturation (VS). The threshold voltage is about 0.5V.

The middle plot shows that the output conductance g_{ds} increases with the decreasing of the channel length L from $8L_{min}$ to $2L_{min}$. The minimum of the output conductance g_{ds} is in weak and moderate inversion regions.

The lowest plot presents the intrinsic gain A_u. It shows that the maximum of the gain is around the border between moderate and strong inversion regions (biasing voltage V_{GS} around 0.6V). Transistors with a larger channel length have a greater value of the intrinsic gain.

Fig. 3 presents the results from the investigation of the intrinsic gain A_u at a constant channel length $L=4L_{min}=88$nm and a different channel width $W=(2,4,6$ and $8)L_{min}$. Hence, the aspect ratio W/L of the transistor takes the following values: 0.5, 1, 1.5, and 2. The obtained result shows that the characteristics for different aspect ratios W/L in Fig. 3 are merged into one. This means that at a constant channel length the intrinsic gain A_u is independent of the channel width W. Consequently, the different values of the A_u in Fig. 2c are due only to the different values of the channel length L.

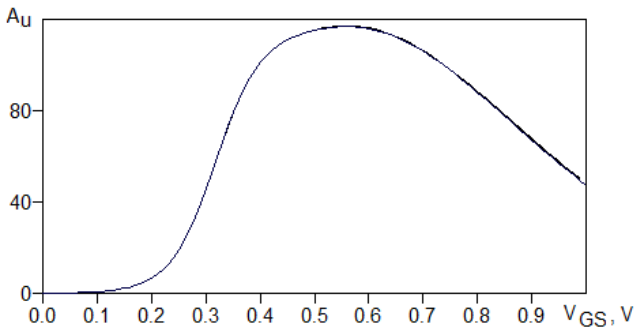

Fig. 3. Results from the simulations of the intrinsic gain A_u vs V_{GS}. ($L=4L_{min}=88$nm, W=(2, 4, 6 and 8)L_{min}, W/L=0.5, 1, 1.5, 2)

The intrinsic gain of the 22nm bulk CMOS transistors by using successive AC simulations is investigated in [9], as well. The comparison between the results presented in [9] and the results from the simulations by using Transfer Function Analysis presented in Fig. 2c shows that they have a close similarity. Fig. 4 gives the relative error ε between these results for the most commonly used input voltage range V_{GS} from 0.4V (moderate inversion) to 0.8V (strong inversion). The error does not exceed 5%. It is due to the different methods for computing the intrinsic gain in both types of analysis.

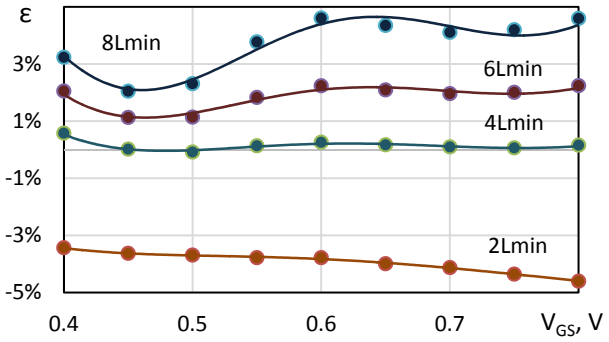

Fig. 4. The error ε between the results obtained by successive AC simulations and the results by using Transfer Function Analysis.

B. Examination of the performance indicators in terms of the quiescent current I_D

Fig. 5 shows the intrinsic gain A_u (low plot) and the transconductance g_m (top plot) of the transistors with channel length $L=(2,\ 4,\ 6,\ 8)L_{min}$, aspect ratio $W/L=1$ and drain voltages $VD1=VD2=0.6$V at quiescent current I_D in the range from 10nA to 20µA. To this aim the current source I1 is used instead of the voltage source V2. The four regions of operation are denoted on the graph. It is seen that the recommendable operating currents are from 70nA (moderate inversion) up to 7µA (strong inversion). The maximum of the intrinsic gain is around the border between moderate and strong inversion regions. The increasing of the channel length leads to the increasing of the intrinsic gain.

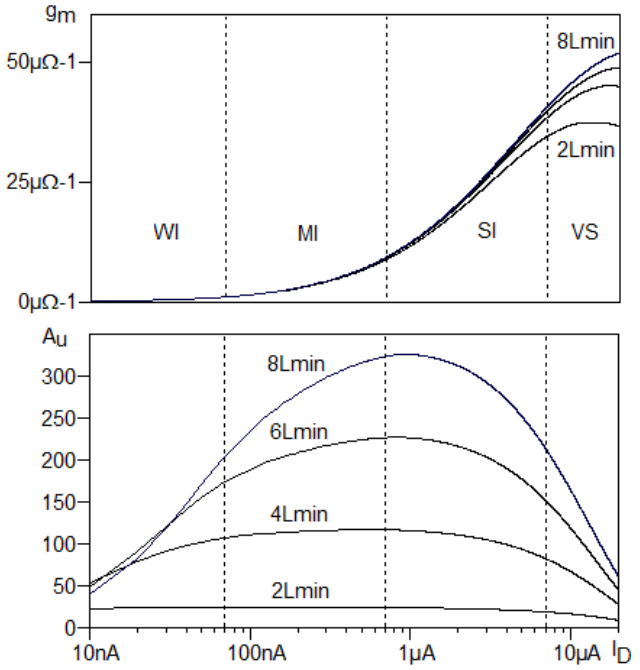

Fig. 5. a) The transconductance g_m (top plot) and b) the intrinsic gain A_u (low plot) vs the quiescent current I_D for $L=(2,4,6,8)$Lmin and $W/L=1$.

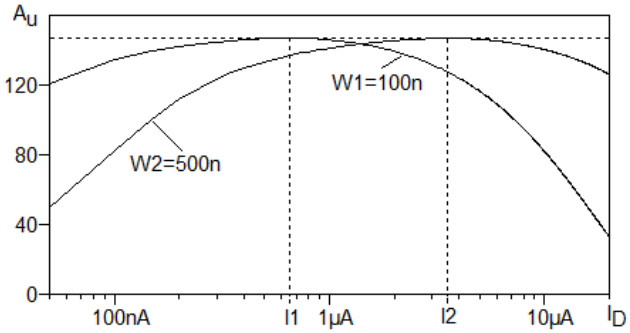

Fig. 6. Intrinsic gain A_u vs quiescent current I_D at values of $W1=100$nm and $W2=500$nm.

Fig. 6 presents the intrinsic gain A_u of the transistors with fixed channel length $L=100$nm and channel width W equal to 100nm and 500nm (aspect ratio $W/L=1$ and 5). The graph shows that the maximum of the intrinsic gain depends only on the channel length L. The channel width W determines the

value of the operating current where this maximum appears (I1 for W1=100nm and I2 for W2=500nm). This graph is suitable for use when dimensioning a concrete analog CMOS circuit.

Another useful plot is shown on Fig. 7. It presents the intrinsic gain A_u vs the channel length L for three values of the quiescent current I_D – 70nA (the border between weak and moderate inversion regions), 700nA (the border between moderate and strong inversion regions) and 7µA (the border between strong inversion and velocity saturation regions), at W=200nm. This graph can be used for preliminary choice of channel length L and quiescent current I_D in the initial stage of the design procedure.

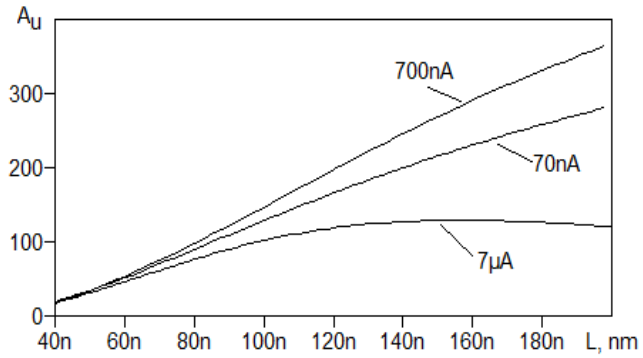

Fig. 7. The intrinsic gain A_u vs the channel length L for quiescent currents I_D=70nA, 700nA and 7µA, at W=200nm.

C. Examination of DC operating point

The LTspice simulator gives the possibility to determine the DC operating point of the transistors in the presented circuit. To this aim, an .OP command is used. It allows to check the mode of operation of the transistors and the values of the operating currents and voltages. Fig. 8 shows the results from the OP analysis of the test-circuit in the conditions of Fig. 5. The curves present the change of the overdrive voltage V_{GS}-V_{th} vs the current trough the examined transistors. The straight lines indicate the values of drain-source voltage *VD1* and *VD2* of the transistors. The overdrive voltage is smaller or equal to the drain-source voltages of the both transistors for the whole range of the drain current I_D. Hence, the both transistors operate in strong inversion region, as required.

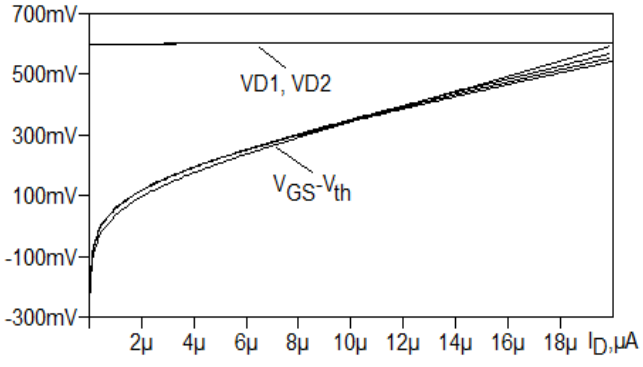

Fig. 8. The overdrive voltage V_{GS}-V_{th} and the drain-source voltages *VD1* and *VD2* vs input current *I1*.

IV. Conclusion

The paper summarizes and expands the possibilities to use the Transfer Function Analysis of LTspice simulator for characterization of integrated CMOS transistors to the needs of analog circuit design. To this aim the well-known approaches for determination of transconductance g_m, output conductance g_{ds} and intrinsic gain A_u, by using successive DC simulations, are described and theirs drawbacks are presented. To avoid them a modified test-circuit and procedures for investigation of the key performance characteristics of CMOS transistors are developed (Fig. 1). The circuit is applied to examine the transistors with different sizes from 22nm bulk CMOS technology. The obtained results present the basic performance indicators of the transistors in terms of the biasing gate-source voltage V_{GS} (Fig. 2, Fig. 3 and Fig. 4) and in terms of the quiescent current I_D (Fig. 5, Fig. 6 and Fig. 7). A simple way to check the mode of operation of the transistors by using DC operating point analysis is demonstrated (Fig. 8).

With minor changes in the polarity of the sources the presented circuit can be used for investigation of pMOS transistors.

The considered approach can be applied for determination of the basic performance parameters of new unknown technologies in the initial stages of circuit design and dimensioning.

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Removing Multiple Switching by Using Circuit with Dynamic Hysteresis

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Abstract - **A novel method for removing multiple switching at the edges of digital signals based on a comparator with dynamic hysteresis is presented. The proposed concept is analytically investigated and a CMOS circuit is designed based on the obtained results. Simulations with Spectre simulator demonstrate its correct operation.**

Keywords - **Schmitt-trigger, dynamic hysteresis, CMOS**

I. Introduction

It is often needed in practice to recover a clock or other digital signal from a noisy input signal with small amplitude. The standard solution is to use a comparator with hysteresis, which in reality represents Schmitt-trigger [1-3]. However, if the amplitude of the input signal varies in a wide range, then it is not easy to choose the threshold levels of the hysteresis. If the hysteresis is small, then multiple switching can appear at the edges of the output signal. In the opposite case, large amplitude of the hysteresis results in a big time and phase delay of the output signal. To solve this problem, a comparator with dynamic hysteresis is proposed in [4]. Here, the amplitude of the hysteresis can be made large without adding a phase delay to the output signal. It is possible to extend the difference between the threshold levels so much, that the upper one becomes higher than the supply voltage and the lower one less than the ground potential. Then this comparator can be used to remove multiple switching at the edges of digital signal, which is applied at its input. Thus, the original features of the dynamic hysteresis, which were employed initially in mixed-signal circuits, e.g. ADC [5], are implemented in a digital design.

Such a CMOS comparator is the topic of the presented paper. The work is organized as follows. In the section II the basic principles of the Schmitt-trigger with dynamic hysteresis are shown. In the section III a circuit of CMOS comparator with dynamic hysteresis capable to remove multiple switching at the edges of digital signal is proposed and investigated. Simulations with Spectre simulator are used to check its operation and their outcome is shown in section IV. In the last section of the paper some conclusions based on the achieved results are presented.

II. Dynamic Hysteresis Principle

The idea behind the classic Schmitt trigger (ST) concept is the use of positive feedback (PF). It causes fast transition time at the output and two different input thresholds (hysteresis). Thanks to these features ST is used mostly to turn noisy or slowly varied input signals into clean digital output signals. Hence ST is very convenient for comparator circuits, except to the fact that a comparator needs only one switching level for positive- and negative-going input signal. Voltage-transfer characteristic of a non-inverting ST and its schematic symbol are shown in Fig. 1(a) and Fig. 1(b) respectively.

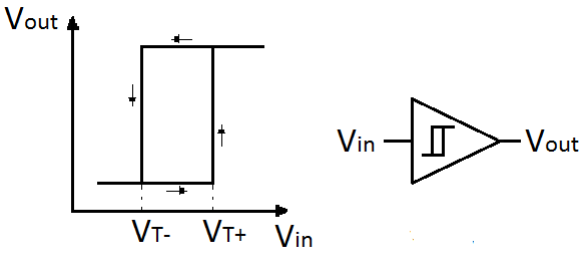

Fig. 1. (a) Voltage-transfer characteristic of a non-inverting ST. (b) Schematic symbol of non-inverting ST.

The Fig. 2(a) depicts ST input/output signals and the variations of the threshold between both levels, higher $VT+$ and lower $VT–$. It is worth to note: First, the two switching levels are the same as the threshold levels $VT+$ and $VT–$. And second, between two switchings the threshold stays stable. It is known that for a system with feedback (Fig. 2(b)) the gain K_F equals: $K_F = K_0/(1- \beta K_0)$, where K_0 is the gain without feedback and β is voltage-transfer coefficient of the PF circuit itself. The necessary and sufficient condition for existing of trigger effect is $\beta K_0 > 1$

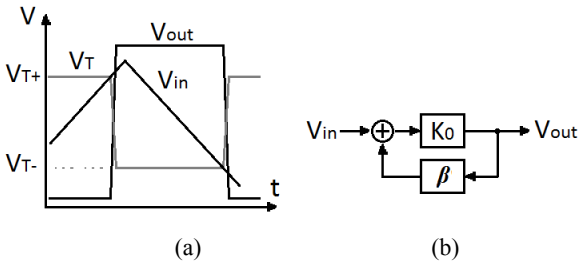

Fig. 2. (a) ST input/output signals and the variations of the threshold between both levels, higher $VT+$ and lower $VT–$. (b) Principle schematic of ST.

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As mentioned in the introduction, sometimes it is difficult to choose the right threshold levels of the hysteresis in the ST. Fig. 3(a) shows what happens when the amplitude of the hysteresis (*VT+ - VT–)* is too small and Fig. 3(b) when it is too large.

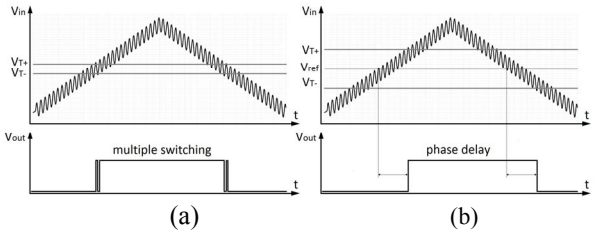

Fig. 3. (a) Input/output signals of ST with small amplitude of the hysteresis. (b) Input/output signals of ST with large amplitude of the hysteresis.

It is desirable to keep the inherent ST's speed and noise immunity and to create new schematics with only one switching level. For this purpose the threshold must behave as is shown in Fig. 4(a). This should be feasible if every switching generates after some delay t_D a signal to stop PF operation by neutralizing or breaking it off and restore initial value V_{ref} of the circuit threshold (Fig. 4(b)). So during a period of time t_D the threshold voltage changes to be in the opposite direction of the input signal change.

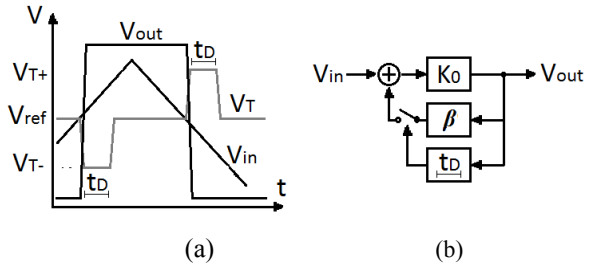

Fig. 4. (a) Desired variations of the threshold between both levels, higher *VT+* and lower *VT–*. (b) Principle schematic.

The new comparator (Fig. 4(b)) has one switching level V_{ref} keeping the thresholds, higher *VT+* and lower *VT–* like a ST but only for period t_D after it has switched. This time-domain phenomenon is called "Dynamic Hysteresis" (DH) [4]. If the interval t_D is controllable then the time domain insensibility can be adapted so that the noise added to the input signal to be rejected. At the moment when the comparator begins to switch, its threshold is always the same (Fig. 4(a)). Therefore no additional phase delay is added to the input signal no matter how big is the amplitude of the hysteresis. Thus the threshold levels *VT+* and *VT–* can be made high and respectively low enough to ensure that no multiple switching appears at the edges of the output signal.

III. CMOS Transistor Level Implementation

A proposed CMOS implementation of Comparator with DH is shown in Fig. 5 [6]. It is based on the ST from [3].

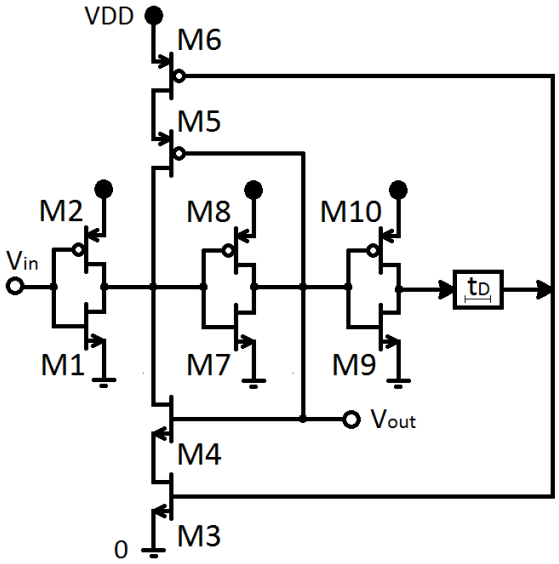

Fig. 5. Circuit of CMOS comparator with dynamic hysteresis.

Here the inverter M1/M2 determinates the switching level for the input signal. The inverter M7/M8 together with M4 and M5 build PF (Fig. 4(b)). M3 and M6 serve as switches enabling or breaking the PF. The block producing the delay t_D can be implemented in different ways. Some of them are shown in Fig. 6(a,b,c,d).

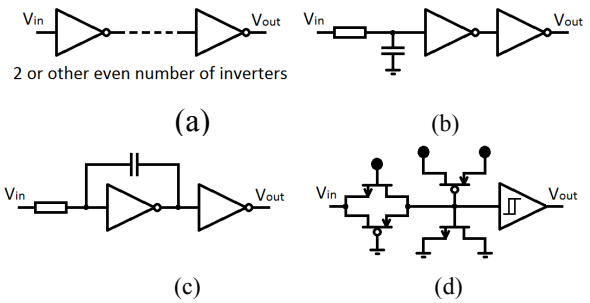

Fig. 6. (a) Delay with inverters. (b) Delay with low-pass filter. (c) Delay with integrator. (d) Delay with low-pass filter built using only transistors.

The circuit from Fig. 6(a) is suitable for some nanoseconds delay, from Fig. 6(b) for some hundred nanoseconds delay, from Fig. 6(c) up to some microseconds delay and from Fig. 6(d) for pure digital CMOS process avoiding use of resistors and capacitors. If the delay t_D is much longer than the switching delays of the transistors in the circuit, then the duration of the DH, and therefore the time domain insensibility depends only on t_D. When needed, t_D could be made controllable.

After the ST with DH has changed its state and the hysteresis is active, the threshold level depends on the ratio *RonM1/(RonM5+RonM6)* for the upper threshold or *RonM2/(RonM3+RonM4)* for the lower threshold. *Ron* is the channel resistance of MOS transistor

working in linear region with gate-source voltage equal to the supply voltage. Let
RonM1>>RonM5+RonM6 and
RonM2>>RonM2+RonM3 .
This means that if M5 and M6 (or M2 and M3) are simultaneously set switched on, M1 (or M2) cannot change the voltage at its output. Therefore the upper threshold level is higher than the supply voltage and the lower is less than the ground potential. Let the amplitude of the input signal of a ST with DH, whose transistors satisfy this condition, is always between the supply voltage and the ground. Then the comparator does not react on any change of its input, from the switching event to the end of the duration of the DH.

The circuit from Fig. 5 was designed in 350nm AMS CMOS Technology [7]. The width/length of the transistors are as follows (in micrometer): M1 0.4/1.1, M2 0.4/0.35, M3 and M4 1/0.35, M5 and M6 2.8/0.35. The block producing the delay t_D was implemented like in Fig. 6(d). t_D equals nominal about 400ns.

IV. Simulation Results

Results from transient simulation of the proposed circuit with Spectre simulator are shown in Fig. 7.

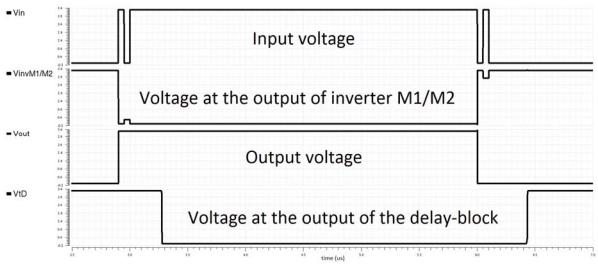

Fig. 7 Spectre simulator results.

It can be seen, that the output signal stays stable during the period t_D despite the multiple switching of the input signal.

V. Conclusion

The concept of Schmitt-trigger with dynamic hysteresis was originally introduced for circuits processing analog signals. However this paper shows that it could be successfully used in the digital domain too. The presented CMOS circuit based on this concept is able to remove multiple switching at the edges of digital signals and its time domain insensibility could be made controllable. Transistor level simulations of solution implemented in pure digital CMOS process demonstrate its capability.

Acknowledgments

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Low Noise Power Supply for Precision Analog-to-Digital Converters in Battery Monitoring Systems

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Abstract – **The subject of this article is the development and the testing of a low noise DC-DC power supply for high precision Analog-to-Digital Converters and signal conditioning circuits in a battery monitoring systems. The synthesized structural diagram includes a low voltage input DC power supply, a resonant voltage inverter, a fast recovery rectifier, a filter and a linear voltage regulator. Different types of rectifiers and filters are tested as well as different linear voltage regulators. A Zero Voltage Switching Royer oscillator is used for maximal efficiency of the step-up converter and minimal radio interference and noise.**

Keywords – **DC-DC converter, Zero Voltage Switching, Royer oscillator, Low-noise power supply**

I. Introduction

In almost every portable data acquisition system the main part is the power supply. It generates all of the voltages required for system operation from a single low voltage DC power supply. In some of the cases the powered circuits are analog front-end circuits working with very small signals and Analog-to-Digital Converters (ADC) which are sensitive to the power supply voltage ripple and Radio Frequency (RF) interference. Switching Mode Power Supplies (SMPS) are widely used because of their ability to step up DC voltage and for their higher efficiency. But they generate a lot of RF interference and output ripple, that affects the accuracy of the measurement. Usually up to 6 Least Significant Bits (LSB) of the *12-bit* ADC resolution can be lost. The signal-to-noise ratio is also affected. With a standard SMPS the noise floor can be increased with more than 40 dB even if a linear voltage regulator is used to regulate its output voltage.

These problems can be solved by using a resonant Zero Voltage Switching (ZVS) oscillator also known as Royer oscillator [1]. The output voltage of the oscillator is rectified, filtered and regulated with a wideband Low Dropout (LDO) linear voltage regulator [2]. The absence of hard-switching regulator decreases the generated noise and interference significantly. The efficiency is lower compared to a standard SMPS due to the usage of a linear voltage regulator. If the input voltage tolerance is narrow the efficiency can be maximized to levels comparable with a standard SMPS.

In this paper an inductive-capacitive filtration is compared to a capacitive filtration. The efficiency, interference and output noise are tested. A series resistive-capacitive circuit is used to reduce the ringing of the secondary winding when the rectifier diodes are switched off. The interference spectrums with a capacitive and inductive-capacitive filters are simulated and compared to each other.

II. Structure of the Low Noise Power Supply

The structural diagram of the power supply is represented on Fig. 1. The DC voltage from the battery is applied to the ZVS oscillator which uses a transformer for a load. The transformer has two primary and several secondary windings for the different output voltages. The secondary voltage can be electrically connected to the input or completely isolated. The high frequency AC voltage is rectified by bridge rectifier with super-fast recovery diodes. It is then filtered with a capacitive or inductive-capacitive filter. The rectified and filtered voltage is then applied to the LDO regulator for voltage regulation and filtration of the remaining noise and high frequency ripple.

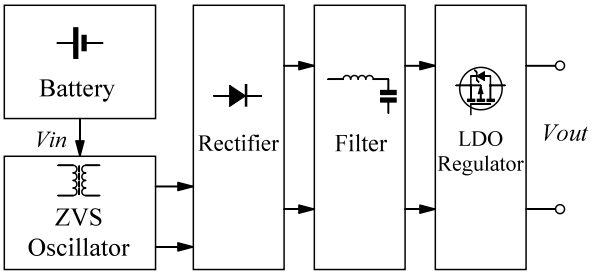

Fig. 1. Low Noise Power Supply structural diagram

III. Structure of the Zero Voltage Switching Oscillator

The stepping up of voltage and the galvanic isolation is performed by a resonant ZVS self-oscillating converter with a transformer. The push-pull circuit known as Royer oscillator consists of a transformer with one center-tapped primary winding, a resonant capacitor, two transistors and a feedback winding. The switching happens normally at zero voltage where the switching losses are very small. The primary and secondary voltages are very close to sine waveform with low harmonic components [3]. The input voltage is applied to the center tap of the primary through an inductor. It acts as a current source for the working frequency of the oscillator [4]. The circuit has two modifications - with bipolar transistors and with MOSFET transistors. The MOSFET version does not use a separate

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feedback winding as the control of the gate of each transistor is done with a Schottky diode connected to the drain of the transistor in the opposite arm of the oscillator.

The schematic of the MOSFET version of the oscillator is shown on Fig. 2:

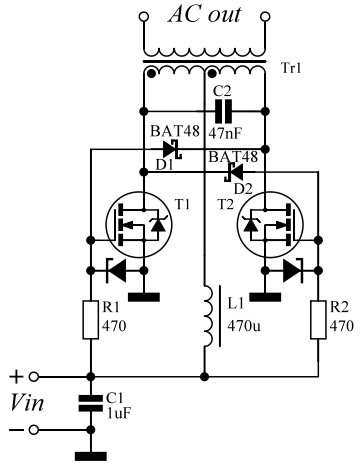

Fig. 2. MOSFET ZVS oscillator schematic diagram

The MOSFET version has a number of advantages:
– does not need additional feedback winding which simplifies the transformer construction and the schematic;
– the value of the resistors R1 and R2 does not depend on the drain current (a higher power can be achieved with less losses into the gate resistors);
– in applications with high power the use of MOSFETs with low channel resistance can reduce the on state power losses.

As can be seen from the advantages listed above, the MOSFET version becomes more effective at high power levels [4]. For low power applications the circuit becomes more inefficient due to the following:
– the relatively high threshold voltage of the MOSFETs limits the minimal input voltage to about 6V;
– the high gate-source capacitance requires a lower R1 and R2 values to achieve a reasonable switching times even for low power applications. This increases the idle power consumption of the oscillator.

For that reason the bipolar version of the oscillator is more appropriate in this case. Its schematic diagram is represented on Fig. 3:

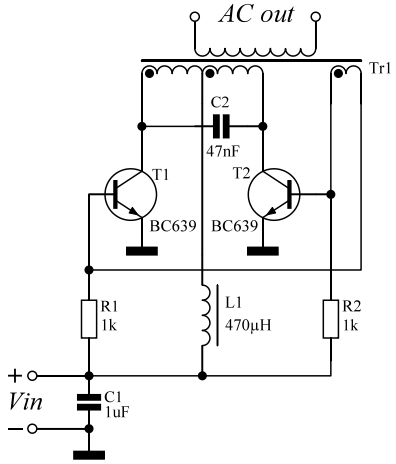

Fig. 3. Bipolar ZVS oscillator schematic diagram

The oscillation frequency depends on the resonant frequency of the parallel resonant circuit, formed from the inductance of primary winding of the transformer Tr1 and the capacitance of C2 [4]. It is given by Eq. 1:

$$F_{osc} = \frac{1}{2\pi\sqrt{L_{Tr1}C_2}} \quad (1)$$

If the secondary winding has a capacitive load the reflected secondary capacitance should be calculated and added to the primary side in order to calculate the resonant frequency accurately.

The primary winding inductance determines the circulating current in the resonant circuit. For a constant supply voltage and working frequency the current is inversely proportional to the primary inductance [5]. The losses in the primary resonant circuit are proportional to the circulating current so its value is affecting the idle current of the oscillator. When the circulating current is high, the losses in the contour and the idle current of the oscillator are high too. Due to that fact, the inductance of the primary winding should be calculated for circulating current which will give the desired idle current of the oscillator.
The inductance of the choke L1 is chosen to be at least 4 times higher than the inductance of the primary winding in order to be a good constant current source for the working frequency.

IV. Structure of the Rectifier and Filter

The secondary voltage from the ZVS oscillator is rectified by bridge rectifier with super-fast recovery diodes. The working frequency of the oscillator is chosen to be 45kHz in order to achieve a smaller transformer core with low switching and ferrite losses. The filtration of the rectified voltage is done with two different arrangements - capacitive filtration or inductive-capacitive filtration. The first concept has advantage of simple and compact construction without inductive elements. The drawbacks are lower power factor with around 180 degree conduction angle, and high peak currents distorting the oscillator waveform and producing more interference. The inductive-capacitive filter has better power factor with near 360 degree conduction angle, with lower peak currents and less interference radiation [6]. It requires around 1,3 times higher secondary voltage for the same output voltage. The circuit diagram of the rectifier with the two different filter arrangements is represented on Fig. 5:

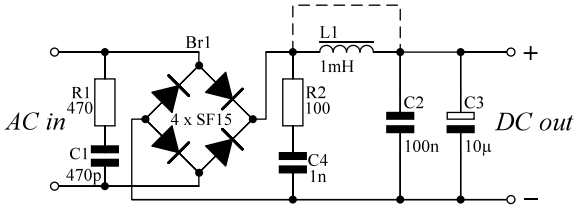

Fig. 5. Rectifier and filter circuit diagram

The circuit R1, C1 damps the ringing of the secondary winding when the diodes from the bridge rectifier turns off.

The R2, C4 circuit damps the ringing of L1. C3 is the main output filter capacitor bypassed by C2.

In the inductive-capacitive filter configuration, the rectifier conduction angle is close to 360 degree. The output current of the ZVS oscillator is with a trapezoid shape and due to this the power factor is less than one. If the output load current is relatively constant in time, the values of C4 and L1 can be chosen in such way that the secondary current of the ZVS oscillator is very close to a sinusoid. This means that the power factor will be very close to one and the generated interference will be the lowest.

V. Structure of the Low Dropout Voltage Regulator

The wideband low dropout voltage regulator is designed using a P channel MOSFET transistor in common source configuration for pass element and operational amplifier for error amplification. The basic circuit is known as Sulzer regulator. The pass element is replaced by PMOS transistor to reduce the minimal forward voltage drop. The circuit diagram of the regulator is shown on Fig. 4:

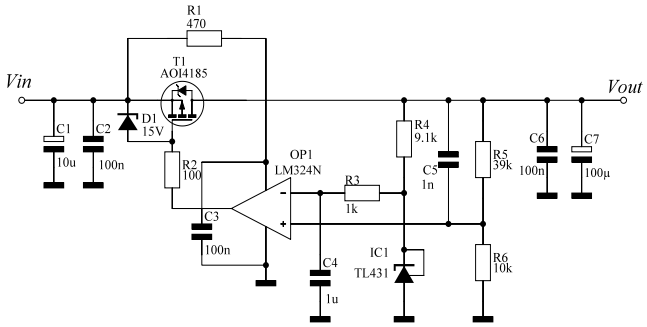

Fig. 4. Low Dropout Voltage Regulator circuit diagram

The use of PMOS in common source configuration for pass element gives the regulator incomparably low minimal voltage drop less than 20mV at 1A current. The Sulzer circuit concept gives the regulator excellent input ripple rejection with low output noise and low output resistance under 100mΩ.

LM324N is chosen for operational amplifier due to its low cost, single power supply with wide range from 3V to 32V and the wide input and output voltage ranges. The supply voltage for the operational amplifier is taken from the input of the voltage regulator and is filtered by R1 and C3. The reference voltage is produced by a shunt regulator with TL431 powered from the output of the regulator. This technique improves the ripple rejection ratio significantly. The feedback is taken from a resistive divider R5, R6. The value of the output voltage is given by Eq. 2:

$$V_{out} = U_{ref} \frac{R5 + R6}{R6} \qquad (2)$$

The capacitor C5 compensates the frequency response of the voltage divider for high frequencies and improves the stability of the regulator.

The MOSFET in common source configuration is effectively a variable current source. The phase shift with the complex load connected to the high impedance drain terminal is undefined and makes the circuit prone to oscillation. The capacitors C6 and C7 are stabilizing the regulator [2].

VI. Experimental results

A full simulation test of the low noise power supply is done in LT Spice. The bipolar transistor version of the ZVS oscillator is tested together with the rectifier and the filter. The LDO regulator is tested separately.

The collector voltage waveform of T1 is shown on Fig. 6. On Fig 7 is shown the voltage at the center tap of the primary winding of the transformer. The secondary winding waveform is shown on Fig. 8. On Fig. 9 is shown the secondary current of the oscillator. For each diagram the oscillator works with 6V input voltage, inductive-capacitive output filter and 100mA load current at 14V DC:

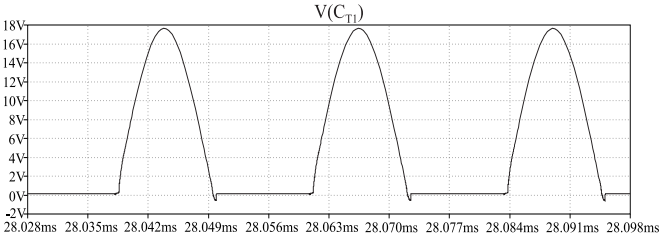

Fig. 6. T1 collector voltage waveform

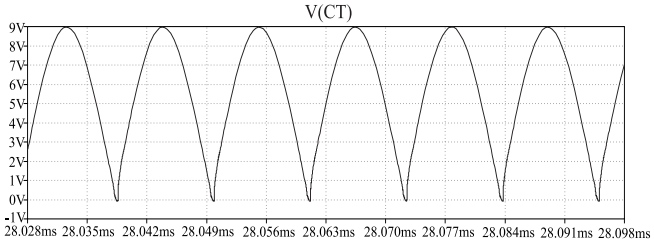

Fig. 7. Primary winding center tap voltage waveform

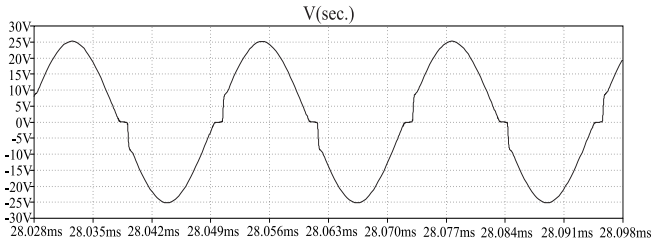

Fig. 8. Secondary winding voltage waveform

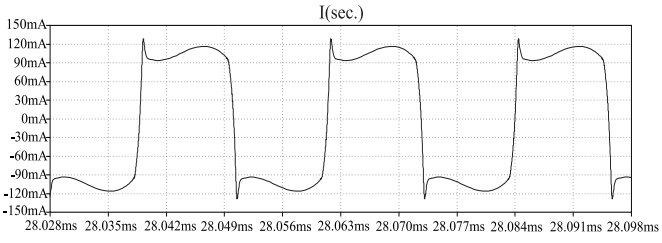

Fig. 9. Secondary winding current waveform

The LDO voltage regulator simulation is represented on the following diagrams. On Fig. 10 a voltage step change with 4 volt amplitude and 100 ns rise and fall times is applied to the input of the regulator and the reaction of the output voltage can be seen on the second subplot.

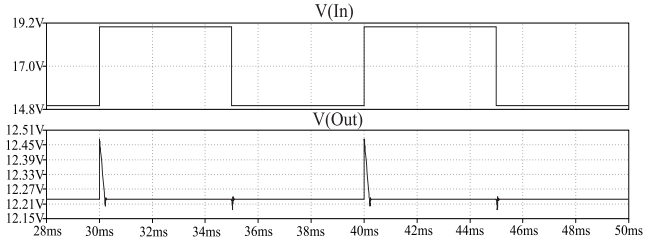

Fig. 10. Input and output voltages of the LDO regulator

The reaction of the LDO regulator to a load current step change is represented on Fig. 11. The load current is stepped from 0 to 200 mA with 100 ns transitions, the reaction of the regulator is represented on the second subplot.

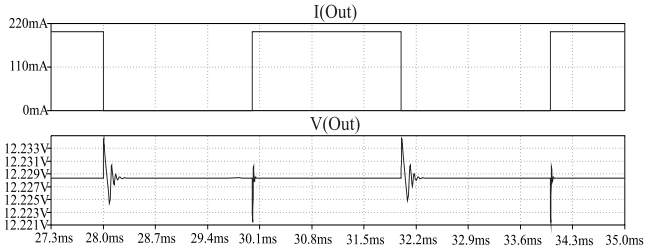

Fig. 11. Output current and voltage of the LDO regulator

The spectrum of the output ripple voltage with capacitive and inductive-capacitive filtering is compared on Fig. 12 and Fig. 13.

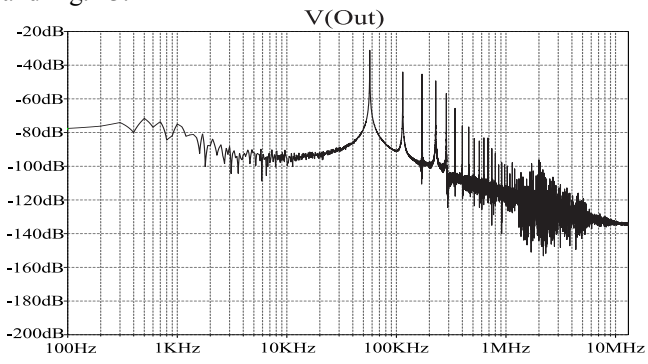

Fig. 12. Output spectrum with capacitive filtering

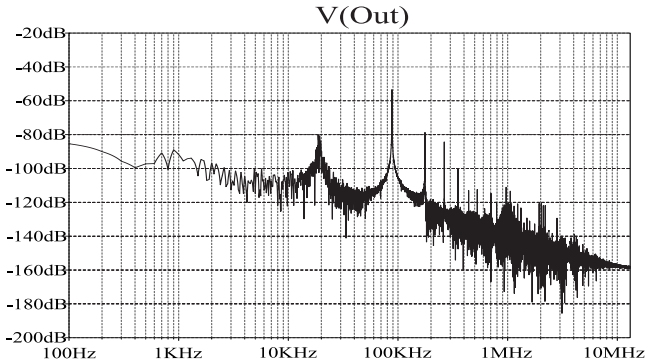

Fig. 13. Output spectrum with inductive-capacitive filtering

VII. Conclusion

The developed low noise DC-DC power supply have simple construction, relatively high efficiency and excellent RF interference characteristics. The design can be scaled easily in size and power to work from 1 to 60 volts input voltage and from 1 mW to 100 W output power. This makes the field of application of the design very wide. The practical tests confirmed the simulation results completely. The influence of the power supply output noise to a standard successive approximation ADC was tested and the noise dropped to around 2-3 LSB compared to a 5 LSB with a standard SMPS module (AIMTEC AM1D-0512DZ) with LM7806 linear voltage regulator at its output. The influence of the power supply was also observed as a noise floor reduction in the analog signal conditioning circuit. The noise floor dropped from -40dB with the standard SMPS to -75dB with the low noise power supply.

From the experiments we can conclude that the power supply finds wide range of application from all type of mobile data acquisition systems to the telecommunications equipment. The low output noise makes the converter suitable for millivolt range measurement in battery monitoring systems.

The developed wide band LDO linear voltage regulator showed excellent parameters in the testing with high input ripple rejection and extremely low voltage dropout. Under 20 mV with 0.5 A load current at 7V input voltage. These properties combined with the low cost and the ability to be scaled to high power applications makes the use of the regulator possible even without the ZVS step-up converter.

Acknowledgements

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Low Noise Preamplifier Suitable for High Impedance Sources

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Abstract – **The amplification of low signals from inductive transducers is not an easy task. Existing integrated amplifiers are good enough but in some applications the requirements are for better signal to noise ratio and high gain. For example the LT1028/LT1128's voltage noise is less than the noise of a 50Ω resistor. Here we are discussing the practical aspects for designing an ultra low noise preamplifier with input voltage noise less than 5Ω resistor, which is about 0.3nV/√Hz.**

Keywords – **Low Noise Preamplifier**

I. INTRODUCTION

This paper covers practical aspects for building a contemporary ultra low noise preamplifier. The purpose of the experiments is to use this preamp on the first stage at the reproduce magnetic audio head. The signal generated from the head depends on the tape speed and the reference flux, but the typical values are between 0.17mV (tape speed of 4.76cm/s and track width of 0.6mm) and 4mV (tape speed of 38cm/s and track width of 2.75mm). The playback head has typical inductance about 200mH and resistance about 220Ω up to 350Ω. The self thermal noise of the head is about 1.9nV/√Hz to 2.4nV/√Hz and can be calculated by the simplified equation for the environment temperature of 25°C [4]:

$$Vn = 0.128\sqrt{R} \qquad (1),$$

where the R is the impedance in Ω and the Vn is the voltage variance in nano-volts per hertz of bandwidth. Because of the high source impedance of the head, it is good to use low input current noise stage on the front. For this purpose the input with JFET (Junction gate Field-Effect-Transistor) is better than the BJT (Bipolar Junction Transistor). There are many good working designs that use 2SK170 [1] and 2SK369 [3] on the front. Some of them use discrete components, the other are mixed with operational amplifiers on the second stage [2].

A. Initial research

The 2SK170 and 2SK369 produced by Toshiba are obsolete parts and are no longer supported and manufactured. There is replacement component from Linear Technologies, which part number is LSK170 [5]. It is good to be used but is hard to be found and it is very expensive. The input voltage noise of the LSK170 is about 0.9nV/√Hz, which is perfect for most designs. There is another good JFET transistor for the first stage, produced by NXP. Its part number is BF862 [6], it is easy to find and is not so expensive. Its input voltage noise is better than the LSK170 and is about 0.8nV/√Hz.

The source impedance is important for the type of the first stage. The JFETs have significant voltage noise compared to the good bipolar low noise transistors. On the other hand, the BJTs have significant current input noise, so the high impedance adds additional noise component. For the low impedance sources this component is relatively small, compared to the significant input voltage noise of the JFET. Comparison of some good low noise BJT [1] shows the proper ones for the input stage. As can be seen, the noise of the transistor primary depends on its equivalent base spreading resistance ($r_{bb'}$).

TABLE 1. LOW NOISE BJT

Model	Beta	Vn [nV/√Hz]	$r_{bb'}$
2N5210	350	2.01	227.9
2SC2362	188	1.55	130.5
2SC2909	155	1.47	115.4
2N5551	131	1.41	104.5
2SC2240	174	0.96	41.5
KSC3503	107	0.72	17.6
MJE15030	88	0.63	10.1
2SC3601	135	0.51	1.9
2SC2547	274	0.51	1.7

For low source impedances, the $r_{bb'}$ of transistor should be added to the source resistance r_s. That way it is performing as additional noise generator. There are other good transistors, not listen in Table 1. The 2SB737/2SD786 are listed on the specs with $r_{bb'}$ of a 2Ω but in the measurement their $r_{bb'}$ is much higher and is about 7.5Ω[7]. The 2SA1316/2SC3329 have $r_{bb'}$ of 2Ω and e_n of 0.6nV/√Hz. The wideband transistor BFW16A has h_{FE}>40 and measured $r_{bb'}$ of 4Ω. The 2SA1083-1085 and 2SC2545-2547 family belongs to the Hitachi. They have equal measured $r_{bb'}$ values about 14Ω. In the measurements, the commonly available BC337 ($r_{bb'}$=30Ω) is slightly better than the SMD version BC817-40. The 2SA1312/2SC3324 ($r_{bb'}$=20Ω) are the SMD replacement of the 2SA970/2SC2240. Obsolete 2SC2263U ($r_{bb'}$=15Ω) was designed for head preamps and its h_{FE} is 520-1040.

Analog Devices produces a pair of matched transistors. Its part number is MAT12. Their input voltage noise is 1nV/√Hz and the $r_{bb'}$ is 28Ω. THAT Corporation also produces array of four matched transistors. They call their array *THAT 300* and consist of four NPN (THAT 300), four PNP (THAT 320) and a pair of two NPN and two PNP

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(THAT 340). The input voltage noise for the PNP transistors is 0.75nV/√Hz; while the noise for the NPN is 0.8nV/√Hz. PNP base spreading resistance is 25Ω, while the NPN is in the range of 30Ω to 32Ω.

The BJT transistors have significant input current noise. For example typical Shot noise of a low noise transistor with β of 100 and 1mA collector current will produce 1.8pA/√Hz input current noise [8]. This high input current noise will produce another noise component at high source resistance. For example, the resistance of a typical moving magnet cartridge is about 1.5kΩ. The additional noise component, generated by the input current noise will be about 2.7nV/√Hz. The self thermal noise for 1.5kΩ source is about 4.96nV/√Hz. Adding different noise components can be done using:

$$Vs = \sqrt{V_1^2 + V_2^2 + \ldots + V_n^2} \qquad (2),$$

where *Vs* is the equivalent noise from the *n* voltage noise sources. The equivalent noise from the source based on the example above will be 5.65nV/√Hz (for the BJT) instead of 4.96nV/√Hz if we use JFET.

B. Topology

There are many good working designs [1,2,3] for low noise pre-amplifiers using JFET input. Traditional designs use good low noise op-amp and a differential pair of JFET in front of it. These designs use negative voltage feedback (VFB). The design presented in this paper use current feedback (CFB) in a type of a Comlinear amplifier. One primary difference between the CFB and VFB amps is that the CFB amplifier does not have a constant gain-bandwidth product. While there is a small change in bandwidth with gain, it is much less than the 6 dB/octave we see with a VFB op amp. Current feedback amplifiers have excellent slew-rate capabilities and this was a major for the design choice.

To rate the noise product of the amplifier, it is good to know how different noise components reflect to the design.

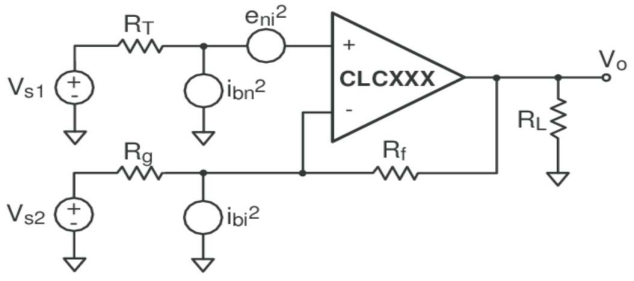

Fig. 1. Components of Current Feedback Amplifier

The equation for the output voltage noise density is [9]:

$$e_{no} = \sqrt{\begin{matrix}(G\cdot e_{ni})^2 + (G\cdot i_{bn}\cdot R_T)^2 + (G\cdot e_{Rt})^2 + ((G-1)e_{R_G})^2 + \\ +e_{Rf}^2 + (i_{bi}\cdot R_F)^2 + (e_{ns1}\cdot G)^2 + (e_{ns2}(G-1))^2\end{matrix}} \qquad (3),$$

where:

- G = 1 + R_F / R_G; G is the gain of the amplifier;
- e_{no} is the voltage noise density seen at Vo (V/√Hz);
- e_{ni} is the non inverting input noise voltage (V/√Hz);
- e_{ns1} and e_{ns2} are voltage noise densities (V/√Hz) produced by V_{S1} and V_{S2};
- e_{Rt}, e_{Rf}, e_{Rg}, are the thermal noises of the resistors R_T, R_F and R_G (V/√Hz);
- i_{bn} and i_{bi} are the amp's input current noises (A/√Hz);

The load resistor (R_L) has a negligible contribution to the noise because the output resistance of the amp is very small. We can remove the second source V_{S2}, and ground the left terminal of R_G in unbalanced design. Also the i_{bn} of the JFET input is in the range of fA (femtoampere), so we can also remove this component from the noise calculations. To lower the noise of the amplifier it is good to use low values for the R_G and R_F.

Nakamichi [10] uses that kind of designs in their reference head playback amplifiers in the Dragon model (released in 1982) and in BX-300E (released in 1984).

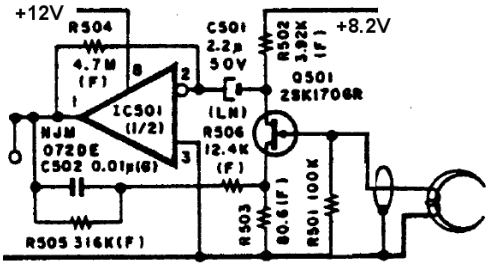

Fig. 2. Nakamichi Dragon playback amplifier

As can be seen from Fig 2 and 3, both designs use significantly high source resistors. The second major problem is the high input capacitance of the JFET. In this paper we use cascode configuration to eliminate the Miller capacitance problems with the JFET, thus allowing direct drive from the audio head.

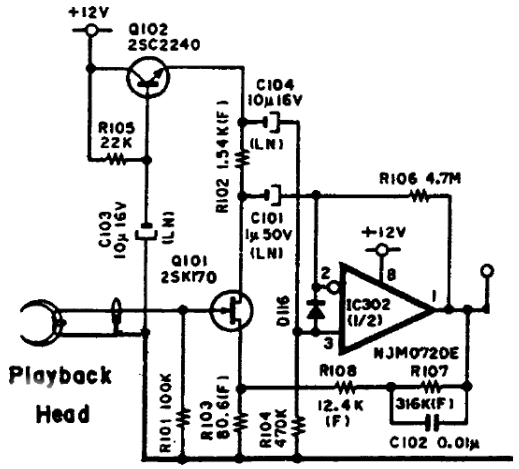

Fig. 3. Nakamichi BX-300E playback amplifier

As can be seen, both designs use direct head connection without coupling capacitor in the input. It is important to lower the noise in the input stage. Also the electrolytic capacitor has third harmonic distortion. A 1μF/63V was tested unbiased and the readings show 0.002% distortion. When soldering, we need to make sure that we don't exceed the maker's recommendations for time and temperature. Likewise, if it's at all possible, never operate an electro at

(or near) its maximum operating temperature, unless we accept the manufacturer's rated life at full operating temperature. For most caps, this ranges from 1,000 to 2,000 hours. That's not very long! In reality, most electrolytic caps exceed their claimed lifetime by a wide margin, even if they are operating at close to the maximum rated temperature. For every 10°C reduction of operating temperature, life approximately doubles, so a 125°C cap operated at 55°C should last for at least 128,000 hours - close to 15 years.

Design on Fig. 3 reduces both negative effects from the first coupling capacitor. The second interesting approach used in the Fig. 3 is the power supply ripple cancellation. The AC ripple from the supply filter (Q102) goes to the pin 3 of the IC302. That reduces the ripples at the output of the amplifier. Similar approach is used in the final design described down.

II. Project Goals and Implementation

The initial research shows some problems on the existing designs. One of the problems was the need of JFET input stage for the high input impedance sources. There is no good enough JFET, so paralleling was a decision to reduce the noise of the JFET.

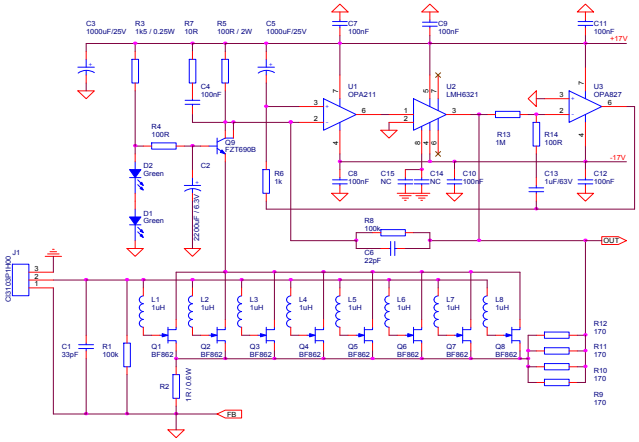

Fig. 4. Test bench of LNA

The test bench is based on the designs on Fig. 2 and 3, also follow the ideas of other low noise projects [1,2,3]. It uses:

- Eight parallel BF862 for the input stage. That approach reduces the equivalent input noise by square root factor of 8. So the equivalent input noise is 0.283nV/√Hz instead of 0.8nV/√Hz for a single transistor. The noise component at the output of the amplifier with gain of 40 is just 11.3nV/√Hz instead of 32nV/√Hz for a single JFET input. Paralleling 8 JFETs increase the input capacitance and the Miller effect.
- High gain BJT (FZT690B) in the cascode configuration to reduce the Miller effect. The collector load resistor of the BJT is only 100Ω, which allows the use of good bipolar SiGe amplifier with relative high input current noise on the second stage instead of precise expensive FET op-amp. We use OPA211 as the buffer amplifier with input voltage noise of 1.1nV/√Hz and current noise of 1.7pA/√Hz. FZT690B has a gain of 400 at 1A collector current. The measured noise of the transistor is 0.6nV at Ic=1mA and 0.38nV at Ic=10mA. Suitable transistor is also FZT849, which measured noise is about 0.5nV/0.21nV (the $r_{bb'}$ is less than 2Ω at 10mA).
- Current feedback design (CFB) with low resistance of the feedback network. This design uses 39Ω to 1Ω, which ensures gain of G=40. This gain is good enough for amplifying the input low signals in the range of 1-4mV. The thermal noise from the 1Ω resistor is just 0.128nV/√Hz and when it is amplified by a factor of *G-1*, it appears as 5nV/√Hz. For example if we use 80Ω as source resistor in the feedback network, the noise component generated by the resistor at the output will be 44.6nV/√Hz.
- High current buffer acts as a follower between the output of the OPA211 and the feedback network. Feedback network cannot be connected directly to the output of the OPA211 because of its current limit. The buffer is LMH6321 and has ability to supply ±300mA. This unity gain buffer has a voltage noise density of 2.8nV/√Hz and current input noise of 2.4pA/√Hz. The current noise is not important at all, because the buffer is connected to the low output impedance of the OPA211. The slew rate of the buffer is about 210 V/µS at 50Ω load.
- Power supply ripples cancellation circuit on pin 3 of U1. Even an extremely quiet power supply will still have something like 8nV/√Hz to 10nV/√Hz noise; under these circumstances, even with a local RC filter, achieving 0.3nV/√Hz is impossible (at least because a large electrolytic still has hundreds of milliohm impedance, not low enough to short the power supply noise voltage, usually with a much lower output impedance). By referring both op-amp inputs (in AC) to the positive power supply rail, the power supply noise is now appearing on the op-amp common mode, being therefore rejected through the op-amp CMRR. The overall head amp PSRR is down to better than -50dB.
- An inverting servo, built around an OPA827 JFET input op-amp is taking care of setting the OPA211 op-amp common mode voltage, so that the output offset is cancelled. That way the design removes all coupling signal capacitors.

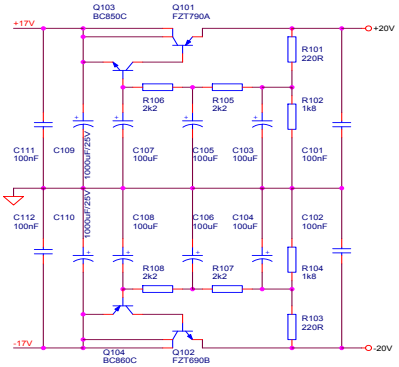

Fig. 5. Power Supply Filter

- The power supply noise has to be filtered out. A standard emitter follower power buffer (capacitance multiplier) does a pretty good job, however there's one thing that it can't filter out: the emitter follower $r_{bb'}$. To avoid that contribution, we need some sort of local feedback loop, to obtain a significant lower equivalent $r_{bb'}$. This is easily achieved by using an Sziklai configuration for the emitter follower. By including the power device in a

current feedback loop, its $r_{bb'}$ is effectively cancelled. It's now the low power device (which can be a low noise device) that dictates the equivalent $r_{bb'}$ of the emitter follower. The $r_{bb'}$ of BC550C/560C and BC850C/860C is about 150Ω so it is better to use BC817/807-40 or 2SC3324/2SA1312 even ZXTN2018F/ZXTP2027F ($r_{bb'}$ =3.3 Ω). It is only the Q103 and Q104 $r_{bb'}$ (Fig. 5) that contributes to the power supply noise. Divided by the head amp PSRR, this contribution is negligible.

III. PCB Design and Prototyping the LNA

Design was made on double-sided PCB using ground planes on both layers. Ground planes are connected to the shield ground. The base material is FR4 with thickness about 1.55mm. The copper thickness is 55µm. The standard copper thickness is 35µm but it is very important to have low resistance tracks around the feedback network because of the low resistance of the feedback network.

Most of the components are SMD. Wirewound resistors are the best choice for noise, followed by metal film, metal oxide, carbon film, and lastly, carbon composition. However, wirewound resistors are not readily available in large resistance values, and are usually inductive, which can cause instability problems in some cases. Many people prefer the "sound" of carbon comps, claiming they sound warmer than film or wirewound types. This is possibly due to distortions generated by the modulation of the contact noise current by the AC signal. Since this noise has a 1/f frequency characteristic (similar to pink noise), it is more pleasing to the ear than white noise. However, pleasing noise is still noise, and in my opinion, it should be reduced to the lowest possible level. The signal distortion is a different topic altogether. The electrolytic capacitors are based on the Panasonic FC Series Aluminum (105°C Low ESR) Electrolytic Capacitors. Some of them are SMD but the large capacitances are TH radial. The critical capacitors (C2, C5) are shielded with local metal folio cap, which is connected to the shield ground.

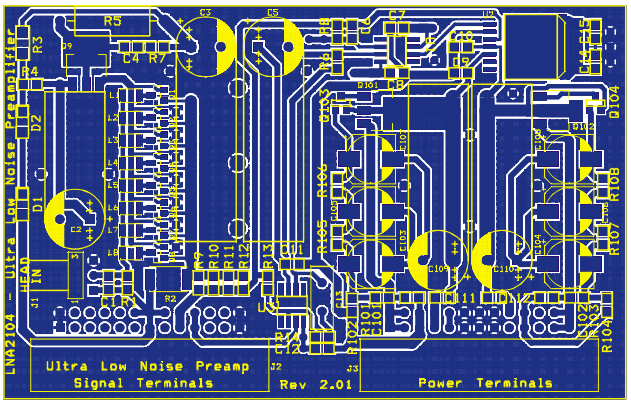

Fig. 6. Top layer of the LNA

Routing of the board is very critical for the good final results. One urgent thing is to avoid the current loops. The JFETs are placed close each other. A shielding copper plane is placed on the bottom side of the board. The design implements tree different grounds. One is the shield ground plane on the top and bottom layer. Both shield grounds are connected together but are not connected to the signal and power ground. Power ground comes from the power supply connector and first it reaches the filter capacitors C109-C110. Common net from the capacitors is used as reference signal ground and is connected to the ground pin of the feedback resistor R2. The ground pin of the input signal is connected also to the R2. Ground pin of the R2 acts as a reference pint to the analog ground. The track that connects the source terminals of the JFETs is placed on the top layer. For this track it is important to be as short as possible, also to be with enough width to avoid voltage difference on the source terminals of the transistors. This track is shielded on the bottom layer.

IV. Conclusion

The corner frequency of this low noise amplifier is remarkably low. This is another proof that BF862 is an excellent low noise JFET. The corner frequency is about 15Hz. The self-noise is around 4nV/√Hz at 10Hz and 1nV/√Hz at 40Hz. The level of harmonic noise (50Hz plus odd harmonics) is very low. This is a direct result of a compact SMD construction. The measured slew rate is about 40V/uS. The preamplifier was designed to operate at output level of 100mV RMS. The test shows significant overload ability. The output goes linear without clipping up to 6Vpp. The preamplifier is suitable both for high and low impedance sources because of its low input noise level (0.3nV/√Hz at 1kHz), which is better than most of the BJT.

This low noise amplifier will be used as a head preamplifier for a reference tape reproducer, which development was started at the end of 2015. Also this preamplifier will be used in the first stage of custom-made laboratory signal to noise meter [11]. Adding precise a-weighted filter to the output will be the next task in the project.

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Special Postdetermination of Logical Functions: Optimization "Balar" Procedure in Sequential Syntesis

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Abstract – In this article a problem of special postdetermination of excitation functions of triggers with two logic inputs is presented. BALAR theorem is formulated. A place in sequential synthesis is showed. Reduction of two in one logic inputs is proved.

Keywords – **sequential synthesis, special postdetermination, Balar theorem, dual input triggers, programmable logic matrix type of media.**

I. INTRODUCTION

In the theory and practice of logical design, one can hardly find something better developed and more common than the formal descriptions of the basis types of elementary automata, i. e. D-, T-, RS-, JK- triggers and their application in fundamental procedures of synthesis and analysis of synchronous sequential circuits (SC). In the course of more than 30 years [5-18] the theoretical foundation and applied aspects of this issue have stayed, in my opinion amazing invariant. Hence the steady professional stereotype that everything related to the topic has already been completely and finally settled.

A. Special Postdetermination of Exitation Functions of Dual Input Triggers

The special postdetermination of incompletely determined logical functions (LF) as a new methodology and algorithmic technology in combination synthesis [3,2,1] may successfully be applied to the excitation functions of triggers in the synthesis of a particular SC. Among the different cases of special postdetermination, priority is given to those in which double implicative relation of equivalence (equality and counter equality) because of the reduced number of LF to be performed. It can be assumed that this ranging criterion is valid for any kind of elements at microarchitectural level – from a random primary ones (AND, OR, NAND, NOR, XOR) to the indisputably established regular programmable environment (logical matrixes and ROM) in their varieties.

The special postdetermination of the LF, in terms of methodology, brings about the idea of a principally new approach in sequential synthesis, i. e. special postdetrmination should be applied to the actual automata descriptions, and particularly the basic matrices at the input of the triggers with two inputs (RS and JK), whish contain definitive indeterminacy due to the existence of doubled jumps. Special postdetermination in this case is applied prior to the standard procedure of SC synthesis, i. e. to put it figuratively, "on a genetic level". The aim is to obtain specially postdetermined (reduced) triggers, in which for the couple of excitation functions in the coded table of jumps of a random SC there always exists, unconditionally and without any further processing, a double implicative relation of equivalence (equality and counterequality). In other words, any such preliminarily postdetermined trigger with two logical inputs will always be controlled by a single excitation function.

Nature of the research problem is formulated in the following principal "BALAR" theorem: In any sequential circuits (finite automata), synthesized with dual input triggers (RS, JK), each of them always and unconditionally can be operated with a single excitation function.

The proof of the theorem using analytical definitive forms of excitation functions of dual input triggers. Consequences of proven theorem can be summarized:

Consequence 1.

In the synthesis of arbitrary SC special postdetrmination of excitation functions of dual input triggers reduces always and unconditionally trigger type RS in trigger type D and trigger type JK - in trigger type D or T.

Consequence 2.

Well-known elementary transformations trigger type RS in trigger type D and trigger type YK in type D or T, used alone and regardless of the procedure for the synthesis of SC cases are part of the proven theorem. Reductions under investigation 1 apparently reduced twice the number of required excitation functions management features dual input triggers. In the implementation of SC in random matrix structures leads unconditionally to twice cut the number of control lines to logic inputs of the triggers.

I believe that the results of this study can be regarded as certain contributions to the theory of sequential synthesis and used as a practical approach for optimal realization of any finite automaton. As the name of the proven theorem and of the algorithmic procedure I suggest abbreviation BALAR /**B**asic **AL**gorithm for **A**utomata **R**eductions/.

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B. Balar Procedure in the Methodology of Sequential Sinthesis

I will try to present in an illustrative form my vision on the place and influence of the described researches to the methodology and technology of sequential synthesis. In my opinion there is an interesting and non-trivial analogy between the role and importance of the BALAR theorem in sequential synthesis and the role and importance of the theorem of De Morgan in combinatorial synthesis.

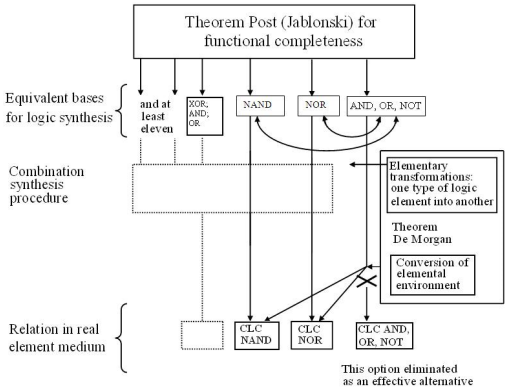

Figure 1. Combination synthesis

Well-known fundamental De Morgan theorem has at least two important applications in combinatorial synthesis.

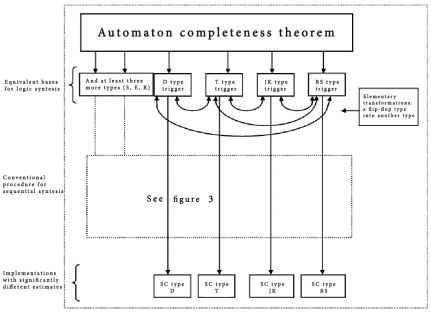

Figure 2. Conventional sequential synthesis

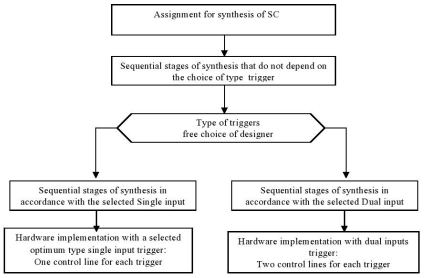

Figure 3. Conventional sequential synthesis

Alphabetical known elementary transformations of one type of trigger to another are carried out separately and fully independent from the conventional procedure for sequential synthesis. In the course of this procedure previously selected type triggers in any way can not be changed. As a result of synthesized SC receive specific circuit implementations for each of the main types of triggers with significantly different estimates.

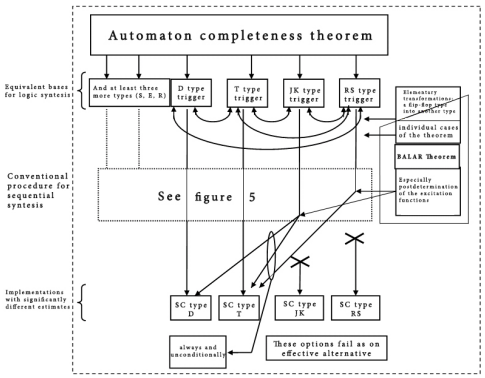

Figure 4. BALAR procedure in sequential synthesis

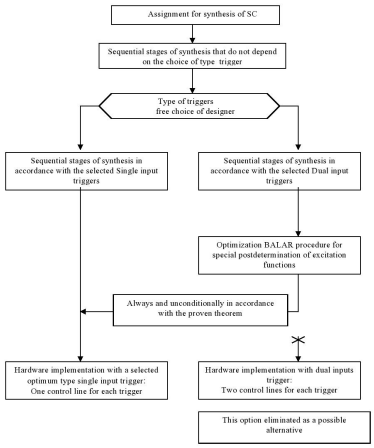

Figure 5. BALAR procedure in sequential synthesis

If the designer decide and implement optimization BALAR procedure for special postdetermination, he always unconditionally and completely independent of their wishes and preferences will reach the same decision - triggers two logic inputs to manage with only one excitation function. As a result of synthesizing the SC will always receive circuit implementations for both types single input triggers, which ensure optimum conversion in a matrix medium.

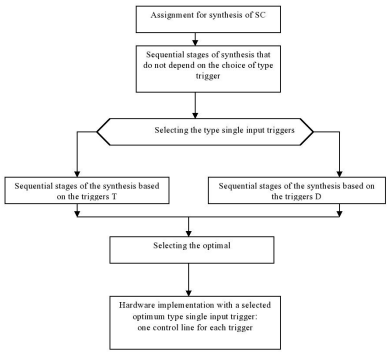

Figure 6. Prospects in sequential synthesis

According proven BALAR theorem dual input triggers in any SC always and unconditionally can be reduced in single input triggers. My view is that due to this dual input triggers eliminated as an effective alternative procedure for sequential synthesis and in this context are unnecessary. I believe that such an approach fully meets the foreseeable

realities and perspectives in computer electronics and microarchitecture, which undoubtedly prevail programmable logic matrix-type environments.

II. CONCLUSION

The article defined the problem of special postdetermination of excitation functions of triggers two logic inputs as possible optimization in the synthesis of arbitrary sequential scheme. Brought the main performances and results of the analytical test which has been shown that in each sequential scheme with arbitrary function transitions each flip-flop with two logic inputs /RS, JK/ can always and unconditionally to manage only a single excitation function. At regular programmable logic matrix type of media /ROM, PLA, PAL/ this leads to optimal conversion result of halving the number of functional lines, which manage the logic inputs of flip-flops. Illustrated is the author's view on the role and place of proven BALAR theorem and the eponymous optimization procedure in the theory and practice of contemporary sequential synthesis.

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Integration of the European Bachelor Master Degree Concept at Belarusian Universities for Physics and Engineering Students

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Abstract – **In order to facilitate the introduction of the bachelor master degree concept at Belarusian universities, courses and teaching materials are developed for master-level programs in physical sciences. A demo-course on "applied physics", including Electromagnetic Compatibility and System Theory, introduces a powerful learning environment by using a digital learning platform like Blackboard® or Moodle.**

Keywords – **bachelor master degree concept, Belarusian universities, learning environment, Electromagnetic Compatibility.**

I. Introduction

The Erasmus+ project "Improvement of master-level education in the field of physical sciences in Belarusian universities" is an educational collaboration between three European Union universities (Riga Technical University (RTU), University of Cyprus, KU Leuven), four Belarusian universities (Belarusian State University (BSU), Grodno State University (GrSU), Gomel State University (GSU), Belarusian State Technological University (BSTU)), the Ministry of Education of Belarus and two industrial partners. The project aims to improve the relevance of master degree programs in the field of physics in Belarusian universities.

The Bologna Process, designed to ensure comparability in the standards of higher education qualifications, has led to the European bachelor master degree concept [1]. The overall vision of this concept focuses on a student-oriented and interactive approach combining different new teaching and learning methods [2]. Digital teaching and learning, based on the latest ICT technology, is one of the crucial elements of the concept. As a consequence, most European Union universities have implemented a digital learning environment. The Bologna Process also attracts considerable attention outside the European Union. The Bologna Process Ministerial Conference in 2015 in Yerevan (Armenia), i.e. in a country outside the European Union, indicates the interest of non-European countries [3].

The integration of this European bachelor master degree concept at the Belarusian universities includes a transition from the educational 5 plus 1 system to the 4 plus 2 system. The bachelor program reduces from 5 to 4 years implying a challenge to prepare the graduated bachelors for the labor market in a shorter period of time. The master program increases from 1 to 2 years implying the need for new up-to-date course material. An increase of the number of master students is expected and a larger part of these master students must be prepared for the industry i.e. not only to realize a PhD. It is important to comply with the European Credit Transfer and Accumulation System (ECTS).

This modernization of the physics and engineering educational programs requires a sustainable implementation of innovative ICT based teaching and learning methods. This challenge requires the development and the integration of scientifically based digital didactics focusing on the strategies to plan, realize and evaluate a powerful learning environment and learning practices via e-learning [4]. The approach of this digital didactics differs fundamentally from the conventional instructor-centered model. E-learning fits well with the notion that learning is an active process of constructing knowledge and that instruction is the process by which this knowledge construction is supported [5]. As a consequence, there is also a need to develop training programs for the teachers who face a substantially changed role [6].

In order to obtain an integrated instructional design framework providing a flipped classroom for the physics and engineering students at the Belarusian universities, a number of objectives have been formulated. A demo-course on "Applied Physics" in the digital learning commercial platform Blackboard® or open source platform Moodle is needed. The development of an electronic library (containing didactic materials) for teachers and the development of a virtual laboratory for distance experimentations similar with [7] is useful.

II. Improving the Master Level Education

Updating courses and teaching materials for the master programs in physical sciences in the fields of Functional Nanomaterials and Photonics forms the keystone of the Erasmus+ project. European Union and Belarusian universities collaborate to develop e-books on: "functional nanomaterials", "photonics", "guidelines on master thesis", "applied informatics" and "applied physics". The present paper will mainly focus on the course on applied physics and its integration in a digital learning environment.

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The Erasmus+ project also aims to realize Belarusian teacher and student mobility to the participating European Union universities. It is an objective to improve the teachers' qualifications and skills by introducing up-to-date ICT teaching technology and improving English language skills. Improving the students' ICT skills, English language skills and teach physical sciences is a related goal.

The course on "applied physics" is a demo-course to all participants (teachers and students) by introducing a learning environment using a digital learning environment.

III. Model of a learning environment

A powerful learning environment consists of different components determining the teaching practice. Figure 1 presents a didactic model [8] which indicates the interrelationship between the learning processes, the learning outcomes, the student characteristics and the required assessments.

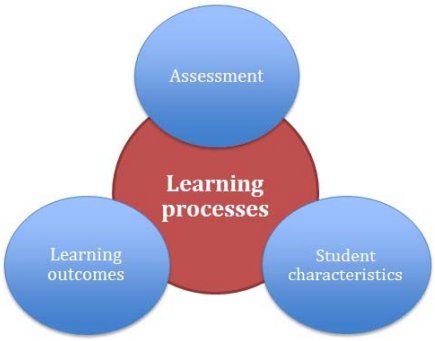

Fig. 1. Components of the learning environment

A. Learning outcomes

"The learning outcomes are narrow statements that describe what students are expected to know and be able to perform by the time of graduation. These relate to skills, knowledge and behaviors that students acquire in their matriculation through the program." [9]. The learning outcomes are important for the teacher(s) when taking decisions on the design of the learning environment. Aware of the knowledge, attitudes and skills to be reached, the students are also able to manage their learning activities.

Since the learning outcomes are the basis for the design of the learning environment, they will determine the role of the ICT technology. Even though this ICT technology is important in e-learning, it can never be a goal in itself i.e. it is a tool. The ICT technology can facilitate a clear and transparent communication on the learning outcomes and, even more, it can optimize the follow-up of the learning process. Fast and with ease, the teacher can check up if the students pursue their objectives in an efficient way.

B. Student characteristics

As actors in the learning environment, the students are responsible for their own learning. There are several student characteristics [10], amongst them: prior knowledge, learning level, motivation and interests.

The learning outcomes have to be adapted to the prior knowledge of the students, as this determines strongly which new information the student can process in an active and systematic way. Therefore, it is important to activate the prior knowledge during the learning process allowing the student to build upon this knowledge [11]. In e-learning, the prior knowledge may relate both to the course subject and to the ICT field.

It is also necessary to offer teaching matter that is in line with the learning level of the student. A balance between the concretization and the abstraction of the teaching matter must be found.

Furthermore, the learning should fit with the needs and requirements of the student to nourish his motivation. The nature of this motivation can be intrinsic as well as extrinsic. In the first case, the will to learn lies with the student himself and in the teaching matter while it lies outside the student and outside the teaching matter in case of an extrinsic motivation.

C. Assessment

The assessment includes the determination and the evaluation of the result of the learning process i.e. the achievement of the learning outcomes. The evaluation methods, having sufficient variation, must be consistent with the didactic methods and the learning activities. In practice, the assessment plays a crucial role since students adjust their learning activities to the assessment [12].

There are many aspects involved in the assessment, such as: moment, type, objective, evaluator, previous feedback. The moment of the assessment will trigger or support the learning activities. There are two main types of assessment. A process evaluation focuses on the learning processes. The teacher examines to what extent and in which way the student acquired outcomes through the learning process. Using a product evaluation, the teacher evaluates the acquired learning outcomes of the student based on the results of the learning process.

Much depends on the objective of the assessment. A formative evaluation focuses on the progress of the learning processes. This intermediate evaluation, not taken into account in the final evaluation, provides feedback to encourage and guide the student where necessary [13]. In contrast, a summative evaluation is aimed to pronounce a final assessment.

Several evaluators are involved in the evaluation process. As a consequence, this process obtains a more diverse character. Besides the teaching team, potential evaluators are: externals from the professional field, fellow students ('peer assessment'), the student himself ('self-assessment').

The assessment is closely linked to feedback (see formative evaluation). A digital learning environment gives the teacher the opportunity to follow up the student independent of location and time. The integration of automatic and individual feedback is possible. This feedback can be supplemented with learning tips and references to interesting learning materials.

D. Learning process

Learning in a powerful learning environment is an active process. Several components influence the learning process

of the student: subject contents, learning activities, student support.

Due to the exponential growth of knowledge, an inexhaustible supply of subject content is available. This implies the teacher has to make well-informed choices. The ICT technology allows subject contents to be more dynamic, responding to the need of actualization and optimization. Digital contents can be adapted easily. Digital content can be stored for long periods of time implying they can be re-used. This means an added value for the lifelong learning which is considered as the central learning paradigm for the future [14].

Several kinds of learning activities are possible. In a student-oriented approach, a major function of the teacher is the support of the students carrying out the learning activities. This support can be very different [15]. For solving a complex task in a computer-based learning environment, for instance, support can be directed towards the content of the task, the strategies for solving a problem or the handling of the technology of the environment. The way and the extent to which support considers the specific needs of the individual student, can also vary during the learning process itself.

IV. Demo-course "applied physics"

A. Learning content

An extensive survey has been implemented to prepare the elaboration of the learning content and the didactic approach. Taking into account that the Ministry of Education of Belarus has set the task for Belarusian universities to reform their curricula for the majority of specialties in order to make a transition from the existing 5 plus 1 training system to the 4 plus 2 training system, the project team arranged a survey aiming to understand the needs of potential employers. Therefore, the main target of the survey was to identify the training requirements of practice-oriented masterships for the planned 4 plus 2 system and to provide an input to new two-years master level training programs "applied physics" and other training programs in the project.

The demo-course "applied physics" is a collaboration of five universities i.e. BSU (including the Scientific Research Institute of Nuclear Problems), GrSU, GSU, RTU and KU Leuven. The course illustrates the broad applicability of physics by dealing with electricity and magnetism, electrical engineering, modern measuring techniques (e.g. including diffraction methods, electron microscopy, magnetometry), Electromagnetic Compatibility and system theory.

Electromagnetic Compatibility deals with conducted and radiated emission and immunity issues. System theory, including the use of MATLAB®, provides the scientific foundation to design EMC filters. Theoretical course material, exercises, "self-evaluation" questionnaires and laboratory demonstrations [16] are combined.

B. Didactic approach

E-learning platforms are especially useful when teaching "physics". Some authors state that computational "physics", based on a scientific problem-solving paradigm, provides a more flexible and efficient education than a traditional 'physics' course [17].

A type of blended learning increasing opportunities for implementing this paradigm is the flipped or inverted classroom. This educational technique has two parts: interactive group learning activities inside the classroom and computer technology-based independent activities outside the classroom [18].

To develop an integrated instructional design framework providing a flipped classroom for the physics and engineering students at the Belarusian universities, a demo-course has been designed in the digital learning environment 'Blackboard®', integrating principles also useful in 'Moodle'. Workshops will be organized to train the Belarusian teaching staff in the methodical and didactic use of a digital learning environment. The emphasis lies on a student-oriented approach where the students interact with the fellow students, their teachers and the subject contents.

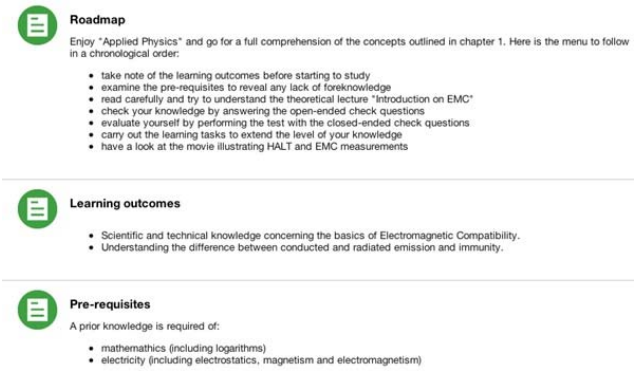

Fig. 2. First three elements of the introductory chapter on EMC

The toolbar of the demo-course "Applied Physics" contains six buttons: Announcements, Information, Contacts, Documents, Tools, Master Thesis. While the buttons "Information" and "Contacts" contain rather general information about the course and teachers, the student enters the actual virtual workplace using the button "Documents". In the present example, this component of the course is divided into nine chapters.

Each chapter is subdivided into a fixed number of elements: Roadmap, Learning outcomes, Pre-requisites, Theoretical Lecture, Self-evaluation, Learning tasks. The "Roadmap" explains the menu to be followed by the student. The learning outcomes and the required prior knowledge of the student are also given. Figure 2 shows the first three elements of an introductory chapter on Electromagnetic Compatibility.

In the element "Theoretical lecture", the student finds a document containing the theory he has to understand and process. This document can be illustrated by a set of objects like: videos, MP3's, scanned images, links to websites, animations,… The latter object allows to show dynamically many physical situations and concepts that are often difficult to apprehend by the students.

Having studied the theoretical lecture, the students can carry out a "self-evaluation". To develop this element, different tools of the Blackboard®-platform are used: questionnaires, quizzes, discussion forums, blogs, chats. Figure 3 shows the self-evaluation element of this introductory chapter on EMC. The self-evaluation is

twofold. The student can check his constructed knowledge by answering a sequence of open-ended questions. Finally, the student can evaluate himself by performing a test with closed-ended check questions.

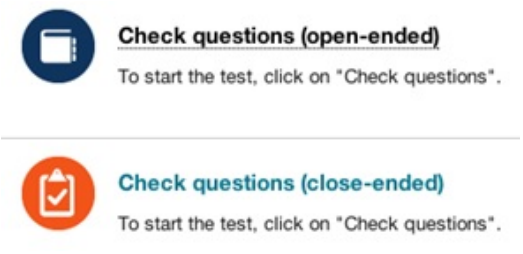

Fig. 3. Self-evaluation of the introductory chapter on EMC

Specific attention is devoted to the indispensable support of the student. In both cases of the "self-evaluation" element, automatic feedback is provided allowing the student to estimate his level of progress. Furthermore, an interesting possibility of the digital learning environment is to send personal messages to users within this platform. The student can ask questions to his teachers in order to clarify specific aspects of the theory or the exercises. The student feels more confident if he knows that his teachers will answer his doubts and questions personally and private.

In the last element "learning tasks", the student can extend his knowledge by carrying out some learning activities. The learning tasks are authentic and outlined in a meaningful context. This means they occur in a real-life or professional situation. Based on papers available in literature (e.g. [19]) in combination with questionnaires, the master degree students get familiar with the scientific literature (journal and conference publications) and organizations like IET or IEEE.

V. Conclusions and Acknowledgement

By integrating the bachelor master degree concept at Belarusian universities for physics and engineering students, the present work contributes to a unification of educational systems of the European Union and Belarus. Stimulating the use of English as teaching and research language is a challenge which facilitates the use of digital learning platforms in order to realize collaborations between professors and students at universities in the European Union and Belarus. In a next step, realizing mobility of professors and students between Belarus and the European Union will further enforce the educational collaboration.

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Survey on Collaborative Learning Practices

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Abstract – **The paper discusses the experience in promoting knowledge work practices in secondary and university education. The results of conducted pilots with analysis of students' reflections are considered for several cases at different educational levels. Design patterns to capture pedagogical solutions which seem to successfully address challenges faced are also presented.**

Keywords – **Collaborative learning, Knowledge creation, Cloud technologies, Education in electronics**

I. Introduction

Knowledge has always been a factor of production, and a driver of economic and social development. A current challenge for education is to prepare learners for the emergent knowledge society through appropriate pedagogical practices that promote competencies for sharing, creating and working with knowledge and knowledge artefacts in an innovative way.

Thrialogical approach [1] builds on the assumption that learning is not only individual knowledge acquisition or adoption of existing social and professional practices, but also the creation of new knowledge and practices in collaboration with others. A set of design principles [2] was developed to guide the implementation of the trialogical approach to learning in educational settings as follows:

DP1 – Organising activities around shared objects

DP2 – Supporting integration of personal and collective agency and work (through developing shared objects)

DP3 – Fostering long-term processes of knowledge advancement with shared objects (artefacts and practices)

DP4 – Emphasising development and creativity on shared objects through transformations and reflection

DP5 – Promoting cross-fertilization of various knowledge practices and artefacts across communities and institutions

DP6 – Providing flexible tools for developing artefacts and practices

The trialogical design principles served several purposes, especially to provide a concrete starting point for pedagogical development and also as a framework for analysis and reporting findings but also for choice and use of technology. How these design principles are applied in transforming courses from traditional face to face learning towards practices that expose students to collaborative knowledge creation supported by digital technology is reported in [3, 4, 5].

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This paper summarises the experience in promoting collaborative learning at the TU-Sofia and the Technology School "Electronic Systems" with special focus on the students' self-reflections of knowledge work practices related to the modified and implemented courses.

II. Collaborative Knowledge Practices Questionnaire

The Collaborative Knowledge Practices Questionnaire (CKP) was developed within the KNORK project [6] for measuring generic competences related to collaboration, knowledge creation and use of digital technology. It is based on the trialogical approach and its design principles and aims at collecting students' evaluations of knowledge practices and associated competences important for life. The aim is to evaluate students' self-assessed competence-development during courses by using Likert scales ranging from 1 (strongly disagree) to 5 (strongly agree) to the next seven statements:

1. Learning to collaborate on shared objects (relates to DP1).
2. Integrating individual and collaborative working (relates to DP2).
3. Development through feedback (relates to DP3 & DP4).
4. Persistent development of knowledge-objects (relates to DP4).
5. Understanding various disciplines and practices (relates to DP5).
6. Interdisciplinary collaboration and communication (relates to DP5).
7. Learning to exploit technology (relates to DP6).

The CKP questionnaire also includes open questions asking what has been positive or impressive in the course, what has been challenging or disturbing in the course and other comments.

The following section provides example cases with results from the CKP questionnaire used in university and secondary education. The cases have targeted students and course participants on different educational levels – high secondary school, bachelor and master university degree. The attention is drawn specifically to the collaborative aspects of learning purposefully aiming at creating or developing shared artefacts and especially those making use of digital technologies.

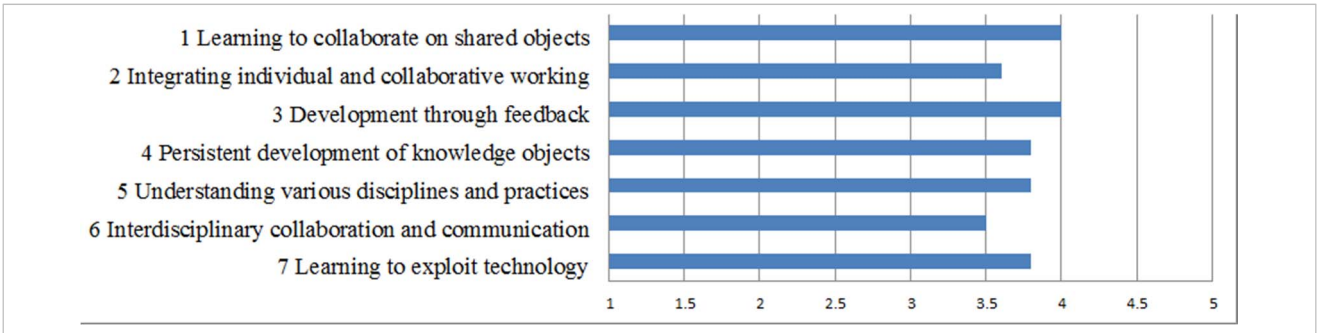

Figure 1. CKP-questionnaire results from the Semiconductor Devices course

III. Finding from Example Cases

A. Semiconductor Devices

This is a basic compulsory course for the second year bachelor students in the field of Electronics, Computer Technologies, Telecommunications and Automatics. The goal is students to obtain knowledge on principle of basic semiconductors devices under diverse operating conditions, to can design and analysis simple circuits with them, to calculate their important parameters, and to use devices in solving engineering problems.

The course was restructured to introduce collaborative team work on shared report with using cloud computing technologies, up-to-date communication tools for student-teacher connection, continuous monitoring and assistance of students' activities. Since these students are at their 3rd semester of study and haven't any engineering background for preparing the semester long project, we decided to give students opportunity to work collaboratively in groups with clear role of each participant within several two-week cycles for practical training, collectively preparing shared report including measured data.

Students work in teams of 2-3 persons on common report, which includes shared design & analysis tasks – circuit design, parameter calculation, simulation, as well as measured data and their interpretations. All participants had to register individual Google accounts. The completed document on the long-term group work is created in Google Drive as a shared document with the possibility of collaboration between the team members and the teacher. For inter team communications students can choose their preferred tools (chat, conferences, e-mail, forums). For student-teacher communications are used Google applications: Gmail, Calendar, Drive и Google+.

At the end of the course, the CKP questionnaire was used to ask the students how they had learned collaboration and knowledge work practices during the course. The data were collected using an online form after the course. Figure 1 presents results of the CKP-questionnaire as scales (sum variables) regarding the parts concerning what students experienced that they had learned.

For the students in this course it was their first attempt to work in teams. As can be seen from the figure they give high score on their experience to collaborate on shared objects, which they consider challenging and useful to understand the benefits of collaborative working. Students commented that have understood how important is the expertise and commitment of others in development of common products, but have some problems in integrating individual and collaborative working. Especially challenging, according to the students, has been to organize and coordinate collaboration with other course participants. A recurring issue which has annoyed course participants is team members who have seemed to lack interest in the subject and slowed down the whole group.

The positive aspects identified from students are mainly related to the possibility to study in an innovative and engaging way at any time at any place and to have at the same time immediate support from teachers by receiving timely feedback and help. This is especially pointed not only from the score observed in figure, but in open questions as well. Learning to exploit technology, innovative way of working in teams using up-to-date cloud computer technologies were appreciated. The lowest score is on interdisciplinary collaboration, because this course is the first basic engineering and the shared objects do not need intensive communication with other subjects to fulfil the common tasks.

B. Digital IC Design

This is compulsory course of bachelor degree 4th year students. The goal is student to learn core curriculum as they work on the 3 months long project, to go through all stages of the design cycle, and to acquire skills in teamwork and creating common shared documents, which is continuously monitored, taking into account the individual contribution of each team member. Working in small teams, the students are required to design a digital Application Specific Integrated Circuit (ASIC).

The design workflow is based on HDL (Hardware Design Language) modelling, verification and synthesis. The main design artefacts (VHDL models and test-benches) are text files; therefore we are able to borrow many tools and workflows from the software development community. Projects are hosted on GitHub – one repository per project. In parallel with the code development, the teams are required to create and maintain a Google Docs document which is one of the major deliverables. Initially the document contains the technical specifications of the design. Later on, the students have to add description of the implemented algorithms and architectures, argumentation of the trade-offs made and the results from the simulation, synthesis and physical design.

Student works in teams of 2-3 persons in continuous 3 months long shared common project with iterative design

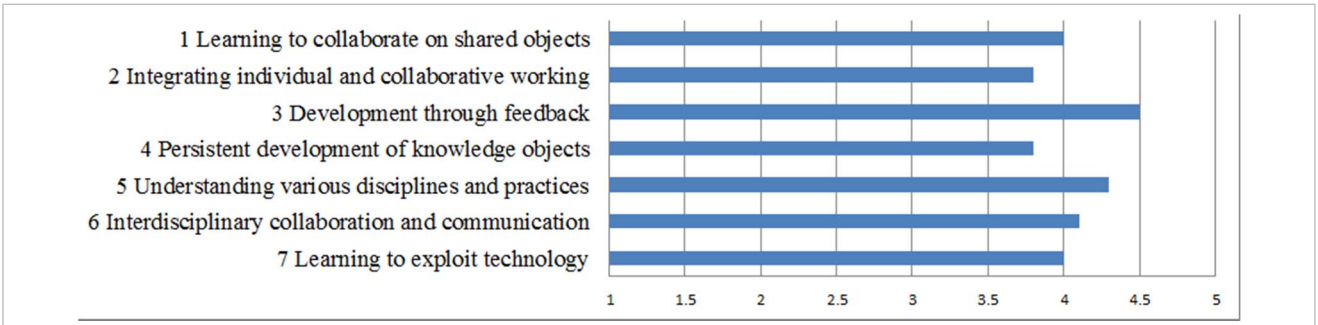

Figure 2 CKP-questionnaire results from the Digital IC Design course

process to improve circuit performance in order to fulfil technical specifications. Team members have a collaborator rights for the respective repositories, but they were asked not to commit directly. Each change had to be peer reviewed before it can be committed to the project repository.

The students perform planning, sharing the drafts, getting feedback from the teacher and other students, improving the project and project report, submitting relevant documents. They use forums and blogs for discussing problems and exchanging views and opinions. Google Tools are used for collaborative development of a common shared object in the cloud – Google Drive, Docs, Sheets; Google calendar – to set deadlines and to monitor progress – assignments, intermediate stages reporting, deadline for submission of project. Most of development takes place outside the regular classes. For their intra-team communication, the students are free to choose whatever tools they prefer (chat, conferencing, email). For student - teacher communications we decide to use the Google tools.

The results in Figure 2 shows that the course practices had a strong emphasis on collaboration on shared object (challenging common interdisciplinary engineering project), and the students reported having especially learned to understand various disciplines and practices why working on the project. Students have expressed appreciation of learning new things, developing teamwork competence and using new technological platforms for teamwork.

The design task provided students with a "real world" shared object to be worked on with external experts from industry, applying practices commonly used in the companies. In such situation development with timely obtained feedback from teachers and professionals is very important and it is appreciated by students, giving the highest score in this scale. By integrating technology into learning experiences, students are more engaged in their learning inside and outside of university and get an opportunity to collaborate productively and to communicate using technology, which is indicated on the graphic. Students benefit by learning this way together subject-matter knowledge with a better understanding and confidence to use cloud platform for their own professional career plans. Digital technology also allows teachers to keep track of students' progress all the time creating unprecedented opportunities for personalized learning.

C. CAD in Electronics

The CAD in Electronics course in the Technology School "Electronic Systems" was re-designed to be project oriented. All group activities are organized around shared objects – collaboratively development of common project, and preparation of shared report.

Working in teams of 2 persons, the students are required to design and simulate digital and analog circuits. During the long term projects teams have to gather information, discuss the given problem in collaborative environment, analyse and simulate the digital or analog circuit using dedicated CAD software – Cadence Orcad Capture and Pspice. For the collaborative project development the environment consists of public cloud based services, which makes the participation of each member independently of the others in any place and at any time – Google Drive, Google Docs, Google Sheets, Google calendar.

The pilot course using collaboratively development of shared project has been conducted with two 11 grade classes (17 year's old school students) within 15 weeks.

After the course the participants were asked several questions to evaluate students' self-reflections concerning knowledge work practices related to their experiences in the implemented CAD course, to observe their progress and what they had learned. The results of the CKP-questionnaire are summarised in Figure 3.

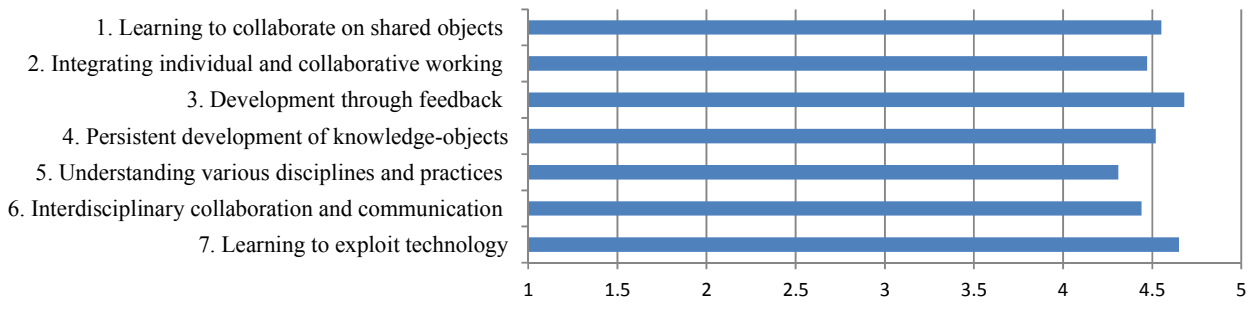

Figure 3. CKP-questionnaire results from the CAD in Electronics course

IV. Design Patterns

Another way to analyse and describe the cases has been to construct educational design patterns from the cases. The educational problems are namely often typical and the same problems show up in various educational settings and contexts. The idea of educational design patterns is to capture pedagogical solutions which seem to successfully address challenges. Design patterns are a structured way of collecting solutions that address recurrent problems. They can help to learn from the many creative and innovative ideas generated by students and teachers in the different cases and to see how these ideas can be used constructively in other contexts facing similar educational problems.

Educational Design Pattern – Synchronization of Course Activities with Many Teachers and Students

When a course is a basic compulsory course for several faculties, many teachers and huge amount of students are involved in course activities. When a course comprises of several scheduled activities, it need to be carried out within a pre-defined period. If some of the group supervisors are not regularly teachers, but external experts, they are not always well-informed about the different phases and activities of a course. This creates difficulties in tasks distribution, monitoring and students' work feedback. It the supervision is not adapted to course activities including the timing of tasks distribution and feedback, this may disturb and delay the students' work. The same problem arises if some students do not follow scheduled tasks on time. This could spoil the quality of the team work.

As a solution of this educational problem the Google Calendar may be used from leading lecturer to create a plan of course activities within the whole semester. It is shared with all course participants and need to be strictly scheduled by both teachers and students.

This practice could be applied in courses, which involve interaction between students and supervising teachers over time, especially supervisors who are external to the course in order to synchronize several activities with many players in the process.

Educational Design Pattern – Continuous Student-Teacher Communication Embedded in a Developed Document

Ongoing monitoring of the learners' progress, the need to check regularly their reports, to give them feedback and to correct wrong decisions with ideas how they to continue requires huge amount of time from lecturer especially in cases with many students and external experts. The problem arises because students don't work regularly in time and the teachers need to check reports several times to observe students' questions so to provide them a feedback on time. The situation becomes more difficult with external teachers or industry experts, which are not strongly involved in the process. This issue requires a solution, which allows teachers to be informed promptly that some student need help so to give feedback and answer in time to given context, particularly to the posed question, without need to read the whole shared report.

As a solution of this educational problem we are proposing a workflow, based on questions and answers embedded in the project report and automatically generated email notifications.

Prerequisites

- The professors and students have Google accounts
- Google Docs is used for collaborative project report authoring

It's important to note that the professor should remain the owner of the shared document. Also, in order to guarantee reasonable access control, the document should be shared with Gmail accounts only.

Questions and answers

- When a student need, he/she opens the shared document and adds a comment. The comment should be attached to some text in the area to which the question is related.
- The owner of the document (i.e. the teacher) receives an email containing the text of the comment and a hyperlink to the comment itself.
- By clicking on the hyperlink, the teacher gets to the exact place in the Google document where the comment is located, thus the context of the question is established.
- The teacher reviews the text and answer the question by adding "Reply" to the comment.

The proposed design patterns allows for more focused, context aware student to teacher communication. All questions and answers remain in the shared document. They might be hidden or even deleted, but still will be available in the documents history. This pattern might conceivably be applied to any collaborative learning activity centred on shared artefacts.

V. Conclusion

The paper has concerned the students' self-reflections of knowledge work practices and associated competences related to their experiences in the implemented courses. Survey findings from a number of cases are presented and accompanied by educational design patterns which emerged from observations in the cases.

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The "Technological Entrepreneurship and Innovations" Programme of Study at the Technical University of Varna – a new challenge for the Bulgarian Higher Education

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Abstract –**The aim of the authors is to share and exchange experience with leading European and world universities, which provide similar programs of study, to identify the problems and the directions for modernizing educational programs, which contribute to the development of the economy based on knowledge and innovations. It also presents our views and the measures to be taken in order to develop "the triangle of knowledge" and "start-up" enterprises on the territory of the university.**

Keywords – **technological entrepreneurship; innovations; "triangle of knowledge"**

I. INTRODUCTION

Entrepreneurship is considered to be the main driving force of economic growth. In turn, technologies are crucial in the development of entrepreneurial activity. The need for personnel with the qualifications of entrepreneurs, who better know the technology, is constantly rising. In response to the demand for such specialists most universities around the world provide educational programs in technological entrepreneurship.

A. Comparative analysis of the university courses in «Technological Entrepreneurship» in Europe and USA

Most of the universities, which have been the subject of this study, offer courses in Technological Entrepreneurship and Innovation, and these include Harvard University, Stanford University, McMaster University, University Saint Mary, The University of Pittsburgh, Technical University of Varna [17, 16, 7, 6, 4, 18]. Others offer courses only in Technological Entrepreneurship, such as the University in Eindhoven, the European Centre of Innovation and Technologies, University College London and the Centre for Entrepreneurial Training[5, 8, 14], and still others combine technological entrepreneurship, innovation and management such as MIT Entrepreneurship Center, Arizona University[9]. There is a great variety of different versions of the course such as Technological Entrepreneurship and Innovation, Entrepreneurship and Innovation Management (KTH Royal Institute of Technology, Stockholm)[15],Technological Innovation and Entrepreneurial Management (Reccanati Business School, Tel Aviv)[12], Entrepreneurship and Innovation (University of Canberra)[10], Technological Innovation, Entrepreneurship and Strategic Management (MIT Sloan School of Management)[20] . The course specifics are determined by the demand for specialists in the area.

Different universities have a different approach, methods and courses depending on the demand for specialists. Most universities run Master's degree courses such as Harvard University, University San Antonio in Texas, University of Pittsburgh, University Saint Mary in Canada, McMaster University[17, 3, 4, 6, 7] in Ontario and others. Just a few run a Bachelor's degree course such as the University of Canberra [10], Australia, and University of Arizona [9] provides both a Bachelor's and a Master's course in Technological Entrepreneurship. MIT Sloan School of Management [20] in Cambridge, USA and the Technical University of Eindhoven [5], the Netherlands offer even PhD courses.

The course is most commonly offered at American universities and they are the ones that demonstrate greater flexibility about the methods of training, the ways of qualification and the opportunities for development. An interesting example of different training is the Business School in Stanford, which provides a highly flexible interactive training with video lectures and online seminars. According to the school the unique approach it has adopted manages to train their students to become effective innovators. (Stanford University [16]) Another example of flexibility on the Master's degree courses is training on particular days of the week in order to allow for planning and ability to combine working or other engagements with the course of study. Such is the example with the University Saint Mary [6] in Canada, Quebec Reccanati Business School[12], Tel Aviv, Israel. In TU-Varna [18] are available different educational forms like distance learning and regular learning in all degrees- bachelor, master and PhD.

In most universities, which provide Master's degree courses in TEI, the training evolves in 3 stages:

- Courses
- Development of skills through seminars
- A project – Business Plan

An exception to the rule is University Saint Mary [6] in Canada where half of the training is in the form of placement in an industrial enterprise. Another interesting example of how training is conducted is Reccanati Business School [12] in Tel Aviv, where apart from the

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standard forms of lectures and seminars the course offers seminars during the holidays and visits to companies during the academic year. The curriculum also puts special emphasis on case studies, team work and practical projects. (Recanati Business School Tel Aviv [12]). With the Bachelor's degree courses there is a greater variety of curricula. For example, Arizona University [9] teaches the foundation of technologically based innovation with special emphasis on leadership, entrepreneurship and the basics of management and with special attention to project leadership and innovation processes and development. (Arizona State University [9]). The Australian National University, Canberra [10] runs a course in Entrepreneurship and Innovation, which students can take together with another course offered by the university so that they can meet the needs of employers. Students can supplement their education with additional placement in the last year of their training and most of them have the opportunity to study one semester in an international partner institution on a foreign educational course. Thus, the course ensures a high degree of flexibility through the possibility to choose the option of an open course in more than 50 fields of study in all the six faculties of the university. (University of Canberra [10], Australia) At TU-Varna [18] the Bachelor's degree course provides a good combination of engineering and economic subjects, which supplies students with technological and entrepreneurial knowledge and prepares them for work in existing technologically based companies, and also gives them the opportunity to acquire the skills needed to start their own innovation enterprises.(TU-Varna [18]) All European universities offer student exchange under different programmes, such as Erasmus, in conformity with the policy of the European Union of the 1990s for raising the quality of higher education. (Bologna process)

Some universities offer full-time and extramural modes of study, and the latter covers a longer period of time. Such an example is Saint Mary's University [6], Canada with a 20-month long course for full-time students and 28-month long course for extramural studies. Other institutions, apart from their full-time courses, offer short courses for students from other faculties, such as University College London [14]

In Europe there has been a growing interest in entrepreneurship and innovation. What is more, the policy of the European Union aims to support that activity through organisations such as the European Institute in Innovation and Technologies (EIT) [8] and the Knowledge Innovation Community (KIC). The mission of the Institute is to enhance sustainable development in Europe and competitiveness by expanding the capacity of technologies in EU. (EIT)

Creating more work places through the fast growth of innovation companies is one of the major goals of EU. The activities of EIT through KIC (Knowledge Innovation Community) are to support innovation in existing companies and to open up new business opportunities. The vital elements of providing support to entrepreneurial activities are ensuring access to funding and giving support in the development of business skills. (EIT) [8]

'Majorities in the US, the European Union, and China associate themselves with attitudes often ascribed to entrepreneurs. Americans, however, are more likely than those in the European Union and China to see themselves as risk takers, competitive, and confident they can accomplish difficult tasks.'[1] in order to deal with this deficit in the entrepreneurial aptitude EIT [8] aims to create a more favourable environment in Europe for the development of talent, entrepreneurship and innovation. One of the challenges is to bring about a change in the way entrepreneurs are perceived and appreciated in Europe. (EIT) For the purpose, the Knowledge Innovation Community (KIC) have developed its own educational courses which focus on entrepreneurship and innovation and are based on the partnerships between universities, companies and research centers. As a result of that cooperation graduates get degrees from two universities, gain international experience as well as entrepreneurial qualifications and innovation skills. The Community started its activities in 2011 and for the first year managed to attract more than 600 students. EIT [8] expects that 10000 Master's students and as many PhD students will have completed the KIC courses until 2020 and thus will integrate excellent scientific and technical knowledge with entrepreneurial skills.

There are three main services KIC provides as business support, which help entrepreneurs to turn their ideas into successful businesses. These services are focused on areas such as technologies, market assessment, increase of human resources, mentoring and last but not least risk capital through specific innovation techniques of KIC.(EIT) [8]

What is characteristic of all universities is that they have Centers for Technological Entrepreneurship and Innovation, which support the students on the respective course by putting them in contact with various financial institutions, existing technological enterprises and aid start-up technological enterprises. Some universities use these centers to offer short courses for students from other programs of study and faculties who have an interest in starting their own business so that they can develop additional skills. An example of this is the Centre for Entrepreneurial Learning in SfEL London [22], which works in cooperation with the University of Hong Kong and runs one week course in entrepreneurship, creativity and innovation in Shanghai, Beijing and London and is part of an international course in business and management.(CfEL) We should mention the support provided by the Centre of Entrepreneurship and Business Interaction at University College London [14] (UCL), which maintains close contact with the European system of mentoring and investment Seedcamp, which itself supports many of the graduates in Technological Entrepreneurship.

The course at University Saint Mary [6] in Canada is structured in such a way that it creates T-shaped specialists. According to Steve Philp [2] of Open Group T-shaped specialists are "individuals who are experts or specialists in a core skill but also have a broad range of skills in other areas. A t-shaped person combines the broad level of skills and knowledge (the top horizontal part of the T) with specialist skills in a specific functional area (the bottom, vertical part of the T). They are not generalists because they have a specific core area of expertise but are often also referred to as generalizing specialists as well as T-shaped

people."[2]. That is a great advantage for students at university, because it gives them a broad specialisation. (Saint Mary's University[6])

B. Concept and Implementation of the courses in Technological Entrepreneurship at Technical University-Varna.

Training on the Bachelor's, Master's and PhD degree courses in Technological Entrepreneurship started at the Technical University –Varna[18], at the department of "Economics and Management" /now Industrial Management/ in the autumn of 2011 with admission of students on the Bachelor's course. The start of teaching that course, which is new for Bulgaria, was necessitated by the objective needs of the labour market and the business in a country that is in a deep crisis and the experience of the department and the university in training "engineer-managers" on the "Industrial Management" course, which itself was offered for the first time in Bulgaria in the distant 1991 when the country was in a period of transition from planned to market economy.

Technology Entrepreneurship and Innovation course is a "hybrid". It combines modern engineering education, with an emphasis on technology and innovation, with in-depth and comprehensive knowledge of economics, management and entrepreneurship.

Students of this specialty receive:

• fundamental engineering training with an emphasis on technology, management and development of enterprises in different economic sectors and creation in new ones;
• fundamental training in the field of technological innovation and creativity;
• fundamental economic and management training;
• specialized training in entrepreneurship and in particular of technological entrepreneurship;
• specialized training in high and green technology as an object of management;

In "TEI" course students acquire following skills:

• Development of entrepreneurial and managerial competence;
• creative thinking and generating new ideas;
• design of high-tech processes;
• business opportunities analyzing and identifying successful business ideas in the field of high technologies;
• market and competitors analysis, evaluation, creating and developing their own competitive advantages;
• developing business plans for start ups in the field of high technologies and skills for effective management;

The training ends with a state exam or thesis defense. The «Technological entrepreneurship» course, taught together with the students on the «Industrial Management» course, is based not only on the knowledge, skills and key competences in the field of entrepreneurship and innovation, but also in the field of management so that it can integrate the symbiosis of the entrepreneurs-innovators and managers in the manner of «Hewlett and Packard», «Steve Jobs and Steve Wozniak» and others.

The University «Technological Park» will serve as a real base for practice and placement of the students on the "Technological Entrepreneurship" course so that their knowledge will be transformed into skills and key competences. The academic authorities of the university are considering and preparing a project for setting up and building up a «virtual technological park» as the next step in the development of the Technological park, thus developing «the triangle of knowledge», which integrates scientific research carried out at leading universities in the region (technical, economic and medical) and their commercialisation in order to stimulate the development of the business, to build up and develop the regional economy, on the basis of knowledge and innovation. The participation of students from the fields of engineering of priority for the region, and of those on the Technological Entrepreneurship course in the «virtual technological park» has been planned not only as a practice but also as a place for innovation and entrepreneurship.

Students who successfully complete this education will be able to work as:

• entrepreneurs who can create, organize and control technology and high-tech enterprises;
• experts - business development; innovative development; technological development and others in different kind of companies;
• experts in national, regional and local institutions - in entrepreneurship and innovation;
• consultants or participants in advisory teams related to the promotion of small and medium business of the company, regional and national level;
• experts in technological development and innovation in science - research organizations;
• experts in innovation, technology and entrepreneurship in structures and projects of the EU and others.

In 2015 finished first graduates of this unique specialty and have yet to be analyzed as the realization of its graduates and the strengths and weaknesses encountered during training.

Since the beginning of autumn students on the «Technological Entrepreneurship» course have student placement in real business conditions as part of an European project and with European funding. The programme for the placement has been developed in such a way that it helps the process of study to be adapted as much as possible to the needs of business and the other representatives of the labour market.

TU-Varna[18] also runs a PhD course in Technological entrepreneurship, which will prepare specialists for the business sector and as research workers and innovators in the field of Technological entrepreneurship. [2]

II. CONCLUSION

As a whole the course in Technological Entrepreneurship and Innovation is a new course worldwide. The Technological Entrepreneurship and Innovation course is quite new for Bulgaria too and is to be established further. Sofia University "Kliment Ohridski"[21] has created such a course with a focus on information technologies, but there has not been much interest in it and no students have enrolled on the course this academic year. Technical University - Varna developed the course in 2011 and it is gradually gaining momentum. Technical University – Varna[18] works for the constant development and improvement of the course

curriculum and draws on the experience of other universities with traditions in that area.

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Creativity and Technology Entrepreneurship as a Factor in the Accelerated Smart Growth of the Industrial Sector in Bulgaria

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Abstract – **The aim of the present paper is to study the link between creativity and technology entrepreneurs and its importance for the success of enterprises. An attempt has been made to evaluate the creativity of a certain number of entrepreneurs from Bulgarian industrial companies, as an example of creativity and its benefits. The paper also considers the link between creativity and technology entrepreneurship and the strategy for smart specialization as a factor in economic growth.**

Keywords – **Creativity, Technology Entrepreneurship, Education**

I. Introduction

In Bulgaria the issue of creativity and technology entrepreneurship as factors in fulfilling the aims of the "Europe 2020" strategy for smart growth has not been researched and there are no scientific publications on the matter. For that reason we base our thesis of creativity and technological entrepreneurship as factors in the accelerated smart growth of the industrial sector of the Republic of Bulgaria on the research and generalizations of leading American and European researchers cited in the paper and listed in the bibliography, as well as on interviews and surveys the authors have conducted with businessmen from the industrial sector, lecturers and students in "Technology Entrepreneurship" at the Technical University Varna (TUV). It should be pointed out that the course of study in "Technology Entrepreneurship", not only at TUV but in the Republic of Bulgaria as a whole, was first run 3 years ago and practically we can speak of business people in the real industrial sector of the country as early as the beginning of the 90s with the transition of the country from a centralized planned economy to a market economy. Practically no engineering graduates in "Technology Entrepreneurship and Innovation", who have received special training in creativity both theoretically and practically, have entered the business. Thus, the present research which studies the link between creativity and technology entrepreneurship is the first of its kind but it will continue in the coming years.

A. The role of creativity and technology entrepreneurship as factors in economic growth

A great part of the researchers [1,2] state that creativity grows in importance in gaining a competitive advantage in a fast developing economy and in a united global market With the development of technologies and innovation creativity is of key importance for business managers as it is considered to contribute indirectly to the development of new products, the improvement of old ones or the establishment of completely new businesses which bring about a competitive advantage for the company [1]. Some authors [3] believe that "creative entrepreneurship" has been influenced by globalization as a process and leads to changes in the corporate culture of the organisations at all levels: that of the individual, the team or the whole organization. On the other hand, modern technological society makes it necessary to integrate technologies and creativity in order to promote a certain idea or create a new product or service. At the same time the acquisition of knowledge together with creative thinking could contribute to the development of entirely new products or services which emerge out of seemingly unrelated ideas or sources. [3] In a global economy creativity helps the entrepreneur to express himself/herself in regard to the technological opportunities in ways which directly lead to a competitive advantage for the company. It is perceived as "a structure of ideas and products which are new and potentially useful" [3], and for the entrepreneur, apart from this usefulness, the link between the technological innovation and the profitability of the newly developed products or services from an economic point of view is important. Florida [4] believes that there is a direct link between creative ability and the concentration of technologies in certain areas. On the other hand, in relation to the link between education and creativity the authors believe that education has a great impact on the creative abilities of technology entrepreneurs and support Florida's belief with the fact that it is in great cities where most Technical Universities in Bulgaria are located that there is a concentration of technological enterprises. Some authors [5] believe that at the basis of the process of coming up with entrepreneurial ideas is the acquired knowledge of better understanding of the markets and the way they function, of the customers and the problems they have as well as a good knowledge of technologies which will led to the creation of a new product or service.

B. The link between creativity and technology entrepreneurship and the role of training in forming it

Over the last few years a study has been carried out of the degree of creativity of students in "Technology Entrepreneurship and Innovation" at the Technical

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University Varna and of practicing technology entrepreneurs in Bulgaria through a test, developed by Ettile and O'Keefe[6] *in their book "Innovative Attitudes, Values, and Intentions in Organizations*. It is based on several years' study of attributes possessed by men and women in a variety of fields and occupations who think and act creatively. There are 40 questions in the test. From 1 to 39 the respondents have to do a choice between three different answers (Agree, Undecided/Don't Know and Disagree). The 40th question contains a list of terms that describe people whish have to choose 10 from them. The evaluation is made of 5 rating scale where 5 is Almost always true and 1 is Almost never true)

The study reveals that students demonstrate a considerably higher level of creativity than of entrepreneurs. Most of the students score slightly over the average creativity, while the predominant number of entrepreneurs is average creative. That could mean that with age, with the acquisition of knowledge, skills and experience the creativity of business people decreases or can be explained with the fact that most of the entrepreneurs are in their most active working age between 30 and 50 when a person has other priorities too like starting a home, a family and looking after children. That is why entrepreneurs at that stage in their lives are less willing to take risks because of the priorities they have whereas students and young entrepreneurs under 30 are not thus burdened. Exceptions with over the average levels of creativity are most often with entrepreneurs over 50. That fact to some extent disproves the thesis that knowledge, skills and the experience gained over the years diminish the degree of creativity and supports the idea for the link of creativity and the extent to which risks are taken and priorities are changed. Entrepreneurs over the age of 50 are not busy raising children as they would have already grown up, they already have a home and fully commit themselves to their business.

If we look at figure 1 we can clearly see that the highest number is that of average creative entrepreneurs between the ages of 30 and 40, while with those over 50 they are distributed equally between average creative and those over the average degree of creativity. That fact, according to some authors completely disproves the theory that knowledge, skills and the experience gained "kill" creativity in people. In support of these statements is the view of the authors [7] of the book ´Encyclopedia of Creativity, Invention, Innovation, and Entrepreneurship´ who think that "Creativity usually comes from extensive, diverse knowledge rather than from eccentric or inherently gifted individuals with a bent toward bizarre imagery". On the other hand, they support the thesis that when one has something to lose he does not dare to be creative. The study raises the question whether creativity is directly related to our willingness to take a risk – another feature typical for an entrepreneur like Richard Cantillon and his followers.

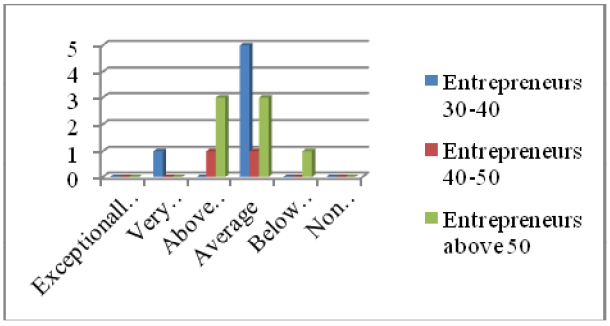

Fig. 1. Degree of creativity of entrepreneurs in terms of age

If we look figure 2 we can see clearly that the highest number of students have a level of creativity over the average and that of very creative while with practicing entrepreneurs the highest number is that of the average creative ones and that number decreases proportionately to the increase in the degree of creativity. That could come in support of the thesis that when you have nothing to lose you can afford to be creative and to take risks.

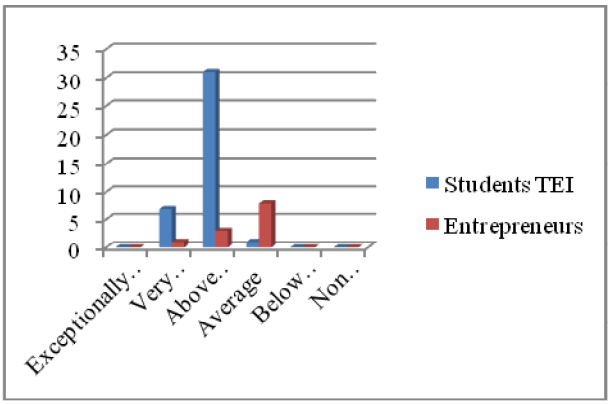

Fig. 2. Proportion between the degree of creativity of students in TEI and practicing entrepreneurs

If we look at figure 3 we cannot fail to observe the fact that with age their creativity changes within quite narrow boundaries. As it can be seen on the graph below the profile in the last year of their studies has changed and the number of those who scored very creative has fallen and the number of those with above average creativity has risen. We can also notice an increase in the number of students who are average creative. That change can be explained again with age and the increased responsibilities of young people as they near graduation. On the other hand, overall data show that students on the Technology Entrepreneurship and Innovation course of study score a level of creativity much higher than the average one. At the university they take a specialized course of training in creativity, and the development of that quality has been integrated into other main disciplines such as Economics, Technology Entrepreneurship, Technology Transfer, Franchising and Outsourcing, Basics of Entrepreneurship, etc.

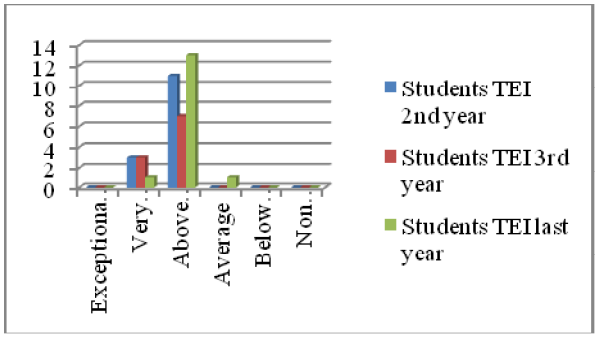

Fig. 3. Creative level of students according to their year of study

In interviews with the respondent entrepreneurs, between the ages of 30 and 50, say that the circumstances force them to be cautious, to check the reliability of the business and to strive for minimizing the risk. Such considerations are caused by a number of factors: on the one hand it is the economic crisis, on the other hand it is the lack of support by the state, imperfect legislation, taxation policy, etc.

Hunter et al. [8] see creativity as an interaction between the individual and the situation, which is facilitated by the appropriate environment of the climate. Regarding university education in Technology Entrepreneurship and Innovation and the creation of favourable conditions for the development of technology entrepreneurs the course of study has good results in stimulating students'creative abilities. The test results unambiguously point at the high degree of creativity of our students. In the interviews with the students they voice their concern about starting a business and name as the main reason for their concern the lack of trust in them, which is mainly due to their age, lack of trust by the financial institutions, by the state and the lack of support under various programs. That is why we would like to look at the policies of the EU and RB for stimulating technology entrepreneurship in young people[9].

C. Outlining the directions for development at the government and corporate level and in the educational system.

As a whole the EU [10] has found out that in the past program period not much attention has been paid to starting businesses and to emerging technological enterprises and so these two segments are included in the new innovation policy of the European Union and so is the link between science and business, that is the strengthening of the relations between the elements of the triangle of knowledge (business-knowledge-science) with regard to SMEs, entrepreneurship and technologies. These highlights have been incorporated both in the innovation policy of Bulgaria and the new action plan Entrepreneurship 2020 [11], which contains a few aims, which are directly related to the issue, namely:

- Development of entrepreneurial knowledge and training
- Creating an environment where entrepreneurs will develop successfully

As far as Bulgaria is concerned for the new program period in the Innovation strategy of smart specialization of the Republic of Bulgaria, the technological development is directly related to OP „Science, Knowledge and Smart growth" [10]. At the same time the "Erasmus for young entrepreneurs" program [12] was set up and it aims to provide young entrepreneurs with the opportunity to exchange experience and ideas with experienced entrepreneurs from other countries.

Smart specialization [13] as a strategic development approach in Bulgaria which aims to support scientific research and innovation in order to maximize knowledge potential in the different regions. It is done on the basis of regions because the strategy aims to specify the objectives and the tasks for every region depending on its capabilities, capacity and needs, and then to set particular tasks. For the NER (North East region), where TU- Varna is located the task of the university is to prepare innovative, creative, smart and capable young people, who can develop their own business in the field of technologies. In that way the university will further the capabilities of young people so that they can set up a competitive business and thus make their own contribution to the economic development of our country. The specialty of Technology Entrepreneurship and Innovation has been opened in order to meet the increased need for technology entrepreneurs in business, and at the same time to improve the link between business and science.

The authors [7] also endorse the recommendation of Carayannis, which says: „Encouraging the wide sharing of best practices as well as mistakes within universities, government entities, or companies can help to eliminate redundancies of effort and prevent the repetition of unproductive pursuits, while providing an atmosphere for synergy, remote reference, and the fertile interaction of ideas."

II. Conclusion

The present study has done a review of the literature on creativity and its link with technologies and entrepreneurship. It also includes a survey of the degree of creativity of students on the course of Technology Entrepreneurship and Innovation at the Technical University Varna and some technology entrepreneurs from business, which determined their degree of creativity and how it changes in terms of age, extent of knowledge and experience gained. Finally, it outlines further directions for development at the government and corporate level and in education. The present study sets the necessary prerequisites for a more detailed study of the issue in order to improve the link between education, science and business as well as to develop the creativity of young people.

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Software Implementation of a Module for Encryption and Decryption Using the RSA Algorithm

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Abstract – **The paper describes MS EXCEL-based application implementing the processes of encryption and decryption of texts in English and/or Bulgarian using the RSA algorithm. The processes of encryption and decryption are illustrated. The material is used in the educational process in the course "Telecommunication Security" but it can be applied in other disciplines involving issues of cryptographic information protection.**

Keywords – **Encryption, Decryption, RSA algorithm, English/Bulgarian texts, MS EXCEL.**

I. INTRODUCTION

The paper describes one of the cryptographic methods for information protection – algorithm RSA, implemented using MS Excel. Cryptographic methods for protection are known as means for converting the information as a result of which its content is hidden. The task of cryptography, i.e. secret data transmission is the protection of information that needs protection from malicious actions of various entities. This is done by methods based on secret algorithms to convert the information including algorithms that themselves do not appear secret, but use secret parameters. Encryption algorithms using keys suggest that no one can read the data, except one who has the key for their decryption.

RSA is one of the first practical public-key algorithms (cryptosystems) and it is widely used for secure data transmission. In such a cryptosystem, the encryption key is public and differs from the decryption key which is kept secret. In RSA, this asymmetry is based on the practical difficulty of factoring the product of two large prime numbers, the factoring problem. RSA is made of the initial letters of the surnames of Ron Rivest, Adi Shamir and Leonard Adelman, who first publicly described the algorithm in 1977. The English mathematician Clifford Cocks working for the UK intelligence agency GCHQ, had developed an equivalent system in 1973, but it was not declassified until 1997 [6].

In the RSA algorithm the property "comparability of the numbers" is used. This is a relationship between two integers a and b, executed exactly when $a - b$ is divided by the number m (notations: $a = b \pmod m$). The algorithm is based on the fact that modern computers calculate the numbers as a product of large primes which involves complex and lengthy calculations.

Since the module is used in the course "Telecommunication security" for the convenience of students the effect of each of the three modules is illustrated with different colors:

- module for determining the multiplicative inversion;
- module for encryption of texts in Bulgarian and/or English;
- module for decryption of texts in Bulgarian and/or English.

MS Excel module developed covers the demonstration of multiple options and contains the following files:

1. *RSA_encryption.xls* – for encryption of texts in English and/or Bulgarian using the RSA algorithm with the following seven worksheets:

- 17e – for demonstration of the process of encryption of texts in English using the RSA algorithm, where $e = 17$ and $n = 2773$;
- 7e – for demonstration of the process of encryption of texts in Bulgarian using the RSA algorithm, where $e = 7$ and $n = 55$;
- 23e – for demonstration of the process of encryption of texts in English using the RSA algorithm, where $e = 23$ and $n = 55$;
- 31e – for demonstration of the process of encryption of texts in English and/or Bulgarian using the RSA algorithm, where $e = 31$ and $n = 4067351$;
- 13e – for demonstration of the process of encryption of texts in English and/or Bulgarian using the RSA algorithm, where $e = 23$ and $n = 77$;
- 37e – for demonstration of the process of encryption of texts in English and/or Bulgarian using the RSA algorithm, where $e = 37$ and $n = 77$;
- 157e – for demonstration of the process of encryption of texts in English using the RSA algorithm, where $e = 157$ and $n = 55$;

2. *RSA_decryption.xls* – for decryption of texts in English and/or Bulgarian using the RSA algorithm with the following three worksheets:

- 157d – for demonstration of the process of decryption of texts in English using the RSA algorithm, where $d = 157$ and $n = 2773$;
- 23d – for demonstration of the process of decryption of texts in Bulgarian using the RSA algorithm, where $d = 23$ and $n = 55$;

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- 37d – for demonstration of the process of decryption of texts in English and/or Bulgarian using the RSA algorithm, where $d = 37$ and $n = 77$.

II. DESCRIPTION OF THE PROGRAMMING MODULE

For implementation of cryptosystems with public keys the most important algorithm is the RSA algorithm, proposed by Rivest, Shamir and Adelman in 1978 in their paper "On Digital Signatures and Public-Key Cryptography" in Communications ACM. RSA scheme is based on the fact that two large prime integers p and q are easily chosen and multiplied, but it is much more difficult to factorize their product $n = p.q$. Therefore, the product as part of the encryption key can be publicly available; while the multipliers, which the product decomposes to, that can "expose" the key to deciphering, remain hidden. If the length of each multiplier is more than 100 digits, the multiplication can be performed in seconds rather tiresome factorization of multipliers (primes) results may require billions of years.

The message in the RSA scheme is first presented as integers from the interval $(0, n-1)$. Each user chooses his/her own value of n and a pair of positive integers e and d in the way described below. The user publishes his/her encryption key, the pair of numbers (n, e) in a public catalog. The decryption key comprises a pair of numbers (n, d) where d is kept secret. The encryption of the message M and the decryption of the ciphertext C is defined as follows [1, 2, 3, 4, 5]:

$$\begin{aligned} C &= E(M) = (M)^e \pmod n \quad \textit{for encryption}, \\ M &= D(C) = (C)^d \pmod n \quad \textit{for decryption.} \end{aligned} \tag{1}$$

This is easily calculated. The result of each operation is an integer from the interval $(0, n-1)$. In the RSA scheme n is the result of the multiplication of two large prime numbers p and q: $n = pq$.

Although n is public, p and q are "hidden" because of the great complexity of the factorization of n. Then the function, called Euler's function is determined:

$$\phi(n) = (p-1)(q-1). \tag{2}$$

The parameter $\phi(n)$ has the interesting property, described by Diffie and Hellman: for each integer X from the interval $(0, n-1)$ and any integer k the following relationship is valid [4, 5]:

$$X = X^{k\phi(n)+1} \pmod n. \tag{3}$$

Therefore, if all other arithmetic operations are executed by modulo n, the arithmetic operations in the power are done by modulo $\phi(n)$. Then randomly a large integer d is selected, being relatively prime with $\phi(n)$, which means that $\phi(n)$ and d should not have a common divisor different from 1. This is written in the following manner:

$$\mathrm{GCD}[\phi(n), d] = 1. \tag{4}$$

In this case, GCD means "greatest common divisor" and the last condition will be satisfied by any prime number larger than the largest of (p, q). The parameter e, $0 < e < \phi(n)$, is further found:

$$ed \mod \phi(n) = 1, \tag{5}$$

which is equivalent to selecting e and d satisfying the following condition:

$$X = X^{ed} \pmod n. \tag{6}$$

Therefore,

$$E[D(X)] = D[E(X)] = X \tag{7}$$

and the correct decryption is possible. One possible way to break the cipher when known the key (n, e) is to factorize n into the multipliers p and q, to calculate $\phi(n) = (p-1)(q-1)$ and d. All these operations, except the factorization, are simple actions.

Using the RSA scheme

In the example from the paper "On Digital Signatures and Public Key Cryptography" of Rivest, Shamir and Adelman $p = 47$ and $q = 59$ are selected in the role of prime numbers. Therefore, their product is $n = pq = 2773$ and the function of Euler is $\phi(n) = (p-1)(q-1) = 2668$. The parameter d is chosen to be co-prime with $\phi(n)$, for example $d = 157$. Then the value of e is calculated, as a variation of Euclid's algorithm for calculating GCD described below is used for this purpose.

$$ed \mod \phi(n) = 1, \text{ i.e. } 157e \mod 2668 = 1. \tag{8}$$

Therefore, $e = 17$.

In their paper Rivest, Shamir and Adelman considered as an example the following plaintext: ITS ALL GREEK TO ME, where each letter is replaced with two-digit numbers from the interval $(01, 26)$, corresponding to its position in the alphabet and the space is encoded with 00. As a result, the plaintext is written in the following manner:

0920 1900 0112 1200 0718 0505 1100 2015 0013 0500.

Each character is presented by an integer from the interval $(0, n-1)$. Therefore, in this example the encryption may be presented in the form of a block of four digits, since this is the maximum number of digits that always gives a number less than $n-1 = 2772$. The first four digits (0920) of the plaintext are encrypted as follows:

$$C = (M)^e \mod n = (920)^{17} \mod 2773 = 948. \tag{9}$$

Continuing the process for the remaining digits of the plaintext the ciphertext is obtained:

$C = 0948\ 2342\ 1084\ 1444\ 2663\ 2390\ 0778\ 0774\ 0229\ 1655$.

The plaintext is recovered using the decryption key.

$$M = (C)^d \mod n = (C)^{157} \mod 2773. \tag{10}$$

So the decrypted text is obtained:

0920 1900 0112 1200 0718 0505 1100 2015 0013 0500.

Calculation of *e*

To calculate the parameter e a variation of the Euclidean algorithm is used to calculate GCD of $\phi(n)$ and d. First, the sequence of values $x_0, x_1, x_2, \ldots$ is calculated, where $x_0 = \phi(n)$, $x_1 = d$, and $x_{i+1} = x_{i-1} \mod x_i$, until $x_k = 0$ is received. Then $\mathrm{GCD}(x_0, x_1) = x_{k-1}$. For each x_i the

numbers a_i and b_i are calculated where $x_i = a_i x_0 + b_i x_i$. If $x_{k-1} = 1$, b_{k-1} is the multiplicative inversion of $x_1 \mod x_0$ i.e. $b_{k-1} = x_1 \mod x_0$. If b_{k-1} is negative, the decision will be $b_{k-1} + \phi(n)$. The method for calculating e using d and $\phi(n)$ for the considered example is illustrated in Fig. 1.

i	x_i	a_i	b_i	y_i
0	2668	1	0	–
1	157	0	1	16
2	156	1	–16	1
3	1	– 1	17	

$y_i = \left\lfloor \frac{x_{i-1}}{x_i} \right\rfloor$ $\lfloor . \rfloor$ - integer

$x_{i+1} = x_{i-1} \mod x_i$

$x_{i+1} = x_{i-1} - y_i x_i$

$a_{i+1} = a_{i-1} - y_i a_i$

$b_{i+1} = b_{i-1} - y_i b_i$

Fig. 1. Calculation of e using d and $\phi(n)$ for the example considered

Module for determining the multiplicative inversion

Fig. 2 shows the module for determining the multiplicative inversion implemented in MS Excel.

The values in the blue cells are entered by the user, such as p and q are primes, and d is the secret key of the user (for decryption).

p =	47
q =	59
n =	2773
FI =	2668
d =	157

Correction? 2668

n = p*q
FI = (p-1)*(q-1)

Iteration	i	x_i	a_i	b_i	y_i
0	0	2668	1	0	
1	1	157	0	1	16
2	2	156	1	-16	1
3	3	1	-1	17	

Note 1: Values in the blue cells are entered by the user.
p, q - primes, d – secret key of the user (for decryption).

Note 2: If x_i is not equal to 1 in the last iteration, the bottom row is copied as many times as necessary to fulfill the condition. One may need to delete some of the rows, the goal is $x_i = 1$ again in the last executed iteration (actions performed by the user).

Note 3: If the value of b_i is positive in the last iteration, then it is the multiplicative inverse of d, i.e. the exponent e for the encryption of messages. If the value of b_i is negative in the last iteration, it is necessary to make the following correction: to obtain the multiplicative inverse of d, the value of FI is added to the resulting value of b_i.

Fig. 2. Module for determining the multiplicative inversion implemented in MS Excel

In the case when x_i is not equal to 1 in the last iteration, the last row is copied as many times as it is necessary to fulfill the condition. One may need to delete some of the rows, the aim again is to obtain $x_i = 1$ in the last executed iteration (actions performed by the user, in particular students).

The value of b_i in the last iteration, if positive, is the multiplicative inverse of d, i.e. the exponent e for the encryption of messages. In the case when b_i is negative at the last iteration, it is necessary to make the following correction: the value of FI is added to the resulting value of b_i to obtain the multiplicative inverse of d.

The values of n and FI are calculated according to the formulas:

$$n = p.q \text{ and } \text{FI} = (p-1).(q-1). \quad (11)$$

Module for encryption of texts in Bulgarian and/or English

The module allows performing the complex calculations done for encryption using the RSA algorithm:

$$C = E(M) = (M)^e \mod n. \quad (12)$$

Since having powers in a large number, and the exponent is a large number, this calculation cannot be performed using MATLAB and MS Excel, therefore in order to avoid this difficulty the algorithm SM (Square-and-Multiply), proposed by Douglas Stinson, in his book "Cryptography Theory and Practice", 1995, is used.

Fig. 3 illustrates the process of encryption of texts using the algorithm SM, where for the convenience of students the different stages in the calculation of the ciphertext are presented with different colors. The value of the plaintext is entered by the user, and e is the public key for encryption. In the second column e is represented in binary notation: $e = 17_{(10)} = 10001_{(2)}$. In the first row for calculating the modular multiplication 1 is always written. If in the binary representation of e there is 1, the result of the line above is squared and multiplied by the code of the plaintext. In fact, the result obtained in the operation "modular multiplication" is the remainder of dividing the number squared and multiplied with the code of the plaintext by modulo n.

Module for decryption of texts in Bulgarian and/or English

The module allows performing the complex calculations done in the decryption using the RSA algorithm:

$$M = D(C) = (C)^d \mod n. \quad (13)$$

Since having powers in a large number, and the exponent is a large number, this calculation is performed using the algorithm SM (Square-and-Multiply).

Fig. 4 illustrates the reverse process, decryption of texts using the algorithm SM, again to facilitate students the different stages for calculation of the code of the plaintext are presented with different colors. The value of the ciphertext is entered by the user, and d is the secret key of the user for decryption.

The ciphertext is the encoded text, i.e. the text to be decrypted. In the second column d is represented in binary notation, where $d = 157_{(10)} = 10011101_{(2)}$. If there is 1 in the binary representation of d, then the value of the modular multiplication in the line above is squared and multiplied with the ciphertext. The result is the remainder of dividing the number squared and multiplied with the code of the ciphertext by modulo n.

e: 17 **Plaintext:** 920 **Modulo:** 2773

№	$e_{(2)}$	Modular multiplication	Method of calculating the modular multiplication
0		1	
1	1	920 x 1^2 = 920	
2	0	920^2 = 635	920^2 = 846400 = 305 x 2773 + 635
3	0	635^2 = 1140	635^2 = 403225 = 145 x 2773 + 1140
4	0	1140^2 = 1836	1140^2 = 1299600 = 468 x 2773 + 1836
5	1	920 x 1836^2 = 948	920 x 1836^2 = 3101224320 = 1118364 x 2773 + 948

$920^{17} \bmod 2773 = 948$

Fig. 3. Module for encryption of texts in English and/or Bulgarian

d: 157 **Ciphertext:** 1084 **Modulo:** 2773

№	$d_{(2)}$	Modular multiplication	Method of calculating the modular multiplication
0		1	
1	1	1084 x 1^2 = 1084	
2	0	1084^2 = 2077	1084^2 = 1175056 = 423 x 2773 + 2077
3	0	2077^2 = 1914	2077^2 = 4313929 = 1555 x 2773 + 1914
4	1	1084 x 1914^2 = 2246	1084 x 1914^2 = 3971121264 = 1432066 x 2773 + 2246
5	1	1084 x 2246^2 = 1945	1084 x 2246^2 = 5468255344 = 1971963 x 2773 + 1945
6	1	1084 x 1945^2 = 737	1084 x 1945^2 = 4100799100 = 1478831 x 2773 + 737
7	0	737^2 = 2434	737^2 = 543169 = 195 x 2773 + 2434
8	1	1084 x 2434^2 = 112	1084 x 2434^2 = 6422001904 = 2315904 x 2773 + 112

$1084^{157} \bmod 2773 = 112$

Fig. 4. Module for decryption of texts in English and/or Bulgarian

III. Conclusion

The paper describes one of the widely used cryptographic algorithms – the RSA algorithm. MS EXCEL-based application developed for implementing the processes of encryption and decryption of English and/or Bulgarian texts using the RSA algorithm is presented in details.

The material is used in the educational process in the course "Telecommunication Security", compulsory in the curriculum of the specialty "Telecommunication Systems" for the "Bachelor" degree but it can be applied in other courses involving cryptographic methods for information protection.

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MS Excel-Based Application for Encryption and Decryption of English Texts with the Hill Cipher on the Basis of 3×3-Matrix

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Abstract – **The paper describes MS EXCEL-based application implementing the processes of encryption and decryption of English texts using the Hill cipher based on the matrix of size 3×3. The processes of encryption and decryption of 6-character words in English are illustrated. Numerous examples obtained by the application developed are presented in the paper. The material is used in the educational process in the course "Telecommunication Security" but it can be applied in other disciplines involving issues of cryptographic information protection.**

Keywords – **Encryption, Decryption, Hill cipher, English texts, MS EXCEL.**

I. INTRODUCTION

In classical cryptography, the Hill cipher invented by Lester Hill in 1929, was the first polygraphic substitution cipher based on linear algebra, which practically processed more than three symbols at once [2, 3, 5].

Operation of the Hill cipher

Each letter is represented by a number modulo 26. Often the simple scheme $A = 0$, $B = 1$, ..., $Z = 25$ is used, but this is not an essential feature of the cipher. To encrypt a message, each block of n letters (considered as an n-component vector) is multiplied by an invertible matrix of size $n \times n$, again modulus 26. In order to decrypt the message, each block is multiplied by the inverse matrix of the matrix used for encryption.

The matrix used for encryption is the cipher key, and it should be chosen randomly from the set of invertible matrices of size $n \times n$ (modulo 26). Of course, the cipher can be adapted to an alphabet with any number of letters, but all arithmetic operations should be done by modulo the number of letters in the alphabet instead of modulo 26 [2, 3, 4, 5, 6, 7].

Example: Let the encryption key is:

$$\boldsymbol{A} = \begin{pmatrix} 6 & 24 & 1 \\ 13 & 16 & 10 \\ 20 & 17 & 15 \end{pmatrix} \quad (1)$$

and let the plaintext (the message for encryption) is *CIPHER*. Then the plaintext is represented by the following two triples:

$$CIPHER \rightarrow \begin{pmatrix} C \\ I \\ P \end{pmatrix}, \begin{pmatrix} H \\ E \\ R \end{pmatrix} \rightarrow \begin{pmatrix} 2 \\ 8 \\ 15 \end{pmatrix}, \begin{pmatrix} 7 \\ 4 \\ 17 \end{pmatrix}. \quad (2)$$

The encryption is performed as follows:

$$\begin{pmatrix} 6 & 24 & 1 \\ 13 & 16 & 10 \\ 20 & 17 & 15 \end{pmatrix}.\begin{pmatrix} 2 \\ 8 \\ 15 \end{pmatrix} = \begin{pmatrix} 219 \\ 304 \\ 401 \end{pmatrix} \equiv \begin{pmatrix} 11 \\ 18 \\ 11 \end{pmatrix} (\text{mod } 26) \quad (3)$$

$$\begin{pmatrix} 6 & 24 & 1 \\ 13 & 16 & 10 \\ 20 & 17 & 15 \end{pmatrix}.\begin{pmatrix} 7 \\ 4 \\ 17 \end{pmatrix} = \begin{pmatrix} 155 \\ 325 \\ 463 \end{pmatrix} \equiv \begin{pmatrix} 25 \\ 13 \\ 21 \end{pmatrix} (\text{mod } 26) \quad (4)$$

$$\begin{pmatrix} 11 \\ 18 \\ 11 \end{pmatrix}, \begin{pmatrix} 25 \\ 13 \\ 21 \end{pmatrix} \rightarrow \begin{pmatrix} L \\ S \\ L \end{pmatrix}, \begin{pmatrix} Z \\ N \\ V \end{pmatrix} \rightarrow LSLZNV\ . \quad (5)$$

The matrix $\boldsymbol{A}$ is invertible since there is a matrix $\boldsymbol{A}^{-1}$ such that $\boldsymbol{A}.\boldsymbol{A}^{-1} = \boldsymbol{A}^{-1}.\boldsymbol{A} = \boldsymbol{I}_3$, where $\boldsymbol{I}_3$ is the identity matrix of dimension 3×3. The inverse matrix of the matrix $\boldsymbol{A} = \begin{pmatrix} a_{11} & a_{12} & a_{13} \\ a_{21} & a_{22} & a_{23} \\ a_{31} & a_{32} & a_{33} \end{pmatrix}$ can be calculated by the formula:

$$\boldsymbol{A}^{-1} = \frac{1}{\det \boldsymbol{A}} \begin{pmatrix} A_{11} & A_{21} & A_{31} \\ A_{12} & A_{22} & A_{32} \\ A_{13} & A_{23} & A_{33} \end{pmatrix}, \quad (6)$$

where $\det \boldsymbol{A}$ is the determinant of a matrix $\boldsymbol{A}$ with size 3×3 defined by expression (7) and A_{ij} is the adjugate of the element a_{ij} in the i-th row and the j-column of matrix $\boldsymbol{A}$:

$$\det \boldsymbol{A} = a_{11}.a_{22}.a_{33} + a_{12}.a_{23}.a_{31} + a_{13}.a_{21}.a_{32} - \\ - a_{13}.a_{22}.a_{31} - a_{11}.a_{23}.a_{32} - a_{12}.a_{21}.a_{33} \quad (7)$$

The adjugate or the algebraic addition A_{ij} of the element a_{ij} is calculated by expression 8 [1]:

$$A_{ij} = (-1)^{i+j} D_{ij} \quad (8)$$

where D_{ij} is the sub-determinant, which is derived from the determinant of the matrix $\boldsymbol{A}$ when crossing of the i-th row and the j-column of the matrix $\boldsymbol{A}$ [1]. In the case the sub-determinants D_{ij} are determinants of the second order and they are calculated by expression (9):

$$D_{ij} = \begin{vmatrix} a & b \\ c & d \end{vmatrix} = a.d - b.c\ . \quad (9)$$

Formula (6) is valid after the modular reduction if the modular multiplicative inversion is used for calculating

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$(\det \boldsymbol{A})^{-1}$. Therefore, in this case, after a preliminary calculation of adjugates A_{ij} according to expressions (8) and (9) transformations led to the following expression for the inverse matrix:

$$\boldsymbol{A}^{-1} = \begin{pmatrix} 8 & 5 & 10 \\ 21 & 8 & 21 \\ 21 & 12 & 8 \end{pmatrix} (\text{mod } 26). \quad (10)$$

To decrypt the ciphertext the following operations can be performed:

$$LSLZNV \rightarrow \begin{pmatrix} L \\ S \\ L \end{pmatrix}, \begin{pmatrix} Z \\ N \\ V \end{pmatrix} \rightarrow \begin{pmatrix} 11 \\ 18 \\ 11 \end{pmatrix}, \begin{pmatrix} 25 \\ 13 \\ 21 \end{pmatrix}, \quad (11)$$

$$\begin{pmatrix} 8 & 5 & 10 \\ 21 & 8 & 21 \\ 21 & 12 & 8 \end{pmatrix} \cdot \begin{pmatrix} 11 \\ 18 \\ 11 \end{pmatrix} = \begin{pmatrix} 288 \\ 606 \\ 535 \end{pmatrix} \equiv \begin{pmatrix} 2 \\ 8 \\ 15 \end{pmatrix} (\text{mod } 26), \quad (12)$$

$$\begin{pmatrix} 8 & 5 & 10 \\ 21 & 8 & 21 \\ 21 & 12 & 8 \end{pmatrix} \cdot \begin{pmatrix} 25 \\ 13 \\ 21 \end{pmatrix} = \begin{pmatrix} 475 \\ 1070 \\ 849 \end{pmatrix} \equiv \begin{pmatrix} 7 \\ 4 \\ 17 \end{pmatrix} (\text{mod } 26) \quad (13)$$

Therefore, after decrypting, the following meaningful text is obtained:

$$\begin{pmatrix} 2 \\ 8 \\ 15 \end{pmatrix}, \begin{pmatrix} 7 \\ 4 \\ 17 \end{pmatrix} \rightarrow \begin{pmatrix} C \\ I \\ P \end{pmatrix}, \begin{pmatrix} H \\ E \\ R \end{pmatrix} \rightarrow CIPHER. \quad (14)$$

II. MS EXCEL-BASED APPLICATION FOR ENCRYPTION AND DECRYPTION OF ENGLISH TEXTS WITH THE HILL CIPHER BASED ON 3×3 MATRIX

Based on the algorithm to encrypt and decrypt English texts using the Hill cipher based on a matrix of size 3×3 [2, 4, 5, 6, 7] MS EXCEL-based application for graphically illustrating the processes of encryption and decryption was developed. It is used in the course "Telecommunication security" for easy assimilation of the material studied by students as the steps at each stage of encryption and decryption of texts are tracked in details.

Description of the application developed

The developed MS EXCEL-based application contains the following modules:

1) Module **"Matrix"** (worksheet A, Fig. 1);

2) Module **"Inverse Matrix"** (worksheet A^(-1), Fig. 2);

3) Module **"Encryption"** (worksheets ENC0, ENC1, ENC2, ENC3, ENC4 and ENC5, Fig. 3);

4) Module **"Decryption"** (worksheets DEC0, DEC1, DEC2, DEC3, DEC4 and DEC5, Fig. 4).

Algorithm for encryption/decryption using the Hill cipher

1. Each letter is represented by a number modulo 26 (26 is the number of letters in the English alphabet) using the simple scheme $A = 0$, $B = 1$, ..., $Z = 25$ (Table 1). In some references the following scheme: $A = 1$, $B = 2$, ..., $Y = 25$, $Z = 0$ is used but this does not affect the processes of encryption and decryption. This transformation is realized in MS EXCEL by using *=CODE(address)-65*, where the built-in function *CODE* determines the ASCII code of the symbol written in the cell, whose address is specified as an argument to the function (*address*). It should be noted that the ASCII code of the symbol A is 41 (hexadecimal), i.e. 65 (decimal). Therefore, to obtain a numeric code 0 for the letter *A* it is required to remove the number 65 by its ASCII code (for the uppercase letters of the English alphabet).

TABLE 1. NUMERICAL PRESENTATION OF THE LETTERS OF THE ENGLISH ALPHABET

Letter	A	B	C	D	E	F	G	H	I	J	K	L	M
Code	0	1	2	3	4	5	6	7	8	9	1	1	1
Letter	N	O	P	Q	R	S	T	U	V	W	X	Y	Z
Code	1	1	1	1	1	1	1	2	2	2	2	2	2

2. The matrix $\boldsymbol{A}$ is selected (Module **"Matrix"**, Fig. 1), which meets the following two conditions: 1) the matrix $\boldsymbol{A}$ is invertible, i.e. its determinant is different from zero; 2) its determinant has no common divisors with the number 26, i.e. is not divisible by 2 and 13.

In the module **"Matrix"** (Fig. 1), the calculation of the determinant of the matrix $\boldsymbol{A}$ is done in stages by formula (7) and it is represented by color codes in order to easily assimilation of the material studied by students.

The determinant of the matrix $\boldsymbol{A}$ is determined in modulo 26, as it is realized in MS EXCEL using the function *=MOD(address;26)*, where *address* is the address of the cell containing the value of the determinant of the matrix $\boldsymbol{A}$ in reality. The built-in function *MOD* practically determines the remainder in division with 26 of the number in the cell with the specified address. After determining the determinant of the matrix $\boldsymbol{A}$ in modulo 26, two conclusions are displayed depending on its estimated value:

1) If the calculated value is different from zero, then the message "The determinant of the matrix is different from 0 - correct choice of matrix!", otherwise the message "The determinant of the matrix is equal to 0 - wrong choice of matrix!" This is implemented in MS EXCEL by the function:

=IF(address<>0; "The determinant of the matrix is different from 0 - correct choice of matrix!"; "The determinant of the matrix is equal to 0 - wrong choice of matrix!"), where *address* is the address of the cell containing the value of the determinant of the matrix $\boldsymbol{A}$ modulo 26.

2) If the greatest common divisor of the determinant of the matrix and the number 26 is different from 1, the message for wrong choice of matrix appears and otherwise – for correct choice of matrix implemented in MS EXCEL by the operator:

=IF(GCD(address;26)<>1; "The greatest common divisor of the determinant of the matrix and the number 26 is different from 1 - wrong choice of matrix!"; "The greatest common divisor of the determinant of the matrix and the number 26 is equal to 1 - correct choice of matrix!"), where *address* indicates again the address of the cell containing the value of the determinant of a matrix in modulo 26 and using the built-in function *GCD* (*greatest common divisor*) *GCD(address;26)* determines the greatest common divisor of the determinant of the matrix (the number in the cell with the address specified) and the number 26.

3. The inverse matrix of the matrix $\boldsymbol{A}$ is calculated (module **"Inverse Matrix"**, Fig. 2, the worksheet A^(-1)) for each of the matrices selected in the previous module.

In the module **"Inverse Matrix"**, the calculation of the determinant of the matrix A is implemented in stages using the relationships (6), (7), (8) and (9), and it is presented with color codes in order to more easily assimilation of the material studied by students. Here, in advance the adjugates of the elements are calculated according to the relationships (8) and (9), then the inverse matrix is displayed on the basis of equation (6). In determining the elements of the inverse matrix the modular reduction is used on the base of the modular multiplicative inversion to calculate $(\det \boldsymbol{A})^{-1}$. The mapping between $\det \boldsymbol{A}$ and $(\det \boldsymbol{A})^{-1}$ is given in Table 2 and it is based on the fact that the remainder when divided the product of $\det \boldsymbol{A}$ and $(\det \boldsymbol{A})^{-1}$ by 26 is 1.

TABLE 2. CORRESPONDENCE BETWEEN $\det \boldsymbol{A}$ AND $(\det \boldsymbol{A})^{-1}$

$\det \boldsymbol{A}$	1	3	5	7	9	11	15	17	19	21	23	25
$(\det \boldsymbol{A})^{-1}$	1	9	21	15	3	19	7	23	11	5	17	25

In the module **"Inverse Matrix"** when calculating the determinant of the matrix $\boldsymbol{A}$ in MS Excel the built-in function is used: *=MDETERM (address 1:address 2)* where *address 1:address 2* indicates the "array", i.e. the area of cells which the determinant will be calculated for. The modular multiplicative inverse of $\det \boldsymbol{A}$ in the application developed is determined using the pre-established correlation table in the case of English (Table 2) and several input calls to the built-in function *IF*:

=IF(address=1;1;IF(address=3;9;IF(address=5;21; IF(address=7;15;IF(address=9;3;IF(address=11;19; address1)))))),

where *address* is the address of the cell containing the determinant of the matrix $\boldsymbol{A}$ according to equation (6) and *address1* is the address of a remote, invisible to the application, cell in which the extension of the formula is written because of the impossibility of simultaneously embedding the number required of calls to the built-in function *IF*, i.e. it is written the following text in the cell with address *address1*:

=IF(address=15;7;IF(address=17;23;IF(address=19; 11;IF(address=21;5;IF(address=23;17;25)))))

4. Breaking the message for encryption into blocks of 3 letters. Each block of three letters (considered as a 3-component vector) is multiplied by the invertible matrix $\boldsymbol{A}$ of size 3×3 again modulo 26 (module **"Encryption"**, worksheets ENC0, ENC1, ENC2, ENC3, ENC4 and ENC5, Fig. 3).

In the module **"Encryption"** by matrix multiplication the encryption of 6-letter English words using the example matrix and each of the five selected valid matrices in the module "Matrix" is done, as previously each 6-letter word is divided into 2 blocks of 3 letters.

The calculation of multiplying the matrix $\boldsymbol{A}$ by the three component vector $\boldsymbol{P}$ containing the part of the plaintext (after transformation of any letter into a number modulo 26 using the simple scheme $A = 0$, $B = 1$, ..., $Z = 25$, Table 1, by using the function *CODE*), is implemented in stages by equation (15) and it is represented by color codes in order to easily assimilation of the material studied by students:

$$\boldsymbol{C} = \boldsymbol{A}.\boldsymbol{P} \Rightarrow \begin{pmatrix} c_1 \\ c_2 \\ c_3 \end{pmatrix} = \begin{pmatrix} a_{11}.p_1 + a_{12}.p_2 + a_{13}.p_3 \\ a_{21}.p_1 + a_{22}.p_2 + a_{23}.p_3 \\ a_{31}.p_1 + a_{32}.p_2 + a_{33}.p_3 \end{pmatrix} \quad (15)$$

As a result of the multiplication of the matrices (performed again in modulo 26) using the relationship (15) the three-component vector $\boldsymbol{C}$ is obtained, which is used for building the ciphertext. The ciphertext is obtained by transformation of the numbers from 0 to 25 in symbols based on Table 1, which is realized in MS EXCEL using the function *=CHAR(address+65)*. The built-in function *CHAR* displays the character with the specified ASCII code, calculated by adding up the decimal number 65 (the ASCII code of the character *A*) and the value stored in the cell, whose address is specified as an argument to the function (*address*).

At the bottom of the module the 6-letter English word for encryption and its equivalent ciphertext are displayed.

Fig. 3 illustrates the operation of the module **"Encryption"** when selected matrix (Option 1) and text for encryption MATRIX.

5. Decrypting the ciphertext – to decrypt the message, each block is multiplied by the inverse matrix of the encryption matrix. The module **"Decryption"** (Fig. 4, worksheets DEC0, DEC1, DEC2, DEC3, DEC4 and DEC5) is analogous to the module "Encryption".

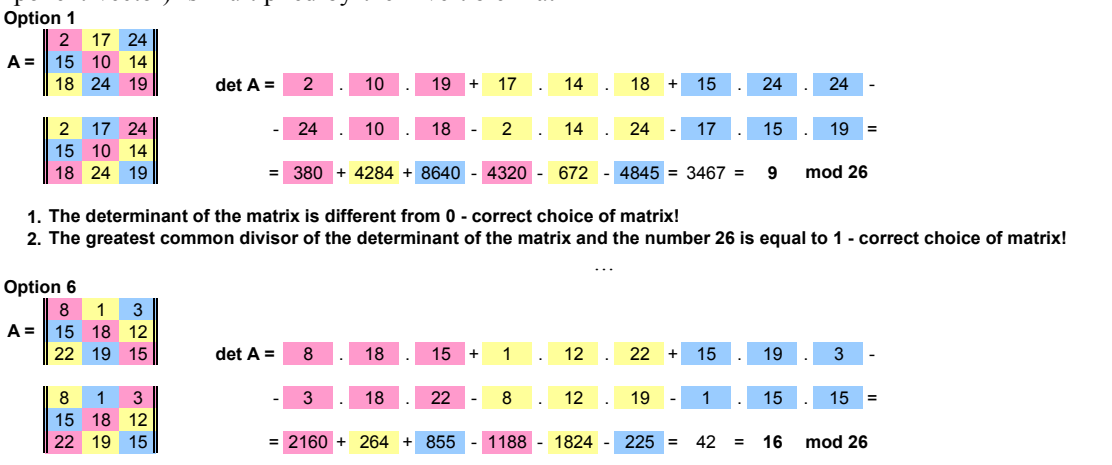

Fig. 1. Illustrating the operation of the module "Matrix" of the application developed

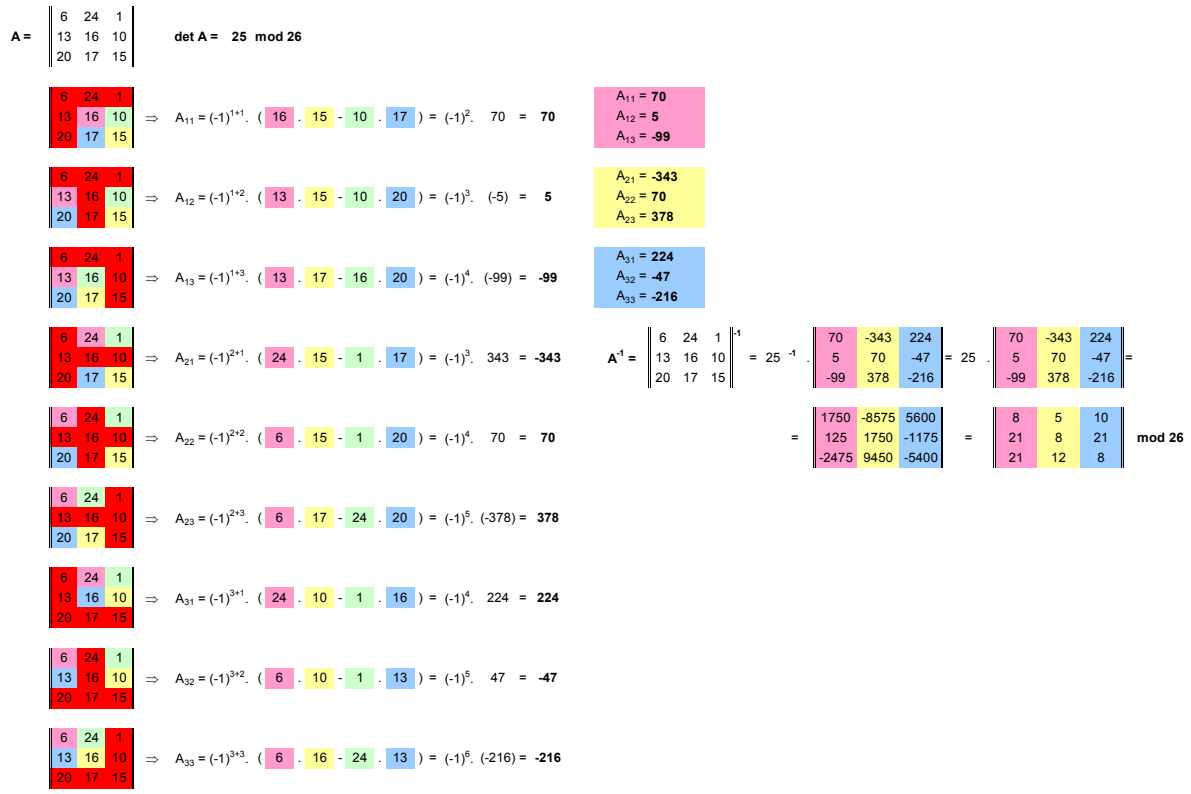

Fig. 2. Illustrating the operation of the module “Inverse matrix”

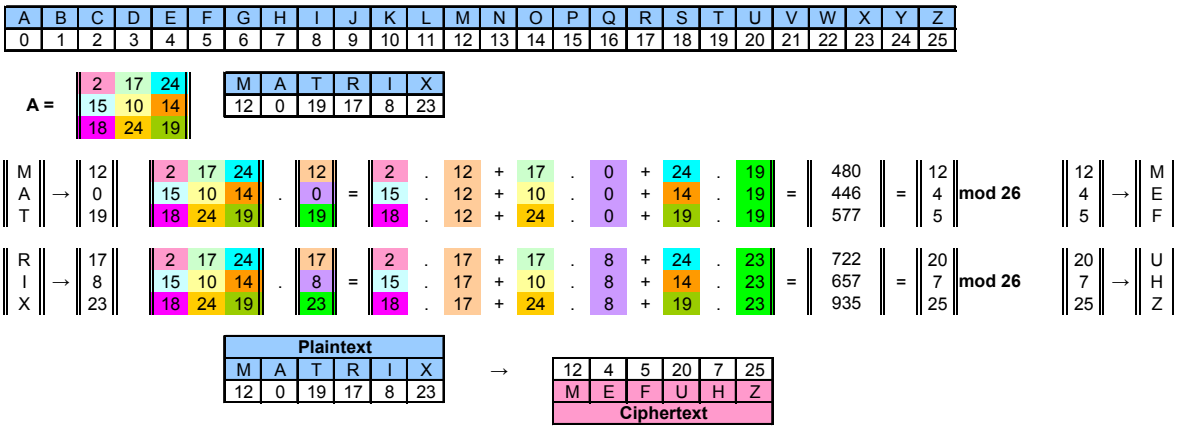

Fig. 3. Illustrating the operation of the module “Encryption” when selected matrix (Option 1) and text for encryption MATRIX

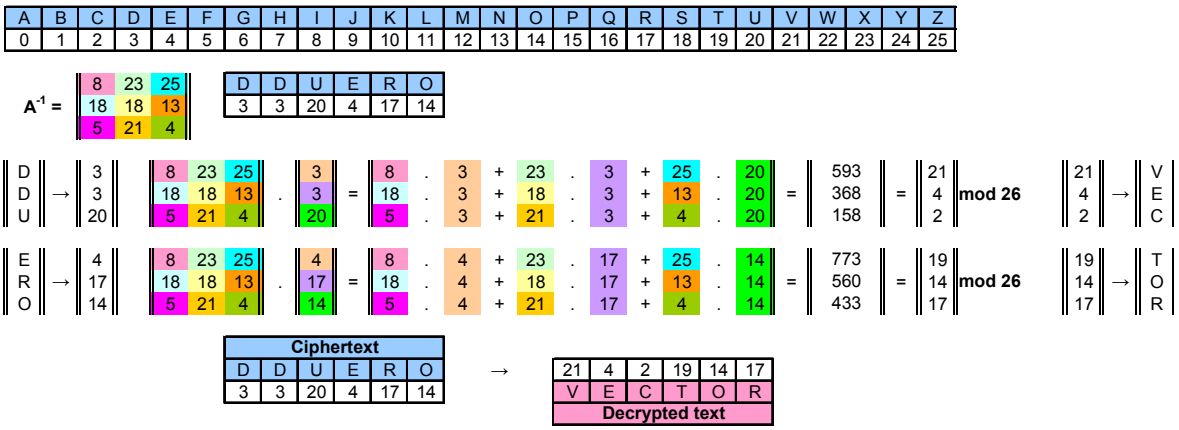

Fig. 4. Illustrating the operation of the module “Decryption” when selected matrix (Option 3) and text for decryption DDUERO

In the module **"Decryption"** (worksheets DEC0, DEC1, DEC2, DEC3, DEC4 and DEC5, Fig. 4) again by matrix multiplication the decryption of 6-letter ciphertexts (from English) is realized using the example matrix and each of the five selected valid matrices in the module "Matrix" and their corresponding inverse matrices calculated in the module "Inverse Matrix" as in advance each 6-letter word is divided into 2 blocks of 3 letters.

The calculation of multiplication of the matrix $\boldsymbol{A}^{-1}$ with the three component vector $\boldsymbol{C}$ containing the part of the ciphertext (after transformation of any letter into a number modulo 26 using Table 1, by the function *CODE*) is implemented in stages by equation (16) and it is represented by color codes in order to easily assimilation of the material studied by students:

$$\boldsymbol{P} = \boldsymbol{A}^{-1}.\boldsymbol{C} \Rightarrow \begin{pmatrix} p_1 \\ p_2 \\ p_3 \end{pmatrix} = \begin{pmatrix} \dot{a}_{11}.c_1 + \dot{a}_{12}.c_2 + \dot{a}_{13}.c_3 \\ \dot{a}_{21}.c_1 + \dot{a}_{22}.c_2 + \dot{a}_{23}.c_3 \\ \dot{a}_{31}.c_1 + \dot{a}_{32}.c_2 + \dot{a}_{33}.c_3 \end{pmatrix} \quad (16)$$

where $\dot{a}_{ij}$ are the elements of the inverse matrix $\boldsymbol{A}^{-1}$.

As a result of the multiplication of the matrices (again performed in modulo 26) by equation (16) the three-component vector $\boldsymbol{P}$ is obtained by which the deciphered text is built. The decrypted text is obtained by transforming the numbers from 0 to 25 in letters based on Table 1.

At the bottom of the module the 6-letter word of the ciphertext and its equivalent decrypted text are displayed.

Fig. 4 illustrates the operation of the module "Decryption" when selected matrix (Option 3) and text for decryption DDUERO.

Results using the MS Excel-based application developed

In the module "Matrix" the sample matrix and 5 valid options and an invalid option for choosing the matrix $\boldsymbol{A}$ of size 3×3 are realized in order to illustrate the reaction of the application in both cases (Fig. 1). In the module "Inverse Matrix" the inverse matrix $\boldsymbol{A}^{-1}$ of the example matrix and each of the five selected matrices in the previous module is determined (Fig. 2). The results are summarized in Table 3.

TABLE 3. SELECTION OF MATRIX $\boldsymbol{A}$ AND ITS INVERSE MATRIX $\boldsymbol{A}^{-1}$

Option	$\boldsymbol{A}$	$\boldsymbol{A}^{-1}$
1	$\begin{pmatrix} 2 & 17 & 24 \\ 15 & 10 & 14 \\ 18 & 24 & 19 \end{pmatrix}$	$\begin{pmatrix} 4 & 5 & 20 \\ 5 & 14 & 8 \\ 20 & 20 & 23 \end{pmatrix}$
2	$\begin{pmatrix} 18 & 24 & 13 \\ 19 & 7 & 4 \\ 23 & 14 & 7 \end{pmatrix}$	$\begin{pmatrix} 17 & 18 & 25 \\ 3 & 19 & 17 \\ 5 & 18 & 24 \end{pmatrix}$
3	$\begin{pmatrix} 15 & 3 & 7 \\ 11 & 5 & 6 \\ 8 & 9 & 12 \end{pmatrix}$	$\begin{pmatrix} 8 & 23 & 25 \\ 18 & 18 & 13 \\ 5 & 21 & 4 \end{pmatrix}$
4	$\begin{pmatrix} 3 & 21 & 1 \\ 11 & 10 & 13 \\ 22 & 18 & 11 \end{pmatrix}$	$\begin{pmatrix} 2 & 7 & 1 \\ 3 & 21 & 8 \\ 10 & 6 & 11 \end{pmatrix}$
5	$\begin{pmatrix} 9 & 11 & 4 \\ 16 & 19 & 13 \\ 23 & 20 & 16 \end{pmatrix}$	$\begin{pmatrix} 4 & 22 & 25 \\ 11 & 0 & 7 \\ 13 & 9 & 9 \end{pmatrix}$

In the module "Encryption" the encryption of 6-letter English words using the example matrix and each of the five selected valid matrices in the module "Matrix" is implemented. The selected 6-letter words in the field of cryptography are *MATRIX*, *CIPHER*, *LETTER*, *COLUMN*, *VECTOR*, *LENGTH*, *STRING*, *MODULO*, *RESULT*, *LINEAR*, *SECRET*, *CAESAR*, *RIVEST*, *SHAMIR*, *METHOD*, *NUMBER*, *SECURE*, *ATTACK*, *THEORY*, *AMOUNT* (Fig. 3). In the module "Decryption" the decryption of 6-letter encrypted English words using the example matrix and each of the five selected valid matrices in the module "Matrix" is realized (Fig. 4). The results of the operation of both modules are summarized in Table 4.

TABLE 4. RESULTS WHEN ENCRYPTION AND DECRYPTION OF ENGLISH TEXTS USING THE APPLICATION DEVELOPED

№	Plaintext (Decrypted text)	Ciphertext (Option 1)	Ciphertext (Option 2)	Ciphertext (Option 3)	Ciphertext (Option 4)	Ciphertext (Option 5)
1	MATRIX	MEFUHZ	VSTRDO	BMMYBQ	DPFIUR	CXIVVJ
2	CIPHER	GITWTZ	HYDBVY	DWICRK	HLPSAX	KPETTT
3	LETTER	ADFURH	VBAJPO	YVOATC	GSDCCB	LFNXDJ
4	COLUMN	MMJKEL	VYHLWR	TCOLUI	ZTBNPT	IZIAPY
5	VECTOR	CTSINN	GTHPHY	DDUERO	TLKEYZ	HWXDLB
6	LENGTH	MXVJOV	VDKFPL	ILUOVR	ASPIJF	NFVFCG
7	STRING	NWLRWY	NXTOHS	EFZTHT	CLPRKI	XMAFLU
8	MODULO	WYLRIG	TAZATK	JMYPVL	VZDTSM	ODGTJU
9	RESULT	OBQHAX	MHBNNT	DDYYZT	XTUYFP	JKFNWW
10	LINEAR	CLNAMF	NFOHOD	UFEXQC	GGJDFP	FDXAZA
11	SECRET	WAQMPJ	EOQZLI	KWWKJK	KEWYGF	GAGNXV
12	CAESAR	WIICOX	KCWZUN	GUMZOK	KWKTDL	IGGWPK
13	RIVEST	YFNQMH	RVAXSJ	KPSNOG	GUVTDX	NVDYDC
14	SHAMIR	ZCYWED	YBSFON	FZZLOI	TICNRX	FFIETG
15	METHOD	CSXMBZ	NUXHJO	NGWMJK	JDZGWX	UVKVBV
16	NUMBER	ERGKHV	MTNXLQ	BDMQDO	DFYAMV	VQHRBL
17	SECURE	WAQJGM	EOQOVY	KWWPRX	KEWFAK	GAGTTG
18	ATTACK	ZOLOEE	BBJWCU	IBJYSI	CVFAUQ	ZKIKMS
19	THEORY	TVOJOY	QKRKNA	WIDNTH	ATQHMU	EVRTBG
20	AMOUNT	UEIPUT	CKGJBV	EOQEJL	GQGOZZ	GUWJIK

III. CONCLUSION

The paper describes one of the classical ciphers – the Hill cipher. MS EXCEL-based application developed for implementing the processes of encryption and decryption of English texts using the Hill cipher based on the matrix of size 3×3 is presented in details.

The material is used in the educational process in the course "Telecommunication Security", compulsory in the curriculum of the specialty "Telecommunication Systems" for the "Bachelor" degree but it can be applied in other courses involving cryptographic methods for information protection. Moreover, the material presents the application of linear algebra (operations with matrices, determinants and number theory) in the field of information and communication technologies, which can enhance the interest of students in studying mathematical courses.

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Intelligent Meaningful Education Process and Targets in Electric Bicycle Design

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Abstract — **the paper emphasizes on the main targets that should be achieved in an intelligent meaningful high quality education process. The main steps of a convenient electric bicycle transport vehicle design are considered, together with some important practical targets that should be taken under consideration during that process. The paper underlines the need for regular complete study of all ecological problems at schools and universities, and contemporary methods for their solution, because each person can contribute both to increase them and to solve them.**

Keywords — **electric bycicle, electric bike, battery, brushless dc motor, quality, education, ecology**

I. INTRODUCTION

The transport is one of the biggest polluters in our world today leading to health problems, climate cataclysms and many other consequences which cost too much to human population. People don't study ecology in schools and universities as a common major and don't really have a clear vision about this matter. If they do, they will acquire on time that understanding that they are not beyond the nature as they think which is an illusion, but a dependable part of it. This way with every little thing they do every day, instead of destroying the nature as they do nowadays, they will promote it and the world will turn in to a paradise for a short period of time. In order this to happened people should understand why it is necessary and how they could help. There is a Bulgarian saying which states that an old wood can not be straighten. This saying means that people should be taught ecology in schools and universities while they are young, that way they will achieve that understanding and acquire the habit not to destroy every living thing around them.

Even if people have respect towards nature which creates a healthful living ambience for them-selves, they will still have many problems to solve. It is not enough to just teach people ecology. In order the education process to be really helpful they should know how they could solve their problems in a matter good for everyone. People should be taught how to live in symbiosis with nature and all matters from all levels of science they study should be practically oriented and connected to real life examples, which will make them understand why they study those majors and will help them apply the acquired knowledge in their lives.

This paper aims to give a common definition of what an intelligent meaningful practical education process should look like. Such a definition is needed in times of changes when education transforms from its traditional form to more interactive and computerized one. Despite of the education form change the main targets for high quality education process are still the same. Another target of this paper is to give an example of how students could be stimulated to study with desire and thus fully involved in a high quality education process. The example consists of ecological problem formulation and the electric bicycles given for partial solution, from which point an actual engineering problem solving could start, for example in the field of power supplies. At the same time, with the example, our practical experience in the field of electric bicycle design for convenient everyday use, which could save money, promote good health and help for the ecology problems solution, is shared.

II. DEFINITION OF AN INTELLIGENT MEANINGFUL PRACTICAL EDUCATION PROCESS

The education methods used nowadays could be divided in two main groups:

- Education oriented towards memorizing information;
- Education oriented towards creativity and understanding of the taught material.

The difference between the two comes from the way the taught material is presented to students, the way the practical exercises are led and the type of exam which they should take at the end of the course.

A. Education Oriented towards Memorizing

In this type of education, generally teachers lead their lecture mostly like speakers talking in front of a public which is supposed to listen. The public which are the students are not really involved in the process because in this way they don't really have to do anything but to listen.

During exercises students generally have to investigate some setups for example and make conclusions. They aren't really pushed to create anything but mostly just to analyze. So

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such kinds of uniform exercises don't really stimulate their creativity.

The exams generally are either tests or a type of exam which requires students to develop some kind of scientific topic. Both types of exams directly require from students mostly to memorize information. In this case students are marked based on the memorized information stated in their work and not on their real understanding and ability to implement the taught material.

This type of education process doesn't stimulate understanding and creativity in students but mostly gives them information about certain matter and could be fairly called lower quality informational education.

B. Education Oriented towards Creativity and Understanding

In this type of education, generally teachers lead their lectures in an interactive mode, making students wonder and ask questions. The teacher emphasizes on the main problems and stimulates students to look for decisions together with him, evolving all of them in the education process and making them an important part of the work. The teacher makes sure that students understand the practical application of the knowledge they receive and why they have to study this matter, which allows students to keep track of where they are in science.

During exercises student's creativity and thinking is stimulated trough practical problem solving. Their task is given in a manner close to real life. Instead of telling them what they have to do step by step, their task is given in a more general manner. For example, instead of telling students measure this, estimate that under those conditions, the task would just say find what is the correlation between those parameters or it could just say, I am a client and I need you to create this and that for me. In this way students are stimulated to think for a way to find the correlation, or to create what ever a real client may want from them. Student should be stimulated to create their own setups either on paper, or in simulation, or in real and then to investigate their behavior.

The exams generally are given as a real life practical tasks which they have to solve. Students are allowed to use any books and information sources they might need. The final goal of the exam is a good solution of the tasks to be created. In this case students are marked based on their skills, understanding, creativity and knowledge. The task, of course, should not be too difficult and the time given should be more than enough.

This type of education process stimulates understanding and creativity and prepares students directly for real life. It could be fairly called a high quality meaningful education process developing human abilities and creating real applicable skills based on understood knowledge.

C. Characterisitcs of the High Quality Education

In order an education process to be meaningful and helpful people should be made to think and solve problems in real time. This will stimulate their mind development and increase their potential. People learn and understand efficiently only trough real experiences. They should face the problems first, then they should have some time to look for a decision them selves and to be stimulated to do so and after that they could be helped with the answer.

There is Bulgarian saying stating that forcefully nothing good happens. In order the education process to be effective students should be stimulated to work willingly against of forcefully making them to do so. They are the main product of education and the whole process should be oriented with respect of the characteristics of their mind. In order this to be achieved students should be given a good motive and answer why they need it. This will involve them and give them purpose to go forward with desire.

So, what are the main characteristics of the high quality education?

- First of all work environment should always be calm and inspiring excluding stress, because it is detrimental for human development. This of course doesn't mean education without laws and rules. There should be a correct to everybody order which should be respected.
- Second, students should understand "Why" they study this matter because this will give them purpose. The teacher should emphasize on real life problems that need to be solved with the science taught and connect them with examples to student's real lives. Students should understand that their help is needed. This way they will face the problems from their point of view and things will become personal for them. Thus, science will come closer to student's hearts and minds and will give them purpose to go forward with desire, which will automatically make the whole education process more effective.
- Third, show students the whole picture. Explain them what they are going to study in general and how this knowledge will help them to achieve a better lifestyles. This will make things even more personal.
- Forth, demonstrate some type of contemporary works, software or technology in an interesting way and explain its application in a way close to student's lives which will help you to grab their attention. Let them try it and touch it. The first impression is very important. This will give students a visual and material appearance of the science they study which will help them concentrate on the future work.
- Structured approach. Once they have a vision of the whole picture and their attention has been won, the big and difficult for solving problem should be broken down to smaller, easier for solving tasks. This way, students can easily keep track where exactly in science they are and what's the real life application of it. This will connect the knowledge from different majors they study into one whole integral knowledge network in their minds and will keep misunderstandings away.
- From this point after, the solving of the small problems could start in a manner orienting the whole education process towards creativity and understanding of the matter. This means students to be involved in the education process in an interactive manner, facing the problems and working together with the teacher towards their appropriate solution.

III. Transport Pollution and Electric Vehicle Facts

This is an example of real life problem which will involve students in the education process and will stimulate them studying with desire. First they should face a real problem and understand how it affects them personally, then they should be informed how important their help is and how they can be part of the solution.

According to briefing of the European Environment Agency (EEA), published February 2015, transport is responsible for 25% of European Union (EU) greenhouse gas emissions and contributes significantly to air pollution, noise and habitat fragmentation. 95% of all kilometers traveled, both passenger and freight, in the EU are powered by oil derived fuels, [1]. Emissions of air pollutants from transport have generally declined over the past two decades, but still around 90% of city dwellers in the EU are exposed to air pollutants at levels deemed harmful to health by the World Health Organization, and transport is a large contributor to this [3,7].

Another EEA report states that the rate of car occupancy continues to decline and in the last years fall down to 1.45 passengers per car, [10]. This practically means that most of the cars are driven with only one passenger in them, which means a lot of pollution for the transportation of only one person.

Electric vehicles (EVs) can reduce urban pollution caused by transport more than 82% if they fully replace the oil derived fuel cars [2]. Battery costs for electric vehicles have dropped by more than 60% since 2009 and at the same time the EV sales for 2015 for EU are from 55% to 78% up [4,5,6]. Despite these facts EVs have still negligible share of the world's transport market.

In previous work, which is in process of publishing, a driving cost evaluation of a converted small electric vehicle has been done. The estimation is for Smart Fortwo, which driving cost, when converted to electric vehicle, would be 2.3 times higher than that with the original gasoline engine. The average citizen even in more developed countries cannot really afford to pay 2.3 times higher driving cost for vehicle with limited range. Another conclusion is that the high cost of batteries is standing in front of the massive spread of electric vehicles today. The problem is that the heavier the vehicle the higher becomes the driving cost and at the same time the lower the weight of the vehicle the lower the driving cost.

IV. Electric Bycicle Could add Value to Peoples Lives

In order students to study with desire, once they have faced the problem, they could be involved in the solution by letting them know how they could be in help.

What people can afford to buy or create them selves are electric bicycles. The most expensive and unaffordable part of all electric vehicles are the batteries, so the lighter the electric vehicle the cheaper the batteries and the cheaper the electric drive system. The bike it-self weights around 20-30 kilograms and the rest is the weight of the rider and its luggage. In previous work it has been calculated that the driving cost of our electric bicycle is €1.3 per 100kms run. More economic motorcycles on the market today consume 1.2 liters gasoline per 100km. If we add the oil change, that makes about the same riding expense.

Taking under account that most of the cars are driven with only one passenger in them [10], which is the driver and this tendency becomes worst with time, every one could help by replacing the car with an electric bicycle for every day use, when the weather is nice of course. In order people to use electric bicycles every day, they need this transport vehicle to become convenient for them. Convenient means:

- The bicycle to be conveniently designed;
- A well practically arranged transportation lane systems to exist;
- A high level of road safety to be assured;
- Bicycle parking spots with either security guard or parking cells where they could be locked in a dry and secure place.

All of the preconditions needed for the bicycle to be used massively, as an alternative transport vehicle during the warm months of the year, can be created only with the help of governments, because it is there job to create them for everyone.

The more people use electric bicycles or just regular ones, as an alternative every day transport vehicle, instead of the dirty cars, the cleaner will become the environment.

The visualization of the studied science is very important. Now the teacher should demonstrate some type of technology and let students even try it, if they could, so they have some real experience in the science field they are going to explore. People learn easy by example. For this purpose an electric bicycle has been created, fig. 1.

Fig. 1. Side view of the created electric bicycle

The electric bike we have created weights around 30 kilograms and the rest is the weight of the rider and its luggage. The full weight, together with a rider and luggage, is from 100 to 110 kg. The minimum motor power in order the vehicle to be able to go up a steep hill by its-self is 1kW for every 100 kg of weight [8,9]. Our bike has a 1kW brushless DC motor integrated into a 26" rim. It is better the motor to be

integrated into 28" rim, which will allow for longer spokes, stronger rim construction and better shock absorption. The integrated motors are with big diameter and the short spokes are one of the weak spots of the electric bicycle. On a flat road it goes with 50km/h and it could make a run of more than 60km. The run could be extended even to 100 km if special manner of riding is applied. The battery is unbranded Chinese LiFePO4 48V/20Ah. The maximum consumed current is limited to 25A. The actual current value varies, depending on the driving conditions. The price of the bicycle, including just the parts and without the work done, is €1200.

In order the bike to be convenient for everyday use it must have at least a front shock-absorber and a seat with springs. In our case this second model has front and back shock absorbers. The back one is not visible, because it is under the battery and controller which are integrated into the frame. If the DC motor is more than 500W it must be back mounted onto an iron bike frame, otherwise if it is in front, the bike might become dangerous for riding. In this case it is better the battery and controller to be in front, so the weight is balanced and the back rim unloaded with 6-7 kg of weight, because it is overcharged anyway. This way the bike riding becomes more stable. A big enough luggage compartment is a must, but it should be specially designed if the frame is with back shock-absorber. The bike should have an ON/OFF switch.

What should be taken under consideration during the electric bicycle design is:

- What's the desired maximum riding speed – for 1kW motor the maximum speed is 50km/h and around 30km/h for 500W motor, for 100kg weight. A 500W motor can not climb a steep hill by itself. Motors with power under 250W have the purpose to help the rider by discharging him.
- What's the desired bike run for one cycle of the battery- in order to roughly calculate the battery capacity, it could be accepted that when the bike goes with maximum speed on a flat road, the motor consumes close to 70%-80% of its maximum power. For over 60kms run with one 1kW of motor power and maximum speed of 50 km/h, a 1kWh of batteries are needed. A 500 W motor would propel the bike with maximum speed of 30km/h, and for 60kms run it will travel 2 hours with 500W energy consumption, so the battery capacity in this case is also 1KWh.
- Front or back wheel mounted motor – motors with power under 500W could be front or back wheel mounted and an iron bike frame is required. Motors with power over 500W must be back-wheel mounted onto an iron bike frame. The wide spread aluminum frames could break and create dangerous situations for the riders.

V. CONCLUSIONS

A high quality education program should have a well-structured approach towards students, who are its main product, and should take under consideration the limitations of the human mind. The whole education process should be arranged in a manner that will make students face adequate real life problems, which will give them experience, studying purpose and stimulus for work with desire, and will make them think. That way they will feel needed and will do their best to succeed and be in help. Education with desire should give better results than forceful education. Once they understand the problems they should be stimulated to work for finding proper solutions. It is very important students to be involved in the education process, to be stimulated to work in real time as equally qualified members of work team, instead of just being observers.

This paper suggests that the electric bicycles are able to help for the partial solution of the ecology problems in urbanized areas where the transport pollution is on a very high level and states some important tips for convenient electric bicycle design which will stimulate its everyday use.

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Control Design Procedure for Prototyping Resonant Converters with Reverse Diodes

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Abstract – **The aim of this paper is to present methodic for the design and verification of a controller for resonant inverter using hardware in the loop configuration. Peculiar to the power electronics converters is that their hardware realization is expensive, consumes significant time and is associated with an existing support infrastructure – powerful mains grid, water cooling with high performance and providing safety measures both for the human and material resources. All this contributes in making the education of power electronics specialists' difficult without the usage of modern tools for evaluation, tuning and diagnostics of the industrial plants.**

Keywords – **Education, Power Electronics, Resonant inverters, Hardware in the loop, Hardware modeling**

I. Introduction

In the field of power electronics the achievement of goals such as conversion with higher efficiency, higher power density with the possibility of components reduction has always been interesting to the designers. Resonant power inverters are receiving renewed interest because of this trend and the potential of these inverters to achieve both higher switching frequencies and lower switching losses. Moreover the design of a controller for such devices has always being a challenge for the designers because of the hazardous parameters related to them – high operating voltages and currents, disastrous consequences when operating in the wrong regime and high cost of repair or renewing of the design. Thus a hybrid evaluation of the combined system converter – controller is necessary. This methods are known as "*Hardware in the loop*" (HIL) and "*Rapid Controller prototyping*" (RCP) depending on which is realized by hardware and which in software. When the evaluated device is designed in software this is called HIL, otherwise when the evaluated controller is in software and the controller in hardware this is RCP. Important aspect of the education is the creation of an analytical model of the examined conversion device, which allows an easy interfacing between the real-world hardware and the studied simulated device. This requirement preconditions for the use of the tools developed and offered by the National Instruments company, which combine the software platform, interfacing hardware and rich set of libraries, developed by other engineers. The main goal of this paper is to focus on the proper description of the power converter in software, which could be used for Hardware in the loop evaluation. The realization of this type of test benches are particularly useful in the field of power train systems [15], engine electronic controls [16], wind and solar generators [5] control system, electric vehicles and many more.

II. Converter Operation

In order to create authentic description of a resonant power inverter, a good understanding of the processes involved in the inverter must be known. On Figure 1 a typical topology of a transistor parallel resonant full-bridge inverter is shown. This configuration has three main parts:

1. Power switches *VS1* to *VS4*, which are usually MOSFETs with parasitic reverse diodes, are configured to form a square-wave generator. This generator produces a bipolar square-wave voltage U_p, by alternating switch pairs *VS1, VS3* and *VS2, Vs4* with almost 50% duty cycle. A small dead time is needed between the consecutive transitions, both to prevent the possibility of cross conduction and to allow time for zero-voltage switching (ZVS) to be achieved.
2. The resonant circuit, also called a resonant network, is composed from the resonant inductance L_r, load inductor with parameters R_T and L_T, and load capacitor C_T. Particularly this circuit can be viewed as composition of two resonances – parallel one composed from the R_T, L_T and C_T, and serial formed by L_r and the equivalent capacitance Z_{CT} of the parallel resonant tank. A basis for this assumed transformation is given by the specific appliance of the inverter – for induction heating, where the resistance of the inductor is way too less than its inductance.
3. The analytical schematic can operate in two main regimes with switching frequency above and under resonance of the series tank. In the transistor circuits the preferred regime is above resonance frequency, because this way can be realized the zero-voltage switching (ZVS) which leads to lower losses.

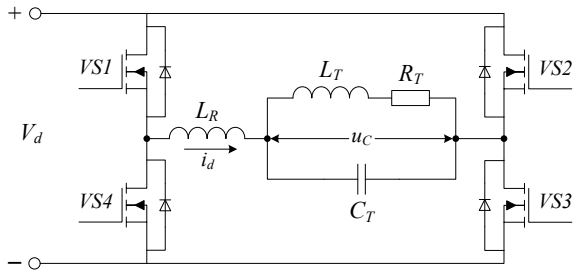

Fig. 1. Full-bridge parallel resonant converter schematic

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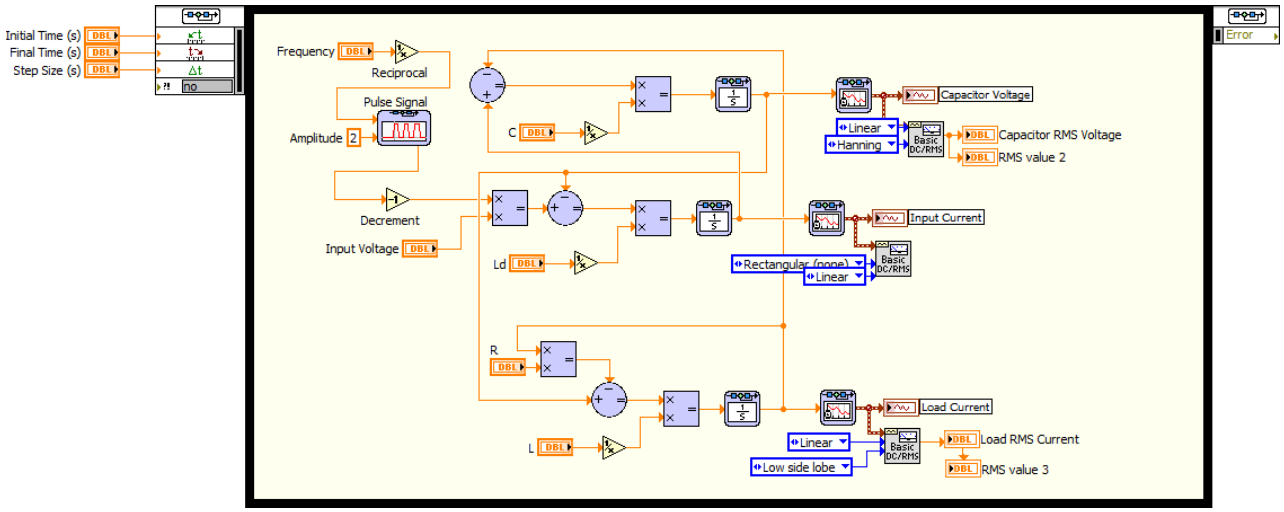

Fig. 2. LabVIEW Block diagram of the program

Fundamentally, the series resonant network of a resonance inverter with reverse diodes presents a minimum impedance to the sinusoidal current at the resonant frequency – this is sometimes called the resonant circuit's selective property. Away from resonance, the circuit presents higher impedance levels. The amount of current, or associated energy, to be circulated and delivered to the load is then mainly dependent upon the value of the resonant circuit's impedance at that frequency for a given load impedance. As the frequency of the square-wave generator is varied, the resonant circuit's impedance varies to control that portion of energy delivered to the load.

III. MODELLING

In order to prepare a Hardware-in-the-loop or Rapid controller prototype test set up a good understanding in the underlying processes in the devices is required. Thus an authentic model which trustworthy forms the output variables, based on the input influences is required. For the creation of the model are used in conjunction the methods of the instantaneous values, switching functions and the state variables [3, 4]. From the circuit operation is known that in transient and steady state operation there are two intercommutation intervals, which are formed from the sequential operation of two transistors and their reverse diodes. Depending on the operating mode – under or above resonance – the difference is in the conduction sequence. The created model allows the examination of the electro-thermal converter in wide changes of the operating frequency.

In the description of the model the method of the state variables [1, 2, 8, 11] will be used. The switching function is given as following:

$$F(\omega t) = \begin{cases} +1 \\ -1 \end{cases} \tag{1}$$

Since the reactive elements of the circuits are three (L_r, L_T and C_T) the system of differential equations will be of third order. Also it is assumed an ideal voltage source, supplying the input of the inverter. It is presented in generalized form for the two intercommutational intervals. It will have the following description:

$$\begin{cases} \dfrac{du_C}{dt} = \dfrac{1}{C_T}\left(i_{Lr} - i_{L_T}\right) \\ \dfrac{di_{L_T}}{dt} = \dfrac{1}{L_T}\left(u_C - R \cdot i_{L_T}\right) \\ \dfrac{di_{L_r}}{dt} = \dfrac{1}{L_r}\left(F(\omega t) \cdot U_d - u_C\right) \end{cases} \tag{2}$$

A resonant inverter is designed using the method of the first harmonic approximation (FHA), given in literature source [1, 3], using the following desired inverter specifications:

- Input Voltage $U_d = 300$ V
- Operating frequency $f = 10$ kHz
- Output voltage RMS value $U_T = 450$ V
- Load power factor $\cos(\varphi_T) = 0.2$

For a complete study of the processes in the converter are given designs for both above and under resonance frequency.

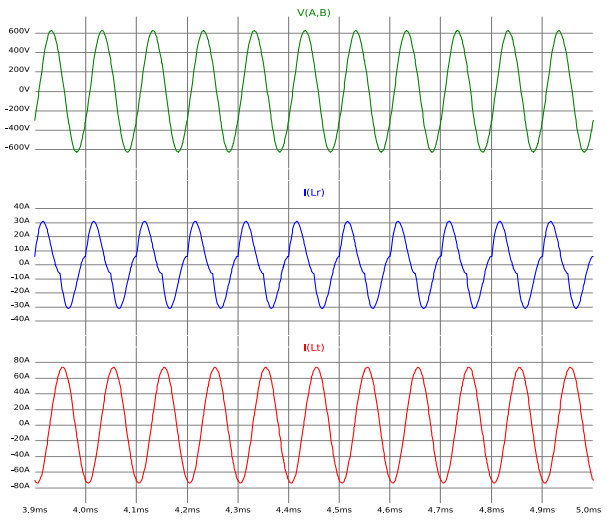

Fig. 3. LTSpice waveforms

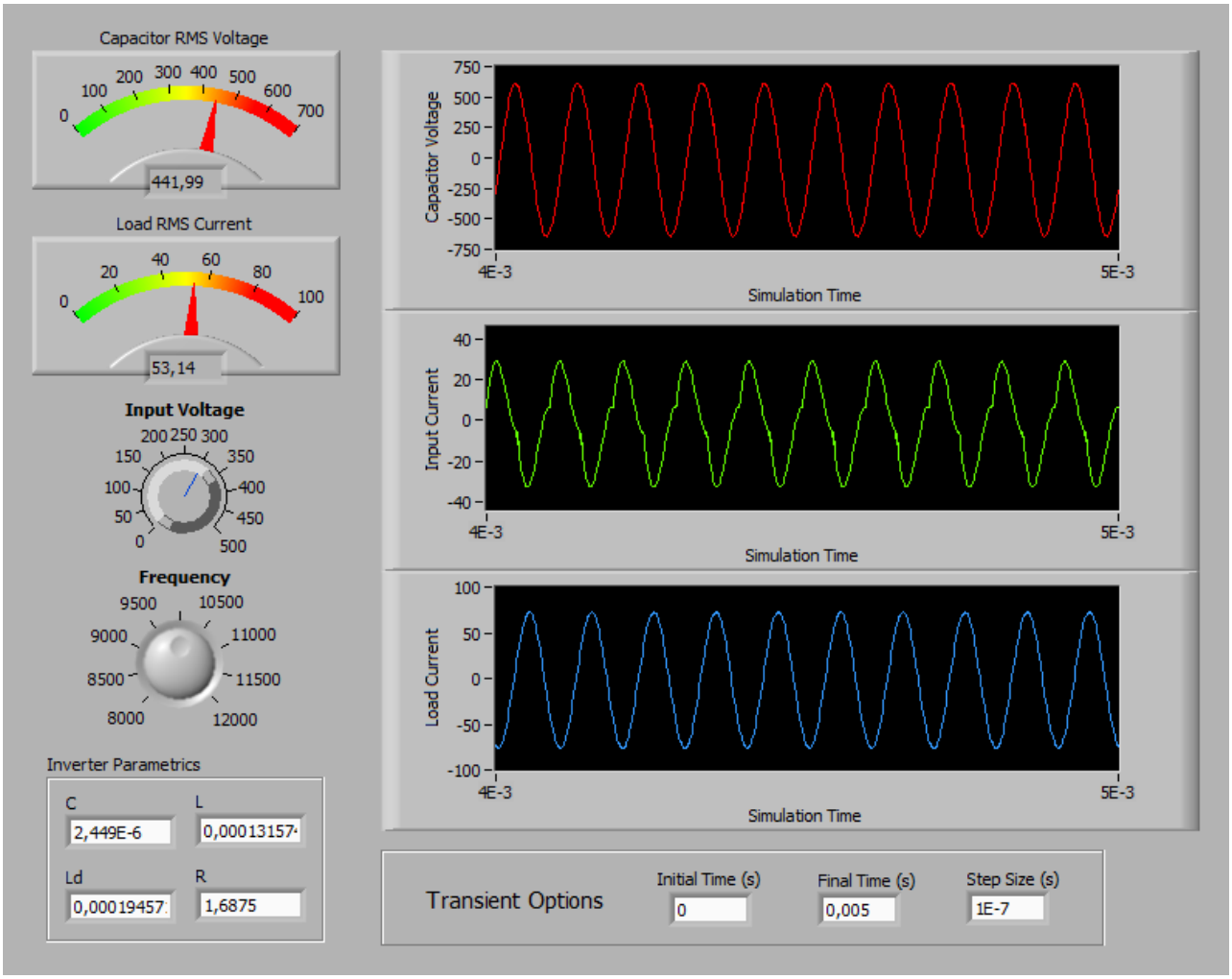

Fig. 4. LabVIEW Front Panel of the program, displaying below resonance operation

A. Operating under resonant frequency

The values of the elements in hot regime (after passing the Curie temperature) are [1, 2]:

- Capacitor capacitance C_T = 2,449 μF
- Resonance inductance L_r = 194,5713 μH
- Load inductor L_T = 131,57384 μH
- Load resistance R_T = 1,6875 Ω

These values are entered in the realized LabVIEW program with a block diagram shown on figure 2. The results of the study along with the set specifications are visualized on the front panel, shown on figure 4. Indicators are placed for quick observation of the main values of the industrial converter. With their aid the user can easily check whether he has correctly calculated and designed the power circuit.

The model is verified with the specialized CAD simulation software LTSpice®. The results for comparison are shown on fig. 3 and can be observed a very good concurrence (difference below 2%).

B. Operating above resonant frequency

A design for above resonance operation is calculated using the same inverter specifications. The only difference between the values in the different regimes is the resonant inductance L_r = 324,115μH. Results of the investigation is shown on figure 5. The results of the operation of this regime are verified. Again, there is a good concurrence between the simulations and the modeling.

IV. Conclusions

The usage of LabVIEW allows during the training of employees, specialists and developers to advance their skills and knowledge in an accessible and flexible way. In LabVIEW there aren't accompanying risks both for the employee safety and also for the executive board, which have invested significant resources for the creation and development of given production factory.

The work proposes the usage of the visual programming for the modeling needs of power electronic converters. A successful verification of the model is conducted.

A consideration for future model expansion is to be developed by adding the change of load parameters during real technological process. In this case will be used regulator for maintaining of the specified output parameters using the appropriate feedback.

Using the developed hardware for data acquisition and signal generation from the National Instruments Company,

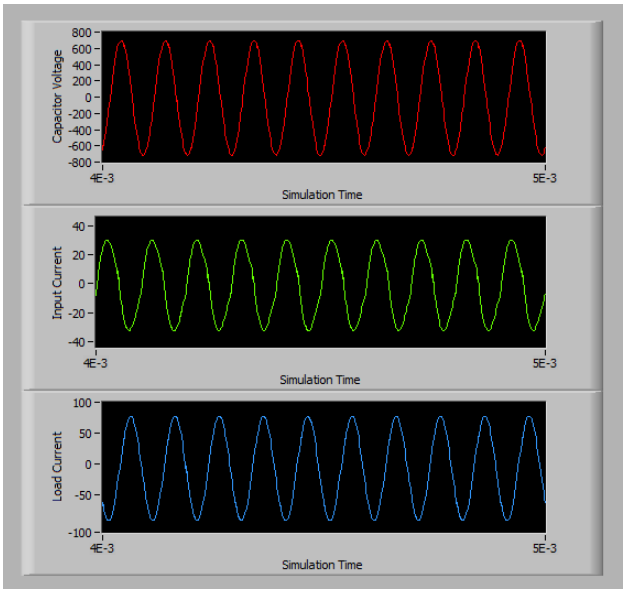

Fig. 5. Above resonance operation waveforms

the test set-up can be expanded even further into Hardware in the loop or Rapid Controller prototyping test bench.

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Development and Implementation of Digital Phase Locked Loop on Xilinx FPGA

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Abstract – **The subject of the article is development and an implementation of a digital Phase Locked Loop on programmable logic devices from the FPGA XILINX family. The synthesized structural diagram includes 4 MHz reference crystal oscillator, frequency pre-divider, phase frequency detector, digital filter, digitally controlled oscillator and programmable frequency divider. Different types of phase frequency detectors are developed and tested as well as different solutions for digitally controlled oscillators and programmable frequency dividers. The synchronization time, the phase jitter and the overall stability are tested for each individual configuration and different frequency relations.**

Keywords – **Digital Phase Locked Loop, Digitally Controlled Oscillator, Phase Frequency Detector, Digital Filter, Programmable Frequency Divider, FPGA.**

I. Introduction

The phase synchronizers are widely used in today's electronics for generating signals with different random frequencies from a single reference crystal oscillator where the stability of the generated frequencies is equal to that of the reference oscillator. That gives flexibility for user configurable frequency with a defined step. The traditional analog Phase Locked Loops (PLL) have significant drawbacks as slow synchronization when starting and expensive components for the Voltage Controlled Oscillator (VCO) and the filter [1]. Therefore the completely digital type of PLL is preferred.

The VCO is replaced by Digitally Controlled Oscillator (DCO) and the analog filter is replaced with a digital one. The digital PLL also maintains a fixed phase difference but due to the discrete frequency step of the DCO, there is uncertainty of the phase. For that reason sometimes the digital PLL is called Frequency Locked Loop (FLL) [2]. The FLL has a number of advantages over the standard analog PLL:

– completely digital design – everything except the reference oscillator is implemented on the chip;
– high synchronization speed even when the DCO frequency is far from the desired;
– longer service life – less aging components

The FLL is implemented on a Field-Programmable Gate Array (FPGA) integrated circuit of Xilinx Spartan-3A family.

The FPGA logic devices are used to implement any logical function.

A Hardware Description Language (HDL) or logical diagrams are used for configuring of the FPGA.

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II. Structure of the Frequency Locked Loop

The structural diagram of the Frequency Locked Loop is represented on Fig. 1. The reference frequency from the 4 MHz crystal oscillator is applied directly to the FPGA to be divided by the frequency divider *M*, defining the desired frequency step. The frequency is then applied to the *Fi* input of the phase frequency detector. The output signal from the DCO is divided by the programmable frequency divider *N* and is applied to the F_0 input of the detector.

The phase frequency detector generates two signals indicating the difference in phase and frequency [3]. These two signals are applied to the digital integrator along with a clock signal. The digital integrator generates the *16 bit* digital code *F* controlling the DCO. The output frequency of the DCO equals the frequency step *Fi* multiplied by the coefficient *N*. The DCO consists of external 16 MHz RC oscillator and a *16 bit* programmable frequency divider.

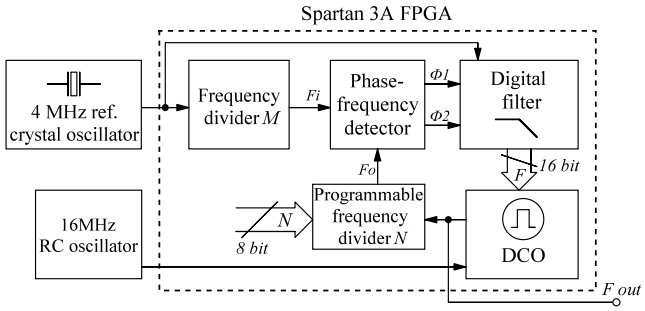

Fig. 1. Frequency Locked Loop structural diagram

III. Structure of the Digitally Controlled Oscillator

The first examined version of the DCO consists of a programmable frequency divider. Its logical diagram is represented on Fig. 2. The programmable frequency divider is built using one *16 bit* reversible parallel loadable binary counter and a T-type flip-flop. The counter is permanently configured for counting down and the Terminal Count (TC) output is connected with the synchronous load input PL. Every time, when the counter reaches zero, TC goes high and the next clock pulse loads the counter with the value *F* applied to the parallel load inputs. Then the process of counting down starts again. The TC signal is also connected to the T input of the flip-flop so every time the counter loads the *F* number, the flip-flop toggles its output level.

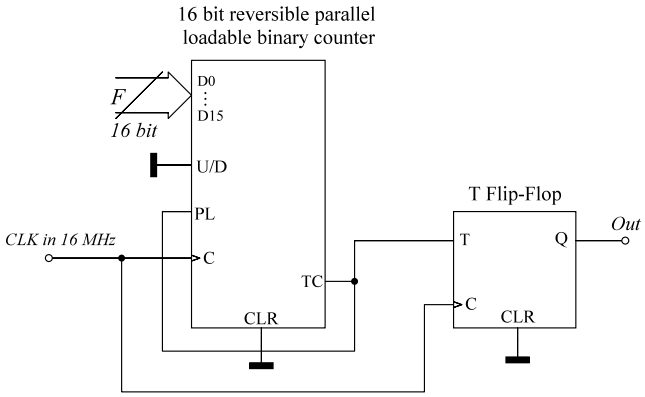

Fig. 2. Logical diagram of the programmable frequency divider for the first DCO version.

The output signal of the DCO is square wave signal with 50% duty cycle and frequency given by the Eq. (1):

$$F_{out} = \frac{F_{in}}{2(1+F)} \tag{1}$$

The range of the output frequencies when using 16 MHz input clock signal is from 122 Hz to 8 MHz with period step of 250 ns. The usable frequency range with reasonably small frequency step is up to about 100 kHz [2].

This configuration is simple and effective but has a drawback. If the frequency has to be changed from low to high value quickly, the value of *F* applied to the parallel load inputs of the counter is changed, but the counter will continue the countdown until it reaches zero and the new value is loaded. So the worst case delay of the frequency change is half period of the lower frequency. This can be a problem when a quick and relatively large frequency jump is required and can lead to problems with synchronization. Due to that reason a second version of the programmable frequency divider is developed. The structural diagram is represented on Fig. 3:

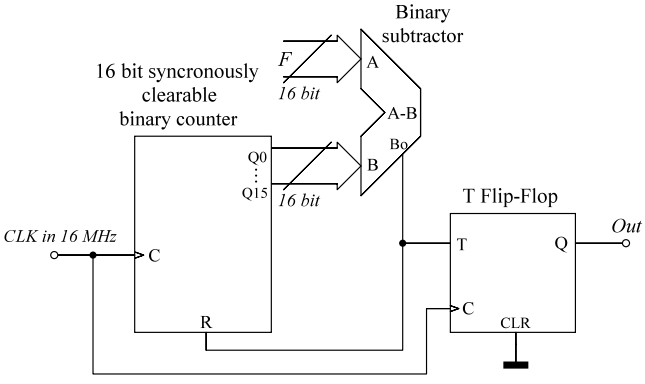

Fig. 3. Structural diagram of the programmable frequency divider for the second DCO version.

The structure includes a standard synchronously clearable *16 bit* binary UP counter, *16 bit* binary subtractor and a T-type flip-flop. The *16 bit* value *F* is connected to the A input of the subtractor, and the *16 bit* output of the binary counter is connected to the B input. The subtractor performs A-B and outputs the difference and the borrow signal [4]. The difference is not used while the borrow signal is connected to the synchronous clear input of the counter and the T input of the flip-flop. The counter increments on every clock cycle of the input signal. Once it exceeds the number F, the borrow output of the subtractor goes high and on the next clock cycle the counter resets to zero and starts to count up again. At the same time the T-type flip-flop toggles its output level. The resulting frequency is given by the Eq. (2):

$$F_{out} = \frac{F_{in}}{2(2+F)} \tag{2}$$

The operation is almost equivalent to that of the previous divider. The frequency range is slightly different from 122 Hz to 4 MHz with the same period step of 250 ns. The reaction to step frequency change from low-to-high in this case is faster. When the number *F* is changed with its new value lower than the previous and the counter has reached a higher value, the borrow output goes high immediately and resets the counter. In this case the change in frequency happens with worst case delay of half period of the higher frequency. This reduces significantly the response time of the DCO to large frequency steps and makes the FLL operation more stable.

IV. Structure of the Phase Frequency Detector and Digital Loop Filter

There are different topologies for phase detectors with different phase angle ranges in which they produce linear output. Most of them has periodical phase-to-voltage response with 180º period and they are not sensitive to frequency differences [3]. That is why they are only applicable when the DCO frequency range is narrow.

The startup process within large range of frequency differences is difficult and can lead to false synchronization to a harmonic frequency. Due to this fact in the FLL a phase frequency detector is used. This type of detector indicates not only the phase difference but also the difference of the frequencies [3]. This allows the FLL to lock successfully at the exact frequency and phase from random DCO frequency at the startup.

The phase frequency detector will be examined along with the digital filter. The combination of the two modules generates the control code *F* for the DCO based on the difference in frequency and phase of the two input signals. The digital filter in this case is digital integrator built with a reversible *16 bit* binary counter [5].

The logical diagram of the phase frequency detector with the integrator is shown on Fig. 4. The phase frequency detector consists of two D-type flip-flops (**A** and **B**) with permanent logical "1" applied to the D inputs and common asynchronous reset signal [3]. The two signals to be compared are applied to the clock inputs of the two flip-flops. When one of the flip-flops receives a rising edge on its clock input, the corresponding Q output goes high. The high level through the XOR gate goes to the Count Enable (CE) input of the counter and it starts counting [6]. This state continues until the other flip-flop receives rising edge and sets its Q output in logical "1". With both Q outputs in

high state the AND gate generates logical "1" at its output which quickly resets both flip-flops. In this configuration the two flip-flops can be both in logical "1" for just about 20 ns as this is the time needed for asynchronous reset. This could theoretically lead to 1 count error in the digital integrator every cycle. This error is eliminated by combining the Q outputs through XOR gate which excludes the short time in which both outputs are high.

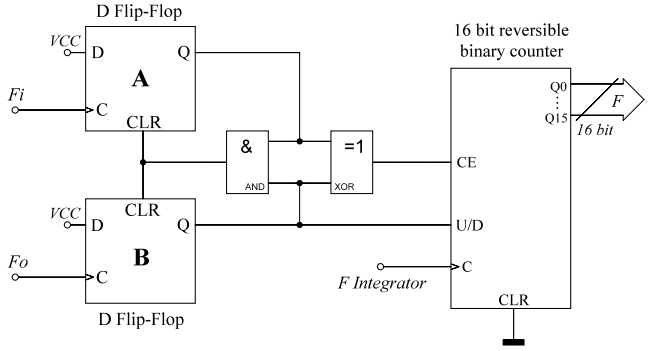

Fig. 4. Logical diagram of the phase frequency detector with digital integrator.

The direction of counting UP or DOWN depends on that which of the two flip-flops has been triggered first. The UP/DOWN signal for the counter is taken from the Q output of flip-flop **B**. If F_0 is leading F_i the **B** flip-flop will be triggered first and the counter will count n pulses in UP direction until the **A** flip-flop is triggered and the structure returns to its initial state. This will systematically increase the value F which will decrease the DCO frequency until the zero phase difference is restored.

The opposite thing happens if F_i is leading F_0. In this case the **A** flip-flop is triggered first and the counter counts n pulses in DOWN direction. The value F is decreased to restore the zero phase difference.

The amount of pulses which the digital integrator will accumulate for a period of time is dependent on its clock frequency *F integrator*. This frequency is equivalent to the time constant τ of the RC circuit in the analog filter in an analog PLL and the stability of the system depends on it [6]. The main consideration when choosing this frequency is that its period should be equal or greater than the period step of the DCO. In this case *F integrator* should be less than 4 MHz.

This type of phase frequency detector is insensitive to the duty cycle of the signal as it is edge triggered [3]. It has a simple construction and high speed of synchronization as an advantage but has higher instability when implemented in the FPGA architecture especially with higher values of frequency multiplication N. It is also sensitive to the clock signals routing [5]. A good stability in wide frequency range cannot be achieved without changing *F integrator*. The need of adaptive changing of this frequency makes the circuit more complex.

The second version of the phase frequency detector which is examined consists of two *16 bit* binary counters and a *16 bit* subtractor. This detector acts as phase frequency comparator and digital integrator in the same time. Its logical diagram is shown on Fig. 5. The principle of operation is the following. The two frequencies F_0 and F_i are applied to the clock inputs of the two counters. Every counter counts up with the frequency of the signal. The outputs of the two counters are subtracted from one another by the binary subtractor. The difference between them is used to control the frequency of the DCO. If one of the compared frequencies is higher than the other, the corresponding counter is running ahead of the other and the difference between them increases or decreases which changes the DCO frequency. For example if F_i is running faster than F_0 the difference A-B at the output of the subtractor will decrease. This will increase the frequency of the DCO along with F_0 frequency until the same frequency as the reference F_i is achieved.

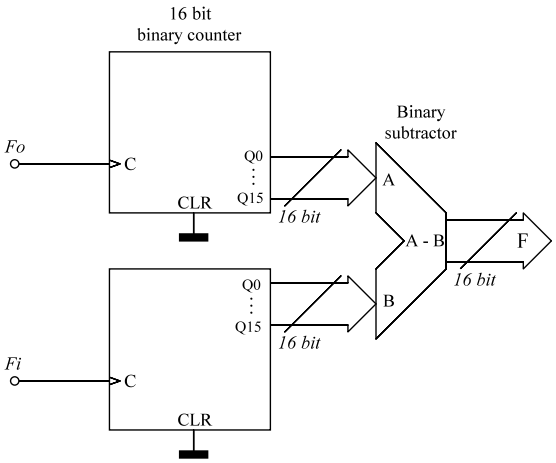

Fig. 5. Logical diagram of the phase frequency detector with counters and subtractor.

This phase frequency detector has very wide linear phase range within 65536 cycles. Unlike the first examined version, this detector is not of the integrating type. For example with a constant phase difference between the two signals F_0 and F_i the first detector will continuously increment the value F while the second version outputs a constant value depending on the difference in the number of cycles. A system built with the integrating detector will maintain a zero phase difference while with the non-integrating type it will maintain a constant phase difference. The advantage of this solution is the extreme stability of the FLL over almost the whole frequency range even at high F_{out} to F_i ratios. The drawbacks are the higher phase uncertainty and the very low synchronization speed at low F_{out} frequency.

V. Experimental results

The implementation of the digital frequency locked loop on the FPGA chip shows good results as expected. The design is purely digital with no analog components. The frequency stability of the output signal is the same as the stability of the reference crystal oscillator. The main factor which determines the stability of the system is the phase frequency detector and the digital filter solution. The different concepts are giving completely different results as frequency and phase stability and synchronization speed. The logical diagram of the implementation is shown on Fig. 6.

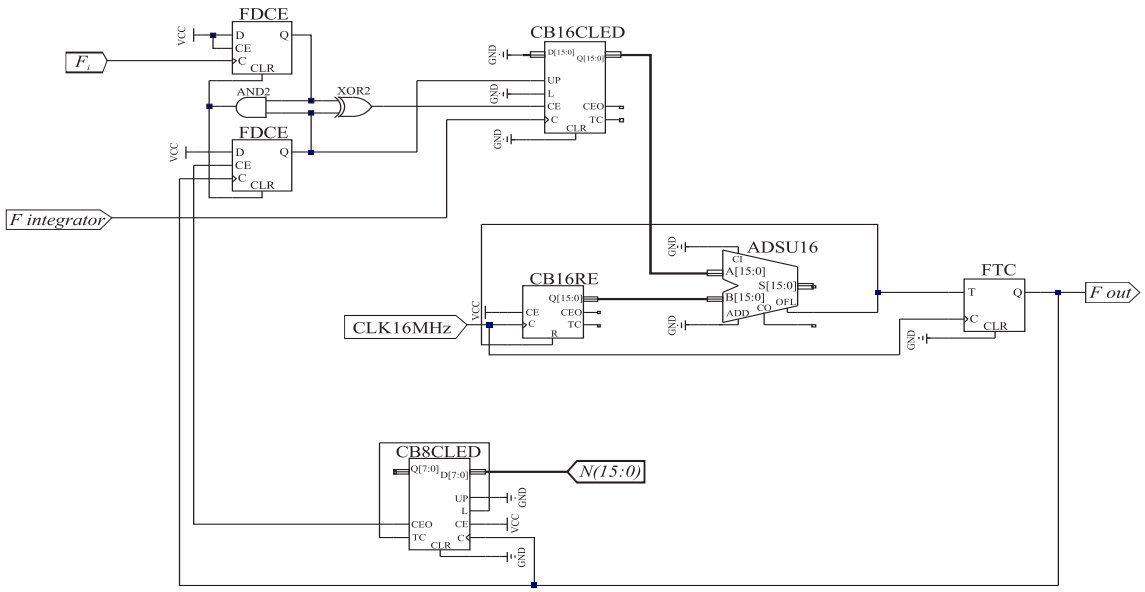

Fig. 6. Logical diagram of the digital FLL implementation

The first examined version of the detector with the two flip-flops is sensitive to the clock signal routing into the FPGA and in some configurations especially when the clock inputs of the triggers are connected to combinational pins there are problems with the synchronization. In some cases the system unlocks periodically at random intervals from 5 to 15 seconds and locks again which results in output signal frequency disturbance. The partial solution to this problem is to feed the clock pins only from clock dedicated signals and no combinational outputs. In this case the CE pins of the counters and the flip-flops are used. The sensitivity to the clock routing is still a big factor in performance with this type of detector and filter.

The second examined version of the phase frequency detector with the two counters and subtractor is very stable and insensitive to the clock signals routing but has a very low synchronization speed.

The direction for further development and achieving better performance is using the best from the two concepts. A hybrid detector is developed in which the most significant *12 bits* are generated from the fast counter integrator while the least significant *4 bits* are generated from the detector with two counters and subtractor. It can be analyzed as fast integrator with dead zone in which the other detector is active. This is going to achieve the stability of the second detector and the high synchronization speed of the first one.

VI. Conclusion

The completely digital PLL gives a good and flexible solution to clock signal generation problems in digital systems. It is a good alternative to the analog PLL with comparable phase jitter and much higher synchronization speed. It is good for systems which are turned on and off frequently or when the frequency is changed often. The absence of external parts and analog stages makes the design more reliable and stable in time. The capacitors and the analog integrated circuits in the analog filter and VCO of the standard PLL are expensive and reduce the reliability of the whole design. It is better alternative to direct digital synthesis as well, when a square wave signal is needed due to the greater simplicity of the method.

If the FLL is made adaptive it can achieve excellent performance and stability in very large frequency range.

If the DCO input clock frequency is high enough, the output period step is so small that the phase uncertainty is almost equal to that of analog PLL system.

Acknowledgements

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Statement-level Energy Simulation in Embedded Systems Using GCC

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Abstract – **The following paper discusses energy simulation of C programs in embedded systems. An Instruction Set Simulator (ISS) has been implemented for early code analysis that will help software developers in optimizing their programs in terms of energy consumption. The ISS is called Powot Simulator and performs timeless code simulation by assigning each assembler instruction a base energy cost and grouping instructions together to represent each statement of C code. This tool depends heavily on the GNU Compiler Collection (GCC) toolchain and a custom energy model of the target microprocessor.**

Keywords – **energy simulation, instruction set simulator, energy optimization, embedded systems**

I. Introduction

Embedded software developers often write code that works in battery-backed devices or eco-friendly equipment. Usually they finalize their code, measure its execution time and power consumption, and try to anticipate battery life with the acquired data. They have no preliminary knowledge of what the results might be, because they write code at high levels of abstraction. Even if any assembly analysis is done, it can only estimate time performance, as long as data dependency is not involved. That is why several energy/time simulators have been developed like gem5, Simple Power, Wattch, etc. In this paper a new one is proposed called Powot Simulator. It is an Instruction Set Simulator that was first introduced in [1] and did energy estimations on a C function-level basis. This approach, however, yields results that can be erroneous due to dependency of function's code on input data. Version 2 of the simulator addresses this problem – by analyzing code on a statement-level basis one can achieve better energy estimates and localize the power-hungry sections of code. This could aid optimizations at the early stages of firmware development.

II. Related Work

In [2] a statement-level energy analysis is presented. The consumed energy is divided in two components – energy consumed by C operators and energy consumed by C control statements. An ARM9TDMI microprocessor has been modeled. The validation of the results is done with the help of a third-party ISS. The errors do not exceed 11 %. The model parameters are very close to the ones present in this paper – effects of instruction parameters like data location and size, base energy cost of a single instruction, and operator-level parameters like number of times each operator is executed.

Authors in [3] propose an interesting method for simulation by using Virtual Instruction Set (VIS). This helps raising the level of abstraction and makes simulations universal. Of course, bigger errors in the output results are introduced. An important thing to note is that the data dependency problem is solved by inputting typical data for the benchmark under test.

The work presented in [4] tries to estimate energy consumption in nested loop programs depending on the mapping of each loop to a dedicated processor array. According to the authors, optimal mappings could be achieved when some data remains unchanged over a certain period of time.

It is worth noting the work in [5] that presents statement-level timing estimation. The model in [5] is relevant because energy simulation depends on timing. The authors divide a C program in a set of small, elementary components that are called atoms. No absolute timing is used, only the relative cycles per instruction (CPI). A set of benchmarks is evaluated. An average of 3-4 % error is introduced.

The work in [6] tries to combine the fast simulation time of high-level static analysis of code with the accuracy of low-level dynamic analysis. The simulator is supplied with a set of mathematical models. The link between the abstraction levels is done with a pseudo instruction set, just like in [3], whose instructions are grouped in sequences called Kernel Instruction Set (KIS).

III. Statement-Level Instruction Set Simulator

According to [7], the Electronic System Level (ESL) design flow starts with functional description of the system and then descends to architectural and pipeline-accurate architectural levels. The latter two include a well-defined instruction set of the processing elements, therefore a simulator that operates on architectural level is called instruction set simulator (ISS).

The proposed simulator in this paper, Powot Simulator v.2, is an ISS that has no other information than the instruction set of a microprocessor and a model that assigns base energy costs to each instruction. In [8] a definition to the term "base energy cost" is given as the energy consumed by the basic processing elements that are activated for a non-overlapping execution of an instruction.

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```
1  void function_one(void){                    ∑E = ?
2      int a, b, c, choice;                    002 nJ
3   choice = function_two(&a, &b, &c);         500 nJ
4      switch(choice){                         030 nJ
5      case 1:                                 005 nJ
6    a *= a;                                   015 nJ
7          break;
8      case 2:                                 005 nJ
9    a = (a * b) + c;                          050 nJ
10         break;
11   }
12 }                                           005 nJ
```

Fig. 1. Example of data dependency in a C program

A. Fighting Data Dependency

There are two existing methods for dealing with data dependency: inputting values to the simulation environment, which then passes them to the tested application (e.g. the gem5 [9] simulator's emulated Linux terminal), and connecting the simulator to real hardware (like MATLAB's connection to development kits). A new method is proposed in this paper – simulate energy on a statement-level basis to aid the software developer (or an optimization tool) while writing the code.

Consider the case shown in Fig. 1. If we analyze code at function level, we would sum all of the energy values on each line inside function_one( ) and get the result 612 nJ. But executing the application would take either case 1 or 2 and not both. In the first case we would get 557 nJ and in the second 592 nJ. In both cases a data dependency error is introduced and the reason for this is line three. If we change the approach and analyze this code at statement-level, we can make comparison between different statements, e.g. "a *= a;" and "a = a*a". Currently there's no way for the programmer to tell which one is more energy-efficient or whether there's any difference at all. This is where the ISS may help by exposing statement energy to the developer.

B. Conditional Instructions and Hamming Distance

Statement-level analysis is not a straight forward method. Not always can one tell that the energy cost of a statement is constant due to the presence of conditional instructions. One such example is the ARM IT block. It can include up to four instructions inside it that will be executed if a condition is met (Fig.2). This would yield different energy results because the instructions might have different base energy costs. Hamming distance of operands, on the other hand, may also alter the base energy cost of an instruction. This leads to small, statement-level data dependency that theoretically might have negative impact. Changing an operand from 0x00 to 0xFF would lead to eight zero-to-one gate-level transitions, while 0x00 to 0x55 would lead to half of that. Nevertheless those problems are neglected in the present work and the experiment is carried out.

```
ITTE    NE          If NE flag is set
ANDNE   r0, r0, r1  then r0 = r0 & r1
ADDSNE  r0, r0, r1  then r0 = r0 + r1
MOVEQ   r0, r1      else r0 = r1
```

Fig. 2. ARM conditional instruction

C. Microprocessor ISA energy model

The model is a tab-separated text file that contains energy profiles for all microprocessor instructions. Each profile includes energy values for different conditions of execution, or domains. For example, an instruction may have one value for the 10-Megahertz clock domain and completely different value for the 80-Megahertz. More information about the model itself, as well as measuring model data, can be found in [10].

IV. ISS Modules and Features

The proposed instruction set simulator has been implemented under Linux. Qt Creator development environment has been used. Qt provides a rich set of cross-platform C++ classes that ease programming and will allow porting the simulator to Windows and Mac OS. The Powot Simulator v2 project builds a shared object library (libpowot_simulator.so) that could be part of a bigger development environment. A block diagram of the ISS is shown in Fig. 3. The input is the linked object file of the firmware that must not contain multi-threading and OS. So far, only single core microprocessors are supported. The object is passed to the block "External tool invoke" that invokes three programs from the GCC toolchain: gdb (debugger), nm (list symbols in file) and objdump (display disassembly). The simulator relies on the output of those programs entirely and cannot work without them.

The simulator descends in the function call tree of the program down to the last function that contains no user API calls. Consequent simulator blocks are invoked in this process also. Special function calls are distinguished with the help of the microprocessor's energy file. In it there is a list with all the special APIs and the corresponding changes they make to the system, e.g. dfs(10); changes system clock to 10 MHz, dvs(1.8); changes system voltage to 1.8 V. The block, called "Assign instruction base energy", is the core of the simulator. Each instruction is assigned a base energy cost from the model file. Grouping of assembly instructions and summing their base energies will provide the base energy cost of a statement. But statements usually are embedded in loops. And loops are usually data-dependent. One might think that Powot Simulator should analyze loops but this goes against the chosen approach. Energy optimization could be achieved if the statements inside the loops are optimized. That is why loops are not considered here with only one exception – for loops. For loops with constant boundaries (upper and lower) are easy to detect and simulate. This analysis is done to support static affine nested loop programs used for high-level system synthesis [11].

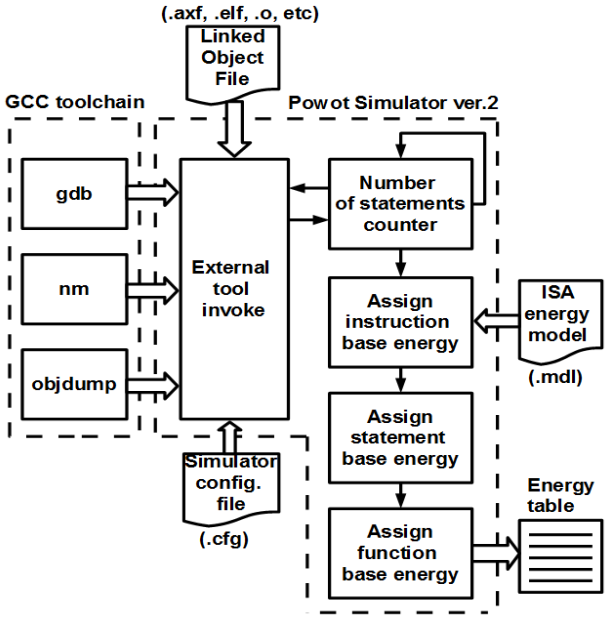

Fig. 3. Block diagram of Powot Simulator v.2

V. Hardware Platform and Benchmarks

Results produced by the simulator have to be verified. For this purpose tests on real hardware are considered best. The chosen platform is Texas Instruments' development board TM4C123G with an ARM Cortex-M4-based deeply-embedded microcontroller. The modeling of the microcontroller was done with a bench oscilloscope and without any automation. This means that absolute errors are expected to be high.

Example programs, or benchmarks, for deeply-embedded microcontrollers are scarce. Most of the existing benchmarks assume the presence of an OS and a file system. In the current example we lack both. For this specific type of microcontrollers there is a very good benchmark suite called BEEBS [12]. Only 10 out of 86 benchmarks were investigated. Separate bare-metal programs with only static for loops were also tested.

VI. Experimental Results

The experiments must estimate the errors of the simulation compared to real hardware energy measurements. First a function-level comparison between separate benchmarks is done. Then the DFS domain and the

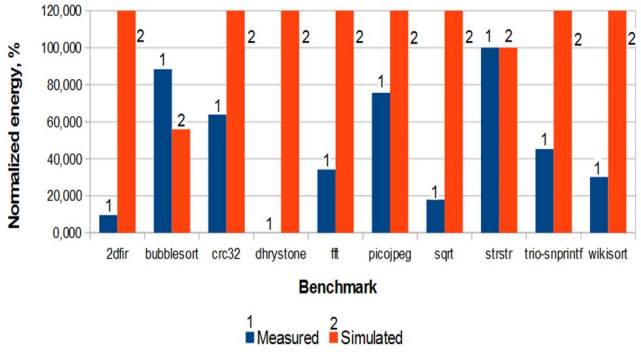

Fig. 4. Measured and simulated energy results for benchmarks, normalized to strstr.

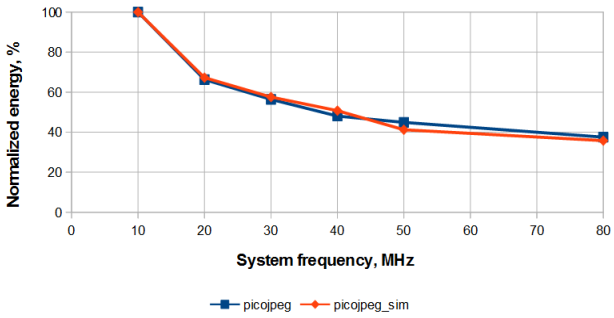

Fig. 5. Normalized measured and simulated energies for different system frequency of "picojpeg".

memory domain results are verified. No DVS tests were performed due to lack of such function in the target microcontroller. Some observations on instruction operands are also given. Simulator performance results are shown in the end.

A. Function-level benchmark comparison

Normalized to the "strstr" benchmark results are shown in Fig. 4. As stated before accuracy is affected by the input data. For this reason we cannot make benchmark comparison with the proposed ISS. Base energy cost of a function is a purely static estimate and depends more on code size than on input data. Errors of more than 100 % were measured and this was expected.

B. Statement-level DFS analysis

If we compare a benchmark not to others but to itself, we can tell accurately how much energy reduction we can have when the program is executed in different domains. In Fig. 5 normalized results for the frequency domain of the "picojpeg" benchmark are shown. The relative error is no greater than 4 %. The biggest relative error introduced in the other nine benchmarks is 6,2 %. Statement-level simulations require the simulator be accurate for frequency scaling inside the analyzed code. To test this, a C function was written with three static for loops performing dummy calculations. One of the for loops is placed inside a different frequency domain, i.e. there is a frequency change API before and after it. In Fig.6 the current consumption I_{DD} (trace two) of such a program is shown. Time frame is measured with trace one. The simulation was successful and yielded very good results with relative errors of less than 1 % for five frequencies other than the default. The DFS-enabled microprocessor model must contain accurate energy estimates of the DFS functions themselves in order to take transitional states into account. This is important because sometimes the transitions from one frequency to another may consume more energy than the optimization itself.

C. Statement-level memory analysis

In deeply-embedded microcontrollers code is executed mainly from the non-volatile memory. The programmer can place sections in the volatile memory but currently there is no way to tell whether this would be better solution from

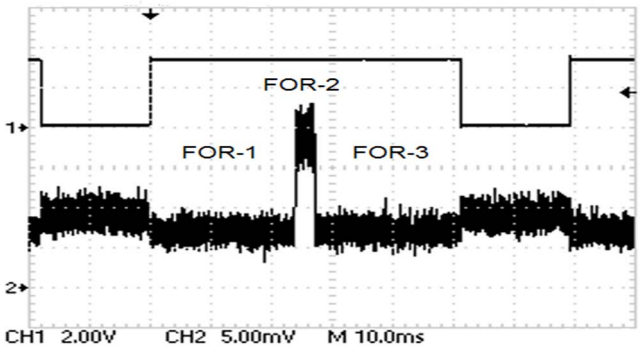

Fig. 6. Dynamic Frequency Scaling, 10 □ 80 MHz and 80 □ 10 MHz, of a static for loop.

energy point of view. By using memory domains in the ISS this problem is solved. For the chosen microcontroller, executing from SRAM, rather than FLASH, does lead to energy savings. Table 1 shows the results for the simulated and measured energy reduction. The deviation may be called "inter-domain error" (example is for domains FLASH, SRAM) and for this case is within 5 %.

D. Instruction operands and domain analysis

Assessment of addressing modes is not fully supported yet. However the simulator can detect instructions with different number of operands. Experiments were performed with the ARM Cortex-M instruction "add". The assembler generated 16- or 32-bit Thumb instruction depending on the number of operands. The two versions had noticeable differences in energy consumption.

E. Simulator performance

Simulation elapsed time can be measured with the help of software timers. The PC had 4 Gb of RAM and a dual core Intel processor running Ubuntu 14.04. Each simulation was started ten times and the average result of the elapsed time compared to the benchmarks' number of lines is given in Table 2.

VII. Conclusion

An Instruction Set Simulator was proposed in this paper. Data dependency is evaded by making the analysis on a statement-level abstraction rather than function-level. It can help programmers chose optimal energy code during the development. Future improvements may include: simulating peripheral modules, adding true addressing modes to the model (currently exist on a primitive level) and automating the process of model measurement.

TABLE 1. SIMULATING FLASH AND SRAM ENERGY CONSUMPTION

System freq., MHz	for(i = 0; i < 10000; i++){ … }		
	Measured reduction ($E_{FLASH} - E_{SRAM}$), %	*Simulated reduction ($E_{FLASH} - E_{SRAM}$), %*	*Error, %*
10	5,399	5,449	-0,050
20	9,852	9,520	0,332
30	8,323	11,886	-3,563
40	10,167	11,555	-1,388
50	6,205	11,191	-4,986
80	4,548	8,930	-4,382

TABLE 2. SIMULATION TIME

Benchmark	Lines of code	Average time, ms
2dfir	54	38,7
bubblesort	57	53,5
crc32	72	44,3
dhrystone	259	170,9
fft	139	166,0
picojpeg	1844	4110,6
sqrt	43	51,1
strstr	93	52,3
trio-snprintf	7282	4781,0
wikisort	492	2136,7

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Model Based Development of Ride Quality Real Time Monitoring System

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Abstract – **The continuously rising trend of complexity in electronics control units for transport vehicles requires a complete new approach of development to handle this complexity. Investing engineering effort to produce tens of thousands pages of native language specification could be irrelevant in the context of the future electronics devices. That is why the model-based development using formalized specification is identified to resolve many problems of the future embedded software development. It is considered to ensure a set of advantages like functional testing at specification level, and some other prerequisites for fast time to market, decreased to minimum number of defects. The current paper examines an exemplary process flow of building formalized specification as well as test specification, up to level of generation of optimized source code for the target system.**

Keywords – **Model based development, formal notation, formalized specification.**

I. INTRODUCTION

The constant trend of increasing computing power, combined with the big volume of integrated memory in contemporary microcontrollers enables the integration of huge number of features in one electronic device. It can be observed that not only the number of features is increased, but also their individual scope and functional complexity [7] have been enlarged too.

"Document-based development has severe disadvantages: There is the danger of misunderstandings and misinterpretations of functional requirements since they are written in natural language which could result in incorrect system behavior. Therefore, contradicting requirements can hardly be recognized before the realization of the system" [7]. High level of interpretation due to the personal lexical capabilities of the specification engineer and development engineer from the other site may deform the initial idea of the feature significantly. All these subjective factors are pursuing the complete development process and maintenance of electronics devices. The risk of increasing the overall number of defects in the electronic device or decreasing the efficiency of the development process, and respectively increasing time to market is another negative effect of the current development process in the automotive industry [7].

The necessity of improved efficiency in the software development for embedded devices and especially in the specification maintenance process requires deep dive into the shortcomings of the current process and preparation of a strategy for significant improvement. The subjective factors pursuing the process creation, expressing the content of the specification are within the main problems to be avoided. A prerequisite for their existence is the use of informal descriptive language specification [7],[8]. It is considered that a transition to a formalized description method, used in an environment that contributes to avoidance of unnecessary levels of freedom can solve the problem. This is due to the capabilities of this approach for eliminating subjective factors [7] such as the interpretation of the specification because formalized method of description; the ability to enhance the understanding by visualization the functional model; the possibility of testing [8] and improve the functional model before target system is available [7].

The availability of tools for creating a formalized method of description like MatLab®, Simulink®, Scade® facilitates the development of functional specification and may enable the required improvements in the process. In addition, these software tools are capable to generate high-quality source code [7] compliant to commonly accepted in the industry requirements like MISRA.

Based on so presented problems and reviewed opportunities, the goal of the current experiment is to create functional specification of ISO2631 [1] by formal notation in MatLab/Simulink environment. The formalized specification shall be possible to generate source code. The complete development phase shall provide possibilities of testing, validating and analysis on achieved results.

II. SYSTEM OVERVIEW

The goal is to create a transport vehicle suspension diagnostic system for monitoring in real time. The system shall collect information from accelerometers with digital communication interface. The received information is processed in order to assess the ride quality in accordance with ISO2631. As it was already determined in [2], an unacceptable variation in the suspension system characteristics could be identified by indirect indicator – such as the reference mode of ride quality, defined by ISO2631 – Fig 1, derived in [2].

Based on vehicle dynamics monitoring by accelerometers, traveling on a representative section of a path, it is possible to determine deviation from the reference characteristics in the suspension system of the vehicles [2]. The reference model is the ride quality rating

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defined by ISO2631, preliminary determined for this representative road. It is necessary the acceleration measurement as well as receiving of this data to be completed in real time. The formalized specification will be limited to functional model in accordance with ISO2631. The final target system will use the same functional model and it is required to prove the same characteristics defined in ISO2631.

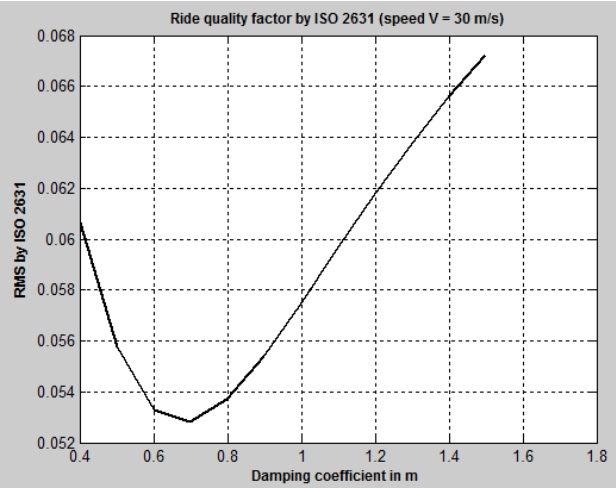

Fig. 1 – ISO 2631 ride quality as function of damping coefficient at 30 m/s

III. Different Stages during Creation of Specification with Formal Notation

A. Creation of discrete functional model in MatLab

The ride quality assessment is realized by measurement of vibration by accelerometers, mounted on the interior surface of the transport vehicle – seat, floor, table according to ISO2631. The effect of absorbed vibration by the human body is directly dependent by the amplitude and frequency of the vibration it-self in the transport vehicle [3]. Due to this fact, it is required that accelerometers have the necessary capabilities in amplitude and frequency aspect.

The realization of physiological model for ride quality assessment according to ISO2631 is based on weightening filters, defined in the standard. They are filtering particular frequencies of the vibration signal to represent the human perception – accumulated tiredness [4].

The different filters defined in ISO2631 contain several separate sub-filters, cascading in different combination realizing different transfer functions. Different filters are used depending on the measurement setup and their application defined in the standard - ISO2631 according to the weight filter W_k is provided to assess the comfort of a seated man on the axis Z.

The individual components of filters defined in ISO2631 and ISO8041 are represented as analog translation functions. Band-pass filter is realized by cascading of high-pass and low pass filter. The remaining weightening filters are "acceleration-velocity transition" and "upwards step filter". These components can be described in the s-domain:

High-pass filter:

$$H_h(s) = \frac{s^2}{s^2 + \frac{w_1}{Q_1}.s + w_1^2} \tag{1.1}$$

Low-pass filter:

$$H_l(s) = \frac{w_2^2}{s^2 + \frac{w_2}{Q_2}.s + w_2^2} \tag{1.2}$$

Acceleration-velocity transition:

$$H_t(s) = \frac{\frac{w_4^2}{w_3}.s + w_4^2}{s^2 + \frac{w_4}{Q_4}.s + w_4^2} \tag{1.3}$$

Upwards step filter

$$H_s(s) = \frac{s^2 + \frac{w_5^2}{Q_5}.s + w_5^2}{s^2 + \frac{w_6}{Q_6}.s + w_6^2} \tag{1.4}$$

The resulting filter is defined as a combination of equations (1.1), (1.2), (1.3) and (1.4). They are structured in Table 1. The respective numerical values of frequency and quality factor according to ISO2631, used for realization of required filters are available in ISO2631. The corresponding angular frequency is calculated by the known formula:

$$w = 2.\pi.f \tag{1.5}$$

TABLE 2. WEIGHTENING FUNCTIONS IN ISO2631

Weightening Function	Resulting Filter
$W_c(s)$	$H_h(s).H_l(s).H_t(s)$
$W_d(s)$	$H_h(s).H_l(s).H_t(s)$
$W_e(s)$	$H_h(s).H_l(s).H_t(s)$
$W_m(s)$	$H_h(s).H_l(s).H_t(s)$
$W_f(s)$	$H_h(s).H_l(s).H_t(s).H_s(s)$
$W_j(s)$	$H_h(s).H_l(s).H_s(s)$
$W_k(s)$	$H_h(s).H_l(s).H_t(s).H_s(s)$

The construction of transfer functions as per ISO 2631 is implemented through bilinear transformation. Using the bilinear transformation for the synthesis of digital filters consists in the replacement of the s-parameter from s-analog domain by a complex parameter, as follows:

$$s \to 2.\frac{(1 - z^{-1})}{(1 + z^{-1})} \tag{1.6}$$

Bilinear transformation is capable to provide a complete correspondence of j.ω axis from s-domain in z-domain. As a result, the following transfer ISO2631 functions are achieved and shown on Fig 2.

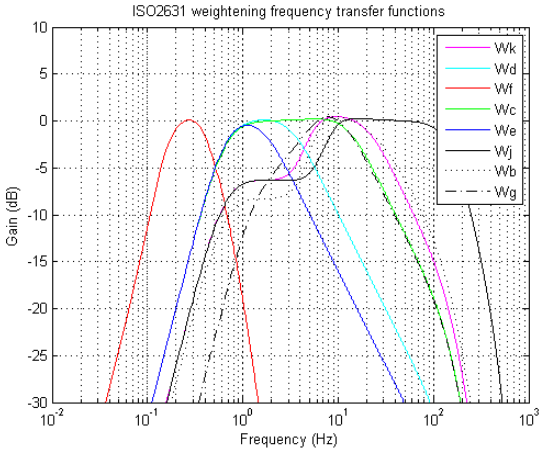

Fig. 2 – ISO 2631 Transfer functions

B. Validation of functional model in MatLab

After the model construction is complete, it is necessary to perform an intermediate validation of model. The validation is based on checking the precision of the achieved results.

The process of validation is based on using a sinusoidal signal as input stimuli, with defined amplitude, frequency, turned into discrete with particular sampling frequency. Indeed, it is composing only one frequency, which enables the easy calculation of output-filtered data, based on frequency transfer function provided in tables 3 and 4 in ISO2631. By taking the respective value from the table, it is easy to calculate the RMS as it would be the same result by filtering the input stimuli. The same input signal is provided to constructed ISO2631 model in Matlab, and filtered output signal is obtained. The comparison between both resulting data is used to calculate error resulting in the MatLab model in contrast to analytical table data in the standard. As it can be observed by the resulting data (Fig. 3) for the error, it can be very high in some particular cases (Wf). The transfer function's gain for that frequency are respectively very low, even close to zero, so the final impact on filter data is negligible. Additionally, this information is possible to be used to limit the frequency threshold on the input signal

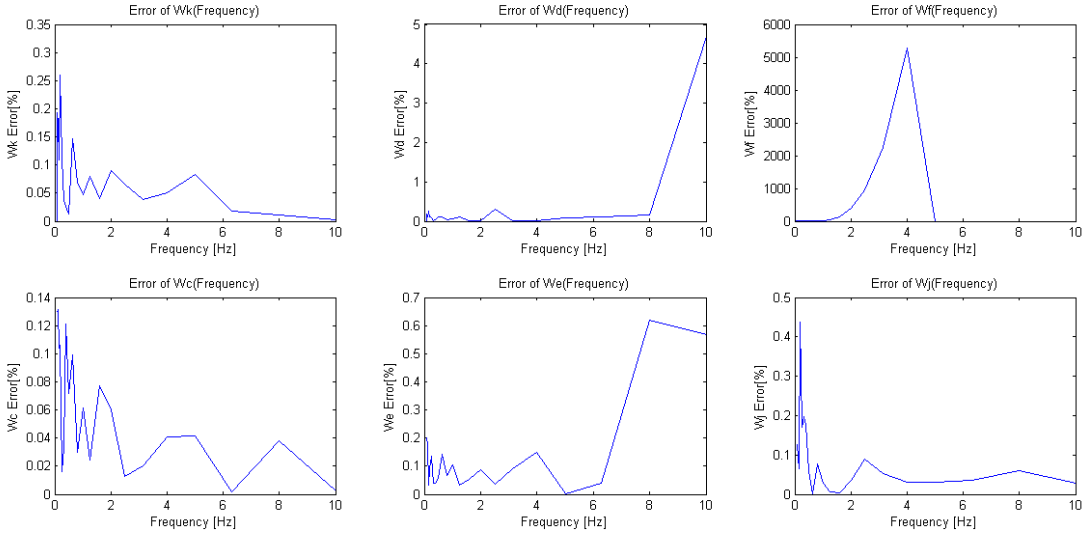

Fig. 3 Absolute error achieved with the functional model of ISO2631

C. Transferring the model in Simulink

The creation of transfer function in Simulink is the final stage of functional specification by formal notation preparation. It is going to be used for completing the test and additional tuning of the functional model if required. It will be used also for source code generation that is going to be used in the final target system.

It is possible to use this model as basis for synthesis of validation test cases. To support this task a dedicated test specification is required. It is required in order to define the complete format of the input stimuli to be used for validation, as well as definition of the expected resulting output. This approach shall enable the construction of so-called back-to-back tests. These kind of tests uses parallel tests by providing same signal to simulation environment of the model and the physical target system, flashed with the resulting from the model software. The goal is to compare and analyze the eventual deviation between both outputs. Usually, for successful realized formal specification is considered the fact the deviation between both resulting outputs is within the acceptable tolerance, defined in the test specification. Accompanying the functional model with test specification will facilitate the required criteria for applying intermediate validation in

every stage. The transfer function, representing the physiological ISO2631 model is shown on Fig. 4

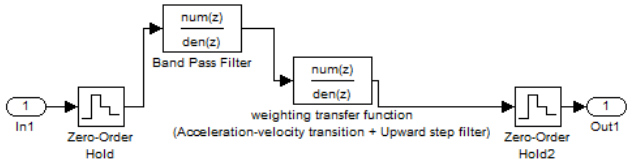

Fig. 4 – ISO 2631 Wk Functional Model in Simulink

It is built by cascading band-pass filter and combined weightening function by acceleration-velocity and upward step filter. The realization of transfer function for both filters are extracted as nominator and denominator from the MatLab model.

D. Validation of Simulink model

The usage of similar approach already used for validation of MatLab model is applicable also for validation of the Simulnik model.

It is also possible to apply back-to-back tests between the models in MatLab and Simulink, as shown in Fig. 5 for Wk filter. The total error does not exceed $4{,}5.10^{-3}\%$, which is considered as a negligible and acceptable error. The resulting ISO2631 filter in Simulink is shown on Fig. 6

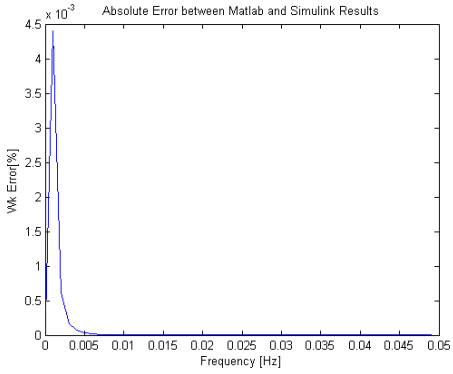

Fig. 5 – Comparison test of ISO 2631Wk in MatLab and Simulink

E. Generation of source code for ISO2631 filters and integration of the software into the target system

The already validated filter, realizing the ISO2631 psychological digital filter can be used for generation of source code. Simulink provides a facility for code generation – "Real-Time Workshop", taking even in account some specifics of the used microcontroller. In the particular case 32 bit, TMS320F28335 DSP is going to be used. It is equipped with floating-point arithmetic capability and going to provide the required calculation power, in order to achieve the required real-time work. Additionally, Simulink provides extended settings, using the so-called Target Language Compiler (TLC), enabling the selection of different software architectures – such like AUTOSAR [5] based system. The main argument for choosing this type of architecture is the already available real-time development environment, examined in [6]. It is able to provide the necessary facility for diagnostic and bring-up of the operating system, aiming realization of the real-time operation.

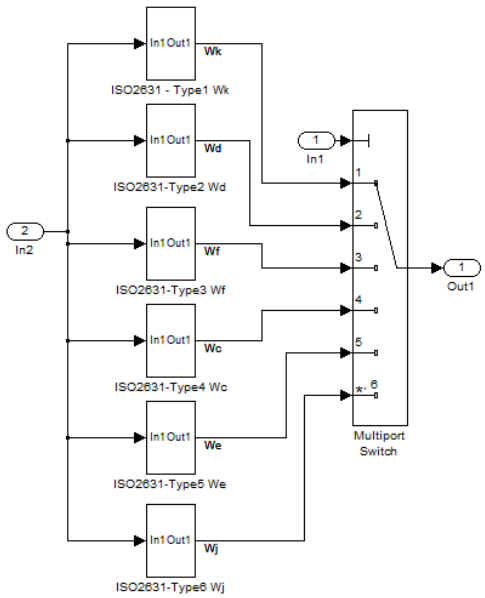

Fig. 6 – Realized ISO2631 digital filter in Simulink – formalized functional specification

IV. Conclusion

Realization of functional specification with formal notation, based on model-based development is an appropriate method for respectively complex systems development [8]. It provides a systematic development process, supported by rich set of development tools [7]. The approach enables the possibility for intermediate test and validation in the between the different stages even without a necessity of physical target system. Last, but not least is the capability of the method to eliminate the subjective factors around the process of specifying and implementing a feature and provide rapid facilities for tests and improvement of the functional model.

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DSP Realization of Hough Method for Line and Circle Recognition in Raster Images

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Abstract – **This paper describes a realization of Hough method of image processing over embedded DSP microprocessor module. The method consists of coordinates conversion of some points from particular raster coded image to the 2D parameters space using line or circle parameters in parametric equations. In the conversion result in 2D space the parameters of the lines or circles can be found.**

Keywords – **DSP, embedded, Hough transform**

I. Introduction

The lines and circles recognition are one of the main problems for image recognition in smart cameras for industrial and civil applications. The DSP microprocessors in embedded system provides of opportunity for very small realization using of direct connection with the cameras or image sensors nearby the object of recognition. This architecture is very useful for multi-object and multi-cameras purposes - the stream of real-time data can be reduced dramatically.

The Hough transform [1] is method for pixel-by-pixel transformation of the suspected pixels of belonging to line or circle to the 2D space of parameters according to particular parametric equation of line or circle. The suspected pixels are defined in advance by using some classical edge detection algorithm.

Let we have a line which is based on the next parametric equation Eq.1 [1]:

$$Y = a * X + b \tag{1}$$

Where: X and Y are coordinates in $[X, Y]$ space and a and b are particular parameters of given line in $[X, Y]$ space.

The Hough transform defines an 2D space based on the parameter variables as a coordinates $[A,B]$. In this manner every pixel in $[X,Y]$ space will be transformed to the [A,B] space like a line using next Eq.2:

$$b = -a * X + Y \tag{2}$$

The result of this transform is that only pixel-member of the particular line will have a single common point in [A,B] because they have the same A and B coordinates.

The other method of presentation of straight line in parametric space is to use a polar method [2] of representation in $[X, Y]$. This method will be explained for better understanding here.

The fig.1 is used for graphical background, where T_1 and T_2 are points that line of Eq.1 cross the axes in $[X_1, 0]$ and $[0, Y_1]$ respectively. Using Eq.3:

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$$\frac{Y - Y(T_2)}{X - X(T_2)} = \frac{Y(T_1) - Y(T_2)}{X(T_1) - X(T_2)} \tag{3}$$

After substitution of particular coordinates of T_1 and T_2 in Eq.3, we obtain Eq.4:

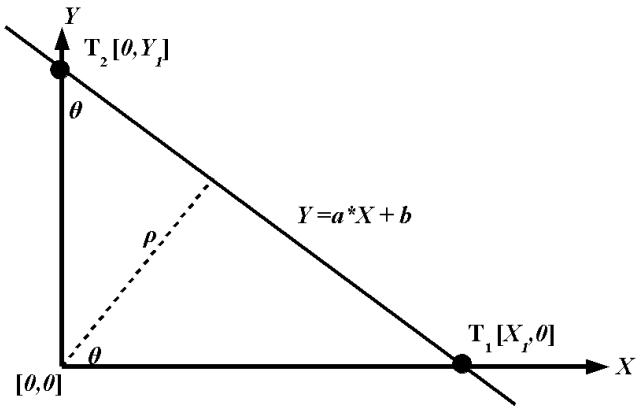

Fig.1. Hough transform of line in polar coordinates

$$Y = -\frac{Y_1}{X_1} * X + Y_1 \tag{4}$$

And if we take Eq.1 obtain Eq.5:

$$\begin{cases} a = -\dfrac{Y_1}{X_1} \\ b = Y_1 \end{cases} \tag{5}$$

To obtain polar parameters θ and ρ from Fig.1, we consistently have Eq.6:

$$\begin{cases} \rho = \cos(\theta) * X_1 \\ \rho = \sin(\theta) * Y_1 \end{cases} \tag{6}$$

From Eq.5 we have Eq.7:

$$\begin{cases} a = -\dfrac{Y_1}{X_1} = -\cot g(\theta) \\ b = Y_1 = \dfrac{\rho}{\sin(\theta)} \end{cases} \tag{7}$$

And finally from Eq.1 we obtain the polar representation of line, Eq.8:

$$X * \cos(\theta) + Y * \sin(\theta) = \rho \tag{8}$$

According to Eq.8 in [θ, ρ] space every point from straitght line in [X, Y] space will add the different sinusoid in [θ, ρ] space but all of that sinusoids will have the same common point [θ_1,ρ_1] from the parameters of the particular line. This is the idea of line recognition in raster image.

The Hough transform [1] can be used for the circle recognition also. The corresponding method can be used for transform from [X, Y] space to [A, B, R] space according to the next parametric representation of the circle, Eq.9 [1]:

$$(X-a)^2+(Y-b)^2=r^2 \quad (9)$$

Where a and b are coordinates of the centre and r is the radius of the circle. The 3D output [A,B,R] space can be reduced to 2D [A,B] space in case of constant or known value of the r.

It is important to know that Hough transform must be applied after some of the methods for edge detection – Sobel, Gradient etc.

In this current work, a rotation angle between two special graphical shapes (fiducial markers) from different cameras must be obtained.

A. Custom board specification

The custom DSP board, based on ADSP-BF516 is made, Fig.2.

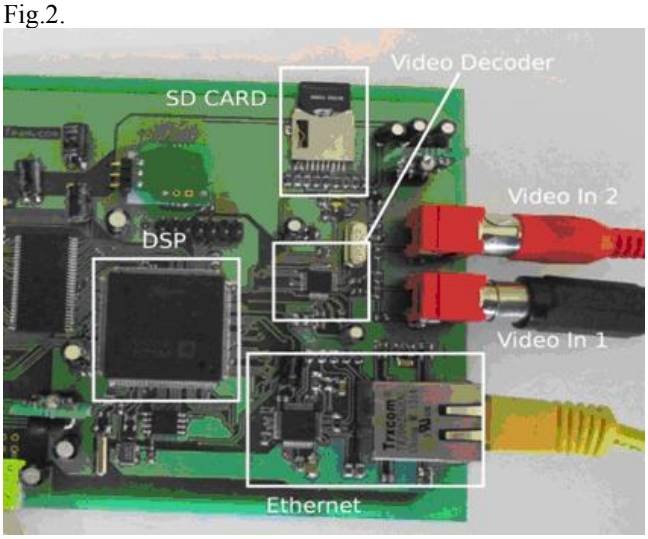

Fig.2. DSP board for two cameras video capture

The board includes next main parts:

- ADSP BF516 DSP unit, running at 300MHz
- SDRAM 16M x 16 bit memory running at 100MHz
- TVP5150 – two analog inputs video decoder

The two cameras are directly connected to the different analog inputs of TVP5150. The inputs can be switched internally by program code. The parallel output of TVP5150 is connected to the PPI (Parallel Peripheral Interface) of the BF516. This interface is especially designed to capture video data stream ITU-656 specification in real-time. The embedded DMA (Direct Memory Access) technique is used for real-time data transfer directly to the particular data buffers in SDRAM memory without any MPU interventions. The end of input procedure is DMA interrupt request event. The program code starts after this.

Note: The input video data are splitted into two semi-frames – odd and even. A program code is used for combine into single common frame.

B. Method of proceeding

The used algorithm of shapes recognition includes these steps:

- Capture images from Camera 1 and Camera 2
- Extract area of interest from both images
- Transform captured image data to gray scale format using threshold method over both images
- Apply Sobel [4] transform for edge detection over both images
- Apply Line Hough [5], [6] transform in area of interest over both images
- Apply Circle Hough [5], [6] transform in area of interest over both images
- Apply Lines recognition procedure
- Compare both results form images and determine of the fiducial markers displacement and rotation angle.

C. Results

The two input images include areas of interest are shown in Fig.3 and Fig.4 respectively:

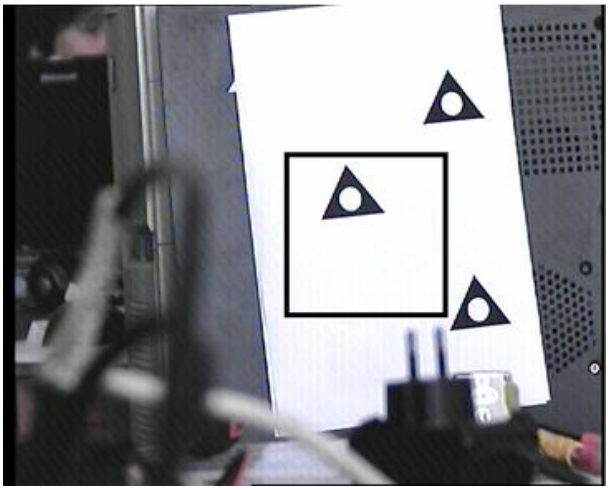

Fig.3. Camera 1 input image with area of interest

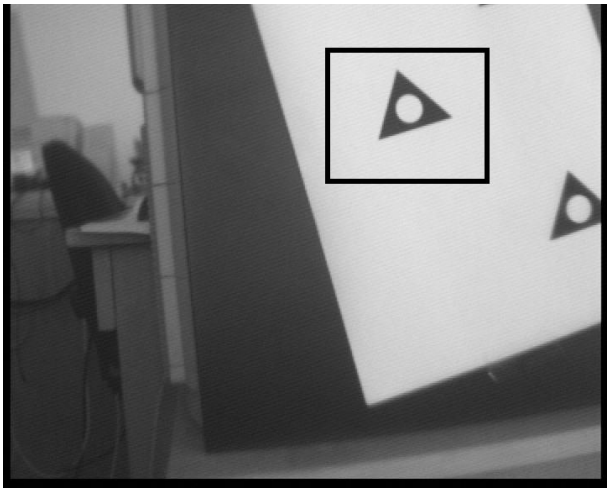

Fig.4. Camera 2 input image with area of interest

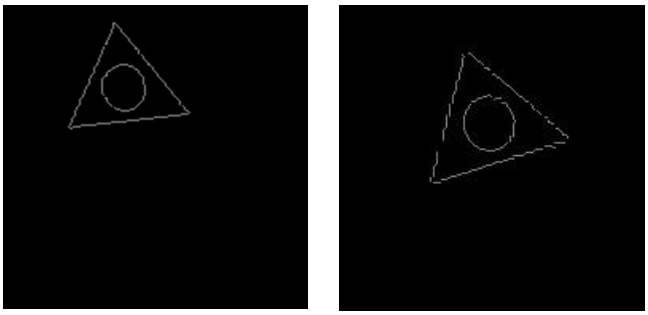

Fig.5. Camera 1 and Camera 2 area of interest after Sobel filter

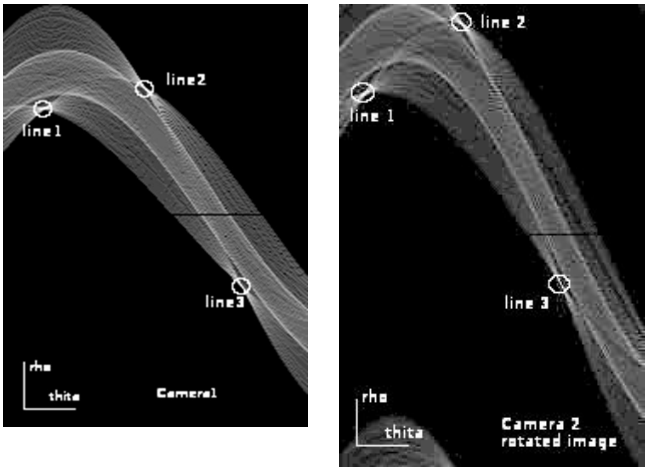

Fig.6. Both areas of interest after Hough Line transform

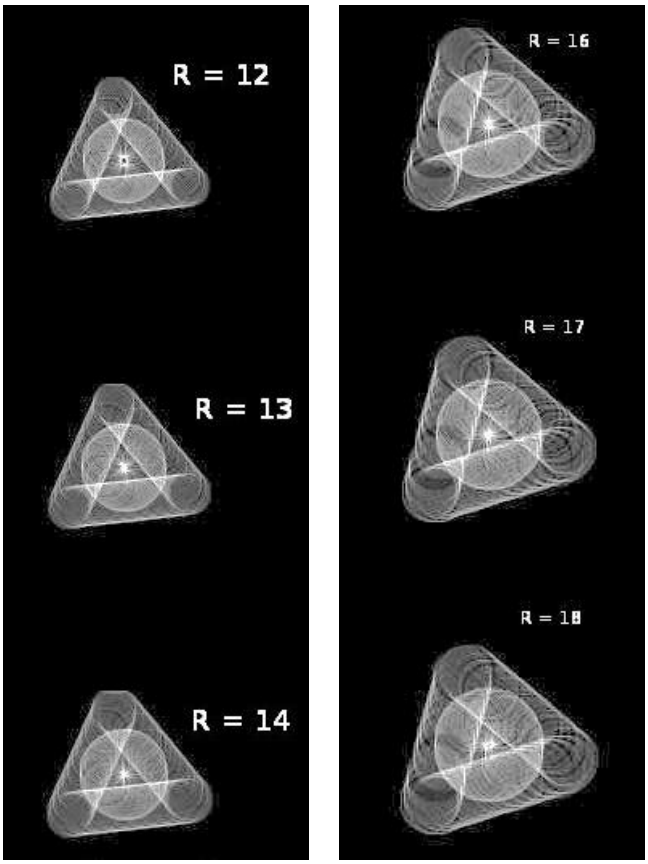

Fig.7. Camera 1 and Camera 2 area of interest after Hough Circle transform

After applying a Sobel filter [4] to each of areas of interest only, we obtain new images, shown in Fig.5 - left and right respectively. As can be seen on Fig.5 the threshold levels are calculated well because only few points in both images are lost from border shapes.

Fig.6 shows the result of Hough-Line transform according Eq.8 over both images.

Fig.7 shows the result of Hough-Circle transform according Eq.9 over both images.

Line1: ρ =68, θ = 23^0;
Line2: ρ =82, θ = 83^0;
Line3: ρ =-74, θ = 141^0;

Centre of the circle [a,b]: [75,52]
Radius: r=14

Line1: ρ =83, θ = 15^0;
Line2: ρ =124, θ = 72^0;
Line3: ρ =-29, θ = 130^0;

Centre of the circle [a,b]: [94,73]
Radius: r=17

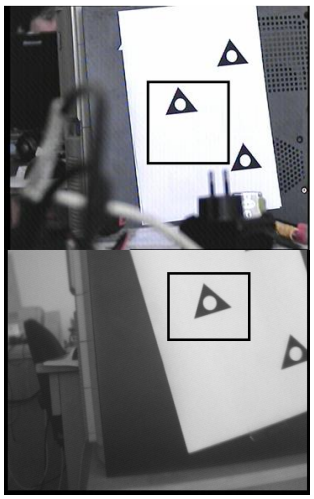

Fig.8. Camera 1 and Camera 2 area of interest after Sobel filter

Fig.8 shows the results of line and circle recognition procedures over both images in selected areas of interest respectively. The parameters of the lines and the circles are integer values and angles θ – in degrees.

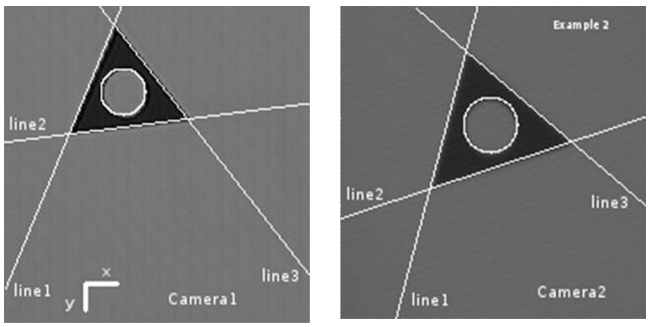

Fig.9. Camera 1 and Camera 2 area of interest after proceed all recognition procedure

Fig.9 shows the results of recognition of the full lines image according of the recognized parameters over-placed on the original grayscale images.

The other results from the recognition procedure are the next parameters;

- Total Horizontal Displacement is 19.
- Total Vertical Displacement is 21.
- Rotation angle is 10 degrees.

The total execution time includes all procedures of the described method for both of the images are 6.06129 sec.

Notes: The rotation angles are looking for in single degrees step from 0 to 359 degrees for all of the border points of each image from Fig.5.

II. Conclusion

The described application of DSP can be used for object recognition of the different shapes.

The processing speed can be accelerated in case of:

- using smaller areas of interests for both images;
- using smaller range of variation in the angle in Hough-circle procedure.

Using of FPGA preprocessing unit for Sobel filter realization will dramatically decrease execution time of recognition procedure

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Experimental Study of Cloud Computing Based SCADA in Electrical Power Systems

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Abstract – **The paper presents a test bed platform for implementation of Cloud Computing in SCADA systems for Electrical Power Systems. The general idea of the experimental study is to complete operation tests of traditional SCADA systems on cloud computing platforms, and integrate the main application modules of SCADA systems for electrical power metering on the cloud platforms. The logical networking structure of the Control Center of SCADA systems is presented. The virtualization of the different type of servers in the Control Center together with physical networking solution of the cloud platform realization is described.**

Keywords – **Cloud computing, SCADA, Power systems**

I. INTRODUCTION

An electric power system typically involves generation, transmission, transformation, distribution, consumption, and dispatching processes. Electric power is generated and consumed simultaneously and is not available for mass storage or transportation. Thus, as the key to the electric power system, monitoring and dispatching guarantee the reliability and security of electric power generation, transmission, distribution, and consumption, and play a key role in providing high quality and economic electric power. An electric power dispatching and monitoring system is often called a supervisory control and data acquisition (SCADA) system, energy management system (EMS), or distribution management system (DMS) globally. In this article, we call it the electric power SCADA system. In the early stage, the electric power SCADA system mainly used multi computer architecture, consisting of single server and two server cluster systems. Currently, the system uses computer systems with a distributed open architecture [1].

The electric power SCADA system provides SCADA, automatic generation control (AGC), automatic voltage control (AVC), EMS, DMS, dispatcher training system (DTS), geographic information system (GIS), and other useful functions. The software application system is constructed and developed by using the standard CIM model, and software architecture has evolved from the Client/Server architecture to the current Browser/Server architecture. The new generation Smart Grid [2] dispatching and control system uses multi-core computer cluster technology to improve system reliability and processing capacity, and uses a service oriented architecture (SOA) to enhance system interoperability and achieve horizontal integration and vertical interconnection of power grid dispatching services. Hardware infrastructure of these application systems involves high performance servers, complex high speed computer networks, high performance and highly reliable data storage systems, and workstations. The SCADA software is developed based on the platform which consists of Windows, UNIX, and Linux operating systems, and is based on relational databases.

The whole system is connected through computer networks for data exchange and sharing, and application programs share information through an enterprise service bus (ESB). With the development of the traditional IT application systems, IT-based applications have been expanding deeply to another industry field, and encountered various problems and bottlenecks. The same is true for the electric power SCADA system, which is a professional IT application system. The future electric power dispatching center should have high computing capacity, and powerful information acquisition, integration, and analysis functions especially with the advancement of Smart Grid applications.

Existing centralized computing platforms of electric power systems can hardly meet the above requirements, which have become one of the major bottlenecks in the Smart Grid. Some of the major disadvantages of these platforms are as follows [3]:

- Low basic resource utilization and poor scalability. A large amount of basic computing resources to meet the demands in peak hours are idle during off peak hours. To ensure reliability, lots of resources are redundant, and cannot be fully utilized. Contradictions are growing between energy demands and conservation policies. Due to the upgrade of business, the existing IT infrastructure cannot be reused. Currently, analysis and computing in the electric power system rely on the centralized computing platform in the dispatching center. Due to limited computing capacity, poor scalability, and high upgrade costs, large scale power systems suffer from insufficient data storage and analysis capabilities.
- Poor system interoperability leading to information islands. Parallel application systems have their own architectural features, and therefore resources cannot be exchanged or reused.
- Increasing management costs and risks, and decreasing equipment utilization.

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II. SCADA SYSTEM COMPONENTS

The traditional components of SCADA systems are shown on figure 1.

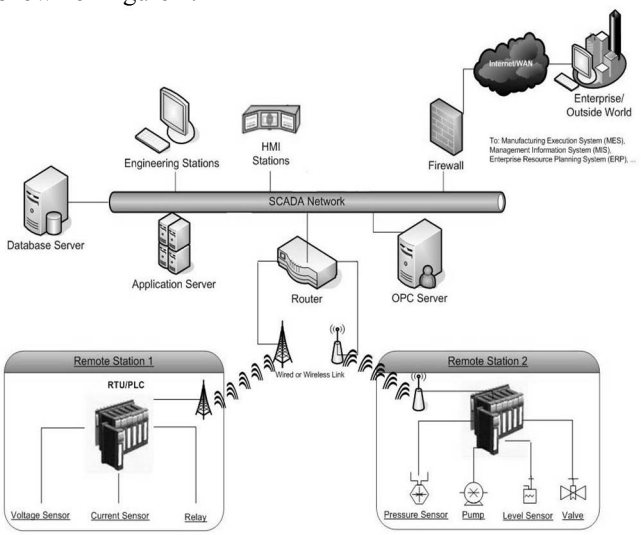

Fig. 1. SCADA network architecture

1. RTU – remote terminal units are connected to sensors. They have telemetry hardware capable of sending digital data to the supervisory system, as well as receiving digital commands from the supervisory system.
2. PLCs – programmable logic controllers are also connected to sensors. PLCs have more sophisticated embedded control capabilities than RTUs. PLCs do not have telemetry hardware, although this functionality is typically installed alongside them. PLCs are sometimes used in place of RTUs as field devices because they are more economical, versatile, flexible, and configurable
3. Telemetry system is used to connect RTUs and PLCs to control center or data warehouse systems.
4. A data acquisition server is a software service which uses industrial protocols to connect software services, via telemetry, with field devices such as RTUs and PLCs. It allows clients to access data from these field devices using standard protocols.
5. HMI is the apparatus or device which presents processed data to a human operator, and through this, the human operator monitors and interacts with the process.6. A Historian is a software service which accumulates time-stamped data in a database which can be queried or used to populate graphic trends in the HMI. The historian is a client that requests data from a data acquisition server.
6. A Historian is a software service which accumulates time-stamped data in a database which can be queried or used to populate graphic trends in the HMI. The historian is a client that requests data from a data acquisition server.
7. A supervisory (computer) system, gathering (acquiring) data on the process and sending commands (control) to the SCADA system.
8. Communication infrastructure.

III. CLOUD COMPUTING TECHNOLOGIES FOR ELECTRIC POWER INDUSTRY

Cloud computing can be used to solve various problems occurred during application deployment, use, and innovation process of the electric power SCADA system. Nowadays most of companies have their own cloud platform and virtual infrastructure, where they run business critical application and store data.

Private cloud advantages [4]:

- It is reliable and scalable. All resources are virtualized and in case of demand more storage or computing without downtime or impact can be added.
- Fast provisioning. Using techniques like templates can deploy thousands machines with few clicks.
- Automation. Pretty much everything can be automated using powercli or REST API. Common user interface: decoupling the computation infrastructure and the input system, enables multiple user interfaces to exist side by side allowing user-centric customization.
- Cost effective.

IV. PRIVATE CLOUD INFRASTRUCTURE

For the purposes of proposed experimental study a private cloud infrastructure is used. It is build and running in Technical University of Sofia, branch Plovdiv and its physical topology is shown on figure 2.

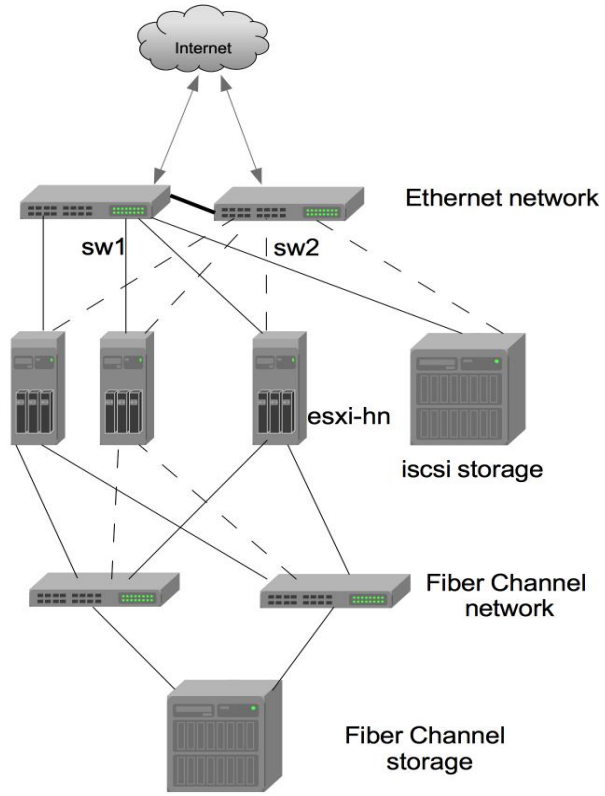

Fig. 2. Private cloud physical topology

The private cloud in use is shared by the university departments and students. Everyone can request computing capacity and after an approval process one could receive VMs with requested parameters. The following types of traffic are recognized:

- Management – this include all traffic generated by virtual infrastructure: vMotion, iSCSI, NFS, fault tolerance, web-based graphical user interface, etc.
- VM traffic – this is traffic generated from all VMs connected to VLAN based port groups – various types, generated by different applications.
- VXLAN traffic – this include traffic generated from all VMs connected to logical switches - various types, generated by different applications.
- SCADA traffic – this include traffic generated from SCADA system servers

Because of the importance and sensitivity of the SCADA traffic and servers a special logical networking that isolates SCADA traffic is proposed. It is based on VMware NSX [5] technology (figure 3).

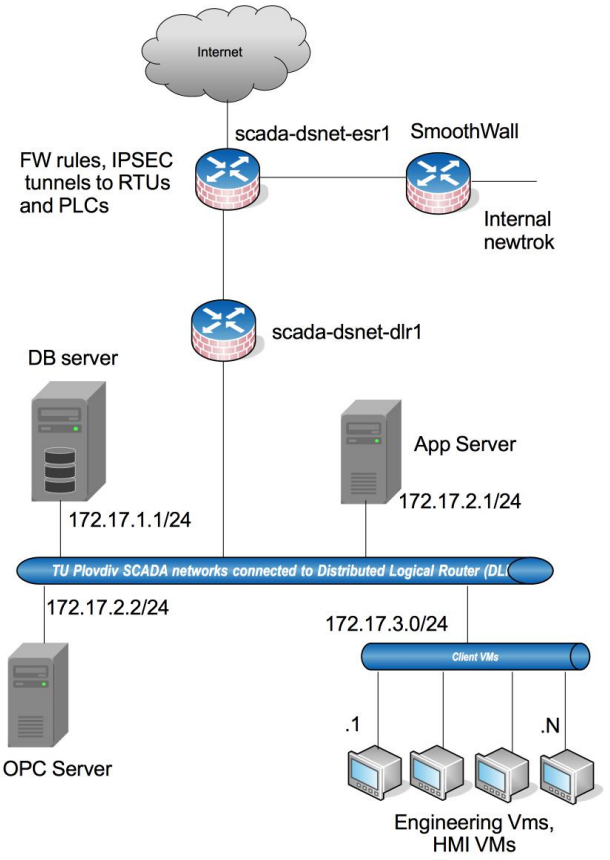

Fig. 3. Private cloud network topology

Entry point of SCADA network is scada-dsnet-esr1. This is NSX router with multiple features including firewall, IPSec and SSL VPN support, load-balancing and other features. A set of firewall rules restrict traffic to/from SCADA servers. IPSec tunnels connect scada-dsnet-esr1 to remote RTUs and PLCs. Through this secure channel data for controlled processes are collected. The scada-dsnet-esr1 runs OSFP with scada-dsnet-dlr1. The scada-dsnet-dlr1 is a distributed logical router (DLR) [6] that optimize routing traffic between different SCADA components. Distributed FW [7] is used to secure the communication.

V. Conclusion

The paper presents an implementation of a cloud-based SCADA system for use in electrical power control systems. The private cloud infrastructure in use is based on VMware platform. Deploying SCADA in cloud infrastructure automatically inherits all cloud advantages:

1. Most of SCADA components are virtual machines: DB server, Application Server, OPC server, Engineering and HMI VMs. This means that we can easily create new ones, clone, backup, take snapshots, HW upgrade - change parameters like CPUs, RAM, HDD, software upgrades.
2. All SCADA components can be protected by technologies like HA and FT [7].
3. All communication nodes are virtual nodes and thus are also protected by HA - scada-dsnet-esr1 and scada-dsnet-dlr1.

The presented test bed platform will allow various types of information flows and configurations to be investigated and analysed and the best set-up for the production services to be selected. Based on the experiments with different configuration of network services in the cloud the traffic flows will be optimized for best performance in terms of delay and resource usage.

Glossary

vSphere - VMware vSphere is the brand name for VMware's suite of virtualization products.

ESXi/ESX – Elastic Sky X. An enterprise-class, type-1 hypervisor developed by VMware for deploying and serving virtual computers.

VXLAN (Virtual Extensible LAN) – A Virtual Network that emulates an Ethernet broadcast domain.

vMotion – VMware vSphere live migration allows you to move an entire running virtual machine from one physical server to another, without downtime.

NSX - VMware NSX is the network virtualization platform for the Software-Defined Data Center (SDDC).

DRS (Distributed Resource Scheduler) – technology for balancing the computing capacity by cluster to deliver optimized performance for hosts and virtual machines.

VDS – VMware vSphere Distributed Switch (VDS) provides a centralized interface from which you can configure, monitor and administer virtual machine access switching for the entire data center.

DLR – Distributed Logical Router. It separates Control and Data plane. Control plane is a VM, but data plane is part of hypervisor kernel.

ACKNOWLEDGMENTS

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Open-source Platforms Application in Introductory Embedded Systems Teaching

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Abstract – **The paper presents the use of open source platforms - Arduino development board and the software IDE in an introductory embedded systems course. Some examples from the laboratory work representing the practical approach for teaching are given. With emphasizing on the practice rather than on the academic theory students master the material easier. The course is directed mainly at the program control of inputs and outputs to convince the students of the flexibility and universality of the programmable devices.**

Keywords – **Teaching, Embedded systems, Arduino, Programming**

I. Introduction

Embedded systems are affecting human lives in many ways. Learning to design and program embedded systems is a critical skill that is necessary for many industry and scientific jobs [1, 2]. In order to prepare the students for the challenges of their future job and to raise their knowledge to the level of the modern technologies, the Faculty of Electronic Engineering and Technologies at Technical University of Sofia accepted a new curriculum for Bachelor degree in Electronics. After many iterations and discussions with companies and employers organizations it was confirmed to emphasize on the embedded systems and especially on the obtaining practical skills in programming. Also all agreed that the practical training has to begin in the first semester in order to help the students in gaining experience for the specialized courses in the next years. Embedded systems courses are closer to functional and practical courses as opposed to disciplinary and formal ones. According to the philosophy of the new curriculum a brand new course entitled "Practice on open source platforms programming" with two hours laboratory work per week was included in the first semester. The aim of the course is to give the students knowledge and practical skills in embedded systems programming and also to introduce them into the world of the modern devices and technologies. After it has been conducted for two academic years, some considerations can be shared. One major part of the course is based on the use of Arduino development board and the software IDE, which are globally recognized as tools for introductory education. The development of projects like Wiring (www.wiring.org.co) and Arduino (www.arduino.cc) that offer immensely popular tools for lower- to intermediate-level software and hardware design was forced by the need of a physical interfacing between the smart machines and the surrounding world. This affects on science and education. Scientists increasingly use publicly available low-cost digital prototyping systems to create measurement tools and other experimental devices. To witness, a Google Scholar (scholar.google.com) query for articles containing the word "Arduino" in their title, excluding legal document, patents and citations, yielded a result of 490 scholarly articles (query result on September 2, 2013) [3]. The major benefits from using Arduino in an educational setting are considered in [4, 5].

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II. The Essentials of the Course

A. Laboratory Set-up

The software IDE provides a lot of preloaded examples. Some of them are used directly but after that the students work on many programs that the teaching team has previously prepared. The first code examples are intended for understanding the basic statements of the programming language for control of digital inputs and outputs. The development board OLIMEXINO-328 based on the microcontroller ATmega328P, and the on-board button and LEDs, which are shown in Fig. 1 and Fig. 2, are enough for understanding the basic statements of the programming language for control of digital inputs and outputs [6].

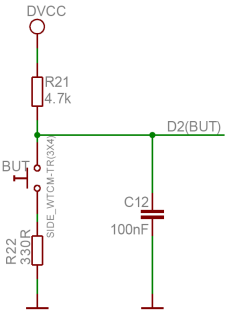

Fig. 1. User button with name BUT connected to ATmega328P pin 32 (digital signal D2)

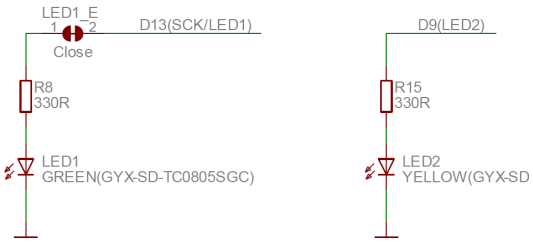

Fig. 2. Light emitting diodes connected to ATmega328P pins 17 (LED1 - digital signal D13) and 13 (LED2 - digital signal D9)

In advance the students have to know only that the digital input reads logic "0" from the pressed button and in order to light the LED a high level must be set from the digital output. Some code examples related to the control of digital inputs and outputs are presented in [7].

B. Loop Organization and Conditional Statements

One of the basic skills in programming is the loop organization. Generally the *for* loop is the most often used statement. It allows some lines of code to be repeatedly executed a specified number of times in a loop. The following code example illustrates the execution of *for* statement in conjunction with using *if...else* statement for flow control. The program controls the on-board LEDs and sets how many times the green one will blink when the yellow one is lit and respectively when it is dark.

```
int State = 0;
int Number = 0;
int Number0 = 5;
int Number1 = 8;
void setup()
{
pinMode(13, OUTPUT); // setting pin 13 as OUTPUT
pinMode(9, OUTPUT); // setting pin 9 as OUTPUT
Number = Number0;
}
void loop()
{
   for (int i = 0; i < Number; i++)
   {
   digitalWrite(13, HIGH); // setting pin13 HIGH
   delay(500); // delay 1/2 sec
   digitalWrite(13, LOW); // setting pin13 LOW
   delay(500); // delay 1/2 sec
   }
   if (State = = 0){
   digitalWrite(9, HIGH); // setting pin9 HIGH
   State = 1;
   Number = Number1;}
   else {
   digitalWrite(9, LOW); // setting pin9 LOW
   State = 0;
   Number = Number0;}
   }
```

The variable State contains the state of the yellow LED and the variable Number – the number of times the green LED will blink. The variables Number1 and Number0 contain the number of times when the green LED will blink when the yellow LED is lit and respectively when it is dark. This example helps the students to master the usage of *for* statement and to understand its essence that with a change of only one variable the number of times of execution of the group of commands is changed. Also the application of the conditional statement *if...else* is included.

C. Arrays

The most common application of loops is in working with arrays. The next code example is intended for this.

In addition this exercise will help the students to understand the operation of one of the most often used indicator elements – the 7-segment LED display, which organization, segments' placement and the connections of the diodes are shown in Fig. 3.

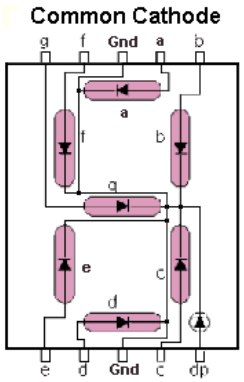

Fig. 3. 7-segment LED display with common cathode organization

The program turns on successively the segments of the display for 1s. Seven pins are intended to drive the segments via current limiting resistors and they are set as outputs. One-dimensional array is declared.

```
/*Setting outputs for every segment*/
int a = 4; // segment a is connected to pin 4
int b = 5; // segment b is connected to pin 5
int c = 6; // segment c is connected to pin 6
int d = 7; // segment d is connected to pin 7
int e = 8; // segment e is connected to pin 8
int f = 9; // segment f is connected to pin 9
int g = 10; // segment g is connected to pin 10
int segment[] = {a, b, c, d, e, f, g};

void setup()
{
   pinMode(a, OUTPUT); // the pin is set as output
   pinMode(b, OUTPUT); // the pin is set as output
   pinMode(c, OUTPUT); // the pin is set as output
   pinMode(d, OUTPUT); // the pin is set as output
   pinMode(e, OUTPUT); // the pin is set as output
   pinMode(f, OUTPUT); // the pin is set as output
   pinMode(g, OUTPUT); // the pin is set as output
}
void loop()
{
   for(int i = 0; i < 7; i++)
   {
   digitalWrite(segment[i], HIGH); // turns the pin on
   delay(1000); // delay one second
   digitalWrite(segment[i], LOW); // turns the pin off
   }
}
```

The next example is slightly harder than the previous one and it is intended for mastering the use of two-dimensional arrays. The 7-segment display is used again. The purpose of the program is to display successively the numbers from 0 to 9 for 1s.

It is based on the previous program. The following two-dimensional array is declared in addition:

```
/*Two-dimensional array - table with 7-segment codes of the numbers from 0 to 9*/
int pattern[10][7] = {
  {1,1,1,1,1,1,0},
  {0,1,1,0,0,0,0},
  {1,1,0,1,1,0,1},
  {1,1,1,1,0,0,1},
  {0,1,1,0,0,1,1},
  {1,0,1,1,0,1,1},
  {1,0,1,1,1,1,1},
  {1,1,1,0,0,0,0},
  {1,1,1,1,1,1,1},
  {1,1,1,1,0,1,1}
};
```

The setup function is the same. The loop function is:

```
void loop()
  {
    for(int x = 0; x < 10; x++)
    {
      for (int y=0; y < 7; y++)
      {
      digitalWrite(segment[y], pattern [x] [y]);
      }
      delay(1000); // delay one second
    }
}
```

In this example two loops are organized. The external loop with the counter *x* is executed ten times and for every step of it the internal loop with the counter *y* is executed seven times.

D. Analog Quantities Measurement

Because of that the processes in the surrounding world are analog but the computers and embedded systems are digital devices, it is of a great importance for the students to understand and master the rules for using analog-to-digital and digital-to-analog converters. The Arduino platform gives the students opportunities to obtain practical skills in this area and appropriate code examples help them herein. The next code example is dedicated to analog-to-digital conversion studying. It also presents the operation of the serial monitor which is used to display the information. A 10k potentiometer is connected between AREF and ground and the voltage derived from its wiper is attached to the analog input A0. The result is 10-bits word and the program reads a number between 0 and 1023.

The maximum value of the code corresponds to voltage value of 5V. After calculations the digital value of the voltage is determined and displayed. The display is refreshed every second.

```
const int analogInPin = A0;  // Analog input pin
long analogIn = 0;              // Digital code
float analogValue = 0;     // Analog input voltage value

void setup() {
  // initialize serial communications at 9600 bps:
  Serial.begin(9600);
}
void loop() {
  // read the analog input value:
  analogIn = analogRead(analogInPin);
  //calculates the analog voltage value:
  analogValue = analogIn * 5.000 / 1024;
  // print the results to the serial monitor:
  Serial.print("code = " );
  Serial.print(analogIn);
  Serial.print("\t voltage = ");
  Serial.print(analogValue);
  Serial.println("V");
  delay (1000); // delay one second
}
```

Two variables are used – analogIn and analogValue. The first one contains the digital code which is read from the analog-to-digital converter and the second one contains the digital value of the input voltage.

D. Signalization

The input voltage value can be produced by various sensors – for temperature, pressure, level of liquors in tanks and etc. So, the measurement of its value can be used not only for visualization but for taking decisions for control of external objects and for signalization too, as it is shown by the algorithm which is depicted in Fig. 4.

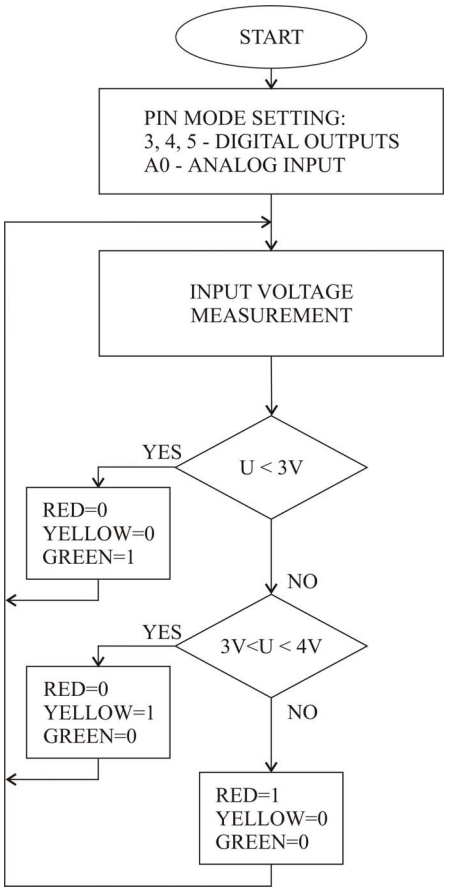

Fig. 4. Algorithm of a program for signalization

For the purposes of the signalization the current value of the input voltage is compared to a previously set one and according to the result of the comparison a command is executed. So, the understanding of the principles of the signalization will give the students useful skills and experience for their future work. The next example introduces to the students the principles of the signalization. The purpose of the program is to switch on green, yellow and red LEDs according to the value of the input voltage. To do this, the mentioned above LEDs are added and are connected to digital outputs 3, 4 and 5 via current limiting resistors. The voltage values are conditional and can be changed in accordance with the concrete application. The serial monitor is used again to visualize the current value of the voltage. The example also presents a practical application of the conditional statement *if…else* in taking decisions.

```
const int analogInPin = A0;  // Analog input pin
int analogIn = 0;            // Digital code
float analogValue = 0;    // analog input voltage value
const int Green = 3;
const int Yellow = 4;
const int Red = 5;

void setup() {
  // initialize serial communications at 9600 bps:
 Serial.begin(9600);
 pinMode(Green, OUTPUT);
 pinMode(Yellow, OUTPUT);
 pinMode(Red, OUTPUT);
}
void loop() {
  // read the analog input value:
  analogIn = analogRead(analogInPin);
  //calculate the analog voltage value:
  analogValue = analogIn * 5.000 / 1024;
  // print the results to the serial monitor:
  Serial.print("code = " );
  Serial.print(analogIn);
  Serial.print("\t voltage = ");
  Serial.print(analogValue);
  Serial.println("V");
  if(analogValue < 3.000) {
  digitalWrite(Green, HIGH);
  digitalWrite(Yellow, LOW);
  digitalWrite(Red, LOW);}
  else if(analogValue < 4.000) {
  digitalWrite(Green, LOW);
  digitalWrite(Yellow, HIGH);
  digitalWrite(Red, LOW);}
  else {
  digitalWrite(Green, LOW);
  digitalWrite(Yellow, LOW);
  digitalWrite(Red, HIGH);}
  delay (1000);   // delay one second
}
```

III. RESULTS

The laboratory work dedicated to programming using Arduino board gives the students basic skills in using C programming language. The statements for loop organization, decisions taking, working with arrays, analog and digital inputs and outputs control are mastered. During the course the students also obtain basic knowledge about the most popular indicator elements and skills to work with them. The initial explanation of the principles of the data conversion and signalization introduces the students to the world of the modern technologies.

After the first approbation of the course "Practice on open source platforms programming" from the new curriculum for Bachelor degree in Electronics at the Technical university of Sofia it was considered that the material attracts the attention of most of the students and they overcome the tasks easily. That's why new examples like control of sensors and signalization were added in order to widen the area of knowledge. The direct program control of external devices and indicators convinces the students in the flexibility and the universality of the embedded systems.

IV. CONCLUSION

In conclusion it can be said that during the introductory education it is better to emphasize on the practice rather than on the punctual academic theory. It is more useful and the students accept the material easier. The success in practical implementation encourages the students and convinces them in the meaning of the learning as a way to improve their skills. The open source platforms - Arduino development board and the software IDE offer friendly environment for beginners and are very useful for the introductory education. The students obtain knowledge and gain practical experience that will be useful in mastering the further courses.

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Development of a Specific Electronic Control System for an Engine Dynamometer

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Abstract – **With the numerous and complex parameter interactions that take place during the operation of an engine, the optimization of its performance in terms of alternative fuels is difficult, as dynamometers with conventional technology are unable to make significant measurements for alternative fuels. In this study, an electronically controlled dynamometer system capable of measuring a number of specific values was developed. The system allows the optimum values for different fuels to be found for the test engine by monitoring parameters such as injection advance, and at the same time communicating with the electronic control unit via a computer interface. The study presents the algorithm and test results of the system.**

Keywords – **Dynamometer, electronic control, eddy current brake, engine test bed, biogas**

I. INTRODUCTION

The expanding use of alternative fuels in gasoline or diesel motor vehicles will be realized in a major way in the near future. However, performance optimization in terms of alternative fuels is not an easy matter when the engines are operating with a numerous and complex interplay of parameters. For this reason, instead of designing a new electronic control system for these engines or developing new software, a method for making changes in existing software or commissioning additional systems was adopted. Consequently, the creation of relevant electronic control and measurement strategies dealing with the optimization of the engine-fuel pair, along with the literature on this topic, will be examined in the sections below.

Erkuş and Sürmen [1] studied the structural changes required in order to optimize operating conditions when using natural gas in a gasoline engine. With this aim, they developed electronic subsystems on their created test system with an algorithm for the program performing control of these subsystems. In another study, Arellano et al. [2] presented a dynamometer-control design for systems with stiff and flexible shafts. Its practical implementation for position control of linear and nonlinear emulated loads was conducted and the experimental results were compared with corresponding simulated loads in order to validate the emulation strategy. The comparisons showed a good agreement between the experimental and the simulation, which confirmed that the system had preserved the dynamics of the desired load when used in a closed-loop system. Yanakiev [3] stated that nonlinear, strongly coupled engine dynamometer plants can be more successfully controlled by applying multivariable techniques rather than by using independent PID controllers. The author also presented an application of the model-referenced adaptive control approach to the engine speed and torque control problem. Bunker et al. [4] stated that the large degree of loop interactions, induction-to-power delays, combustion uncertainties, and engine nonlinearities were included in the difficulties in controlling engine-dynamometer systems. The performance goal was realized by balancing the bandwidths of the loop transfer functions to avoid excessive loop interactions in the closed-loop system. The controllers were designed using a sequential frequency domain approach. In another study, Çelik et al. [5] designed and manufactured a computer-aided engine test stand. This stand enabled the internal combustion engine to be tested with computer control and allowed for experimental data to be transferred to a computer in real time. Engine performance evaluations could be easily carried out with engine tests performed using the stand. Westmayer et al. [6], in their study, proposed an approach for high dynamic torque control of an industrial engine test bed. The main goal was to develop a control concept that was capable of periodic reference tracking at a high control bandwidth while at the same time sufficiently rejecting disturbances coming from external excitations. For that reason, a model predictive control was utilized which offered major benefits compared to classical controllers. Ergenç and Koca [7] developed a programmable logic controller (PLC) control system aimed at using dual-fuel in a mechanical injection system diesel engine. Diesel fuel and LPG were used in the study and, in order to determine the optimum injection advance, they examined the effects of engine performance optimization made via the engine management system. Erkuş et al. [8] evaluated a four-stroke LPG-injected spark ignition (SI) engine run by using a specially developed engine control unit (ECU) to control the ignition timings. Ignition timing values two and four degrees retarded and advanced were applied in addition to the original values of the gasoline engine. Results showed that the engine ran without any problem with up to four degrees of the advanced ignition

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timing values. However, the retarded values caused improper combustion.

As a research project on biogas for use in engines, the present study provides details of the dynamometer apparatus developed to measure the engine parameters that need to be controlled.

II. MATERIALS AND METHODS

2.1. System Design

The software was specially designed for measuring specific engine running and loading parameters and real-time rpm, injection mapping depending on knock control and other operation parameters. The general structure of the system and the software is shown in Figure 1.

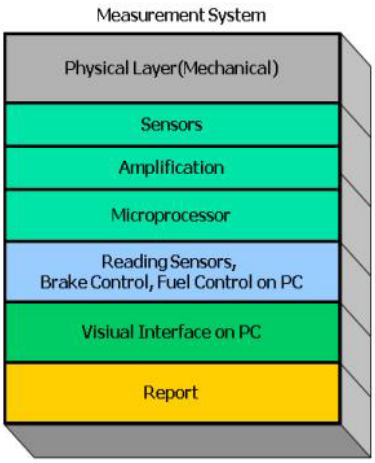


Fig. 1. Layer structure of the system and software

2.2. Data Acquisition System (DAS) and Control Software

The system was designed to control and measure engine operating parameters for all alternative fuels. However, in this study, the system was used to detect the ECU parameters of biogas and CO_2 blended fuel usage. Proportional and controlled experiments were conducted for biogas and other gas mixtures and eight temperature points. The system was operated to detect the confirmed optimum engine performance variables according to their sensor measurements together with the applied brake force fuel-air ratio and gas controls. Under the system, in order to test the obtained optimum values of the movement, the fuel injection could be determined for different fuels or applied to the ignition map. In order to obtain the correct mappings for the different fuel options, knock control as well as performance parameters of the system were taken into account. The eddy current brake system, an important part of dynamometer, was designed for the engine performance and loads; the ECU performance was obtained with other gas and fuel flow sensors. A block diagram of the system, including the developed MS Windows-based software with which all the measurements and controls were made, is given in Figure 2.

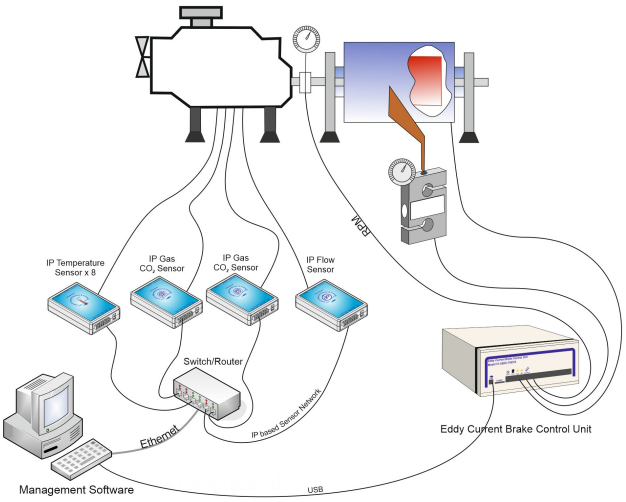


Fig.2. Block diagram of the system

2.3. Eddy Current Control Unit

The AC eddy current control circuit was designed as a single alternans. The eddy current circuit accomplished the brake force by controlling the single alternans of the grid voltage. A block diagram of the eddy current control unit circuit is given in Figure 3.

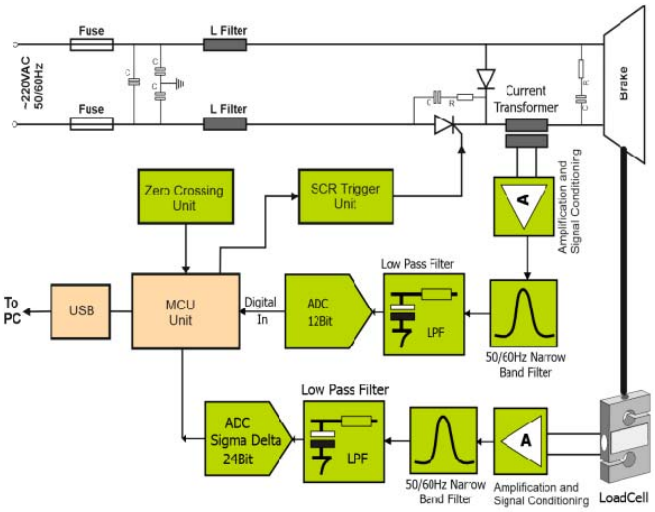


Fig.3. Block diagram of eddy current control unit circuit

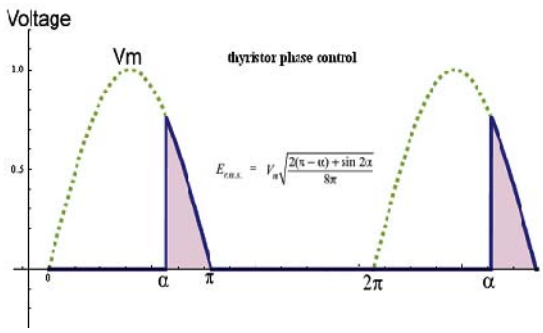
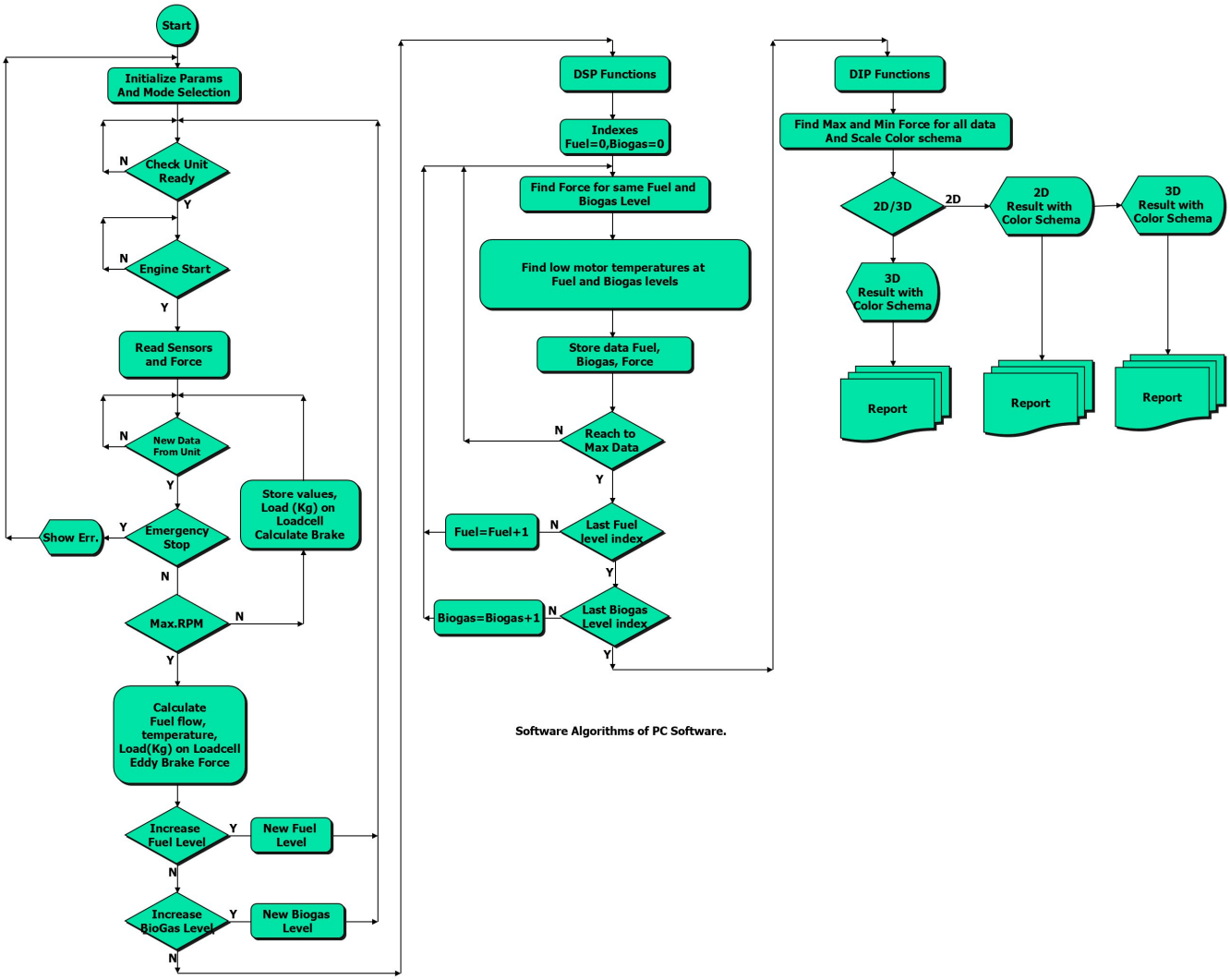


Fig.4. Thyristor phase control

As shown in the block diagram, the load control unit is controlled by a thyristor control unit. Furthermore, the $E_{r.m.s}$ is controlled by a multipoint control unit (MCU) with one microsecond resolution from zero crossing and is changed as seen in Figure 4. The $I_{r.m.s}$ and also $P_{r.m.s}$ changes depend on the $E_{r.m.s}$. The PC software calculates the phase control angle **α** and then sends it to the control unit. A flow diagram of the main program controlling the system is given in Figure 5. Installing the software allowed the search for the knock-free operating point of the engine while increasing the gas level times. As a result of all these data under varying loads, the timing control system infrastructure was then designed after the lowest knock behavior and the lowest engine temperature had been determined.



Software Algorithms of PC Software.

Fig.5. Software algorithm flowchart

III. EXPERIMENTAL STUDY

In this study, the performance tests were conducted on a 4-cylinder 4-stroke direct injection 48 HP diesel engine connected to a conversion kit to allow biogas (methane) use. When the engine was under operation, the developed electronic control system was mounted as seen in Figure 6. The Schenck-215 kW dynamometer, standard commercially available diesel, natural gas and, as a regulator, CO_2 were used for the study. A view of the data collection software is presented in Figure 7.

Fig.6. Dynamometer and control system

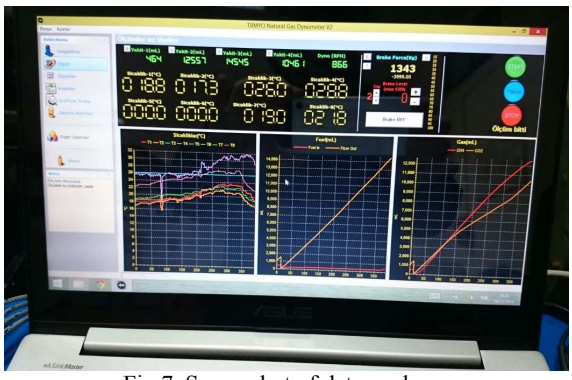


Fig.7. Screenshot of data analyses

Using the diesel and the fuel blends given in Table 1, the engine was started in idling mode, and then, with the engine performing on the secondary fuel supply, it was given full throttle and brought to the desired speed (2600 rpm) after which it was slowed with the braking system until it dropped below 1000 rpm and the engine was braked. At this stage the engine braking force, fuel consumption, soot and temperature values were measured.

Table 1. The fuel blends used in the tests

Fuel	Fuel addition	Name
Diesel fuel		D2
Diesel + natural gas	Level 1	F1
Diesel + natural gas	Level 2	F2
Diesel + natural gas + CO_2	Level 1	FC1
Diesel + natural gas + CO_2	Level 2	FC2

As an example, the torque values in terms of the diesel and the other biogas blends are presented in Figure 8. The suitable rates and operating conditions and all the obtained results in the biogas assessment in terms of of both performance and environmental pollution indicated that it could be used as an alternative fuel in diesel engines.

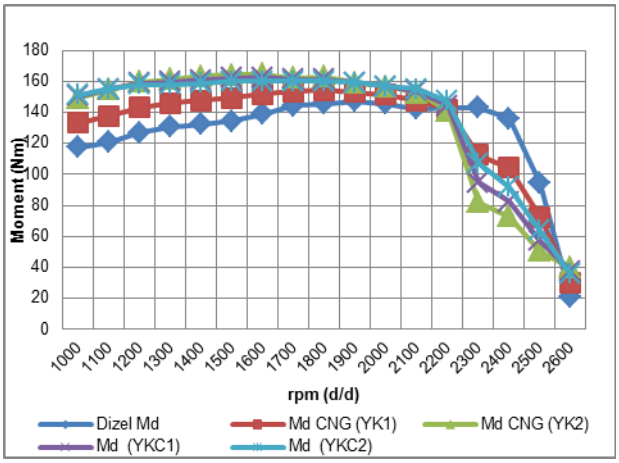


Fig. 8. Torque values for diesel and fuel blends

IV. Conclusion

The concrete outputs of the hardware of this study were integrated with the software to develop a performance testing system. In this way, a control strategy could be established; whichever engine or alternative fuel is used does not matter for enabling this engine-fuel pair to achieve optimum performance. Already, work is being conducted on another diesel engine under the same system controlled by an ECU for reading engine management parameters in order to optimize these parameters for biodiesel use.

As a result, each passing year meets with new vehicle users and fuels like gasoline and diesel in the market, each more efficient in many ways, with the proposed fuel being environmentally friendly and enabling them to use it correctly. Thus, this study is a step towards the development of original electronic fuel control strategies and units. The development of the system in different dual-fuel engine trials is continuing. Studies on the system are expected to contribute to the use of alternative fuels, especially for fully electronically controlled engines.

Acknowledgment

This study is a result of Project No. 2013/88 and was supported by the Uludag University Scientific Research Foundation of Turkey.

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IP Based Smart Energy Metering with Energy Saving

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Abstract – ***Smart measurement and control systems contribute to energy savings and are capable of instantly receiving information about their environments. In this study, an electronic measurement and control system was developed by installing an Ethernet cable under WLAN with remote control power access which has the ability to measure and control electricity consumption. The system uses sensors capable of receiving information on devices connected to the system, and has the energy saving capability to prevent sleep mode power consumption. The development of the electronic measurement and control system and its software are described and the experimental results are presented. In the study, results are given of tests carried out for various establishments by using the system algorithm with the Internet-based Group Socket System.***

Keywords – **IP-Based, Power Distribution Unit, Smart Metering**

I. INTRODUCTION

Because worldwide energy resources are limited, intensive research has been conducted on the most effective way to save energy when using these resources. With this aim, various smart measurement and control systems have been developed. Closure of electrical devices is not always possible by using on/off switches or removing the plug. Consequently, when these devices are left plugged in, over time they also draw standby energy by themselves, and this standby energy can reach large amounts. When examining the literature on the subject given in the following section, it can be seen that the studies are focused on automatic energy control methods for homes, cities and factories.

In one study [1], the researchers accomplished the measurement of very small currents using high precision and multifunction energy metering. In another study [2], by applying a simple and efficient weighted average price prediction filter to the actual hourly-based price values used by the simulation results, it was observed that the combination of the proposed energy consumption scheduling design and the price predictor filter led to significant reduction, not only in users' payments, but also in the resulting peak-to-average ratio in load demand for various load scenarios. Engel et al. [3] stated in their patented study that, unlike pass power controllers which were limited to powering on on/off for all of the computer equipment controlled by a given controlling element, this invention provided a non-manual capability for remotely powering on/off in any one or more components of a system or systems and providing the power status thereof in a selective manner. By being able to selectively activate or deactivate any or all of the components of a data processing system, the ability to conserve electrical energy was optimized. The authors [4] of another study demonstrated the use of multi-agent systems to control a distributed smart grid in a simulated environment. The simulation results indicated that the proposed multi-agent system could facilitate the seamless transition from a grid connected to an island mode when upstream outages were detected. This denotes the capability of a multi-agent system as technology for managing a micro grid operation. Another study [5] discusses again various features and technologies that can be integrated with a smart meter. In fact, deployment of smart meters needs the proper selection and implementation of a communication network that satisfies the security standards of smart grid communication. The paper outlines various issues and challenges involved in design, deployment, utilization, and maintenance of the smart meter infrastructure. In a patented study, Bartone et al. [6] presented a system and method for real-time monitoring and control of energy consumption at a number of facilities to allow aggregate control over the power consumption. The present invention also includes a wireless network for communicating with a number of facilities and allows other information to be collected and processed. In another study [7], high efficiency and performance, low cost PCU architecture with an Ethernet interface was selected from NXP for home appliance application. Chand et al. [8] based their study on background studies and experiences in identification and implementation of fundamental design techniques for making a PCB layout requiring a high degree of EMI/EMC compliance.

In this study, the work of the developed Internet-based Group Socket System was examined in terms of its characteristics of controlling energy consumption according to demand in homes and outside working hours in workplaces. By detecting the standby mode of electronic equipment and automatically cutting the

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energy of the devices, the system seeks to ensure zero energy consumption.

II. MATERIALS AND METHODS

2.1. System Design

The system was designed to control energy by detecting the standby mode of devices and according to demand and outside of working hours cutting their energy consumption to zero. By measuring the active-reactive power factor (Cos-Fi) and the total energy, the built-in web server, can provide information instantly to people connected to the system. A general view of the construction and software of the system is shown in Figures 1 and 2.

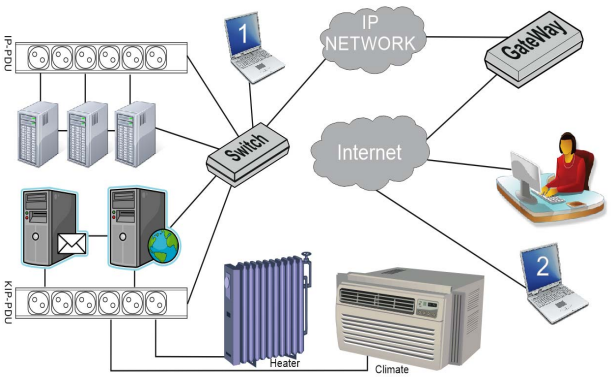

Fig. 1. Energy measurement and control structure of IP-PDU

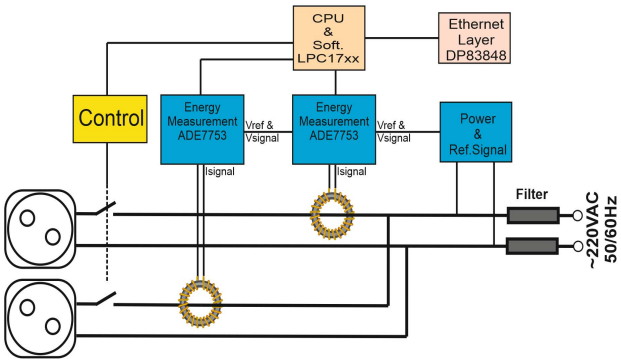

Fig. 2. Hardware structure and software of the system

A schematic of the design is shown in Figure 3. The main processor contains an internal LPC1769 Ethernet circuit. The web server (http), SNMP, E-mail, Telnet, SMS and WOL protocols, web interfaces and ADE7753 energy calculations were optimized on a single processor. The system has a total (potential) energy consumption of 0.8 W/h, but it falls to 0.6 W/h when not calculating and when the Ethernet is not active. In order to measure very sensitive toroidal and network voltage, a reference transformer was used to detect low current measurements. In this way, the network was provided with insulation and thus, except for the 3.3V- and 5V-processor section, was not subjected to any high voltage. Therefore, the necessary security was provided for home and office applications.

Embedded software was developed to identify standby currents in the specified time period, and when they are detected, to cut their energy. Energy is supplied to the computers via the web interface while the WOL protocol with the power-on signal sent via the Ethernet supports its operation. Thus, after energy is provided for the computers to operate, the on/off button must not be pressed.

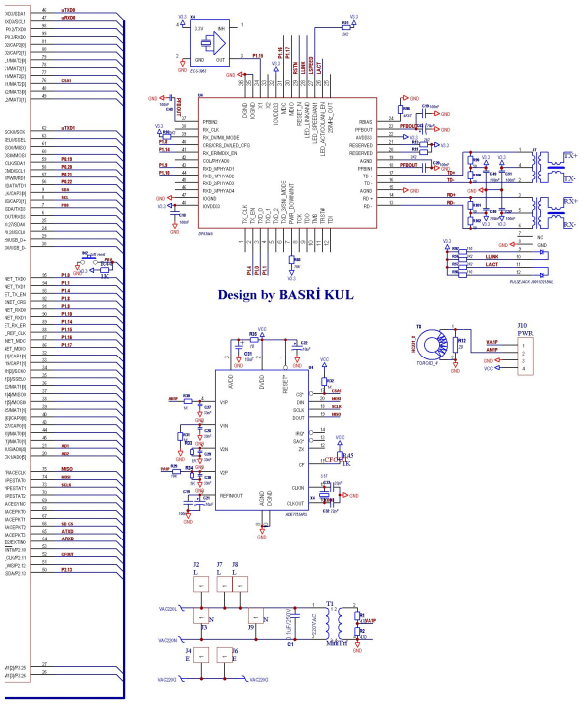

Fig. 3. Schematic of the implemented system design

The design of the PCB is shown in Figure 4. The 2-layer PCB design work passed the EMC testing, although in order to provide highly accurate measurements with ADE7753, the measurement must be read in the zero crossing moments of the network.

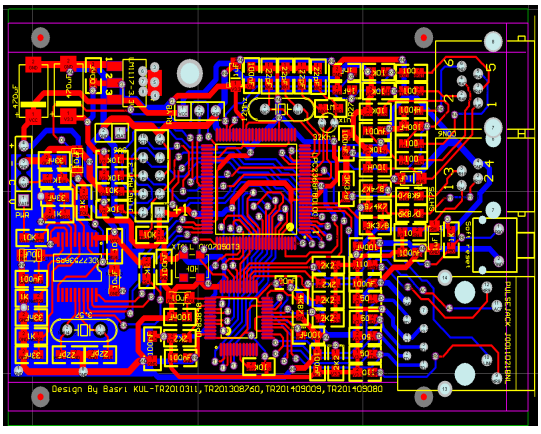

Fig. 4. Implemented PCB of system design passed by EMC

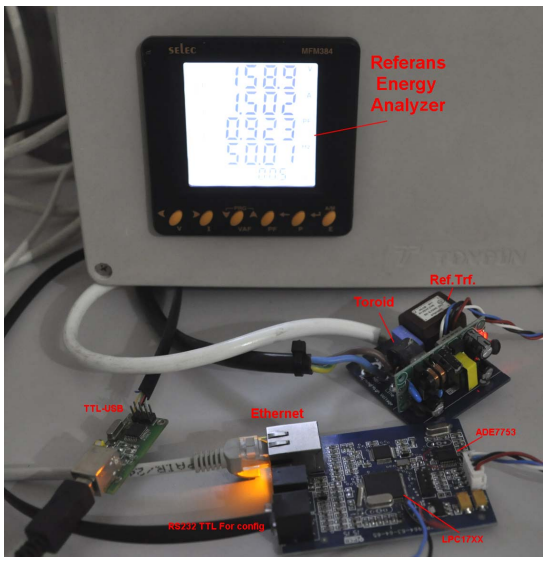

Fig. 5. Complete design of the system without the socket board

2.2. Measurement Control System and Monitoring Software

Despite the on/off switches of the electric devices on being pressed, when they are connected by a plug, this causes them to consume energy called standby current. This energy when considered in terms of individual users is low; however, in places like banks, technology markets and government offices where a multitude of electrical devices are contained, the costs are very high. In these places, switching mode power supplies are used. The main switch is capable of opening and closing of all the devices with these power supplies, but this can lead to a sudden power peak and cause network damage and accidents. Therefore, the devices are left in sleep mode as required. At the same time, opening the sequential switching mode of the devices as required.

In the study, in order to prevent abrupt changes in the voltage and current, a protection filter was designed separately for each device and connected to the system. Thus, instead of protecting the complete system, the aim was individual protection for each of the connected devices. The energy consumption was calculated with the signal coming from the network, after filtering out noise and the values from the power calculation unit according to the on/off status of the electrical devices connected to the power output controlled by the CPU. If the energy consumption limits are exceeded by the equipment connected to a socket, the CPU unit turns off the device that is connected to that corresponding socket. The complete design of the system without the socket board is shown in Figure 5. The necessary internet communications (Email, SNMP support, centralized management software) of the CPU unit manage the all the SMS disposal operations via GSM.

2.3. Working Algorithm of the System

Information on the devices is obtained by determining the power factor and its load characteristic. By performing energy calculations such as the active-reactive power factor (Cos-Fi) and by recording the power measurements of the connected devices, the measurement results for the devices connected to ADE7753 [8] can be expressed in energy measurement graphics. Web interface of the system and their sensors and metering of the equipment are shown in Figure 6.

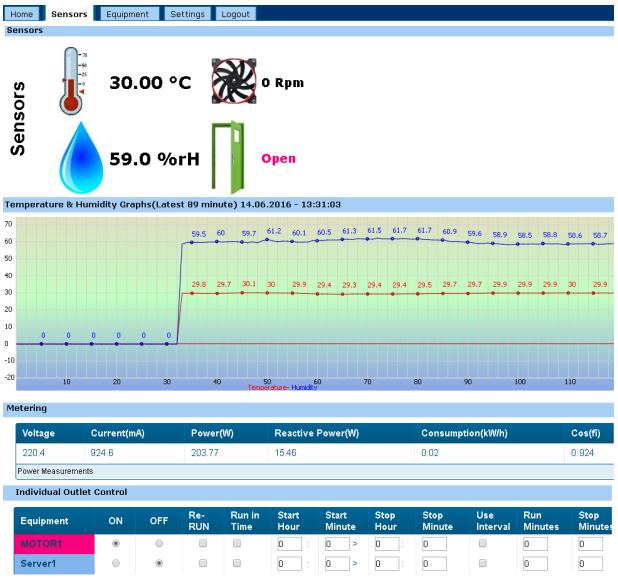

Fig. 6. Metering on the web interface

A timing function was then developed to enable the devices connected to the system to work during certain time periods during the day. This timing function provides energy savings by cutting the power, especially for devices like TVs not working at night and laser printers. However, in devices such as TVs, while the remote control remains inactive over a long period, Internet access continues to be in progress via mobile phones and local Internet or it is provided with any browser.

The properties of the timing function of the system are presented in Figure 7. One period at a certain time of day, intermittent periods at a certain time of day and intermittent modes for All day are shown in the figure.

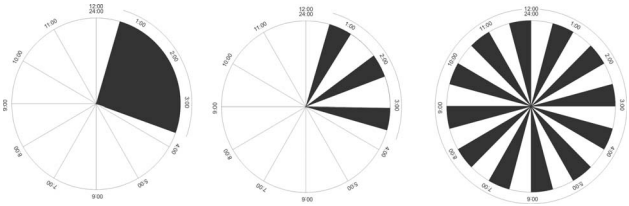

Fig. 7. Timing function block diagram

The Internet access of the devices connected to the web interface of the system and their timing operations are shown in Figure 8.

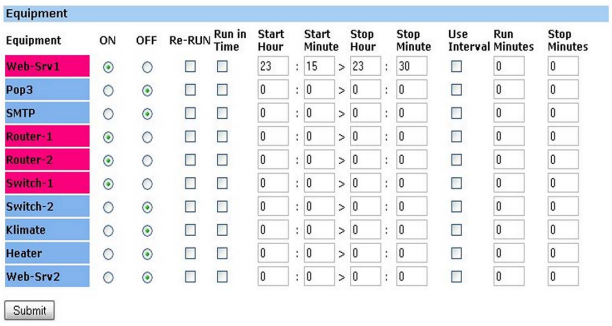

Fig. 8. Timing control of the web interface

III. EXPERIMENTAL STUDY

In the experimental study, in order to measure the contribution towards saving energy made by operating the system, measurements were taken on a variety of electronic devices in an establishment that sells electronic equipment. According to the findings of the measurements, the annual gain of the company amounted to 500,000 TL. Moreover, as a result of analyses of other measurements made for a bank, it was estimated that annual savings reached 2,000,000 TL.

The standby currents in the tests performed on the various electronic devices are given in Table 1. Annual consumption was calculated according to these data.

Table 1. Standby currents of electronic devices used in the tests

BRAND	LCD	STANDBY(ma)Current(
LG	40"	40
LG	42"	20
LG	42"	50
LG	55"	70
LG	55"	43
LG	65"	60
LG(Ultra HD)	84"	20
PANASONIC	47"	20
PANASONIC	55"	40
PANASONIC (1)	50"	20
PANASONIC(Plas	42"	60
PHILIPS	42"	120
PHILIPS	46	130
PHILIPS	47"	54
PHILIPS	55"	120
PHILIPS	55"	380
PHILIPS	55"	50
SAMSUNG	40"	10
SAMSUNG	42"	13
SAMSUNG	46"	20
SAMSUNG	55"	15
SAMSUNG	55"	40
SAMSUNG	60"	53
SAMSUNG	75"	60
SAMSUNG	65"	20
SHARP	70"	35
SHARP	80"	40

IV. CONCLUSION

As seen in the experimental results, energy saving was achieved by periodic time cuts along with the developed IP-based power distribution unit and standby energy management. At the same time, it was possible to calculate the total energy consumption costs by determining the active-reactive power factor (Cos-Fi) and the total enegy measurements. In the study, devices under sudden power surges or current overload were automatically shut off. The results of this study have revealed that by using the power distribution panel, a much higher energy efficiency can be achieved for electrical appliances and equipment in homes and offices. Four patents (numbered TR2010311, TR201308760, TR201409009 and TR201409080) were granted by the Turkish Patent Institute for products developed by the study. Consequently, continuing research conducted in the field of energy losses is seen as an important step for the future.

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On the Design of Power Quality Signal Amplifier

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Abstract – **Design and realization of power quality signal amplifier is described. The amplifier is intended to amplify a digital-to-analog converter output signal to the nominal power line voltage levels. Such an amplifier is commonly used to simulate power quality disturbances in order to test instrument performances, or to analyze the behavior of different electronic devices. The amplifier is designed according the power quality standard EN50160, i.e. the passband of the amplifier is up to the 50th harmonic of the nominal power line frequency. In the paper, experimental tests on commercial power quality instrument are presented.**

Keywords – **power quality, amplifier, power line disturbance, power quality simulator**

I. INTRODUCTION

Power Quality (PQ) is among the greatest challenges of the modern smart grids. The increased utilization of the renewable energy sources and the rapid growth of the electrical vehicles highlight the need for PQ awareness even more. Optimal power quality is defined with international standards. The European power quality standard EN 50160 [1] defines the voltage characteristics of the public electrical energy distribution systems.

Nowadays a special attention is paid to development of sophisticated and reliable measurement systems for PQ monitoring. In the last decade especially attractive are the so called "virtual instruments", which are well suited for development of flexible computer-based measurement systems. The virtual instruments are often used for research in the field of power quality. A lot of scientific papers on virtual instrumentation for PQ analysis (both for measurement or signal generation) have being published [2-8]. However, usually less attention is paid to the signal amplification, which is very important for the practical implementation of PQ signal generators. Power quality amplifiers are used to scale the signals from the PC-based (or any other type) simulators to the nominal power line levels and thereby allow realistic utilization of the generated PQ signals. Such systems can be used to test the performances of the PQ instruments, or to analyze the behavior of different electronic devices due to PQ disturbances. Moreover, a power quality simulator containing a PQ amplifier could be used for realistic PQ disturbances database creation. The need for such database is indicated in [9].

Nowadays, there are commercially available PQ generators on the market. However, they are usually too expensive, especially for the Universities. This paper aims to propose a cheap and flexible power quality amplifier solution providing satisfying output signal accuracy and low harmonic distortion.

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II. POWER QUALITY AMPLIFIER DESIGN

The power quality amplifier is intended to amplify signals generated by a power quality simulator with a "low voltage" output. The simulator can be any type of generic device capable of reproducing analog signals with nominal frequency of 50 Hz (or 60Hz) and simulate PQ disturbances according the standard EN 50160. Commonly, the simulator is realized with a Personal Computer (PC) containing data acquisition (DAQ) card with digital-to-analog (D/A) converter. The D/A converter output signal is usually standardized to a given voltage level, e.g. ±2.5 V, ±5 V or ±10 V. Such voltage levels are not directly applicable to test power quality meters and have to be amplified to the nominal power line voltage of 230V (or 110 V) prior the measurements. The block diagram of the PQ signal amplifier is given in Fig. 1.

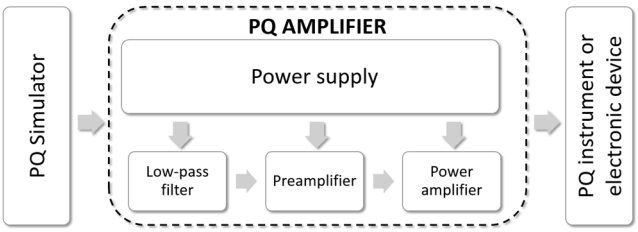

Fig. 1. Block diagram of a power quality test system containing: simulator, amplifier, and instrument or electronic device

The PQ simulator is usually a digital system which reproduces the output signal by a D/A converter. In such case, the D/A converter must meet the metrological requirements regarding the desired output signal quality. Namely, it must have well-enough resolution (which is defined by the required output signal uncertainty), and support high-enough sampling frequency. Theoretically, the sampling frequency has to be at least twice higher than the frequency of the highest harmonic that needs to be generated. According the PQ standard EN50160 (takes up to 50th harmonic), the minimum sampling frequency is 5 kHz (for 50 Hz power grids). However, in practice the sampling frequency should be significantly higher to maintain the accuracy of the higher harmonics.

The generated signal with the D/A converter is amplified by a PQ amplifier to the nominal power line voltage level of 230 V. To do so, several analog signal processing modules are used: low pass filter (restricts the input signal bandwidth and eliminate noise), preamplifier (amplifies the input signal to a given reference level and limits the input voltage level), power amplifier (amplifies the signal to nominal power line level and increase the load current capability).

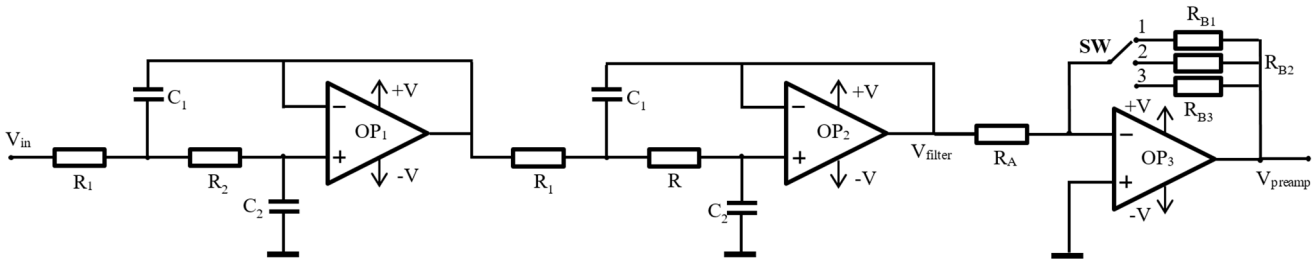

Fig. 2. Electrical circuit of an active unity gain Butterworth fourth order low-pass filter (left) and inverting preamplifier (right)

A. Low-pass antialiasing filter

The filters are characterized by several parameters: width of the pass band, attenuation in the stop band, cut-off frequency and filter order. Every filter type has its own unique properties. The Bessel filter has the most linear phase-frequency characteristics, Butterworth filter have maximally flat pass band and Chebyshev filter have the highest attenuation in the stop band but also ripples in the pass band. When designing an anti-aliasing filter it is necessary to consider the -3 dB attenuation at the cut-off frequency. If this is not taken into account, the signal will be attenuated at higher frequencies (harmonics) and the error caused by the filter at the cut-off frequency will be around 30%. Therefore, to control the errors caused by the non-ideal shape of the amplitude-frequency characteristics in [10] a *CFM* (Cut-off Frequency Multiplier) parameter is proposed. The *CFM* parameter defines a segment of the pass band where the errors caused by the difference between the real and the ideal filter transfer characteristics are controlled to certain defined level (e.g. 0.1%). It is important to note that the *CFM* value decrease with the filter order. However, the value of CFM stabilizes for a filter order higher that four and further increase carry benefit only in the attenuation in the stop band. Hence, if a Butterworth fourth order filter is designed, the value of the *CFM* parameter will be 2.18. This means that the filter cut-off frequency should be 2.18 times higher than the frequency of the highest harmonic in the signal spectrum. Hence, a fourth order Butterworth low-pass filter in a Sallen-key configuration (realized as a cascade of two two-pole filters) [11] was designed. The realized filter is given in Fig.2 (left side).

When designing a filter we must choose appropriate quality factor Q and define the cut-off frequency f_c. Considering that 50th voltage harmonic (f_{50} =2.5 kHz) has to be analyzed, the cut-off frequency of the filter is 5.45 kHz (*CFM*=2.18). The cut-off frequency is defined as:

$$f_c = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}}, \qquad (1)$$

whereas the filter quality factor is:

$$Q = \sqrt{\frac{R_1 R_2 C_1 C_2}{C_2\sqrt{R_1 + R_2}}}, \qquad (2)$$

The Q factor determines the height and width of the peak of the frequency response of the filter. As this parameter increases, the filter will tend to "ring" at a single resonant frequency near f_c. In order to implement a second order Butterworth filter the Q factor should be 1/√2. Hence, the passive components R_1, R_2, C_1 and C_2 are calculated according the values for f_c and Q by using (1) and (2).

B. Preamplifier

In the proposed solution, the preamplifiers role is to amplify the input signal (coming from the D/A converter) to a standardized reference level. The idea is to design an amplifier capable of reproducing the power line voltage with any standard D/A converter output voltage levels. This was achieved by setting the maximum output preamplifier voltage to a reference level of ±10 V. Hence, the preamplifier must have variable gain in discrete steps (4, 2, and 1 times) in order to accept different standard input voltage levels (±2.5 V, ±5 V and ±10 V), respectively. Such solution can be easily implemented with a classical operational amplifier in inverting or non-inverting configuration and with a gain selector switch. The realization of the preamplifier block is given in Fig.2.

The gain of the preamplifier is determined by the switch SW, which selects one of the resistors R_{B1}, R_{B2} or R_{B3}. The output signal can be then expressed as:

$$V_{preamp} = -\frac{R_{B_{SW}}}{R_A} V_{filter}\Big|_{SW\in\{1,2,3\}}, \qquad (3)$$

where V_{filter} is the output signal of the anti-aliasing filter. The negative sign in (3) denotes that the phase of the input signal is inverted, which is expected having in mind the inverting configuration of the operation amplifier.

All operational amplifiers in the filter and the preamplifier sections (OP_1 to OP_3) are supplied with a symmetrical power supply of ±V. In practice, these sections were realized by using a low-noise and low-offset operational amplifiers OP07 [12].

C. Power amplifier

The power amplifier role is to amplify the input signal (standardized to a V_{ref} = ± 10 V) to the power line voltage level. However, in order to be able to generate voltage swells, the power line voltage level should be placed near the middle of the D/A converter analog output voltage range. The electrical circuit of the power amplifier is given in Fig.3.

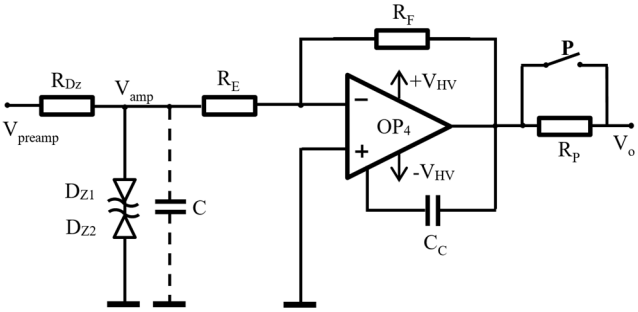

Fig. 3. Electrical circuit of the power amplifier with limiter

The input stage of the power amplifier consists of a voltage limiter formed by the Zener diodes D_{Z1}, D_{Z2} and the resistor R_{Dz}. The limiter ensures that the input voltage of the power amplifier doesn't exceed a given maximal value. This module is very important considering that the gain of the power amplifier is relatively high, and thus, it can cause saturation or even damage in case of input voltage transients (e.g. from the power supply). The resistor R_{DZ} limits the inverse current through the Zener diodes and is calculated according the following parameters: the reference voltage level, the Zener diode breakdown voltage, and the Zener diode power. In case when a voltage transient (positive or negative) higher than the maximal input reference level occurs, one of the Zener diodes is forward and the other one inversely polarized. In such case, the input voltage of the power amplifier is limited to:

$$V_{amp} = \left(V_{DZ_F} + V_{DZ_{BR}}\right) \leq V_{ref}\,, \qquad (4)$$

where V_{DZF} is the forward bias voltage, V_{DZBR} is the breakdown voltage of the Zener diodes, and V_{ref} is the maximal allowed reference level (±10 V in this case). On the other hand, when inversely polarized, the Zener diodes can inject a significant amount of noise at the input of the power amplifier and worsen its metrological performances. This can be reduced by placing the capacitor C in Fig.3 in parallel with the diodes. The resistor R_{DZ} and the capacitor C in this case form a passive first order low-pass filter that reduces the noise effects. The cut-off frequency of the filter has to be well above the PQ generator pass-band (which is *CFM* times higher than the frequency of the 50th harmonic of the power line frequency). In the current realization, a first order passive RC filter with a cut-off frequency of 22.5 kHz was realized.

The power amplifier scales the preamplifier output signal to the nominal power line voltage levels. The gain of the power amplifier is defined as:

$$A_{PA} = \frac{V_o}{V_{amp}} = -\frac{R_F}{R_E}\,, \qquad (5)$$

where V_{amp} is the input, and V_o the output voltage of the power amplifier. Having in mind that in the current realization V_o=± 400 V, and V_{amp}=V_{ref}=± 10 V, the gain of the power amplifier is A_{PA}=40 times. Hence, the values of the resistors R_F and R_E are determined according A_{PA}. As it can be seen from Fig. 3, the power amplifier is in inverse configuration and shifts the phase of the input signal. However, the preamplifier and the power amplifier compensate the phase (by double inversion), so the output signal of the amplifier is finally in phase with the input signal of the antialiasing filter.

The power amplifier was designed by using APEX PA97 [13] high voltage operation amplifier (OP_4 in Fig.3). The amplifier is capable of delivering 10 mA at 500 V (power of 5 W), which is sufficient to test PQ meters or to supply some low-power electronic devices. The power amplifier is supplied with symmetrical power supply of V_{HV} = ±410 V. The capacitor C_C serves as a decoupling capacitor which prevents amplifier oscillations. Finally R_p is a short-circuit protection resistor which can be removed by the switch P after safe wiring of the PQ amplifier. It is important to bridge R_p during measurements because it increases the output resistance of the amplifier and decrease the signal accuracy.

D. Power supply

All modules in the PQ amplifier are supplied with electrical energy from two power supply units. The antialiasing filter and the preamplifier units contain standard operational amplifiers supplied from symmetrical power supply of ±15 V. This power supply unit was designed classically, i.e. it consists of the following components: double secondary transformer, a full wave rectifier, capacitor filters, and a monolithic voltage regulators LM7815 and LM7915. Considering that this is a well-known solution it will not be analyzed in details in this paper.

The power amplifier is supplied from a separate "high voltage" power supply unit given in Fig. 4.

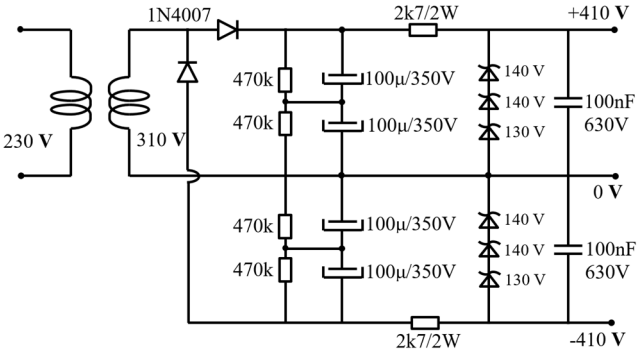

Fig. 4. Practical realization of the symmetrical "high voltage" power supply for the power amplifier module

This module ensures symmetrical power supply of ± 410 V for the power amplifier. The voltage from the power line is increased from the nominal 230 V to 310 V with a power transformer. The secondary voltage is then rectified and doubled with a diode-based voltage doubler and a capacitor banks. In the practical solution given in Fig. 4, the electrolytic capacitors are wired in series to increase the maximal capacitor voltage (due to lacking of higher voltage capacitors). In such case, the resistive voltage dividers ensure symmetrical distribution of the voltage through the capacitors. The capacitor voltage is then regulated to a ± 410 V with six Zener diodes with power of 5 W.

III. EXPERIMENTAL VERIFICATION OF PQ SIGNAL GENERATOR

The PQ amplifier was experimentally verified by using the PQ analyzer Fluke 435. The reference voltage waveforms, were generated by PC based virtual PQ signal generator [8]. The experimental system including PQ signal generator and reference instrument Fluke 435 is given in Fig. 5 and Fig.6.

The experiment was performed by using a data acquisition card NI PCIe 6343 containing analog output channel with maximal output voltage of ± 10 V. Signal with the first seven high-order odd harmonic was generated by using a virtual PQ generator with sampling frequency of 100 kS/s. The screenshots obtained from the FLUKE 435 front panel are given in Fig. 8 and Fig.9. The example given in Fig.8 represents signals with high-order harmonics, whereas the example given in Fig.9 shows occurrence of a burst transients.

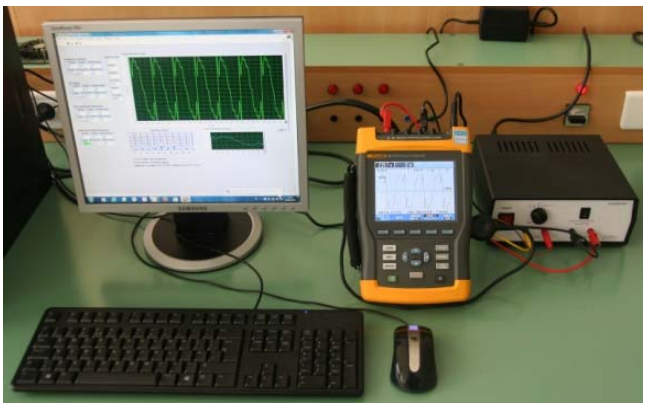

Fig. 6 Experimental system for verification of PC-based PQ signal generator

Fig. 7 Practical realization of the PQ amplifier

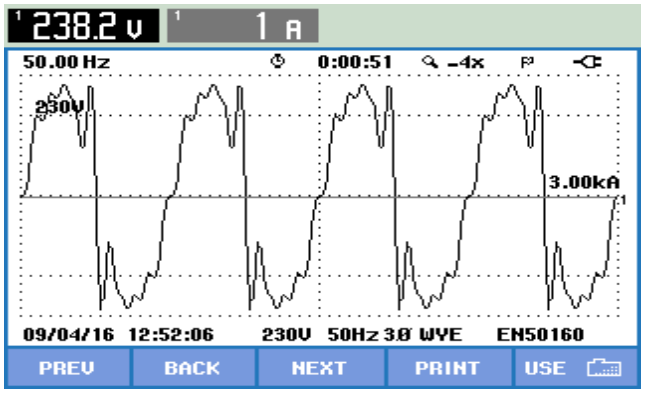

Fig. 8 Screenshot from the FLUKE 435 instrument. Signal with harmonics generated by PC and amplified with the PQ amplifier.

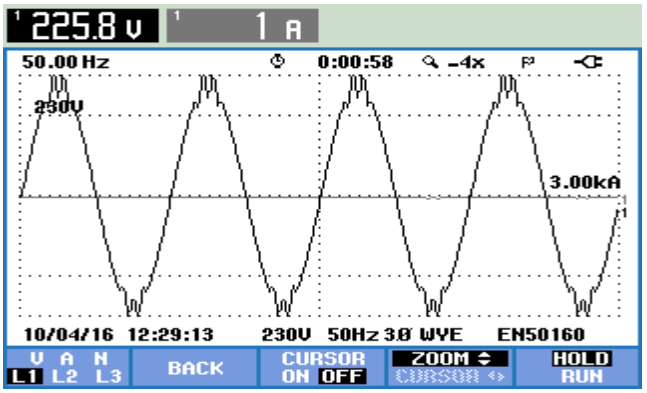

Fig. 9 Screenshot from the FLUKE 435 instrument. Burst transients generated by PC and amplified with the PQ amplifier.

IV. Conclusion

In the paper, design and implementation concepts regarding power quality amplifier were presented. The PQ amplifier was systematically conceived in three building blocks: antialiasing filter, preamplifier, and power amplifier with voltage limiter.

The antialiasing filter was realized as a cascade of two two-pole low-pass Butterworth filters in a Sallen-key configuration. To calculate the cut-off frequency of the filter, the concept of Cut-off Frequency Multiplier (CFM) was accepted. The CFM value for the filter was 2.18. In order to generate signals up to 50th harmonic of the nominal frequency, the cut-off frequency of the filter was 5.45 kHz. The preamplifier module amplifies the filtered signal of the D/A converter with standard voltage levels (±2.5 V, ±5 V or ±10 V) to a reference output voltage of ±10 V. Variable amplification was achieved with a range selector switch. The power amplifier was realized with gain of 40, i.e. it scales the preamplifier signal to the nominal power line voltage level. Simple voltage limiter at the input of the power amplifier was also proposed. Practical design considerations of the power amplifier power supply were also presented.

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Using Motion Capturing Sensor Systems for Natural User Interface

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Abstract – **This paper describes the design and implementation of a natural sensor-based interface intended for 3D graphics software packages and virtual reality (VR) environments. The interface operates through natural pointing gestures and replaces the conventional pointing devices which are usually used to interact with such software environments. It is implemented on the basis of the motion capturing sensor system (MCSS) Microsoft Kinect for Windows. The prototype integration with the 3D software package Blender as well as implementation details and challenges are discussed.**

Keywords – **Motion Capturing, User Interface, Kinect for Windows, Blender.**

I. Introduction and Motivation

Desktop computing is moving away from the Graphical User Interface (GUI) based model of interaction, towards natural user interfaces (NUI), where the basic control functions are embedded in the physical appearance and behavior of the controlled UI elements [1]. Here the term "natural" refers to interfaces, which replace conventional input through a command line interface or interface devices with communication means that are closer to the way human beings communicate.

Natural user interfaces, which can be controlled by gestures or voice for example, these days, have come to complement the most common user interfaces such as keyboards, computer mouse devices and screens [1]. They give users the opportunity to interact with computers and other technical devices in an intuitive and natural way.

Gesture based interfaces have become popular nowadays with the development of the new generation of MCSS like Microsoft Kinect, Leap Motion, Sony EyeToy, etc.

The potential of the natural sensor-based touchless way of controlling computers extended by possibilities of depth sensing has already found its place in entertainment, 3D scanning, advertising, industry or even medicine. Modern developments in the field of gesture recognition systems show that they have the potential to become an integral part of human computer interfaces and will be an interesting area for future investigations [2, 3].

The aim of this paper is to design and implement a natural touchless interface based on motion capturing sensor systems and to examine different approaches for designs of touchless interactions.

The main contributions of this paper include:

- Development of a concept for using MCSS by the implementation of NUI for 3D graphics applications and VR environments.
- Examination of possibility of using alternative data interfaces for communication between applications.
- Simulative implementation of an application which integrates MCSS with a specific graphics application and evaluation of its performance.

II. Natural User Interfaces

A. NUI Overview

Human-Computer Interaction (HCI) is a design discipline that brings together different research areas, including computer science, electronic engineering, psychology and physics. It deals with the user-oriented design of interactive systems and the interfaces between these systems and users [4, 5].

While the increase in computing power has been more or less continuous, that has not been the case with the interfaces between human beings and computers. The common view is that the human-computer interfaces have passed through several phases. These phases are not exactly defined but can be considered as the phase of typing commands (command line interface), followed by the phase of graphical user interfaces (GUI). More specifically, most computers with which people interact regularly are based on the so called desktop metaphor which is based on a common set of interface elements, usually referred to as WIMP (windows, icons, menus, pointers) [1, 6].

Increasingly, the concept of "Invisible Computing" relates to alternative natural interfaces. "Invisible Computing" refers to the transition from interactively operable to touchless automatically acting interfaces. This means that interactively operable interfaces are being replaced by smart touchless interfaces. To achieve this,

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alternative interfaces, which do not follow the WIMP paradigm, are necessary [7].

B. Gesture-Based Interfaces

Compared to the progress made in the field of speech recognition based HCI, there have been a number of recent advances in gesture processing which have made gesture-based interfaces more powerful and popular.

One of the first highly successfully gesture-based interface products was the Wii Remote. It was released in 2005 and was sold more than 6.2 million time in 2007. After Wii Remote another gesture-oriented interface with a successful release was Kinect. Other popular devices were the iPhone and iPad with their gesture-oriented touch screen functions [3].

The design of the proposed sensor-based NUI is based on the taxonomy suggested by Wobbrock et al. In their study they classify the gestures into four basic subsets on the basis of the natural behavior of nontechnical users in their interaction with computer systems. In our first design we use only two of these subsets) (TABLE 1) [2, 8].

TABLE 1. TAXONOMY OF GESTURES FOR NATURAL INTERACTION

Form	distinct path	with any hand pose
	distinct hand pose	with any path
Flow	discrete	response occurs after the user acts
	continuous	response occurs while the user acts

III. SYSTEM OVERVIEW

For the simulative implementation and evaluation of the proposed NUI concept the connection of the *Kinect* for Windows with the Blender software package was chosen.

A. Microsoft Kinect

Kinect was developed as a controller with the functionality to turn touchless body movements into actions without the need to hold additional hardware.

The Kinect MCSS is based on a depth sensing technology which includes an Infrared (IR) camera and IR emitters positioned in a certain distance between them. The principle of depth sensing is to emit a predefined pattern by the IR emitter and to capture the reflected image that is deformed by physical objects using the IR camera. The dedicated algorithm then compares the original pattern and its distorted reflected image and determines a depth on the basis of the variations between the two patterns. The resulting depth image has a horizontal resolution of 512 pixels, a vertical one of 424 and 1 mm depth resolution at distances up to 8 meters.

Additionally, the device is equipped with a color (RGB) camera with up to 1920x1080 pixels resolution, which may be used as a further data source for recognition. Another component of the device is a multi-microphone array for voice input, which makes voice source direction recognition possible. Fig. 1 shows the main Kinect sensor components [9].

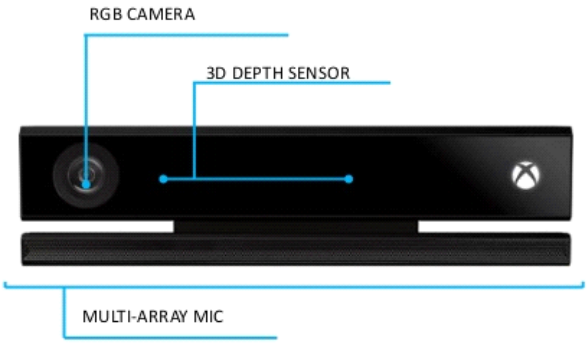

Fig. 1. The main Kinect sensor components.

The Kinect software architecture is shown in Fig. 2. It is a conventional layered architecture with the Kinect sensor as the bottom layer. Further there are the two layers for the drivers as well as for the runtime environment. The top layer forms the programming interfaces that can be addressed by applications that use Kinect. As it can be seen in Fig. 2, there are three different programming interfaces available: namely for native Windows applications, for .Net applications and for Windows RT applications.

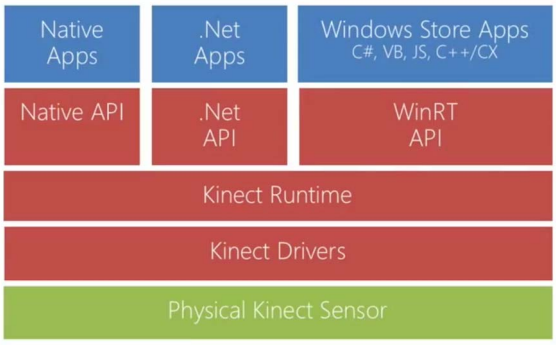

Fig. 2. The Kinect software architecture.

B. Blender

Blender is a software package aimed at supporting high-resolution production quality 3D graphics, modeling, and animation. The open source software is maintained by the Blender Foundation with a large user base and has over 0.5 million downloads per year (status 2015). The official release under the GNU general public license (GPL) is available for Linux (source and prebuilt binaries), Mac OS X, and Windows on 32- bit and 64-bit platforms.

The graphical user interface (GUI) is designed and streamlined around an animator's production workflow with a Python application program interface (API) for scripting. The final composited output can be high resolution still frames or video. The package has numerous uses for game theory and design, video editing, and graphics animation, scientific visualization, etc. [10, 11].

IV. IMPLEMENTATION

A. The NUI Blinect

In this section the prototype implementation of the touchless NUI called Blinect is described. The application structure is shown in Fig. 3.

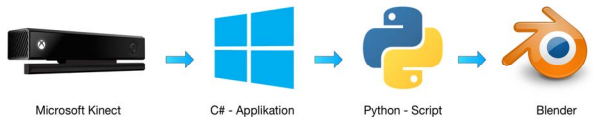

Fig. 3. Blinect application structure.

The relevant sensor data (depth, color, skeleton data) from Kinect are acquired by means of an application written in the C# programming language. The task of this software part is to filter the data and calculate the position of the right hand in a three-dimensional space. It packs this information in OSC-messages and sends them over a network to a host specified with a port and an IP address.

The Python script, which is used as a Blender add-on, implements a server that awaits incoming connections on the defined IP address and port. The server receives the OSC-messages and uses the data for the X-, Y-and Z-coordinates to manipulate the corresponding object.

Depending on the light conditions the Kinect camera records video with a framerate of 15 to 30 frames per second. The C# application sends OSC-messages to the server with the same rate. This means, that the position of the object in Blender can be changed up to 30 times in a second, which enables control in real time.

B. Communication

An important feature of the proposed approach is the use of the Open Sound Control (OSC) protocol for data exchange. The OSC protocol is used for communication between the Windows application and Blender. OSC is a digital media content format for streams of real-time audio control messages. It separates control data from stream meta-data that is essentially not time-dependent. Naturally, such a format has found an application outside audio technology, and OSC has been used in domains such as show control and robotics. It is also optimized for modern network technologies and makes it possible to develop applications that can communicate in real time [12, 13].

Normally, multiple OSC-Messages are bundled and sent together (Fig. 4). Since Blinect only uses positional information for a single joint of a tracked human body, it is enough to send one single message per recorded image/frame. If multiple joints have to be tracked, their positions will have to be sent in separate messages.

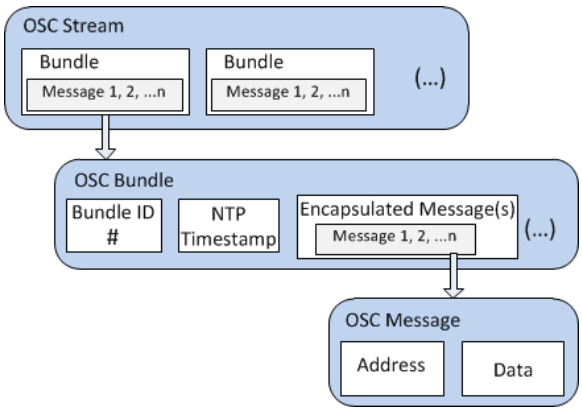

Fig. 4. OSC format.

The OSC protocol can use both TCP and UDP to send the messages. The message itself is composed of the address of the parameter that is to be modified and the corresponding parameter changes. OSC allows for much higher data transfer rates in comparison to the MIDI protocol, to which OSC is an alternative.

C. Windows Application

The class diagram of the Windows application is shown In Fig. 5. For clarity in the *MainWindow* class only the attributes and methods used for reading and packaging of the Kinect data are shown. The methods needed for the graphical representation are not included in this diagram.

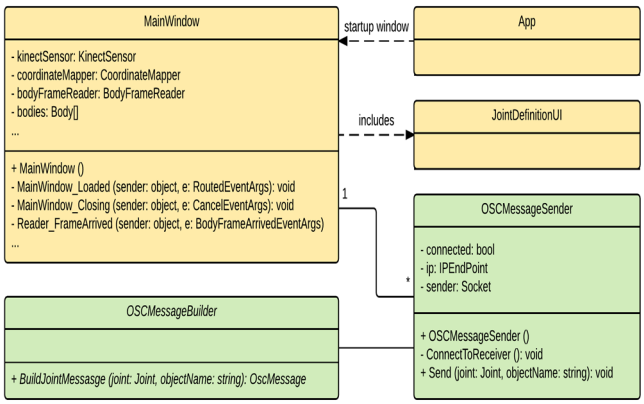

Fig. 5. Class diagram of the Windows application.

There are two classes responsible for the communication using the OSC protocol: *OSCMessageBuilder* and *OSCMessageSender*.

OSCMessageBuilder is responsible for generating an OSC message, which can then be sent. It contains a method to which the joint coordinates and the name of the object to be moved in Blender have to be passed. From the object name, an address with the Format *joint-object name* is generated.

An *OscMessage* object is created from the address and the X-, Y- and Z-coordinates of the specified joint and sent as a return value to the calling object.

Apart from the *OSCMessageBuilder* there is also a class *OSCMessageSender* available. It includes a Send method to which joint coordinates and the name of the object to be moved in Blender can be passed. The *OSCMessageSender* "knows" the IP address and the port on which the messages are to be sent.

V. Experimental Results

The user interface of the Windows application Blinect is shown in Fig. 6. In order to evaluate Blinect, multiple tests focusing on various factors were performed. Special attention was given to the following parameters:

- Different objects in Blender;
- Different distances between the testing person and Kinect;
- Different light conditions;
- Different number of users in front of Kinect;
- Different Receiver-Engines.

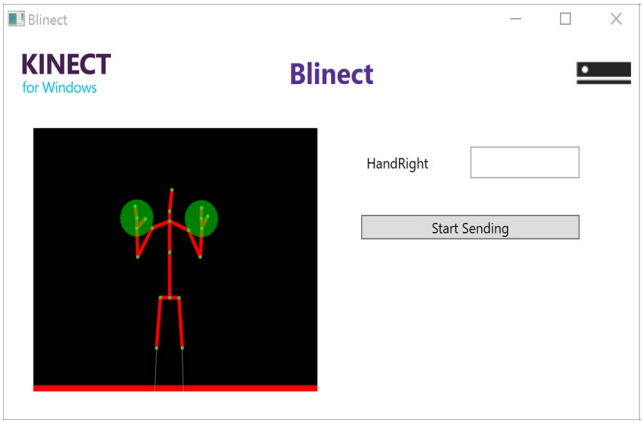

Fig. 6. The user interface of Windows application Blinect.

A. Different objects in Blender

Blinect can be used for any object. The user has only to define the names of the corresponding Blender-Objects in the Windows application.

B. Distance between User and Kinect

Blinect was tested for different distances between to the user and Kinect. The results can be summarized as follows:

- With a distance of under 50 cm the Kinect recognition does not work properly.
- When the distance is between 50 and 100 cm, Blinect is able to function but the recognition is not reliable.
- With distances between 100 and 400 cm Blinect's function is stable and without problems.
- When the distance is over 400 - 450 cm, Blinect can function but the recognition is not reliable.

Thus, the conclusion can be made, that Blinect can be used with a high degree of reliability with distances between 100 cm and 400 cm.

C. Light conditions

Blinect was tested under the following light conditions: room with artificial lighting (illuminance $150 - 1000\ lx$); room with daylight (illuminance $>\ 10\,000\ lx$) and room without lighting (illuminance $<\ 1\ lx$).

The results of these tests clearly indicate that Blinect can be used irrespective of what the light conditions in the room are.

D. Number of Users

Blinect works with one user properly. When more than two test users are present, the application is not completely stable and unusable movements of Blender object can be visible. That is why Blinect is not suitable for simultaneous use by several users.

E. Rendering Engines

Blender provides in its standard distribution two different rendering engines – Blender Render and Render Cycles and the game engine Blender Game. Blinect has been tested with these three available engines and works properly with all of them.

VI. Conclusion and Future Work

This paper deals with the design, implementation and integration of a sensor-based touchless interface with a 3D graphic software environment. The proposed design is focused on natural user interface perspective. The final implementation was based on subjective user tests that evaluated the most natural approaches for realization of the touchless interactions. The results of the evaluation are promising. The designed interface has been successfully integrated with the *Blender* application as a demonstration of using touchless interactions in a real case scenario.

With the user studies, which have been conducted we try to show that these novel technologies can help the users to complete their tasks more effectively than with existing user interfaces.

The results we have presented can be used as a foundation for further research. A possible enhancement would be the use of all 25 skeletal joints of a person for better motion capturing by using the Kinect for Windows.

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Data Acquisition System for Parameters of the Environment, Working in Harsh Conditions

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Abstract – **In this article is presented DAQ system designed to work autonomously for 1 year at temperatures as low as -40°C**

Keywords – **DAQ, harsh conditions**

I. Introduction

The environment can be described with parameters like temperature, humidity, light intensity, gas composition, magnetic field, radiation intensity, etc. In this system is chosen to be monitored temperature, light intensity, magnetic field and acceleration. All sensors are using I^2C communication interface with the central MCU. These types of sensors are compact, easy to use and have low power modes. The tradeoff is that they are usually less accurate than more complex solutions. There are many data acquisition systems (DAQ) on the market. The aim of the currently developed system is to achieve high reliability in low temperatures (-40°C) with long battery life and expected service period of one year. The ambient conditions creates some requirements: the system should have a battery capable of delivering sufficient current in -40°C, the system should have a transparent lid in order to work the light intensity sensor, the system should be enclosed in water tight box. In case of damage to the system partial or complete data recovery should be possible.

II. Block Diagram and Algorithm

The system (Figure 1) consists of a microcontroller (MCU) Microchip PIC16LF1829, 4 EEPROM chips STmicro M24M01, TAOS TLS260 digital-to-light converter, Microchip TCN75A I2C temperature sensor, Honeywell HMC5883L 3-axis digital magnetometer, Freescale MAG3110 3-axis digital magnetometer, Freescale MMA8652FC 3-axis digital accelerometer and Microchip MCP79402 I2C real-time clock with SRAM. PC command line user interface is available using optical isolated USB to UART interface with FTDI FT234XD (not shown on the block diagram for simplicity).

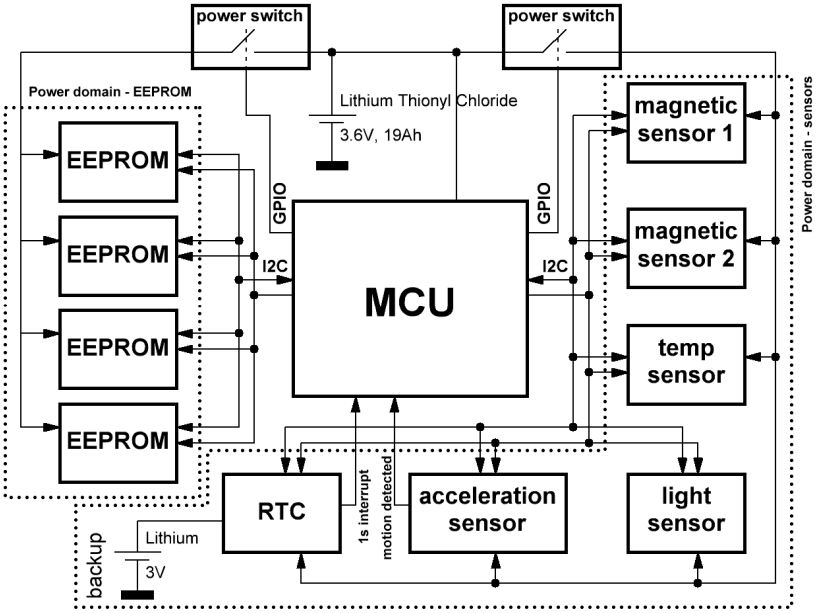

Figure 1. DAQ block diagram

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The MCU is running at 125kHz clock frequency in order to reduce the current consumption while the MCU is not in Sleep mode. The peripheral chips are in low power mode most of the time, only the accelerometer and the RTC are constantly running. The average current consumption is less than 100μA.

At low temperature battery internal resistance increases and the ability of the battery to sustain discharge current is reduced dramatically. The choice of proper battery chemistry is critical. One of the most appropriate types of batteries are the Lithium Thionyl Chloride (LTC) ($Li/SOCl_2$), they can work at temperatures from -55°C to +85°C [1]. LTC batteries have high specific energy density (~650Wh/kg and ~1280 Wh/dm^3), nominal battery voltage of 3.6V and shelf life of more than 10 years [1]. Tadiran TLP-93111/A was chosen for this design. This is size D cell, 3.6V 19Ah, in parallel with super capacitor. The expected battery life of the system is more than 10 years.

Split power supply is used for the microcontroller and the peripheral chips, part of the MCU reset/initialization sequence is to turn off the power supply for the peripheral chips for half a second. This will discharge the filtering caps and reset the state machines of the chips, leading to repeatable and known behavior of the ICs during system initialization/re-initialization. The RTC and the accelerometer are the only constantly running chips. They are capable to wake up the MCU. The RTC is waking the MCU once per second, this "heart beat" signal is used from the MCU to keep track of time, check the alarm for long term full sensor data acquisition (once per 30min) and clear for the watch dog timer. If the "heart beat" signal is not present the system continues to keep track of time using the watch dog timer. In this mode the system is reset once per 4 second, all the ICs are power-cycled and re-initialized in order to restore normal working condition. All measurements are performed normally. The other source of interrupt, the accelerometer, provides information for sudden vibration or change in orientation. This is indication for dynamic environmental conditions. This signal triggers once per second full sensor capture for 1minute if there isn't sequential high acceleration event. In case of continuous acceleration (vibrations) the system continues to record data once per second. The memory for dynamic events is 90 minutes. If the memory is full the oldest records will be overwritten. For long term measurements there is enough memory for 13 mounts. In order to improve the possibility for data recovery in case of system damage, all measurements are written to four external I^2C EEPROM chips. The EEPROM packets are 64 bytes long and containing 4 bytes timestamp and 3 measurement data (MD) packets from 3 sequential measurements (Figure 2).

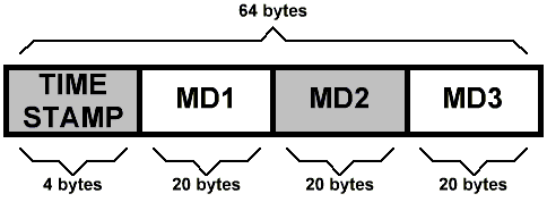

Figure 2. EEPROM PACKET

This memory partitioning leads to the following pros and cons: the memory utilization for measurement data is 93%, there is no EEPROM page change in the middle of the packet, one write cycle on every 3 measurements – power saving, one or two measurements will be lost in case of a power failure, only one third of the measurements has true time stamps, the time stamps of the other two thirds are calculated (30minute offset), fixed packet length means easy address generation – easy data recovery with external system. Additionally the EEPROM packets are interleaved in time across the 4 EEPROM chips (Figure 3), if one of the chips is defective only one fourth of the data will be lost, equally spread across the data acquisition period (13 mounts maximum).

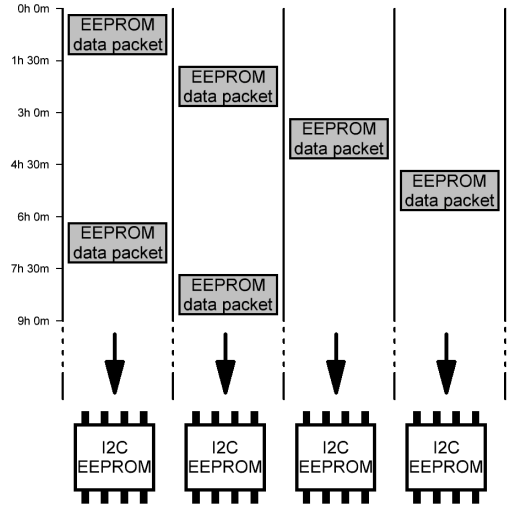

Figure 3. EEPROM PACKET SPLIT

The 20 byte measurement data packet contains 4 bytes for ambient light data, 6 bytes for magnetic field data for X, Y and Z axis, 5 bytes for the second magnetic data X, Y and Z axis in combination with 1 bit indicating the gain of the light sensor and the two least significant bits for the temperature, 1 byte for temperature, 3 bytes for acceleration X, Y and Z axis and 1 byte for battery voltage measurement (Figure 4). The acceleration and the battery voltage are non-important parameters and they are recorded with reduced resolution. The acceleration is used only to help estimate the orientation of the measurement system in the space. All measurements are stored in raw format without any data processing, in this way is ensured minimal CPU load during data acquisition. All the necessary data processing is done during data dump via the USB interface.

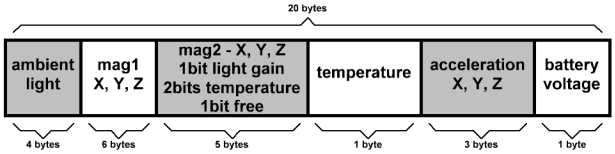

Figure 4. MEASUREMENT DATA (MD) PACKET

The firmware is written in assembly language in order to produce small, fast executing code. During the implementation the following rules were followed: no

blocking statements are used, all functions are implemented with state machines (services), all services have equal priority for the CPU time, all hardware control functions are handled by interrupts, if multiple services are requesting the same resource (I^2C) the first function detected the resource availability is using the resource, all other functions are waiting with equal priority. Unexpected state is handled with reset. Unexpected errors like NOT ACK from I^2C peripheral chip are handled according to the error priory. Some errors are ignored, others triggers reset. The extensive use of state machines have the advantage of simple, short prototype code to handle each state, easy implementation of error handling, easy implementation of parallelism. For example while one function if using the CPU for calculations, another function is transferring data via the I^2C bus. The watch dog timer is enabled, but not cleared anywhere in the code. For the normal operation of the program is necessary the CPU to enter and leave sleep mode at least once per 4 seconds (watchdog timeout), this will reset the watchdog timer. If the 1 second signal from the RTC is missing, or some of the services are stuck at some state, the watchdog will reset the CPU. The Microchip's PIC16 architecture is using banked memory, in order to ensure that the most important variables are not overwritten due to firmware bug (the bank pointer is set for a wrong bank) those addresses are reserved in all banks. One of those important variables is the time stamp. The time stamp is the current time and date in seconds from 1st of January 1970.

III. Measurement Data

Two prototype systems were produced. The first system was sent in December 2015 with the annual Bulgarian Antarctic expedition to Livingston Island. It was returned in March for data evaluation and performance assessment. Currently it is recording data in Sofia. The second system was sent with the second part of the same expedition on January 2016 and is still there, gathering data. It will be returned with the next expedition in 2017. The data from the first system indicates that it was working correctly. The light intensity sensor was set to too long integration time leading to saturation. This is clearly visible on Figure 5, during the day the temperature increases, therefore the sun is shining, but suddenly the light intensity drops, at 16 o'clock. The sensor saturation was further confirmed while investigating the raw data (the result from the ADC conversion)

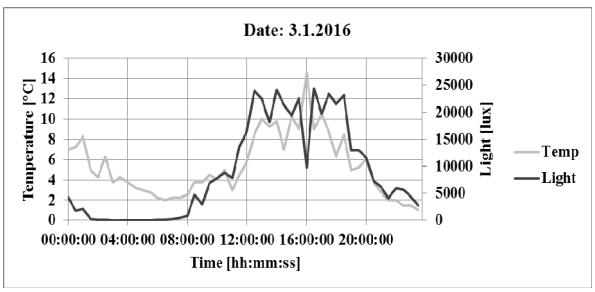

Figure 5. Light intensity and temperature

On Figure 6 is shown the average daily magnetic field from sensor Mag1 and Mag2 and the average daily temperature for January 2016 on Livingston Island. In Table 1 is shown the correlation coefficients between the same parameters at the same time period.

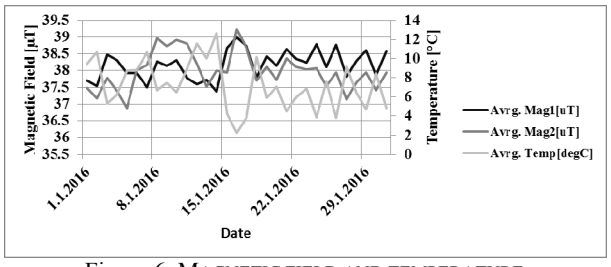

Figure 6. Magnetic field and temperature

	Temp[degC]	Mag1[uT]	Mag2[uT]
Temp[degC]	1		
Mag1[uT]	-0.9919	1	
Mag2[uT]	-0.3777	0.3922	1

Table 1. Correlation coefficients, data from January 2016

There is strong correlation between the temperature and the magnetic field measured by sensor Mag1, but the correlation coefficient for sensor Mag2 is much worse. The correlation coefficient between Mag1 and Mag2 is also low. They are measuring the same magnetic field, at the same conditions and the same time. After further investigation it was clear that Mag1 has tighter spread, less noise, than Mag2. In Table 2 is shown the sigma for every sensor axis, calculated from the measurements for January 2016 (1488 points).

	X [uT]	Y [uT]	Z [uT]
σ_{Mag1}	0.272	1.318	0.919
σ_{Mag2}	3.938	3.707	2.763

Table 2. Statistical deviation, data from January 2016

In order to reduce the effect of noise on the data analysis an average should be calculated. In this case, an average of the measurements performed on the same temperature at different time is the most appropriate. On Figure 7 is shown plot of measurements count over temperature.

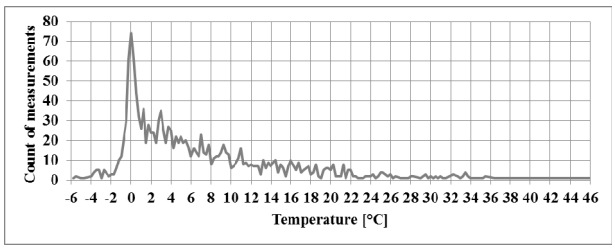

Figure 7. Measurements count at different temperatures, in January 2016

the average magnetic field from the two sensors over temperature.

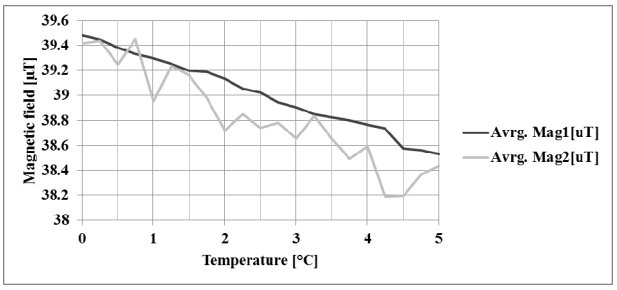

Figure 8. AVERAGE MAGNETIC FIELD OVER TEMPERATURE

If we calculate the correlation coefficients again we get the following (Table 3).

	Temp[degC]	Mag1[uT]	Mag2[uT]
Temp[degC]	1		
Mag1[uT]	-0.9963	1	
Mag2[uT]	-0.9366	0.9264	1

Table 3. CORRELATION COEFFICIENTS, DATA FROM JANUARY 2016 – AVERAGE OVER TEMPERATURE

Now there is clear correlation between temperature and Mag1, temperature and Mag2, and Mag1 and Mag2. Mag1 sensor is Honeywell HMC5883L and Mag2 is Freescale MAG3110. On Figure 9 is shown one of the assembled prototypes.

Figure 9. ASSEMBLED DAQ

IV. CONCLUSION

The DAQ system is working as expected. During the use of the system a problem with lost real time clock setting was encountered, but the reason behind it is not discovered so far. The integration time of the light sensor should be adjusted to avoid saturation. The magnetic sensors have clear negative temperature coefficient.

ACKNOWLEDGMENTS

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http://www.tadiranbatteries.de/pdf/product-data-catalogue-tadiran-lithium-batteries.pdf

Ten Dimension of Freedom Sensor Module

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Abstract –

A combined sensor system, based on MEMS, which allows measuring the temperature, and determining the magnetic field, acceleration and angular acceleration at the common coordinate system is described. Thus, the system provides a total of 10 values, characterizing 4 different physical quantities.

Keywords – **MEMS, accelerometer, gyroscope, magnetometer**

I. Introduction

Combined (Multi-parameter and multidimensional) sensors are particularly popular and sought after in recent decades. They have relatively limited application (eg. in robotics) due to their size, consumption and cost.

Recently, due to the growing use of microelectronic mechanical sensors (MEMS), the situation rapidly changed. Incorporating different MEMS created opportunities for building a compact, highly-sensitive and low-power consumption combined sensors. In terms of money the final cost of an individual product is acceptable. In terms of accuracy of the individual sensors improvement is desired. This problem is partly solved by the second generation MEMS, which have embedded high resolution analog-to-digital converters. They have a set of individual calibration and correction coefficients determined by the manufacturers in special conditions in the production facilities. This allows to improve greatly the accuracy after repeated measurements and appropriate mathematical processing of the obtained data. The additional data for the parameters of the surrounding environment (eg. temperature), allows to introduce adjustments to counter the impact of these physical parameters.

There are now available inexpensive sensor modules, including one or more MEMS, usually 3D magnetic sensor and for example 3D accelerometer. Typically, these modules do not allow to use the full capabilities of the MEMS incorporated - eg. signal conversion completed, exceeding the preset level in any of the directions. Often, when having multiple sensors, the axes of their individual coordinate systems are not aligned.

A specialized combined system of different types of MEMS is created, where measures to avoid the above mentioned shortcomings are taken.

II. Basic Design

The proposed combined sensor system includes a three-coordinate high-sensitivity magnetic sensor, three-coordinate accelerometer and three-axis gyroscope with built-in temperature sensor. Commercial MEMS are used. This makes it possible to achieve high sensitivity and very good capacity for fixing the orientation of the sensor system.

A. Structural diagram

The structural diagram of a sensor system is shown in Fig. 1. It is customary to use sensors which support the same interface system - in this case I2C. The second requirement for compatibility requires them to able to operate at the same supply voltage

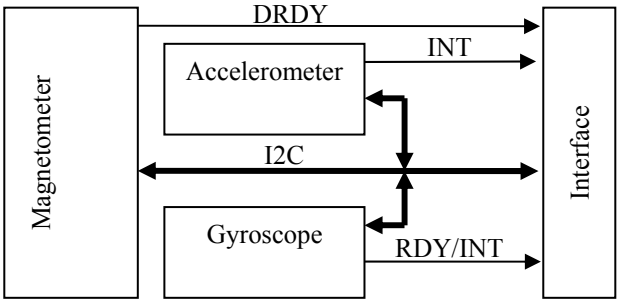

Fig. 1. Structural diagram of a sensor system

Another essential requirement is the interface should include signals that carry information about the end of the conversion, the readiness of sensor data exchange or interruption upon the occurrence of certain pre-defined events. As in the standard I2C interface such an opportunity is not provided, should be built individual connections of individual sensors to the control system.

B. Schematic diagram

As a magnetic sensor three-coordinate digital magnetometer MAG3110 [1] is used. As an accelerometer and gyroscope are used respectively MMA8652 [2] and L3G4200D [3]. When selecting attention is drawn to the following:

- Three sensors to maintain 400 kHz Fast Mode compatible I2C interface.
- To ensure stable operation at supply voltage 3,3V.

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The selected components fulfill these conditions. The schematic diagram of the combined sensor is shown in Fig. 2.

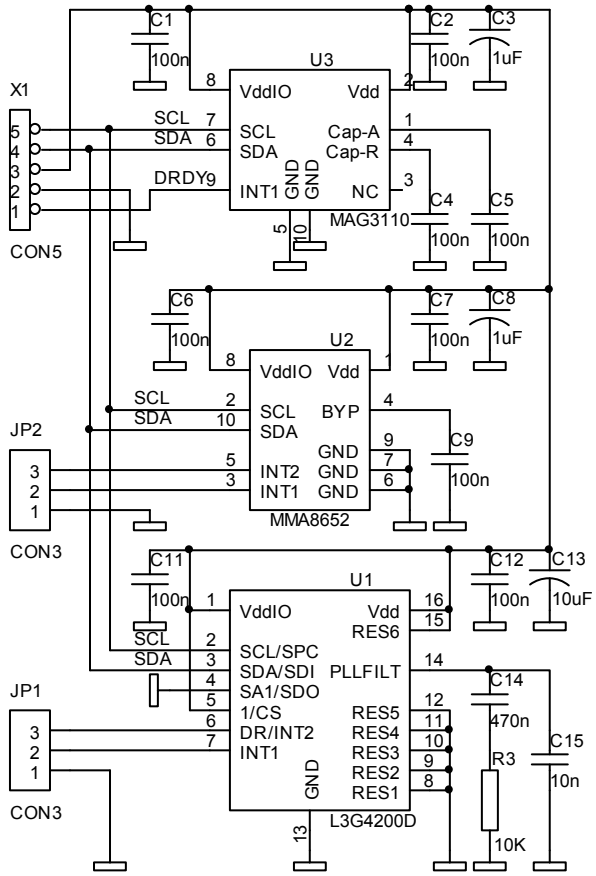

Fig. 2. Schematic diagram of the combined sensor

C. Construction

The general view of the board is shown in Fig. 3. Small size and weight, and the location of jacks allow connection to the processor board without any additional stiffening elements.

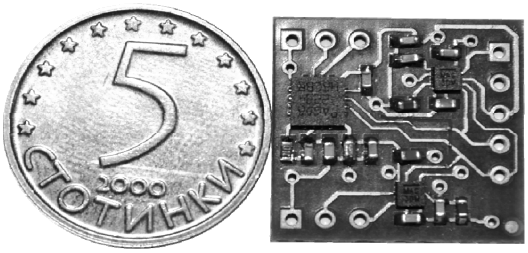

Fig. 3. General view of the board

D. Algorithms and Software procedures

Algorithms are designed and Software procedures are developed for processor series PIC18 and PIC24 using compilers MPLAB C18 and MPLAB C30 including:

a) Initialization;
b) Calibration;
c) Control of modes of measurement
d) Set parameters for tracking and recording of events
e) Procedures for detection, recognition and tracking of the objects.

E. Technical Parameters

The main technical parameters are given in table 1.

TABLE 1. MAIN TECHICAL PARAMETERS

	MAG3110	MMA8652	L3G4200D
I2C Address	0x0E	0x1B	0x68
Sensitivity	0.10 μT/LSB	1/1024 g/LSB	8.75 mdps/digit
Full-scale range	±1000 μT	±2 g	±250 dps
Output Data Rates	up to 80 Hz	up to 800 Hz	up to 800 Hz

Table 2 includes the current consumption measurements for the different sensors in the module.

TABLE 2. SENSORS CURRENT CONSUPTION

SENSOR	AVERAGE CURRENT
Accelerometer MMA8652	0,049 mA (ODR = 100 Hz)
Gyroscope L3G4200D	6,1 mA (ODR = 100 Hz)
Magnetometer MAG3110	0,137 mA (ODR = 10 Hz)

F. Field of applications and experimental results

Similar modules are widely used in:

- Inertial navigation systems of unmanned marine vessels (UMV), unmanned ground vehicles (UGV) and unmanned aircraft system (UAS);
- Robotics;
- Indoor navigation;
- Human–computer Interaction (HCI).

The proposed module is used in the systems for detection, recognition and tracking of ferrous magnetic floating objects.

Fig. 4 presents signals from magnetic sensor mounted on the sea-floor at a depth of 16 m, when passing an object that has parameters as follows:

- Length [m]: 88
- Beam [m]: 15
- Draft [m]: 3,6
- Speed [kn]: 9,8

In the figure, Hx, Hy, Hz and Hmod are longitudinal, transverse, vertical component and the modulus of the vertical magnetization of the ship. The marker shows the bow and stern of the ship.

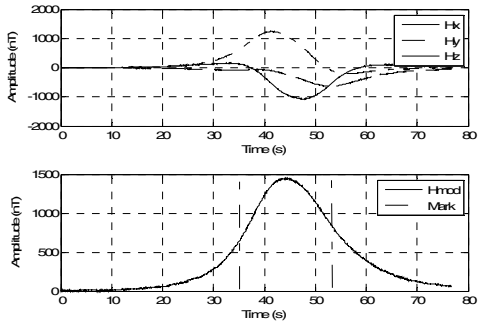

Fig. 4. Signals from magnetic sensor

On the Fig. 5 are shown signals from magnetic sensor, when the module is mounted on a floating platform, in a wavy sea, without any passing object.

An intentional interference causes similar magnetometer readings.

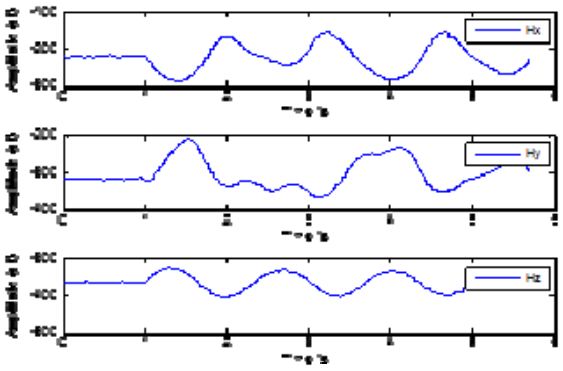

Fig. 5 Signals from magnetic sensor on floating platform.

A data fusion algorithm is developed and implemented for detecting orientation in three dimensions to improve the calculation of the heading of the ferromagnetic floating object.

An example of gyroscope and accelerometer raw data are shown on Fig. 6 and Fig. 7.

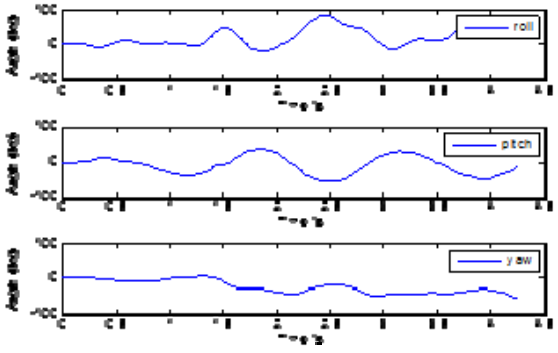

Fig. 6 Gyroscope raw data.

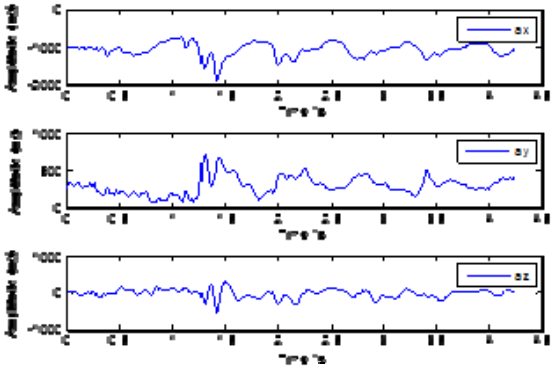

Fig. 7 Accelerometer raw data.

III. Conclusion

The combined sensor system includes a three-coordinate high-sensitivity magnetic sensor, three-coordinate accelerometer and three-axis gyroscope with built-in temperature sensor. It is suitable for embedding in the systems for detection, recognition and tracking of ferrous magnetic floating objects.

Acknowledgement

The present research is supported by the Institute of Metal Science, Equipment and Technologies, BAS.

The results are used in the system for detection, recognition and tracking of ferrous magnetic floating objects.

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System for Functional Diagnostics in the Oil Industry

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Abstract – **This report is dedicated to a new type of system used for testing electronic modules and designed specifically for the needs of the petroleum industry. After testing the electronic modules, the system makes a decision – suitable – unsuitable. Different communication modules communicate between the fuel dispensers and the POS (point of sale) system. The main goal is to raise the efficiency of the process and to decrease the price of the final product, also there will be no need of unskilled workers. The main tests of the system are being run on the communication modules – part of the communication system "BOX 69" – developed by ROHE Automation LTD.**

Keywords –**Petrol Industry, Diagnostic System, Communication Protocols, Convertor Modules, Fiscal System**

I. INTRODUCTION

"Measure what is measurable, and make measurable what is not so."
/ Galileo Galilei/

This system is designed especially for the needs of the petroleum industry. It affects the final link in the distribution of products of that indusrty. Because of the fast development and the increase of gas stations and trading points for trading fuel, the need of equipment and fuel installations for measuring and fiscalisation, increase. There is a problem, when it comes to choosing the type of the fuel dispenser and the level measuring system (TLG system). They are many types of fuel dispensers from different manufacturers. That brings up the need of wide range communication protocol support on a physical and logical level. System BOX69 allows the connection of more the one type of fuel dispensers, with different physical and logical communication interface to the POS system. Fig. 1 shows a block diagram of BOX 69 system.

Because of the different configurations, demanded by the market. The system is module based. The communication is based on a bus topology interface (fig.2).

The goal of the diagnostics is to collect information for the values of a certain number of parameters of a certain product /with a complete functionality/ or on a certain part of it /with an incomplete functionality/, to rate it "suitable – unsuitable".

If it's rated unsuitable – the cause should be pointed out.The products are being tested during their manufacturing as well during as their exploitation.

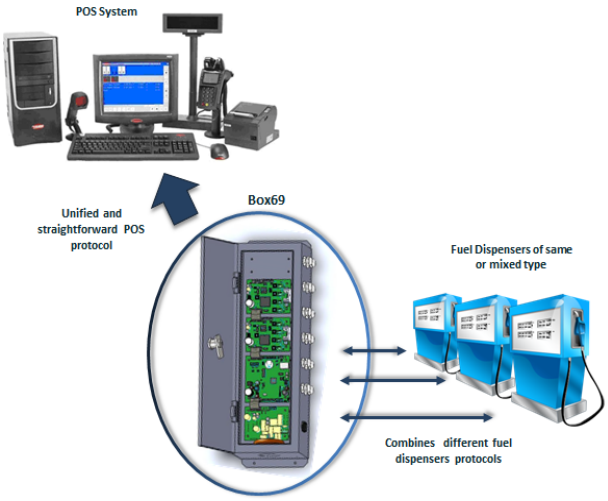

Fig. 1 – Block diagram of system "BOX69"

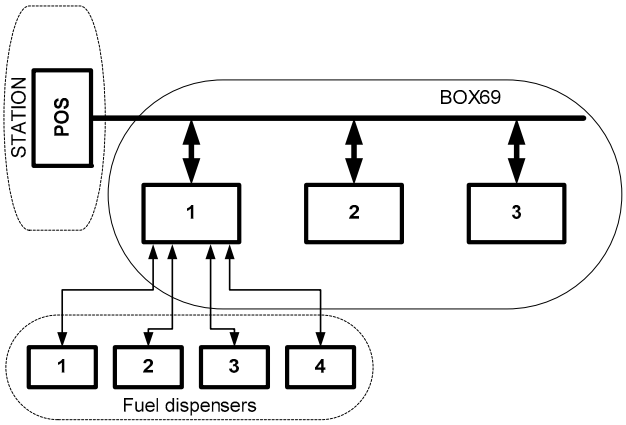

Fig. 2 – Block diagram of interface type

During their automatic diagnostic the product is being tested by an automated system, which creates stimulating signals by previously set algorithm. It measures the signals of the outputs of the tested device or in certain control points compares the results with the values stored in the memory. It rates the product as "suitable – unsuitable" and examens the "unsuitable" products for the cause of the rejection.

II. SYSTEM SPECIFICATION

A. *Automated diagnostic system*

The Automated diagnostic system includes: technical resources and diagnostic algorithms /programs/ (fig.3)

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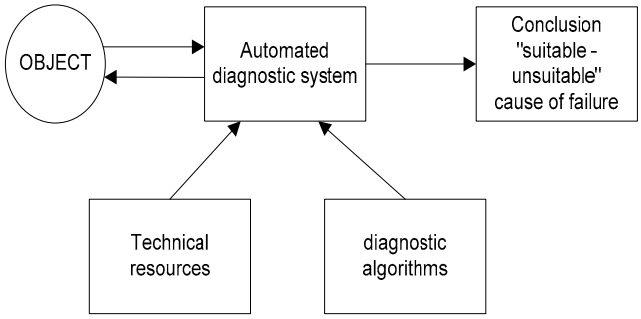

Fig. 3 – Block diagram of automatic diagnostic system

B. *Main purpose of the functional diagnostics, advantages and disadvantages.*

The main purpose of the synthesized diagnostic algorithms is to decrease the need of skilled workers.

- Reaching optimality in the numbers of the executed parameters.
- Preventative control - set to increase the reliability of the device.
- Decreasing the required amount of additional equipment.

The purpose of the diagnostic algorithms is the functional diagnosis connected to:

- Easy coupling and communication testing equipment testing facility;
- Minimising the execution time of a previously set checking with verification response type - "suitable-unsuitable";
- Simplified method of testing without the need for highly qualified personnel, which increases efficiency and reduces the costs for the certification of products;

Like any testing procedure, functional diagnostics has its flaws, some of which are:

- Complexity of checks to detect defects - especially with multiple and "illogical" (incorrectly oriented diodes, transistors, ICs, LE, etc.) malfunctions;
- Occurrence of destructive effect due to the fact that some faults at power or input signals may arise additional forcibly caused failures (secondary defects);
- Inability to detect hidden defects;
- Relatively high complexity and labor intensity greater intellectual development tests;
- Need for additional highly qualified personnel to detect damage in unfit devices without establishing a specific reason.

C. *Block diagram of test verification device*

Fig. 4 is a block diagram of the device developed for functional diagnostics. In the next few paragraphs is considered the device of integrated communication interfaces.

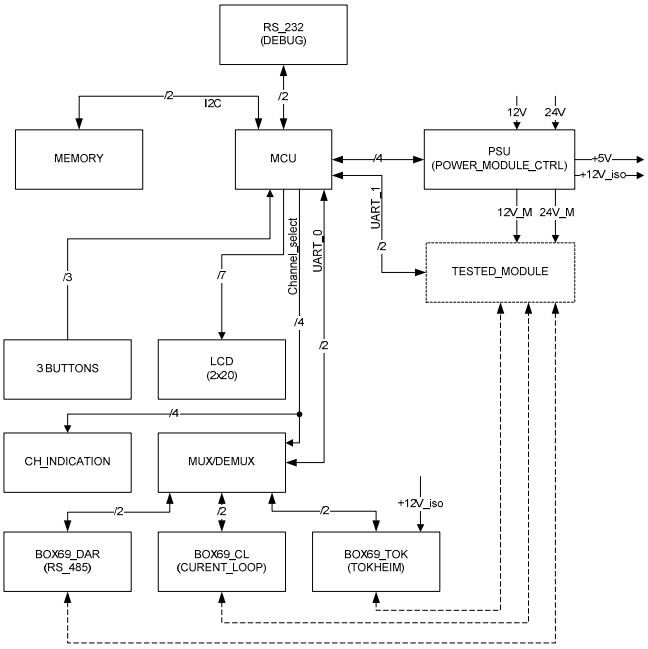

Fig. 4 – Test verification device - block diagram

D. *Exchange information with modules type DART*

The exchange of information with a type DART, is performed by a communication unit BOX69_DARh (RS - 485). The main purpose of this block is to convert data from standard TTL / CMOS signal into a signal according to standard EIA RS485. Designed for unipolar differential reception and transmission of digital information. This allows you to engage in independent parallel operation of up to a 32 transmitter and receiver 32, meaning: there can be up to participant correspondents with transfer rate up to 4Mbit / s. This calls for certain related to buffering schemes, providing larger input impedance and taking measures in case of a power shortage. [1]

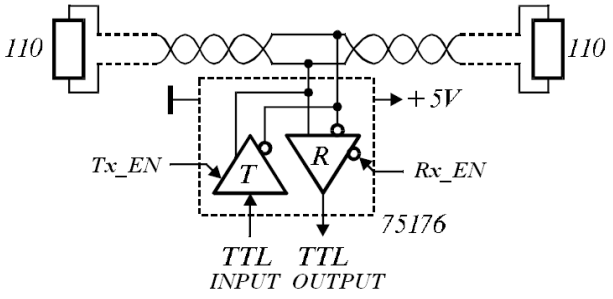

Fig. 5 – RS-485 IEE STANDART

The transmitter must have input authorization to manage its inclusion in the line and current protection in a conflict situation when more than one transmitter tries to transmit simultaneously.

Fig. 5 shows the inclusion of correspondent RS - 485 line. The line is terminated at both ends at the - remote transponder - transmitters, with its characteristic impedance. [1]

E. The exchange of information with a type BOX69_CL (CURRENT LOOP)

In industrial and hazardous areas, electronic communications available, often performed CURRENT LOOP (circuit) implemented with communication block BOX69_CL (Current Loop). The block diagram of this type of interface is shown in Fig. 6.

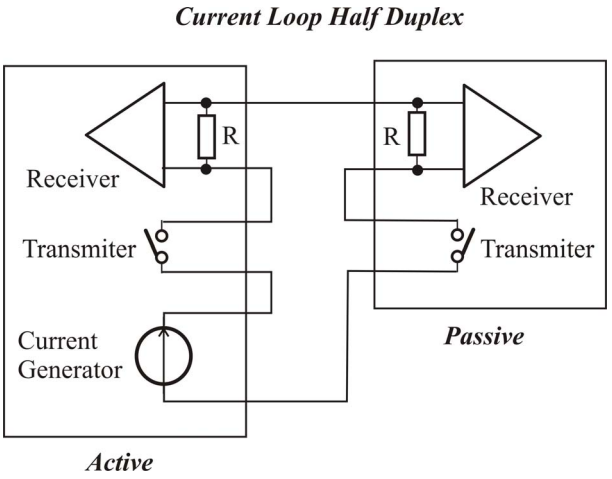

Fig. 6 – CURENT LOOP - BLOCK DIAGRAM

Test communication module must contain the active part of the scheme shown in Fig. 6. The testing module must contain the passive part of the scheme communication duplex (half - duplex - each one). Scheme tested module is shown Fig. 7.

Basic requirement imposed on the testing devices of this type is the presence of chains galvanic isolation. For tangible (because of the requirement not high speed communication protocol) is selected galvanic isolation through ordinary optocouplers with phototransistor. In the receiving part is switching implemented in two states in one of which, the receiver hears transmitted from the transmitter, the other condition, the echo is not heard.

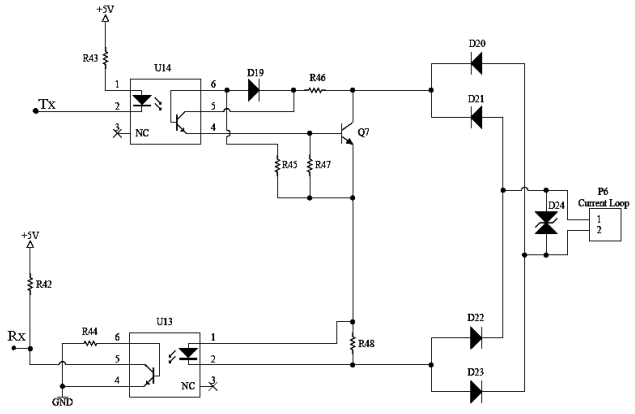

Fig. 7 – CURENT LOOP - SCHEME

In the mode of data transmission in the direction of the test module in the transistor output of the opto-isolator, become clogged, and if static mode, it is uncapped. This provides digital communication with two closely defined relative to the line states - logical "1" (20mA / 40mA) and a logical "0" (0A).

At the entrance are placed diodes to protect against reverse inclusion and bidirectional suppressor (transient diode) to protect against industrial disturbances induced in the communication line [6].

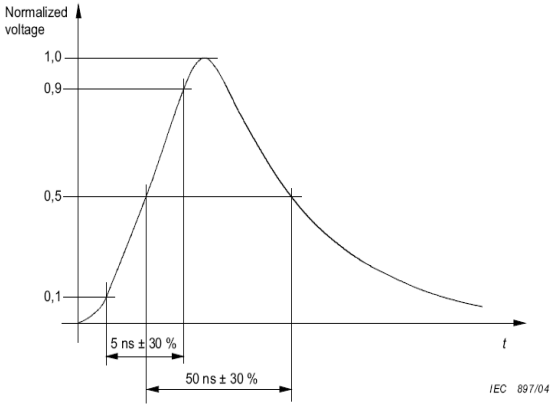

Fig. 8 - A typical form of impulse test BURST

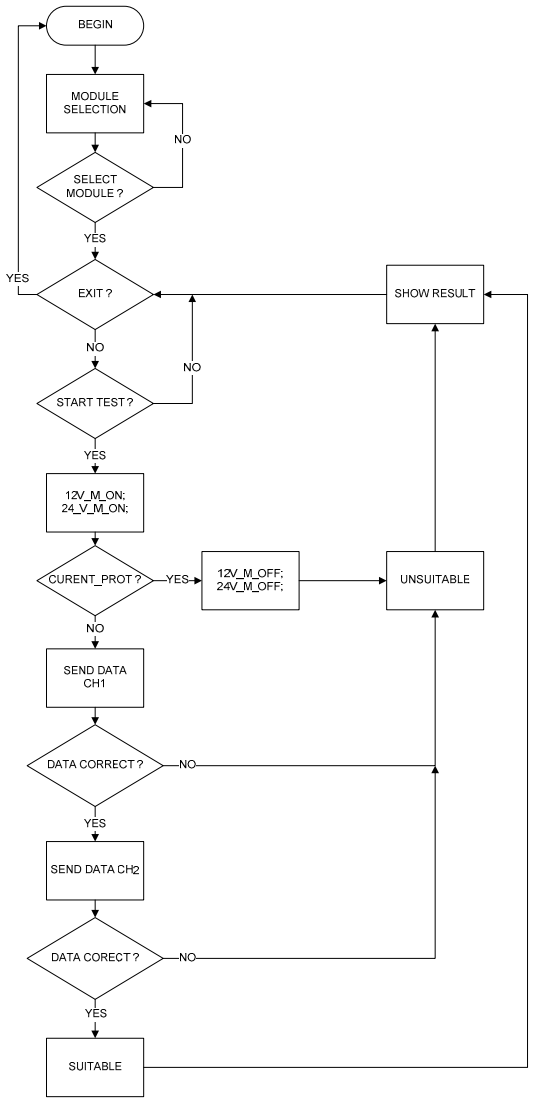

Fig. 9 - Block diagram of the algorithm for functional diagnostics communication module

The standard test form to test pulse which must withstand the test modules is shown in Fig. 8[7] [8].

In Fig. 9 and Fig. 10 shows the structural diagrams of procedures performed test operations based on the principle of the functionally diagnostics. Through this diagnostic test which is the primary certifying readiness for work and communication ability.

Functionally test diagnostics is a major initial procedure, authorization to perform any follow subsequent internal testing procedures

Fig. 10 is a block diagram of the software of the test device. The program implements sequence communication procedures implent of tests required.

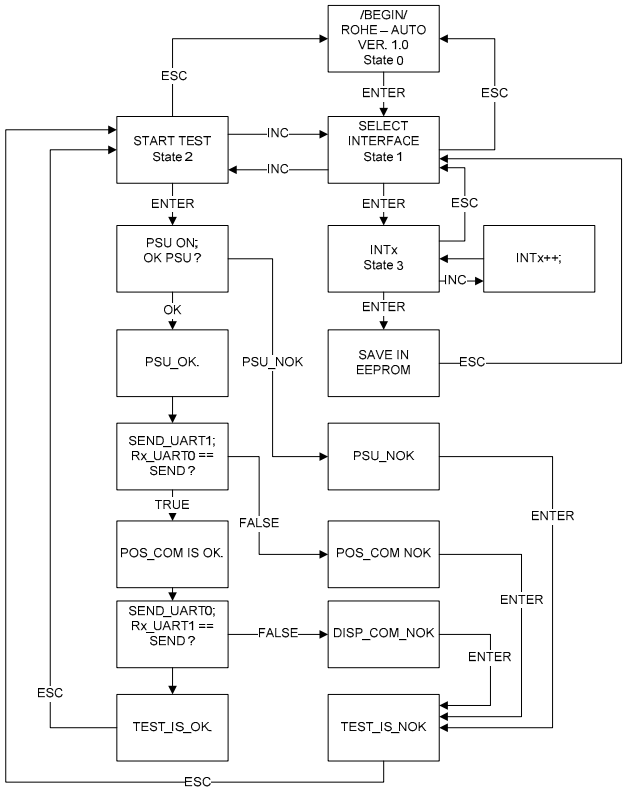

Fig. 10 –TEST ALGORITHM - BLOCK DIAGRAM

Before proceeding to the test procedure there should be selected type of test communication module. For this, there must be a separate menu, which are introduced all possible communication modules. After selecting, the module can proceed to the tests.

The testing procedure for functional diagnostics communication module consists of several procedures.

The first test procedure is checking for short circuits in the power line.

To the module is fed power supply and check the possibility of his performance through primary inspection short circuit caused by it. This is the simplest test for the possibility of performance.

Starting with switching power module and check the indicator signals for shorting in the power lines. When have short, off voltage supplied to the module and establishes result "unsuitable." Failure protection is extended to the next test.

After verification of power, check the communication line of the fiscal system to the dispenser by sending data. Data is sent via a communication channel input and expected output. Upon receipt of valid data, they are compared respectively with the same data, the test is valid and passes to the next testing procedure. When invalid data is displayed result is "unsuitable." The operator must lift the tested module production test and pass a test of the next module.

Upon successful test of communication of the fiscal system to the dispenser proceed to test the communication line in the opposite direction - from the column to the fiscal system. Again, as above algorithm deciding on the type of "suitable - unsuitable" and displays relevant results. If all test procedures were successfully completed, tested module is declared "suitable." Otherwise, the unit is defined as "unsuitable" and sent to the repair facility for detailed diagnostics and repair. After the repair, the unit must be subjected to the test again.

Block diagram reflecting more detail the operating principle of the testing algorithm is shown in Fig. 10.

The code is written in C language. The compiler is C18. Integrated development environment (IDE) is MPLAB 8.92.

III. CONCLUSION

In the publication is viewed a system for verification of electronic modules designed specifically for the needs of the oil industry. Verification of test modules through the system with a view to taking a decision on commissioning. The decision of the system is attestation principle of the " suitable - unsuitable". Discusses communication modules communicate between fuel dispensers and single fiscal system. In this study achieved the primary objective - increasing the efficiency of the production process. Lowering the cost of service of the final product and is no longer necessary service highly skilled workers, while product quality is maintained. Actual tests of the system are made of tested modules - part of the communication system type "BOX69", produced by "ROHE Automation" LTD.

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Realization of Adaptive Weather Station for Work in Antarctic Conditions

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Abstract – **This paper describes the realization, calibration process and initial experimental data analysis of the prototype version of adaptive weather station. The device relays on an ultra-low power micro architecture and adaptive power distribution mechanism. It is dynamically reconfigurable for working in high performance, real time transfer mode with direct operator control; and ultra-low power, fully autonomous, self-monitoring, long-term measurement mode. For convenience the collected data of the environmental parameters could be initially analyzed and visualized by specialized end-user software tools.**

Keywords – **Weather Station, Ultra-Low Power Management, Self-Monitoring, Dynamically Reconfigurable, Global Warming, Data acquisition**

I. INTRODUCTION

Monitoring of the ambient parameters is important task for a number of activities. This includes, but is not limited to, studying the weather and the climate, preparing whether forecasts, collecting reference data for other studies, for aviation and navigation purposes, etc. Each of those tasks requires specific monitoring and/or logging system.

Typically, for studying the climate changes, is necessary to analyze data from long-term measurements of the environment parameters (like temperature, barometric pressure, humidity, etc.). The data from the daily measurements are then logged in sets of different time frames (in conditions defined by World Meteorological Organization [1]) and analyzed to define the tendencies in the climate changes.

At the same time collecting a reference data for other studies requires measurements to be focused on current weather conditions. In this case is used equipment allowing monitoring of environmental parameters in real time – measurements are done continuously, and a suitable interface is provided for communication with the user and/or other systems. Data from these measurements can be then used as a reference in order to take into account possible errors in the further processing of data from other measurements taken in parallel or used as an input for other systems.

In order to support a research of Bulgarian Antarctic Expedition was requested to provide systems for environmental control on two different bases – measuring environmental parameters in real time as an aid to perform parallel measurements; and securing long term environment measurements in order to log statistical information on climate changes during the winter season. These conditions make two contradictory system requirements. The first ensure monitoring of a wide range of parameters, where the high performance of the system is priority; and the second – long-term measurements, where the total power consumption should be as low as possible. The last one requires a great reduction of the parameter count and a data logging rate, which are a priority for the first one.

The optimal solution is to create an adaptive compact system that ensures all the necessary measurements to support experiments performed in real-time (respond within specified time constraints [2]) and able to autonomously provide series long-term measurements, by dynamically reconfiguring its working rate.

II. DESIGN OF THE DEVICE

A. Hardware Design.

Key factors affecting the development of the system with the specified requirements are the working conditions under which the system operates, power consumption, autonomy and cooperativeness. A special feature is the combination of high power consumption real-time monitoring system of the environmental parameters and minimum power consumption requirements for long-term measurements. For the purpose of which was developed a specialized power control system that could isolate from the power source all unnecessary subsystems, for the duration of their passive states, and switch them on again when necessary. Management is fully electronic, as the specifics of the working conditions do not allow use of mechanical switches or moving parts.

Figure 1. Prototype presents the prototype of the weather station.

The control subsystem is based on a microcontroller and includes user interface for direct work with the system, interfaces for data transfer with other systems, real-time clock, and a data memory.

The Device has USB interface designed for direct transmission of data to the computer systems, so the operator can monitor real-time measurements.

Real-time clock provides a time stamp required for the synchronization of the measured parameters with a global database.

The sensor subsystem contains all the necessary sensors and peripherals required for the operation of the station. Sensors are prioritized and divided into 2 main groups.

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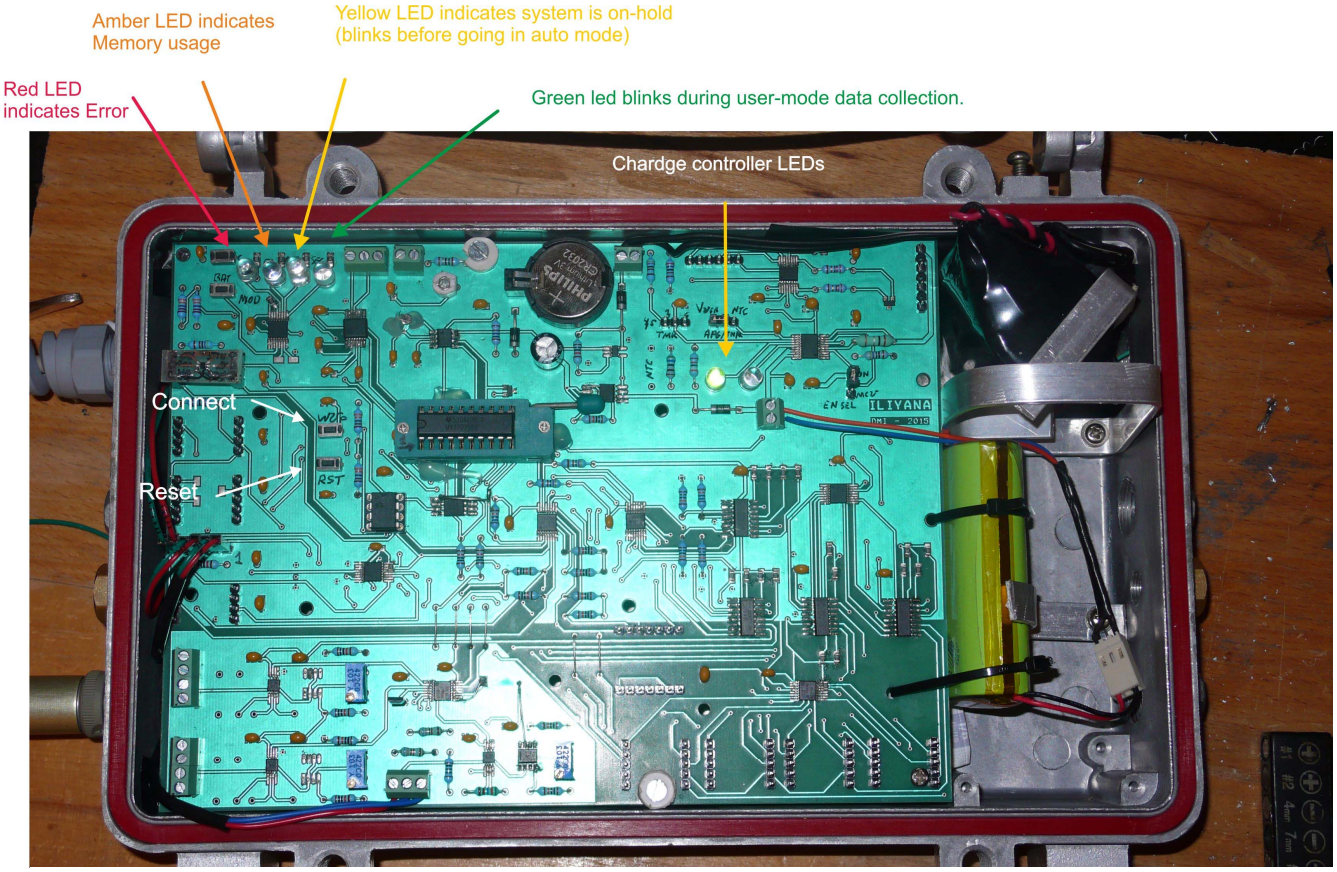

Figure 1. Prototype of the Adaptive Weather Station

The first group contains the basic sensors for the station – temperature sensors, pressure sensor, and temperature compensated humidity sensor.

The second group of sensors is used for the purposes of the research. It includes an accelerometer, a light sensor, and a magnetic field sensor.

The sensor subsystem includes three expansion interfaces for adding additional sensor modules. The interfaces are equipped with controllable power supply, two analog inputs, a digital interface for data transmission, and two digital ports with general purpose.

B. Firmware Design

System management is executed by embedded software, including algorithms for determining the operating modes of the system (autonomous control or subordinate work), powering the sensors, synchronization, error detection, analysis and reconfiguration of the operating modes, the data logging and transmission.

There are three main algorithms that build the firmware:

- Self-diagnostic
- Power Management
- Data collection

Self-diagnostic algorithm is executed during the first (diagnostic) system scan after restart. Its main task is to check the system health status and to configure appropriate working mode. It is executed in two phases.

Component detection - during this phase firmware is scanning all peripherals within the system. Each scan is performed for a predefined period of time (2x sensor's maximum response time); if a response does not appear during this time frame, the program cancels the scanning process, flag the sensor as unusable, and log an error message. Once detection scanning is completed a watchdog (WDT) starts monitoring the system during its normal operation. Component detection is performed only once after restart, as this is high power consuming operation. If sensor fails during normal working mode, WDT will restart the system and the failed sensor will be detected during new diagnostic scan.

Error detection – this phase is active during the normal operation mode of the system. It logs all errors that could appear – mode change, reset, manual scan requests, inappropriate user configurations (invalid input data, syntactic error, invalid command, etc.), data memory overflow, etc.

Power Management algorithm is executed immediately after initial initialization and have the responsibilities to perform power-up and power-down sequences necessary to prepare the peripheral devices for work, and to switch them off to save the power. This program is in direct service of data collection algorithm. Additionally, this program monitors the traffic upon the user interfaces and can change the working mode from user-controlled (UI Mode) to autonomous if a defined time of user inactivity expires, and vice versus if the user request control. In cooperation with Data collection algorithm, Power Management also monitors the battery status, and can switch between primary and secondary source depending on the battery levels. It can also cut down the power exhaustive sensors, if

the secondary source drops below predefined thresholds, and keep the system active for longer periods.

Data collection algorithm is the main program that is running during normal operation mode. Its main task is to collect data from the sensors and record them in the embedded memory. It also provides vital data for Power Management and Self-diagnostic algorithms in order to keep them function properly. It is also responsible for user communication and all data exchange including acceptance of control commands and data conversion for real-time user usage.

C. PC Application (Offline tool).

A specialized computer application is designed to provide easy control over the station during the real-time operation, and easily retrieve data collected during long-term measurements.

The application enables direct recording and storing data obtained during real-time operation of the station. It can be processed immediately and visualized on the display for direct monitoring and / or exported as a file for further analysis. It also provide current device status data, and set of options for configuration setup.

III. CALIBRATION

Essential part in realization of data acquisition systems is calibration of its sensors in order to achieve maximum accuracy. Although all sensors could be fine calibrated, this process is intended to the custom designed analog sensing elements like platinum RTD.

On Figure 2 is presented the calibration graph of the platinum RTD (temperature value as function of LSB).

The calibration of the front-end electronics consists of performing multiple measurements over set of calibration resistors and defining the average value and standard deviation per each resistance. For building the calibration function are used 48 different resistors that correspond to exact temperature value, as defined in the RTD's lookup table.

As a result we achieve a linear equation that describes the measured temperature as function of the LSB:

$$y = 0.221811x - 372.615678$$

Where the coefficient of determination is:

$$R^2 = 0.999947$$

This result premises the use of linear equation.

IV. EXPERIMENTAL DATA

Some initial experimental data is shown on Figure 3. It is collected during setup process in the base camp at Bulgarian Antarctic base on Livingston Island. The graph presents the correlation between the humidity (the top line with right axis) and temperature (middle graph is from platinum RTD and lowest is from TMP112 smart sensor).

The two temperature graphs have identical trend lines, where the TMP112 is around 0.5°C lower than platinum RTD, which is matching the specification of the sensor [3]. TMP112 is measuring the temperature inside the device case, and due to this its graph is smoother. The graph of the platinum RTD has some peaks due to its higher sensibility and because it is measuring the temperature outside of the device case, where is affected by sudden airflows and/or radiation. The peak to peak deviation of the platinum RTD is within the range of one LSB, which also match the device specification and does not affect the accuracy.

The shape of humidity graph is similar to the RTD's one, and the reasons are the same – it is outside of the case. Trend line is correlating with the temperature, which is exactly as expected.

The device is equipped with a third temperature sensor, which is measuring the temperature inside the microcontroller.

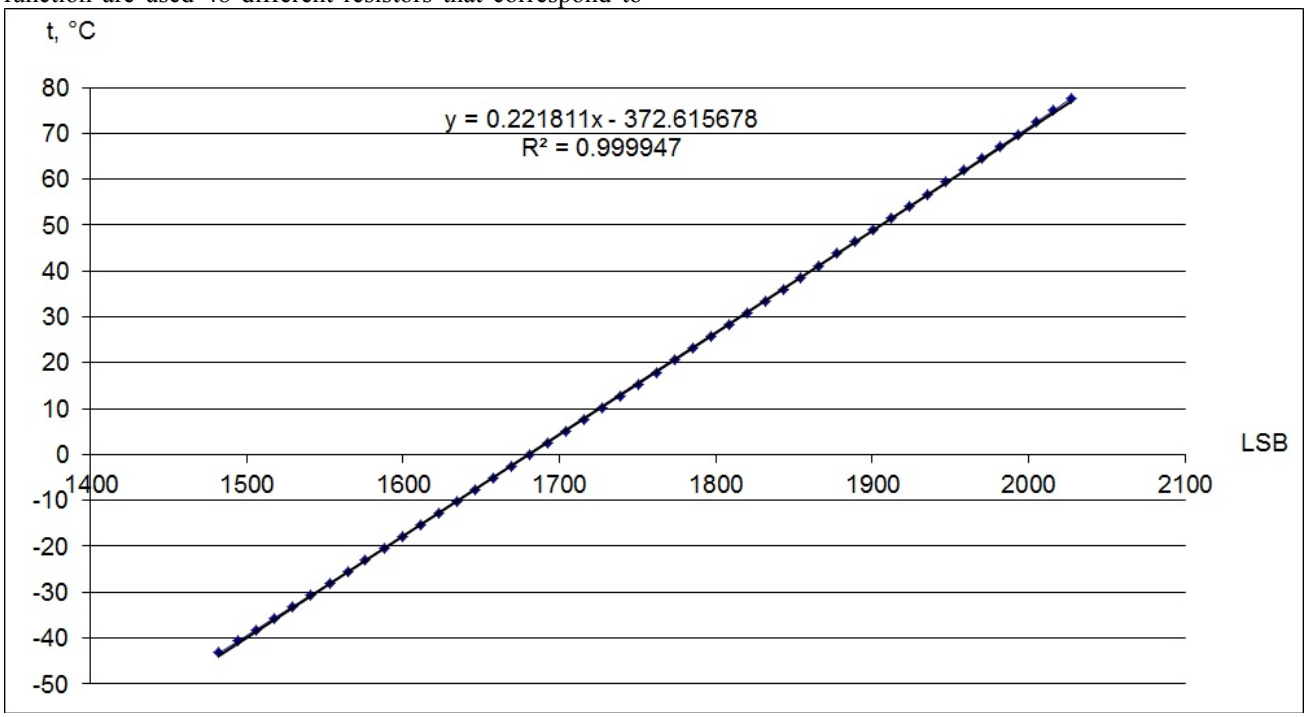

Figure 2. RTD calibration graph

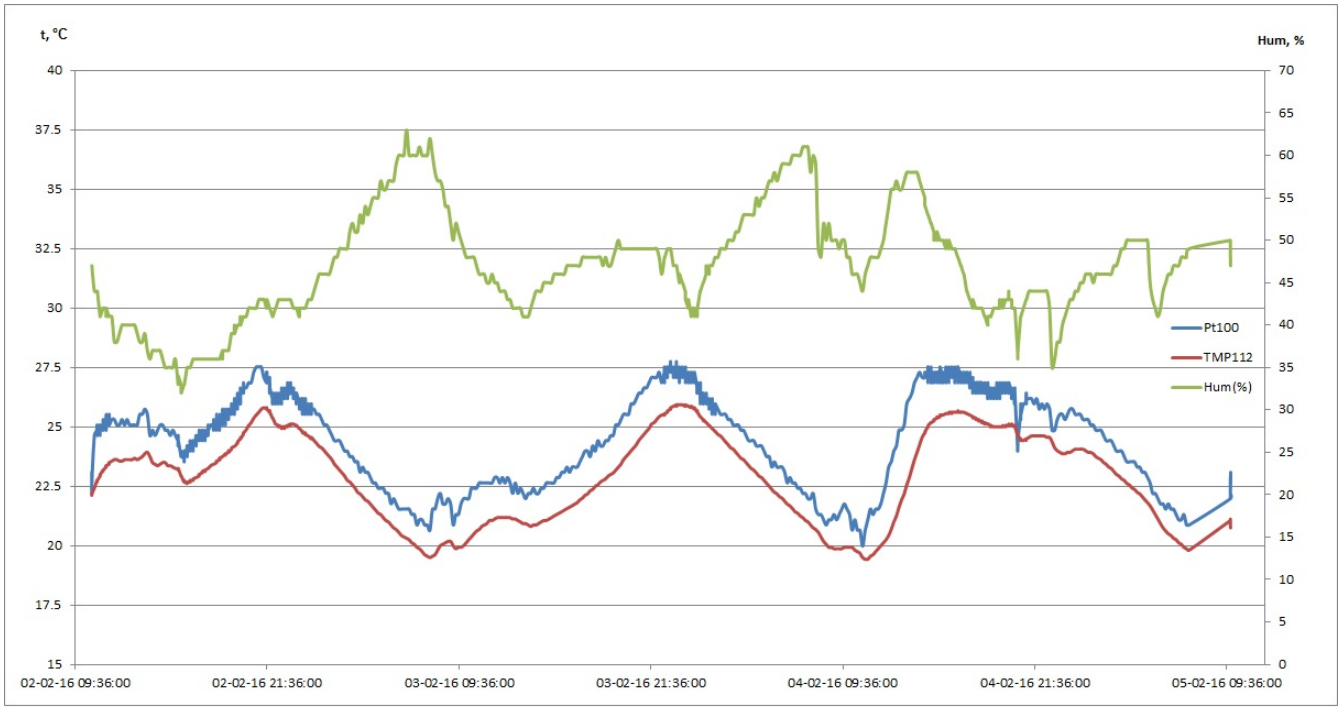

Figure 3. Experimental data

Although this internal sensor is recording temperature, its data is more valuable in term of logging microcontroller activity. As the graph on Figure 4 shows, the internal sensor indeed follows the trend line of the temperature (RTD's line shown here for reference), but the deviation is higher and accuracy is way lower. Interests here are the area of high disturbance, where the internal sensor data have big amplitudes. These periods actually corresponds to the timeframe when the device is under direct user control and works in high performance. The status log messages are shown on top of the graph and actually indicate the events like mode change and manual log requests. This effect on the internal temperature sensor is expected, as the microcontroller is running at full performance during user mode and generates more heat.

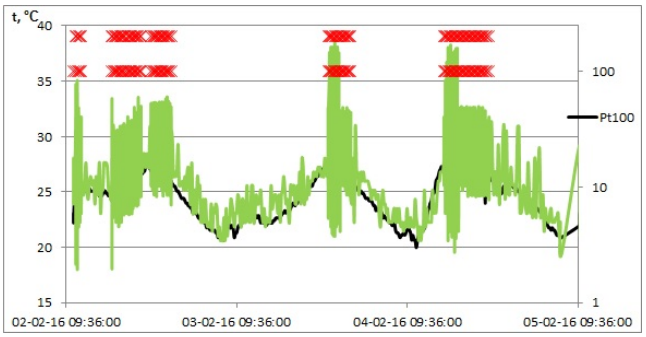

Figure 4. Status data

V. CONCLUSION

First prototype of the adaptive weather station was built and sent to Bulgarian Antarctic base on Livingston Island, during 24-th Antarctic expedition. The system was set in autonomous mode and left to collect data during winter season. The results are expected to be collected during 25-th expedition in the end of 2016.

For a future evaluation of the project in aspect of software environment is planned development of specialized online tool that will be able to transfer the data from the system through web application.

For the evaluation of the project in aspect of hardware design is planned development of a specialized anemometric system without moving components that will be capable of measuring high-speed winds in harsh arctic environment.

ACKNOWLEDGEMENT.

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The authors would like to express highest gratitude to S. Chakalov, V. Popov, and Ts. Popova for their invaluable input.

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Actual Sun Position Determination for Smart Solar Panels Orientation Management

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+*Abstract* –**The paper presents a technical solution for actual sun position determination that is used for smart solar panels orientation. The system is comprised of multiple sensor units, real-time clock module, motor control DAC module and wireless RF module. The signals from the photodiodes and the mathematical calculations based on the RTC system data, along with the solar panel temperature and sun radiation measurements as feedback for the system, form together a data stack which is used for the development of an algorithm for intelligent solar panel orientation management.**

Keywords – **actual sun position, sensors, sun position calculations, panel orientation**

I. INTRODUCTION

Solar energy is one of the most important sources which used to produce power, without pollution compared with the conventional source of fossil fuels [1]. Considering the keystone rate at which fossil fuels are consumed today, studies [2] suggest that most of the known reserves of fossil fuels are likely to get exhausted by the end of this century. Energy crisis, as evinced by frequent power solar radiation is usually converted into other forms of energy such as thermal and electrical energy. Using solar panel systems to produce electrical power is still one of the best ways to exploit solar energy. The growth of solar panel cell technologies is still rising.

Increasing the efficiency of photovoltaic systems is possible by implementing sun-tracking systems which can deliver 40% more energy compared to static ones [3, 5, 6].

For the implementation of such system an optical sensor or array of sensors for measuring sun angular placement and other values are needed. The proposed solution is based on optoelectronic sensor block as well as on other sensors for measuring temperature and solar radiation. The presented system is based on microprocessor which has integrated software functionality for calculating sun position using mathematical calculations. The measured values for sun radiance, temperature and angle of displacement are also processed. By analyzing and evaluating results from measured and calculated values, maximum accuracy should be achieved.

II. PRINCIPE OF OPERATION

A. Block Diagram

The system is based on microcontroller which offers the needed basic and peripheral functionalities. Fig. 1 shows the block diagram of the system.

The microprocessor unit chosen for the research and development process is MSP430F5529 from Texas Instruments. It offers a built-in 12-bit ADC with analog multiplexer on its input and two independent hardware communication modules which can be configured to various interfaces. Along with the key features described

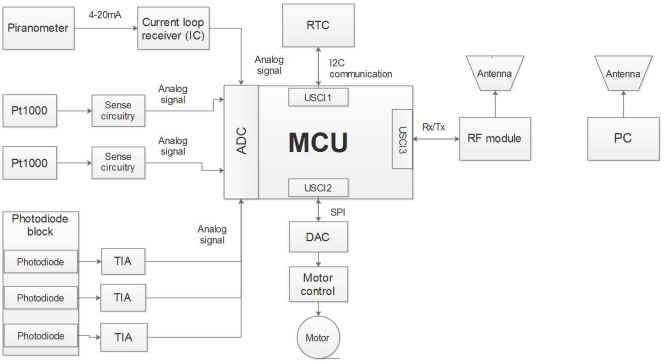

Fig. 1. Sensor Block Diagram

above it has reasonably low consumption and high performance. The MCU unit has to sample signals from the photodiode block, temperature sensors and pyranometer. The signals from all these sensors are processed and conditioned to voltages within the range of the ADC.

The pyranometer used is a ready-made commercial device with 4-20mA output and 0-1500W/m^2 range. Its output is received by a current loop receiver integrated circuit which converts the current output signal into voltage.

The used temperature sensors are industrial PT1000 which are connected to typical sense conditioning circuitry for RTD sensors. Again the voltage levels are set within the input range of ADC.

The photodiode sensor block is based on three photodiodes which are arranged at different angles. Three transimpedance amplifier circuits are used to gain, filter and convert the low current signals to usable voltage signals which are sampled by ADC.

Another keystone in the system design is microcontroller communication with the peripheral devices. The ones already included in the design are RTC (RealTimeClock) device, DAC and RF communication module.

The RTC device is a monolithic integrated circuit with can deliver date and time values through I2C interface. The device is autonomous of power, it uses a huge capacitor for power source in standby mode and a 32768Hz oscillator.

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The digital-to-analog converter is an integrated circuit which is controlled from the MCU through SPI interface. The converter is 10-bits accurate and its output is used as control signal for motor control device which is not an object of this development stage in particular.

The RF module provides wireless serial RS-232 interface between a PC and the microcontroller. This functionality is extremely helpful and irreplaceable for the appropriate adjustment when setting the system control.

B. Theoretical sun position determination based on mathematical calculations

Methods of theoretical calculation of the sun position as a function of position and time are called "passive". Over time mathematical formulas are composed, in which by using information about the time, day and geographical location, it is possible to calculate the exact position of the sun in the sky. Determining factors when making calculations are leap years and differences in summer and winter time.

Earth is constantly changing its geometry to the sun, which determines the need of angles calculation of sun incidence for any particular point in tim. In daily practice time is set by a certain date (day of the year) and an hour a day. Using these parameters carry out the necessary calculations for the direction of the sun are done. The parameter declination (angle of incidence) δ - (1) is introduced.

$$\delta = 23{,}45° \times \sin\left[\frac{360°}{365} \cdot (N + 284)\right], \qquad (1)$$

where N is the number of day of the year, counting from the 1 January.

There is also another parameter to specify the position of the Earth in its non-stop cycle. This parameter is called the "hour angle" or angle local time - ω. This is the angle between the plane of the meridian for the examined place on Earth at a specific time of day and the meridian of the place where the sun is at the very moment. To determine the hour angle, the true solar time should be known. It is obtained from standard time (hour), which is carried at the time meridian for a given time zone. Then it's adjusted to the angular difference between the local meridian and standard meridian time zone, and a repair of non-stationary angular velocity of rotation of the Earth is added:

$$T_{sol} = t_{st} - 4(l_{loc} - l_{st}) + E \qquad (2)$$

$$\omega = 15 \times (T_s - 12). \qquad (3)$$

In addition declination and hour angle, to determine the geometry of the sun is necessary to set the latitude of the location - φ. To determine the position of the sun relative to a stationary earth observer coordinates azimuth of the sun to the south direction A_z and elevation angle of the sun h are used (Fig. 2, Fig. 3). The elevation angle h is defined as the angle between the direction of the sun and the plane of the horizon.

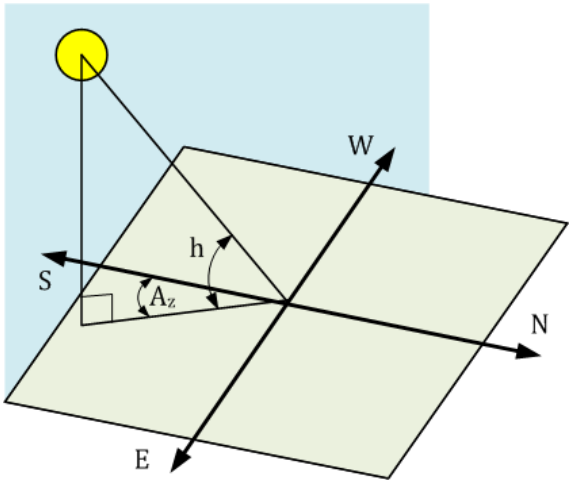

Fig. 2. Elevation angle and azimuth of the sun

Altitude angle and azimuth of the sun are changing constantly and are determined by the declination (day of the year), hour angle (hours a day) and latitude of the location in question, using the equations:

$$\sin h = \sin\varphi \,.\sin\delta + \cos\varphi.\cos\delta\,.\cos\omega \qquad (4)$$

$$\sin A_z = \frac{\cos\delta.\sin\omega}{\cos h} \qquad (5)$$

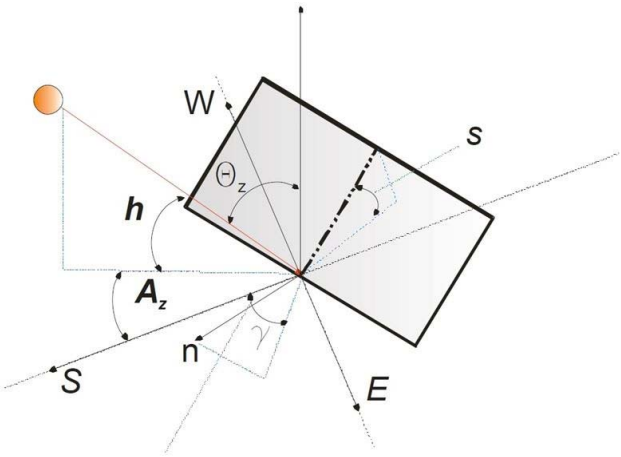

Fig. 3. Geometric characteristics of the Earth surface

B. Determining elevation angle by calculations using signals from photodiodes

To calculate the angle Θ_z, in east-west direction three identical photodiodes deployed at a different angle are used. In the middle (Fig. 4), Ph1 is located horizontally, while the other two are symmetrically placed on both sides of the angle α. The photocurrent generated by each of the photodiodes can be described:

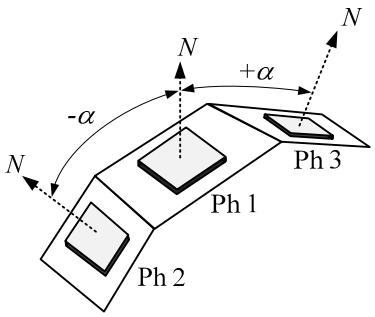

Fig.4. Geometric positioning of the photodiodes.

$$I_{Ph1}(\Theta) = E_{sun}.R_{Ph}.A_{Ph}.cos(\Theta) \quad (6)$$

$$I_{Ph2}(\Theta) = E_{sun}.R_{Ph}.A_{Ph}.cos(\Theta - \alpha) \quad (7)$$

$$I_{Ph3}(\Theta) = E_{sun}.R_{Ph}.A_{Ph}.cos(\Theta + \alpha), \quad (8)$$

where E_{sun} is the instantaneous irradiance produced by the sun, R_{Ph} – sensitivity of the photodiodes, A_{Ph} is the photosensitive area.

The received signals from each of the photodiodes is a function of the instantaneous light from the sun and its angular position Θ_z. The mathematical function for calculating of Θ_z angle can be obtained after measuring the photocurrent values: $I_{Ph1}(\Theta)$, $I_{Ph2}(\Theta)$, $I_{Ph3}(\Theta)$ and performing mathematical operations.

Two auxiliary mathematical functions f_1 and f_2, necessary for calculating Θ, have been verified for hardware realization. They are constructed so as to ignore the influence of the irradiance and the parameters of photodiodes.

$$f_1(\Theta, \alpha) = cos(\alpha) - \frac{I_{Ph2}(\Theta)}{I_{Ph1}(\Theta)} \quad (9)$$

$$f_2(\Theta, \alpha) = \frac{(I_{Ph2}(\Theta) - I_{Ph3}(\Theta))}{I_{Ph1}(\Theta)} \quad (10)$$

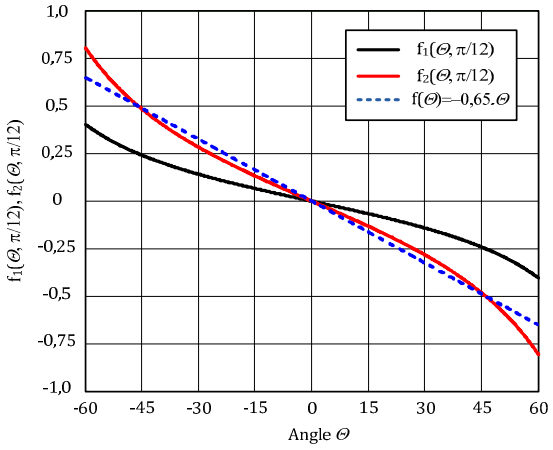

Fig.5. Relations of the auxiliary mathematical functions from the angle Θ.

Fig. 5 shows the graph of functions (9) and (10) for angle α = 15°, as well as the linear approximation of function (10). Function (10) which uses information from the two lateral photodiodes has twice as large slope. This results in greater sensitivity in determining the angle Θ and is a reason for hardware implementation in the device.

Once defined functions (9), (10) can be analyzed, the sensitivity and accuracy of measurement and the angle Θ is calculated as follows:

$$\Theta = arctan[K.f(\Theta, \alpha)], \quad (11)$$

where K is the coefficient depending from the function.

C. *Optoelectronic photodiode block*

The selected sensor is silicon photodiode type BPW34. Its spectral sensitivity is in the range of 0.4 to 1.1 micrometers, with a maximum sensitivity of 0,6 A / W. Sun light has a wide range of intensity, from dozens of lx to 150 000 lx, or expressed in energy units from approximately zero to 1200 W/m^2. The used photodiodes are in short circuit mode and that way providing a strictly linear dependence of the photocurrent generated by the solar radiation (11):

$$I_{Ph} = \int_0^\infty A_{Ph} E_{sun}(\lambda)\, R_{Ph}(\lambda) d\lambda \quad (11)$$

The spectral characteristics are shown on Fig. 6 in relative units, where: curve 1 - the solar radiation; curve 2 – the spectral response of the photodiode; dotted curve 3 - the sensitivity of the human eye and 4 – the product of curve 1 and curve 2. These characteristics are necessary for determining the coefficient of radiant flux from the sun as the source, by the set spectral characteristics of the photo detector.

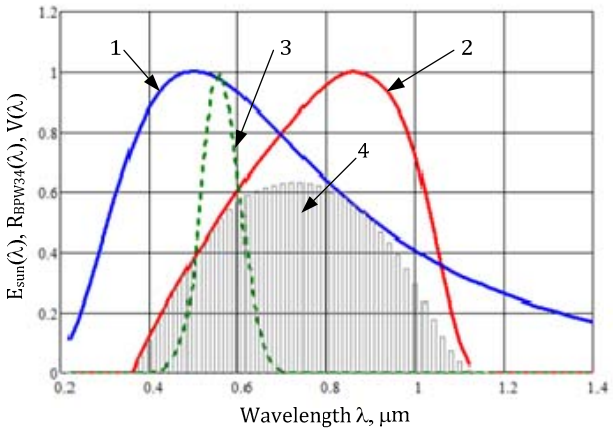

Fig.6. Spectral characteristics.

Using the spectral characteristics and numerical values for the sensitivity and the area of the photodiode the photodiode current is calculated relative to the solar radiation and shown on Fig. 7.

III. HARDWARE REALIZATION

The sensors circuitry is functionally composed of two parts. First part consists of the physical sensor – photodiods, suitably located to determine the position of the sun, temperature sensors, and etc. And the second part is normalizing circuits such as tranceimpedance amplifiers, current sensing ICs and instrumentation amplifiers. The

useful normalized signal from each type of sensor is connected to relevant ADC's input of the microprocessor.

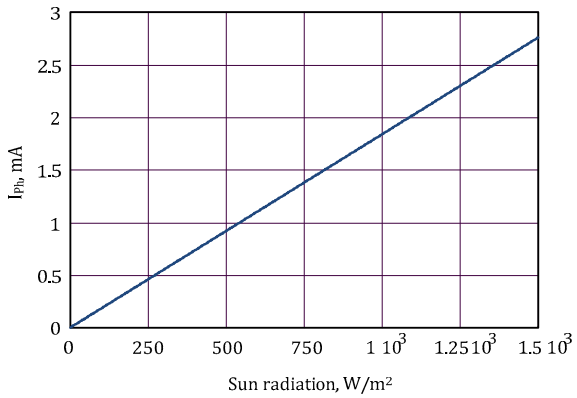

Fig.7. Relations of the photodiode's current relative from the solar radiation.

As the movement of the sun in the sky is a slow process, as well as the movement of clouds, which drastically reduce optical flow reaching the ground, the bandwidth of the used amplifiers does not need to be wide. Also the requirements for the response time and resolution of the ADC are completely covered by the MSP430F5529's 12-bit, built-in ADC. When the microprocessor is capable of digitizing the incoming voltage signals, then they can be processed through the built-in sun position calculation algorithm. After determination of sun coordinates, the microprocessor is creating control signal for the motor driving mechanism.

The resulting data and signals enable management on two coordinates: east-west and the altitude according to the specific terms of reference of the solar system.

IV. Conclusion

This paper proposes a solution of sun position determination for managing solar panel systems. The theoretical calculation of sun position using mathematical methods combined with sensitive optoelectronic front-end leads to an uncompromisingly accurate sun position determination.

The next step is comparing the theoretical results in the sun position determining with measured via the proposed route through auxiliary mathematical functions.

The presented solution is easily adaptive for implementation in various solar panel systems. The ongoing research on the topic of solar panel orientation dependencies to increasing effectiveness in solar plants can lead to a universal management solution for solar renewable plants.

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Virtual Colorimeter for Water Analysis

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Abstract – **The water quality analysis is important for human health and environmental protection. There are many physical and chemical methods for such analysis, with different accuracies, complexity and time consumption. In the presented paper, a colorimetric method, based on virtual instrumentation is suggested and considered in details. At the end of the paper, the concentration of free chlorine in water is determined for example.**

Keywords – **Colorimetric methods, Event-driven programming, LabVIEW, Virtual instrumentation, Water quality.**

I. Introduction

Water quality is determined by the presence of impurities in the water, which are harmful to human health. Organic contaminants include microorganisms such as pathogenic bacteria, viruses and algae that may cause disease or death for people [1, 4, 8]. Chemical contaminants include carcinogens, metals (such as copper, iron, arsenic, lead and manganese), nitrate (fertilizer byproducts) and purification products (such as chloramines). Unlike indirect methods of measuring biological contaminants, chemical contaminants can be measured directly because of their homogeneous distribution, different chemical properties, and well developed physical measurement. Chemical pollutants can be quantified using a variety of instruments that are categorized into those based on chromatography or radiation measurement.

Perhaps the simplest and most common method for measuring chemical pollution is based on radiation or light measurement. There are several forms of measurement of water quality based on light. Indicator solutions can be added to the water sample to obtain a characteristic change of color due to the presence of specific chemical substances. Then, the concentration of the target substance can be quantified based on the degree of discoloration.

In the present paper a virtual colorimetric technique for water analysis is suggested and implemented. This technique can be characterized with flexibility, easy calibration and fast data collection. Because in practice, the chlorination is one of the most commonly used methods for the decontamination of wastewater, as an example the concentration of free chlorine in water is considered in details.

II. Colorimetric method for water quality estimation

A. Theory of operation

Photometric methods are based on determination of the coefficients of transmittance and absorbance, using selective absorption of light by the molecules of the analyte. When light passes through a substance, the energy of the light wave decreases, as part of the wave energy is convert into energy of the secondary radiation, which has a different spectral composition and different direction of propagation (photoluminescence) [1, 3, 9].

If, in a given sample, light is irradiated, the intensity of this light passing through a homogeneous absorbing medium decreases exponentially. The absorbed part of the radiation is proportional to the concentration of the absorbing particles and depends on the thickness of the layer, b. The decrease in intensity, dI_λ (at a certain wavelength, λ), after passing through extremely narrow layer, db, is given by the expression:

$$dI_\lambda = -\alpha_\lambda I_\lambda db \qquad (1)$$

The coefficient α_λ, characterizes the absorbency of the medium for a certain wavelength, λ. It depends only on the number of the absorbing particles of the substance and not depend on the intensity of light.

By integrating equation (1) from 0 to b, for the intensity I of the irradiated light, after mathematical manipulations, gives the following expression is achieved (also known as the Beer–Lambert's Law):

$$I = I_0 e^{-\alpha_\lambda b}, \qquad (2)$$

where I_0 is the intensity at $b = 0$.

The amount of light that passes through a solution is known as transmittance, T, and can be expressed as the ratio of the intensity of the transmitted light, I, and the initial intensity of the light beam, I_0. The transmittance is changed from 0 to 1 and usually is given as a percentage by the formula:

$$T = \frac{I}{I_0}.100,[\%] \ . \qquad (3)$$

Many experiments are designed to use a colorimeter for measure a related, dimensionless parameter - absorbance (*A)*. The relationship between transmittance and absorbance is inverse and logarithmic and can be expressed as:

$$A = \lg\frac{1}{T} = \lg\frac{I_0}{I} = abc \ , \qquad (4)$$

where a is absorptivity and has a dimension [$L.g^{-1}.cm^{-1}$]; b is the thickness of the absorbing layer in [cm] and c is the concentration of the test substance in [$g.L^{-1}$].

Limitations of Bouguer-Lambert-Beer law are:

- the light source must have a narrow band of wavelength and must be monochrome;
- the relationship between the absorption concentration is linear, but only up to a certain concentration of the solutions;

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- at high concentrations molecules may be polymerized resulting in a cloudy suspension, which will affect the absorption;
- the presence of fluorescent molecules in solution will impact significantly on absorption [1, 3, 9].

B. Water pollutants detectable by colorimeter

Most pollutants dissolved in water are colorless and a colorimetric procedure involves adding some type of chemical (or "reagent") to the sample. Usually these substances are with specific chemical composition and can be used only for certain water ingredient. In Table 1 are generalized the main water pollutants, the reagent required, wavelength of light source (light emitting diode - LED) and concentration range that are needed for their determination by colorimetric method [1, 8, 10]. This summarized information can be used for the design and implementation of systems for analyzing the quality of water.

TABLE 1. WATER POLLUTANTS DETECTABLE BY COLORIMETER

Pollutant	Range, mg/L	Reagent	Colour	Wave-length
Chlorine Free, Cl_2	0,02 to 2,00	DPD	pink	520 nm
Chlorine Dioxide, ClO_2	0,04 to 5,00	Glycine	pink	520 nm
Formaldehyde, CH_2O	0,003 to 0,5	MBTH	blue	640 nm
Nitrate, NO_3	0,2 to 30,0	Chromo-tropic acid	yellow	460 nm
Phosphorus, PO_4^{3-}	1,0 to 100,0	Molybdate in an acid	yellow	460 nm
Iodine, I_2	0,07 to 7,00	DPD	pink	520 nm
Alkalinity, $CaCO_3$	25 to 400	TNT870	shade of blue	640 nm
Bromine, Br_2	0,05 to 4,50	DPD	pink	520 nm
Hardness Ca and Mg as $CaCO_3$	0,008 to 1	Hardness ULR set	shade of blue	640 nm

C. Methodology for colorimeter calibration

Theoretically, the output signal of the colorimeter is voltage that varies in a linear way with transmittance. For more accurate measurement the colorimeter must be calibrated which can easily be done using virtual technologies.

The calibration methodology includes the following steps:

1. Using the information summarized in Table 1, choose the appropriate reagent according to the investigated water pollution.
2. Select the color of the light from a LED to achieve maximal absorbance.
3. A set of solutions, so called calibrants in which the analyte concentration is known, must be prepared.
4. Measure output voltage for each calibrants and collect the corresponding data
5. Establish a calibration function using the resources of virtual technologies for approximation and curve fitting. The transfer function of colorimeter is most appropriate to be approximate with exponential, a second-order polynomial or conventional linear model.

III. DESIGN OF THE VIRTUAL SYSTEM

A. Software Design

The software design of the virtual system is implemented by using a so called event-driven state machine architecture. By definition, event-driven state machine is a variant of finite-state machine, but the transition from one state to another are initiated by events or messages. A typical layout of event-driven state machine architecture is shown in Fig. 1. This design pattern can be divided in three main components – ***Queue reference***, ***User events*** and ***Main state machine***.

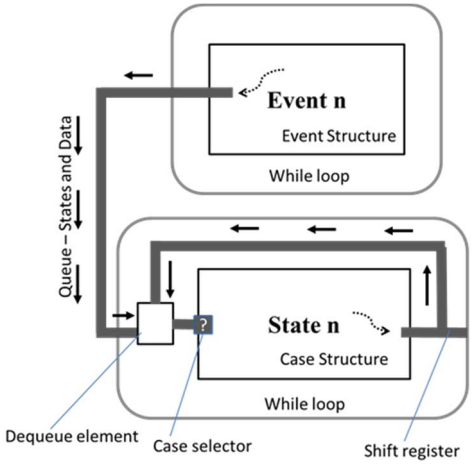

Fig. 1. A layout of event-driven state machine architecture

The ***Queue reference*** represents a command and data-messaging pipeline where the queue accepts data packets added by producer and releases these data packets to consumer. The data packet is composed of a cluster containing an enumerated constant and a variant data item. The enumerated constant assembles names of the state machine cases in the consumer process. Therefore, these enumerated names are similar to command names that denote which state name contains the corresponding code for processing the command. In order to achieve more flexibility, the type of data that migrate through the queue is ***Variant***.

The next main component of the presented event-driven state machine architecture is ***User event***. This component consists of ***While loop*** and ***Event structure***. In an event-driven programming, the software code waits for event to occur, responds to this event and returns to waiting state for the next event. Each event generates data packet in the queue, which manipulates the reaction of the main state machine.

The last component from the presented architecture is ***Main state machine***. It consists of a set of states and a case selector that determines which code to be processed. Usually in LabVIEW, a state machine is formed by a while loop, a shift register, a case structure, and an enumerated type case selector.

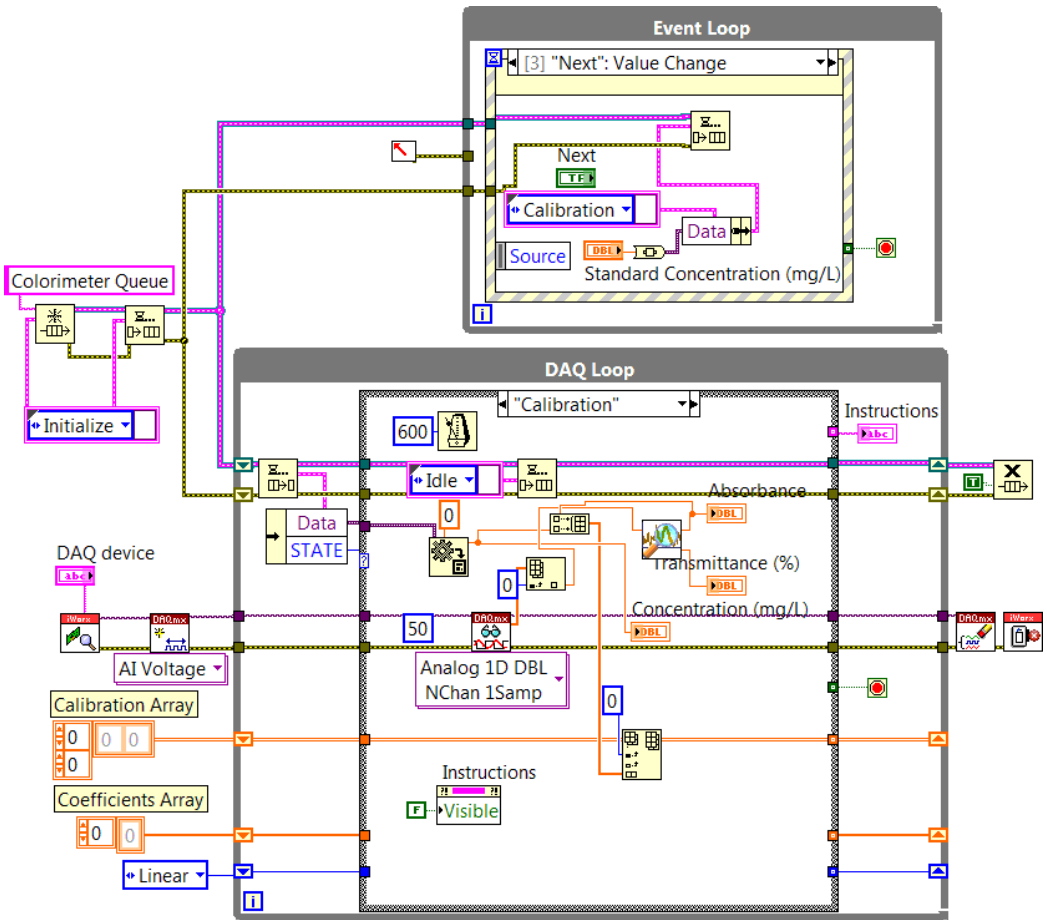

Fig. 2. The LabVIEW implementation of the event-driven state machine

The LabVIEW implementation of the described event-driven state machine is shown in the Fig. 2. In the top part of the figure is placed event structure, which generates data packet to queue for each event like a push of a button. The created events for Virtual colorimeter are ***New Calibration*** – to prepare colorimeter for calibration procedure, ***Next*** – to enter new concentration value and measure the absorbance, ***Finish*** – to execute ***RegressionSolver.vi*** and determining calibration equation, ***Measure*** – to measure concentration in sample and ***Exit*** – to stop the execution and to release the resources. Additional events are provided for loading data from file and for saving data to file. The main state machine is labeled as ***DAQ loop***. Here are positioned various functions for control of data acquisition, manipulating data and visualization of results. ***Shift registers*** and ***Queue Operations*** functions establish the communication between various states of the ***State machine***. Similar to the event structure there are a number of states for control of measuring process and manipulating the data. The default state is ***Initialize*** followed by ***Idle*** state. In the ***Calibration*** state is obtained data for preparation of the standard curve. ***Curve fitting*** for estimation of the calibration equation is making up in ***Regression*** state by calling the ***Regression Solver.vi*** function. The actual measurement of a sample of water is performed in ***Measurement*** state. In states ***Load from File*** and ***Save to file*** are called functions for read from and write to files. There are mandatory states for the error handling and stopping the execution.

B. Colorimeter CTSN-100

In the presented project a commercial colorimeter CTSN-100 by iWorx Systems Inc. is selected for absorption measurement. The base parameters of the colorimeter are summarized in Table 2.

TABLE 2. THE BASE PARAMETERS OF COLORIMETER CTSN-100

Parameter	Value
Blue, Green and Red Peak Wavelength	460 nm, 520 nm, 640nm
Input Range in Absorption (*A*)	0 - 1,4
Input Range in Transmittance (*T*)	100% - 4%
Output Range	2,5V – 0,1V
Transfer function	V_{out}=25mV.T,% A = $\log_{10}$ (2,5V/V_{out})
Supply voltage	±15V

C. NI myDAQ

Actually, any DAQ device with DAQmx drivers can be used to acquire data from the colorimeter. The reason to select the myDAQ as measuring device in this project is the presence of the breakout board IX-MYDAQ. This board enables the connection of the iWorx transducers to the National Instruments myDAQ device without additional cables and power supplies. The data acquisition device myDAQ includes two analog inputs with 16 bits resolution at sample rate up to 200 kS/s. It provides power supplies with +5, +15, and -15 volt.

IV. Determining the Free Chlorine Content of Water with Virtual Colorimeter

There are many water pollutants that can be analyzed by the presented colorimetric approach. Some of these pollutants are summarized in Table 1. In order to prove reliability of the presented approach, the determination of the concentration of free chlorine with virtual colorimeter is studied in this chapter. Chlorination of drinking water and swimming pools has been practiced for almost hundred years.

In addition to DPD, the other widely used reagent for determination of free chlorine is the orthotolidine (or o-tolidine). Orthotolidine is an organic compound with the chemical formula $(C_6H_4(CH_3)NH_2)_2$. It reacts with small amounts of free chlorine to produce solutions with a yellow to orange colour. In the present project for the colorimetric analysis of water is used this reagent. To analyze yellow liquids with colorimeter, the most appropriate is blue LED.

In order to establish a calibration function, a set of standard solutions (calibrants) is required. The four standard solutions with concentration of chlorine 0,1 mg/L, 0,6 mg/L 1 mg/L and 3 mg/L are prepared and filled in four cuvettes. In each cuvette are dropped exactly three drops of orthotolidine. To measure absorption equal to zero, or with other words, to eliminate the offset of colorimeter, a blank cuvette filled with distilled water is prepared. Cuvettes are placed in the colorimeter in sequence and for each one is entered concentration of the chlorine (for blank cuvette it is zero) and is measured absorption for the blue light. Finally the button ***Finish*** is pressed and the calibration curve is displayed as is shown in the Fig. 3.

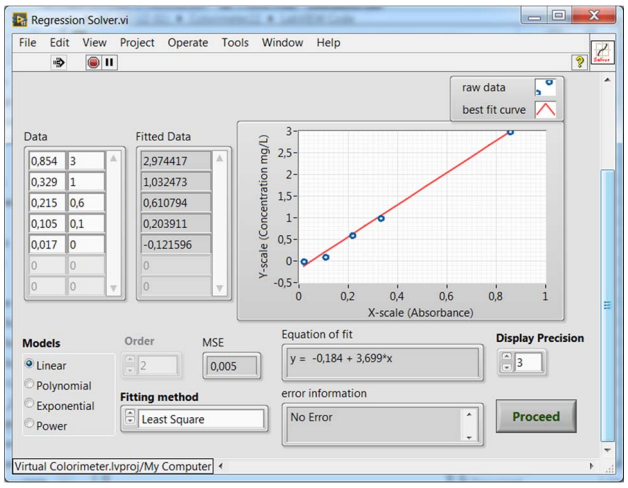

Fig. 3. The obtained calibration curve for determination of free chlorine

As can be seen on the figure the most appropriate model for regression of the calibration curve is linear. The achieved calibration equation is:

$$c = -0{,}184 + 3{,}699.A \qquad (5)$$

Once the calibration equation has been obtained it is possible to measure the concentration of free chlorine in a sample of water. The process of determination of free chlorine content in a sample of water from swimming pool is shown in figure 4. The concentration of chlorine is 0,9 mg/L for absorption of blue light equal to 0,3.

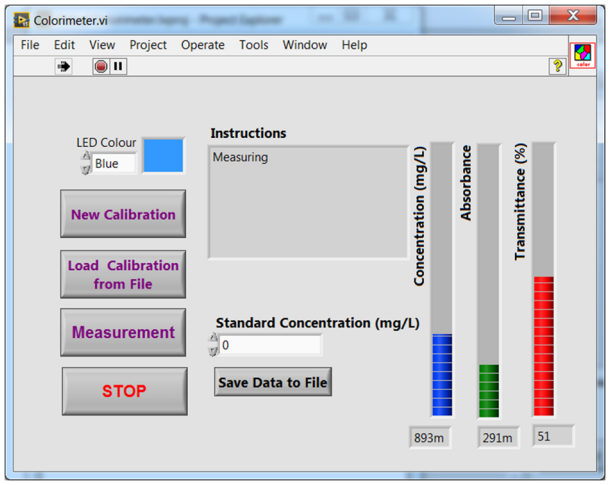

Fig. 4. The front panel of virtual colorimeter with measurement results

V. Conclusion

In present paper is suggested a virtual system for water analysis using colorimetric method. This approach allows easy calibration and fast data analysis for various water pollutants. The more important pollutants of water that can be analyzed with developed virtual colorimeter are summarized and presented. As example, the concentration of free chlorine in water is determined, following introduced methodology. It is difficult to estimate exactly the accuracy of virtual system because there are many different sources of errors. Particular attention is paid to the software part of the virtual system using event-driven programming.

This research is supported by Project № DUNK 01/3/2009

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Cloud-managed ZigBee Sensor Networks

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Abstract – **The main advantages of the open global standard ZigBee are mesh networking, low cost, low-power, low-complexity, reliability and operation on unlicensed frequency band, available worldwide. These benefits enforce ZigBee as one of the widely used standards for low-data-rate and short-range communications, used in wireless sensor networks. In recent years, with increasing interest are the management of sensor nodes beyond the borders of the personal area network and data collecting. In this paper is presented an approach to involve ZigBee based sensor networks in cloud technology in order to manage the network, collect and present the measured data.**

Keywords – **Cloud platforms, ConnectPort, IEEE 802.15.4, Wireless Sensor Networks, ZigBee**

I. Introduction

A wireless sensor network may consist of a large number of sensor nodes with arbitrary density. Therefore, major interests when considering sensor networks are communication, network management, and data aggregation, manipulation and analysis. This is of particular interest when is implemented in cloud platforms, because this requires the access to the network from any device with web browser, anywhere in the world. Another advantage of using cloud platforms with sensor networks is that the data from sensor nodes is online.

The ZigBee Alliance has developed a low-cost, low-power-consumption, two-way, wireless communications standard. The ZigBee standard is based on IEEE 802.15.4, which operates at license free frequency band, and provides reliable, low-power and secure communication [3, 9, 11]. Solutions adopting this standard are implemented in industrial controls, consumer electronics, home and building automation, PC peripherals, medical sensor applications and even toys. Other popular standards that use IEEE 802.15.4 PHY and MAC layers are 6LoWPAN and WirelessHART [4].

According to the official definition "cloud computing is a model for enabling ubiquitous, convenient, on-demand network access to a shared pool of configurable computing resources (e.g., networks, servers, storage, applications and services) that can be rapidly provisioned and released with minimal management effort or service provider interaction" [6]. The definition lists a five essential characteristics of cloud computing: on-demand self-service (a consumer can acquire resources based on service demand), broad network access (cloud services can be accessed remotely from heterogeneous client platforms), resource pooling (resources are pooled and shared by consumers), rapid elasticity or expansion (resources can be rapidly provisioned and released with minimal human involvement), and measured service (resources are controlled). However not every cloud platform exhibits all five characteristics.

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II. Sensor Network Architecture

While numerous sensors are connected directly, through the use of existing local area networks, with controllers and data processing stations, the number of sensors that send information wirelessly increases [2]. This is important because many network applications with hundreds or thousands of sensor nodes are often located in remote and inaccessible areas. For this reason the sensor nodes, except sensor element, need to have opportunities for processing and storing the data. In presented project the developed sensor nodes use open-source microcontroller platform Arduino. This popular platform was chosen because it has many advantages over other systems as: relatively inexpensive, cross-platform, simple and clear programming environment, open source and extensible software and hardware. Actually, in present wireless network, the sensor nodes are built by Arduino Uno or Arduino Mega 2560 boards, Wireless Proto Shield, XBee Series 2 radios and a number of sensors. XBee radio frequency modules meet IEEE 802.15.4 standards and operate within the Industrial, Scientific and Medical (ISM) 2.4 GHz frequency band.

The gateway is an interface between Internet Protocol (IP) network and a wireless sensor network, containing XBee radio frequency modules and is intended to provide connectivity between heterogeneous networks. The overall architecture is presented on Fig. 1.

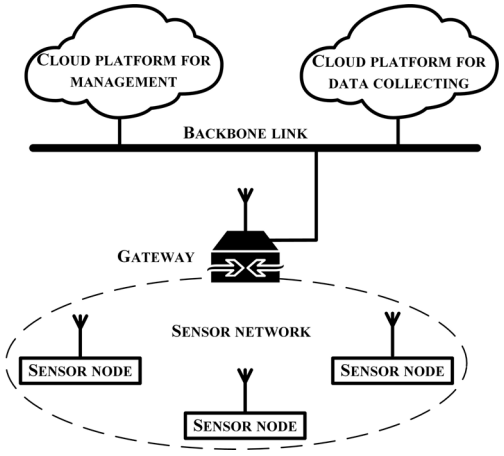

Fig. 1. Architecture of cloud-managed ZigBee sensor network

As a gateway can be used dedicated hardware device like Digi's ConnectPort or software, running on personal computer with XBee radio module and Internet connection. The connection between the personal computer and the radio module is through universal serial bus (USB) to serial base unit called SparkFun XBee Explorer USB. The highlight of this interface board is an FT231X USB-to-Serial converter, which translates data between computer and the XBee module. SparkFun XBee Explorer USB board also is used for configuration of each XBee module used in the network. For reading and modifying of module's parameters, the XBee first must be configured into Command Mode. In this mode incoming characters are interpreted as commands. The supported Command Mode options are AT Command Mode and Application Programming Interface (API) Operation. By default, XBee modules act as a serial line replacement (Transparent Operation). As an alternative to the default Transparent Operation, API operations are available. This API operation requires that communication with the module to be done through a structured interface – data is communicated in frames in a defined order. The API specifies how commands, command responses and module status messages are sent and received from the module using a Universal Asynchronous Receiver/Transmitter (UART) data frame. Fig. 2 shows communication methods and modes with the radio frequency modules.

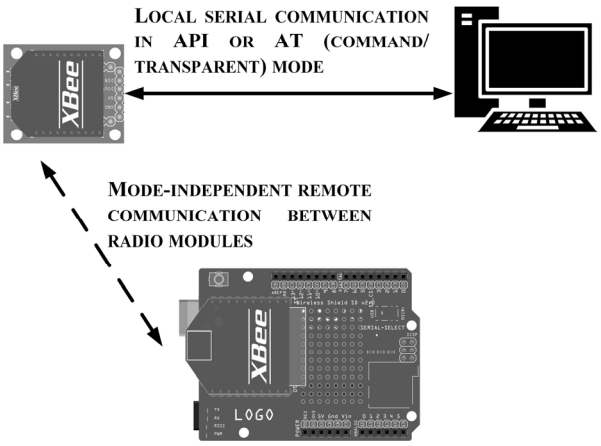

Fig. 2. Local and remote communication

For programming the XBee modules a XCTU software is used. The role of a particular device in the network depends on radio firmware, which stores the program code in a module's persistent memory, that provides the control program for the device. On Fig. 3 is shown the graphical view of personal area network (PAN). Each module is labeled with its role (C – coordinator, R – router). The coordinator is IEEE 802.15.4 full-function device that provides network synchronization, responsible for associating and disassociating devices into PAN. The ZigBee router is an IEEE 802.15.4 full-function device, which is not the ZigBee coordinator but may acts as an IEEE 802.15.4 coordinator within its personal operating space, which is capable of routing messages between devices and supporting associations. The quality of the connection between the two nodes is displayed as a number close to the line that connects them. This number named Link Quality Indication is between 0 and 255, where 0 is the weakest connection and 255 is the strongest connection.

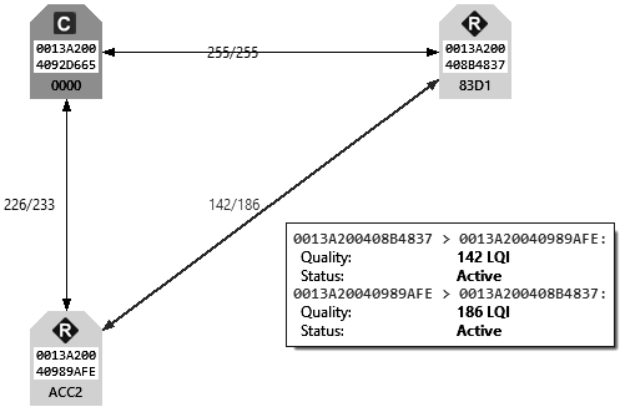

Fig. 3. Graph view of the personal area network

III. REMOTE MANAGEMENT

As a network grows, the complexity of effectively managing the network assets grows exponentially. With cloud platforms like Device Cloud by Digi® can be overcome important problems of a dynamic device network, such as: centralized control over large numbers of devices, reducing service complexity, maintaining high levels of security, provisioning and decommissioning of equipment, adding functionality to device networks, etc. The use of this platform enable reliable communication for many real-world applications, such as, working control systems and sensing networks. In addition it provides flexible management [10]. Fig. 4 shows current state and historical statistics about XBee Internet Gateways.

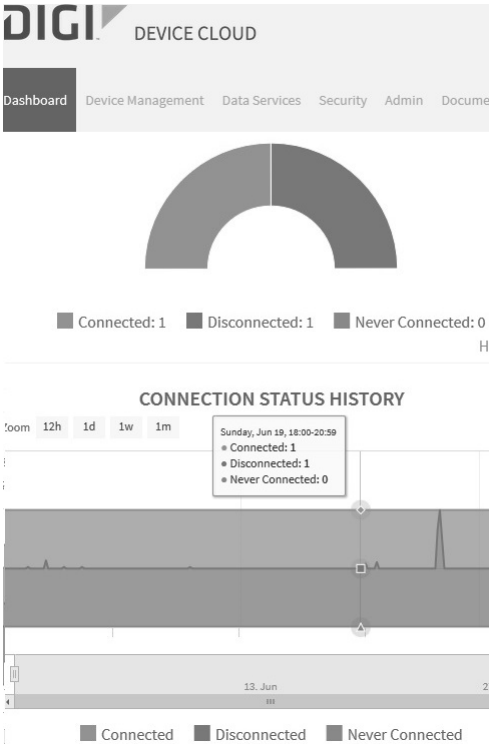

Fig. 4. Current state of devices and historical statistics on performance metrics for each gateway

In the display is shown a summary of the number of devices connected, disconnected, or never connected to the cloud. Never connected denotes a registered device that has not yet connected to Device Cloud.

Fig. 5 shows the Device Cloud Device Management view, which allows monitoring and managing a variety of devices. Depending on Device Cloud Edition and service bundles, the Device Management view provides different options.

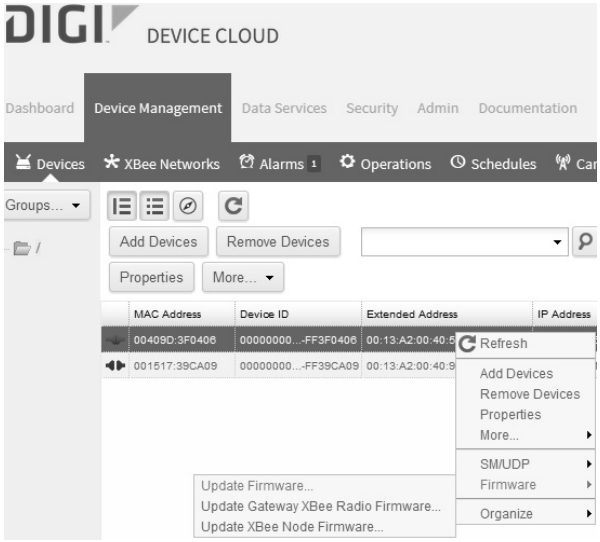

Fig. 5. Management of selected device

As can be seen from the figure, a many features for managment are available: adding and removing of devices, firmware update of the gateways or XBee modules, sending of messages and assigning to group. In order to perform firmware update for multiple devices at the same time, all devices must be of the same type. After update, the processed devices will automatically reboot when the updates are complete.

On Fig. 6 are shown main network properties for the selected node. Displayed options strongly depend from the type of connected device.

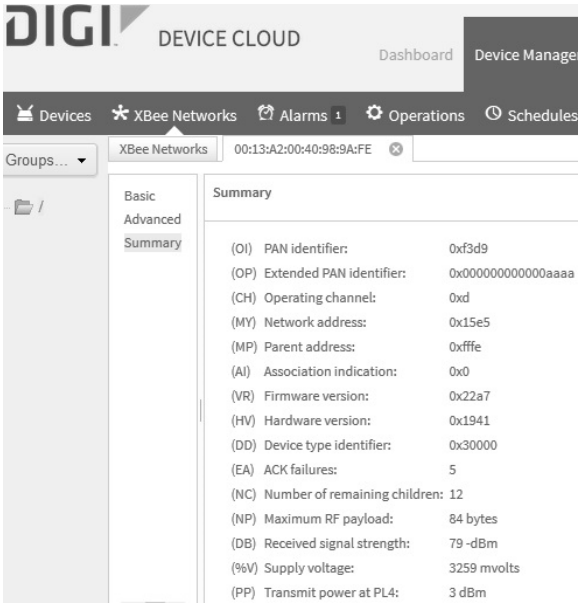

Fig. 6. Properties for a particular network device

As can be seen in the figure Network properties are: PAN identifier, operating channel, network address, firmware version, hardware version, device type, maximum radio frequency payload, received signal strength and supply voltage transmit power.

IV. DATA COLLECTING AND ANALYSIS

Cloud infrastructures are aggregates of computing, storage, and networking resources deployed along centralized or distributed data centers devoted to support various services and applications [5]. The Internet of Things (IoT) provides access to a broad range of embedded devices and web services. The measured data from each sensor is acquired and processed by the wireless sensor node. Then the data is sent to the cloud platform for data collecting – ThingSpeak™ [12, 13]. ThingSpeak is an IoT platform, which enables sensors, instruments and websites to send data to the cloud and to store it in a channel. The primary element of ThingSpeak activity is the channel, which contains data fields, location fields, and a status field. Once data is entered in the ThingSpeak channel, this data can be analyzed, visualized, manipulated or interact with social media, various web services, and other devices. Besides data storing, the platform provides applications for visualizing and analysis the data with MATLAB® functions. Fig. 7 shows gathered, stored and visualized data about the measured temperature and a histogram of a temperature variation during 24 hours.

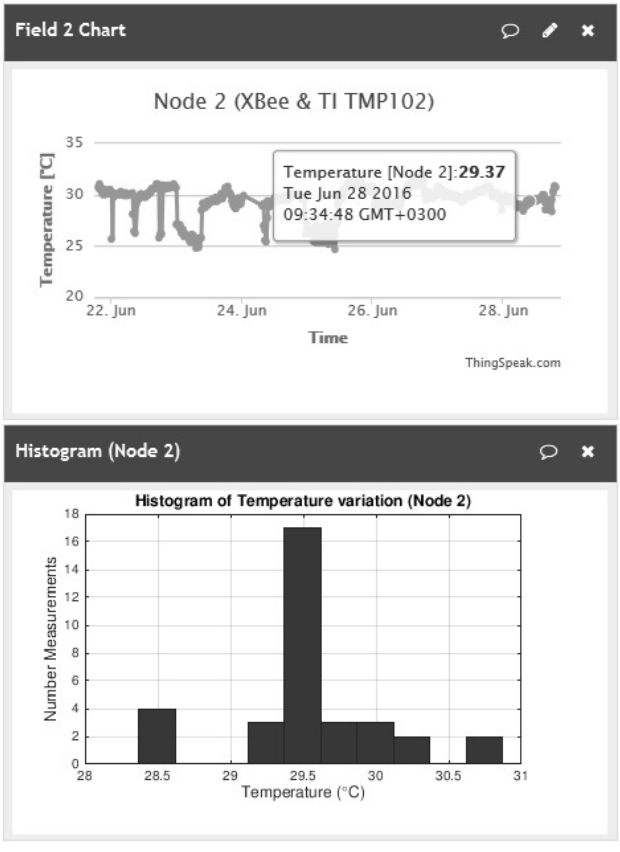

Fig. 7. Measured temperature and histogram of variation of temperature.

In presented project, as sensing element for temperature measurement is used sensor TMP102 by Texas Instruments. This precise device offers an accuracy of ±0.5 ˚C without requiring calibration or external component signal conditioning. Because temperature sensors are highly linear, the device does not require complex calculations or lookup tables to derive the temperature. The on-chip analog-to-digital converter offers resolutions down to 0.0625 ˚C. The sensor is specified to operate over supply voltages from 1.4 to 3.6 V with the maximum quiescent current of 10 µA over the full operation range. The device is specified for operation over a relatively high temperature range and is suitable for extended temperature measurement in variety applications [7].

In order to illustrate various applications capable to work in clouds, an example of measuring an ethanol concentration in air is presented in the end of this paper. A MQ-3 gas sensor by Zhengzhou Winsen Electronics is used to measure the existence of gas. As a sensitive material of this gas sensor is used SnO_2, which has lower conductivity in clean air. When the target ethanol gas exists, the sensor's conductivity gets higher along with the increasing gas concentration. The Arduino microcontroller board converts the change of conductivity to correspond output signal proportional to gas concentration. The sensor has high sensitivity to ethanol in air, but can resist to the interference of gasoline, smoke and vapour. The main features of the sensor are good sensitivity to ethanol in wide range, long lifespan, low cost and simple drive circuit [8].

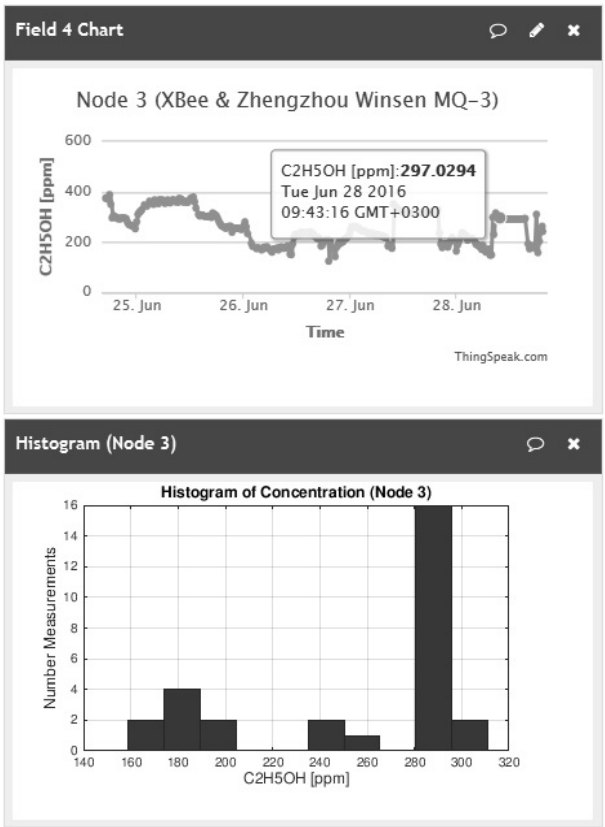

Fig. 8. Measured concentration of ethanol in air and histogram of concentration variation

Should be noted, that for wireless applications of such chemical sensors, an additional power supply or energy harvesting system is required. Fig. 8 shows gathered, stored and visualized data about the measured ethanol concentration in air and a histogram of its variation over 24 hours.

The sensor output voltage is scaled to a measured physical value with equation, obtained from a specific sensor calibration. Although many chemical sensors are linear over a limited range, these sensors exhibit a slight but progressively more nonlinear characteristic in large measurement range. Consequently, over an extended span, curve fitting is necessary to achieve a high level of precision [1].

V. Conclusion

The use of cloud platforms facilitate remotely monitoring and management of networks and contained devices via any device connected to the Internet. This technology provides access to the data anytime, anywhere and allows device integration. The proposed and implemented approach, expands the capabilities of the sensor network beyond the local mesh. Since devices are associated with the cloud platforms through Internet that allows on line management and monitoring of the status of network devices. Moreover, it is possible to be scheduled automatic tasks, such as receiving notifications when a particular device enters a particular state. This reduces the need for physical intervention and maintenance, the time for its implementation and increases the performance.

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Calibration Techniques for Microwave Moisture Meters

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***Abstract*—Microwave moisture meters are used for fast measurement of the water content in organic and inorganic bulk materials like grain, sand, and animal feed. The operating principle is based on the very high relative dielectric permittivity and loss factor of water, so the effective electromagnetic parameters of the tested sample depend highly on the water content. The density of the test sample also influences the measurement results, therefore it should be taken into account in device calibration. This work presents several solutions for correction of the influence of the density on the moisture measurement data.**

***Keywords*—Microwave sensors, moisture meters, calibration techniques.**

I. Introduction

Moisture control is required in manufacturing lines across, various industries like animal feed, construction materials and pharmaceuticals. The most challenging requirement for the sensors is their very short response time, because they are most often used for the automation of the manufacturing process and therefore need to provide real time information on the water content of a moving material.

Water has a very high relative dielectric permittivity due to the polarity of its molecules. For the microwave range the value is $\varepsilon_{\mathrm{r}} = 78.3$ [1]. The other components of the typical granular materials which require moisture control, like fats and carbohydrates for the feeds and non-organic substances in the construction materials, have a significantly lower permittivity. For instance the carbohydrates have a dielectrinc constant of about $\varepsilon_{\mathrm{r}} = 5$ [2], and the figure for dry sand is $\varepsilon_{\mathrm{r}} = 3 - 6$ depending on the composition [3]. Additionally water exhibits significantly higher dielectric losses in the microwave range. Therefore the water content of any material can be measured simply by determining its complex dielectric constant and converting the data correspondingly.

There are multiple methods for permittivity measurement depending on the type of material. Normally all methods require knowledge of the dimensions of the sample. The granular materials can be easily measured, because they can be poured into a vessel and they conform to its shape. Several methods for moisture measurement have been developed, of which we will consider two: Insertion loss method [4] and Resonator method [5].

The generalized schematic of the insertion loss method is presented in Fig. 1. The setup consists of two antennas. A generator is connected to one and a detector to the other. It is possible that the detector can be set up to measure the amplitude, but also the phase of the received signal. For the latter an external reference connection to the generator is needed. The granular material under test is placed between the two antennas. The amplitude of the detected wave varies with the losses of the material between the two antennas, therefore corresponding to the complex component of the dielectric permittivity, and the phase of the detected signal corresponds to the real part. A significant benefit of this method is that it requires no time delay, as the interaction between the material and the propagating wave is instant, and is therefore very suitable for moisture meters integrated in a production line.

The second method under consideration in this work is presented in Fig. 2. The sensitive device is an open resonator, that is a resonator that allows interaction between the electromagnetic field and the test sample. An example of suitable resonators are microstrip ring or line resonators, which have the material placed on top of them. The resonator used in this work is an open-ended coaxial stub, as shown in the figure. It consists of a a coaxial line with inner diameter of 50 mm and center conductor diameter of 8 mm, shortened at one side and open at the other. The open ended side contacts the test sample through a thin dielectric cover, which prevents the material from flowing into the resonator. The resonator is fed using two L-shaped stubs.

The resonators are characterised by their resonant frequency and quality factor. When the resonator is loaded both parameters change, the resonant frequency shifting due to the real part of the load's dielectric constant, and the quality factor due to the losses. The measurement setup contains

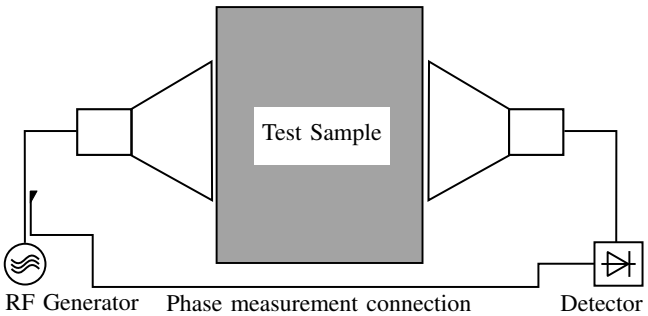

Fig. 1. Generalized schematic diagram of an insertion loss microwave moisture meter.

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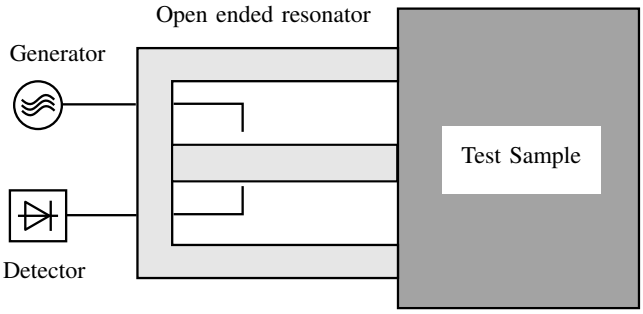

Fig. 2. Generalized schematic diagram of a resonator based microwave moisture meter. We use coaxial resonator, shown in cross-section, which is a coaxial line with inner diameter of 50 mm and center conductor diameter of 8 mm, shortened at one side and open at the other.

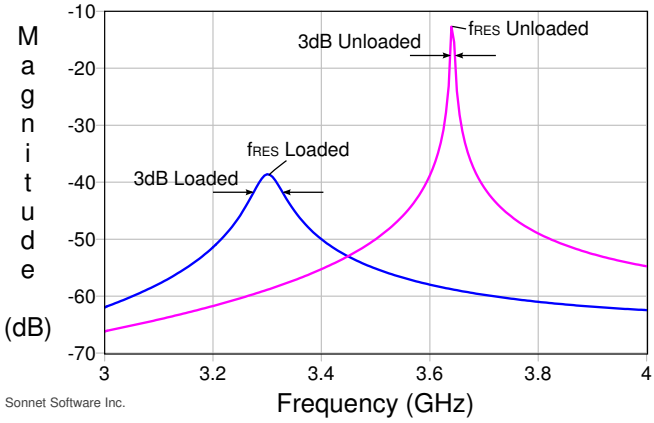

Fig. 3. Typical example of a frequency response of an unloaded and a loaded resonator. Shown are the resonance frequency and the -3 dB bandwidth in both cases.

a tunable generator and an amplitude detector, which are used to measure the resonator's frequency response. A data processing unit is needed to determine the position of the resonant frequency and the -3 dB bandwidth, which corresponds to the quality factor. Additional drawback is that the measurement takes time, as the measurement of the frequency response requires sampling several data points. The exact number depends on the algorithm for finding the maximum and the 3 dB bandwidth, but it is usually about 20 points.

Both methods presented above suffer a drawback. They measure the *volume* based water contents in the material, and the regulations in the various industries requires control of the *mass* based water contents. In other words, if two materials have the same water contents, but different density, both methods will show different results for the complex permittivity and therefore read out different moisture content. Therefore a calibration technique is required in order to determine both the moisture content and the density of a given material from the measured data.

This paper compares the moisture measurement accuracy that is obtained using different calibration techniques. Section II describes the calibration techniques. Section III shows the results and Section IV draws the conclusions.

II. Calibration techniques

The calibration techniques used in this paper are an extension of a technique developed by Kocsis *et al.* [6]. The method is developed for computing the mass moisture content and the density of a test sample using the resonator based technique described in the previous section and depicted in Fig. 2. We measure the frequency response of the resonator in the two cases: unloaded, that is when it is not in contact with the test sample; and loaded. Typical results are presented in Fig. 3, which sows the simulated data for a microstrip line resonator. When there is moisture in the resonator field, the raised dielectric permittivity of the medium causes the resonant frequency to decrease and the raised dielectric losses cause the quality factor of the resonator to decrease. As the quality factor is inversely proportional to the -3 dB bandwidth, the latter increases.

Both increased density and increased moisture content of the sample lead to change in the central frequency and the

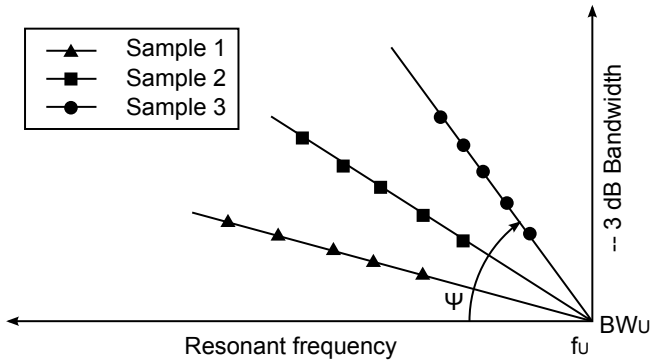

Fig. 4. -3 dB bandwidth plotted vs. resonance frequency for three samples with different moisture. The samples are with varying density. The origin of the graph is placed at the unloaded resonance frequency f_U and bandwidth BW_U.

quality factor of the resonator. In order to develop a method for computing the two parameters, the bandwidth is plotted versus the resonant frequency. The resonator is loaded with three samples of the same material, but different moisture. The density of the material is varying. The results are shown in Fig. 4. It has been experimentally verified that the locus of measurement points of a material with fixed moisture and varying density is a straight line, passing through the origin of the coordinate system, which is set at the unloaded resonance frequency f_U and bandwidth BW_U. In other words the angle ψ, which is given by

$$\psi = \arctan \frac{f_L - f_U}{BW_L - BW_U}, \tag{1}$$

where f_L and BW_L are the measured resonance frequency and bandwidth correspondingly for a loaded resonator, is constant for a material with constant moisture. To complete the calibration we need to compute a linear or polynomial interpolation

$$M = f(\psi), \tag{2}$$

which computes the sample moisture M, which has to be obtained for the test samples using other methods, e.g. gravimetric measurement. That leads to the following measurement algorithm:

1) We measure the unloaded resonator frequency and bandwidth;

2) We load the resonator with a test sample and measure the loaded resonance frequency and bandwidth;
3) We compute the angle ψ using eq. (1);
4) We compute the moisture using the interpolation (2).

This method is extremely convenient, because it does not require knowledge of the density of the test sample, as we average the angle obtained for the different points, shown in Fig. 4. Furthermore, we compute the calibration parameters, which are the coefficients of the interpolation function $f(\psi)$ directly from the measured data and the sample moisture without intermediate steps like the complex permittivity.

The calibration technique described above can be extended to any set of two parameters that depend on the dielectric permittivity and the losses of the test material. We can simply plot the two parameters measured for different test samples on a plot similar to the one presented in Fig. 4. If a visual inspection suggests that samples with constant moisture lay on a line, similar to the lines in the figure, we can define a similar angle ψ and compute a similar interpolation function $f(\psi)$ in order to decouple the density from the moisture content. Finally we can perform several measurements on test samples with known moisture content and compute the standard deviation of the results in order to compare the accuracy of the calibration techniques.

In this work we consider four measurement setups:

1) Resonator based method, as described above and shown in Fig. 2. The two parameters used are resonator frequency and bandwidth.
2) Insertion loss method, as shown in Fig. 1. The two parameters are the magnitude and the phase of the transmitted wave.
3) Insertion loss method, as shown in Fig. 1, with additional measurement of the reflected wave from the radiated antenna. The two parameters are the magnitude of the transmitted and reflected wave.
4) Insertion loss method, as shown in Fig. 1, with a single measured parameter the magnitude of the transmitted wave. This method is less precise, as it can not compensate for the sample density, but is the easiest to realise, so it is interesting to know its accuracy in order to confirm its applicability to cheaper and less critical solutions.

III. Results

The resonator based method from Fig. 2 was tested with sugar beet for animal feed manufacture as material sample. The unloaded resonator has a frequency of 1400 MHz and -3 dB bandwidth of 6.3 MHz. Three test samples were prepared with a moisture content of 62.3 %, 64.3 %, and 66.9 %. The density of each sample could be varied by applying mechanical pressure on it. Each sample was measured several times with varying density, and the resonance frequency and the -3 dB bandwidth were recorded. The results are presented in Fig. 5, where a plot of the resonance frequency vs. the bandwidth is shown. The lines show the approximations for the locus of constant moisture points. We compute the slope of these lines, which can be expressed as $\tan\psi$ and obtain a relation between the slope and the moisture of each sample, shown in Fig. 6. Here we have

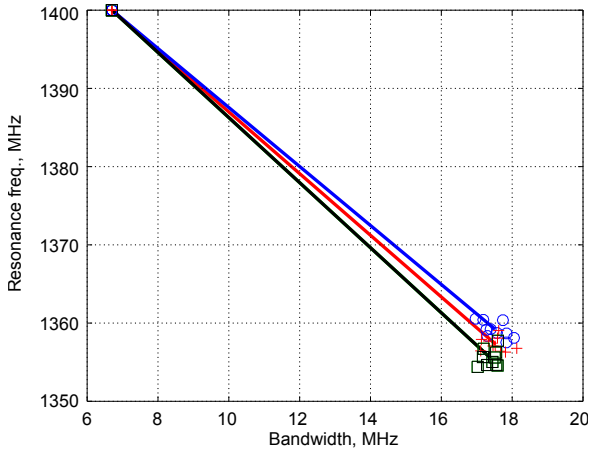

Fig. 5. Resonator based method results using sugar beet.

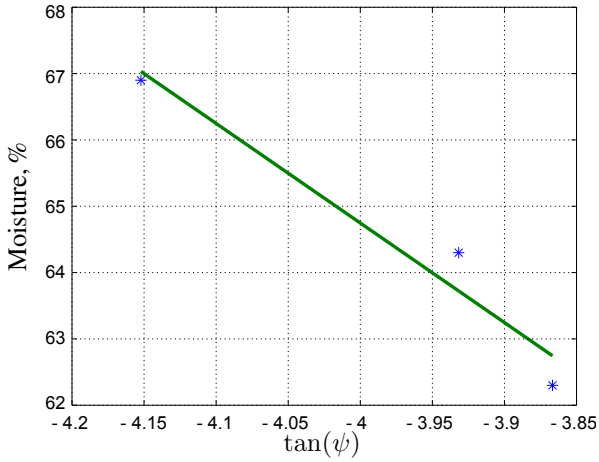

Fig. 6. Interpolation for computing the moisture as a function of the line slope.

modified the interpolation from (2) to the form

$$M = f(\tan\psi), \tag{3}$$

because the tan function is computation extensive and the measurement software is to be implemented in an embedded controller, which could risk the real time measurement requirement.

The insertion loss method from Fig. 1 was tested with wheat as a sample material. The moisture of the three samples was 10 %, 12 %, and 17 %. The density of the samples was varied by applying mechanical pressure. The results are presented in Fig. 7, where the two variables are the insertion loss and the phase delay. Similarly to the resonator method described above, we compute the average slope ψ of the measurement points of each sample and compute a regression (3) for computing the moisture content of the sample.

A modification of the last method is to measure the reflection coefficient of the transmitter antenna additional to the insertion loss. This technique is simpler to realise, because the phase measurement can not directly distinguish between the phases ϕ and $\phi + 360°$, and a complicated post processing may be required to do that. The results are presented in Fig. 8, and once again a regression in the form (3) is computed.

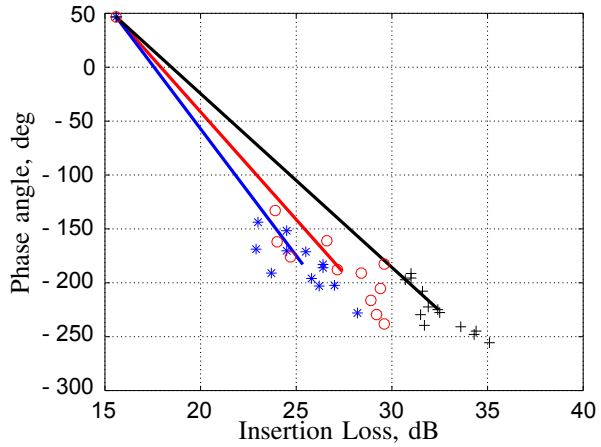

Fig. 7. Insertion loss vs. phase angle for an insertion loss based moisture measurement with additional phase measurement.

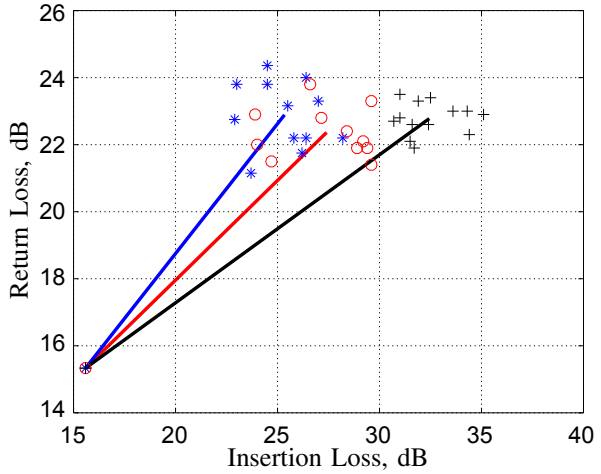

Fig. 8. Insertion loss vs. return loss for an insertion loss based moisture measurement with additional return loss measurement.

The correct measure to compare the calibration techniques is to study their relative standard deviation. We compute the moisture for each sample for each sample measurement performed using the algorithm described in the previous section and evaluate the standard deviation of each method. Since the methods are tested with materials of different moisture, we define the relative standard deviation as the ratio between the computed deviation and the sample moisture. The results are presented in Table I. In this table we have included a technique which maps directly the insertion loss to the moisture. This simpler technique can not compensate for the sample density, but can still find application in less critical and cheaper solutions.

All the measurements in this section have been performed using the Anritsu MS2036C VNA. The antennas and resonators were developed in house.

The results show clearly the advantage of the resonator based method in terms of accuracy. This method has the drawback, though, that a single measurement can take up considerable time. The in house developed device based on this method uses a search algorithm to define the resonance point and the bandwidth and this requires the measurement of about 30 to 50 frequency points. Each requires a retuning of the VCO, which takes several milliseconds

TABLE I
RELATIVE STANDARD DEVIATION OF THE DIFFERENT METHODS

Calibration method	Relative standard deviation
Resonator based	3 %
Insertion loss with phase	8.9 %
Insertion loss with reflect	14.7 %
Insertion loss only	14.3 %

to stabilise, thus rendering the measurement time several 100s of milliseconds. Therefore an experiment with moving sample, as can be expected when the sensor is integrated in a production line, could show a degradation of the accuracy obtained here.

The insertion loss based methods are instant, but show smaller accuracy. It is evident from the table that measuring the transmitter antenna reflection coefficient does not contribute the deembedding of the sample density. The measurement of the phase delay doubles the accuracy of a single measurement. As the method is instant, the accuracy can be additionally increased by performing multiple measurements on the same sample and averaging them. This can be done also in a production line. A drawback of the insertion loss method is its limited dynamic range. For samples with very high moisture content (say 60 % and above) the insertion loss is too great to be measured correctly.

IV. Conclusions

This paper compares several methods for calibration of microwave moisture meters depending on the device technology. The methods deembed the sample density from the measurement results. The insertion loss method, which correlates the losses of a microwave transmitted through the sample, shows good results for instant measurements of low moisture samples. The measurement can be made more precise by measuring the phase delay of the signal. The resonator based method, which correlates the resonance frequency and quality factor of a resonator, contacting the material, shows good results for precise measurement of high moisture samples.

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Adaptive Magnetizing Current Observer of Single-Phase Collector Motor Drive

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Abstract – **Adaptive magnetizing current observer of single-phase collector motor has been proposed in the paper. The electro-mechanical energy conversion in a single-phase collector motor is being represented trough a system of non-linear differential equations that includes the resistances and dynamic inductivities of the armature and field winding, spinning E.M.F. The observer gain matrix is designed to achieve quickly and accurately performance by the definition of a non-linear reference model. The experimental results show the improvements with regard to the robustness of parameter uncertainties and load disturbances in the proposed scheme. The observer performance has been very good even though the load torque is varying.**

Keywords – **Single-phase serial collector motor, Adaptive magnetizing current observer**

I. INTRODUCTION

Single-phase collector machines are being used mainly in household electric appliances and power tools. Closed-loop drives have superior dynamic performance, and allow for the implementation of energy-saving techniques [1, 2]. Most closed-loop drives require feedback of variables that are either unavailable or expensive to measure. In reality, it is impossible to achieve a completely "sensorless" closed-loop drive, i.e. having no voltage, current, or speed information.

For the optimal motor control, such as control provides maximum performance, optimum stabilization, the optimal adjustment of the position, it is necessary to have information about the dynamic torque on the motor shaft. This problem can be solved by means of direct measurement or by means of the state observer [3]. The first approach requires the use of torque sensor on the shaft of the motor which determine the rotational angle of the shaft.

Evaluation of the static moment using the observer requires the determination of easily measurable coordinates such as rotation speed and current of the motor. Since these values are measured in the common system of slave control, static moment can be calculated by the computer system [4].

The object of this work is to develop a magnetizing current adaptive observer of single-phase collector motor. It is necessary to investigate a performance of proposed observer for the dynamic and steady-state modes.

II. MATHEMATICAL MODELS

A. Magnetizing Current Observer

The mathematical models have been developed under the generally accepted assumptions [5, 6].

Electro-mechanical energy conversion in the single-phase collector motor can be shown using the equations for the instant values of the quantities [5, 6]. The state equation of the single-phase collector motor are given by [1]:

$$\dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{B}\mathbf{u} \tag{1}$$

where:

$$\mathbf{x} = \begin{bmatrix} i_a & i_{st} \end{bmatrix}^T; \quad \mathbf{u} = u_s; \quad \mathbf{A} = \begin{bmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{bmatrix}; \quad \mathbf{B} = \begin{bmatrix} b_1 \\ b_2 \end{bmatrix};$$

$$a_{11} = -\frac{L_m L_{st}}{L_e}\omega_m - \frac{(R_a + R_f)L_{st}}{L_e};$$

$$a_{12} = -\frac{L_m L_{st}}{L_e}\omega_m + \frac{R_{st} L_{fsd}}{L_e};$$

$$a_{21} = \frac{L_{sfd} L_m}{L_e}\omega_m + \frac{(R_a + R_f)L_{sfd}}{L_e};$$

$$a_{22} = \frac{L_{sfd} L_m}{L_e}\omega_m - \frac{R_{st}(L_a + L_f)}{L_e}; \quad b_1 = \frac{L_{st}}{L_e}; \quad b_2 = -\frac{L_{sfd}}{L_e};$$

$$L_e = L_s(L_a + L_f) - L_{fsd} L_{sfd}; \qquad L_a = L_{ad} + L_{a\sigma};$$

$$L_f = L_{fd} + L_{f\sigma}; \quad L_{st} = L_{std} + L_{st\sigma};$$

R_a, R_f, R_{st} – active resistances of armature winding, field winding, including the resistance of the brushes contact and the winding, that corresponds with the steel losses;
L_{ad}, L_{fd}, L_{sd}, L_{fsd}, L_{sfd} – dynamic inductances of the windings;
$L_{a\sigma}$, $L_{f\sigma}$, $L_{s\sigma}$ – static inductances of the windings;
$M=\psi_\delta(i_m)i_a$ – electromagnetic torque;
ψ_δ – air intermediate space linkage flux;
$i_m=i_a+i_{st}$ – magnetizing current;
$e=\psi_\delta(i_m)\omega_m$ – spinning E.M.F.;
ω_m – angular speed of the rotor.

The full order state observer which estimates the motor current and the magnetizing current is written by following equations:

$$p\hat{\mathbf{x}} = \mathbf{A}\hat{\mathbf{x}} + \mathbf{B}\mathbf{u} + \mathbf{L}\tilde{\mathbf{y}}; \ \tilde{\mathbf{y}} = \hat{\mathbf{y}} - \mathbf{y} \tag{2}$$

$$p\hat{\mathbf{x}} = (\mathbf{A} - \mathbf{L}\mathbf{C})\hat{\mathbf{x}} + \mathbf{B}\mathbf{u} + \mathbf{L}\mathbf{y}; \ \hat{\mathbf{y}} = \mathbf{C}\hat{\mathbf{x}} \tag{3}$$

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where: $\mathbf{L} = \begin{bmatrix} l_1 \\ l_2 \end{bmatrix}$.

Figure 1 shows the block diagram of the developed observer.

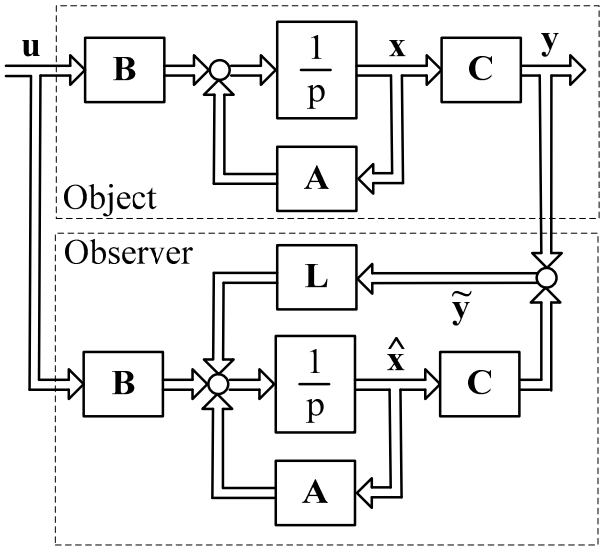

Fig. 1. Block diagram of the observer

Where ˆ means the estimated values and **L** is the observer gain matrix which is decided so that (3) can be stable. **L** is calculated by the following equation so that the observer poles S_O are proportional to those of the single-phase collector motor S_M (proportional constant k_p>1):

$$S_O = k_p S_M \tag{4}$$

Choice of k_p determining the observer's performance, in general, is a complex task. Usually selected k_p so that the observer's performance can be several times greater than the system's performance, which is closed thereby.

Characteristic polynomial of the object is determined by the expression

$$H_M(p) = \det[p\mathbf{I} - \mathbf{A}] = 0 \tag{5}$$

Characteristic polynomial of the observer shall be determined by the expression

$$H_O(p) = \det[p\mathbf{I} - (\mathbf{A} - \mathbf{LC})] = 0 \tag{6}$$

The determination of the elements of the matrix **L** is achieved by the equivalence ratios for the same degree of operator p of the characteristic polynomial of the closed system with those of the desired characteristic polynomial.

$$H_M(p) = p^2 - (a_{11} + a_{22})p - a_{12}a_{21} + a_{11}a_{22} = 0 \tag{7}$$

$$H_O(p) = p^2 + (l_1 - a_{11} - a_{22})p - l_1 a_{22} - a_{12}a_{21} + a_{11}a_{22} + l_2 a_{22} = 0 \tag{8}$$

The resulting system of equations defining elements of the matrix **L**:

$$\begin{cases} -k_p(a_{11} + a_{22}) = l_1 - a_{11} - a_{22}; \\ k_p(-a_{12}a_{21} + a_{11}a_{22}) = -l_1 a_{22} - a_{12}a_{21} + a_{11}a_{22} + l_2 a_{22}. \end{cases} \tag{9}$$

The coefficients of the matrix of the observer are:

$$\begin{cases} l_1 = -(k_p - 1)(a_{11} + a_{22}) \\ l_2 = -(k_p - 1)\dfrac{a_{12}a_{21} + a_{22}^2}{a_{12}} \end{cases} \tag{10}$$

B. Adaptive Scheme for Speed Estimation

When the motor speed is not measured, unknown parameters are included in the state observer equation (3). In order to derive the adaptive scheme, Lyapunov's theorem is used. The estimation error of the armature current and magnetizing current is given by the following equation:

$$p\mathbf{e} = (\mathbf{A} + \mathbf{LC})\mathbf{e} - \Delta\mathbf{A}\hat{\mathbf{x}} \tag{11}$$

where

$\mathbf{e} = \mathbf{x} - \hat{\mathbf{x}}$;

$$\Delta\mathbf{A} = \hat{\mathbf{A}} - \mathbf{A} = \begin{bmatrix} -\dfrac{L_m L_{st}}{L_e}\Delta\omega_m & -\dfrac{L_m L_{st}}{L_e}\Delta\omega_m \\ \dfrac{L_m L_{sfd}}{L_e}\Delta\omega_m & \dfrac{L_m L_{sfd}}{L_e}\Delta\omega_m \end{bmatrix};$$

$\Delta\omega_m = \hat{\omega}_m - \omega_m$.

From the Lyapunov function candidate [4], we can find the adaptive scheme for the speed estimation:

$$-2\Delta\omega_m \frac{L_m L_{st}}{L_e}(\hat{i}_a + \hat{i}_{st})e_{ia} - \frac{2\Delta\omega_m}{\lambda}\frac{d\hat{\omega}_m}{dt} = 0 \tag{12}$$

$$\frac{d\hat{\omega}_m}{dt} = -\lambda\frac{L_m L_{st}}{L_e}(\hat{i}_a + \hat{i}_{st})e_{ia} \tag{13}$$

Where $e_{ia} = i_a - \hat{i}_a$.

The following integral adaptive scheme is used in order to improve the response of the speed estimation.

$$\hat{\omega}_m = K_I \int (\hat{i}_a + \hat{i}_{st})(i_a - \hat{i}_a)dt \tag{14}$$

where K_I is positive constant.

III. Received Results

The on-line monitoring systems imply two main parts: hardware (sensors, transducers, ADC, serial transmission) and software (field module programming, transmission protocols, user interface). The Hall Effect based current transducer, LTS 15-NP was used in the current measurement circuits. The accuracy of the current transducer used in the circuit is better than ±0.2 % at 25 °C and has a bandwidth of 100 kHz [7]. This transducer

requires a unipolar power supply of +5V, and can measure DC and AC currents. The reference point of the transducer with zero primary current is 2.5 V, which is equal to the half of the supply rail voltage. The maximum gain of $(0.625/I_{PN})$V/A (I_{PN}=15A) can be achieved and the output voltage of the current transducer can be given by $V_{out}=(0.625/I_{PN})I_P+2.5$. The Hall Effect based voltage transducer, LV 25-P was used in the voltage measurement circuits. The accuracy of the voltage transducer used in the circuit is better than ±0.9 % at 25 °C [8]. This transducer requires a ±15V power supply, and can measure DC, AC and pulsed voltage. The maximum gain can be achieved and the output voltage of the voltage transducer can be given by $V_{out}=0.01V_P$ (V_{PN}=400V). The NI USB-6009 board work as the measurement platform. This board is compatible with Simulink®, and includes: 8 analog inputs at 12 or 14 bits, up to 48 kS/s; 2 analog outputs at 12 bits; 12 TTL/CMOS digital I/O lines; and One 32-bit, 5 MHz counter.

The block diagram of the developed monitoring system is shown in Fig. 2.

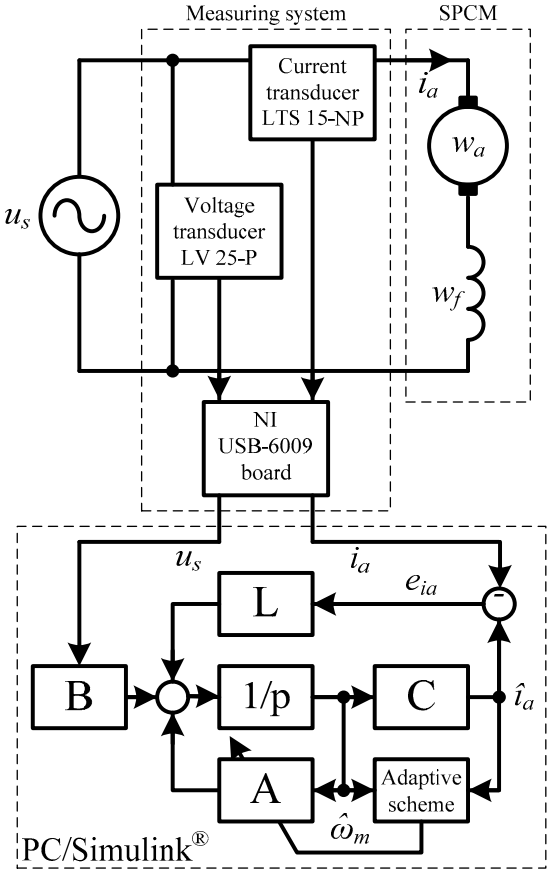

Fig. 2. Adaptive observer and motor drive

The basic circuit of the proposed scheme consists of a single-phase collector electric motor (SPCM) for HPT type BUR2-160E having ratings as 182W, 230V, 50 Hz which is connected to drive power tool BUR2-160E. The technical data of the electric motor are given in Appendix.

System voltage control can be used as a soft start and to adjust the rotational speed of the machine. Experimental research is carried out when setting the voltage U_s from 2,5s to 6,0s voltage increases from 0 to $U_{s.ref}$=100V. Parameters of the magnetizing current observer k_p and adaptive scheme for speed estimation K_I are k_p=10, $K_I=10^5$. Fig. 3 and fig. 4 shows the measurement supply voltage.

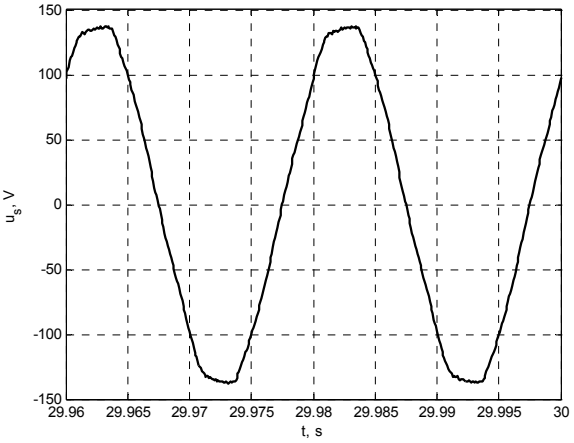

Fig. 3. Dependence $u_s=f(t)$

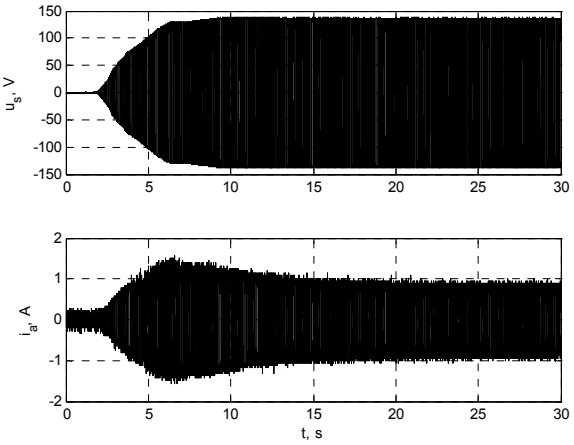

Fig. 4. Dependences u_s, $i_a=f(t)$

With the use of the simulation models the dependencies of the observed characteristics of the examined motor and the mechanism are found out in a function of time. Parts of the received results are being shown in the respective figures.

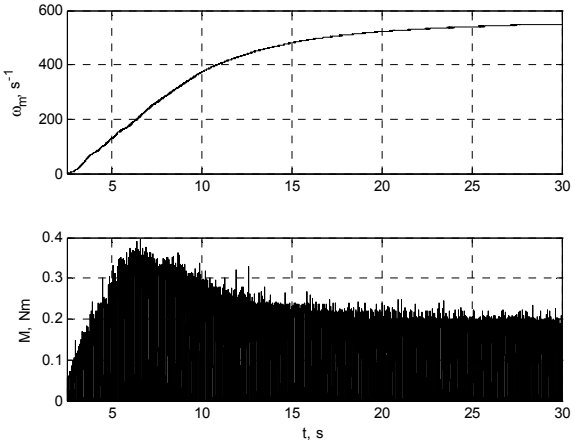

Fig. 5. Dependences ω_m, $M=f(t)$

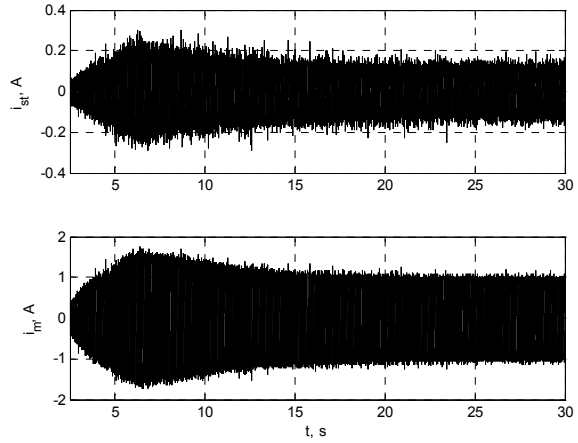

Fig. 6. Dependences i_{st}, $i_m=f(t)$

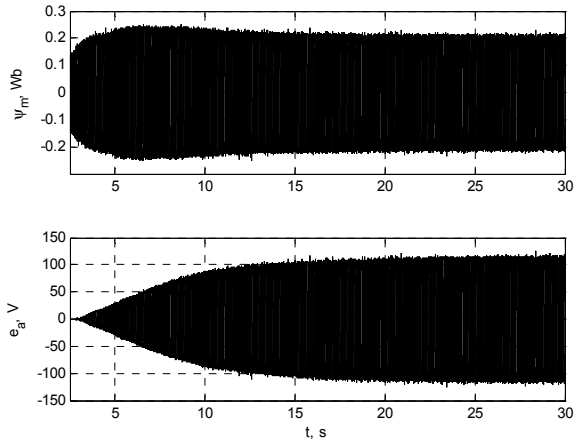

Fig. 7. Dependences ψ_m, $e_a=f(t)$

The measured (i_{am}) and the observed (i_{ao}) motor current are presented in fig. 8.

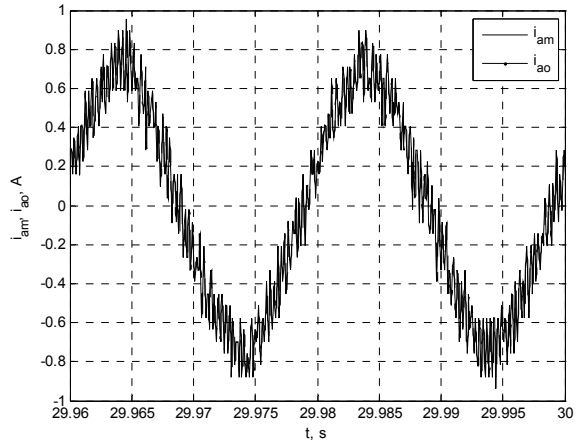

Fig. 8. Dependences i_{am}, $i_{ao}=f(t)$

From the figure can be read fast and accurate action of the observer, where it appears that the actual value reaches the set.

IV. CONCLUSION

A magnetizing current adaptive observer of single-phase collector motor has been proposed in the paper. The electro-mechanical energy conversion in a single-phase collector motor is being represented trough a system of non-linear differential equations that includes the resistances and dynamic inductivities of the armature and field winding, spinning E.M.F. The observer gain matrix is designed to achieve quickly and accurately performance by the definition of a non-linear reference model. The experimental results show the improvements with regard to the robustness of parameter uncertainties and load disturbances in the proposed scheme. The observer performance has been very good.

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APPENDIX

Technical data and parameters of a single-phase collector electric motor for HPT type BUR2-160E:
P_N=182W; U_{aN}=230V; I_N=1,88A; U_{brush}=2,5V f=50Hz; η_N=53%; cosφ_N=0,93; n_N=27081min^{-1}; J_m=0,03.10^{-3}kgm^2;
R_a=3,2Ω; R_f=11,2Ω; $L_{sfd}=L_{fsd}=L_{sd}=L_{fd}$; $L_{a\sigma}$=4,5.10^{-3}H; $L_{f\sigma}$=3.10^{-3}H; $L_{s\sigma}=L_{f\sigma}$.
Approximating correlations for defining of parameters:
$L_{ad}(i_a)=w_a(a_1b_1/(b_1+|i_a|)^2+c_1)$; $L_{fd}(i_a)=w_fa_2b_2/(b_2+|i_a|)^2$; $\psi_\delta(i_m)=w_aa_3i_m/(b_3+|i_m|)$; $R_s(I_a)=a_4+b_4e^{c4I_a}$;
w_a=264; w_f=376; a_1=0,984.10^{-4}; b_1=-0,7143; c_1=0,4321.10^{-4}; a$_2$=6,9764.10^{-4}; b_2=0,6723; a_3=4,9257.10^{-4}; b$_3$=0,5329; a_4=56,259; b_4=604,12; c_4=-1,709.

Fully Integrated PVT Detection and Impedance Self-Calibration System Design

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Abstract – **The paper presents a fully integrated PVT variation detection and on-die resistance calibration system for high-speed applications. The proposed system separately measures and compensates the MOS device resistance deviation due to process, voltage and temperature variation. Temperature detection is performed in a range of -40°C to 125°C independently from supply voltage variations. Logic block of mixed-signal system automatically starts MOS resistance calibration process when PVT variation is detected. The design is implemented in 28nm CMOS process. The presented compensation method can be used in the I/O circuits of such standards as DDR (Double Data Rate), USB (Universal Serial Bus), PCI (Peripheral Component Interconnect), etc.**

Keywords – **self-calibration, PVT compensation, temperature, resistance variation, CMOS**

I. Introduction

With continues shrinking of CMOS technologies, the components of integrated circuits (IC) become more inaccurate and sensitive to external factors such as temperature or supply voltage variations. On the other hand IC fabrication process becomes more complicated and has significant impact on IC component quality and precision [1]. One of the most sensitive analog blocks of high-speed ICs are communication input/output (I/O) blocks. As I/Os are placed on the border of IC, the far ends of the chip can be in different process-voltage-temperature (PVT) conditions. The reliability of ICs I/O performance is based on accurate on-die resistance termination phenomena, which is required to reduce reflections in transmission lines [2]. Variation of CMOS based resistor due to PVT variations can reach about ±50%, while the resistances of NMOS and PMOS transistors can be different in same conditions [3]. MOS resistance values in the far ends of the IC can also be different at the same moment. To eliminate the PVT effect on I/O performance a novel calibration system is developed which includes PVT detection and resistance calibration blocks. In terms of reducing production costs it is not profitable to increase the number of IC external pins [4]. In proposed calibration architecture internal high-precision quartz generator frequency is used as reference parameter which allows using multiple calibration circuits in the same IC without any additional pin. Next chapters describe details and advantages of proposed fully integrated self-calibrated mixed-signal PVT variation detection and compensation architecture.

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II. System Architecture

Proposed compensation system estimates supply voltage and operating temperature variations during whole period of IC operation and starts termination resistance calibration circuit if PVT variations are detected, Fig. 1. System contains power supply and temperature deviation detection blocks, MOS resistance calibration block and logic block. The information from PVT detection block is analyzed and resistance calibration block is controlled by logic block.

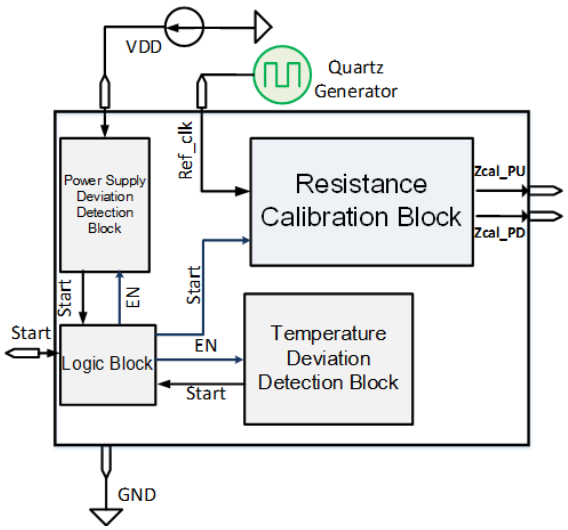

Fig. 1. PVT variation detection and resistance calibration system

Power supply and temperature deviation detection blocks can be switched off by EN signals from logic block if it is not needed to track PVT fluctuations all the time. Logic block starts MOS resistance calibration when posedge *Start* signals are registered from detection blocks. PVT variation detection precision is programmable by logic block which makes the proposed mechanism more universal and user friendly.

A. Temperature deviation detection block

The principle of temperature detection is based on measurement of the difference between two logarithmic amplifiers with a shared voltage bias and load resistance parameters, Fig.2. The bias voltage is generated internally and can be implemented by a simple resistive divider. The circuit can operate in two modes, when $V_{bias1}=V_{bias2}=V_{bias}$ (common bias mode), and when $V_{bias2}=m_bV_{bias1}$ (scaled bias mode, m_b is the bias scaling factor). Both current branches in Fig.1 have identical, preferably matched diodes.

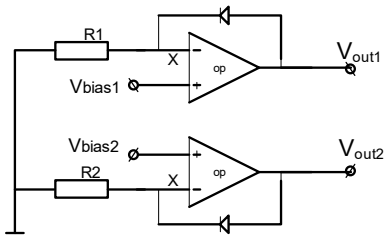

Fig 2.Temperature detection and sensing circuit principle

The output voltage difference after differential amplification by A, (V_{det}) will be described as:

$$V_{det} = A \cdot (V_{out\,2} - V_{out\,1}) \quad (1)$$

For common bias mode, when $V_{bias1}=V_{bias2}$ and $R_2=m_rR_1$, the following expression will take place:

$$V_{out\,2} - V_{out\,1} = V_T \cdot \ln\frac{1}{m_r} \quad (2)$$

For scaled bias mode, when $V_{bias2}=m_bV_{bias1}$ and $R_2=R_1$, the following expression will take place:

$$V_{out\,2} - V_{out\,1} = (m_b - 1) \cdot V_{bias} + T \cdot \frac{k}{q} \cdot \ln(m_b) \quad (3)$$

The resistor scaling can be used along with bias voltage scaling in order to increase the detected voltage range:

$$V_{out\,2} - V_{out\,1} = (m_b - 1) \cdot V_{bias} + T \cdot \frac{k}{q} \ln\left(\frac{m_b}{m_r}\right) \quad (4)$$

As it can be seen from Eq. 2-4, the detected voltage is strictly proportional to temperature and has no dependence on other factors such as operating voltage, logarithmic amplifier bias voltage and process corner. The parameters A, m_b and m_r serve as detected voltage scaling factors, which can be defined for a specific application. The detected voltage can be stored or processed after analog to digital conversion.

The introduction of bias voltage scaling can be used to center the detected voltage range around a specific DC offset value.

The temperature detection system consists of the logarithmic amplification pair with sensing diodes, controlled gain differential to single amplifier, bias generation and control blocks, Fig. 3.

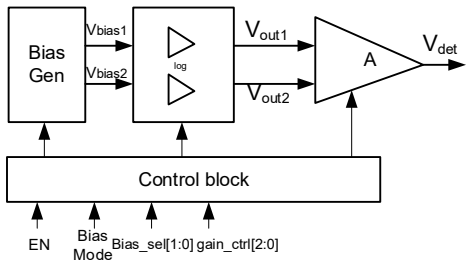

Fig 3. Detection circuit block diagram

The control block implements basic digital logic and performs signal conditioning to control the bias generator operation mode, dual to single amplifier gain and allows to put the circuit into power down when detection is not required. The sensing diodes in this paper were implemented as forward biased drain-bulk diodes of PMOS devices [5].

B. Power supply deviation detection block

Detection of supply voltage variation is implemented by mixed-signal circuit. Analog block is responsible for power supply deviation detection, while digital part is responsible for comparing deviated values with reference (Fig. 4).

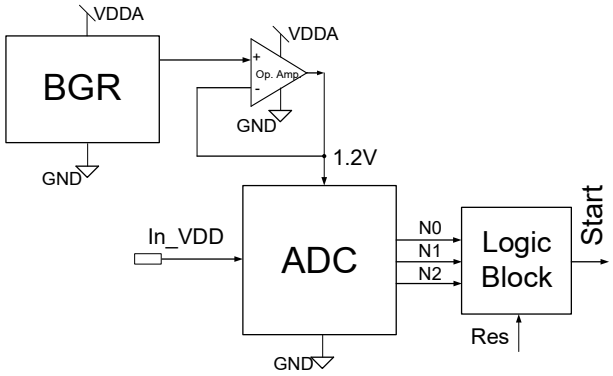

Fig 4. Power supply detection and estimation system architecture

Supply voltage value at the start time of IC operation is considered as a reference. During further operation deviated power supply voltage value is being compared with the reference value. When deviation is detected by digital logic block, *Start* posedge signal announcing PVT variation is generated. At this moment as a reference value new supply voltage serves, instead of previous values. So reference value is not fixed and it is changed after each detected PVT variation.

Reference voltage value is converted to binary code by analog-digital converter (ADC) and is stored in the register. When power supply voltage is deviated from reference one, corresponding binary code is also changed which is being detected by logic block during comparing current equivalent code with the reference one stored in the register.

For accurate detection system it is mandatory to have almost PVT independent ADC circuit. To provide mentioned requirement, output voltage of designed bandgap reference (BGR) circuit is used as a power supply for ADC block. Output voltage of designed BGR is 1.2V with 2.1% high precision during all possible PVT fluctuations [6]. For analog-digital conversions 3-bit flash ADC circuit is chosen which input voltage is the *In_VDD* power supply of the system. Flash ADC resistor values are selected accordingly to provide reference voltages to the inputs of comparators in the range of ±10% of *In_VDD*.

Designed operational amplifier is very stable to PVT fluctuations and operates as a voltage follower. It serves as a buffer for the output voltage of BGR to be able to feed the ADC block.

Simplified timing diagram of power supply deviation detection logic block is presented in Fig. 5, where *Res* is the logic block reset signal, *Ref_code* is the reference equivalent 3-bit code during previous calibration and is stored in register, N is the corresponding ADC output 3-bit code of the exact supply voltage value (values are chosen randomly). *Start* is the output signal of detection circuit which announces the PVT variation and launches the resistance calibration circuit.

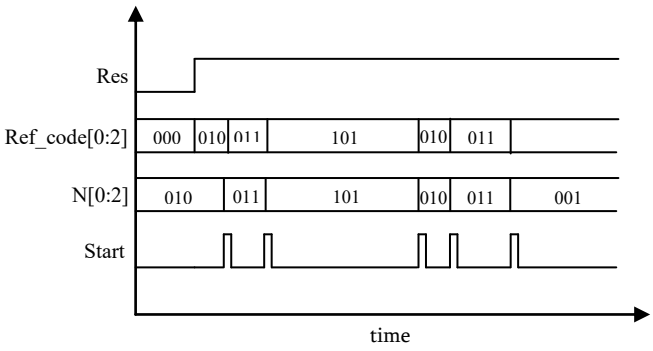

Fig. 5. Power supply deviation detection logic block simplified timing diagram

C. Resistance calibration block

Proposed method provides opportunity to realize NMOS and PMOS transistor resistance parallel calibration. As a reference parameter only reference clock frequency of quartz generator is used. PMOS and NMOS resistance calibration circuit is presented in Fig. 6. Analog block of calibration circuit contains two VCOs for NMOS and PMOS resistance calibration. Logic block compares VCO output frequencies with reference clock frequency. As a result of frequency variation logic block generates N-bit thermometric code which corresponds to resistance variation. Logic block is a RTL code which controls the calibration system.

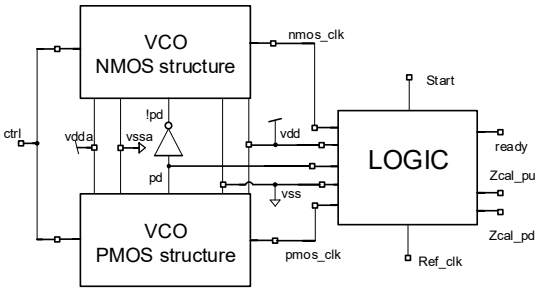

Fig. 6. PMOS and NMOS resistance calibration circuit

PVT detection is based on current variation effect in VCO biasing circuit (Fig. 7).

In VCO biasing circuit, the correctly designed and negative-feedback connected operational amplifier is very stable due to PVT fluctuations. The positive input of operational amplifier in negative feedback circuit gets V_{ctrl} signal which controls VCO output frequency. The second input of operational amplifier duplicates V_{ctrl} voltage and is connected to drain of the resistive NMOS transistor (circled transistor in fig. 7). It operates in triode region and the gate is connected to the highest voltage.

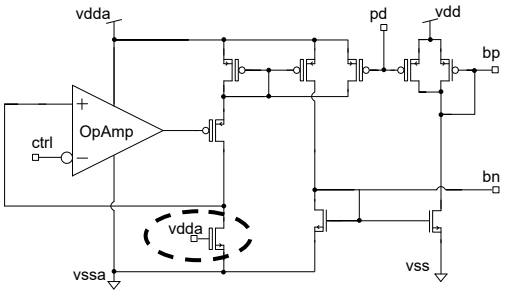

Fig. 7. VCO biasing circuit (NMOS structure)

Drain voltage of the observed transistor is stable and equal to V_{ctrl} so the current flowing through the transistor will be determined by the following equation (5):

$$I_{NMOS} = \frac{V_{ctrl}}{R_{NMOS}}, \quad (5)$$

where I_{NMOS} is the current flowing through NMOS transistor, V_{ctrl} is the control voltage of VCO and R_{NMOS} is the resistance of triode connected NMOS transistor.

R_{NMOS} is a CMOS resistor based on NMOS transistor which is very unstable to PVT fluctuations. Variations of R_{NMOS} result in variations of I_{NMOS} which flows through VCO biasing circuit current mirror and generates bias voltages responsible for VCO output frequency. So the VCO output frequency variations are only result of NMOS resistance variations. Proposed method inaccuracy is about 8%. The same approach for PMOS based resistor variation detection is used.

Logic block consists of two counters (to count VCO output posedge transitions during *Ref_clk* single period), two decoders (to convert ($\log_2$N)-bit binary counter result to N-bit thermometric code), two registers (to save calibration codes) and control block (to control RTL block). Fig. 8 shows simplified timing diagrams for the described compensation mechanism [7].

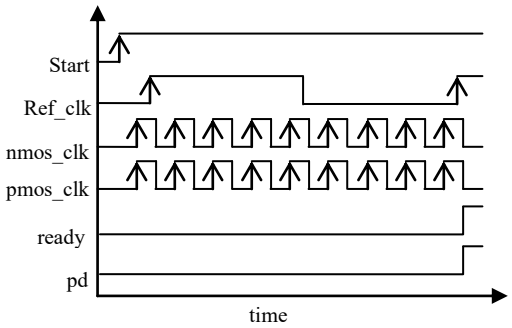

Fig. 8. Resistance calibration logic block simplified timing diagram

III. Simulation Results

The proposed system was designed and implemented for a 28nm CMOS process, with 0.9V core device and 1.8V thick-gate nominal voltages. Simulations have been

performed using Synopsys circuit level simulator Hspice [8]. The temperature detection circuit was simulated for -40°C to 125°C temperature range. Fig. 9 shows DC sweep simulation results for the common bias operation mode.

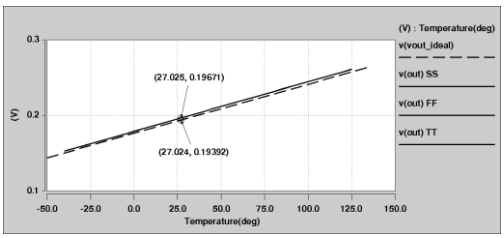

Fig. 9. Detector output voltage dependence on temperature

The considered circuit had the resistor scaling factor m_r=1/12 and dual to single amplifier gain was set to 3. The mentioned plot shows detector circuit voltage dependence on temperature in range of -40°C to125°C for SS minimal voltage, TT typical voltage and FF maximal voltage PVT corners. The dashed line corresponds to ideal dependence following from expression (3). The simulated voltage values show less than 3 mV deviation from theoretical value. As the formula (3) suggests the detected voltage is expected to have no dependence in supply voltage or process corner. The detected voltage is 196.6 mV at room temperature with range of 152 mV to 260 mV for -40°C to 125°C temperature range. The detected voltage can be stored or processed after analog to digital conversion. For example a 3 bit and 6 bit digital conversion will yield ~20°C and ~2.5°C per bit temperature detection resolution respectively.

The power supply detection circuit was simulated for 0.81V to 0.99V voltage range (±10% of 0.9V supply voltage). Simulation results using 3-bit ADC show ~25mV per bit supply voltage detection resolution. For higher precision more ADC bits are required. For example with 6-bit ADC detection resolution is ~3mV per bit supply voltage.

MOS resistance calibration precision is estimated according to measured VCO frequency variation detection system inaccuracy. System non-ideality is presented in Fig. 10.

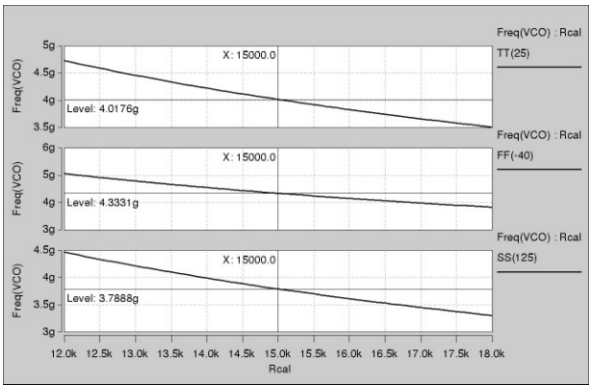

Fig. 10. NMOS structure VCO output frequencies with 15k Ohm ideal resister at three main corners

It is seen from the graph that with ideally constant resistor (15k Ohm in the graph) used instead of described circled NMOS transistor in Fig. 7, VCO output frequency is not constant in three main corners. In typical case *nmos_clk=4.02GHz*, in best case *nmos_clk =4.33GHz* and in worst case *nmos_clk=3.79GHz*. So provided method inaccuracy is about 8%. About the same inaccuracy has PMOS resistance variation detection circuit.

IV. Conclusion

A fully integrated PVT variation detection and compensation circuit is presented. The suggested system employs a principally new temperature detection method which is based on differential amplification of logarithmic amplifier outputs. For providing high accuracy and supply independency of power supply variation detection circuit it is fed by high precision BGR. The latter does not require external sensor elements and has good stability over PVT variations. When temperature or supply voltage change is detected a digital control module starts the on-die impedance calibration block which compensates for MOS device impedance variation. PVT detection precision is controllable by user and is limited by ADC accuracy. The significant advantage of the presented method is capability of impedance compensation without any external elements with 8% precision. The solution was implemented in a 28nm process.

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PLL Control Voltage Stabilization Method for High-Speed Systems

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Abstract – **High-speed PLL control voltage stabilization method is presented in the paper. Fully integrated modified PLL circuit is designed accordingly. Stabilization principle is based on compensation of the LPF MOSFET capacitor output voltage which is unstable due to gate oxide leakage currents. Stabilization is implemented by using analog latch circuit and holding correct VCO control voltage. Latched voltage can be refreshed by digital logic block when PVT variation is detected in the system. The presented compensation method can be used in the I/O circuits of such standards as DDR (Double Data Rate), USB (Universal Serial Bus), PCI (Peripheral Component Interconnect), etc.**

Keywords – **PLL, VCO Control Voltage, Analog Latch, Stabilization, PVT Detection**

I. INTRODUCTION

Phase locked loop or PLL is a control system which generates frequency for the system. PLLs are widely used in radio electronics, telecommunication and other electronic applications [1]. As technology moves deeper into sub-micron, device sizes become smaller. Now days they can go down until 7nm. Due to mentioned above processes PVT variations become more significant which cause a lot of undesirable effects, including MOSFET transistor gate oxide leakage current increase, threshold voltage deviation, etc [2]. Device parameter variations can affect on system performance, as well as change power consumption. All these factors make the system unstable and reduce its accuracy.

PLL is one of the most sensitive circuits to PVT variations. The main high-speed block of PLL is voltage controlled oscillator (VCO) which output frequency depends on its control voltage. Usually MOSFET based capacitor is used in PLL low-pass filter (LPF) block. VCO control voltage is provided by LPF block capacitor which leakage currents can drop the control voltage value. As a result VCO output frequency can be changed. Besides control voltage fluctuations, PVT variations also affect on VCO generated frequency value. PVT variations can change frequency from target value by up to 50% [3]. To recover frequency required nominal value more PLL cycles are needed. In this paper PLL control voltage stabilization methodology is proposed which allows increasing control voltage stability. In next chapters proposed method and accordingly realized mixed-signal circuit solution are described.

II. PVT VARIATION EFFECT ON HIGH-SPEED PLL

Manufacturing process non-ideality is becoming more significant in modern sub-micron technologies. Devices are becoming more sensitive to process-voltage-temperature (PVT) variations which can cause MOSFET threshold voltage and gate oxide capacitance quality deviations, and devices key parameters can move far from typical values. It can effect on performance of system especially in high-speed systems.

As it was mentioned, PLL (especially VCO block) is one of the most sensitive circuits to PVT variations. Based on this fact, VCO can be used to detect PVT variations. A 5-stage differential VCO and its delay cell used in proposed design are presented in Fig.1. and Fig.2 correspondingly.

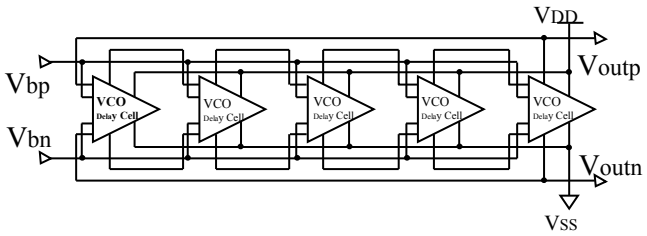

Fig. 1. Voltage controlled oscillator with 5 stage structure

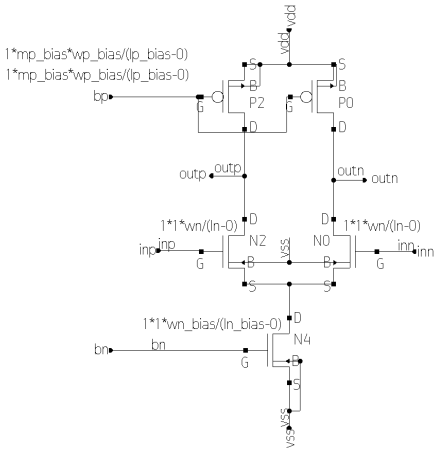

Fig. 2. Differential delay cell

Following expression shows VCO's output frequency when bias circuit is designed correctly:

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$$F_{vco} \sim \frac{I_{tail}}{2 * C_n * N * V_{swg}}, \quad (1)$$

where output frequency of VCO is F_{VCO}, source current is the I_{tail} (tail current), VCO delay cell output capacitance is the C_n, N is the number of VCO's stages and finally V_{swg} is the voltage swing in the VCO output. For saturated current tails [4]:

$$I_{tail} \sim k(V_{gs} - V_{th})^2 * (1 + \lambda * V_{ds}), \quad (2)$$

where:

$$\begin{aligned} V_{gs} &= V_{dd} - V_{bp} = f(V), \\ V_{th} &= f(\mathrm{P}, \mathrm{T}), \\ C_n &= f(\mathrm{P}). \end{aligned} \quad (3)$$

Here V_{gs} is a function of supply voltage, V_{th} is a function of process and temperature and C_n is a function of the process.

On the other hand, technologies move deeper into sub-micron and decrease gate oxide (C_{OX}) thickness, and in the meantime increase the leakage current.

Usually MOSFET based capacitor is used in PLL low-pass filter (LPF) block, which losses became significant as mentioned. Due to charge dissipation in LPF block VCO control voltage value will be decreased and correspondingly drop output frequency. As a result more cycles will be necessary for recovering deviated frequency.

III. PVT Variation Detection Mechanism

PVT detection mechanism is based on comparison of reference clock frequency with VCO output frequency. As a reference clock high precision quartz generator output frequency is used [5]. The PVT detection block diagram is shown in Fig. 3.

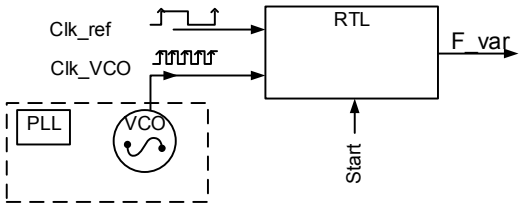

Fig. 3. PVT detection circuit block diagram

RTL block compares the VCO output frequency (*Clk_VCO*) with reference clock frequency (*Clk_ref*) and generates binary code which contains information about VCO frequency change. Knowing f_{VCO} frequency code for typical condition allows detecting PVT changes when frequency is degraded.

With *Start* signal RTL's counter block starts counting the *Clk_VCO* posedge transitions from reference clock first posedge transition until the second posedge transition. As a result counter returns N-bit binary code. When the calculation is finished and binary code is generated *ready* signal is switched high to announce the end of counter work. RTL control block input and output timing diagrams are presented in Fig. 4.

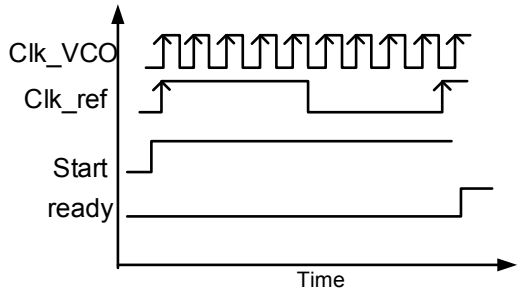

Fig. 4. Timing diagrams of PVT detection control block

By positive *ready* signal digital comparator is enabled which compares new counted N-bit *CNT* code with reference code which corresponds to VCO output frequency during previous PVT settings. RTL block diagram is shown in Fig. 5.

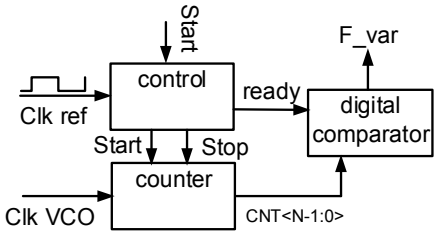

Fig. 5. RTL block diagram

If the PVT settings are changed, N-bit *CNT* code will also be changed and will not match with reference code value stored in N-bit *Ref_code* register anymore. As a result digital comparator will generate positive *F_var* signal which inform other blocks that PVT variation is detected. Comparator operation cycles are presented in Fig. 6 block diagram.

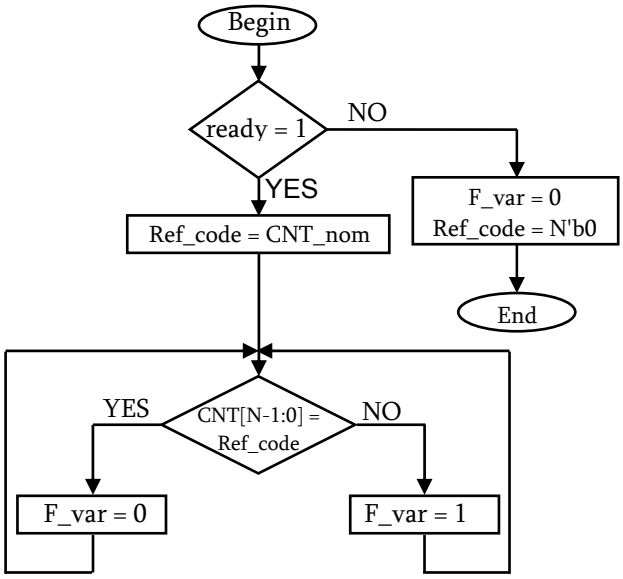

Fig. 6. Digital comparator operation block diagram

When *ready* signal is not active (*ready=0*), *F_var=0* and *Ref_code=N'b0*. With positive value of *ready* signal VCO output nominal frequency corresponding code (*CNT_nom*) is saved in *Ref_code* register. During all operation period comparator compares N-bit *CNT* code value of exact moment with reference code. When difference is detected the *F_var* signal is generated. *F_var* signal value remains high until *CNT* code is not equal to *CNT_nom*. This process is periodical during circuit operation.

CNT code and *Ref_code* register sizes are chosen according proportion of VCO maximum frequency across all PVT corners and quartz generator reference frequency. For example if the VCO maximum frequency is 7GHz and reference clock frequency is 100MHz, it means that counter will count 70 VCO output signal posedge transitions during reference clock single period. So to be able to store number 70, 7-bit register (maximum ability will be 128) will be required.

Digital comparator input and output timing waveforms for random 7-bit *CNT* code values are presented in Fig. 7. It is assumed that VCO output nominal frequency at typical PVT conditions is 5GHz, reference clock frequency is 100MHz, so *CNT_nom=50*.

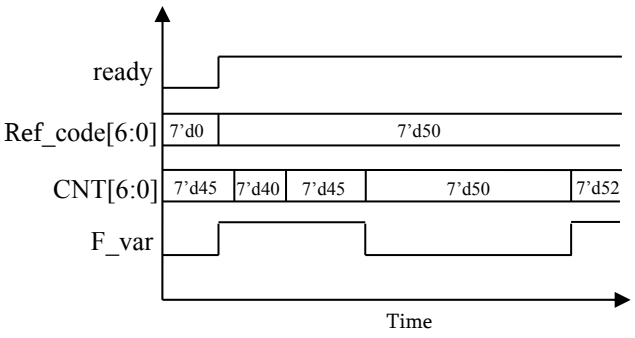

Fig. 7. Timing diagrams of digital comparator

Control block is responsible for detection activation and deactivation also it is controlling the counter and digital comparator parts.

IV. Proposed PLL Structure

As it was mentioned in chapter II, due to charge dissipation in LPF block VCO control voltage value will be decreased and correspondingly drop output frequency. To overcome this fact and avoid from more operation cycles for recovering deviated frequency, new PLL structure with control voltage stabilization block is proposed (Fig. 8).

The key scheme of proposed circuit is analog latch which is based on operational amplifiers operating as input voltage followers. Operational amplifiers are high gain and very stable to PVT fluctuations so analog latch don't add any inaccuracy to the main circuit.

The role of analog latch is to store fixed VCO control voltage instead of getting it from LPF block. This method gives an opportunity to exclude LPF cap leakage current influence on control voltage value.

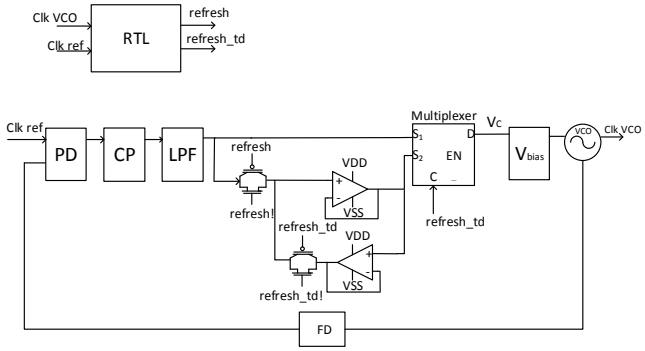

Fig. 8. The proposed PLL structure

During operation one of two paths is in active mode and is selected by multiplexer which is controlled by *refresh_td* signal. *Refresh_td* signal is provided by RTL block and follows digital comparator output *F_var* signal after some Δt delay time.

At the beginning of circuit operation and at the time when PVT variation is detected (which means VCO frequency is changed), PLL is in refresh mode (*F_var=1, refresh=1, refresh_td=1*) and added analog latch block is disabled by transmission gates which are being controlled by *refresh* and *refresh_td* signals of RTL block.

When PLL fixes the target control voltage on LPF block capacitor, transmission gates are switched (*F_var=0, refresh=0, refresh_td=1*). In this stage multiplexer is still passing LPF output voltage and refresh-controlled transmission gate is open. After Δt delay time, which corresponds to operational amplifier settling time, *refresh*-controlled transmission gate is switched off and *refresh_td*-controlled one is switched on. It is important to exclude switching on both transmission gates at the same time to avoid uncontrollable voltage values between two transmission gates (analog latch input). In this stage multiplexer takes stored control voltage from analog latch.

Behavior of *RTL* block *F_var, refresh* and *refresh_td* signals is presented in Fig. 9.

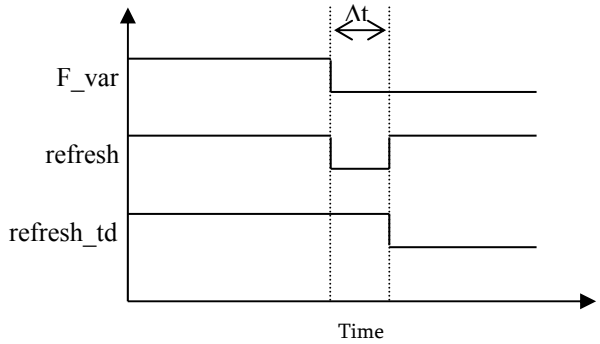

Fig. 9. Timing diagrams of F_var, refresh and refresh_td signals

Starting from this moment VCO control voltage is contributed from analog latch which is excluding mentioned leakage current error. PLL remains in this mode until RTL block detects PVT changes and generates *F_var* signal accordingly. It opens the standard PLL loop and after few cycles PLL recovers the target frequency.

V. Simulation Results

Simulations have been performed using Synopsys circuit level simulator Hspice for 27 PVT corners, including SS (slow-slow), TT (typical-typical), FF(fast-fast), SF (slow-fast), FS (fast-slow) with supply voltage and temperature variations using 28nm technology node [6]. VCO control voltage stabilization methodology was tasted on classical 5GHz PLL and 100 MHz stable reference clock.

The VCO output frequency for general PVT corners is shown in Table 1 (main 3 PVT corners are highlighted).

Temp.	Voltage	TT	FF	SS
-40	max	6,16	7,27	5,25
25	max	5,79	6,53	4,76
125	max	5,25	6,16	4,35
-40	min	4,40	5,40	3,27
25	min	4,15	5,14	3,35
125	min	3,96	4,84	3,12
-40	typ	5,40	6,35	4,34
25	typ	5	6,02	4,11
125	typ	4,64	5,53	3,76

Table 1. VCO Frequencies For General PVT Corners

As it is seen from the table there is more than 50% frequency variation due to PVT fluctuations. For sensitive circuit such as VCO it will affect generated frequency. For high accuracy and proper operation of proposed circuit, low offset and high gain operational amplifiers are used in analog latch block. To have wide input swing thick oxide MOS transistors are chosen. Operational amplifier input/output waveforms at typical conditions are presented in Fig. 10, where it is seen that operational amplifier supports wide range for VCO control voltage.

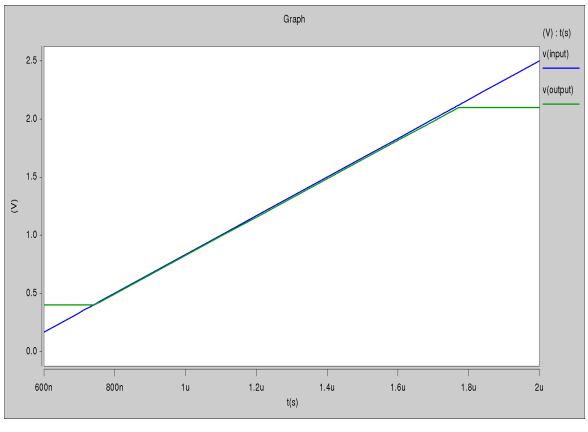

Fig. 10. Operational amplifier input/output waveforms at typical conditions

Operational amplifier Δt settling time is defined by user in RTL block, which should be equal to amplifier input/output delay at the worst PVT conditions. Δt delay also depends on change of input voltage.

Simulation results of operational amplifier for full input swing at the worst PVT corner are presented in Fig. 11.

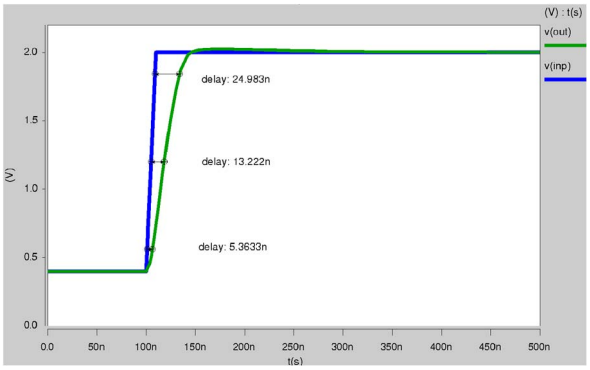

Fig. 11. Operational amplifier input/output delay simulation at worst PVT conditions

As it is seen from the simulation measurements, Δt settling time is ~25ns for the worst case.

VI. Conclusion

High-Speed PLL control voltage stabilization method is proposed and fully integrated mixed-signal circuit is designed in 28nm technology node. As a core scheme analog latch circuit is used which stores fixed VCO control voltage instead of getting it from LPF block. This method gives an opportunity to exclude LPF cap leakage current influence on control voltage value. Latched voltage is refreshed by proposed digital logic when PVT variation is detected in the system. PVT detection mechanism is based on comparison of reference clock frequency with VCO output frequency. As a reference clock high precision 100 MHZ quartz generator output frequency is used. Temperature and supply voltage deviation detection precision is programmable by user. It makes the proposed circuit usable for different system requirements.

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Power and Signal Integrity Design of TSV in 3D Ring Oscillator

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Abstract – **The coupling between adjacent through-silicon vias (TSVs) in 3D IC has been designed and analyzed from the power and frequency view. At first presented 2D 13 stage ring oscillator which consists of 45nm VTH CMOS transistors. Then 3D ring oscillator has been explored which consists of 3 tiers, where each tier consists of 4 or 5 inverters and each tier connected to the next tier vertically by TSV. The frequency and power is measured for schemes and compared to each other to show the impact of TSV coupling.**

Keywords – **3D IC, TSV, Coupling**

I. Introduction

Three-Dimensional IC (3D IC) has attracted much attention as a promising method of improving IC performance. 3D integration can provide higher performance, lower power consumption, decrease the length of global interconnects and increased functionality. 3D IC packages can handle multiple heterogeneous dies such as Logic, Memory, Analog, RF, and Micro-Electrical Mechanical Systems (MEMS) at the various nodes, from 28nm for high speed logic to 180nm for Analog.

3D integrated circuit manufactured by stacking silicon wafers and/or dies and interconnecting them vertically using through-silicon vias (TSVs), these vertical integrations can drastically decrease wire delays and interconnect power. However, vertical integration brings new challenges, such as heat removal, manufacturing costs, and TSVs placement. In TSV-based 3D-IC, signal integrity is becoming one of the major obstacles due to coupling, high frequency loss, and electromagnetic radiation, where thousands of vertical interconnections are routed in a very small 3D space.

Still now many works have been done for TSV coupling. It was proven that TSV introduce several new coupling sources to 3D ICs, which are bad to the circuit's SI (Signal Integrity) performance. Several works have been done to illustrate TSV-to-device coupling, TSV-to-wire coupling, and TSV-to-TSV coupling and etc.[1]. In our work we will concentrate only to TSV-to-TSV coupling deeper; exploring signal, power and ground TSVs; coupling between each of them in an example of 13 stages 3D Ring Oscillator. [1] studied a specific case of TSV-to-TSV coupling considering only horizontal/vertical TSV coupling, but there is also diagonal coupling between TSVs, so we will go deeper and look also at diagonal coupling. [2], [5] show only crosstalk between signal TSVs and [3] shows coupling between signal and ground TSVs. There is still not considered crosstalk between signal and power TSVs.

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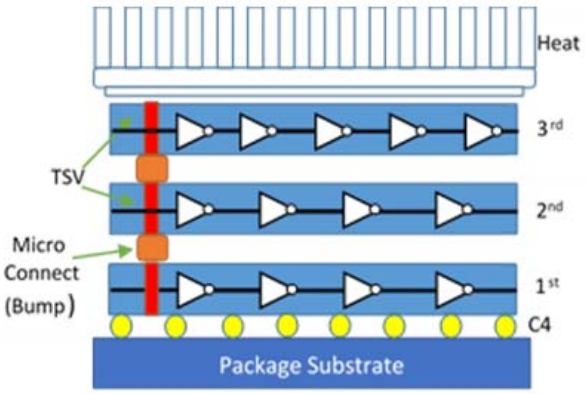

Fig. 1. Illustrative 3D system for 13 stage RO

So we will explore TSV-to-TSV coupling by focusing signal-power, signal-signal, signal-ground TSV coupling and consider both horizontal/vertical and diagonal coupling in one paper.

After evaluating TSV coupling we should find a way to reduce TSV coupling. There are several possible ways to reduce the TSV induced coupling. Shielding by using Power/Ground TSVs [1], Buffer insertion, increase the distance between TSVs [4]. We will go through all of these options and show pros and cons for every mode.

This paper is organized as follows. In Section II 13 stages ring oscillator is presented both for 2D and 3D technologies, in Section III given the TSV electrical model, illustrated RLC parameters of TSV and review TSV coupling model, shows basic formulas for capacitance computation. Details of measurement results are presented in section V. Conclusions are given in Section VI.

II. Ring Oscillator

The single-ended ring oscillator is the digital oscillator, produced by cascade connecting of an odd number n of inverters in a loop. The advantages of using a ring oscillator are: low complexity layout, easily achievable high frequencies, and large tuning range. The main drawbacks of using ring oscillators are poor phase noise performance, and frequency variations with changes in process, power supply voltage and temperature.

The ring oscillator's output frequency is given by:

$$f = \frac{1}{2 * t_{dl} * N}$$

Where t_{dl} is the time-delay for a single Inverter and N is the number of Inverters in the Inverter chain.

The more stages there are, the lower the frequency will be. To increasing the number of inverter stages, a frequency divider further reduces the test structure's output signal frequency. The reduction in frequency is exponentially proportional to the number of dividers in the chain.

In the figure 2 is shown 13 stages ring oscillator. Every stage consists of 45nm CMOS inverter and connect to the next one. It presents itself a simple 2D ring oscillator. For the investigation we first designed and measured 2D ring oscillator in order to compare the measurement with 3D ring oscillator.

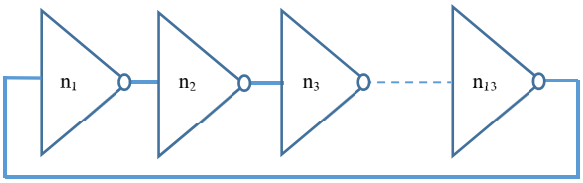

Fig. 2. Ring Oscillator

A 3D ring oscillator is shown in figure 3, it is designed based on the above-mentioned designed 2D ring oscillator. Four cascaded inverters are on the two layers chips, and the top logic chip with five inverters connections. In the first one, TSVs used only for signal interconnections (figure 3a), and in the second TSVs are used also for power and ground nets (figure 3b), which is more in line with reality. TSVs are bring violations of the scheme, such a frequency decreasing, delay increasing, power infractions. Also there are coupling between TSVs. Al these issues are discussed and presented.

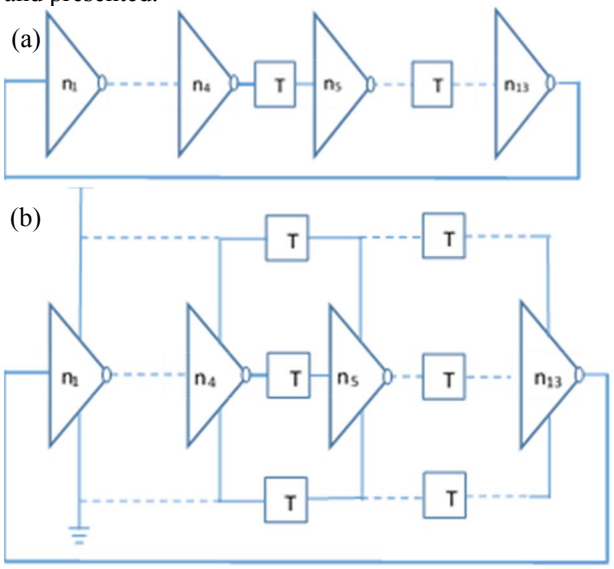

Fig. 3. 3D Ring Oscillator a) TSV used only for signal wires, b) TSV used for power, ground and signal wires

III. Analytical Model of TSV and TSV-to-TSV Coupling

A. Electrical model of TSV

A TSV is a vertical electrical connection passing through a silicon die. TSVs are copper vias with diameters that may range from 1 to 30 microns. The TSV model and the parameters used in our design described in figure 4 [6]. The TSV model corresponds to the π shaped model.

In one side 3D technology provide low power consumption due to the short interconnects but in the other side inserting TSV in design brings new parasitic RLC which causes variation of the scheme.

Beside these during fabrication TSV itself may have some defects and deviation of parameters. Likewise, there are coupling between TSVs. Therefore, we have also considered the variation of Resistance, Capacitance and Inductance of the TSV model. C is splitted in C_{Ox} and C_{Si} to represent oxide and silicon contributions; consequently, G_{Si} is the parasitic conductance due to silicon losses.

For demonstrating variation of R, C and L parameters in the TSV of scheme of Figure 3b R parameter was changed from 20 mΩ to 200 mΩ, C_{ox} was changed from 270 fF to 350 fF and L from 25 pH to 250 pH. Then the dependence of R, C and L from average power and frequency was presented correspondingly.

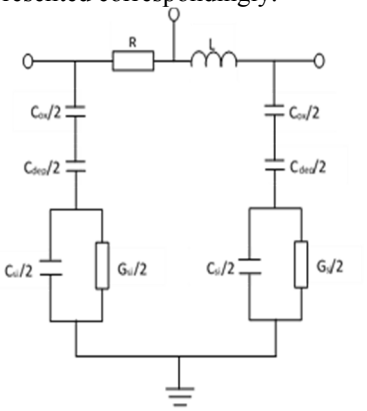

Fig. 4. Electrical model of TSV

B. TSV-to-TSV Coupling

TSV-to-TSV coupling capacitance is affected by TSV-to-TSV distance, TSV dimensions, the number of surrounding TSVs, and their distribution. The TSV coupling capacitance is very big (~10fF) so that it has huge impact on timing and interconnect power. In figure 5 is shown coupling between 2 TSVs, it consists of parallel connected C_{TT} capacitance and R_{TT} resistance. We can simplify this model by removing $R_{TT,}$ the simplified model is shown in figure 6. We also need to consider that in 3D design each TSV is surrounding by several TSVs. So there exist horizontal/vertical and diagonal capacitive coupling.

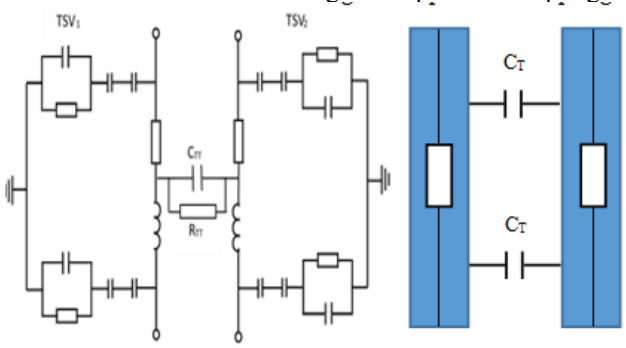

Fig. 5. Coupling between 2 TSVs and Simplified RC model

Thus, to compute capacitive coupling between two adjacent TSVs, we need to discuss two components. The first component is the coupling capacitance between the sidewalls of the TSVs (C_{c1}), and the second component is the coupling capacitance between the corners of the TSVs (C_{c2}). Hence, total C_{TT} is computing as follows:

$$C_{TT} = 4(C_{C1} + C_{c2})$$

IV. Simulations and Measurements

In this section the analysis results are presented for ring oscillator. At first the 2D 13 stages ring oscillator was designed and presented delay time, rise and fall time, power, frequency and duty cycle. For further exploration the same parameters are calculated for 3D ring oscillator. In this section are shown that by TSV infusion we can both reduce the power of interconnect and improve overall performance and the most important considering coupling of TSV. At first we calculated all parameters for the scheme showed in figure 2a, and consider capacitive coupling between signal TSV. We have choose the value of C_{TT} very small (approximately 1fF) and gradually grow it using sweep operation in HSpice simulation. To see the coupling between signal TSV and power TSV, also signal TSV and ground TSV the scheme in figure 2b is used. In this case the problem is more complicated because we need to discuss 3 cases of TSV coupling also calculate both vertical/horizontal and diagonal coupling.

As mentioned previously we first explore 2D 13 Ring Oscillator to be able to compare the variation of the performance thus of 3D RO. 2D RO has the following performance: the frequency of Oscillation is 3 GHz, value of the power supply is set to 1.0V, the average power consumption of scheme is 184uWt, gate delay and duty cycle correspondingly equal to 0.33ns and 50%. After converting the RO to 3D RO, which has a 3 tier and every tier has 4 inverters (1st and 2nd tiers consist of 4 inverters and 3rd tier of 5 inverters). The performances of this circuit is shown in table 1.

Table 1. 3D Ring Oscillator Performance

Power consumption	122uWt
Oscillation frequency	0.92GHz
Delay	0.42ns
Duty Cycle	50%

The simulation results show that 3D integration is reformed power performance, while frequency and timing suffered. The frequency is decreased by 30% and the timing is deteriorating by 21.42%. For further survey we have consider capacitance coupling between TSVs. First let us introduce the coupling between two adjacent TSVs. The Coupling capacitance C_{TT} is set to 1fF and regularly increased to 20fF by sweep operation of HSpice simulator. The power and frequency throughput is shown in figure 6.

As we can see from the charts the impact of crosstalk to the power consumption not so substantial it is flapped between 118uWt to 123uWt. However, the crosstalk has a big impact to the oscillation frequency, the greater capacitance the lower frequency.

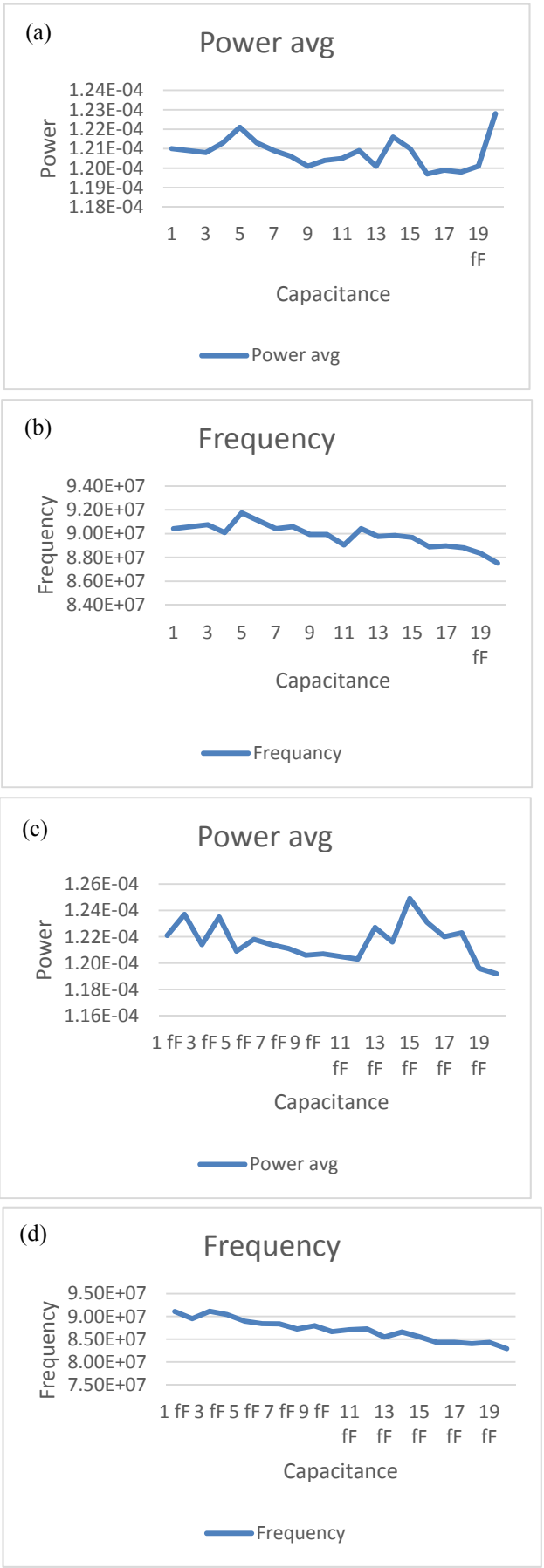

Fig. 6. Average power consumption (a) and frequency (b) for crosstalk; average power consumption (c) and frequency (d) for VDD noise

Further is discussed coupling between signal TSV and TSV in the power supply net (VDD). In this case the VDD has constant value 1.0V and it cause the frustration to the signal net, so the power TSV acted as an aggressor and the signal TSV as a victim, and noise was discussed caused by the power. After power and frequency analysis for every mode are shown the measurement results of Voltage drop correspondingly for ground net and supply net. It is obvious that TSV coupling also caused voltage drop in supply net, so we have presented the impact of coupling in power and ground nets to see which type of coupling is more emphatic for performance.

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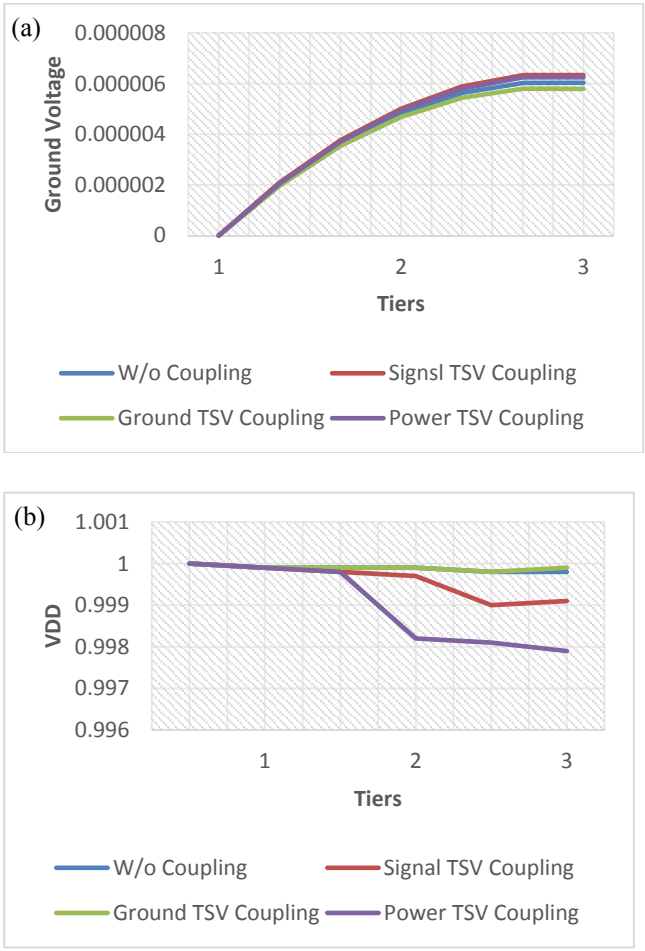

Fig. 7. a) Ground voltage degradation, b) Supply voltage degradation

V. Conclusion

This work investigated TSV coupling under high speed operation of a 3D Ring Oscillator and using a SPICE simulator. Both the analyzed results, and the measured results show that the effect of TSVs dominates the delay of 3D Ring oscillator, and the proposed 3D Ring oscillator is an attractive and promising candidate for the stacked 3D IC testing.

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Analysis of the Impact of CNTFET Model Parameters on its Transfer and Output Characteristics

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Abstract – **The influence of internal parameters on transfer and output characteristics of a Carbon Nanotube Field Effect Transistor are studied in this paper. For the purposes of the study a CNTFET compact model is used. The compact CNTFET model is coded in Verilog-A and it is simulated in Cadence Spectre circuit simulator. In particular, we have examined how the transfer and output characteristics are altering when changing single parameters or sets of parameters. To compare the simulations results a cost function consisting of the two parameters is employed to quantify the impact of 430 model parameters. The sum of total 430 model parameters are examined and 59 are found to have negligible or no impact on output static characteristics. Three groups of internal model parameters have been recognized, according to their impact on output static characteristics.**

Keywords – **Carbon nanotube, CNTFET, modeling, Verilog-A, Cadence**

I. INTRODUCTION

Research in the field of a carbon nanotube (CNT) device shows that they are good alternative for replacement of the classical MOSFET transistor in some applications. The operating principle and structure of CN devices are similar to conventional MOSFET transistors, in addition some of the manufacturing processes are identical.

In order to enable component design, a couple the CN behavioural models based on MOSFET are created. Four models have been developed: HEMT model [1], Schotky barrier Carbon nanotube field effect transistor (SB-CNTFET) [2] and transistor with single well CN with ability to create channel using three parallel nanotubes. The model was published in 2008 and since then is constantly updated with addition or correction of different functions [3]. The latest version of the carbon nanotube FET is Virtual source MOSFET (VS-CNFET) developed by the same team [4], [5]. The distinction between single well CN FET model and VS-CNTFET is the different description of the carriers in the channel. Leading team working in the field of development and modelling of Carbon nanotube field effect transistors are the Stanford university [6], [7]. This enables new component design and evaluation and their behaviour in the electrical circuits and systems.

The purpose of developing a CNTFET model is to be implemented in all the circuit simulators and used in industry. CNTFET contains descriptions of important size and process parameters such as channel length and width, gate oxide, etc. First level is decription of intrinsic channel region. Second level describes the parasitic capacitance and resistance between the source and drain regions and Carbon nanotube. The third level describes the possibility to change to three the number of the carbon nanotube parallel combinations. The CNTFET model is implemented in Cadence Virtuoso libraries and it is ready to be used in the Vurtuoso Spectre simulator. Thus enabling the use of the CNTFET model in design of circuits and systems.

The single well CNTFET compact model is a physical model containing a large number of parameters. The model consist of three layers. Layer 1 describes the intrinsic behaviour of MOSFET-like CNFET. Layer 2 incorporates the device nonidealities: the capacitance and resistance of the source and drain CNT regions. Layer 3 models the interface between the CNFET transistor and the CNFET circuits. The model consists of 492 parameters for level L1. These parameters related to the technology, the geometry and physical constants are 62. The internal parameters of the model are 430. Due to the specificity of the CNTFET compact model [6] parameters, loops and arrays are not used. The parameters are vectorised and summarized.

The number and the type of descriptions of the parameters do not influence the performance of the simulator e.g. increase the simulation time. However, the large number of variables, impact the extraction of the parameters, thus making the complex procedure increasingly difficult.

This paper investigates influence of all the 430 internal CNTFET model parameters, in order to find parameters with negligible impact. In addition, the it is presented the influence of the combination between three parameters. The impact of parameters on the transistor output and transfer characteristics is considered, enabling to rejection of the non-significant parameters. The results of the analysis are used as a procedure to simplify the parameter extraction.

II. PARAMETERS IMPACT ON I-V CHARACTERISTICS

The CNTFET Stanford compact model is described using Verilog-A and it is for HSPICE. After a modification, the model is implemented in Cadence. The CNTFET model is

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verified using literature references data [7]. According to the literature, $V_G = 0.9$ V, $V_D = 0.9$ V, the drain current is around 0.42 µA. The CNTFET channel is created with single-wall Carbon nanotube.

The model is valid for a wide range of chirality values and carbon nanotube diameter. The parameters influence on the *I-V* characteristics is important part of the research related to the model development. This article studies the influence of all internal 430 parameters. The influence of parameters is heightened in change of the output static *I-V* curves of the Carbon nanotube. Comparison between *I-V* curves of the CNTFET transistor with all parameters and *I-V* curves with reduces parameters. The results are obtained through the following procedure:

- Conducting a simulation in Cadence Spectre simulator;
- Exporting the simulation results in text file;
- Manipulating the data and calculating the errors in Matlab;

Matlab code is developed to compare the results of simulations, when one or combinations of some parameters are removed.

The parameter influence is quantified using graphical and numerical approaches. The static output behaviour of single well CNTFET transistor is described as,

$$I_D = f(V_{DS}), V_{GS} = 0.9\,V \quad (1)$$

where I_D is a drain current, V_{DS} is a voltage applied between drain and source terminals and V_{GS} is a gate voltage.

Figure 1 shows comparison between static output characteristic of CNTFET complete model and CNTFET model with reduced parameter *Qs_sub15*. Reducing the parameter *Qs_sub15* does not influenced the output static behaviour of the transistor and the two *I-V* curves show no difference. It is worth mentioning that not all model parameters have influence over the output static characteristics (DC simulations) e.g. small-signal parameters do not impact static *I-V* curves, but they do impact transient behavior.

Figure 2 shows comparison between output characteristics of CNTFET complete model and CNTFET model without parameter *Charge_sub10*. Reducing parameter *Charge_sub10* results in an increased drain current at same drain/source voltage. It is worth noticing that behaviour of the drain current change. When V_{DS} is between 0 and 200 mV, I_D of complete model is greater than I_D of the reduced model. After V_{DS} becomes greater

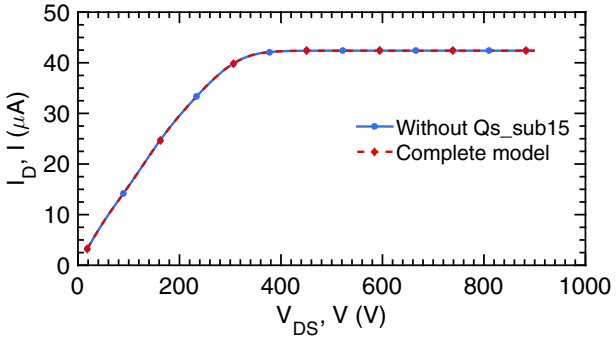

Fig. 1. Comparison between CNTFET complete model and reduced model without *Qs_sub15* parameter

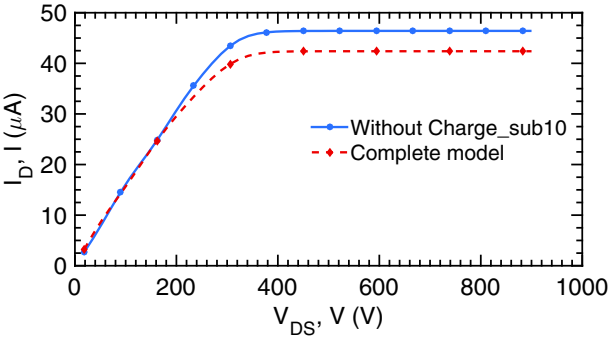

Fig. 2. Comparison between CNTFET complete model and reduced model without *Charge_sub10* parameter

than 200 mV, I_D of the reduced model becomes greater then I_D of the complete model.

Graphical approach is visual and the results are easy to interpret. However, due to high amount of parameters it is not convenient to visualization. Moreover, graphical approach is not suitable for quantification and precise comparison. Therefore, numerical methods are applied for a better understanding of the results and reducing the number of parameters with minimal cost of performance.

III. Cost Function of the Reduced Model

The ideal quantitative metric should provide insights of the two domains of model evaluation i.e. model performance measure and error distribution. A single metric delivers only single domain of model interpretation and, therefore, only underlines a certain aspect of the error characteristics. In order to battle this problem a combination of metrics is applied. First, area under curve between complete and reduced model is calculated. It represents the area similarity between two models, however it does not take into account discrepancies in instantaneous I_D. Therefore, second measure applied is root mean square error. It represents the difference in the dynamic of the signal. The cost function to be minimized is that both these metrics must be minimal in an optimal estimate, by adjusting model parameters.

Area under curve (AUC) for the complete model is given by,

$$A_C = \int_{0\,mV}^{900\,mV} I_D dV_{DS} \quad (2)$$

where A_C denotes the area for the complete model. A_C is calculated be performing numerical integration via the first degree closed Newton-Cotes formulae i.e. trapezoid rule, given by,

$$A = \int_1^N f(x)dx \approx \frac{b-a}{2N} \sum_{k=1}^{N} (f(x_k) - f(x_{k-1})) \quad (3)$$

where *f(x)* represents I_D discretized in 50 values of V_{DS}. The illustration of trapezoidal rule for numerical integration is shown on figure 3. Then the relative error δ between two functions *f(x)*, which represents complete model, and *g(x)*, which represents reduced model is given by,

$$\delta = \frac{A_R - A_C}{A_C} . 100\% \quad (4)$$

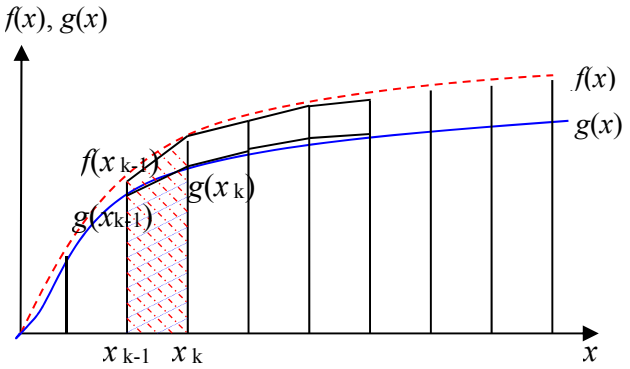

Fig. 3. Illustration of trapezoidal rule for numerical integration

where A_R is AUC of the reduced model and A_C is AUC of the complete model.

The second metric of the cost functions is the root mean square error, given by,

$$RMSE = \sqrt{\frac{\sum_{k=1}^{N}(f(x_k)-g(x_k))^2}{k}} \quad (5)$$

The optimization cost function has a two objective functions i.e. δ and RMSE and the input parameters are all internal 430 model parameters. The cost function is given by,

$$\arg\min \delta, RMSE, \text{subject to: } P_n, \text{n} \in [1,430] \quad (6)$$

Table 1. Internal parameters errors

Parameters	Direction	AUC δ, %	RMSE
Charge_sub10	↑	8.30	3.40 µA
Charge_sub29	--	0	0
ld_op10	--	0	0
ld_op25	--	0	0
c_vds_sub10	--	0	0
c_vds_sub29	--	0	0
trans_c_sub10	--	0	0
trans_c_sub29	--	0	0
current_sub11	↓	-16.81	6.79 µA
current_sub29	--	0	0
T11_0	↑	5.49	3.71 µA
T29_0	--	0	0
l_op11_0	Group 2		
l_op29_0	Group 2		
fermi_op11_0	--	0	0
fermi_op19_0	--	0	0
T11	Group 2		
T29	Group 2		
l_op11	Group 2		
l_op29	Group 2		
fermi_op11	--	0	0
fermi_op29	--	0	0
FDOS11	Group 2		
FDOS29	Group 2		
fermi_d11	↑↓	5.49	3.71 µA
fermi_d29	--	0	
fermi_s11	↑↓	-22.31	8.07 µA
fermi_29	Group 2		
Coeff_J11	Group 2		
Coeff_J29	Group 2		

where Pn is the parameter in the model. Minimum error in both metrics is required to ensure minimum influence of the reducing parameter.

Table 1 shows the influence of internal parameters. Based on cost functions of all 430 internal parameters, they could be classified in three major groups. The first group includes all parameters that do not any impact on the characteristics. These parameters do not impact dynamic [8] and static output characteristics. Here is the list of dropped parameters (59 in total) that describe optical phonons scattering and some gate to source/drain/sub capacitances: *fermi_op21_0 – fermi_op29_0*, *Qs_sub10 – Qs_sub15*, *Qs_sub20 – Qs_sub25*, *fermi_op10 – fermi_op15*, *fermi_op20 – fermi_op25*, *Rd_op10 – Rd_op15*, *Rd_op20 – Rd_op25*, *Qop_10 – Qop_15*, *Qop_20 – Qop_25*, *Qop_sub_1 and Qop_sub_2*.

Figures 4, 5, 6 and 7 show the *I-V* curves with parameters with biggest cost function results. It worth mentioning that any single metric is not able to capture the intricacies in changing the behavior.

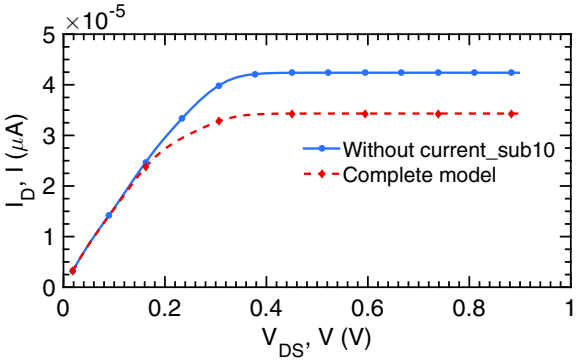

Fig. 4. Comparison between CNTFET complete model and reduced model without *current_sub10* parameter

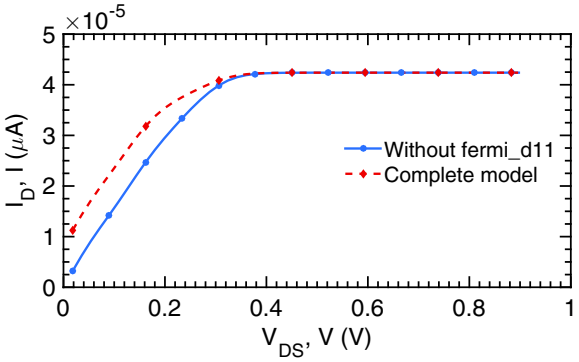

Fig. 5. Comparison between CNTFET complete model and reduced model without *fermi_d11* parameter

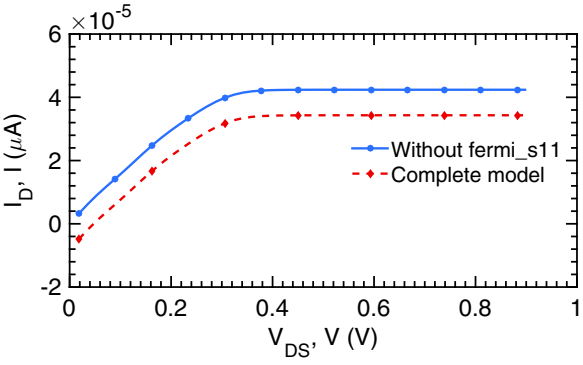

Fig. 6. Comparison between CNTFET complete model and reduced model without *fermi_d11* parameter

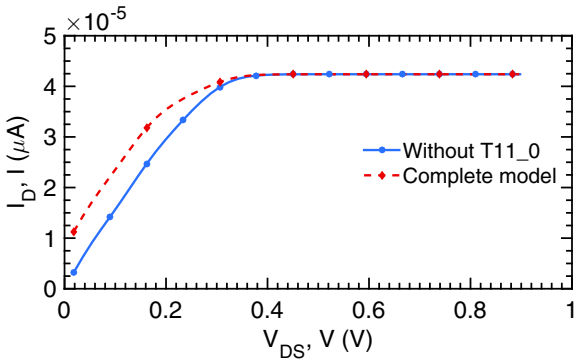

Fig. 4. Comparison between CNTFET complete model and reduced model without *fermi_d11* parameter

We have adopted the following standard to assess the parameters impact – if the parameter does not have cost function greater than {0.025%, 1.0 μA}, the influence of the parameter is accepted as unimportant and it is reduced from the model. All simulations are conducted using identical set of geometry and technology parameters. The value of each internal model parameter is nulled. In result we have obtained a simplified model applicable to memory circuits.

Using the described approach, the first group of parameters are reduced from the model. The third group are parameters which have a high value cost function i.e. impact on the output characteristics and they are not suitable for reduction from the CNTFET model. Group 1 parameters consist of 59 parameters and the reduction of the number of parameters, therefore leads to easier procedure of parameters extraction.

In order to verify the behaviour of the model with reduced internal parameters, it was designed a dynamic random-access memory (DRAM) [8]. DRAM storage cell was designed with the CNFET reduced model. To prove the effectiveness of the simplified model, we implement in Cadence Spectre circuit simulator both simplified and Stanford CNTFET compact models in a 16-bit 1T-DRAM in Verilog–A code. AMS 0.35 μm technology design kit is used. The results are published in [8] and simulations of write and read operations gave almost equal results. In the present we used additional mathematical technique (namely, we applied the cost function) to evaluate the significanece of paramters in static output *I-V* characteristics. This shows the applicability of the simplified CNTFET model to memory circuits.

IV. Conclusion

This paper presents a methodology to study the impact of CNTFET internal parameters on transfer and output characteristics. The model was developed in Stanford and it is codded in Verilog-A and simulation results are obtained via Cadence Spectre circuit simulator.

To compare the results of simulations the cost function consisting of two metrics was proposed. Internal parameters are classified in three major groups. The first group has a negligible impact on the output characteristics. The second group are impossible to be reduced due to their influence on CNFET tranconductance or because they are foundational parameters. The third group has a higher cost function and they have a significant impact on output characteristics. The results show that group one, consisting of 59 parameters has no almost no impact on the output *I-V* characteristics and they could be reduced.

In conclusion it was composed a reduced model without group of 59 internal parameters, that it could be used in studying in DC simulation of static output characteristics CNTFETs.

Acknowledgement

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Investigation of Power Losses in Synchronous Buck DC-DC Converter with Zero Voltage Switching

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Abstract – **In this paper a synchronous buck dc-dc converter with Zero Voltage Switching (ZVS) for low power applications is presented and investigated in Cadence with a CMOS 0.35 μm technology. Power losses in the converter's components are evaluated and analyzed. The results obtained show that the efficiency of the standard switching-mode buck dc-dc converter can be increased by about 3.6 % if ZVS technique is used.**

Keywords – **Power losses, synchronous buck dc-dc converter, zero voltage switching, Cadence.**

I. Introduction

Switching-mode dc-dc converters are part of envelope amplifiers, which are used to deliver the desired energy to the transmitter's power amplifier (PA) in modern battery powered wireless communication devices [1]. The last generation mobile phones have great functionality, because the signal spectrum is used very effectively [2]. The reason is that orthogonal frequency division multiplexing (OFDM) modulation is performed. The information is transferred using several sub-carrier frequencies. The output signal has big variation of the amplitude. Therefore, in order to prevent distortion of the transmitted information, the power amplifier should be linear. The disadvantage of linear PAs is that those circuits have low efficiency performance.

One of the problems of modern smart phones is that battery has to be recharged more often. The battery energy can be saved if efficiency of envelope amplifier is increased. The function of envelope amplifiers is to supply dynamically changeable voltage to drain or collector of PA's RF transistor as a function of envelope signal [3]. The switching-mode buck dc-dc converters are usually used when low frequency and dc voltages have to be delivered to PAs. The rest of the power is supplied by fast tracking speed linear amplifiers. Both linear amplifier and switching-mode converter stages can operate in different hybrid envelope amplifier architectures [2].

Switching-mode converters ensured almost 80% of overall transmitter's PA energy [3]. The efficiency of envelope amplifier is calculated by:

$$\eta_{EA} = \frac{P_{out(av)}}{P_{in(av)}}, \tag{1}$$

where η_{EA} – efficiency of the envelope amplifier, $P_{out(av)}$ – average output power, $P_{in(av)}$ is the average input power.

The power losses in the MOS transistors of synchronous buck dc-dc converter are discussed in Section II *A*. In Section II *B* power losses in the low-pass filter of the converter are considered. The effect of zero voltage switching (ZVS) technique on the switching power losses in the main PMOS transistors is described in Section II *C*. Investigation results of power losses and efficiency of the buck dc-dc converter with ZVS are presented in Section III.

II. Power Losses in the Switching-Mode Buck DC-DC Converter

A. Power losses in the MOS transistors of buck dc-dc converter

The schematic of synchronous buck dc-dc converter is shown in Fig. 1.

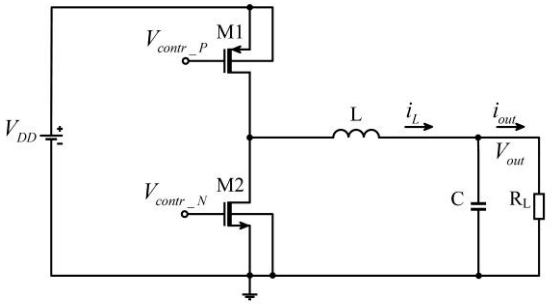

Fig. 1. Synchronous buck dc-dc converter.

The efficiency of the whole buck converter system can be expressed by:

$$\eta = \frac{P_{out}}{P_{out} + P_{losses}}, \tag{2}$$

where P_{out} is the output power of the dc-dc converter; P_{losses} are total power losses in the dc-dc buck converter. Most of the power losses in the converter are indicated in the output MOS transistors *M1* and *M2*. Those losses can be divided into conduction and switching power losses [4]:

$$P_{loss,MOS} = P_{sw} + P_{cond}. \tag{3}$$

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On the other hand, the switching power losses in the output MOS transistors *M1* and *M2* are equal to [2]:

$$P_{sw} = f_s . C_{tot} . V_{DD}^2, \quad (4)$$

where C_{tot} is the output total capacitance of the MOS transistors, f_s is the switching frequency of the buck converter, V_{DD} is the power supply. The conduction losses can be calculated by [4]:

$$P_{cond} = I_{source}^2 . r_{on,p} + I_{sink}^2 . r_{on,n}, \quad (5)$$

where I_{source} and I_{sink} are the sourcing and sinking current of the MOS transistor respectively, while $r_{on,p}$ and $r_{on,n}$ are the on-resistances of PMOS and NMOS transistors.

B. Power losses in the low-pass filter of buck dc-dc converter

The other distributor of losses in the buck dc-dc converter is the filter inductor *L*. The total power dissipated in filter inductor, assuming that the inductor parasitic impedance scale linearly with the inductance [5], is equal to:

$$P_{ind} = b\left[\frac{I^2}{\Delta i_L f_s} + \frac{\Delta i_L}{3 f_s} + \frac{C_{L0} V_{DD}^2}{R_{L0} \Delta i_L}\right], \quad (6)$$

where *b* is a coefficient depending from the parasitic capacitance and parasitic series resistance of the filter inductor, C_{L0} and R_{L0} are respectively the parasitic stray capacitance and parasitic series resistance per 1 nH inductance, Δi_L is the inductor current ripple.

The other source of the power losses in the switching-mode buck dc-dc is filter capacitor *C*. They are obtained due to the effective series resistance of the capacitance R_C. If monolithic capacitor is implemented utilizing the gate oxide capacitance of a MOSFET transistor, the total power dissipation of filter capacitor [5] is equal to:

$$P_{cap} = d \Psi f_s \Psi \Delta i_L, \quad (7)$$

where *d* is a coefficient depending on technology, effective series resistance of the filter capacitor for MOSFET transistor with channel width of 1 μm, gate oxide capacitance, channel length of the MOSFET transistor.

C. Zero Voltage Switching

The circuit of synchronous single phase switching-mode buck dc-dc converter with ZVS is shown in Fig. 2. The advantage of those type of circuits is that the main power transistor *M1* can be switched on and off respectively at zero voltage [6].

The zero voltage switch-off of the main PMOS transistor *M1* of dc-dc converter is because of the capacitor C_r. The Zero voltage switching-on state of the PMOS transistor *M1* is ensured by the diode D_r.

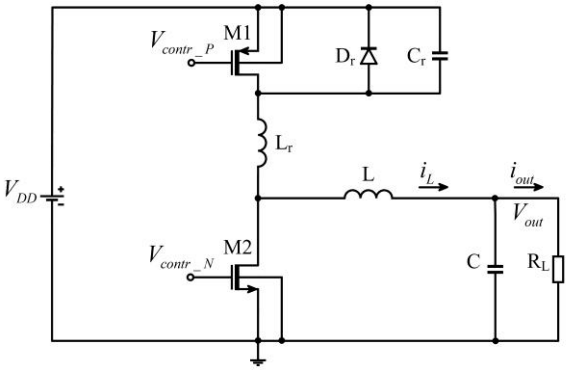

Fig. 2. Synchronous buck dc-dc converter with ZVS.

The function of this component is to clamp to zero capacitor voltage V_c, when transistor *M1* is at switch-off state [6]. The effect of ZVS will leads to zero switching power losses of main PMOS transistor *M1*. Thus the total power losses in the MOS transistors of synchronous dc-dc converter could be decreased. They are equal to [5]:

$$P_{tot,MOS} = a\sqrt{\left(I^2 + \frac{\Delta i_L^2}{3}\right) f_s}, \quad (8)$$

where Δi_L is the inductor current ripple, *I* is a dc current supplied to the load, and *a* is a coefficient depending on the equivalent series resistance of the transistors, the input total capacitance of the MOS transistors C_{tot}, and the power supply V_{DD}.

III. INVESTIGATION OF POWER LOSSES AND EFFICIENCY OF BUCK CONVERTER WITH ZVS

Synchronous buck dc-dc converter with Zero Voltage Switching is investigated in Cadence with a CMOS 0.35 μm technology.

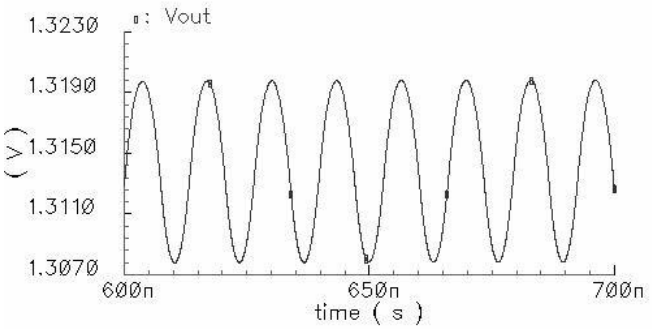

Fig. 3. The output voltage V_{out} of buck dc-dc converter with ZVS.

The supply voltage V_{DD} is chosen to be equal to 3.6 V, which is the standard output voltage of lithium-ion batteries. The main power PMOS transistor *M*1 is formed by four "*modprf*" transistors connected in parallel. Their sizes (W/L) respectively are equal to 150/0.35 μm. The NMOS transistor *M*2, which replaces the diode in the standard buck dc-dc converter circuit, is formed by two "*modnrf*" transistors connected in parallel. Their sizes

(W/L) respectively are equal to 150/0.35 μm. The mode of operation of transistors *M1* and *M2* is regulated by two pulse generators V_{contr_P} and V_{contr_N} , respectively. The value of the filter inductor of the investigated circuit is equal to 300 nH. The filter capacitor is equal to 5 nF. The value of resonant inductors L_r is equal to 30 nH, while resonant capacitor C_r is equal to 5 pF. The switching frequency *fs* of the investigated buck dc-dc converter with ZVS is equal to 76 MHz.

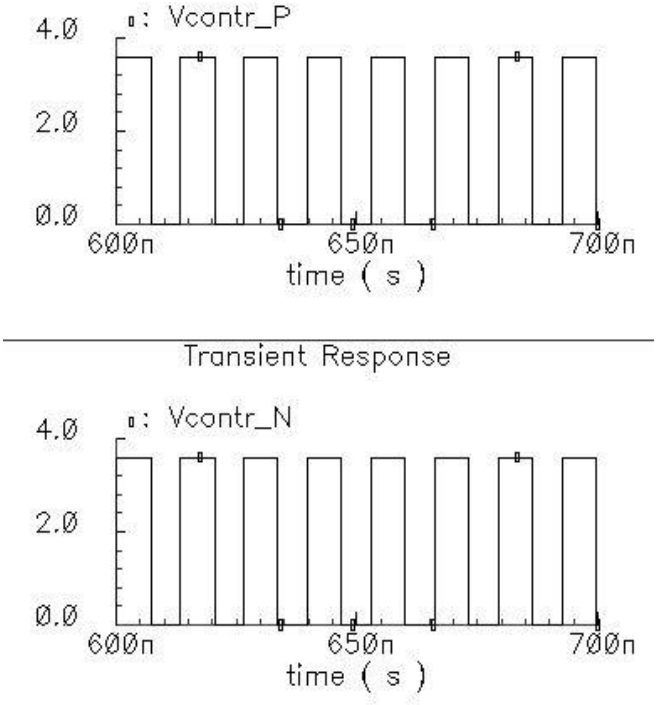

Fig. 4. The waveforms of V_{contr_P} and V_{contr_N}.

The average value of output voltage $V_{out(av)}$of buck dc-dc converter with ZVS is regulated to be equal to 1.3 V. The waveform of output voltage V_{out} is shown in Fig. 3. The waveforms of control pulses V_{contr_P} and V_{contr_N}, which regulate respectively transistors *M*1 and *M*2, are shown in Fig. 4.

TABLE 1. POWER LOSSES IN FILTER INDUCTOR *L* AND FILTER CAPACITOR *C* OF DC-DC CONVERTER WITH ZVS AS A FUNCTION OF THE LOAD R_L

	R_L=10 [Ω]	R_L=15 [Ω]	R_L=20 [Ω]	R_L=30 [Ω]	R_L=48 [Ω]
P_{out} [mW]	116.9	112.65	84.5	56.3	35.2
P_{ind} [mW]	3.4	3.1	2.8	2.1	1.9
P_{cap} [mW]	0.24	0.21	0.19	0.11	0.06

The power losses in filter inductor *L* and filter capacitor *C* of the buck dc-dc converter with ZVS are investigated. The average value of output voltage $V_{out(av)}$ is equal to 1.3 V. The results are shown in Table 1. The waveform of control signal V_{contr_P}, which determine the mode operation of PMOS transistor *M*1, and voltage and the capacitor's voltage V_{Cr} are shown in Fig. 5. As can be seen from the picture, the PMOS transistor is switching on at zero voltage, while *M*1 is switching-off at voltage higher than zero. The reason is the fact that *M*1 is non-ideal switch.

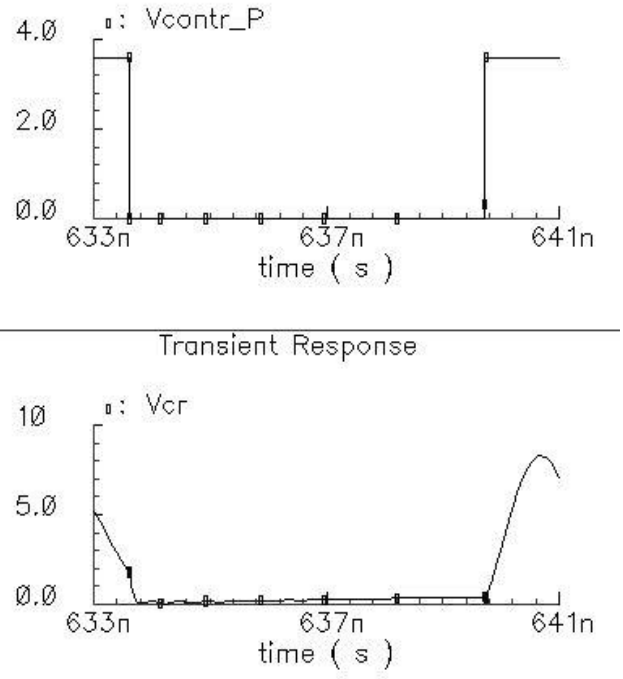

Fig.5. The waveforms of V_{contr_P} the capacitor's voltage V_{Cr} .

The total power losses in PMOS and NMOS transistors and the efficiency of the buck dc-dc converter with ZVS as a function of the load R_L are investigated. The results are shown in Table 2. The results presented in Table 1 and Table 2 show that power losses in the MOS transistors dominate in buck dc-dc converter.

TABLE 2. POWER LOSSES IN PMOS AND NMOS TRANSISTORS AND EFFICIENCY OF DC-DC CONVERTER WITH ZVS AS A FUNCTION OF THE LOAD R_L

	R_L=10 [Ω]	R_L=15 [Ω]	R_L=20 [Ω]	R_L=30 [Ω]	R_L=48 [Ω]
P_{out} [mW]	116.9	112.65	84.5	56.3	35.2
P_{NMOS} [mW]	22.5	21.7	16.3	10.9	6.87
P_{PMOS} [mW]	14.2	13.63	10.25	6.84	4.56
Eff. [%]	69.95	71.15	75.43	80.15	82.68

In Table 3 the total power losses in PMOS and NMOS transistors and efficiency of standard synchronous buck dc-dc converter without ZVS as a function of the load R_L are presented. The average value of the output voltage $V_{out(av)}$ is equal to 1.3 V.

TABLE 3. POWER LOSSES IN PMOS AND NMOS TRANSISTORS AND EFFICIENCY OF DC-DC CONVERTER AS A FUNCTION OF THE LOAD R_L

	R_L=10 [Ω]	R_L=15 [Ω]	R_L=20 [Ω]	R_L=30 [Ω]	R_L=48 [Ω]
P_{out} [mW]	116.9	112.65	84.5	56.3	35.2
P_{NMOS} [mW]	23.4	22.7	16.7	11.5	7
P_{PMOS} [mW]	17.8	16.3	13.6	9.5	8.3
Eff. [%]	67.6	69.7	73.5	78.6	79.8

Power losses in the main PMOS transistor *M*1 as a function of the load R_L are graphically presented in Fig. 6, respectively when buck dc-dc converter work with and without ZVS.

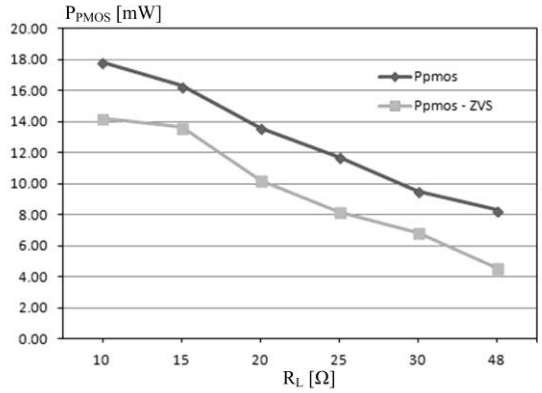

Fig. 6. The power losses in NMOS transistor *M1*, when buck dc-dc converter work with and without ZVS.

Power losses in NMOS transistor *M*2 as a function of the load R_L are graphically presented in Fig. 7, respectively when buck dc-dc converter work with and without ZVS.

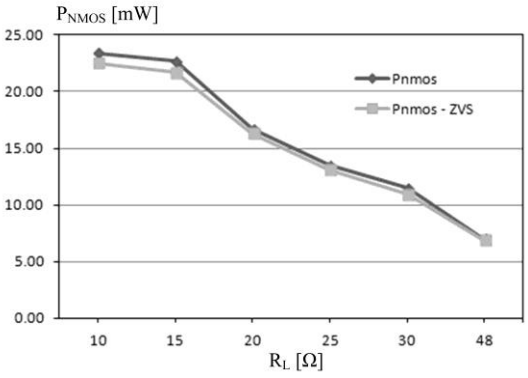

Fig. 7. The power losses in NMOS transistor *M2*, when buck dc-dc converter work with and without ZVS.

The efficiencies of investigated buck dc-dc converter are presented graphically in Fig. 8, when circuit works with and without ZVS. The results presented in Fig. 6 and Fig. 7 show that ZVS leads to decreasing of total power losses in the main PMOS transistor *M*1 of synchronous buck dc-dc converter. This effect helps to increasing of converter's efficiency when ZVS technique is used. The investigations in this paper show that if buck dc-dc converter with ZVS is used as switching-mode converter in the envelope amplifier's hybrid architectures, battery energy of portable electronic devices could be saved. The received results indicate that efficiency of buck dc-dc converter is improved by approximately 1.9% to 3.6%, when the load R_L changes from 10 Ω to 48 Ω.

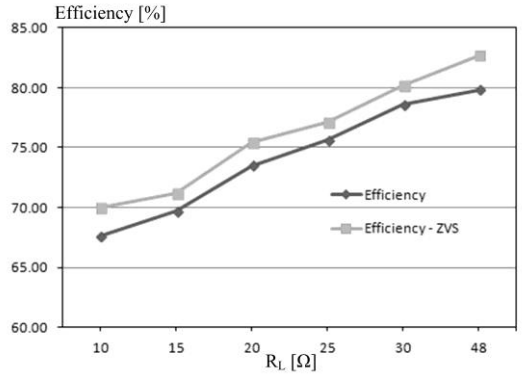

Fig. 8. Efficiency as a function of the load R_L with and without ZVS.

IV. CONCLUSION

A synchronous buck dc-dc converter with Zero Voltage Switching for low power applications has been proposed. Power losses in the converter's components have been investigated and analyzed in Cadence with a CMOS 0.35 μm technology. Battery energy of portable wireless communication devices could be saved if the buck dc-dc converter with ZVS is used as switching-mode converter in the envelope amplifier's hybrid architectures. The results obtained show that the efficiency of the standard switching-mode buck dc-dc converter can be increased by approximately 3.6 % if the ZVS technique is implemented.

ACKNOWLEDGEMENT

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High Precision RC-Oscillator Using R-2R Ladder for Digital Calibration

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Abstract – **This paper presents a fully integrated RC-type relaxation oscillator with high precision over supply, temperature and process calibration by trimming, achieving 50ppm/ºC maximum temperature coefficient and 1% final accuracy in the operating range. The low sensitivity to 1.8V supply is achieved by ratio metric technique and generating supply proportional voltage reference and current source. The small size trimming step of 0.3% and high step linearity is achieved by current source, which use 9 bit R-2R ladder network. The circuit is manufactured at 180nm technology.**

Keywords – **RC-oscillator, R-2R ladder, programmable current source**

I. INTRODUCTION

The precise clock references have wide application range in SoC: communication interfaces, sensor interface circuits, microcontrollers, etc. The circuit parameters have to be stable and with small variation over process, voltage and temperature (PVT), with product parameters calibration for minimum test time. The test time is related to the number of temperature calibration points. Therefore circuits with very low temperature variation by design and single temperature calibration point are preferred. A low time consuming calibration of the process parameters can be created easier, if calibration function is monotonous. The requirements for high precision clock references, together with market pressure for low cost, low components count and low current consumption, drive research and development to look for new solutions, to combine known circuit structures and optimize the existing designs.

II. THE RC-OSCILLATOR DESIGN

A. The RC oscillator architecture and sub-blocks targets

The main targets of this oscillator is nominal operating frequency of about 500kHz typical, a square wave output, fully integrated, with high precision of ±2.5% over process, voltage and temperature (PVT). Due to specific application requirements, the output frequency shall be programmable in ±15% around nominal frequency range with maximum ±0.5% step. The temperature range is automotive (-50ºC to 160ºC), and the supply range is 1.8V ±5%.

The selected structure contains a relaxation oscillator, suitable to produce hundreds of kHz to a few tens of MHz [1] square clock generation. The relaxation oscillator core is presented at Fig.1. It contains two capacitors, two identical current sources and comparators, RS latch on the output, current reference and voltage reference.

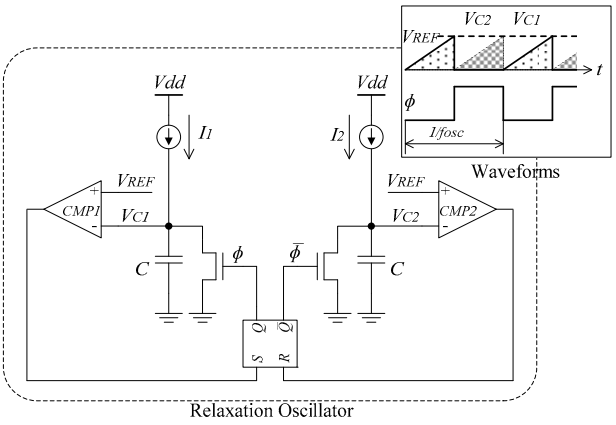

Fig.1: Block diagram of the RC-oscillator.

The oscillating frequency is defined by time constants of charging the two capacitors by constant current I1 and I2, till reaching the threshold level of V_{REF}, and delay *td* of comparators and reset logic. The separate capacitors structure allows discharge time not to be included in total period. Assuming that both branches of the comparators, capacitors, and current sources are identical, the clock frequency can be presented as:

$$1/fosc = Tosc = 2\left(\frac{CV_{REF}}{I_{REF}} + td\right) \qquad (1)$$

As the ASIC, where this oscillator is included, is offering regulated 1.8V internal supply, the reference voltage V_{REF} is designed to be a fraction of this 1.8V supply. It is used a simple resistor divider of 2, with filtering capacitor to suppress supply noise above some level, as well to eliminate the kick-back noise from comparators. The same reference voltage V_{REF} is used also in the current source generator. The V_{REF} is applied at resistor with resistance *R*, to form $I_{REF}=V_{REF}/R$. Substituting in (1) I_{REF} by V_{REF}/R, it can be seen that frequency is now barely dependent on supply and reference voltage.

$$1/fosc = Tosc = 2(RC + td) \qquad (2)$$

There is still dependency from supply related to:

- Limited output resistance of current sources, used to charge the capacitors;
- Delay of comparators and invertors;
- Voltage dependency of resistors.

The target error, related to the supply variation is assumed to be below 0.5%. The respective design techniques that can be used are:

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- Current sources with cascodes for increasing output resistance;
- Comparators with delay *td*<1%Tosc. The assumption here is that only part of the comparator delay time is supply dependent.

The process variation in this technology for resistors is about ±15%, for capacitors ±15%, and assuming ±10% for mismatch, and layout parasitic compensation, it totals ±40%. Due to application specific requirements another ±15% were added, which results trimming range of ±55%. To cover the trimming range and meet the trimming resolution of 0.5% or less, an 8bit DAC is needed.

Regarding the temperature variation, in the used technology are offered very low temperature dependent resistors and capacitors, with temperature coefficients of ±30ppm/ºC, giving about ±1% deviation for the temperature range, which eliminates the need of special temperature compensation related to RC constant. Still has to be considered the temperature dependency related to delays of the comparators and invertors, amplifiers offset drift, leakages of main switches of core oscillators etc. The comparators offset and delays have to be designed low enough, in order to be achieved the total frequency deviation targets. Additionally, to keep comparators delay minimum varying from temperature is used PTAT current reference, which compensate degradation of transistors mobility with temperature.

B. The current source with R-2R ladder

In the practice are used different trimming configurations for RC oscillators: resistors strings, where part of the resistors are shorted; capacitors matrix, current DACs with transistor current sources [2]; or combination of the above [1], [3]. Very often the trimming structure is designed with nominal value, and a symmetrical trimming range around it. To cover the nominal value of the reference current and the trimming range, it was decided to use 9-bit, instead of 8-bit DAC. The simplified circuit, using binary R-2R matrix, is shown at Fig. 2.

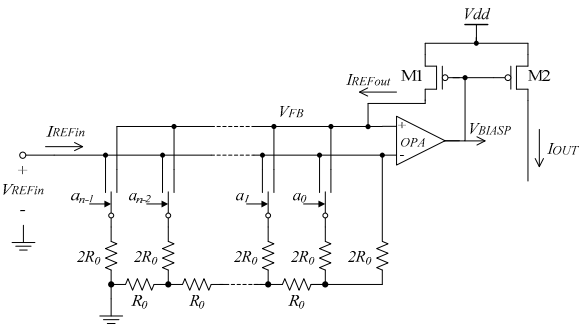

Fig.2: 9-bit configurable current source with R-2R ladder.

Here the sum of R-2R DAC current is converted to voltage at amplifier output, similar to the configuration in [4], but the feedback resistor is replaced by the transistor M1. The output current I_{OUT} is proportional to I_{REFout}, by use of the current mirror M1-M2.

The transistor M1 together with operational amplifier, form a voltage controlled current source. The generated current I_{REFout} is applied at part of R-2R resistor ladder, forming V_{FB}, where the negative feedback keeps equal the voltages V_{FB} and V_{REFin}. The input resistance at V_{REFin} and output resistance at V_{FB} is changing with trim code, which respectively change the input current I_{REFin} and output current I_{REFout}. The output reference current is a sum of all branches current, where the respective switches connect them to V_{FB}:

$$I_{REFout} = \sum I = \frac{V_{REFin}}{R_0 2^n} N \qquad (3)$$

In equation (3) n is the DAC resolution, N is the selected code, and R_0 is the unit resistor. The resistance of the switches, process mismatch, and other parasitic effects are neglected.

During the sub-block design, it should be considered non-ideality of the real devices, which finally will affect circuit performance. Let start with the assumption that $V_{FB}=V_{REFin}$, which depends on proper M1 transistor design. The M1 DC biasing operating point shall put the transistor in saturation. The M1 small signal output resistance r_{oM1} is in parallel to R-2R ladder equivalent resistance $R_{DAC}(N)=(R_0 2^n)/N$. The minimal influence of r_{oM1} can be achieved for $r_{oM1} >> R_{DACmax}$, where $R_{DACmax}=R_0 2^n$, which is easily achieved by adding cascode transistor and long gate of M1. The voltage difference at amplifier inputs is converted to current by M1 transconductance g_{m1}, multiplied by DC gain A_{OPA1}. The M1 output current flow trough $R_{DAC}(N)$ and in this way forms V_{FB}. Finally the V_{FB} dependency from V_{REFin} is:

$$V_{FB} = V_{REFin} \frac{1}{1 + \frac{1}{A_{OPA1} g_{m1\_min} R_0 \frac{2^n}{\sqrt{N}}}} \qquad (4)$$

In equation (4) g_{m1_min} is the g_{m1} for the minimum code (N=1). The g_{m1} is proportional to the square root of M1 drain current, e.g. $g_{m1} = g_{m1\_min} * (N)^{1/2}$.

The resistance of the switches also has effect over circuit linearity. The serial to $2R_0$ switch resistance R_{SW} decreases the current trough the branches. The other effect is that every stage V_{REFin} scale factor is not exactly 0.5, but slightly bigger. The I_{REFout} dependency by R_{SW} is:

$$I_{REFout} = \\ = \frac{V_{REFin}}{\left(R_0 + \frac{R_{SW}}{2}\right)} \frac{1}{2^n} \sum_{i=1}^{n} \left(a_{n-i} 2^{n-i} \left(\frac{R_0 + \frac{R_{SW}}{2}}{R_0 + \frac{R_{SW}}{4}} \right)^{i-1} \right) \qquad (5)$$

In the presented implementation, R_0=58kΩ, V_{REF}=0.9V, giving 15.5µA maximum current. The typical values of main linearity affecting parameters are R_{SW}=135Ω, A_{OPA1}=50dB, $g_{m1(N=320)}$=52µS, r_{oM1}=860MΩ. The output reference current, used in the core of the oscillator is divided by 4, where the nominal targeted current is 2.42µA at trim code 320, with 7.2nA (0.3%) trim step. For the custom case, where area of current source is 0.03mm^2, the achieved typical offset error is 8.37pA, gain error 0.09%, DNL error is ±0.16LSB, and the maximum INL error is 0.3LSB.

In most of the processes resistors with almost 0ppm/ºC TC are not available. Although it was not required for the current case, a design experiment was done to achieve good temperature stability while using two types of resistors. At Fig. 3 a new circuit is proposed. The two resistor matrices, with unit resistors R_1 and R_2, are connected in parallel, sharing the same input reference node V_{REFin}, V_{FB} and ground, as well sharing the same active components as

amplifiers and transistors in the current mirror. The bit control of the matrices is independent from each other.

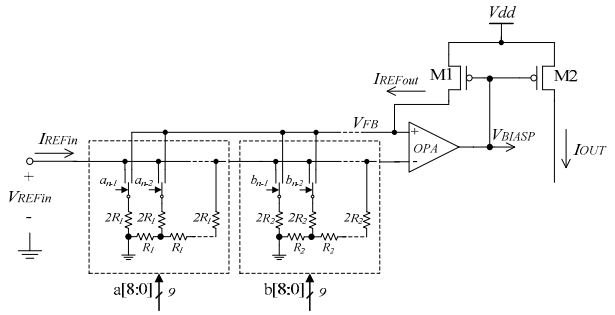

Fig.3: Current source with two resistors type R-2R ladder for temperature compensation

As the resistor structures are parallel, the total output reference current is also sum of the two independent current sources, with their respective N_1 and N_2 trim codes:

$$I_{REFout} = \frac{V_{REFin}}{R_1 2^n} N_1 + \frac{V_{REFin}}{R_2 2^n} N_2 \quad (6)$$

To simplify (6), it is assumed that both trim codes are equal and have maximum values:

$$I_{REFout} = \frac{V_{REFin}}{R_1} + \frac{V_{REFin}}{R_2} \quad (7)$$

The temperature coefficient of the reference current TC_I_{REFout} depends on the first order temperature coefficients of the resistors R_1 and R_2 – $TC1\_R_1$ and $TC1\_R_2$. It is assumed also that for the current case the temperature coefficient of reference voltage has no influence. After differentiation of (7) in respect to temperature, the equation for TC_I_{REFout} is:

$$TC\_I_{REFout} = -\frac{1}{R_1 + R_2}(R_1 * TC1\_R_2 + R_2 * TC1\_R_1) \quad (8)$$

As the target for reference current is zero TC, (8) can be transformed to:

$$R_2 = -R_1 \frac{TC1\_R_2}{TC1\_R_1} \quad (9)$$

And after substituting (9) in (7), R_1 can be calculated by:

$$R_1 = \frac{V_{REFin}}{I_{REFout}}\left(1 - \frac{TC1\_R_1}{TC1\_R_2}\right) \quad (10)$$

Equations (9) and (10) can be used for calculation of the nominal values of the resistors R1 and R2.

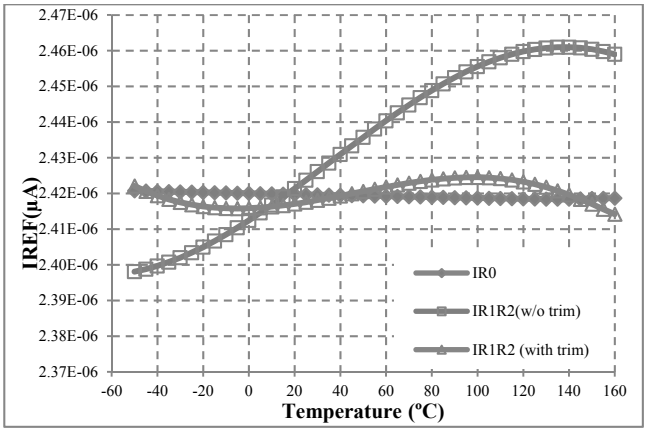

Fig.4: Variation of the reference current over temperature for resistor with "zero TC", and two resistors with different TC type

At Fig. 4 are presented simulation results of original bias circuit, using zero TC resistor ($TC_R_0 \approx \pm 30$ppm/ºC), the second one is using resistors R_1 and R_2 with $TC1\_R_1 = -1365$ ppm/ºC and $TC1\_R_2 = +1567$ ppm/ºC , with values calculated according (9) and (10). As the equations include only the first order (the linear) coefficients, the value of the current is correct for room temperature, while for the full temperature range of (−50÷160)ºC, it deviates from nominal value with 2.6%, having $TC\_IREFout = +130$ ppm/ºC. The best temperature curve that can be achieved with those resistors is the third curve, where the achieved accuracy is ±0.18% and $TC\_IREFout = \pm 36$ ppm/ºC.

C. The RC oscillator final circuit

The simplified block diagram of final oscillator circuit is shown at Fig.5. The voltage reference is a simple supply resistor divider with small capacitor to ground. The reference voltage for current generator is buffered by voltage follower. The second amplifier, responsible for generating V_{BIASP} is realized with a single stage OTA amplifier. The M1 and current sources have cascoding transistors, not shown on the diagram, to make them high impedance and providing supply independent current. The comparators and amplifiers use externally generated current bias source with positive TC, which compensates partially the dependency of *td* time over temperature. The capacitors are MIM (metal-isolator-metal) type, which are usually very linear in most of the processes, with very low temperature and voltage coefficients. The resistors in R-2R ladder are very low TC, which together with low capacitor TC, allows digital calibration in single temperature point.

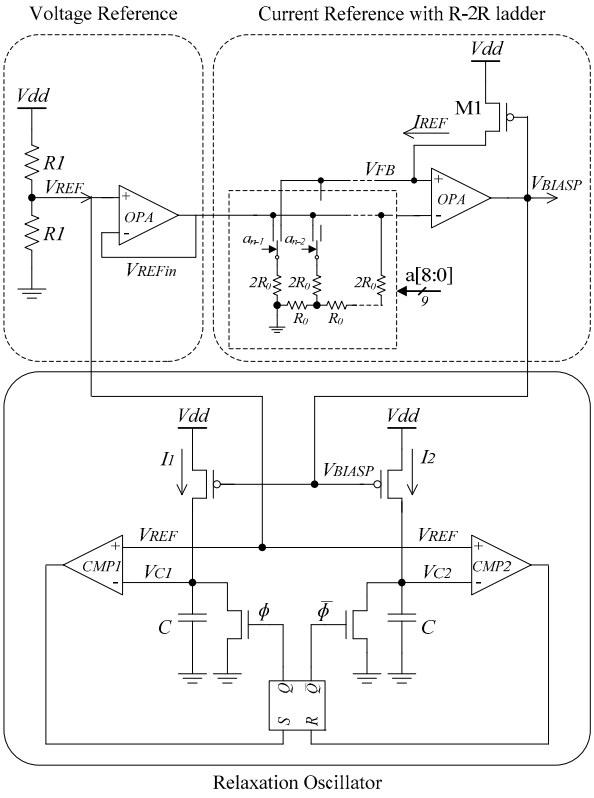

Fig.5: Block diagram of final RC-oscillator circuit

D. RC oscillator simulation and measurement results

The oscillator circuit is manufactured at 180nm technology. Fig.6 shows the measurement results for 6 devices, calibrated at 25ºC, with target clock frequency of 490 kHz. The measured temperature coefficients for most of the devices are about 35ppm/ºC, with maximum value measured of 50ppm/ºC at 160ºC. The variation with supply is below ±0.1%, showed at same figure with solid lines for one device. Fig.7 shows the calibration range of the frequency and measured DNL. The trimming range is digitally limited to be minimum 128, which has to guarantee that circuit will start in all conditions with reasonable frequency.

Table 1 summarizes the achieved results in this work and provides performance comparison with oscillators with similar output frequency, operating range and technology.

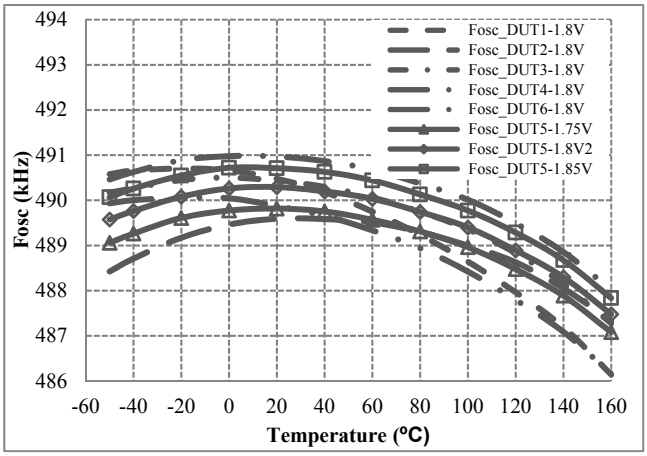

Fig.6: Frequency over temperature and supply.

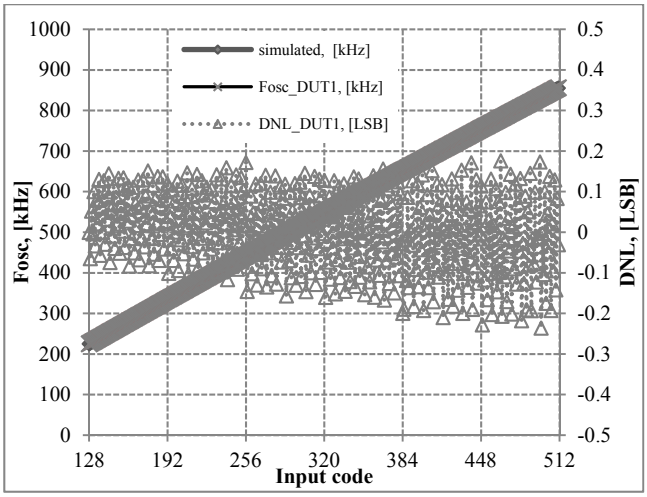

Fig.7: Frequency digital calibration range and DNL.

III. CONCLUSION

In this paper was presented a high precision RC-oscillator, using R-2R ladder, a new way for digital calibration of clock frequency. The circuit is area efficient and suitable for cases where has to be covered high calibration range, small trimming steps and good linearity for implementing time efficient production calibration. The ±1% PVT accuracy is achieved by digital calibration, ratiometric techniques and use of low TC passive components and single temperature calibration point. The low temperature dependency can be also achieved by combination of two resistors with two different TC.

TABLE 1. PERFORMANCE COMPARISON

	[2]	[5]	[6]	[7]	This work
Type	Relaxation	Relaxation	Relaxation	Relaxation	Relaxation
Feature	Digital current source trim	Temp. sensing and self-calibration	Comparator offset cancellation	Power averaging feedback	R-2R current trim
Process	0.13 µm	65 nm	65 nm	0.18 µm	0.18 µm
Area	0.01 mm^2	-	0.032 mm^2	0.04 mm^2	0.053 mm^2
Frequency	16MHz	13.8MHz	18.5kHz	14MHz	576kHz +/-15%
Supply	-	0.6V	1V	1.8V	1.8V
Current consumption	-	88µA	0.12µA	25µA	100µA
Variation with Supply	±1% @1.8V to 6.0V	±0.3% @0.5V to 0.9V	1% /V	±0.75% @1.7V to 1.9V	±0.1% @1.75V to 1.85V
Variation with Temp.	±2% @ -40 to 85ºC	±0.4% @ -55 to125ºC	±0.25% @-40 to 90ºC	±0.75 @ -40 to 125ºC	±0.47% @ -50 to160ºC

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Design and Investigation of Hall Effect Micro-sensors

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Abstract – **The requirements for precision integrated sensors are constantly increasing and the new techniques in the circuit design are of great importance. In this paper a new technology approved Hall effect microsensors are presented, which experimentally prove improved sensor's characteristics.**

Keywords – **Magnetic transducers, Hall effect sensors, Residual offset, Voltage related sensitivity.**

I. Introduction

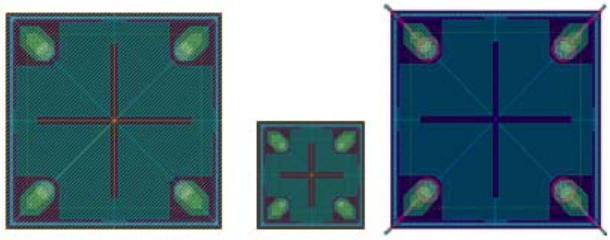
Hall effect sensors are linear transducers commonly used for switching, positioning, speed detection, and current sensing applications. When a magnetic field is applied, its distance from the Hall probe can be determined and the relative position of the magnet can be determined by groups of sensors. Hall element is used for contactless measurement such as linear and angular positions, electrical current and power, etc. The Hall element fabricated by CMOS integrated circuits' technology gives weak output signal (of the order of few millivolts). This signal is always corrupted by offset and noise [1]. If there is no additional information which concerns the value of the magnetic field or the sensor itself, it is impossible this noise to be distinguished [2]. A lot of methods are investigated in order to reduce the offset such as applying new fabrication technologies, designing particular sensor constructions, fabrication of additional control electrodes in the active sensor area applying offset compensation circuits, etc. [3].

The geometry of the sensor has a key role on the Hall-effect microsensors performance and has been studied a lot by the authors. The development of an efficient compact model of CMOS integrated Hall sensors is a big factor that will improve the efficiency and design, and which will widen the applications range of Hall devices in integrated systems [4].

The options for enhancing sensitivity S are: to optimize the geometrical sizes of the Hall plates so that the geometrical factor achieve maximum limit value, at approximately 1; to use semiconducting materials such as *n*-GaAs, *n*-InSb, *n*-Si, etc. with higher carrier mobility or to use small thickness of the sensor [2]. Therefore, the offset voltage and the voltage related sensitivity are key characteristics of Hall effect transducers. They describe its behavior to a degree that will allow one to design it into a larger system.

II. Sensors description and mode of operation

In this paper we present a basic cell which is symmetrical with dimensions 40 × 40 μm and interchangeable terminals. The two contacts are equipotential when applying a supply voltage and in the ideal case there is a zero offset in the absence of magnetic field. In a magnetic field $B \neq 0$, the total Hall voltage generated in the sensor appears between the output terminals [5].



a) b) c)

Fig. 1. Hall effect microsensors: a) 40 × 40 μm cell; b) 20 × 20 μm cell; c) PL cell.

We present two cells with improved technology in order to maximally reduce the raw offset at this stage. The first cell is with different sensor's dimensions. Instead of 40 × 40 μm we designed 20 × 20 μm cell. The specific character of the second cell is that a polysilicon is used for better distinguishing of *p*+ buried layer and *n*+ contacts. This approach aims to avoid the use of field oxide which experimentally proves that leads to crystallographic defects in the structure. All cells have the contacts located inside the active *n*-well region, in order to minimize as much as possible errors, related to the border. In Fig. 1 the three structures are presented. They are manufactured by 0.18 μm CMOS technology.

The measurements involve forcing a voltage (from 0.5 V to 3.0 V by step of 0.5 V) and measuring a voltage (Hall voltage). The basic idea of the four-phase spinning approach lies in reconnection of the relevant contact pairs, whereas the bias contacts become output contacts, and the supply contacts are used as sense terminals. Due to the fact that the Hall structure is symmetric with rotation, this technique leaves the output Hall voltage VH unchanged in value and sign. The Hall plate can be presented as a Wheatstone bridge and the ohmic offset can be represented

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as a small difference ΔR in value of some of the four identical leg resistors, for example $(R3+\Delta R) \neq R1$, $R1 = R2 = R4$. So, the Hall sensor is not symmetric with respect to the location of this "leg resistor" in the Wheatstone bridge. During the terminals' rotation, the polarity of the offset voltage reverses. The Hall signal is rotating in the same direction as the bias voltage, while the ohmic offset rotates in the opposite direction. If those two periodic measurements of the output voltage $V_H + V_{OFF}$ and $V_H - V_{OFF}$ are averaged, the true value of the output Hall voltage will be obtained [6].

In order more automated process of measurements to be achieved, the test equipment presented in [7] was created and implemented. A four-phase spinning method is used for offset compensation, which involves a combination of reversing source voltage polarity and Hall voltage polarity and reverse in the input and output terminals at the same time (Fig. 2).

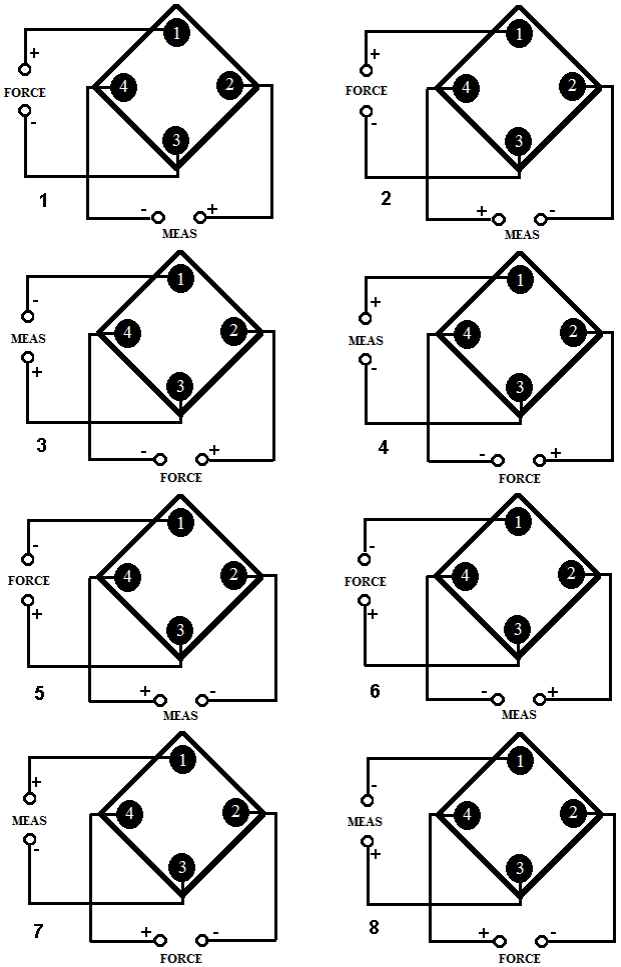

Fig. 2. Four phase spinning method for offset reduction of the Hall sensors.

The equipment gives the opportunity to simultaneously test four Hall plates. It consists of one switching matrix board with 64 relays to switch the Hall plates' diagonals for offset compensation. Also a Keithley 2602 was used for chip measurements. The first channel is used to supply the sensors and the second one is used to measure the output signal. The plates are tested at six supply voltages (0.5 V, 1.0 V, 1.5 V, 2.0 V, 2.5 V, 3.0 V). A LabVIEW program was created which drives the Keithley and the switch matrix board, so consecutively to supply and measure all diagonals of the tested four Hall structures. It also controls the temperature measurements and the value of the applied magnetic field.

III. Experimental Results

When the Hall transducer is biased, a small voltage is presented in the output, even when there is no applied magnetic field. This offset voltage is undesirable, because it constrains the capability of the sensor to read small constant magnetic fields.

The structures are investigated at room temperatures at six supply voltages. The experimental results for the raw offset are given in Table 1 for Hall plates 40 × 40 µm, 20 × 20 µm cell and PL cell. The graphical results are illustrated in Fig. 3.

Table 1. Raw Offset [mV] as a Function of the Supply Voltage [V] for the Three Hall Effect Structures

V_{DD} [V] / Strucure	0.5	1.0	1.5	2.0	2.5	3.0
40x40 µm	0.043	0.068	0.092	0.111	0.135	0.154
20x20 µm	0.013	0.016	0.025	0.031	0.043	0.063
PL	0.009	0.028	0.055	0.083	0.109	0.142

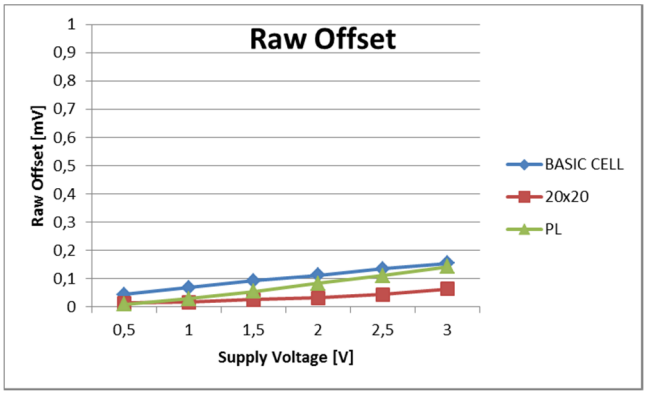

Fig. 3. Raw offset [mV] as a function of the supply voltage [V] for the three Hall effect structures.

The best result for the raw offset presents the technology improved 20 × 20 µm structure, where the maximum value of the offset is 0.043 mV at $V_{DD} = 3$ V, which is an excellent result for Hall sensors, manufactured in 0.18 µm CMOS technology. As a comparison, typical value for Hall sensors manufactured in the same technology is ±10 mV [8]. An excellent result shows also the PL structure with highest offset value of 0.14 mV. The biggest offset is manifested by the basic 40 × 40 µm cell – 0.15 mV.

Different effects could be the reason for this raw offset. Firstly, a raw offset may occur due to contacts misalignment during the technological process. The semiconductor materials, which are used for the manufacturing of Hall effect transducers, are highly piezoresisitive, which means that the electrical resistance of the material changes due to the mechanical deformation. The structures which will be preferred will be the improved 20 × 20 µm cell and the PL cell because they manifest lower raw offset which is a key

factor in sensors' characteristics and defines the sensors performance, which means higher Hall voltage and higher sensitivity.

When the four phase spinning method for offset compensation is used, we achieved a residual offset in order of μV. The experimental results are shown in Table 2 and graphically illustrated in Fig. 4

TABLE 2. RESIDUAL OFFSET IN [μV] AS A FUNCTION OF THE SUPPLY VOLTAGE [V] FOR THE THREE HALL EFFECT STRUCTURES

V_{DD}, [V] / Structure	0.5	1.0	1.5	2.0	2.5	3.0
40×40 μm	-0.26	-0.86	0.7	-1.23	-1.42	-0.92
20×20 μm	-1.56	-0.94	1.48	-0.38	-0.18	0.72
PL	-2.25	-3.32	-2.85	-4.86	-2.53	-3.01

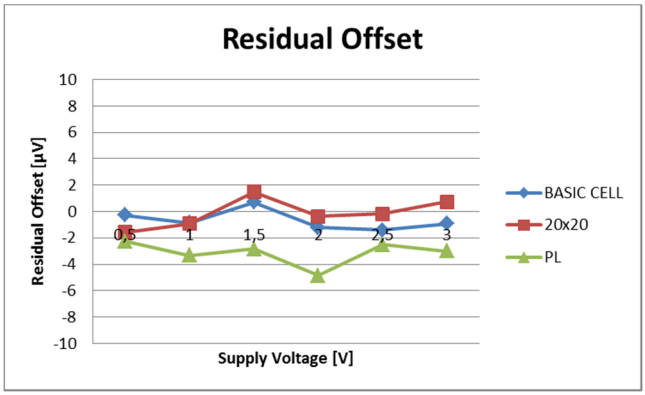

Fig. 4. Residual offset in [μV] as a function of the supply voltage [V] for the three Hall effect structures.

The experimental results clearly show that for all structures the offset is successfully reduced to ±5 μV. The maximum value for the basic cell is –1.42 μV, for 20 × 20 μm is –1.56 μV and for the PL cell is –4.86 μV.

It can be concluded that the offset is compensated to a minimum value which does not affect the output signal of the Hall transducers. Values, which are under 10 μV are absolutely acceptable due to the fact that the output Hall voltage value is of the order of few millivolts. The benefit is that the use of compensation circuit is not necessary, which complicates the whole system.

The next parameter we have investigated is the Hall voltage. The Hall voltage V_H is a main parameter which should be taken into consideration when choosing the optimal Hall effect microsensor. Here we have studied V_H as a function of the supply voltage V_{DD} at constant magnetic field B = 8 mT. The results are given in Table 3 and graphically illustrated in Fig. 5.

TABLE 3. HALL VOLTAGE [MV] AS A FUNCTION OF THE SUPPLY VOLTAGE [V] AT MAGNETIC FIELD B = 8 MT

V_{DD}, [V] / Structure	0.5	1.0	1.5	2.0	2.5	3.0
40x40 μm	0,421	0,843	1,26	1,67	2,07	2,47
20x20 μm	0,447	0,898	1,35	1,79	2,24	2,68
PL	0,464	0,928	1,392	1,851	2,313	2,765

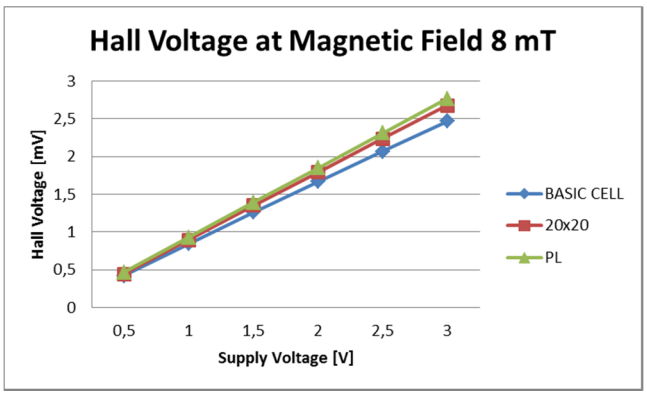

Fig. 5. Hall Voltage [mV] as a Function of the Supply Voltage [V] at magnetic field B = 8 mT.

It is clearly visible from the graphic that the lower the offset of the sensor is, the higher the Hall voltage is. The optimized PL sensor gives maximum value of the output signal of approximately 2.77 mV, then the 20x20 μm cell gives a value of 2.68 mV and the basic cell Hall voltage is maximum 2.47 mV at the higher supply voltage (3 V).
In our case, the best choice is the PL cell, which presents higher output signal and very low raw offset, which automatically leads to higher sensor's sensitivity, which is presented in the next Table 4 and Fig. 6.

TABLE 4. VOLTAGE RELATED SENSITIVITY [T-1] AS A FUNCTION OF THE SUPPLY VOLTAGE [V] AT B = 8 MT

Structures / V_{DD} [V]	40x40 μm structure	20x20 μm structure	PL structure
0.5	0,105284	0,11193	0,117
1.0	0,104722	0,11207	0,1163
1.5	0,104399	0,11158	0,1159
2.0	0,103864	0,11149	0,1155
2.5	0,103337	0,11127	0,1152
3.0	0,10268	0,11108	0,115

The sensitivity of the sensor is the most important parameter investigating magnetic Hall sensors. The voltage related sensitivity is calculated using Eq. 1:

$$S_V = \frac{V_H}{V_{DD} B}, T^{-1} \qquad (1)$$

where V_H – Hall voltage; B – magnetic induction and V_{DD} – supply voltage.

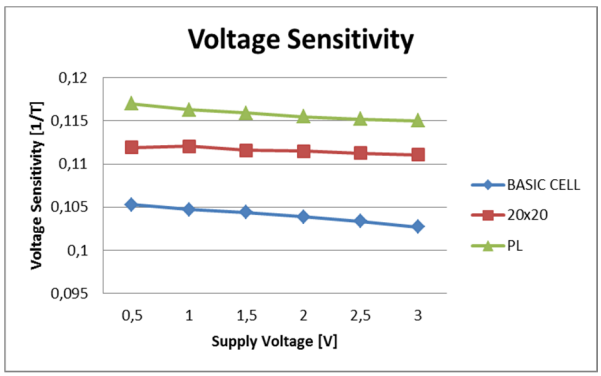

Fig. 6. Voltage Related Sensitivity SV as a Function of the Supply Voltage VDD.

As it can be seen from Fig. 6 the maximum voltage related sensitivity is manifested from the PL cell, then is the 20 × 20 μm cell and the lowest sensitivity is presented by 40 × 40 μm cell. To make a comparison, a typical value for the voltage related sensitivity in the literature is approximately from 0.05 to 0.08 T^{-1}. We achieved much higher value with our optimized sensors.

The polysilicon structure exhibit lower raw offset, which proves that the use of polysilicon instead of field oxide is a good solution for such type magnetic micro-sensors due to the fact that the field oxide isolation leads to more crystallographic defects at the surface of the structure. Also the dimensions of the sensor are critical for such type transducers.

IV. Conclusion

Three technology-improved Hall effect micro-sensors were investigated in order to identify the optimum one that manifests lower residual offset and higher sensitivity which are the main parameters for magnetic transducers. The proved advantages of the PL structure makes it ideal solution for a wide range of automotive applications.

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Microelectronic Circuit Emulating Hydrogen Bonding Network of Green Fluorescent Protein

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Abstract – **Hydrogen Bonding Network in active site of wild type Green Fluorescent Protein during the A→A* state is modeled. A microelectronic equivalent circuit is developed on its basis to emulate the operational principle of the Hydrogen Bonding Network. It is coded in Matlab to investigate its static and dynamic behavior. Output characteristics of static analysis are similar to inversed tunnel diode. The dynamic analysis show that the circuit can operate as amplifier, modulator and amplitude limiter.**

Keywords – **Hydrogen bonding networks (HBN), Green Fluorescent Protein (GFP), proton transfer characteristics, microelectronic circuit.**

I. Introduction

Fluorescent proteins and their hydrogen bonds are increasingly investigated for micro- and bioelectronics applications. Recent studies showed that the way they process the information under controlled light illumination can be described with an analytic function. Based on their functional properties are developed signal processing devices such as photoelements [1], photodiodes [2] and sensors [3].

Key element in protein fluorescence is the chromophore. It is neutral in ground state A of the photocycle and can be excited to state *A**. The latter quickly evolves to an intermediate state *I** that decays in picoseconds. *I** can change to ground state *I* or state *B** [4]. The chromophore participates in a hydrogen bonding network where a proton transfer takes place during the entire photocycle.

The dependence of proton transfer of each hydrogen bond on donor-acceptor potentials and potentials of surrounding residues is determined [5]. The resultant proton transfer characteristics are analyzed for applications in bioelectronics.

In this paper we perform static and dynamic analyses of the equivalent microelectronics circuits that emulate the behavior of the hydrogen bonding network in active site of wild type Green Fluorescent Protein during the A→A* state. Each residue that participates in hydrogen bonding network is juxtaposed to a block-element that is modeled by polynomials.

II. Model and Equations

The hydrogen bonding network (Fig. 1) participating in the photocylce is extracted from the wild type Green Fluorescent Protein in A state. Proton transfer in each hydrogen bond is investigated in [5] where the proton transfer parameter *K* is introduced in analogy to electron transfer constant in traditional electronics. This parameter allows the evaluation of proton transfer between the donor and acceptor of the hydrogen bond; hence we can evaluate the magnitude of the proton current. The calculation of *K* parameter accounts for the influence of donor/acceptor electrostatic potentials. This lets us introduce three- and four-terminal block-elements that are analogous to each heavy atom from the hydrogen bonding network.

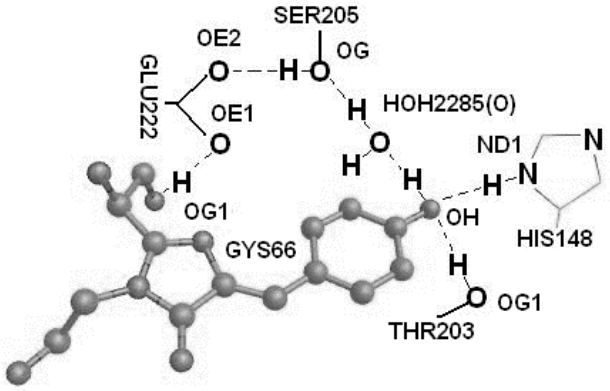

Fig. 1. Hydrogen bonding network consisting of OH and OG1 – oxygen atoms of chromophore GYS66, ND1 – nitrogen atom of Histidine residue HIS148, OG1 – oxygen atoms of Threonine residue THR203, O – oxygen atoms of water molecule HOH2285, OG – oxygen atoms of Serine residue SER205, OE1 and OE2 – oxygen atoms of Glutamic acid residue GLU222.

Most authors [6] consider that the driving force for proton transfer from chromophore to the hydrogen bonding network in A-A* state originates from strong proton acceptor glutamic acid residue GLU222. Hence, the output of the circuit should be between serine residue SER205 and GLU222. On the other hand, still there is no information for proton transfer between histidine residue HIS148 and threonine residue THR203 to the oxygen atom OG1 of chromophore (GYS66) in A-A* state. Therefore, the electrostatic potentials of these residues will influence the proton transfer in hydrogen bond between GYS66(OG1) and water molecule HOH2285. This means that they could be modeled as voltage sources T1 (for THR203) and T2 (for HIS148) at the circuit inputs (Fig. 2).

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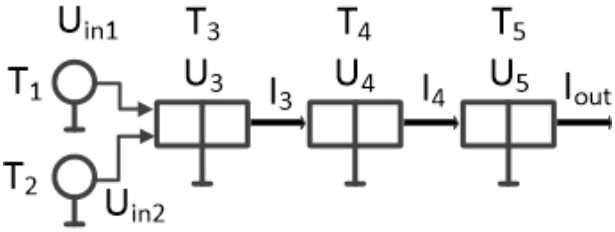

Fig. 2. Electronic circuit emulating the hydrogen bonding network.

The T3 block-element is analogous to oxygen atom OG1 of chromophore GYS66 which is proton donor of water molecule. The water molecule is proton acceptor of (OG1)GYS66 on one hand, and proton donor of (OG)SER205. For this reason, the water molecule HOH2285 is described by the three-terminal block-element T4.

The last block-element T5 is analogous to heavy atom (OG)SER205. It accepts proton from the water molecule and donates proton to GLU222 glutamic acid residue. In the next states *I* and *B* of the photocycle the hydrogen bond SER205(OG)…(OE2)GLU222 is presumed broken, therefore block-element T5 is considered output of the circuit.

The polynomial equations that are used for modeling the equivalent circuit from Fig. 2 are given below.

Block-element T1 describing the first voltage source is given by equation:

$$U_1 = U_{in} \quad (1)$$

Equation (2) describes the second voltage source T2 analogous to HIS148(ND1). Both residues are influencing (OG1)GYS66 in the same time so their notation as first and second voltage source is conditional.

$$U_2 = 1.0066*U_1 + 0.2183 \quad (2)$$

Equations (3) and (4) describe the block-element T3 that emulates GIS66(G1).

$$U_3 = 0.9964*U_2 - 0.2995; \quad (3)$$

$$I_3 = 0.0736*(U_3)^3 - 0.2976*(U_3)^2 + + 0.2104*U_3 + 5.7311 \quad (4)$$

Equations (5) and (6) describe the block-element T4 analogous to water molecule HOH2285

$$U_4 = 0.9606*U_3 + 0.0047 \quad (5)$$

$$I_4 = 0.097*U_4 + 29.599; \quad (6)$$

Equations (7) and (8) describe the output block-element T5 that is derived from SER205

$$U_5 = 1.042*U_4 - 0.2688 \quad (7)$$

$$I_5 = +0.0972*(U_5)^4 + 0.1493**(U_5)^3 - - 0.9863**(U_5)^2 - 2.1764*U_5 + 61.677 \quad (8)$$

These equations are coded in Matlab. The sample code is given below:

```
% T3 block-element GYS66(OH)
% function 3 -> 1inp-1out
% equation for HIS148->GIS66(OH) U3=f(U2)
inp1=out1
U3 = 0.9964*U2 -0.2995;

plot(U2,U3,'linewidth',2);
grid on
set(gca,'fontweight','b','fontsize',14)
title('T3');
xlabel('Uin2 [V]');
ylabel('U3 [V]');
% legend('simulation','data');
set(legend('\bf simulation','\bf
data',1),'fontsize',12);
pause;

% equation for GYS66(OH)->HOH2285 I3=f(U3)
inp1=out1
I3 = 0.0736*U3.^3 -0.2976*U3.^2 +0.2104*U3
+5.7311;

load('ogf1_gys66oh_hoh2285.dat');
U3exp = ogf1_gys66oh_hoh2285(:,1);
I3exp = ogf1_gys66oh_hoh2285(:,2);

plot(U3,I3,U3exp,I3exp,'ro','linewidth',2);
grid on
set(gca,'fontweight','b','fontsize',14)
title('T3');
xlabel('U3 [V]');
ylabel('I3 [pA]');
% legend('simulation','data');
set(legend('\bf simulation','\bf
data',1),'fontsize',12);
pause;
```

III. STATIC ANALYSIS

Static analysis is performed with input voltage from -3 to +3 V. Simulation results of the *I-V* characteristics of each block-element are compared to the data from [5] to validate the model. Fig. 3 and Fig. 4 show *I-V* characteristics of block-element T3 and T4: simulated and reference data from [5] are compared.

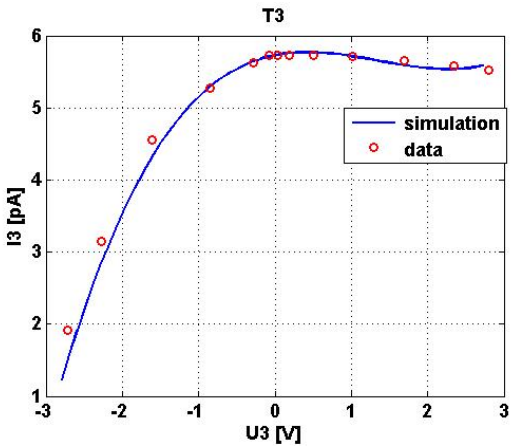

Fig. 3. *I-V* characteristics of T3 block-element (simulation versus reference data from [5]).

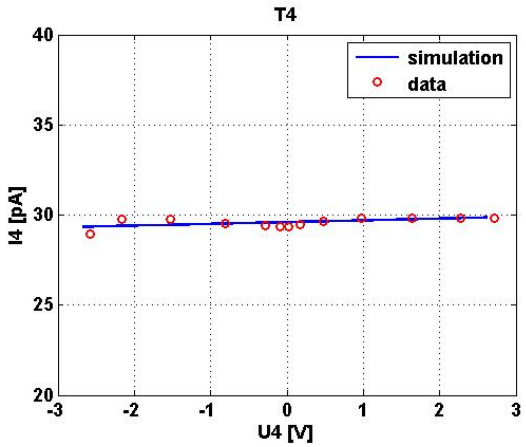

Fig. 4. *I-V* characteristics of T4 block-element (simulation versus reference data from [5]).

Fig. 3 and 4 prove that the polynomials in our model well describe the functional relationships of the block-elements. We obtained similar results for the other block-elements of the equivalent circuit in Fig. 2. The calculated maximum error is 4.32 %.

Afterwards we performed static analysis of the entire equivalent circuit. The results showed that all voltages are linearly changing with the input voltage. For this reason we show just the function of output voltage versus input voltage in Fig. 5. The output voltage range is between -3 and +3 V.

Fig. 6 shows the output characteristic of the circuit.

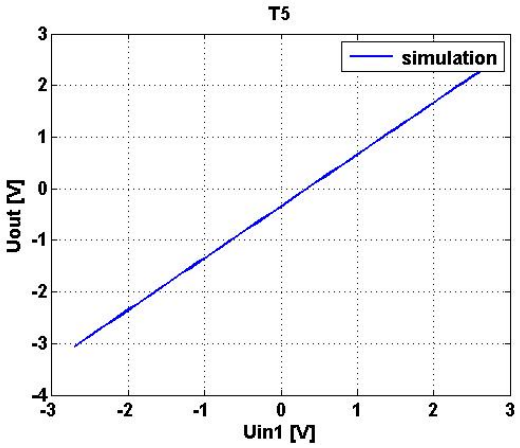

Fig. 5. Output versus input voltage.

The *output* characteristic is non-linear and it is similar to the *I-V* characteristic of a tunnel diode but mirrored. It can be separated in three regions. In the following simulations we move the operating point to study circuit behavior.

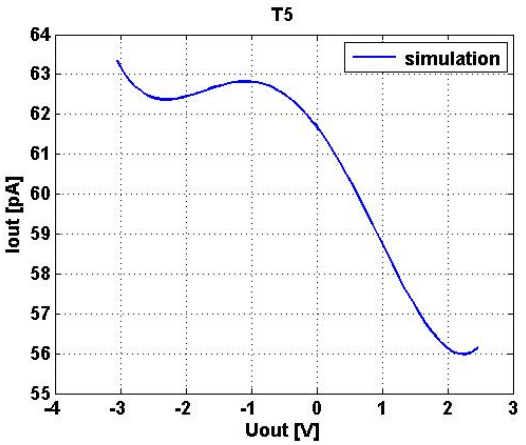

Fig. 6. Output circuit characteristics.

IV. Dynamic Analysis

Proton transfer between each donor and acceptor of hydrogen bonding network is very fast (in picosecond range) [6]. That is why our equivalent circuit of block-elements should operate in THz frequencies.

We use the three regions determined in static analysis to perform simulation of signal transfer with three different sinusoidal input voltages with amplitudes 0.5 V, 1 V, and 3 V respectively.

In the following Fig. 7 we show the output current versus time at amplitude of input voltage of 0.5 V. We may conclude that in this voltage mode the circuit operates as an amplifier.

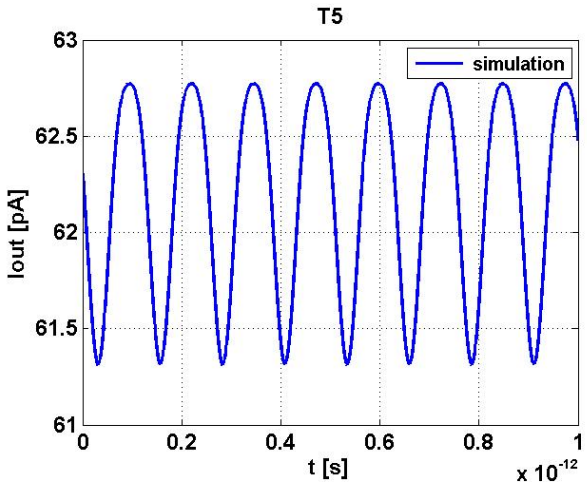

Fig. 7. Output current versus time at amplitude of input voltage of 0.5 V.

In Fig. 8 we illustrate the output current versus time at amplitude of input voltage of 1 V. It can be seen that circuit operates as amplitude limiter.

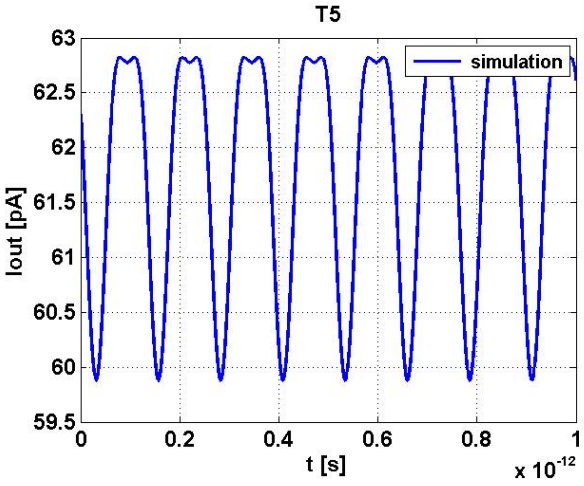

Fig. 8. Output current versus time at amplitude of input voltage of 1 V.

In Fig. 9 we show the output current versus time at amplitude of input voltage of 3 V. The result implies that the circuit operates as modulator.

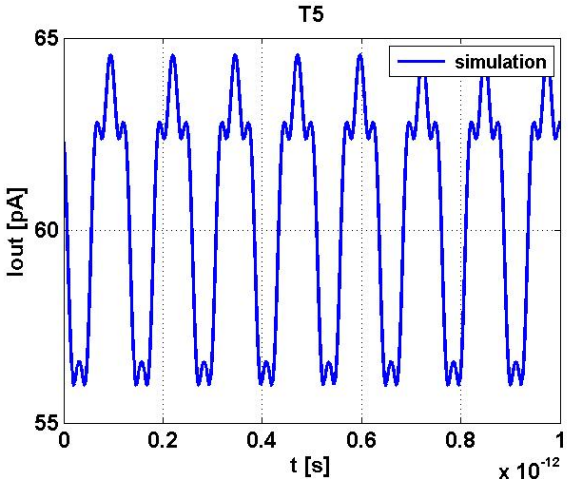

Fig. 9. Output current versus time at amplitude of input voltage of 3 V.

This implies that the circuit could operate as modulator, amplitude limiter or amplifier.

V. Conclusion

The equivalent circuit of block-elements well emulates the hydrogen bonding network in active site of green fluorescent protein during the A→A* state. The performed static analysis showed non-linear output *I-V* characteristic with three regions similar to a mirrored tunnel diode. The dynamic analysis performed in different operating point demonstrated that the circuit can be considered as amplifier, modulator or amplitude limiter.

Acknowledgment

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Modeling and Statistical Assessment of Packaging Stress Impact on CMOS Bangap Reference Circuit

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Abstract – **Mechanical stress sensitivity caused by IC packaging has been analyzed for CMOS test chips of a particular bandgap reference circuit. It has been applied a statistical method for analysis of distributions of measurements obtained from already produced devices. The conclusions have been grounded on theoretical model solved numerically for finding stress dependencies.**

Keywords – **mechanical stress, bandgap, test chip, model, piezoresistance, piezojunction, piezo-MOS, distribution**

I. Introduction

Typically the characteristics of CMOS integrated circuits change after packaging because their primitive components are sensitive to the influence of the mechanical stress. Some of the main mechanisms involved in the stress induced drift are explained with piezoresistance, piezojunction and piezo-MOS effects causing variations in resistors, bipolar and MOS transistors [1]. The bandgap reference circuits are such blocks where these piezo-effects are present and special design measures are needed for their minimization or compensation [2]. Particular interest in this paper, and also in the work described in [3], is the sensitivity to mechanical stress of a low supply voltage CMOS bandgap circuit (Fig. 1).

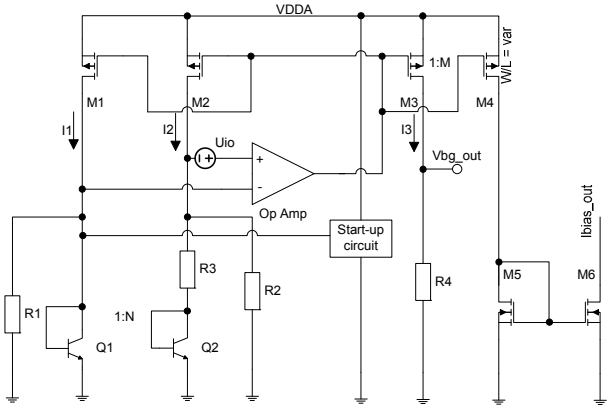

Fig. 1. Schematic of low supply voltage CMOS bandgap reference block showing sensitivity to packaging stress

Such bandgap circuit architecture allows operation at power supply voltages which are close or even below the traditional bandgap voltage [4] as long as the operational amplifier works also at such voltages. However during the process of qualification and test it has been found an unacceptably high drift of its output characteristics after IC packaging because of the significant piezo-effects in CMOS primitives.

Herein, the already performed research summarized in [3] is elaborated on the exact statistical populations of the performed measurements with the test chips providing detailed insight into the behavior of packaging stress. Also the complex non-linear equation used in the numerical circuit model is derived for better understanding of the dependencies.

II. Circuit Model Formulation

A numerical model was developed for finding the dependencies of the output characteristics V_{bg_out} and I_{bias_out} on the stress-induced variations of circuit component properties. It is described by several expressions starting with equalization of the voltages at the inputs of the operational amplifier and taking into account the DC input offset U_{io}:

$$V_{BE2} + U_{io} + I_{e2}R_3 = V_{BE1} \quad (1)$$

where V_{BE1} and V_{BE2} are base-to-emitter voltages of bipolar transistors Q_1 and Q_2, respectively. With I_{e2} is designated the emitter current of Q_2. As explained in [3], equation (1) can be expressed from basic bipolar physics neglecting the influence of Early voltage:

$$V_{BE1} - V_{BE2} = V_T \ln\left(\frac{I_{c1}I_{s2}}{I_{c2}I_{s1}}\right) = U_{io} + I_{e2}R_3 \quad (2)$$

where V_T is the thermal voltage while I_{s1} and I_{s2} are the saturation currents of the bipolar transistors Q_1 and Q_2, respectively, which are extracted from spectre model.

For achieving both accurate and simple model it is important review how matching is implemented in the layout of the investigated bandgap circuit. It can be shown that all resistors and transistors are interdigitized however common centroid technique is applied only for current mirrors and bipolar transistors. This means that ratios between bias currents and saturation currents can be assumed constant, i.e. the relations $I_1 = I_2 = I_3 = I_{bias\_out} / M$ and $I_{s2} / I_{s1} = N$ does not depend on stress distribution. Therefore, equation (3) can be derived if bias currents $I_1 = = I_2$ are expressed from the sum of the respective emitter currents and the currents through the resistors R_1 and R_2:

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$$I_{e1} + \frac{V_{BE1}}{R_1} = I_{e2} + \frac{V_{BE1} - U_{io}}{R_2} \quad (3)$$

In the last equation the emitter currents can be expressed from the respective collector currents using the current gains β_{F1} and β_{F2} which are also extracted from spectre model. Then an expression for emitter current of Q_2 is obtained:

$$I_{e2} = I_{e1} + \frac{V_{BE1}}{R_1} - \frac{V_{BE1} - U_{io}}{R_2} \quad (4)$$

The last equation can be rewritten for the collector currents using the extracted from spectre model current gains β_{F1} and β_{F2} of bipolar transistors. Also the collector current of Q_1 can be expressed from saturation current I_{s1} and base-to-emitter voltage V_{BE1}. Then equation (5) is obtained by replacement of the expressions for collector and emitter currents in (2):

$$\left(\frac{\beta_{F1}+1}{\beta_{F1}} I_{s1} e^{\frac{V_{BE1}}{V_T}} + \frac{V_{BE1}}{R_1} - \frac{V_{BE1} - U_{io}}{R_2} \right) R_3 + U_{io} =$$

$$= V_T \ln \left(\frac{I_{s1} e^{\frac{V_{BE1}}{V_T}}}{\frac{\beta_{F1}+1}{\beta_{F1}} I_{s1} e^{\frac{V_{BE1}}{V_T}} + \frac{V_{BE1}}{R_1} - \frac{V_{BE1} - U_{io}}{R_2}} \right) +$$

$$+ V_T \ln \left(\frac{\beta_{F2}+1}{\beta_{F2}} \frac{I_{s2}}{I_{s1}} \right) \quad (5)$$

After obtaining the typical offset U_{io} from circuit spectre simulations, the equation (5) has all technological inputs for finding a numerical solution for V_{BE1}, which is used to model the relative drifts of bandgap voltage $\Delta V_{bg\_out} / V_{bg\_out}$ and bias current $\Delta I_{bias\_out} / I_{bias\_out}$ as functions of the relative drifts of the resistances $\Delta R_i / R_i$ and saturation currents $\Delta Is_i / Is_i$.

From mismatch study on differential amplifiers it is known that the absolute variation of the input offset $\sigma(\Delta U_{io})$ depends on the absolute variation of the threshold voltage $\sigma(\Delta V_{TH})$, the relative drift of the process transconductance $\sigma(\Delta K_p) / K_p$ and the overdrive voltage V_{dsat} of MOS transistors in the differential pair [5]:

$$\sigma^2(\Delta U_{io}) \sim \sigma^2(\Delta V_{TH}) + \frac{V_{dsat}^2}{4} \left[\frac{\sigma(\Delta K_p)}{K_p} \right]^2 \quad (6)$$

The impact of piezo-MOS effect is known to have significant impact only on the mobility of majority carriers in the channel [6], therefore (6) can be simplified to the expression (7).

$$\sigma^2(\Delta U_{io}) = \frac{V_{dsat}^2}{4} \left[\frac{\sigma(\Delta \mu)}{\mu} \right]^2 \quad (7)$$

The drift defined by (7) is added to the typical offset found by simulation and then replaced in (5) which already provides numerical solution as a function of the stress-induced drift of the mobility $\Delta\mu / \mu$. A summary of the model outcomes is provided in the comparison between the plots in Fig. 2 showing the relative drifts of the bandgap voltage caused by the expected piezoresistive, piezojunction and piezo-MOS effects after packaging.

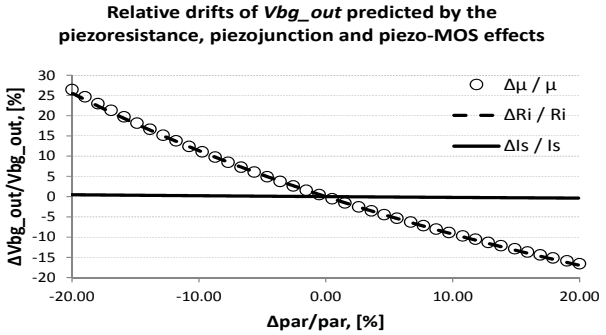

Fig. 2. Modeling of the impacts of the three different kinds of component drifts caused by piezo-effects

Although the impact from piezojunction effect is very small, it is more predictable for the particular investigated bandgap because it does not depend on mismatches. Therefore, the numerical solutions for bandgap voltage and bias current as functions of $\Delta I_s / I_s$ are important for further statistical assessment of the drift after packaging.

III. Configuration Of Test Chips

In Table 1 is summarized the configuration of the test chips produced for the statistical assessment of packaging stress.

TABLE 1. SUMMARY OF TEST CHIPS CONFIGURATION

Test chip name	Resistors	Bipolar transistors
"NPN"	p-poly	NPN
"PNP"	p-poly	PNP
"N-poly"	n-poly	NPN

Images of the fabricated different versions of the bandgap circuit are provided in Fig. 3. More details about their implementation are described in [3].

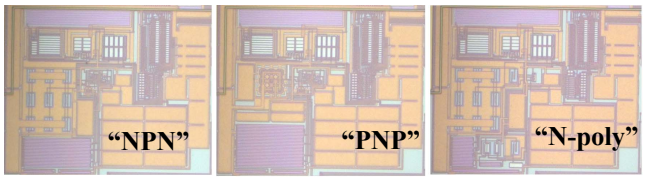

Fig. 3. Optical micrographs of the produced three types of the investigated bandgap reference circuit

IV. Population Study Of Measurements

The mechanical stress impact was evaluated by performing measurements before and after packaging at three temperatures: -40 ^{0}C, 35 ^{0}C and 150 ^{0}C. The relative

part-to-part drifts of the measured parameters V_{bg_out}, I_{bias_out} and R_4 were calculated from the following formula:

$$\frac{\Delta Meas}{Meas} = \frac{Meas_{package} - Meas_{wafer}}{Meas_{wafer}}.100\% \qquad (8)$$

where $Meas_{wafer}$ means the parameter measured on wafer before packaging and $Meas_{package}$ is the same measurement of the corresponding parameter however performed after packaging.

A. Population study of test chip "NPN"

In total 149 parts were evaluated from this test chip and their distributions of packaging induced drifts over temperature are demonstrated in Fig. 4-6.

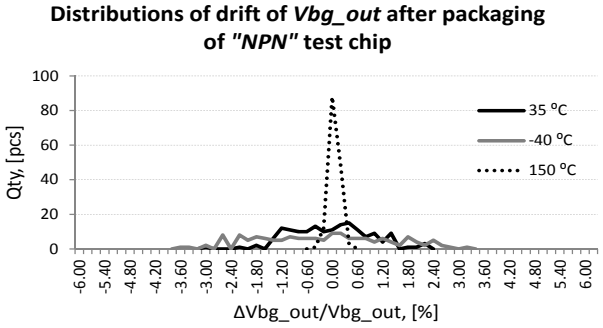

Fig. 4. Distributions of the relative drift of bandgap voltage after packaging of *"NPN"* test chip

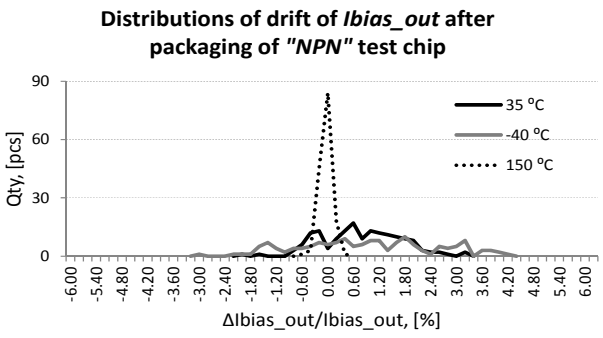

Fig. 5. Distributions of the relative drift of bias voltage after packaging of *"NPN"* test chip

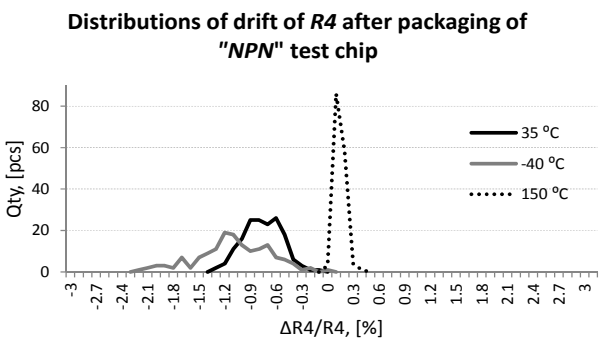

Fig. 6. Distributions of the relative drift of the resistance R_4 after packaging of *"NPN"* test chip

B. Population study of test chip "PNP"

In total 66 parts were evaluated from this test chip and their distributions of packaging induced drifts over temperature are demonstrated in Fig. 7-9:

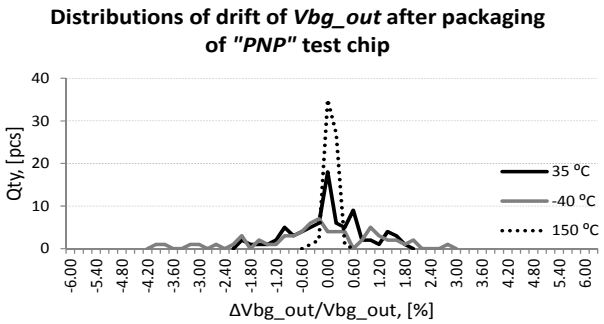

Fig. 7. Distributions of the relative drift of bandgap voltage after packaging of *"PNP"* test chip

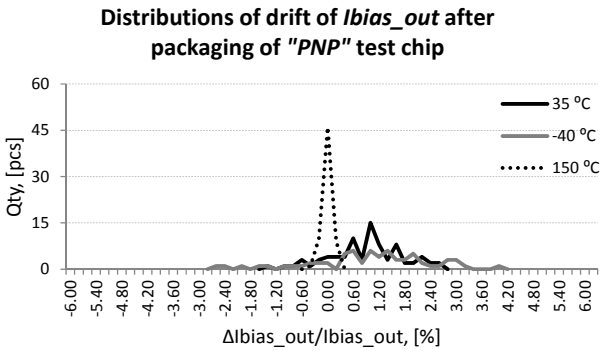

Fig. 8. Distributions of the relative drift of bias current after packaging of *"PNP"* test chip

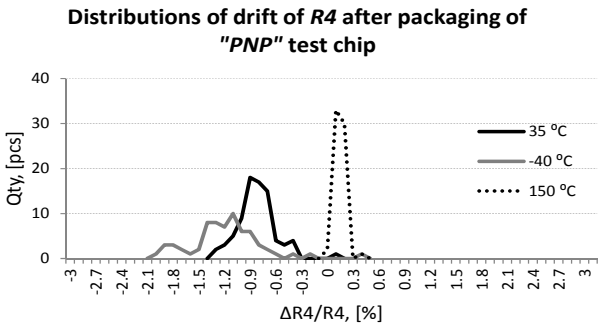

Fig. 9. Distributions of the relative drift of the resistance R_4 after packaging of *"PNP"* test chip

C. Population study of test chip "N-poly"

In total 120 parts were evaluated from this test chip and their distributions of packaging induced drifts of bandgap voltage over temperature are demonstrated in Fig. 10:

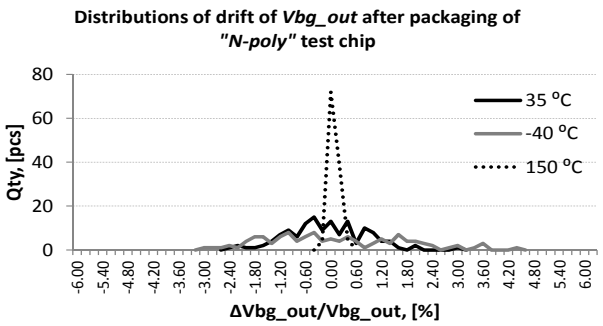

Fig. 10. Distributions of the relative drift of bias voltage after packaging of *"N-poly"* test chip

D. Analysis of distributions

The obtained data from the test chips show that spread of all distributions increases when the chips are cooled down. This is caused by the different thermal expansion coefficients of the materials used in the package – leadframe, silicon and mold (Fig. 11).

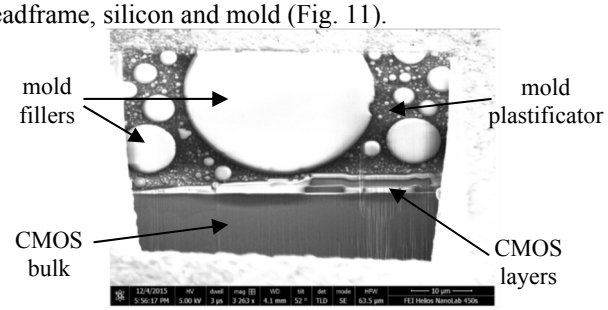

Fig. 11. An example of cross sectional view showing mold compound exerting mechanical stress on the top surface of an IC subjected to failure analysis by Melexis Bulgaria Ltd.

It is observed that distributions of part-to-part relative drifts of bandgap voltage are well centered. However this is not the case for the distributions of the drifts of bias current and resistor R_4. Expectedly, the mean value of polyresistance drifts with stress [7] and that causes also the drift of mean value of the bias current. This is predicted by the model as shown in Fig. 12 – the bias current and bandgap voltage drift inversely to the simultaneous drift of the resistances R_1, R_2 and R_3 ("R1R2R3" curve).

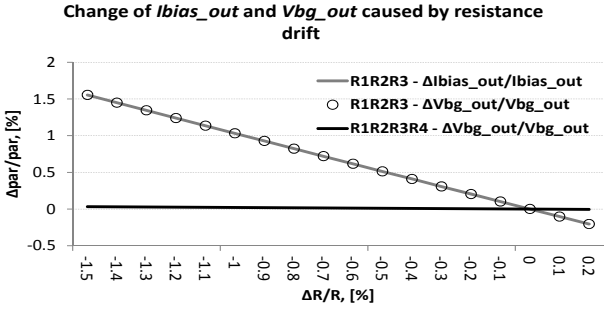

Fig. 12. Model of the relative drift of bandgap voltage and bias current caused by drifting resistances together

In Fig. 12 is also plotted the relative drift of bandgap voltage for the case when all resistors drift together ("R1R2R3R4" curve) causing almost zero drift which matches the observations in Fig. 4, Fig. 7 and Fig. 10.

Comparing the spread of the distributions it is seen that drifts of bandgap voltage and bias currents have at least two times bigger variation than drift of the resistance. Also the variation of the bandgap voltage drift is not smaller than the variation of the bias current drift as it should be if the resistor R_4 was well matched with the other three resistors. This means that dominant part of stress induced variation comes from the combination of piezo-effects and mismatches between the components.

V. CONCLUSION

Statistical assessments of populations of produced test chips were performed in order to check the behavior of the stress sensitive components in the investigated low supply voltage bandgap circuit (Fig. 1). The mean values of the obtained distributions match the sensitivities predicted by solving the model equation (5) for the case when all resistors change together. The distributions of the resistor R_4 drift show that the mechanical stress has a significant part-to-part variation around a systematic component which can be caused for example by randomly distributed mold fillers as seen in the example in Fig. 11. This part-to-part variation of the stress results in significant additional variations of bandgap voltage and bias current drifts proving the existence of mismatches between the resistors and / or between the MOS transistors in the differential pair of the amplifier.

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Advances in Thin Piezoelectric Film based Resonant MEMS Technology

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Abstract – **This work makes an overview of the progress made during the last decade with regard to a novel class of IC compatible piezoelectric devices employing plate-guided micro-acoustic waves in micromachined thin film membranes. This class of devices, originally proposed by the author in 2005, is referred to as either thin film Lamb wave resonators (LWR) or piezoelectric contour-mode resonators (CMR) both employing thin film AlN membranes. Their principle of operation is complementary to the so called thin film bulk acoustic resonators (FBAR), while employing the same technological platform. FBARs are currently widely employed in commercial filters and duplexers for telecom applications.**

Thin film Lamb wave resonators have shown unique performance in both frequency control and sensing applications. Here we demonstrate high quality factors Lamb wave resonators for low noise and thermally stable performance and discuss their application in high resolution gravimetric and pressure sensors.

Ongoing research activities will be further outlined. These are focused on the development of RF Transformer-filters and duplexers with performance comparable to their FBAR counterparts. A specific emphasis is put on the ability of these devices to operate in contact with liquids in view of advanced Bio-sensor applications.

Keywords – **Piezoelectric, RF Resonators, IC, LWR, CMR**

I. Introduction

The microwave electro-acoustics offers unique features in terms of low losses and small form factors for RF filter/duplexer applications as well as low noise frequency sources. Further, this technology enables the design of high-resolution sensors for chemical, physical and biochemical applications.

Currently the electro-acoustic technology is being developed in two parallel branches. These are the thin film bulk acoustic wave resonator (FBAR) technology and the microwave surface acoustic wave (SAW) technology. These two branches of the technology are highly concurrent to each other and have exhibited an impressive progress in performance during the last decade. FBAR technology employs thin film piezoelectric aluminum nitride (AlN) films on Si substrates which are acoustically isolated by micromachining an AlN membrane, while the commercial SAW technology employs single crystal substrates with high mechanical quality and high electromechanical coupling. An advantage of the FBAR technology is its inherent ability to be integrated with IC. One inherent disadvantage of the FBAR concept is its high sensitivity to technological tolerances, which in turn determine a relatively high cost of such an integration thus limiting the development of fully integrated systems. In an attempt to alleviate this technological gap a new class of devices named Lamb wave resonators (LWR) employing the FBAR technological platform was originally proposed by the author [1-3]. The LWR technology combines the integrated circuit (IC) compatibility of the FBAR technology with the low dispersive nature of the SAW technology. The latter makes the LWR technology an IC compatible alternative to the commercially established SAW technology.

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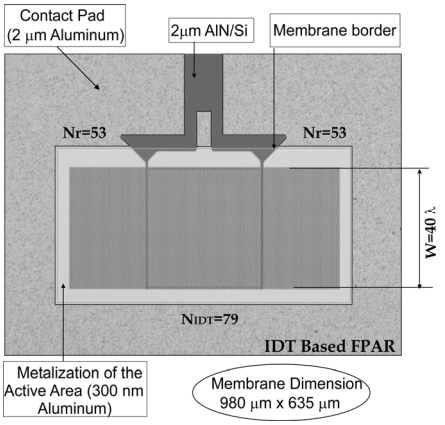
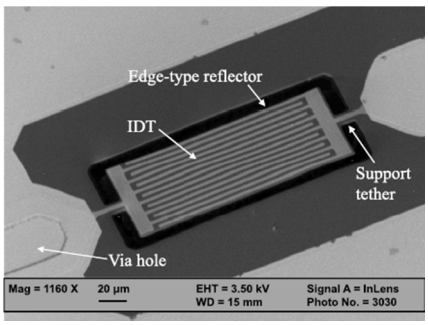
II. The LWR Technological Platform

Lamb wave resonator technology was proposed in two complementary basic designs both employing the lowest order symmetric Lamb wave (S0) [1, 4] .



(a)



(b)

Fig. 1. LWR Topologies as fabricated a) with distributed reflectors [2] b) with suspended edge reflectors [6]

The S0 mode in AlN membranes has mostly been explored because of its unique combination of extremely high velocity, low dispersion (resp. low susceptibility to technological tolerances) and sufficient piezoelectric coupling. In Figure 1 the basic Lamb wave resonator topologies are shown as fabricated. The two basic types of thin film LWRs differ only by the means of energy confinement, while demonstrating quite similar performance [5]. In Figure 1a the LWR employs interdigital transducer (IDT) surrounded by two Bragg reflectors represented by short-circuited metal strip periodic grating with pitch p=λ/2 (λ the wavelength of the Lamb wave) [3]. In Figure 1b the LWR employs suspended edge reflectors, while support tethers are used to suppress energy leak in transversal direction [6].

Most generally the edge type LWRs are smaller in size as compared to the grating-type LWR. Also the term contour-mode-resonator (CMR) is sometimes used to specify S0 LWR employing suspended edges.

The devices have been fabricated on a micro-machined free standing AlN membrane. For brevity we describe only the technological routine of LWR shown in Fig. 1a. As a supporting substrate a (100) oriented low resistive (10 Ω.cm) 4-inch Si wafer has been used. After cleaning the substrate, a 300 nm thick aluminum (Al) film is sputter deposited and then patterned. Subsequently 2 μm thick AlN film having a slightly tensile stress is deposited by reactive sputtering using a reactive balanced magnetron sputter deposition system operated in a pulsed direct current (DC) mode. 2μm thick Al contact metallization pads are then formed on top of the AlN. The top 300 nm thick Al gratings are then patterned by selective RIE. Finally, the Lamb wave devices are acoustically isolated from the supporting Si substrate by etching the Si substrate from the backside using a standard three-step dry etch Bosch process. The fabricated LWRs have demonstrated Q in excess of 3000 at 900MHz resonant frequency, determining a Qxf product in excess of 2.7 10^{12} Hz. Suspended edge LWR technology has demonstrated Q=2200 at 1.17GHz [7] as well as Q=3000 at 850 MHz [6] both representing a Qxf product of the same order.

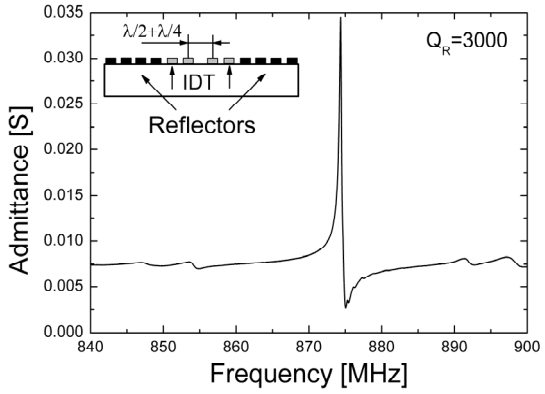


Fig. 2. Close in frequency response of grating type LWR with hiccup topology [8]

In Figure 2 measured response of a typical high Q LWR is shown [8].

The above presented technological platform was further upgraded to enable zero temperature drift performance. For the purpose a composite SiO2/AlN membrane is used. All design rules were thoroughly discussed elsewhere [5, 9, 10]. In this specific configuration an additional step of forming a thermally grown SiO2 over the Si is performed prior to AlN deposition. Devices with zero first order temperature coefficient of frequency (TCF) and second order TCF2 in the range about -31ppb/K^2 and -22ppb/K^2,were experimentally demonstrated when employing AlN thicknesses of d=0.167λ [9] and d=0.09λ [10], respectively.

III. LWRs in Low Noise Applications

Initially LWRs were employed in frequency sources characterized with low noises. In table I results from various literature sources are summarized [5].

TABLE I. PHASE NOISE AT 1KHZ OFFSET [5]

Topology	Resonant Freq. [MHz]	Noise [dBc/Hz]
Edge type LWR	222	-88
Edge type LWR	483	-88
Edge type LWR	583	-93
Grating type LWR	888	-92
Edge type LWR	1050	-81

Here we discuss the specific realization of a grating type LWR stabilized clock in the 900 MHz range running at up to 27 dBm (0,5W) loop power exhibiting a phase noise of –92dBc/Hz at 1 kHz [11]. The close-in phase noise 1Hz intercept point of the oscillator was measured as £(1Hz)=-2dBc/Hz which was then used to determine the LWR flicker noise constant α_R=2.1*10^{-36}/Hz [12]. This value is comparable with some of the best SAW resonators built to date and suggests that the LWR technology is a low noise one. This conclusion has been further supported in an independent study where a 222MHz edge-type LWR has demonstrated phase-noise contribution to the oscillator noise as low as -110dBc/Hz at 1kHz offset [13]. Further the grating type LWR have demonstrated superior power handling capabilities thus enabling performance with feasible thermal noise floor down to TNF=-186dBc/Hz [11]. More specifically the LWR was operated at an incident power level of 24 dBm (250 mW) for five weeks without performance degradation.

The low noise performance of the LWR technology is a prerequisite for the development of high resolution sensors provided that the sensitivity to various external biases is high. The latter motivated extensive research efforts directed towards the investigation of the sensing characteristics of the LWRs. Here we will summarize the results in a more general form.

A. LWR as Pressure Sensors

The use of a high aspect ratio membrane itself promotes higher stress levels in the membrane when exposed to ambient pressure and thus an improved sensitivity to pressure. Grating type LWR configurations typically employ about 2μm thick AlN membrane with area of about 0.5mm^2. Further, the S0 mode has been shown to be more

sensitive than all other modes in the AlN membranes [5] making it a preferable choice when developing a high resolution pressure sensors. In Figure 3 the pressure sensitivity of grating LWR sensor with the above described membrane configuration is shown.

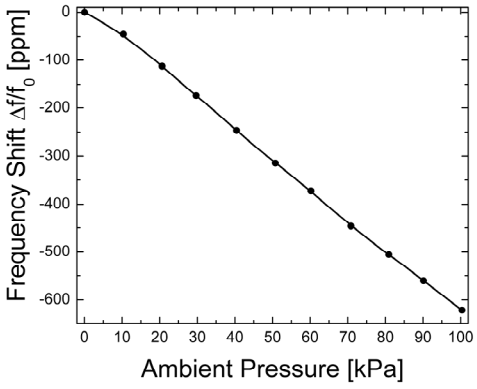


Fig. 3. LWR Pressure sensitivity

Some recent developments have demonstrated LWR pressure resolution bellow the 1Pa level proving thus the feasibility of this technology for the development of a low power wireless microphone [14].

B. LWR as Gravimetric Sensors

The S0 Lamb wave platform appeared to be much more mass sensitive as compared to its SAW and FBAR counterparts [5]. This was initially proven by simulations and has been further confirmed with comparative gas sensing measurements of Xylene performed with SAW and STW on Quartz employing the same sensing nano-layer. The results are summarized in Table II.

TABLE II. SENSITIVITY TO XYLENE OF HMDSO COATED RESONATORS [5]

Mode	Frequency	Sensitivity [Hz/ppm]
SAW on Quartz	430MHz	7.2
STW on Quartz	700MHz	9.1
LWR on AlN	890MHz	33

To relate the sensitivity values to the theoretical findings, the relative sensitivity to Xylene defined as the ratio of the absolute sensitivity (in Hz/ppm) to the unloaded resonance frequency was calculated for LWR, STW and SAW. These sensitivities were found to be in relation **5.0/1.3/1.0** for LWR vs. STW vs. SAW, respectively, which is in excellent agreement with the theoretical predictions.

IV. RECENT RESEARCH TRENDS

In this section we discuss some recent trends in the LWR research.

A. LWR as In-liquid Sensors

S0 Lamb wave in acoustically thin plates has a predominantly length-extensional vibration. This type of vibration, when immersed in liquid, is most generally frictional with respect to the liquid. The latter determines the LWR ability to confine mechanic energy in a manner similar to the quartz crystal microbalance (QCM) employing a transverse-shear bulk acoustic wave. Yet there are differences stemming from the laterally standing wave nature of the S0 mode [15]. In Fig. 4 measurements of LWR sensitivity for various concentrations of ethylenglycol and sucrose in water are shown [15].

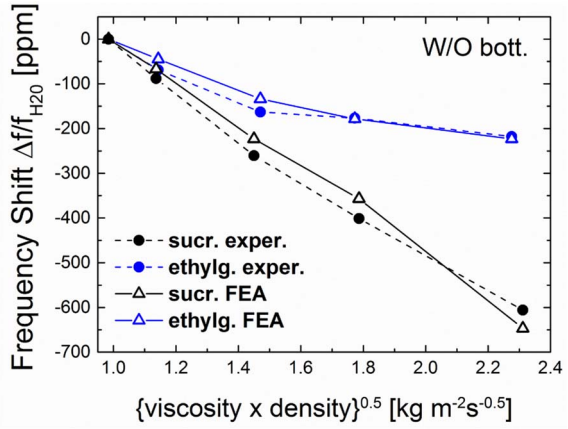


Fig. 4. Experimental vs theoretical influence of liquids mechanical and electrical properties on LWR performance [15].

It was also demonstrated and theoretically verified [15] that by using an electrically isolated LWR with a bottom metallic layer, only liquid mechanical properties can be sensed. S0-LWRs are more sensitive to density than to viscosity variations due to laterally alternating shear displacements propagating into the liquid by coupling part of their energy to longitudinal waves. However, this behavior can only be noticeable with high variations of density and comparable variations of viscosity, which is not the case of common aqueous mixtures. On the other hand, by using an electrically nonisolated from the liquid LWR (as in Fig. 4), the influence of the dielectric permittivity of the liquid is superimposed to the mechanical ones. Thus a pair of LWRs one with bottom electrode and another without can be used to discriminate changes in mechanical properties from changes in electric properties of the liquid. The in-liquid performance of LWR is comparable to its FBAR counterpart employing c-axis tilted AlN for shear mode of operation [16]. It is also noted the ability of the LWR to sense also changes in the electric properties of the liquid. Another advantage of the LWR technology is that it is developed on a commercial technological platform unlike its FBAR counterpart. In conclusion the LWR technology has shown to be a promising candidate for integrated Bio-sensor applications.

B. LWRs in RF Transformers and Filters

A recently proposed idea is to make use of the energy of the interrogation signal to trigger a low threshold electronic switch [17]. Since the power levels at practical distances are insufficiently low the energy is accumulated over a period of time and stored into a capacitor. A RF voltage transformer is typically needed to increase both the output voltage and the energy accumulated. A filter is placed between the antenna and the transformer to provide addressing. The LWR technology can be used in two-port trans-filter configuration with impedance transformation

[17] to transform RF voltages of about 10 times, while filtering the signal input enabled by its resonant behavior.

The use of LWR technology in RF filters for telecom applications has recently attracted great interest. It requires an electromechanical coupling of the Lamb wave exceeding 6% along with $QxKt^2$ product in excess of 100. It has been recently demonstrated that LWR with double sided IDT (on top and bottom of the AlN membrane) can achieve electromechanical coupling Kt^2 of up to 6.5% at specific membrane thickness and electrode material [18]. This resonator topology seems promising for RF filters employing the double mode SAW (DMS) filter principle. It is noted that the high coupling LWR is expected to have figure of merit comparable to FBAR but enables the design of DMS type filters/transformers avoiding multilayer stacks. First experiments with the double-sided IDT topology were made for AlN thickness corresponding to relatively low electromechanical coupling [19]. The results demonstrated are quite promising anyway. QxK_t^2 product in excess of 60 at coupling of about 1.8% has been demonstrated. FBAR technology offers QxK_t^2 in excess of 130 at coupling Kt^2 of about 7%. Obviously boosting the K_t^2 of the LWR has the potential to boost the QxK_t^2 product up to the range of the state of art FBARs.

C. Bandgap engineering of LWR

Bandgap engineering is a term introduced recently by the author [20]. It refers to a specific topology employing the different characteristics of Lamb wave propagation in gratings with the same periodicity but different strip widths. By adjusting the bandgap characteristics of the Lamb waves in IDT and the array of dummy fingers beside the IDT, one can effectively suppress wave diffraction, while eliminating spurious transverse modes in the structure. This principle has recently been proposed theoretically and confirmed experimentally on grating-type LWRs [20]. An extension of this principle has successfully been demonstrated on edge reflector based LWRs [21].

V. Conclusions

LWR technology has demonstrated number of advantages and has already been attempted for commercialization in integrated, zero thermal drift frequency sources and sensors. More efforts are needed for commercialization of this technology. It is noted that the FBAR technology needed 20 years of development and great support of investments until the reach of commercial viability.

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Many thanks to my PhD students G. Wingqvist, L. Arapan, E. Anderas and T. Mirea for their valuable contributions. I was happy to cooperate on the topic with BSAC Berkeley and Honeywell Research Inc, USA, GVR Trade SA, Switzerland, Universidad Politécnica de Madrid, Spain, ISSP-BAS and Sofia University, Bulgaria

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Effect of Anodization Conditions on the Breakdown Voltage of Nanoporous Aluminium Oxide

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Abstract – **Within the work presented the effect of voltage, electrolyte nature and time of anodization on breakdown voltage of nanoporous aluminium oxide layers are investigated. The dielectric layers formed under various conditions feature a pore diameter from 20 to 90nm, and the thickness lies within 1÷14μm. The results reveal that reanodization up to 300V significantly enhances the breakdown voltage. For Al/Al_2O_3 structure, it is found out that breakdown voltage depends mainly on the layer thickness and significantly less on the pore diameter.**

Keywords – **anodic aluminium oxide, reanodization, breakdown voltage**

I. Introduction

The continuously increasing technological requirements imposed by the industry towards electrical devices and electronic components are to some extent due to heat dissipation problems at a situation of continuous miniaturization of the geometrical sizes and increase of the working frequencies. The temperature escalation in devices is a serious problem concerning the accurate and long-life functionality of the device. The aluminium printed circuit boards (PCB), also known as IMSPCBs (Insulated Metallic Substrates Printed Circuit Boards) or MCPCB (Metal Core PCB) are the natural evolution of the PCB technologies corresponding to the crescent requirements towards board's heat conductivity, thermal dilatation and price [1, 2, 3]. Exactly this advantage causes the wide application of the aluminium printed circuit boards, used in powerful DC and AC transformers, LED technologies, switches and semiconductor-based relays. In case of boards, based on aluminium, various techniques are implemented to form a dielectric layer thereupon. Thick anodization is one of the methods thus growing oxide layer of sufficiently dense structure and good dielectric properties. According to this technology the pattering is performed by vacuum plating, which limits both the size of treated surface and conductive layer thickness. That is the reason of looking for another technique for plating a metal on aluminium oxide layer that allows gaining larger thickness. Such technique is electroless metal plating. However, a porous surface is therefore required to ensure the necessary adhesion.

In case of appropriate combination of anodization voltage, solution acidity and temperature, the structure of anodic aluminium oxide (AAO) can be transformed from dense into cell-like nanoporous one, similar to honeycomb. This way, Al_2O_3 layers having thickness from several hundred nm to several hundred μm are formed. They reveal a pore diameter from 0 to over 150 nm. The investigation of the effect of AAO structure on its dielectric characteristics is of practical interest, regarding AAO application as PCB basis. There are scarce investigations on this matter reported in the literature, most of them dealing with anodization of high-purity aluminium in sulfuric acid solution [4, 5] or with reanodization of porous AAO thus thickening their barrier sub-layer [6].

The present work aims at investigating the possibility to improve the dielectric properties of porous AAO by thickening the barrier sub-layer as well as to find out the most appropriate AAO structure to ensure high breakdown voltage.

II. Experimental Details

Samples of 0.1 mm thick aluminium foil (99,5%) were used as working electrodes. The electrode area was degreased by acetone and pickled for 1 min in 4% NaOH at 50° C. The porous AAO was formed in acidic solutions of H_2SO_4, $(COOH)_2$ and H_3PO_4 under the conditions, described in Table 1.

Table 1. Experimental conditions of formation of nanoporous AAO

Electrolyte	Concentration, %	Voltage, V	t, °C
H_2SO_4	10%	20	6±1
$(COOH)_2$	4%	40	14±1
H_3PO_4	5%	120	14±1

Series of samples with thickness from 1 to 14 μm were produced. The thickness of AAO layers was measured by optical microscopy of samples cross-section at a magnification of x500. The Optika microscope supplied with micrometric eyepiece and digital camera Opticam Pro-3 was used.

The next electrolytic process is the reanodization of porous AAO in 2.5% boric acid solution at room temperature. During this process, the barrier layer thickness

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becomes higher as result of the partial filling up the pores with dense oxide at the pore bottom [6, 7]. The reanodization was performed by applying constant anodic current density 1.5 mA/cm^2. After reaching maximal voltage of 300 V, the process continued extra 10 min keeping this voltage constant and the current began to decrease gradually (Fig. 1). Thereafter, the samples were washed by distilled water, dried by hot airstream, and heated for 2 h at 250 °C.

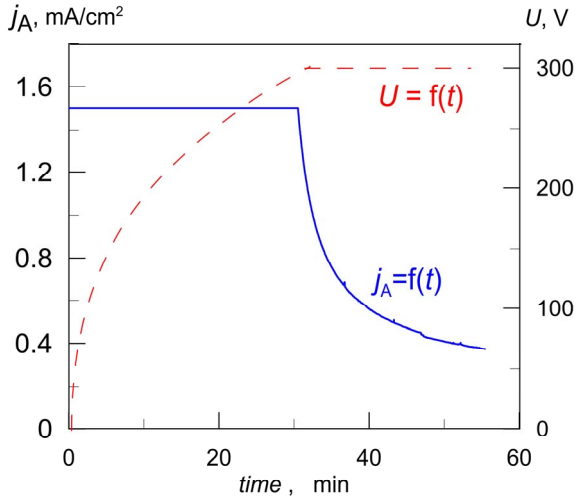

Fig. 1. Kinetic curves of reanodization of 5 μm porous AAO in 2.5% boric acid. The dense curve denotes the dependence of anodic current density j_A on time, while the dotted curve – the voltage/time dependence.

In order to determine AAO breakdown voltage, the uncovered part of the aluminium substrate was connected to the negative pole of the power source (TEC 3), and the positive electrode of the unit, having an area of 0.5 cm^2, is pressed to the dielectric AAO layer (Fig. 2). The voltage is slightly increased up to reaching breakdown value. The breakdown voltage is measured on several (5-10) surface points per sample.

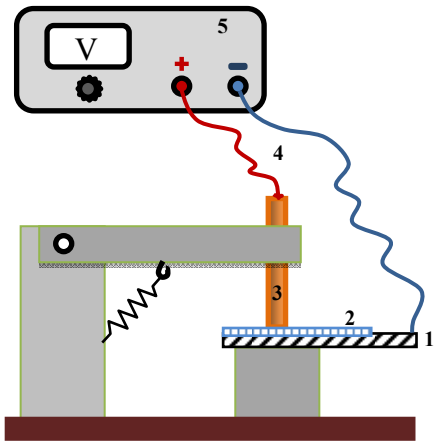

Fig. 2. Schematic representation of experimental setup for breakdown voltage measurements: 1 – aluminium substrate; 2 – dielectric layer of AAO; 3 – positive electrode; 4 – connecting cables; 5 – power source.

The scattering of the breakdown voltage values ΔU, measured on one and the same sample was calculated as a percent according to Eq. 1.

$$\Delta U = \frac{U_{max} - U_{min}}{U_{max}} .100, \% \quad (1)$$

where U_{max} and U_{min} are the maximal and minimal value of breakdown voltage respectively.

III. Results and Discussion

The results obtained for breakdown voltage of AAO on aluminium are presented by three characteristic values – the lower (U_{min}), the higher (U_{max}) and average one ($U_{average}$). The lowest value (U_{min}) represents an important characteristic value limiting the suitability of AAO as an insulating layer. There is no relation found between the value of breakdown voltage and the location of measurement point on the sample surface.

A. Effect of reanodization on breakdown voltage.

For AAO samples with thickness of 6 and 14 μm and formed in oxalic acid solution, breakdown voltage is measured before and after reanodization in 2.5% boric acid in order to increase the barrier sub-layer thickness. The results for breakdown voltage are presented in Table 2.

From Table 2 it is visible that the minimal breakdown voltage increases with 68 and 96 V after reanodization of 6 and 14 μm AAO respectively. The reanodization leads to decrease of value scattering from 41% and 43% before reanodization for 6 and 14 μm AAO to 26 and 13 % respectively after thickening the barrier sub-layer. Hence the effect of reanodization on scattering decrease is more significant at thicker AAO.

TABLE 2. BREAKDOWN VOLTAGE OF AAO SAMPLES BEFORE AND AFTER REANODIZATION

Thickness, μm \ Treatment		After anodization	After anodization and reanodization
6	U_{min}, V	29	155
	$U_{average}$, V	41	167
	U_{max}, V	49	210
14	U_{min}, V	236	332
	$U_{average}$, V	338	360
	U_{max}, V	414	383

B. Effect of AAO thickness and pore diameter on breakdown voltage

The dependencies of breakdown voltage on AAO thickness are plotted in Figs. 3, 4 and 5. Anodic aluminium oxides are formed in 10% H_2SO_4, 4% $(COOH)_2$ and 5% H_3PO_4. According to literature data and our previous investigations, the dielectric layers, grown under the same

conditions have an average pore diameter of 20, 35 and 90 nm, respectively [8-10].

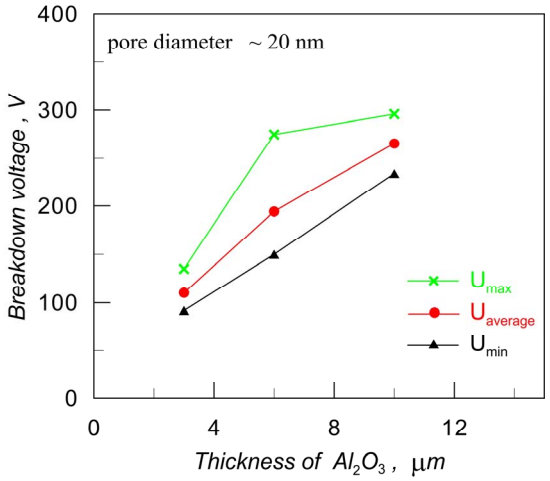

Fig. 3. Dependence of the breakthrough voltage of AAO layers of various thicknesses obtained in a 10% H_2SO_4 solution.

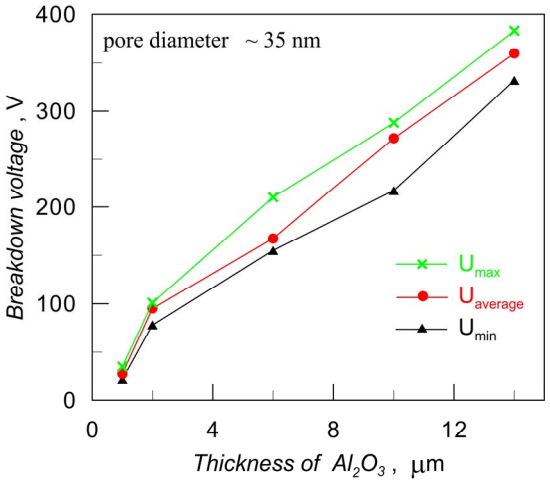

Fig. 4. Dependence of the breakthrough voltage of AAO layers of various thicknesses obtained in a 4% oxalic acid solution.

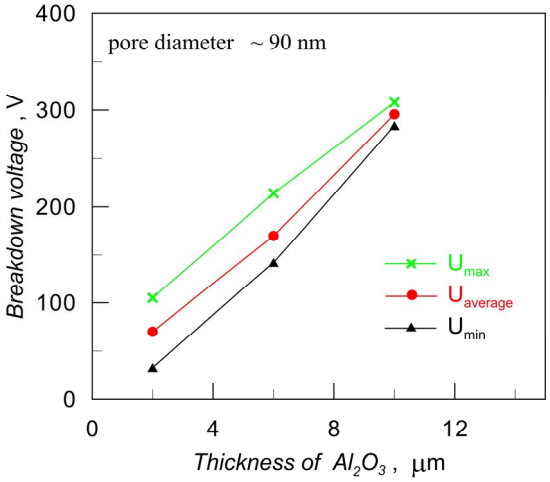

Fig. 5. Dependence of the breakthrough voltage of AAO layers of various thicknesses obtained in a 5% H_3PO_4 solution.

The thickness range of AAO is wider for layers produced in oxalic acid (1÷14 μm). In this case the sharp increase of U_{min} is recorded for thickness beside 3 and over 10 μm. In the range 3÷10 μm the change of U_{min} with the thickness increasing is linear at all oxide layers.

The minimal breakdown voltages U_{min} for AAO formed in three different acid solutions have close values for the relevant thickness. For example, at 6 μm oxide films, the difference in U_{min} is about 10 V what corresponds to below of 8% scattering. These results depict that the breakdown voltage depends mainly on the porous layer thickness. The impact of the electrolyte nature for porous film formation and thence the pore diameter is weak.

The quality of AAO and the suitability of the production process could be estimated by scattering of breakdown voltage values ΔU. It represents the width of the range that contains the values of breakdown voltage related to maximal voltage attained U_{max}. The higher the ΔU is, the less perfect is the dielectric material. The values of breakdown voltage for all samples demonstrate large value scattering, as in some cases the difference between minimal and maximal value exceeds 120 V. The large scattering of breakdown voltage values reaches in some cases 68 % (Table 3). This result could be explained by the technical purity of the aluminium samples used, which defines the presence of defects in the dielectric oxide layer structure. These defects could vary in size and nature. Possibly, the zones characterized by higher defects concentration give the probability for local breakdowns at lower voltages, while in neighbour zones, having more thorough structure, the breakdown voltage could reach many times higher values.

TABLE 3. SCATTERING OF BREAKDOWN VOLTAGE VALUES

Electrolyte	Thickness of AAO, μm	ΔU, %
10% H_2SO_4	3	31.8
	6	45.4
	10	20.9
4% $(COOH)_2$	1	37.1
	2	22.8
	6	26.2
	10	24.6
	12	13.3
5% H_3PO_4	3	68.6
	6	33.6
	10	7.8

There is a general trend of decrease in value scattering of breakdown voltage with the increase of thickness of dielectric layers. With widening of pores from 20 nm (from sulfuric acid) to 90 nm (formed in phosphoric acid) this reduction of ΔU become more markedly.

IV. CONCLUSION

The breakdown voltages of dielectric layers consisting of nanoporous anodic aluminium oxide are measured. The layers have a thickness of 1 to 14 μm and a pore diameter

of 20 to 90 nm. It is found out that thickening the barrier Al_2O_3 sub-layer at pore bottom by reanodization significantly increases the breakdown voltage. At the same time, the thickened barrier sub-layer leads to a decrease in breakdown voltage scattering from 43% down to 13 % along with thicker porous layers. The minimal breakdown voltage increases linearly with the increase of porous oxide thickness and exceeds 330 V for thickness of 14 μm.

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Effect of Saccharine on the Properties of Ni-Co Alloy Coatings Deposited in Citrate Electrolytes

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Abstract – **This paper presents some results, concerning the effect of organic additive (saccharin) on the composition and morphology of the alloy Ni-Co coatings deposited in citrate electrolyte using two types of deposition – constant potential and pulse potential electrodeposition. It was established, that the presence of saccharin in the electrolyte lowers the Co content in the alloy and makes the coatings shine and smooth with nano-sized crystals with average size in length approximately 200-250 nm and in height under 100 nm.**

Keywords – **Ni-Co alloy coatings, citrate electrolyte, stationary and pulse potentiostatic mode electrodeposition**

I. INTRODUCTION

Nanomaterials have attracted extensive interest recently because of their fundamental properties and wide range of applications [1]. Electrodeposition has been recognized as a simple, economical and versatile technique for the preparation of metals and alloys and nanocrystalline materials [2].

The use of appropriate technique of coating deposition is essential to produce materials with desired properties. Electrodeposition will produce nanostructures when the deposit parameter are chosen such that electrocrystallisation results in massive nucleation and reduced grain growth [1]. Potentiostatic deposition technique was mainly used to investigate the mechanism of coating morphology formation, which is specific to the applied potentials. It was shown in literature that the formation of a morphology requires a critical energy for nucleation which is supplied by the applied potential in potentiostatic deposition. Hence, by controlling the applied potential deposits with uniform and desired morphologies can be obtained using potentiostatic deposition. Thus, potentiostatic deposition technique can find significant use in applications where morphology control is critical [4-8].

Recently, *pulse* electrodeposition has received considerable attention for synthesis of nanocrystalline and amorphous alloy coatings [2-6]. The advantage of the pulse over stationary electrodeposition is that the properties of the deposit could be improved by control of pulse parameters, which gives a possibility for producing of nanostructured coatings [2]. Pulse electrodeposition can be used as a means for producing the coatings with properties unachievable by stationary deposition. Plating at extremely high amplitude polarization gives conditions for non-equilibrium growth of the coating, which may results in changes of the alloy phase composition and formation of unusual (anomaly) metastable structures significantly influences the nuclei formation, and thus improves the physical and mechanical properties of the coatings [3]. The presence of pauses between the pulses, on the other hand, allows additional adsorption of organic molecules or the products of a chemical reaction that may change the conditions of alloy formation and/or inhibit the crystal growth process [6].

In recent years an increasing interest exists towards electrodeposition of nano-sized Co and Ni-Co-alloy coatings [8-11] due to their magnetic properties Electrodeposited nanostructured Ni-Co alloy magnetic films have applications in computer read/write heads and microelectromechanical systems, magnetic recording media, sensors, etc. Due to their high hardness, wear resistance, endurance and corrosion resistance, the cobalt alloys are widely used in medicine, in nuclear-power systems, chemical- and oil industry [12-15]. The magnetic properties of electrodeposited Co films can be correlated with their structure and plating conditions [16].

Ni-Co coatings are deposited using mainly sulphamate electrolytes. The raising interest in recent years in using of citrate electrolytes is determined by its ability to serve as pH buffer agent and complexing agent. In citrate baths Ni and Co complexes are formed, adsorbed on the cathodic surface and thus favor the deposition process. Citrate ion is also adsorbed on the cathodic surface, resulting in inhibition of the hydrogen evolution reaction. Therefore, citrates are a possible environmentally friendly alternative to boric acid, used in most electrolytes [17]. The difficulties in using of citrate electrolytes come from its stability and this determine the necessity of its study.

During the deposition of very thin films via electrolysis, an increase of the internal tensions of the coatings is observed in most cases [18]. In order to decrease them, as well as to improve some other properties of the coatings, organic additives are often applied to the electrolyte. The application of pulse mode simultaneously with introduction of organic additives in the solution may significantly enhance the effect of additives [19].

In typical studies of electrodeposited nanocrystals, it is common to tailor the grain size using organic additives to the deposition bath [11]. Usually, the saccharin is used in electrodeposition as brightener [20], but it is established that it has a positive impact on the structure and the

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hardness of Ni-Co alloy coatings [9 -11]. Data about the saccharin influence on the characteristic nano-structural length scales in Co-Ni alloy coatings is very limited [11, 20].

The aim of the presented work is to resume some results, concerning the effect of saccharin concentration on morphology and composition of the NiCo alloy coatings deposited by constant potential and pulse potential techniques.

II. EXPERIMENTAL

The cell with a total volume 150 cm^3 includes a cathode made of electrolytic copper (Merck, 99.97 wt. % Cu), platinum anode and saturated reference calomel electrode (SCE). For the purpose of electrodeposition of Ni-Co alloy coatings, copper cathode plates with dimensions 1.5cm x 4cm were prepared. Prior to each experiment the surfaces of the copper cathodes were cleaned by etching in the especially prepared acid solution; then the cathodes were rinsed several times with distilled water and dried. The anodes were cleaned in hot 1M HNO_3, rinsed with distilled water and dried. All experiments were performed at room temperature (20^{o}C).

The Ni-Co alloys were deposited for 4 min in low acidic citrate electrolyte with composition 0.2M Ni (as $NiSO_4$ $2H_2O$); 0.2M Co (as $CoSO_4$ $7H_2O$); 0.485MH_3BO_3 and 0.4M Na_3citrat with saccharin (SCH) concentration in the range from 0 to 1.2 g.dm^{-3}. The pH of the solution was adjusted to 5.5 using citric acid or sodium hydroxide.

Two type of deposition techniques were applied – deposition at constant potential mode (cpm) and pulse potential mode. The values of deposition potentials of Ni-Co alloys in both modes were selected on the base of the kinetic studies of deposition [21]. The potentials of deposition of the Ni-Co alloy at stationary and pulse mode without and with the presence of addition of 1.0 g.dm^{-3} saccharin correspond to same value of current density i = 7.5 mA.cm^{-2}, determined from the polarization curves, given in [21]. These potentials are different at each deposition mode and electrolyte composition and are in the limits of -1,180V ÷ -1.290V (SCE). The pulse deposition of coatings was carried out through potentiostatic pulses with rectangular shape of the potential. The applied pulse frequency was 500 Hz at pulse filling $\theta = 0{,}5$ ($\theta = \frac{\tau_p}{\tau_p + \tau_z}$, where τ_p is pulse time, and τ_z is pause time). For the purpose a pulse generator was used connected to the input of an especially designed potentiostat connected to the three-electrode cell.

The chemical composition of the coatings was investigated using atomic absorption analysis (AAA). The morphology and the elemental composition were investigated using SEM and Energy Dispersive Spectral Analysis (EDSA) through equipment of Oxford Instruments, JSM-6390- Jeol.

III. RESULTS AND DISCUSSION

The effect of **saccharin** concentration on the chemical composition of the coating (in Co content) is shown in Fig.1. The analysis of the data obtained proves that both in constant and in pulse mode the content of Co decreases with the increase of saccharin concentration in the electrolyte. The content of Co in Ni-Co coatings is higher in the case of pulse mode. The trend of decreasing of Co content in the alloy with increasing of saccharin concentration has also been observed by the other author in sulphate electrolytes [20]. The phenomena was explained by the higher adsorption of saccharin raising its concentration and increasing the cathodic polarization, which impedes the alloy electrodeposition [20]. |According to the others, in acetate solutions, the saccharin facilitate the nickel deposition and hinder that of cobalt [9].

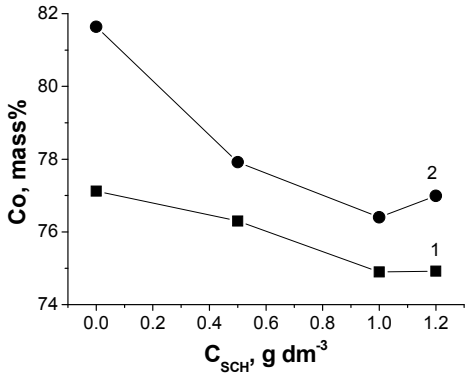

Fig. 1. Dependence of the element composition of the coating (Co-content) on saccharin concentration. 1 – constant potential mode; 2- pulse potential mode of deposition

The effect of saccharin concentration on morphology of the coatings was studied by SEM. The SEM images of Ni-Co coatings deposited at different conditions are shown at Fig.2. Comparing the images without additive in both modes of deposition (cpm, Fig.2a and ppm Fig.2b) it can be said that the application of pulse mode results in formation of finer crystalline Ni-Co alloy structures, while in stationary mode the deposited coatings present clearly shaped needle-like crystallites. The average size of crystals in cpm was about 300-400 nm, while in pulse mode a more fine crystalline structure is observed with a tendency to rounded crystallites with size under 300 nm.

SEM-images of Ni-Co coatings prepared in citrate electrolyte in presence of 1 g.dm^{-3} saccharin in pulse mode are shown at Fig.2c, d. The image with magnification of x100 000 (Fig. 2d) cannot show the structure because of very small dimensions of the crystals in width and especially in height. The obtained images show that in the presence of saccharin combined with application of pulse potentiostatic mode, the Ni-Co coatings are very smooth, shiny, with the dimensions of the crystallites of the coatings with length approximately 200-250 nm and in height under 100 nm. The small dimensions are the reason for the unclear images at microscopic images, even at very high magnifications. This result can be explain with the presence of pauses between pulses in pulse potential mode, in which

additional adsorption of the additives possibly occurs. This may lead to a lower total cathode active surface. It is possible that the pauses relieve the reaction of removal of the hydrogen-gas evolution simultaneously with metals deposition, which could avoid pitting formation and make worse the coating quality.

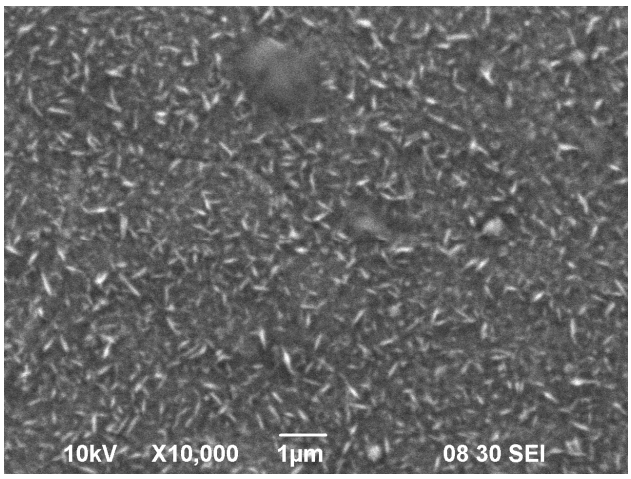

Fig. 2a

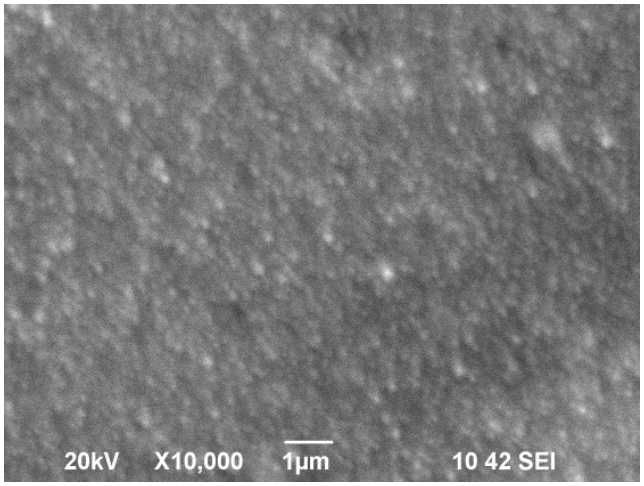

Fig.2 b

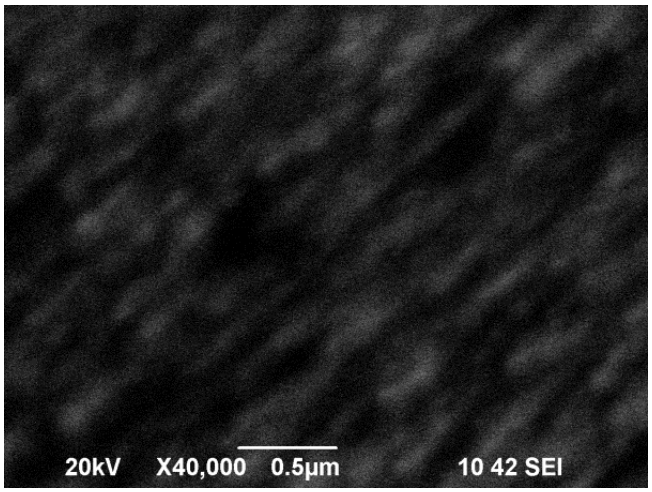

Fig.2c

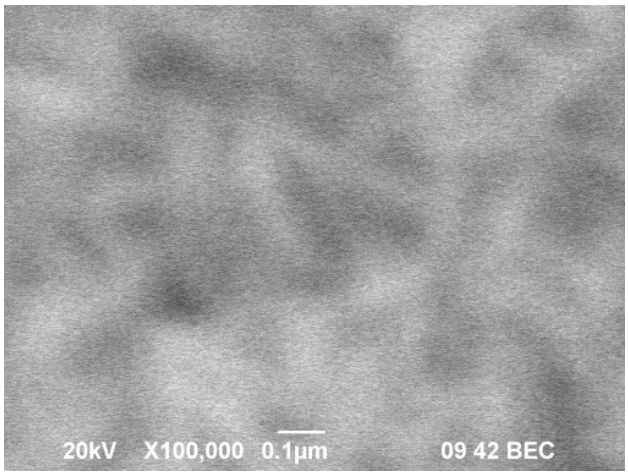

Fig.2d

Fig. 2. SEM - images of Ni-Co alloys, electrodeposited in cpm (a) and in pulse mode (b) without saccharin; in pulse mode with 1.0 $g.dm^{-3}$ saccharin (c, d).

IV. Conclusion

On the base of the presented results it can be concluded, that:

- pulse potential mode of deposition without any organic additives in the electrolyte gives alloy coatings with bigger Co content compared to constant potential mode;
- increasing the saccharin concentration up to 1.2 $g.dm^{-3}$ in citrate electrolyte the Co content decreases in the alloy coating;
- applying the pulse potential mode of deposition and adding of saccharin in the electrolyte makes smooth and shiny alloy coatings with nano-dimensions of the crystals.

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Characterization of Chalcogenide Film on Substrate Specimens by the Graphical Method Using Accurate Refractive Index of the Substrate

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Abstract – **Refractive index of the substrate depending on its absorption is used in the graphical method for optical characterization of a film on a transmitting substrate, from its transmission spectrum. Three amorphous chalcogenide films on identical glass substrates are characterized by the graphical method. Indications are presented that these characterizations are more accurate than previous characterizations of the same films.**

Keywords – **optical characterization, graphical method, thin film, refractive index**

I. INTRODUCTION

The demand for engineering applications of films, which transmit in the middle to far infrared regions and have large refractive indices, determines the significant interest in optical characterization of chalcogenide films [1].

The graphical method has been proposed by Swanepoel, initially for optical characterization of films with uniform thickness [2]. It has been expanded thereafter to characterization of films with non-uniform thickness *d*, described by the variation Δd of the film thickness with respect to the average film thickness $\overline{d}$, whereat $d = [\overline{d} - \Delta d, \overline{d} + \Delta d]$ [3]. The graphical method is applicable to a specimen of a film on a transmitting substrate, by using its normal incidence interference transmittance spectrum $T(\lambda)$ due to light interference from both surfaces of the film, where λ is the wavelength of light. This method also uses tangential points $[\lambda_{tan}, T(\lambda_{tan})]$ between the spectrum $T(\lambda)$ and its two envelopes $T_+(\lambda)$ and $T_-(\lambda)$ drawn around the minima and the maxima of $T(\lambda)$, respectively.

Accurate values of the refractive index $n_s(\lambda)$ and the absorbance $x_s(\lambda)$ and the of the substrate can be computed from the system of two equations for known transmittance spectrum $T_s(\lambda)$ and reflectance spectrum $R_s(\lambda)$ of the substrate [4]:

$$T_s = \frac{(1-R_{sa})^2 x_s}{1-R_{sa}{}^2 x_s{}^2} \tag{1}$$

$$R_s = \frac{R_{sa}[1+(1-2R_{sa})x_s{}^2]}{1-R_{sa}{}^2 x_s{}^2} \tag{2}$$

where $x_s(\lambda) = \exp(-4\pi k_s d_s / \lambda)$; $k_s(\lambda)$ and d_s are the extinction coefficient and the thickness of the substrate; and $R_{sa} = [(n_s - 1)/(n_s + 1)]^2$.

Notably, in all known previous characterizations employing the graphical method, $n_s(\lambda)$ has been computed only from Eq. (1), e.g. in [3,5-6], assuming lack of absorption in the substrate, i.e. $x_s = 1$

It was shown in [4] though that using wider spectrum UV/visible/NIR spectrophotometer and glass substrates leads to up to ~ 3 % smaller x_s, and more than 5 % errors in the characterization of both $\overline{d}$ and the refractive index $n(\lambda)$ of the film.

The graphical method is based on expressing the envelopes $T_+(\lambda)$ and $T_-(\lambda)$ of the normal incidence spectrum $T_+(\lambda)$ for the investigated specimen with non-uniform thickness film, by the envelopes $T_{u+}(\lambda)$ and $T_{u-}(\lambda)$ of the spectrum for a fictional specimen differing only in its uniform thickness $\overline{d}$ of its film, as follows [3]:

$$T_+ = \frac{\sqrt{T_{u+}T_{u-}}}{\theta}\tan^{-1}\left[\sqrt{\frac{T_{u+}}{T_{u-}}}\tan(\theta)\right] \tag{3}$$

$$T_- = \frac{\sqrt{T_{u+}T_{u-}}}{\theta}\tan^{-1}\left[\sqrt{\frac{T_{u-}}{T_{u+}}}\tan(\theta)\right] \tag{4}$$

where $\theta = 2\pi n \Delta d / \lambda$, and λ_{tan} are the same for the transmittance spectra of the investigated and the fictional specimen.

Also, λ_{tan} should satisfy the interference condition:

$$2n\overline{d} = m\lambda_{\tan} \tag{5}$$

where the interference order number *m* is an integer for λ_{tan} corresponding to a maximum of $T(\lambda)$, and a half-integer for λ_{tan} corresponding to a minimum of $T(\lambda)$. Substitution of the above expression for θ in Eq. 5 gives [3]:

$$\frac{l}{2} = \left(\frac{\overline{d}}{\pi\Delta d}\right)\theta - m_1 = S\theta - m_1 \tag{6}$$

where $m = m_1 + l/2$; m_1 is the smallest interference order number, for the longest wavelength max(λ_{tan}); l = 0,1,2,3,… is the count of λ_{tan} with decreasing λ, starting with l = 0 at max(λ_{tan}); and S is the slope of the linear function $l/2(\theta)$.

Furthermore, if $n_{\rm m}$ and $n_{\rm m+0.5}$ are the refractive indices for two tangential point wavelengths λ_m and $\lambda_{m+0.5}$, corresponding to adjacent maximum and minimum of $T(\lambda)$, it follows from Eq. 5 that the film thickness is [2]:

$$d(\lambda_m) = \frac{\lambda_m \lambda_{m+0.5}}{4(\lambda_m n_{m+0.5} - \lambda_{m+0.5} n_m)} \tag{7}$$

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Moreover, in the spectral region of weak absorption in the film, its refractive index can be expressed as [3]:

$$n = \sqrt{M + \sqrt{M^2 - n_s^2}} \quad (8)$$

where $M = 2n_s \frac{T_{u+} - T_{u-}}{T_{u+} T_{u-}} + \frac{n_s^2 + 1}{2}$.

In this paper are reported new results from characterization of three different chalcogenide films, by the graphical method. Each one of these films has been deposited on a glass substrate, and has been characterized in [4] and [5]. Unlike in all known previous graphical method characterizations, e.g. [3,5-6], here is used accurate refractive index of the substrate $n_s(\lambda_{tan})$, accounted for the substrate absorption by simultaneous solution of Eqs. 1 and 2 with respect to $n_s(\lambda_{tan})$ and $x_s(\lambda_{tan})$. All computations are carried out using original computational code developed by the authors.

II. Details of using the algorithm of the graphical method

Graphical method characterization can be performed by following the steps of an algorithm. In all cases of using a particular mathematical operation for consecutive λ_{tan}, the computation should start from the region of negligible film absorption. Therefore, when applied to chalcogenide film specimens with normal incidence $T(\lambda)$ spectra obtained by UV/visible/NIR spectrophotometer, the computation starts from the longest λ_{tan}, i.e. from max(λ_{tan}), and proceeds with the successively shorter wavelengths λ_{tan}.

Elucidating on the presentation from [5], the graphical method algorithm, and the respective computations we perform for characterizations of films, can be executed by following the next steps:

At step 1, the spectrum $T(\lambda)$ of the film on a substrate specimen is obtained and digitized. All three spectra we use have been obtained over spectral region 400-2500 nm, by a double beam UV/visible/NIR spectrophotometer Perkin-Elmer model Lambda-19, as reported in [4] and [5].

Two envelopes $T_+(\lambda)$ and $T_-(\lambda)$ are interpolated, at step 2, along the maxima and the minima tangential points λ_{tan} with $T(\lambda)$. Correspondingly, $T_+(\lambda_{tan})$ and $T_-(\lambda_{tan})$ are determined.

The optical constants $n_s(\lambda_{tan})$ and $x_s(\lambda_{tan})$ of the substrate are computed by solving the system of Eqs. 1 and 2, using available spectra $T_s(\lambda)$ and $R_s(\lambda)$ of the substrates, at step 3.

First approximations $\theta_1(\lambda_{tan})$ of the parameter θ and of the envelope $T_{u-}(\lambda_{tan})$ are computed by solving the system of Eqns. 3 and 4 whereat substituting $T_{u+}(\lambda_{tan}) = T_s(\lambda_{tan})$, i.e. assuming weak absorption in the film, at step 4.

Step 5 begins with preparing a plot including all points $[l/2(\lambda_{tan}), \theta_1(\lambda_{tan})]$. Thereafter, a linear regression line is drawn for $N_{\theta 1}$ points from this plot, visually suitable for linear approximation, for successive $l/2$ starting with $l/2 = 0$.

In the beginning of step 6 are determined the slope S of the regression line and an initial approximation m_{1a} of m_1, in accordance with Eq. 6. $\theta(\lambda_{tan})$ is calculated then for all λ_{tan}, from Eq. 6 written for these S and m_{1a}.

The envelope points $T_{u+}(\lambda_{tan})$ and $T_{u-}(\lambda_{tan})$ from the spectrum for the fictional specimen with uniform thickness $\bar{d}$ are computed, at step 7, by solving the system of Eqs. 3 and 4.

At step 8 is calculated a first approximation $n_1(\lambda_{tan})$ of the refractive index of the film, from Eq. 8.

A first approximation $d_1(\lambda_{tan})$ of the film thickness is calculated from Eq. 7, at step 9.

A first approximation d_{1a} of the average film thickness over the region of weak absorption in the film is determined, at step 10, by averaging $d_1(\lambda_{tan})$ for N_{d1} successive wavelengths λ_{tan}, counted from max(λ_{tan}), over which $d_1(\lambda_{tan})$ are positioned within an apparent tight range {min[$d_1(\lambda_{tan})$], max[$d_1(\lambda_{tan})$]} for this region. In case that there is no apparent max[$d_1(\lambda_{tan})$] or min[$d_1(\lambda_{tan})$], it is represented by d_1[max(λ_{tan})].

At step 11, interference order numbers $m_e(\lambda_{tan})$ are estimated from Eq. 5.

The exact order numbers $m(\lambda_{tan})$ represent rounded $m_e(\lambda_{tan})$, at step 12, taking into account that $m(\lambda_{tan})$ increases by 0.5 for successively decreasing λ_{tan}, being integer for every maximum of $T(\lambda)$, and half-integer for every minimum of $T(\lambda)$.

A second approximation $d_2(\lambda_{tan})$ of the film thickness is calculated from Eq. 5, at step 13.

The finalized average film thickness $\bar{d}$ is identical to the second approximation d_{2a} of the average film thickness, determined by averaging $d_2(\lambda_{tan})$ over the weak film absorption region, for N_{d2} successive wavelengths λ_{tan} over which $d_2(\lambda_{tan})$ are positioned within an apparent tight range {min[$d_2(\lambda_{tan})$], max[$d_2(\lambda_{tan})$]}, at step 14.

The refractive index $n(\lambda_{tan})$ of the film is also finalized, at step 15, by its calculation from Eq. 5.

The thickness variation Δd of the film is determined from the known value of the regression line slope S, at step 16.

The extinction coefficient $k(\lambda_{tan})$ or the absorbance $x(\lambda_{tan}) = \exp[-4\pi k(\lambda_{tan}) \bar{d} / \lambda]$ or of the film, can be computed at step 17, from an equation formulating $T_+(\lambda_{tan})$ [3].

III. Results from graphical method characterization of chalcogenide films

Three thin film specimens are investigated, each of them representing a chalcogenide film on a borosilicate glass substrate BDH-Superpremium with a thickness d_s = 1 mm. The specimen 1 contains a-$As_{40}S_{60}$ film prepared by chemical vapor deposition (CVD), providing relatively non-uniform thickness films. The specimen 2 contains a-$As_{40}S_{60}$ film deposited by thermal evaporation (TE) using a planetary rotary system, producing films with relatively uniform thickness. The specimen 3 contains a-GeS_2 film obtained by TE with oblique deposition in a static system, providing relatively non-uniform thickness films.

The normal incidence $T(\lambda)$ spectra of the specimens 1 and 2 were shown in [4], where the films were characterized by the envelope method [4]. The normal incidence $T(\lambda)$ spectrum of the specimen 3 was shown in [5], where the film was characterized by the graphical method.

Results from graphical method characterization of the film from the specimen 1, the specimen 2, and the specimen 3 are presented in Table 1, Table 2, and Table 3, respectively.

TABLE 1. MAIN RESULTS FROM GRAPHICAL METHOD CHARACTERIZATION OF a-$As_{40}S_{60}$ FILM PREPARED BY CHEMICAL VAPOR DEPOSITION

λ_{tan} (nm)	n_s	x_s	T_+	T_-	θ_1	θ	T_{u+}	T_{u-}	n_1	d_1 (nm)	m_e	m	d_2 (nm)	n
2080	1.487	0.9788	0.8687	0.6338	0.55	0.54	0.9057	0.6144	2.44	2559	5.97	6	2558	2.434
1923	1.493	0.981	0.8675	0.6378	0.57	0.57	0.9082	0.6162	2.443	2734	6.46	6.5	2558	2.438
1787	1.489	0.9825	0.8651	0.6422	0.60	0.60	0.9094	0.6183	2.434	2535	6.93	7	2570	2.440
1670	1.493	0.9833	0.8612	0.6445	0.63	0.63	0.9094	0.6181	2.439	2425	7.43	7.5	2567	2.443
1567	1.492	0.9826	0.8557	0.6431	0.67	0.66	0.9086	0.614	2.45	2466	7.96	8	2558	2.445
1477	1.491	0.9789	0.8472	0.6410	0.70	0.69	0.9043	0.6093	2.459	2431	8.47	8.5	2552	2.449
1397	1.493	0.9756	0.8379	0.6390	0.74	0.73	0.899	0.6046	2.470	2403	9.00	9	2545	2.453
1325	1.493	0.9736	0.8297	0.6371	0.78	0.76	0.8953	0.5999	2.480	2320	9.52	9.5	2537	2.455
1262	1.496	0.9727	0.8232	0.6357	0.80	0.79	0.894	0.5952	2.498	2273	10.07	10	2526	2.462
1204	1.496	0.9714	0.8188	0.6350	0.82	0.82	0.8957	0.5908	2.516	2169	10.63	10.5	2512	2.466
1150	1.499	0.9716	0.8150	0.6354	0.84	0.85	0.8983	0.5873	2.536	2256	11.22	11	2494	2.468
1102	1.498	0.9713	0.8116	0.6362	0.86	0.88	0.9015	0.584	2.552	2219	11.78	11.5	2483	2.472
1058	1.501	0.9719	0.8085	0.6382	0.88	0.91	0.9050	0.5817	2.569	2231	12.36	12	2471	2.477
1018	1.505	0.9731	0.8056	0.6405	0.90	0.94	0.9090	0.5795	2.586	2099	12.93	12.5	2460	2.482
980	1.502	0.9728	0.8033	0.6421	0.92	0.97	0.9152	0.5759	2.606	1973	13.53	13	2444	2.485
947	1.508	0.9754	0.8017	0.6439	0.93	1.00	0.9234	0.5718	2.639	2014	14.18	13.5	2423	2.494
914	1.507	0.9758	0.8009	0.6473	0.95	1.03	0.9324	0.5692	2.66	1908	14.81	14	2405	2.496
885	1.511	0.9782	0.8025	0.6519	0.95	1.06	0.946	0.5667	2.692	2459	15.47	14.5	2384	2.503
857	1.508	0.9832	0.8040	0.6603	0.98	1.09	0.9559	0.5688	2.694	2392	15.99	15	2386	2.508
833	1.510	0.9831	0.8035	0.6670	1.00	1.12	0.9642	0.5691	2.705	1716	16.52	15.5	2386	2.519
808	1.509	0.9857	0.8027	0.6700	1.02	1.15	0.9782	0.5634	2.742	1573	17.26	16	2358	2.522
786	1.510	0.9872	0.8021	0.6724	1.03	1.18	0.9962	0.5555	2.792	1538	18.07	16.5	2322	2.530
765	1.510	0.9881	0.8013	0.6756	1.04	1.21	1.0152	0.5476	2.842	1481	18.9	17	2288	2.537
745	1.509	0.9896	0.7997	0.6788	1.06	1.24	1.0349	0.539	2.893	1401	19.76	17.5	2253	2.543
727	1.509	0.9909	0.7978	0.682	1.08	1.27	1.0578	0.529	2.953	1173	20.67	18	2216	2.553
709	1.509	0.9922	0.7960	0.6846	1.10	1.30	1.0882	0.5156	3.030	1141	21.75	18.5	2164	2.559

$N_{\theta 1} = 5$, Eq. 6 → l/2 = 16.49θ – 8.96; $N_{d1} = 5$, $d_{1a} = 2544$ nm; $N_{d2} = 4$, $\overline{d} = d_{2a} = 2563$ nm; $\Delta d = 49.5$ nm

TABLE 2. MAIN RESULTS FROM GRAPHICAL METHOD CHARACTERIZATION OF a-$As_{40}S_{60}$ FILM THERMALLY EVAPORATED USING A PLANETARY ROTARY SYSTEM

λ_{tan} (nm)	n_s	x_s	T_+	T_-	θ_1	θ	T_{u+}	T_{u-}	n_1	d_1 (nm)	m_e	m	d_2 (nm)	n
2153	1.488	0.977	0.914	0.657	9.0E-5	0	0.914	0.657	2.313	1377	2.97	3	1396	2.319
1850	1.489	0.982	0.914	0.654	4.3E-5	0	0.914	0.654	2.323	1369	3.47	3.5	1394	2.325
1617	1.492	0.984	0.914	0.654	4.3E-5	0	0.914	0.654	2.326	1423	3.98	4	1390	2.323
1441	1.496	0.978	0.911	0.654	1.9E-5	0	0.911	0.654	2.326	1440	4.46	4.5	1394	2.328
1302	1.494	0.974	0.909	0.651	0.5E-5	0	0.909	0.651	2.328	1316	4.94	5	1398	2.338
1185	1.500	0.972	0.907	0.648	0.1E-5	0	0.907	0.648	2.344	1417	5.47	5.5	1390	2.340
1091	1.501	0.972	0.907	0.645	0.1E-5	0	0.907	0.645	2.350	1368	5.96	6	1393	2.351
1009	1.503	0.973	0.906	0.643	0.1E-5	0	0.906	0.643	2.358	1383	6.46	6.5	1391	2.355
941	1.507	0.975	0.906	0.641	0.1E-5	0	0.906	0.641	2.369	1354	6.96	7	1390	2.365
881	1.514	0.980	0.907	0.640	0	0	0.907	0.640	2.381	1576	7.47	7.5	1388	2.373
831	1.510	0.984	0.908	0.640	0	0	0.908	0.640	2.378	1518	7.91	8	1398	2.387
786	1.510	0.987	0.908	0.640	0.07	0	0.908	0.640	2.378	1410	8.37	8.5	1405	2.399
746	1.510	0.990	0.909	0.637	0.14	0	0.909	0.637	2.389	1434	8.86	9	1405	2.411
711	1.509	0.993	0.908	0.633	0.22	0	0.908	0.633	2.401	1476	9.34	9.5	1406	2.425
679	1.508	0.994	0.907	0.631	0.25	0	0.907	0.631	2.408	1503	9.81	10	1410	2.438
651	1.508	0.995	0.907	0.628	0.26	0	0.907	0.628	2.417	1404	10.27	10.5	1414	2.455
625	1.508	0.997	0.907	0.623	0.28	0	0.907	0.623	2.432	1409	10.76	11	1413	2.469
602	1.508	0.998	0.905	0.618	0.31	0	0.905	0.618	2.449	1481	11.25	11.5	1413	2.486
582	1.509	0.999	0.902	0.612	0.34	0	0.902	0.612	2.466	1445	11.72	12	1416	2.508
563	1.510	1.000	0.892	0.602	0.43	0	0.892	0.602	2.483	1260	12.20	12.5	1417	2.527
546	1.510	0.999	0.872	0.584	0.54	0	0.872	0.584	2.516	1617	12.75	13	1410	2.549
531	1.510	0.999	0.817	0.556	0.77	0	0.817	0.556	2.529	1040	13.17	13.5	1417	2.574
517	1.510	0.999	0.722	0.498	0.99	0	0.721	0.498	2.587	1659	13.84	14	1399	2.599
504	1.509	1.000	0.562	0.415	1.25	0	0.562	0.415	2.598	1002	14.25	14.5	1407	2.624
494	1.510	1.000	0.393	0.345	1.48	0	0.393	0.345	2.225	-384	12.46	15	1665	2.661

$N_{\theta 1} = 5$, Eq. 6 → l/2 = -19964θ + 1.84; $N_{d1} = 9$, $d_{1a} = 1383$ nm; $N_{d2} = 10$, $\overline{d} = d_{2a} = 1392$; $\Delta d = 0.02$ nm

TABLE 3. MAIN RESULTS FROM GRAPHICAL METHOD CHARACTERIZATION OF a-GeS_2 FILM OBTAINED BY THERMAL EVAPORATION

λ_{tan} (nm)	n_s	x_s	T_+	T_-	θ_1	θ	T_{u+}	T_{u-}	n_1	d_1 (nm)	m_e	m	d_2 (nm)	n
1847	1.491	0.9822	0.908	0.725	0.09	0.14	0.9095	0.7240	2.097	1673	3.53	3.5	1541	2.079
1621	1.491	0.9840	0.902	0.728	0.33	0.21	0.9052	0.7259	2.083	1590	4.00	4	1556	2.085
1444	1.493	0.9781	0.898	0.729	0.30	0.28	0.9035	0.7254	2.083	1602	4.49	4.5	1560	2.089
1305	1.494	0.9737	0.893	0.729	0.32	0.35	0.9015	0.7234	2.086	1510	4.98	5	1564	2.098
1185	1.500	0.9725	0.887	0.730	0.39	0.41	0.8988	0.7220	2.090	1630	5.49	5.5	1559	2.096
1088	1.502	0.9718	0.881	0.733	0.48	0.48	0.8964	0.7224	2.086	1659	5.97	6	1565	2.099
1011	1.503	0.9730	0.878	0.736	0.54	0.55	0.8978	0.7222	2.091	1423	6.44	6.5	1572	2.113
941	1.507	0.9753	0.876	0.737	0.59	0.62	0.9015	0.7192	2.111	1479	6.98	7	1560	2.118
881	1.514	0.9801	0.871	0.739	0.68	0.68	0.9021	0.7170	2.126	1466	7.51	7.5	1554	2.124
829	1.510	0.9844	0.866	0.739	0.77	0.75	0.9042	0.7118	2.142	1487	8.04	8	1548	2.132
784	1.510	0.9870	0.861	0.741	0.83	0.82	0.9065	0.7082	2.157	1530	8.57	8.5	1545	2.143
742	1.509	0.9895	0.855	0.745	0.91	0.89	0.9072	0.7067	2.163	1630	9.07	9	1544	2.147
707	1.509	0.9922	0.846	0.747	1.00	0.96	0.9047	0.7031	2.169	1343	9.55	9.5	1548	2.16
$N_{\theta 1} = 9$, Eq. 6 → $l/2 = 7.37\theta - 1.04$; $N_{d1} = 12$, $d_{1a} = 1556.5$ nm; $N_{d2} = 13$, $\bar{d} = d_{2a} = 1555$ nm; $\Delta d = 67.1$ nm														

In general, a small standard deviation SDd = SD[$d_2(1:N_{d2})$](nm), or a small relative error REd = $|\bar{d} - d_{1a}|/\bar{d}$ between the first and second approximation of the average film thickness, are indicative of accurate characterization. Therefore, the values of these quantities are shown in Figure 1, for the presented here and the previous characterizations [4] and [5] of the same films from the three specimens.

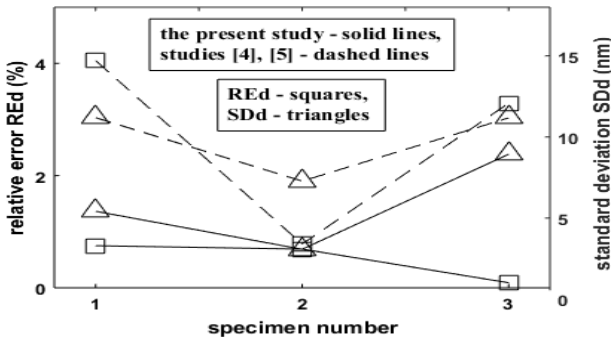

Fig. 1. Values of the thickness error metrics REd = $|\bar{d} - d_{1a}|/\bar{d}$ and SDd = SD[$d_2(1:N_{d2})$], obtained by graphical method characterization of the same 3 films, here and in [4], [5]

IV. CONCLUSIONS

From the results for the film from the second specimen, displayed in the bottom line of Table 2, is seen that its Eq. 6 contains unusual negative slope S of the linear regression line. It is apparently due to flawed measured spectra, since impossible inequality $T_+(\lambda) > T_s(\lambda)$ is observed at 850 nm < λ < 2500 nm. Since $T_+(\lambda) \sim x(\lambda)\, T_s(\lambda)$, this brings on the also impossible inequality $x(\lambda) > 1$ over this spectral region, implying negative film thickness, which leads to $S < 0$. Nevertheless, the characterization algorithm alleviates this inaccurate measurement induced problem, and the characterization is completed.

On the other hand, the final value of the smallest interference order number m_1 is exhibited by $m[\max(\lambda_{tan})]$, while its initial approximation m_{1a} is exhibited by the free term of Eq. 6. Therefore, $(m_{1a},m_1) = (8.96,6)$, (1.84,3), and (1.04,3.5), for the film specimen 1, specimen 2, and specimen 3 respectively. Correspondingly, although the initial approximation m_{1a} differs significantly from the final value m_1, for all three films, the characterization is completed. The results from the last two paragraphs indicate the significant inherent flexibility of the algorithm for characterization of films by the graphical method.

The obtained here value of $\bar{d}$ = 1555 nm, for the film from specimen 3, is outside the range of $\bar{d}$ = 1514 ± 30 nm for the same film, which has been measured by Dektak 3030 mechanical profilometer in [5], but within 2.7% from the center of this range.

Moreover, the data from Figure 1 show that both the standard deviation SD[$d_2(1:N_{d2})$], and the relative error $|\bar{d} - d_{1a}|/\bar{d}$ and are significantly smaller for the presented here three characterizations, compared to the two envelope method characterizations from [4], and the graphical method characterization from [5].

This indicates the higher accuracy of characterization achieved here, in comparison with these from [4-5], showing the merits of using substrate refractive index depending on its absorption, as we do it here, unlike in [3,5-6].

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Accurate Characterization of Film on Substrate Transmitting Specimens by the Envelope Method

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Abstract – **Higher accuracy is accomplished in characterization of thin film on substrate light transmitting specimens by the envelope method. This is a result of more accurate determination of the film thickness variation, based on minimization of film thickness error metrics. Three chalcogenide thin film specimens are characterized, and is shown that their thickness error metrics are better than those for previous characterizations of the same specimens.**

Keywords – **accurate optical characterization, thin film, envelope method, negative feedback**

I. INTRODUCTION

The use of thin light transmitting thin films in diverse engineering applications determines the importance of optical characterization of such films. A review on the methods for such optical characterization shows that the envelope method is amongst the most popular [1]. The envelope method is applicable to a specimen of a transmitting thin film on a substrate, by using its normal incidence interference transmittance spectrum $T(\lambda)$ due to the interference of light from both surfaces of the film, where λ is the wavelength of light. This method benefits from determination of tangential points $[\lambda_{tan}, T(\lambda_{tan})]$ between the spectrum $T(\lambda)$ and its two envelopes $T_+(\lambda)$ and $T_-(\lambda)$ drawn around the minima and the maxima of $T(\lambda)$, respectively.

The envelope method has been developed for a film with uniform thickness on a substrate, by Swanepoel [2]. Thereafter, he has expanded the method to films with non-uniform thickness d, described by the variation $\Delta d > 0$ of the film thickness with respect to the average film thickness $\overline{d}$, whereat $d = [\overline{d} - \Delta d, \overline{d} + \Delta d]$ [3].

The envelope method was advanced to account for the inevitable substrate absorption by Marquez et al. [4]. It was shown there that the two envelopes can be formulated as:

$$T_{t\pm}(\lambda, n, x, \Delta d, n_s, x_s) = \frac{(\tau_{af}\tau_{fs}\tau_{sa})^2}{\theta\sqrt{a_1^2 - b_1^2}} \tan^{-1}\left[\sqrt{\frac{a_1 \mp b_1}{a_1 \pm b_1}} \tan(\theta)\right] \quad (1)$$

where: $\dot{n}_s = n_s - jk_s$ is known; $\dot{n} = n - jk$, n and k are the refractive index and the extinction coefficient of the film; $x = \exp(-4\pi k\overline{d}/\lambda)$; $x_s = \exp(-4\pi k_s d_s/\lambda)$; $j = \sqrt{-1}$;

$$a_1 = (xx_s)^{-1} - (\rho_{af}\rho_{sa})^2 xx_s + \rho_{fs}^2(\rho_{af}^2 xx_s^{-1} - \rho_{sa}^2 x^{-1}x_s);$$

$$b_1 = 2\rho_{af}\rho_{fs}\rho_{sa}[\rho_{sa}x_s - (\rho_{sa}x_s)^{-1}]; \quad \theta = 2\pi n\Delta d/\lambda;$$

k and k_s are nullified in the expressions for the amplitude coefficients of transmission τ and reflection ρ, at the boundaries between all adjacent media, which become:

$$\tau_{af} = \frac{2}{n+1}; \tau_{fs} = 2\frac{n}{n+n_s}; \tau_{sa} = 2\frac{n_s}{n_s+1}$$

$$\rho_{af} = \frac{n-1}{n+1}; \rho_{fs} = \frac{n-n_s}{n+n_s}; \rho_{sa} = \frac{n_s-1}{n_s+1},$$

whereat the subscripts a, f, and s refer to air, film, and substrate, respectively.

Since the experimental envelopes $T_+(\lambda)$ and $T_-(\lambda)$ are described by Eq. 1, the following two equations:

$$T_{\pm}(\lambda_{\tan}) - T_{t\pm}(\lambda_{\tan}, n, x, \Delta d) = 0 \quad (2)$$

should be fulfilled for all tangential point wavelengths $\lambda_{\tan}$.

On the other hand, λ_{tan} satisfy the interference condition:

$$2n\overline{d} = m\lambda_{\tan} \quad (3)$$

where the interference order number $m \geq 0$ is an integer for λ_{tan} corresponding to a maximum of $T(\lambda)$, and a half-integer for λ_{tan} corresponding to a minimum of $T(\lambda)$. Furthermore, if n_{m} and $n_{\mathrm{m+0.5}}$ are the refractive indices for two tangential point wavelengths λ_m and $\lambda_{m+0.5}$, corresponding to adjacent extrema, it follows from Eq. 3 that the film thickness is:

$$d(\lambda_m) = \frac{\lambda_m\lambda_{m+0.5}}{4(\lambda_m n_{m+0.5} - \lambda_{m+0.5}n_m)} \quad (4)$$

A problem with such characterization is the lack of a stringent approach for determination the thickness variation Δd [3], resulting in ambiguity of its value. For some films, the dependence $\Delta d(\lambda_{tan})$ has a plateau, which has been used as an approximation of Δd [4]. Our new observations show though that such a plateau is not available for all films, and even when available it does not always give a relevant Δd.

The following approximations are used in the derivation of Eq. 1 and Eq. 3:

$$n > n_s >> k; n_s >> k_s; \lambda^2/(4n_s t_s) < 1nm; \theta < \pi/2 \quad (5)$$

In this paper is proposed a new approach for accurate optical characterization, based on accurate determination of Δd within the framework of the advanced envelope method [4], of a film on a substrate, using its spectrum $T(\lambda)$. This is realized by performing computations for different values of Δd, and minimization of a particular error metric for the characterization process. This approach is applied to characterization of three different chalcogenide thin film on glass substrate specimens. All computations are carried out using original computational code developed by the authors.

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II. THE NEW ALGORITHM FOR ACCURATE OPTICAL CHARACTERIZATION

The proposed here new algorithm for accurate characterization is based on the existing algorithm from [4]. In all steps based on solving Eqs. 2-4 for several λ_{tan}, the computation should start from the region of negligible film absorption, identified by larger film absorbance $x(\lambda_{tan})$. Therefore, when applied to chalcogenide film specimens, with $T(\lambda)$ spectra obtained by UV/visible/NIR spectrophotometer, the computation starts from the longest λ_{tan}, i.e. from max(λ_{tan}), and proceeds with the successively shorter wavelengths λ_{tan} [5]. The sequential steps of the algorithm and its respective computations are as follows:

At step 1 of the used algorithm, the spectrum $T(\lambda)$ of the film on a substrate specimen is obtained and digitized.

At step 2 are interpolated two envelopes $T_+(\lambda)$ and $T_-(\lambda)$ along the maxima and the minima tangential points λ_{tan} with $T(\lambda)$. Thereafter are determined $T_+(\lambda_{tan})$ and $T_-(\lambda_{tan})$, by finding local minima of the functions $|T_+(\lambda) - T(\lambda)|$ and $|T(\lambda) - T_-(\lambda)|$.

The optical constants $n_s(\lambda_{tan})$ and $x_s(\lambda_{tan})$ of the substrate are derived, at step 3, e.g. from the system of two equations for the transmittance $T_s(\lambda_{tan})$ and the reflectance $R_s(\lambda_{tan})$ of the substrate, as we do. Importantly, steps 4 to 13 are repeated until the error metric of the characterization process is minimized.

At step 4 is set the value of the thickness variation, starting with $\Delta d \approx 0$.

First approximation $n_1(\lambda_{tan})$ of the refractive index and $x_1(\lambda_{tan})$ of absorbance are computed, at step 5, by solving the system of two Eq. 2, whereat Δd_{1a} is known.

A first approximation $d_1(\lambda_{tan})$ of the film thickness is calculated from Eq. 4, at step 6.

At step 7, a first approximation d_{1a} of the average film thickness over the region of weak film absorption is determined by averaging $d_1(\lambda_{tan})$ for N_{d1} successive wavelengths λ_{tan}, counted from max(λ_{tan}), over which $d_1(\lambda_{tan})$ are positioned within an apparent tight range {min[$d_1(\lambda_{tan})$], max[$d_1(\lambda_{tan})$]} for this region.

At step 8, the interference order numbers $m_e(\lambda_{tan})$ are estimated from Eq. 3.

The exact order numbers $m(\lambda_{tan})$ represent rounded $m_e(\lambda_{tan})$, at step 9, taking into account that $m(\lambda_{tan})$ increases by 0.5 for successively decreasing λ_{tan}, being integer for every maximum of $T(\lambda)$, and half-integer for every minimum of $T(\lambda)$.

A second approximation of the film thickness $d_2(\lambda_{tan})$ is calculated from Eq. 3, at step 10.

A second approximation d_{2a} of the average film thickness is determined, at step 11, by averaging $d_2(\lambda_{tan})$ over the weak film absorption region, for N_{d2} successive wavelengths λ_{tan} over which $d_2(\lambda_{tan})$ are positioned within an apparent tight range {min[$d_2(\lambda_{tan})$], max[$d_2(\lambda_{tan})$]}.

At this stage, the average film thickness d_{2a} might be inaccurate, due to an error in Δd. Minimizing an thickness error metric can be used though, for determining an accurate value of Δd. One such a metric is the standard deviation SD[$d_2(1:N_{d2})$] of $d_2(\lambda_{tan})$, for N_{d1} successive wavelengths λ_{tan} starting with max(λ_{tan}), which has been proposed in [2] for accurate characterization of uniform thickness films [2].

Our results show that another such a metric could be the relative error $|d_{2a}-d_{1a}|/d_{2a}$ between the first and second approximation of the average film thickness. Therefore, at step 12 are calculated the values of these two thickness error metrics.

In case that there is no global minimum for either of these metrics with respect to Δd, its value is changed at step 13. Initially, Δd(nm) is changed by a decade i.e. Δd = 10, 20, 30,… until a minimum is reached for these decadally applied metrics. Thereafter, Δd(nm) is changed successively by 1 nm units. After setting Δd in such a way, the algorithm execution is returned to step 5.

Reaching global minimum for both metrics provides finalized values for both the integer Δd and the average film thickness $\overline{d} = d_{2a}$, thereafter the execution continues with step 14. At this step is finalized the refractive index $n(\lambda_{tan})$ of the film, by its calculation from Eq. 3

At step 15, Eq. 2 for $T_+(\lambda_{tan})$ can be solved with respect to the extinction coefficient $k(\lambda_{tan})$ or the absorbance $x(\lambda_{tan})$ of the film.

Knowing that n(λ_{tan}) for most chalcogenide materials obey the Wemple-DiDomenico single-oscillator model [6], it can be verified at step 16 whether the dependence $(n^2-1)^{-1}$ versus (λ^{-2}) would be approximated by a straight line [7].

III. RESULTS FROM ACCURATE OPTICAL CHARACTERIZATION OF CHALCOGENIDE FILMS

Three thin film specimens are investigated, each of them representing a chalcogenide film on a borosilicate glass substrate BDH-Superpremium with thickness d_s = 1 mm.

The specimen 1 contains a-$As_{40}S_{60}$ film deposited by thermal evaporation in a planetary rotary system, producing films with relatively uniform thickness. The specimen 2 contains a-$As_{40}S_{60}$ film prepared by chemical vapor deposition, providing relatively non-uniform thickness films. The specimen 3 contains a-GeS_2 film obtained by thermal evaporation with oblique deposition in a static system, providing relatively non-uniform thickness films.

The spectrophotometrically measured $T(\lambda)$ spectra of the specimens 1 and 2 were shown in [4], where the films were characterized by the existing algorithm of the envelope method [4]. The spectrophotometrically measured $T(\lambda)$ spectrum of the specimen 3 was shown in [8], where the film was characterized by a graphical method.

The refractive index $n_s(\lambda_{tan})$ and the extinction coefficient $k_s(\lambda_{tan})$ of the substrate are obtained by solving the two equations for available measured transmittance spectrum $T_s(\lambda)$ and reflectance spectrum $R_s(\lambda)$ of the substrate.

New and accurate characterizations of the three films from the three specimens are performed here, using the algorithm described in Section II. All steps of this algorithm are included in an original compound computational code, which simplifies obtaining the characterization results.

The results from the new and accurate characterizations of the film from the specimen 1, the specimen 2, and the specimen 3 are shown in Table 1, Table 2, and Table 3, respectively, presented in a common format for film characterization by the envelope method [4] . The thickness

data $d_1(\lambda_{tan})$ and $d_2(\lambda_{tan})$ participating in the calculations of d_{1a} and $\bar{d}$ in Tables 1-3 are underlined.

TABLE 1. RESULTS FROM ACCURATE CHARACTERIZATION OF a-$As_{40}S_{60}$ FILM DEPOSITED BY THERMAL EVAPORATION

λ_{tan} (nm)	n_s	x_s	T_+	T_-	Δd_1 (nm)	n_1	d_1 (nm)	m_e	m	d_2 (nm)	n	x
2153	1.488	0.9765	0.9140	0.6570	0.0	2.299	1369	2.99	3	1405	2.307	1.0000
1850	1.489	0.9819	0.9141	0.6541	0.0	2.313	1366	3.50	3.5	1400	2.313	1.0000
1617	1.492	0.9840	0.9141	0.6540	0.0	2.318	1445	4.02	4	1395	2.310	1.0000
1441	1.496	0.9783	0.9114	0.6539	0.0	2.315	1461	4.50	4.5	1401	2.316	1.0000
1302	1.494	0.9736	0.9087	0.6512	0.0	2.315	1324	4.98	5	1406	2.325	1.0000
1185	1.500	0.9725	0.9074	0.6476	0.2	2.33	1421	5.51	5.5	1398	2.328	1.0000
1091	1.501	0.9718	0.9066	0.6454	0.2	2.337	1362	6.00	6	1400	2.338	1.0000
1009	1.503	0.9730	0.9060	0.6434	0.1	2.347	1369	6.52	6.5	1397	2.343	1.0000
941	1.507	0.9753	0.9057	0.6413	0.0	2.361	1322	7.03	7	1395	2.353	1.0000
881	1.514	0.9801	0.9066	0.6402	0.0	2.377	1529	7.56	7.5	1390	2.360	1.0000
831	1.510	0.9844	0.9076	0.6404	0.0	2.378	1481	8.02	8	1398	2.374	1.0000
786	1.510	0.9872	0.9084	0.6405	0.0	2.382	1374	8.49	8.5	1403	2.386	1.0000
746	1.510	0.9895	0.9087	0.6373	0.0	2.396	1380	9.00	9	1401	2.398	1.0000
711	1.509	0.9929	0.9080	0.6331	7.8	2.413	1438	9.51	9.5	1400	2.413	0.9986
679	1.508	0.9940	0.9073	0.6306	8.9	2.422	1462	9.99	10	1402	2.425	0.9975
651	1.508	0.9949	0.9071	0.6279	9.1	2.433	1346	10.47	10.5	1405	2.441	0.9973
625	1.508	0.9972	0.9070	0.6235	9.9	2.452	1359	10.99	11	1402	2.456	0.9960
602	1.508	0.9985	0.9055	0.6178	10.6	2.473	1424	11.51	11.5	1400	2.473	0.9943
582	1.509	0.9990	0.9024	0.6117	11.3	2.493	1380	12.00	12	1401	2.494	0.9922
563	1.510	0.9998	0.8923	0.6024	14.0	2.513	1199	12.51	12.5	1400	2.514	0.9832
546	1.510	0.9993	0.8723	0.5844	17.0	2.551	1543	13.09	13	1391	2.535	0.9660
531	1.510	0.9989	0.8169	0.5558	22.1	2.567	984	13.54	13.5	1396	2.560	0.9167
517	1.510	0.9991	0.7215	0.4982	24.4	2.631	1587	14.26	14	1376	2.585	0.8290
504	1.509	0.9998	0.5620	0.4149	23.6	2.644	360	14.70	14.5	1382	2.610	0.6734
494	1.510	1.0000	0.3929	0.3451	20.1	2.249	511	12.75	15	1647	2.647	0.4944
$\Delta d = 9$ nm , $N_{d1} = 19$, $d_{1a} = 1401$ nm , $N_{d2} = 20$, $\bar{d} = 1400$ nm												

TABLE 2. RESULTS FROM ACCURATE CHARACTERIZATION OF a-$As_{40}S_{60}$ FILM PREPARED BY CHEMICAL VAPOR DEPOSITION

λ_{tan} (nm)	n_s	x_s	T_+	T_-	Δd_1 (nm)	n_1	d_1 (nm)	m_e	m	d_2 (nm)	n	x
2080	1.487	0.9788	0.8687	0.6338	72.7	2.345	2735	6.10	6	2661	2.316	0.9768
1923	1.493	0.9810	0.8675	0.6378	69.7	2.344	2969	6.60	6.5	2667	2.320	0.9769
1787	1.489	0.9825	0.8651	0.6422	69.4	2.328	2764	7.05	7	2686	2.322	0.9749
1670	1.493	0.9833	0.8612	0.6445	68.0	2.327	2688	7.54	7.5	2691	2.325	0.9736
1567	1.492	0.9826	0.8557	0.6431	66.9	2.329	2813	8.04	8	2691	2.327	0.9710
1477	1.491	0.9789	0.8472	0.641	66.3	2.327	2796	8.53	8.5	2698	2.330	0.9684
1397	1.493	0.9756	0.8379	0.6390	65.8	2.326	2787	9.01	9	2703	2.334	0.9652
1325	1.493	0.9736	0.8297	0.6371	65.3	2.325	2694	9.50	9.5	2707	2.336	0.9615
1262	1.496	0.9727	0.8232	0.6357	64.1	2.331	2688	10.00	10	2707	2.342	0.9594
1204	1.496	0.9714	0.8188	0.6350	62.5	2.336	2542	10.50	10.5	2706	2.347	0.9590
1150	1.499	0.9716	0.8150	0.6354	60.9	2.344	2740	11.03	11	2698	2.348	0.9584
1102	1.498	0.9713	0.8116	0.6362	59.7	2.347	2701	11.53	11.5	2700	2.352	0.9584
1058	1.501	0.9719	0.8085	0.6382	58.5	2.351	2774	12.03	12	2700	2.357	0.9586
1018	1.505	0.9731	0.8056	0.6405	57.6	2.354	2685	12.52	12.5	2703	2.362	0.9586
980	1.502	0.9728	0.8033	0.6421	56.5	2.357	2461	13.02	13	2702	2.365	0.9597
947	1.508	0.9754	0.8017	0.6439	55.3	2.374	2667	13.57	13.5	2692	2.373	0.9604
914	1.507	0.9758	0.8009	0.6473	54.3	2.377	2498	14.08	14	2691	2.375	0.9628
885	1.511	0.9782	0.8025	0.6519	53.1	2.390	3870	14.62	14.5	2684	2.382	0.9669
857	1.508	0.9832	0.8040	0.6603	53.1	2.370	4492	14.97	15	2712	2.386	0.9678
833	1.510	0.9831	0.8035	0.6670	52.9	2.350	2541	15.27	15.5	2747	2.397	0.9724
808	1.509	0.9857	0.8027	0.6700	52.2	2.359	2404	15.80	16	2740	2.400	0.9731
786	1.510	0.9872	0.8021	0.6724	51.4	2.377	2546	16.36	16.5	2729	2.407	0.9757
765	1.510	0.9881	0.8013	0.6756	50.8	2.388	2677	16.90	17	2723	2.414	0.9787
745	1.509	0.9896	0.7997	0.6788	50.4	2.395	2897	17.40	17.5	2721	2.420	0.9802
727	1.509	0.9909	0.7978	0.6820	50.2	2.400	2211	17.87	18	2726	2.429	0.9821
709	1.509	0.9922	0.7960	0.6846	49.7	2.421	1490	18.48	18.5	2709	2.435	0.9836
693	1.508	0.9932	0.7942	0.6856	49.1	2.483	953	19.39	19	2651	2.444	0.9860
$\Delta d = 49$ nm , $N_{d1} = 17$, $d_{1a} = 2706$ nm , $N_{d2} = 18$, $\bar{d} = 2694$ nm												

TABLE 3. RESULTS FROM ACCURATE CHARACTERIZATION OF THERMALLY EVAPORATED a-GeS_2 FILM

λ_{tan} (nm)	n_s	x_s	T_+	T_-	Δd_1 (nm)	n_1	d_1 (nm)	m_e	m	d_2 (nm)	n	x
1847	1.491	0.9822	0.908	0.725	1.10	2.121	1624	3.58	3.5	1524	2.101	1.0000
1621	1.491	0.9840	0.902	0.728	37.9	2.111	1568	4.06	4	1536	2.107	1.0000
1444	1.493	0.9781	0.898	0.729	30.3	2.111	1583	4.56	4.5	1539	2.112	1.0000
1305	1.494	0.9737	0.893	0.729	29.6	2.114	1483	5.05	5	1543	2.121	1.0000
1185	1.500	0.9725	0.887	0.730	34.1	2.119	1626	5.58	5.5	1538	2.118	1.0000
1088	1.502	0.9718	0.881	0.733	39.1	2.113	1666	6.06	6	1545	2.122	1.0000
1011	1.503	0.9730	0.878	0.736	41.1	2.115	1401	6.52	6.5	1553	2.136	1.0000
941	1.507	0.9753	0.876	0.737	41.2	2.137	1468	7.08	7	1541	2.141	1.0000
881	1.514	0.9801	0.871	0.739	44.4	2.151	1471	7.61	7.5	1536	2.147	1.0000
829	1.510	0.9844	0.866	0.739	46.8	2.164	1555	8.14	8	1532	2.155	1.0000
784	1.510	0.9870	0.861	0.741	47.8	2.173	1704	8.64	8.5	1533	2.166	1.0000
742	1.509	0.9895	0.855	0.745	49.1	2.165	2071	9.10	9	1542	2.170	0.9988
707	1.509	0.9922	0.846	0.747	50.7	2.149	1615	9.48	9.5	1563	2.183	0.9929
Δd = 49 nm , N_{d1} = 11 , d_{1a} = 1559 nm , N_{d2} = 12 , $\bar{d}$ = 1539 nm												

For comparative purposes, in Figure 1 are presented data about the thickness error metrics REd = $|\bar{d} - d_{1a}|/\bar{d}$ (%) and SDd =SD[$d_2(1:N_{d2})$](nm), obtained from the characterization of the same 3 films by the proposed here algorithm and the existing algorithms from [4] and [8]. For each one of these films, the values of these metrics are calculated adopting the values of N_{d1} and N_{d2} shown in its respective Table 1-3.

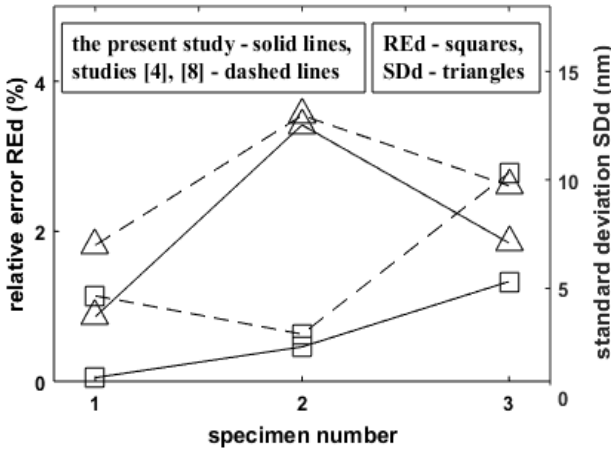

Fig. 1. Values of the thickness error metrics REd = $|\bar{d} - d_{1a}|/\bar{d}$ and SDd = SD[$d_2(1:N_{d2})$], obtained from the characterization of the same 3 films by the proposed here algorithm and the existing algorithms from [4] and [8]

IV. CONCLUSION

A new approach is proposed for accurate characterization of a thin light transmitting film on a substrate, based on accurate determination of the film thickness variation Δd by minimization of thickness error metrics in the envelope method.

The data from Figure 1 show that both $|\bar{d} - d_{1a}|/\bar{d}$ and SD[$d_2(1:N_{d2})$] thickness error metrics have smaller values for the presented here characterizations compared to the previous ones, for all three films. This indicates higher accuracy of the present characterizations, compared to those from [4] and [8]. Since the characterizations of the films from specimens 1 and 2 are performed by the envelope method, both here and in [4], the higher characterization accuracy achieved here is due to the more accurate determination of Δd. Notably, the obtained here value of $\bar{d}$ = 1539 nm, for the film from specimen 3, is within the range of $\bar{d}$ = 1514 ± 30 nm for the same film, which has been measured by Dektak 3030 mechanical profilometer in [8].

Besides, for the films from specimens 1 and 2, the integer values of Δd for which the metrics $|\bar{d} - d_{1a}|/\bar{d}$ and SD[$d_2(1:N_{d2})$] have minima are identical. Only for the film from specimen 3, the metric $|\bar{d} - d_{1a}|/\bar{d}$ predicts Δd = 50 nm, while the metric SD[$d_2(1:N_{d2})$] predicts Δd = 49 nm. Moreover, the obtained here results indicate that minimizing either of the metrics SD[$d_2(1:N_{d2})$] or $|\bar{d} - d_{1a}|/\bar{d}$ can be used as a tool for accurate characterization by the envelope method.

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Optimization of Nonlinear Figure-of-Merits of Integrated Power MOSFETs in Partial SOI Process

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Abstract – **State-of-the-art power semiconductor industry uses figure-of-merits (FOMs) for technology-to-technology and/or device-to-device comparisons. However, the existing FOMs are fundamentally nonlinear due to the nonlinearities of the parameters such as the gate charge and the output charge versus different operating conditions. A systematic analysis of the optimization of these FOMs has not been previously established. The optimization methods are verified on a 100 V power MOSFET implemented in a 0.18 μm partial SOI process. Its FOMs are lowered by 1.3-18.3 times and improved by 22-95 % with optimized conditions of quasi-zero voltage switching.**

Keywords – **Figure of Merit, Gate Charge, Output Charge, Power MOSFET, Silicon-on-Insulator**

I. Introduction

One of the main challenges for state-of-the art very high frequency (VHF, 30-300 MHz) converters to be effectively used in industrial products is the selection of active components, i.e. power semiconductors [1]. For discrete power devices, the Wide Band Gap (WBG) semiconductors such as GaN and SiC are of consideration [2]. For integration of power devices with control and driver circuits on the same die, one promising way is to use Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) at different voltage domains in Silicon-on-Insulator (SOI) processes [3].

Conventionally, different transistor technologies are compared quantitatively using figure-of-merits (FOMs) [4]. Another usage of the FOMs is to evaluate the overall performance of a power device for a switching application [5]. The technology or device that has a lower FOM index value is deemed to have a better performance. The early-developed FOM such as Baliga FOM (BFOM) is solely based on the conduction loss minimization [6], and therefore does not apply to high frequency applications where the switching losses are not negligible. As technologies keep developing with emerging devices, different forms of FOMs are proposed in [4], [5], [7], [8]. However, recent researches show that these FOMs are not consistently used [5], [9]. This is because the FOMs typically consist of trade-off parameters such as on-resistance and gate charge (or certain parts of the gate charge), and these contributing parameters depend on the specific operating conditions. As a result, the FOMs are fundamentally nonlinear and application-dependent on voltage and current conditions. A systematic analysis to optimize the nonlinear FOMs has not been previously established, but it is needed to fully explore the performance potentials of the integrated power MOSFETs, especially for partial SOI processes. In Section II, different evaluation methods are reviewed, and the most suitable test circuit for deriving FOMs is selected and implemented. In Section III, the nonlinearities of the gate charge and its different sub-components are analyzed. In Section IV, the FOMs are then synthesized by using the gate charge and other corresponding parameters. Optimization methods of the FOMs versus specific operating conditions are summarized and discussed. Section V concludes the paper.

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II. Selection and Implementation of Test

Before composing the FOMs of a power MOSFET, the key parameters such as the gate charge and its sub-components have to be known. The first way to obtain various charge parameters is to calculate the integration of the parasitic capacitances as a function of an operating voltage such as the drain-source voltage [4], [10], [11]. However, the calculated results inherently lead to errors. These errors come from the fact that the parasitic capacitances depend on not only the drain-source voltage but also the gate-source voltage [3], which is not taken into account as a variable for the integration calculation. Note that the parasitic capacitances themselves do not provide direct and accurate device-to-device comparisons [12], e.g. a device with a higher capacitance value in [13] switches faster than another device with a lower capacitance value. In addition, a device with a higher on-resistance value in [14] shows a better overall efficiency for a converter, compared to another device with a lower on-resistance value. Therefore, a more accurate way to obtain the gate-charge parameters is needed, particularly for designing a gate-driver circuit [15] as well as calculating the FOMs.

The second way is to simulate the gate-charge behavior during switching transients. There is no standard test circuit for this, and different configurations are compared for choosing the most appropriate test circuit for the purpose of composing the FOMs. Some possible test circuits for evaluating the gate-charge behavior in the transistor turn-on process are shown in Fig. 1. The simplest configuration is to use a resistive load [5], [16], [17], as shown in Fig. 1(a). The configuration that uses a clamped inductive load [18]-[20] is shown in Fig. 1(b). The same circuit in Fig. 1(b) can be reused for a double pulse test (DPT) circuit. By

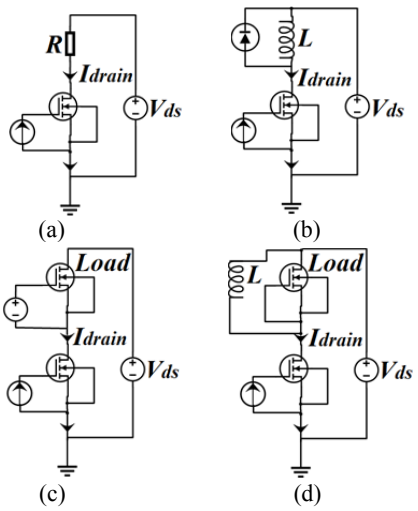

Fig. 1. Several test circuits for gate charge. (a) Resistive load. (b) Clamped inductive load. (c) Active load (simplified bias circuit). (d) Active load combined with an inductive load.

replacing the current source with a voltage-pulse source [21], the transistor turn-on and turn-off energy losses are measured, instead of the gate-charge parameters. For both test circuits in Fig. 1(a) and (b), the voltage transition and current transition occur simultaneously when charging the gate of the transistor. As a result, the sub-components of the gate charge cannot be accurately extracted from the gate-charge curve. Therefore, these test circuits cannot be used for deriving the FOMs that are composed of sub-components of the gate charge.

The configuration that uses an active load [13], [22], [23] is shown in Fig. 1(c) with a simplified bias circuit for the load. Another alternative test circuit is to use a gate-source-shorted active load combined with an inductive load [24], as shown in Fig. 1(d). For both test circuits in Fig. 1(c) and (d), the gate-charge curves are affected by the parasitic capacitances of the active loads as well as the device under test (DUT). Therefore, the resulting gate charge cannot be accounted for solely by the DUT.

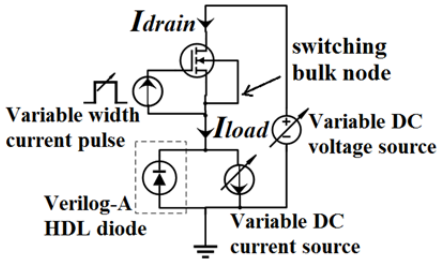

Fig. 2. Selected test circuit for gate charge (for deriving FOMs).

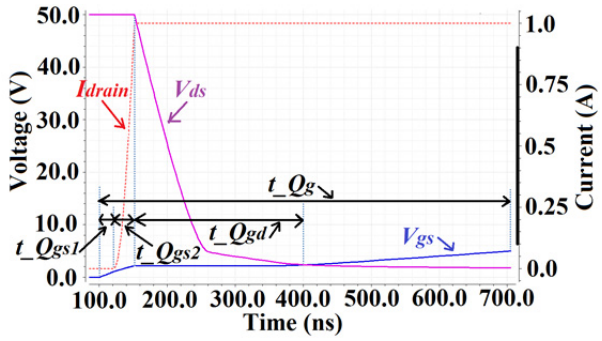

Fig. 3. Simulated transient waveforms and naming conventions.

The principle of the switching power-pole configuration [25] that uses a transistor and a diode is adopted and used for the purpose of deriving different FOMs. With the setup shown in Fig. 2, the voltage and current transitions are separated apart, which results in clear definitions of the sub-components of the gate charge. Provided that the diode is ideal, it is basically equivalent to interchange the positions of the power MOSFET and the load part of the circuit [12], [26]. The bulk terminal of the power MOSFET is connected to the on-chip switching node. This can be done by utilizing the vertical and horizontal dielectric isolation of a partial SOI process. The diode is implemented using the Verilog-A Hardware Description Language (HDL), and it is deliberately modeled with no reverse current and no forward voltage drop. The drain current I_{drain} is always equal to the load current I_{load}.

The DUT is a 100 V power MOSFET implemented in a 0.18 µm partial SOI process with a die area of 0.5276 mm^2. The maximum operating gate-source voltage is 5.5 V. The HiSIM-HV models that are provided by the process foundry are used, which are complete surface-potential-based models based on the drift-diffusion theory [27]. In contrast, the model that is conventionally from a discrete-transistor manufacturer such as [22] uses the most basic Schichman-Hodges model, which is often used for initial manual analysis without considering mobility degradation and an inaccurate model for sub-micron technologies [28]. Using the setup in Fig. 2, the parasitic resistance and/or inductance at the gate terminal do not affect the gate-charge results because the constant-amplitude current pulse is used. The parasitic inductance at the source terminal causes slight errors due to the resulting ringing of the drain current and the drain-source voltage. The results especially for the sub-components of the gate charge are most affected by the parasitic resistance at the source terminal, which is equivalent to adding an extra resistive load to the DUT, as previously discussed for Fig. 1(a).

The simulated transient waveforms are shown in Fig. 3. A current pulse of 1 mA is applied to the gate at 100 ns. The current pulse has a variable pulse width so that the gate-source voltage can be charged to different voltage potentials. The naming conventions are also shown in Fig. 3 and defined as follows: the time interval t_Q_{gs1} starts (t_Q_g starts) when the gate-source voltage V_{gs} starts to increase (i.e. at 100 ns when the current pulse to the gate is applied). The time interval t_Q_{gs2} starts (t_Q_{gs1} ends) when the drain current I_{drain} starts to increase. The time interval t_Q_{gd} starts (t_Q_{gs2} ends) when the drain-source voltage V_{ds} starts to decease. The time interval t_Q_g ends when the final-state (i.e. the state at the end point of the gate-charge event) V_{gs} is reached. The end point of t_Q_{gd} generally has no strict definition, and it is often stated as the point when the final-state V_{ds} or the final-state drain-source resistance R_{ds} (provided that the final-state V_{gs} is high enough to turn the transistor on, the final-state R_{ds} is also called on-resistance) is reached [5], [13], [16], [20], [23], [26]. In fact, both during and after the time interval t_Q_{gd}, V_{gs} still continuously increases (slightly), and the resulting V_{ds} (thus R_{ds}) keeps decreasing, until the final-state V_{gs} is reached. In this paper, the end point of t_Q_{gd} is defined as the intercept point of the extended lines of the V_{gs} curves during and after the time interval t_Q_{gd}.

After the time intervals are obtained, the corresponding charges are calculated as the time intervals multiplied by the gate-charge current. The time interval t_Q_{gs2} multiplied by 1 mA gives so-called Q_{gs2}. The time interval t_Q_{gd} multiplied by 1 mA gives so-called Q_{gd}. The time interval t_Q_g multiplied by 1 mA gives the total gate-charge Q_g.

III. Nonlinearities of Gate Charge

Using the evaluation methods in the previous section, the nonlinearities of the total gate-charge Q_g and its sub-components Q_{gd} and Q_{gs2} versus different operating conditions are shown in Fig. 4. The equivalent R_{ds} is evaluated under the same conditions, and it is derived as the ratio of the final-state V_{ds} to the final-state I_{drain}.

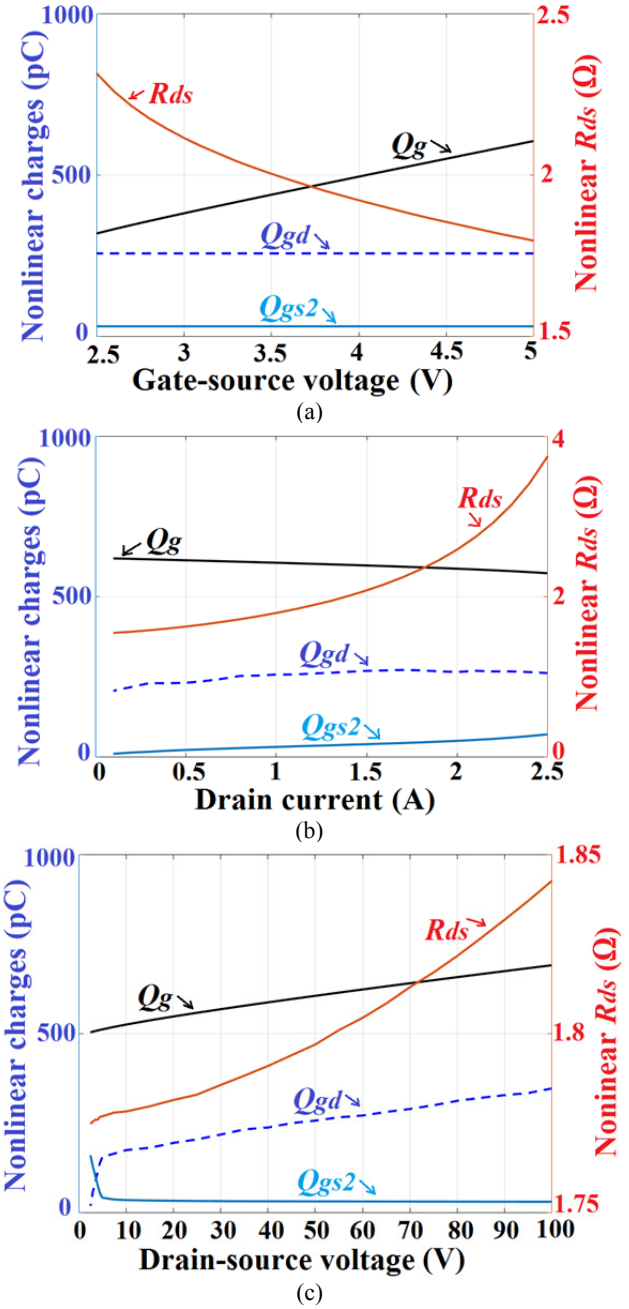

Fig. 4. Gate charge Q_g, its sub-components Q_{gd} and Q_{gs2}, and final-state R_{ds} (simulated). (a) Versus final-state V_{gs} (I_{drain} = 1 A, V_{ds} = 50 V). (b) Versus final-state I_{drain} (V_{gs} = 5 V, V_{ds} = 50 V). (c) Versus original-state V_{ds} (I_{drain} = 1 A, V_{gs} = 5 V).

IV. Optimization of Nonlinear FOMs

The FOMs in (1)-(4) are to be evaluated. FOM_{com1} is commonly used [5], [7]-[9]. FOM_{com2} is also widely accepted [5], [7]. $FOM_{hard\text{-}sw}$ and $FOM_{soft\text{-}sw}$ are proposed in [4] for hard-switching application and soft-switching application, respectively. The soft-switching here generally refers to zero-voltage switching (ZVS) for transistor turn-on transition and/or zero-current switching (ZCS) for transistor turn-off transition.

$$FOM_{com1} = R_{ds} \cdot Q_g \tag{1}$$

$$FOM_{com2} = R_{ds} \cdot Q_{gd} \tag{2}$$

$$FOM_{hard-sw} = R_{ds} \cdot \left(Q_{gd} + Q_{gs2}\right) \tag{3}$$

$$FOM_{soft-sw} = R_{ds} \cdot \left(Q_g + Q_{oss}\right) \tag{4}$$

The output charge Q_{oss} in (4) is analyzed as follows: for

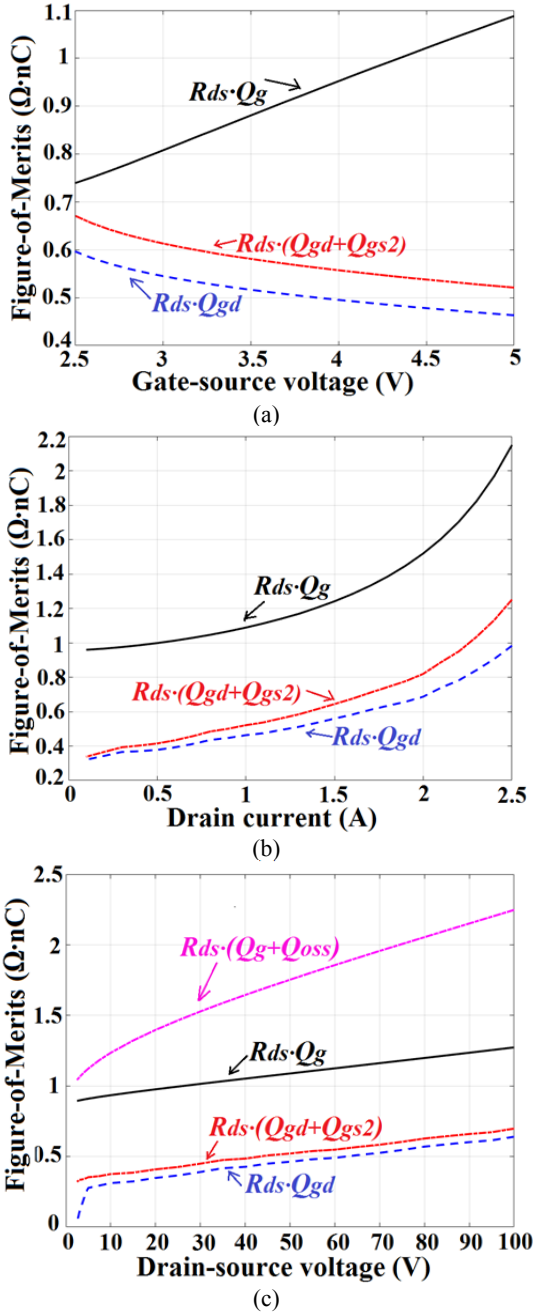

Fig. 5. Nonlinear FOMs (simulated). (a) Versus final-state V_{gs}. (b) Versus final-state I_{drain}. (c) Versus original-state V_{ds}.

TABLE 1. OPTIMIZATION OF NONLINEAR FOMS

Same as in Fig. 5	Best-case FOM vs. Worst-case FOM FOM is lowered: by times (by percentage)			
	FOM_{com1}	FOM_{com2}	$FOM_{hard\text{-}sw}$	$FOM_{soft\text{-}sw}$
V_{gs}	1.5 (32 %)	1.3 (22 %)	1.3 (22 %)	N/A
I_{drain}	2.2 (55 %)	3.0 (67 %)	3.7 (73 %)	N/A
V_{ds}	1.4 (30 %)	18.3 (95 %)	2.2 (54 %)	2.2 (54 %)

the transistor turn-off process, the output capacitance of the power MOSFET is charged to the supply voltage by only a portion of the load current. Therefore, it is difficult to dynamically determine Q_{oss} during the switching transients. Instead, Q_{oss} is estimated with the transistor in the off-state. The gate, source, and bulk terminals are shorted to ground, and the output-charge current is applied to the drain terminal. For the same reason, Q_{oss} (thus $FOM_{soft\text{-}sw}$) is only evaluated versus the drain-source voltage V_{ds}.

The FOMs in (1)-(4) are then derived versus different operating conditions, with the results shown in Fig. 5. The results are also quantitatively summarized in Table 1, versus the same operating conditions as in Fig. 5.

First, the contradicting trends of FOM_{com1} and FOM_{com2} are observed in Fig. 5(a). Another trade-off is between the final-state R_{ds} and the total gate-charge Q_g, as shown in Fig. 4(a). Second, all FOMs in Fig. 5(b) are dominated by R_{ds}. The equivalent R_{ds} increases for high I_{drain} values, due to the quasi-saturation effects and the drain current compression effects [29]. This means that the transistor starts to leave the linear region. Third, Q_{gd} in Fig. 4(c), which dominates FOM_{com2} in Fig. 5(c), quickly vanishes when the original-state (i.e. the state at the start point of the gate-charge event) V_{ds} has a low value (comparable to the V_{gs} values during the time interval t_Q_{gd}). This occurs when the transistor is in the quasi-saturation region before the gate-charge event, with quasi-zero voltage switching. In contrast, if the transistor is forced to be in the linear region, which is closer to the real ZVS, it may not be able to deliver the required final-state I_{drain} or it can deliver the current only after the time interval t_Q_{gd}. Therefore, the operation of the transistor is optimal in the quasi-saturation region rather than deeply in the linear region before the gate-charge event. The maximum improvement of 95 % (theoretically 100 %) is achieved for FOM_{com2}. It indicates that the power MOSFET is suitable for resonant and soft-switching converters (quasi-ZVS is preferred to ZCS).

V. CONCLUSION

A systematic analysis of the optimization of the nonlinear FOMs is performed for a 100 V power MOSFET implemented in a 0.18 µm partial SOI process. The FOMs (compared to the worst-case non-optimized FOMs) are lowered by 1.3-18.3 times and improved by 22-95 % with optimized quasi-zero voltage switching conditions.

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Mathematical Model of an Electronic Converter for Charging of Energy Storage Elements

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Abstract – **In the following paperwork a mathematical model of an electronic converter for charging energy storage elements has been created. The model is verified with simulation and experimental studies. The proposed circuit can be used for charging and voltage equalization over series connected energy storage elements – supercapacitors. The circuit allows modularity.**

Keywords – **Charging supercapacitor, model, voltage equalization.**

I. Introduction

To build a supercapacitor battery, the separated supercapacitor cells must be connected in series or in parallel. To equalize the voltage over the series connected cells different kinds of passive and active methods should be used [1, 2]. One active method for voltage equalization is by using resonant converters with special output circuits [3, 4].

II. Proposed Circuit for Charging and Balancing

Figure 1 shows the circuit for charging and voltage equalization over series connected supercapacitors.

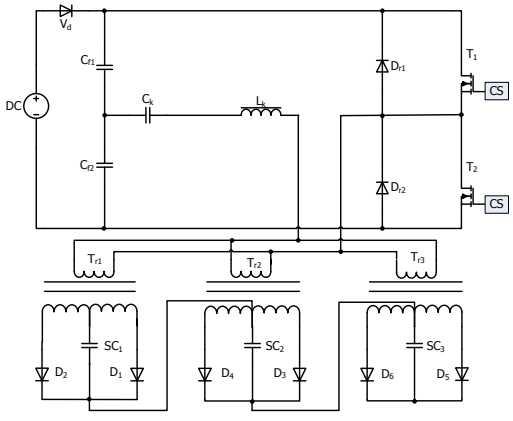

Fig. 1. Proposed circuit

The new in this circuit is the ability of modularity. N – number of modules can be used, made of separated transformers and connected to the rectifiers which charge the energy storage elements. The primary windings of the separated transformers are connected in parallel.

III. Circuit Modeling

A. Simulation results

A simulation model, based on the circuit from figure 1 for charging and voltage equalization over two series connected supercapacitor cells has been made.

The supercapacitors are presented with their equivalent circuit made of series connected resistance (Rsc1 and Rsc2) and the capacitors (Ccs1 and Csc2) which simulate the process of charging and discharging of the supercapacitor. During the simulation study different initial values of the voltage over the supercapacitors are given. The capacities of the studied supercapacitors are equal.

The transformers include one primary winding and two secondary windings. The transformation ratio between the windings is 1:1:1.

Similar simulation model is reviewed in [5].

The studies are carried out for two series connected supercapacitors with equal capacities but charged to different initial voltage over them.

Figure 2 shows the charging current through the two cells – I(Rsc1) and I(Rsc2) in the beginning of the charging process. In the beginning SC2 is charged to the highest voltage compare to SC1. Thus initially the charging current through supercapacitor one – SC1 is the highest.

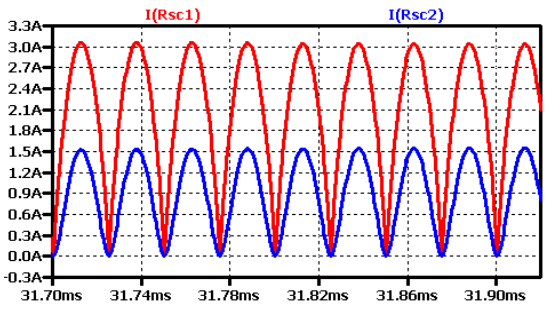

Fig. 2. Charging current in the beginning of the charging process

Figure 3 presents the voltage over the two supercapacitor cells. V(n015) is the voltage over SC1 and V(N017,N015) is the voltage over SC2. Despite of the significant difference between the initial values of the voltage over the two cells, in the end of the charging process the voltage over the two cells is equalized.

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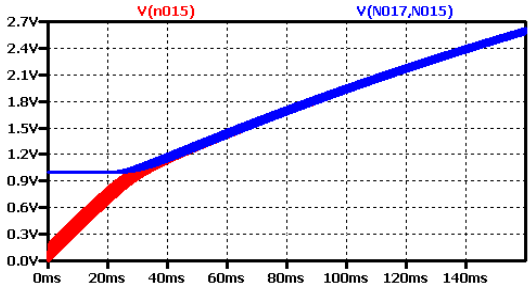

Fig. 3. Voltage over the two cells

Figures 4 and 5 shows the currents through the primary windings of the two transformers – I(L1) is the current through the primary winding of the transformer from the first unit and I(L4) is the current through the primary winding of the transformer from the secondary unit.

In the beginning of the charging process the two supercapacitors are charged to different initial voltage over them. Thus the current through the secondary winding of the transformer connected to the cell, charged to the highest voltage, does not flow. The current through the primary windings in this moment are shown on figure 4.

After the voltage over the two cells is equalized, through the primary windings of the transformers flow equal current (figure 5).

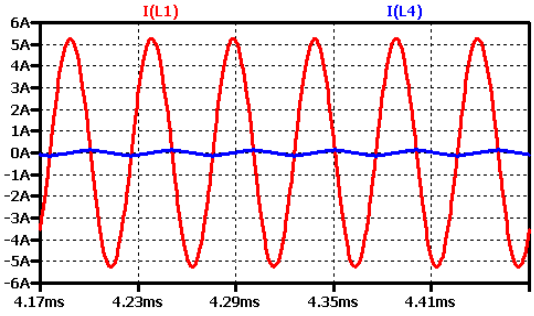

Fig.4. Current through the primary windings in the beginning of the charging process

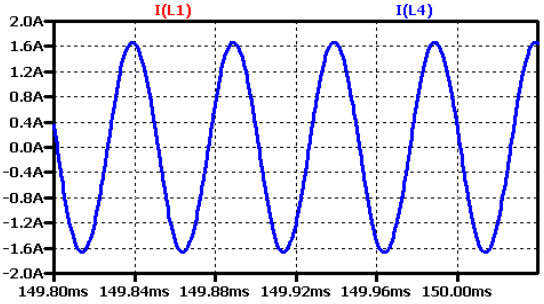

Fig.5. Current through the primary windings in the end of the charging process

B. Mathematical model

Figure 6 shows the circuit of the elements connected to the diagonal of inverter. This circuit is used for the purposes of the analysis. From mathematical point of view the change of the structure can be considered like change of the sign of U_d [6]. This happens in the following way. In the beginning of the half period while T_1 is on, the sign of U_d is positive. In the end of the half period, while D_{r2} is on the sign of U_d is negative. In the following period, while T_2 is on, the sign of U_d is still negative. When D_{r1} is on, the sign of U_d is positive. In the next period this repeats. For the circuit of figure 6 this is record $\pm U_d$.

The created model is valid for bridge and half – bridge circuit. In the case of half-bridge circuit $\pm U_d$ is replaced with $\pm U_d/2$.

A case with two inverter transformers is reviewed. The primary windings of these transformers are connected in parallel and the elements charged by the rectifiers, are connected in series.

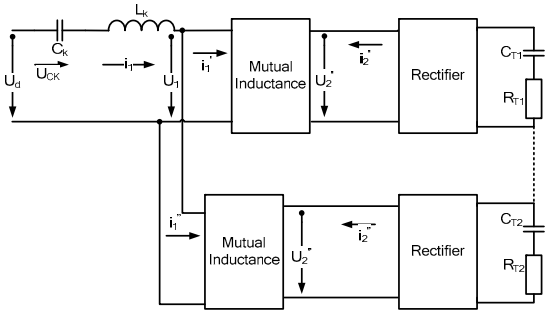

Fig. 6. Block diagram of the elements in the diagonal of the inverter

In the studied case the transformer has the following equivalent circuit (figure 7).

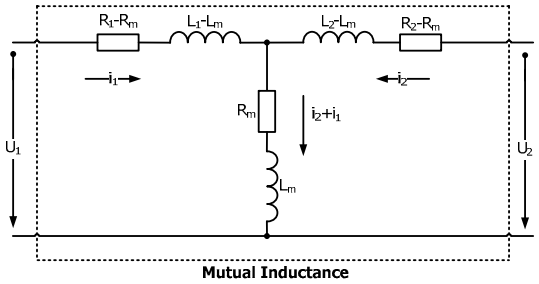

Fig. 7. Equivalent circuit of the transformer

The equations which model the changes of the current and voltage in the transformer are:

$$(R_1 - R_m)i_1 + (L_1 - L_m)\frac{di_1}{dt} + R_m(i_1 + i_2) + L_m\frac{d(i_1 + i_2)}{dt} = U_1 \quad (1)$$

$$(R_2 - R_m)i_2 + (L_2 - L_m)\frac{di_2}{dt} + R_m(i_1 + i_2) + L_m\frac{d(i_1 + i_2)}{dt} = U_2$$

After transformations the system is:

$$L_1\frac{di_1}{dt} + L_m\frac{di_2}{dt} = -R_1 i_1 - R_m i_2 + u_1 \quad (2)$$

$$L_m\frac{di_1}{dt} + L_2\frac{di_2}{dt} = -R_m i_1 - R_2 i_2 + u_2$$

For consolidation of the description for each output of the circuit from figure 6, similar names for the output current and voltage are used. The current and the voltage for the first transformer are named with indexes "prim". The current and the voltage for the second transformer are named with indexes "second". For example the charging current for the first section of the supercapacitor stack is i_2' and for the second stack is i_2'' (figure 6). Each of the sections of the supercapacitors is represented with the value of the corresponding capacity – C_T and active resistance R_T.

The following systems of ordinary differential equations are obtained from the circuit of figure 6:

Differential equations describing the processes in the two mutual inductances:

$$
\begin{aligned}
L_1\frac{di_1^{'}}{dt}+L_m\frac{di_2^{'}}{dt}&=-R_1i_1^{'}-R_mi_2^{'}+U_1\\
L_m\frac{di_1^{'}}{dt}+L_2\frac{di_2^{'}}{dt}&=-R_mi_1^{'}-R_2i_2^{'}+U_2^{'}\\
L_1\frac{di_1^{''}}{dt}+L_m\frac{di_2^{''}}{dt}&=-R_1i_1^{''}-R_mi_2^{''}+U_1\\
L_m\frac{di_1^{''}}{dt}+L_2\frac{di_2^{''}}{dt}&=-R_mi_1^{''}-R_2i_2^{''}+U_2^{''}
\end{aligned}
\qquad (3)
$$

Differential equations describing the processes in the primary winding:

$$
\begin{aligned}
U_1&=\mp U_d-U_{CK}-L_k\frac{d(i_1^{'}+i_1^{''})}{dt}\\
C_K\frac{dU_{ck}}{dt}&=i_1^{'}+i_1^{''}
\end{aligned}
\qquad (4)
$$

Differential equations describing the processes in the two secondary windings:

$$
\begin{aligned}
U_2^{'}&=-sign(i_2^{'})i_2^{'}R_{T1}-sign(i_2^{'})U_{CT1}\\
C_{T1}\frac{dU_{CT1}}{dt}&=sign(i_2^{'})i_2^{'}\\
U_2^{''}&=-sign(i_2^{''})i_2^{''}R_{T2}-sign(i_2^{''})U_{CT1}\\
C_{T2}\frac{dU_{CT2}}{dt}&=sign(i_2^{''})i_2^{''}
\end{aligned}
\qquad (5)
$$

In the upper systems *sign(i)* is magnitude with value +1 or -1. It gives information for the sign of the current *i*.

After remodeling systems (3), (4) and (5) a generalized systems is obtained.

This new generalized system is presented in relative units (6). The voltage is divided to the voltage over the constant DC source – U_d. The current is divided to $U_dC_k\omega$.

The relative units are with index *"N"*.

$$
\begin{aligned}
(L_1+L_K)\frac{di_{1N}^{'}}{dt}+L_m\frac{di_{2N}^{'}}{dt}+L_K\frac{di_{2N}^{'}}{dt}&=-R_1i_{1N}^{'}-R_mi_{2N}^{'}\mp\frac{1}{\omega C_k}-\frac{U_{CKN}}{\omega C_k}\\
L_m\frac{di_{1N}^{'}}{dt}+L_2\frac{di_{2N}^{'}}{dt}&=-R_mi_{1N}^{'}-R_2i_{2N}^{'}-sign(i_2^{'})i_{2N}^{'}R_{T1}-sign(i_2^{'})\frac{U_{CT1N}}{\omega C_k}\\
(L_1+L_K)\frac{di_{1N}^{''}}{dt}+L_m\frac{di_{2N}^{''}}{dt}+L_K\frac{di_{N1}^{'}}{dt}&=-R_1i_{1N}^{''}-R_mi_{2N}^{''}\mp\frac{1}{\omega C_k}-\frac{U_{CKN}}{\omega C_k}\\
L_m\frac{di_{1N}^{''}}{dt}+L_2\frac{di_{2N}^{''}}{dt}&=-R_mi_{1N}^{''}-R_2i_{2N}^{''}-sign(i_2^{''})i_{2N}^{''}R_{T1}-sign(i_2^{''})\frac{U_{CT2N}}{\omega C_k}\\
\frac{dU_{ckN}}{dt}&=\omega i_{N1}^{'}+\omega i_{1N}^{''}\\
\frac{dU_{CT1N}}{dt}&=\omega\frac{C_k}{C_{T1}}sign(i_2^{'})i_{2N}^{'}\\
\frac{dU_{CT2N}}{dt}&=\omega\frac{C_k}{C_{T2}}sign(i_2^{''})i_{2N}^{''}
\end{aligned}
\qquad (6)
$$

Solving the equations is by using numerical methods in MatLab. The individual segments describing system (6) in MatLab are shown on figures 8a to 8d.

As a result of the calculation the voltage over the two cells is obtained (figure 9).

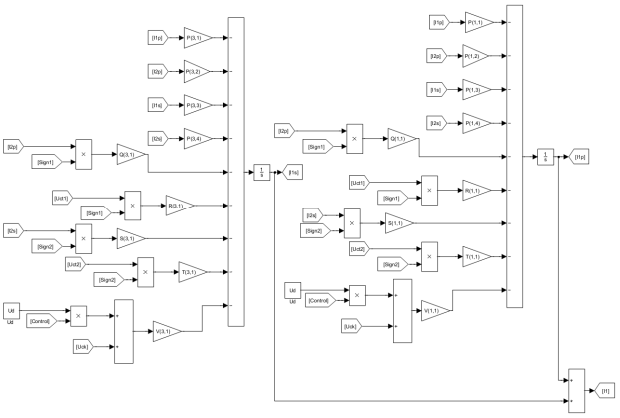

Fig. 8a. MatLab model

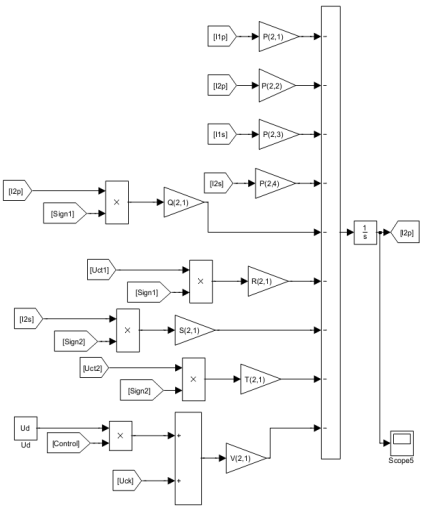

Fig. 8b. MatLab model

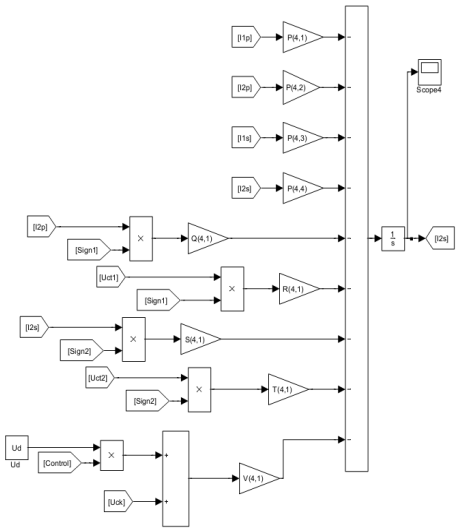

Fig. 8c. MatLab model

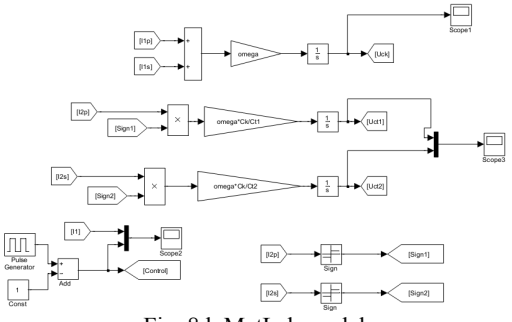

Fig. 8d. MatLab model

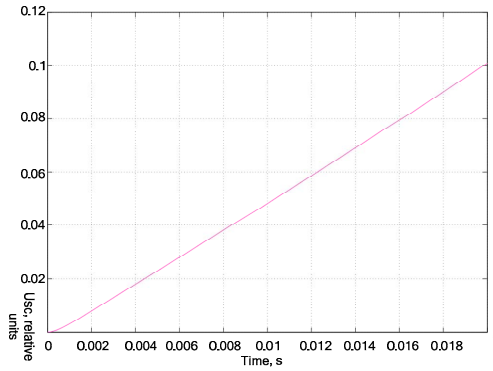

Fig. 9. Voltage over the two cells

Figure 10 presents the waveform of the current through the primary winding of the two transformers in relative units.

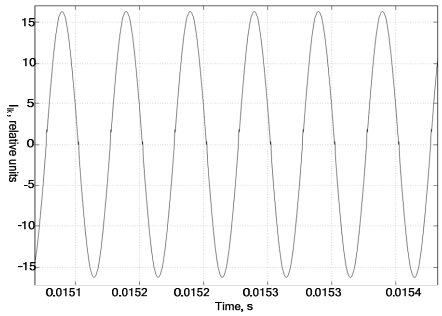

Fig. 10. Current through the two primary windings

IV. Experimental studies

Experimental studies over two units have been carried out, by using the circuit from figure 1. The two supercapacitors are with equal capacities but charged to different initial voltage over them.

The transformers are with transformer ratio 1:1:1 and inductance of the windings 100µH.

Figure 11 shows the waveforms of the current through the primary windings of the two transformers in the beginning of the charging process.

Figure 12 shows the charging current through the two cells in the beginning of the charging process.

Figure 13 shows the voltage over the two supercapacitor cells.

The results obtained from the mathematical and simulation model and the experimental studies are identical.

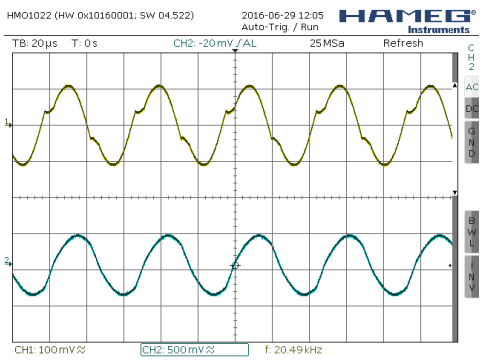

Fig. 11. Current through the primary windings

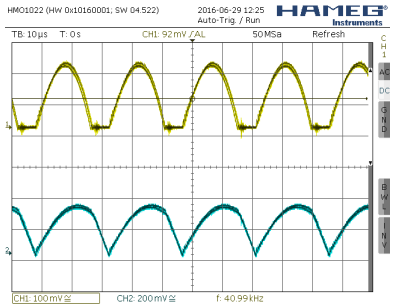

Fig. 12. Charging current through the two cells

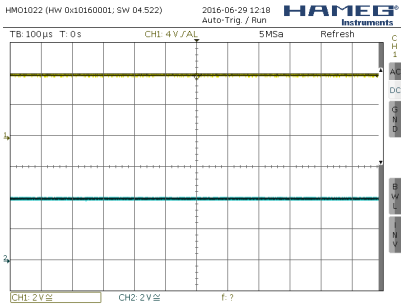

Fig. 13. Voltage over the two cells

V. Conclusion

A mathematical model of an electronic converter for charging supercapacitors has been created.

The results from the mathematical model are confirmed with simulation and experimental studies.

The description of the mathematical model in relative units allows obtaining results for different output conditions (different values of the elements and the power supplying voltage).

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Multiphase Converters for Charging of Energy Storage Elements

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Abstract – **The following paperwork presents a multiphase converter for charging of energy storage elements. Modular principle is implemented for the realization of the proposed circuit on the base of resonant inverter topology with reverse diodes and switching capacitor voltage limitation. The converter consists of six identical modules. Simulation examinations of are carried out verifying the circuit functionality. Results from the converter operation are presented. Main advantages of the proposed topology are higher output power capability and soft-switching (ZVS).**

Keywords – **Battery, charging station, model, resonant converter, supercapacitor, ZVS.**

I. Introduction

For the purposes of charging of energy storage elements (ESE), different types of converters are used. The most commonly used elements for energy storage are rechargeable batteries and supercapacitors [1, 2]. In order to provide fast charging of high-capacity batteries (for example, for electric vehicles), a high-power supply source and a converter are needed [3, 4]. High output power can be obtained from one high-power converter or from several converters supplying common load in parallel. The use of several converters is suitable when a galvanic insulation between the source and the load is necessary. In this way, several transformers with lower power may be used instead of one. Another advantage of the use of several converters is the opportunity to achieve system modularity. Thus, when a power capacity increase is needed, more identical modules may be added.

II. Proposed Circuit for Battery Charging

Fig.1 presents the block-diagram of the proposed converter. It consists of several converters (Conv.1-Conv.n), high-frequency transformers (Tr1-Tr-n) and a multiphase rectifier. The system is supplied by a DC power source. A rechargeable battery stack is used as an energy storage element. The multiphase converter can also be used for charging of supercapacitors [5, 6]. The converters (Conv.1-Conv.n) are resonant inverters with reverse diodes and voltage limitation across part of the resonant (switching) capacitor. By the use of multiphase rectifier, small battery stack current ripple is obtained. Other inverter circuits may also be used for realization of the modules (Conv.1-Conv.n), for example a resonant inverter circuit with reverse diodes.

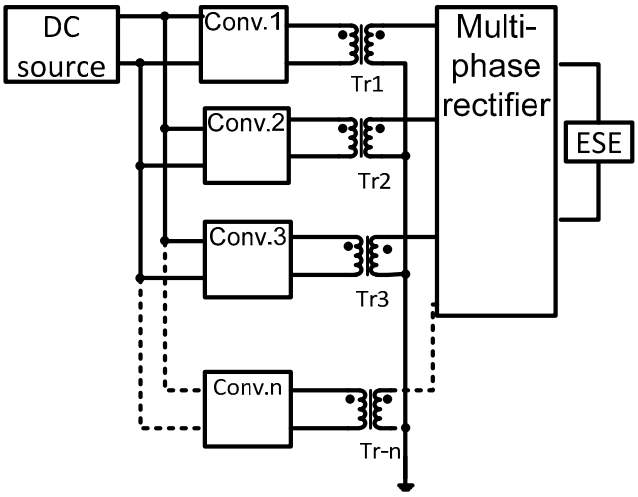

Fig. 1. Block-diagram of the proposed converter.

Fig. 2 presents the circuit of the examined converter. It consists of six identical half-bridge resonant inverters with separated power source. Six high-frequency transformers are connected to the outputs of the inverters. The control pulse sequences of the six units are phase shifted at an angle $\pi/6$ with respect to each other. The resonant inverters operate above the resonant frequency. The operation principle of the single unit is reviewed in [7]. The separate converters are designed in a way that during the ESE charging process conditions for the limiting diodes Dd1-Dd12 operation to occur. These diodes switch on when the voltage across the resonant capacitor part Ck1 – Ck6 equals Ud/2. By variation of the capacitor ratio Ck/Ce, the limitation diodes switching level may be varied, which results in variation of the consumed and charging currents of the multiphase converter. Different values of the charging current may be also obtained by variation of the transformers Tr1-Tr6 ratio.

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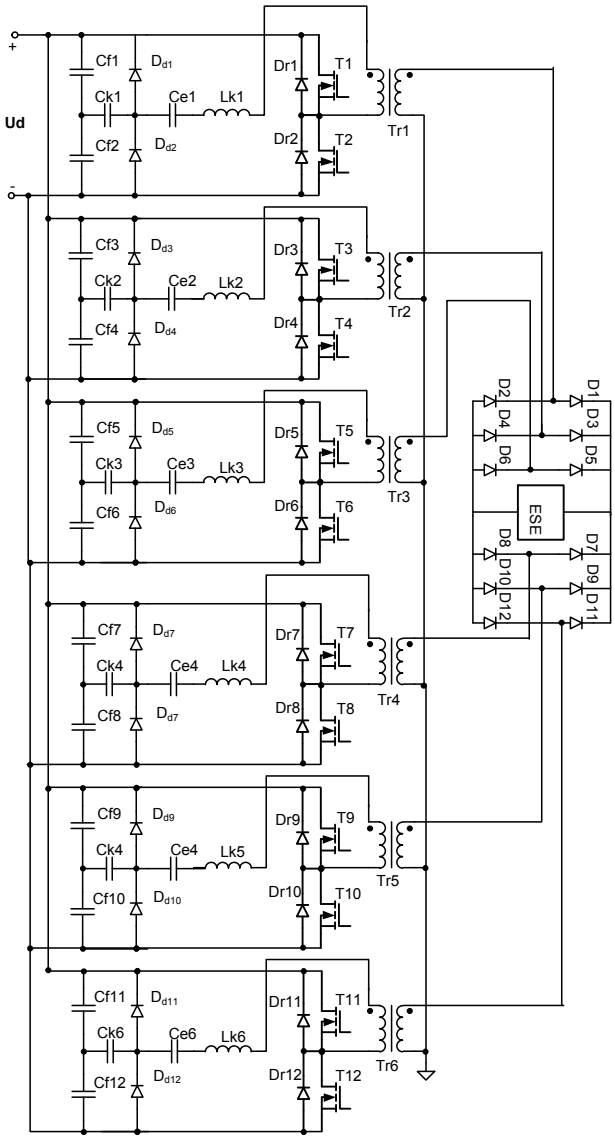

Fig. 2. Multiphase converter circuit

III. CIRCUIT MODELING

A. Simulation results

A simulation model based on the battery charging circuit from Fig. 2 is developed. The used transistor models contain internal reverse diodes. The energy storage element being charged (a rechargeable battery stack) is substituted by an equivalent circuit consisting of three elements connected in series – a DC voltage source representing the initial battery voltage; a series resistor representing the internal battery resistance and a capacitor representing the voltage rise during the charging process. The capacitor value is significantly reduced in order smaller simulation times to be obtained for evaluation of the circuit qualities.

Fig. 3 presents results from the simulation investigations of the examined six-phase converter. Waveforms of the battery stack voltage V(n002), the transformer Tr1 primary coil current I(L11) and the transistor T1 (with internal reverse diode Dr1) current Id(T1) are displayed.

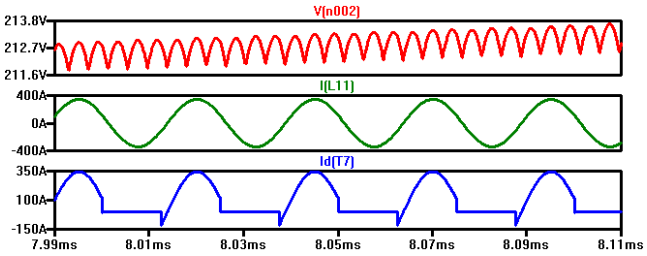

Fig. 3. Waveforms of the battery stack voltage V(n002), the transformer Tr1 primary coil current I(L11) and the transistor T1 current Id(T1).

Fig. 4 presents waveforms of the capacitor Ck1 current I(Ck1), the capacitor Ck1 voltage V(N017, N016), the current Id(T1) through the transistor T1 and its internal reverse diode Dr1 and the limitation diode Dd2 current I(Dd2). From the diagrams, it can be observed that when the capacitor voltage reaches the value of ±Ud/2, the limitation diodes switch on and the unit power consumption from the supply source is ceased. During the charging process, the limitation diodes may switch on either before or after the corresponding reverse diodes. This is determined by the converter operating mode. After a specific moment during the charging process, the capacitor Ck voltage always remains below ±Ud/2 and there is no condition for the limitation diodes Dd to switch on. In this case, the circuit of each separate unit operates as a resonant inverter with reverse diode above the resonant frequency.

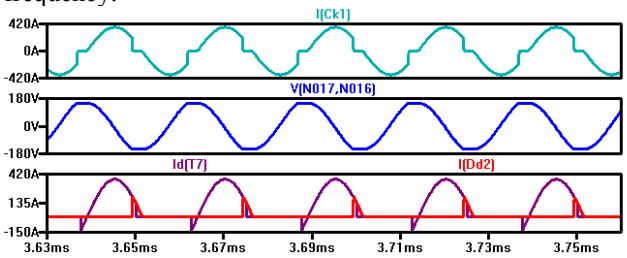

Fig. 4. Waveforms of the capacitor Ck1 current I(Ck1) and voltage V(N017,N016), the transistor T1 and limitation diode Dd2 currents Id(T1) and I(Dd2).

Fig. 5 presents waveforms of the battery stack (ESE) current I(Csc1), the rectifier diodes D1-D12 currents I(D1) – I(D12) and the transformer Tr1 secondary coil current I(L21).

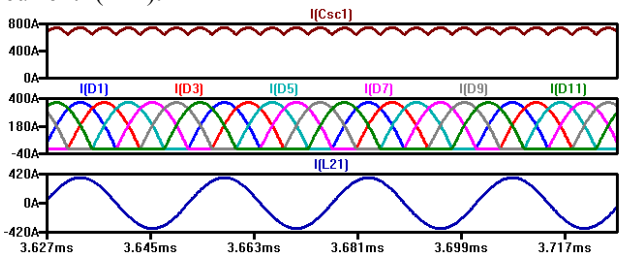

Fig. 5. Waveforms of the ESE current I(Csc1), the rectifier diodes D1-D12 currents I(D1)-I(D12) and the transformer Tr1 secondary coil current I(L21).

From the waveforms, it can be observed that three diodes from the cathode group and three diodes from the anode group conduct simultaneously, which is a specific feature for this converter.

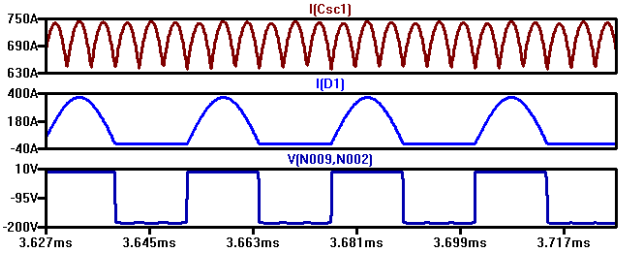

Fig. 6. Waveforms of the ESE current I(Csc1), the diode D1 current I(D1) and voltage V(N009,N002).

Fig. 6 presents waveforms of the storage element (ESE) current I(Csc1), the diode D1 current I(D1) and the voltage V(N009, N002) across this diode. The maximum value of the diode reverse voltage equals the value to which the battery stack is charged and varies during the charging process.

Fig. 7 presents waveforms of the transistor T1 and its internal reverse diode Dr1 current Id(T1), the limitation diode Dd1 current I(Dd1), the transistor T1 voltage V(N003, N020), and the diodes D1 and D3 currents I(D1) and I(D3). From the first waveform, it can be observed that the limitation diode Dd1 switches on before the reverse diode Dr2. After that, there is an interval in which a limitation and a reverse diode conduct simultaneously. The interval of diodes D1 and D3 simultaneous conduction can also be observed.

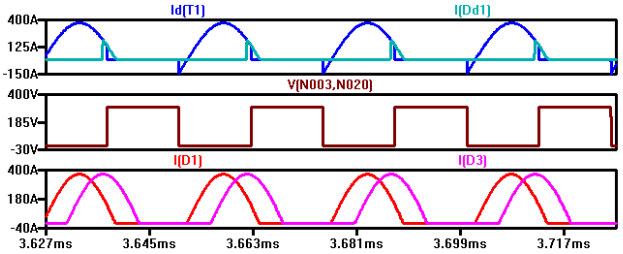

Fig. 7. Waveforms of the transistor T1 current Id(T1) and voltage V(N003,N020) and the diodes Dd1, D1 and D3 currents I(Dd1), I(D1) and I(D3).

Fig. 8 presents waveforms of the transformer Tr1 secondary coil current I(L21), the transformer Tr1 secondary coil voltage V(N009, N015) and the energy storage element current I(Csc1).

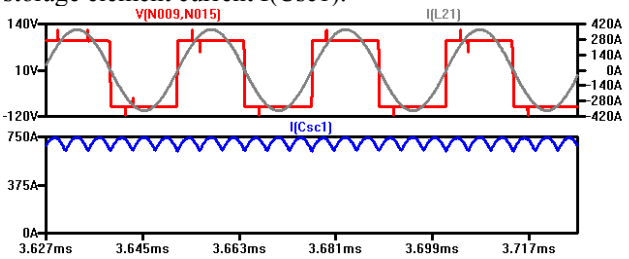

Fig. 8. Waveforms of the transformer Tr1 secondary coil current I(L21) and voltage V(N009,N015) and the ESE current I(Csc1).

IV. Conclusion

A new circuit of multiunit multiphase converter for charging of energy storage elements (rechargeable batteries and capacitors) is proposed. The converter is developed on modular principle. It consists of N number identical resonant converters. In the following paper, the operation of six units is presented. This allows higher output power to be obtained by several lower-power converter units. Another advantage of the proposed converter is the operation with soft switching of the semiconductor devices. The energy storage element charging current has low ripples without the use of filter elements, which is a result of the multiphase rectifier features. Because of the complexity of the multiphase converter charging process, the main circuit voltage and current dependencies may be obtained by numerical methods for differential equations solving [8].

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Ultra Capacitors Charging by Regenerative Braking in Electric Vehicles

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Abstract – **The process of regenerative braking of an electric vehicle with source of energy - battery and ultracapacitor is subject of this work. The studied system is composed of a brushless DC motor, buck-boost DC converter and ultracapacitors. An optimization of the control system for storing maximum energy in the ultracapacitors is performed. The results are useful for the aim of improving the control of energy flows in electric vehicle and achieving maximum range with a single charge.**

Keywords – **electric vehicles, buck-boost converters, regenerative energy, control of energy flows, ultracapacitors**

I. INTRODUCTION

One of the main advantages of electric traction vehicles are the reversible energy flows in the electric machine. Thus, energy created from regenerative braking of the vehicle can be stored. Most often it is reused for supporting acceleration at vehicle departure [5, 9, 10]. Due to its advantages, regenerative braking is widely used in transport: electric and hybrid vehicles, electric bicycles, railways etc. [1, 6, 7].

The system that stores electric energy is in most cases composed of ultracapacitor and battery. This reduces the working stress on the battery and increases its lifetime [8, 9]. The most important property of ultracapacitors is that they store and deliver energy rapidly. This justifies their use to improve the vehicle dynamics, despite their relatively high price at the moment. Due to the specifics and differences between the characteristics of the above two energy storage elements, the use of power electronic converters is necessary, a DC-DC buck/boost converter is used in the studied system. The process of storing energy in ultracapacitors by regenerative braking is examined in the current work.

II. REALIZATION

The block diagram of the studied system is shown on Fig. 1. It consists of the following elements: a brushless DC motor (M), AC / DC converter, buck-boost DC converter and ultracapacitors (UC).

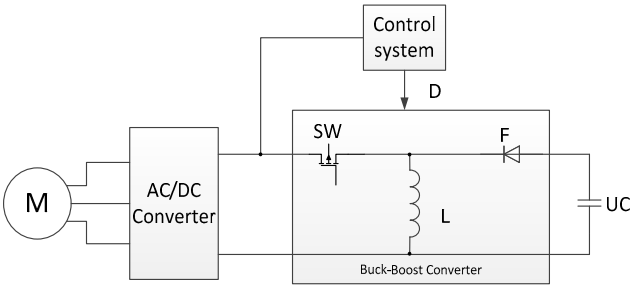

Fig.1.Block scheme

The control system consists of several levels due to the specifics of its components and systems of the electric vehicle and also due to the significant difference in time constants of the individual tracts [2, 6]. The structural diagram of the control system is shown in Fig. 2.

The control system is implemented as a cascade composed of two loops - internal and external. The external uses a signal from the change in motor rotational speed and compares it with a setpoint *(dV / dt) ref*, and the regulator *R1* feeds a reference for the motor current. The internal loop controls the DC converter for obtaining a constant and compliant to the reference motor current, by varying the duty cycle *D* of the electronic switch.

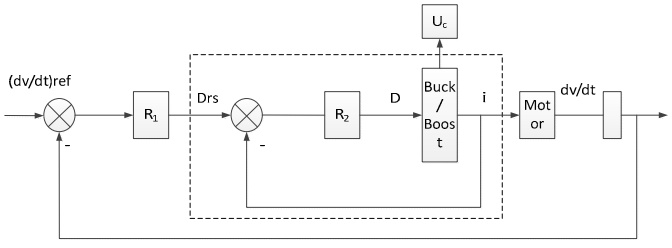

Fig.2. Control scheme

The object of this study is to analyse the operation and setting of the system internal control loop (contoured by a dashed line in Fig. 2).

III. MATHEMATICAL MODELS

A mathematical model of the system is implemented for the simulations. The equivalent circuit of the system is presented at Fig.3. It comprises of a voltage source E_d with

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its internal resistance R_I, a switching transistor VT with its internal resistance in the "ON" state R_{ON}; a filter inductance L and its active resistance R_L; diode VD, a forward voltage V_F and dynamic resistance R_F; UC ultracapacitors with capacity C_{UC} and internal series resistance R_{UC};

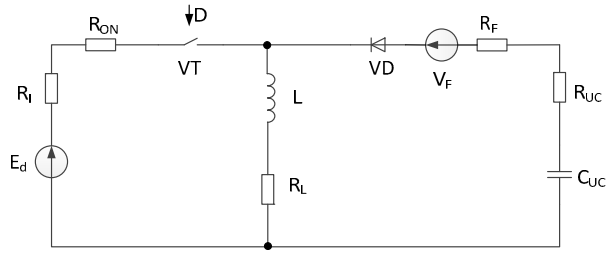

Fig.3. DC/DC Converter

The different stages the converter operation are described mathematically with the following system of equations:

For the conducting state of the transistor -

$$\begin{aligned} L(i_L,\theta)\frac{di_L}{dt} &= E_d - (R_L + R_{ON} + R_I)i_L \\ C_{UC}\frac{dU_{UC}}{dt} &= 0 \end{aligned} \quad (1)$$

where, i_L is the current through the inductance and U_{CUC} is the voltage of the ultracapacitor.

And when the switch is turned off:

$$\begin{aligned} L(i_L,\theta)\frac{di_L}{dt} + (R_L + R_F + R_{UC})i_L + U_{UC} &= 0 \\ C_{UC}\frac{dU_{UC}}{dt} &= i_L \end{aligned} \quad (2)$$

In generator mode the motor voltage at the output of the rectifier is proportional to the speed V of the electric vehicle, i.e. $E_d = kV$. When braking with constant force $\frac{dV}{dt} = const$, E_d is a linear function of time $E_d = E_{d\max} - kt$.

Assuming that $L = const$, i.e. the inductance of the inductor is independent from the current or the temperature, the system equations (1) have the following solution:

When the switch is on

$$\begin{aligned} i_L((n+D)t_p) &= i_L(nt_p)e^{-a/LDt_p} + \left(1 - e^{-a/LDt_p}\right)b \\ U_{UC}\left((n+D)t_p\right) &= U_{UC}\left(nt_p\right) \\ a &= R_L + R_I + R_{ON} \\ b &= E_d / a \end{aligned} \quad (3)$$

where D is the duty cycle.

And when the switch is turned off:

$$\begin{aligned} i_L((n+1)t_p) &= i_L\left((n+D)t_p\right)e^{-a/LDt_p} + \left(1 - e^{-a/LDt_p}\right) \\ U_{UC}\left((n+D)t_p\right) &= U_{UC}\left((n+1)t_p\right) \\ a &= R_L + R_{UC} + R_F \\ b &= E_d / a \end{aligned} \quad (4)$$

The following consideration is taken into account for simplification and easier solution: $L \ll C$, so $U_{UC} \approx const$ for $nt_p < t \le n(t_p + D)$.

The capacity of the ultracapacitors, inductance of the inductor and the operating frequency of the converter are determined.

The ultracapacitors have two functions: to assist the departure and to collect energy when braking.

The necessary power in starting mode of an electric vehicle with mass m and final speed V_{max} is $E = \frac{mV_{\max}^2}{2\eta}$, where η is the efficiency of the energy conversion from the storage element to the wheels.

Assuming, that the energy of the ultracapacitor is $E_{UCS} = kE,\ k \in [0,1]$. The repartition of energy from the two sources by departure is determined by the coefficient k. Assuming that $U_{UC\max} = E_{d\max}$ for the capacity of the ultracapacitor it's obtained $C_{uc} > \frac{2kE}{U_{UC\max}^2}$. The energy charged into the ultracapacitors at constant speed will be $E_{IN} = E_{UCS} - E_{UCRB}$, where E_{UCRB} is the energy that will be stored in the ultracapacitor by the vehicle regenerative braking.

The ultracapacitors should be partially charged before the braking, so that after the process of regenerative braking they can be charged up to their maximum operating voltage. From where the initial voltage of charging in regenerative braking is determined $U_{UCIN} = \sqrt{\frac{2E_{IN}}{C_{UC}}}$.

IV. Results

A numerical experiment – simulation of an electric vehicle with the following characteristics is performed:

Mass of electric vehicle $m = 700kg$;

Acceleration by departure $\frac{dV}{dt} = 2ms^{-2}$;

By assumption the energies drawn from the battery and the ultracapacitor by vehicle departure are equal.

A proportional-integral regulator is used for controlling the motor current. The experiment is carried out under the following assumptions:

- Zero magnetic losses in the inductor;
- The inductor is linear;
- For operating frequency of the DC-DC converter is chosen the maximum possible according to the frequency limits of the circuit components;
- The lower limit of the operating frequency is determined from the requirement for continuous current through the inductor;
- Description of losses in the individual circuit elements is performed according to the methodology shown in [11].

The results of the experiment are presented in table1,2,3. An IGBT transistor of type AN4544 is used, Schottky diode SBR40U300CT and 120 ultracapacitors of type BCAP035 connected in series with capacity 350F, voltage 2.5V, and internal resistance 3.2mΩ. The following anotations are used:

-Ec is the energy in the ultracapacitor at the end of the regenerative braking process

$$\eta = \frac{E_{UC}}{E_{UC} + E_{VT} + E_{R_l} + E_{RL} + E_{VD} + E_{RUC}}$$

Is the efficiency of energy conversion in regenerative braking. The energies in the denominator are respectively: the losses in the transistor, the losses in inductor, diodes and in the ultracapacitor.

- ΔI_{Lmax}- maximum value of ripple current through the inductor

TABLE 1

f=300 KHz, D_{max}=0.85

L [µH]	30	40	50	80	100	110
EUCRB,[J]	50310	50310	50310	50310	50310	50310
η	0.896	0.896	0.8965	0.896	0.896	0.896
ΔILmax [A]	15.19	12.76	9.06	5.81	4.5	4.11

TABLE 2

f=200 KHz, D_{max}=0.85

L [µH]	30	40	50	80	100	110
EUCRB,[J]	50312	50310	50310	50309	50310	50310
η	0.896	0.896	0.896	0.896	0.896	0.896
ΔILmax [A]	23	16.95	13.42	8.35	6.78	6.15

TABLE 3

f=100 KHz, D_{max}=0.85

L [µH]	45	50	80	100	110
EUCRB,[J]	50312	50311	50309	50308	50308
η	0.897	0.897	0.897	0.897	0.897
ΔILmax [A]	30.18	27	16.9	13.1	12.35

In Fig. 4., Fig. 5., Fig. 6. and Fig. 7. are shown the graphical results as following:

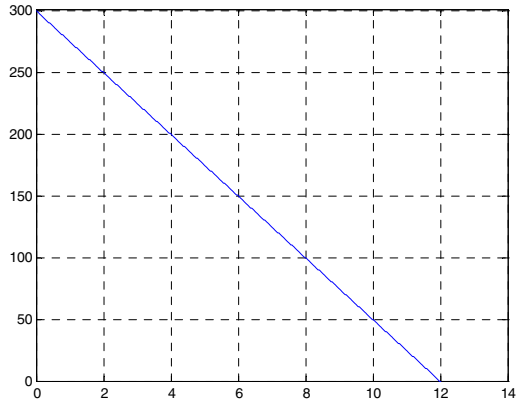

Fig.4. Input voltage of DC/DC converter

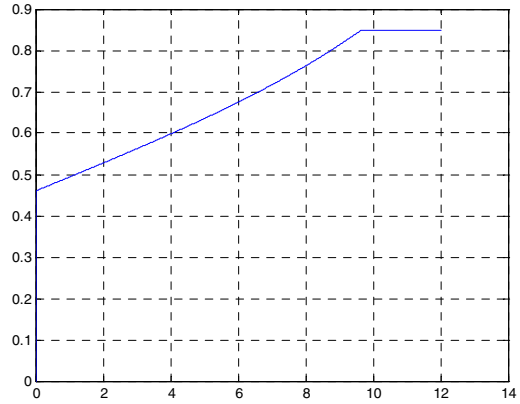

Fig.5. The change of the coefficient in the duty cycle in DC/DC converter

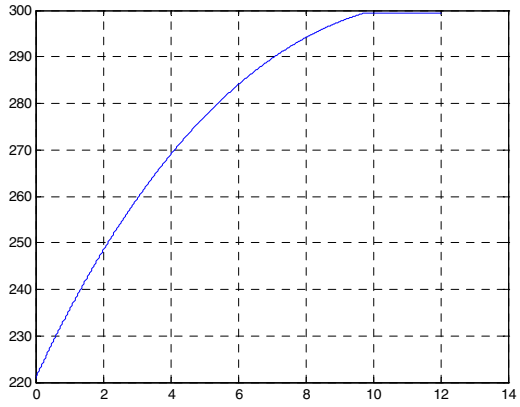

Fig.6. The voltage of the ultracapacitor

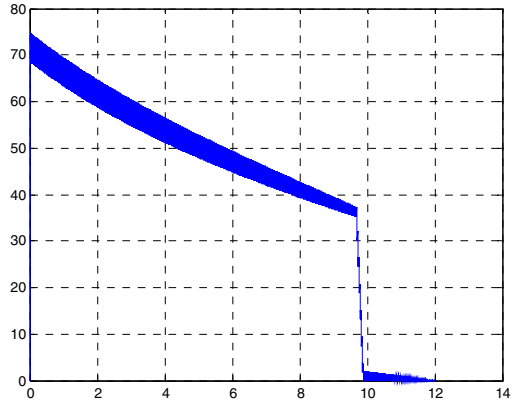

Fig.7. The current through the filter inductance of the DC/DC converter at operating frequency f=200kHz and the value of inductance L=110μH.

V. CONCLUSION

Regenerative braking is an efficient way for improving electric vehicles dynamics and extension of the battery life. As a result from the present research, the following conclusions are made:

- The amount of energy stored in the ultracapacitors depends slightly on the switching frequency of the DC converter;

- Losses in the converter are proportional to the switching frequency;

- The ripple of the motor current is practically independent from the filter inductance L;

- The control system is invariant from the amount of energy recovered and the converter parameters. The influence of the regulator settings on overall system efficiency is weak. The majority of losses in the system are in the ultracapacitors.

A natural extension of this research is a study of the outer control loop of the system.

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Loss Analysis and Improvements of Battery Charging System for Light Electric Vehicles

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Abstract – The paper presents loss analysis and improvements of a battery charging system for light electrical vehicles. Possible solutions and design approaches are presented for reducing weight and improving efficiency of the system. The charger system (1500W) consists of rectifier with inrush current limiting, PFC and resonant DC/DC converter. Presented loss analyses leads to selection of proper switches (SiC) to minimize the switching and conduction losses. Comparative study of using different magnetic materials, wires and winding arrangements is presented, aimed at reducing losses, weight and volume of magnetic components. Design conclusions and recommendations are derived to optimize the charger.

Keywords – **Power electronic converters, Winding arrangements, Power losses**

I. INTRODUCTION

The Electric Vehicles (EVs) become a significant way to reduce our carbon footprint. The benefits of those vehicles can be increased by the use of light and ultra-light EVs as suggested in [1]. Developing such a high efficient vehicle requires meeting many design challenges to keep the weight low and minimize the power losses [2], [3]. The processes in in the propulsion system of an electric vehicle are modeled in [4].

This paper is focused at the losses in a battery charger system intended for EVs. Possible solutions and improvements are presented for reducing weight and improving efficiency.

A typical battery charger consists of three converters: a rectifier with included function of inrush current limiting, a Power Factor Correction (PFC) converter and another DC/DC converter to provide galvanic separation. Analysis and optimization of losses in boost converters and PFC are presented in [5], [6].

The charger is powered by a standard household 230V socket and therefore a rectifier is needed to convert the voltage.

Because of the high power needed (1500 W in the example, studied in this paper) there are bulk capacitors in the charger, so the rectifier should offer inrush current limiting capabilities. The topology in the example uses thyristors and ballast resistors to limit those currents. The usage of a PFC is crucial for meeting the EMI and other requirements for the standartization of the charger (boost converter topology is used in the example as the most common and efficient). To keep the efficiency high, the PFC converter operates at high output voltage 400V or more, therefore another converter is needed to adapt the voltage for charging the batteries. To reduce the switching losses and provide galvanic separation (another requirement for standartization), a resonant DC-DC bridge converter is suitable. Depending on the power, a half bridge or a full bridge topology is used (in this paper the converter used is a half-bridge one). Such a battery charger is presented in [7]. The magnetic components are calculated according to the approach in [8].

The converter system is presented in Figure 1.

In this paper the main sources of losses in the three converters are analyzed. Those are losses in thyristors and diodes of the semi-controlled rectifier bridge, the MOSFET switch, the diode and the inductor of the PFC and the switches and the magnetic components of the resonant DC-DC converter.

To improve the efficiency and reduce the weight of the charger new materials are tested in both switches and magnetics and comparison tables are provided. The study covers the new SiC semiconductor switches, nanocrystalline magnetic materials and different approaches for reducing loses in switches and magnetics.

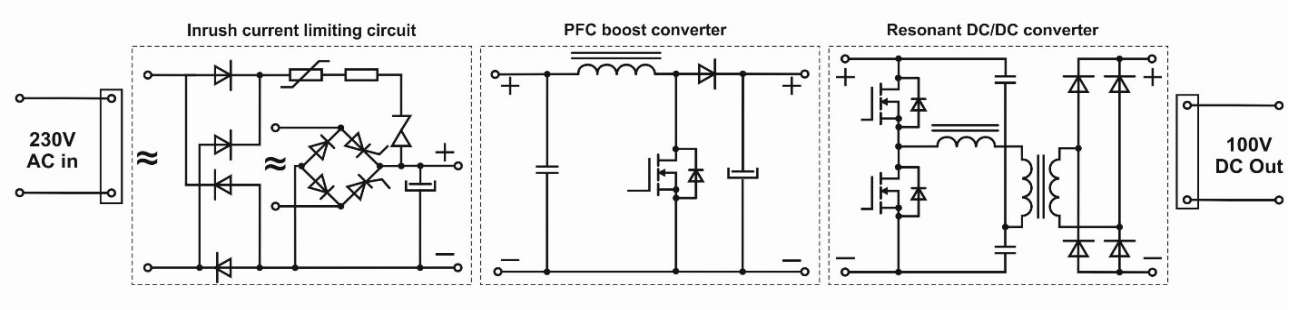

Fig. 1. Block scheme of a battery charger suitable for ultra-light electric vehicles.

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II. Analysis of Power Losses in the Switches

1. Losses in the switches of the input rectifier (inrush current limiting circuit)

The inrush current limiting circuit is realized by a semi-controlled bridge rectifier P101 with two thyristors and two diodes. The losses are determined via measurements and calculations. A DC setup is used to measure the losses in the thyristor – diode circuit. The forward voltage drops of the thyristor $V_{F,th}$ and the diode $V_{F,D}$ are measured and the losses are calculated using the following equations:

$$P_{th} = I_{in} V_{F,th} \quad (1)$$

$$P_D = I_{in} V_{F,D} \quad (2)$$

The obtained losses are 5.20W in thyristors and 3.60W in diodes.

2. Losses in PFC converter switches

To find a solution with low losses in switches, a comparative study is realized including Si and SiC MOSFET transistors. Firstly, using the approach presented in [9] two transistors (a Si and a SiC based) are selected and their main parameters (Table 1) are further used to calculate the losses.

A CREE's C3D10060A Silicon Carbide Schottky Diode is selected for boost diode in PFC converter. The total losses of the SiC diode are evaluated to 6.853 W. These losses are calculated for the worst case with minimum input voltage, maximum diode forward current and maximum switching frequency.

TABLE 1. MAIN PARAMETERS OF THE SELECTED MOSFETS, SI AND SIC BASED SEMICONDUCTORS

Si and SiC MOSFETs	R_{dson}	I_{ds}	V_{gs}	V_{th}	C_{iss}	C_{rss}	E_{oss}	Q_g
	Ω	A	V	V	pF	pF	µJ	nC
STW77N65M5	0.033	69	10	4	9800	6	35	185
SCT3030AL	0.030	70	18	4.2	1526	42	112	104

Conduction losses in the MOSFET switch are calculated as [10]:

$$I_{S,rms} = \frac{P_O}{V_{ac,min}} \sqrt{1 - \frac{8\sqrt{2} V_{ac,min}}{3\pi V_O}} \quad (3)$$

$$P_{S,cond} = I_{S,rms}^{\ 2} R_{ON(100\,°C)} \quad (4)$$

where $I_{S,rms}$ is the RMS current through the switches, P_o is the output power, $V_{ac.min}$ is the grid voltage in the worst case (-15 %) and V_o is the output voltage.

Then total losses are:

$$P_{S,total} = P_{S,cond} + P_{S,ON} + P_{S,OFF} + P_{S,oss} \quad (5)$$

where: $P_{S,total}$ are the full losses in the switch;
$P_{S,cond}$ are the conduction losses;
$P_{S,ON}$ and $P_{S,OFF}$ are the switching losses of the transistor and $P_{S,oss}$ are the losses for charging the parasitic capacitance of the switch.

The results of the calculations are summarized in Table 2.

TABLE 2. LOSSES IN THE SWITCH OF PFC

Si and SiC MOSFETs	Conduction losses	Switching losses	Total losses
STW77N65M5, Si	1.445	7.622	9.067
SCT3030AL, SiC	1.314	3.000	4.314

3. Losses in DC-DC converter switches

The same transistors are used in the resonant DC/DC converter. Main equations used to calculate the losses are:
1) Approximate root mean square current:

$$I_{rms} = 1.11 I_{tr} \quad (6)$$

2) Conduction losses (one transistor):

$$P_{cond} = I_{rms}^{\ 2} R_{d100} \text{duty} \quad (7)$$

3) Total losses in both transistors (hard switch off):

$$P_{totalh} = 2 \cdot (P_{cond} + P_{sw} + P_{gate} + P_{hsw}) \quad (8)$$

Worst case with switching off at the peak current is calculated. The results are summarized in Table 3.

TABLE 3. LOSSES IN THE SWITCHES OF THE RESONANT DC/DC CONVERTER

Si and SiC MOSFETs	Conduction losses	Switching losses	Total losses
STW77N65M5, Si	2.714	37.759	40.473
SCT3030AL, SiC	2.658	16.567	19.225

III. Design and Comparative Study of Magnetic Components Used

The power stages of the battery charging system contains three power magnetic components: a DC choke in the PFC, an AC inductor and a transformer in the DC-DC resonant converter. Operating frequency in both converters is relatively high (50kHz). This fact leads to increasing the importance of the design of magnetic components, as the losses in them will be significant part of the total losses of the converters.

1) Selection of core material

For the design of the components we consider ferrite materials and nanocrystalline materials. The materials considered are:

- Ferrite N87 made by EPCOS [11]. It is MnZn ferrite for use up to 500kHz, which in terms of eddy current losses is highly recommended;
- Vitroperm 500F offered by Vacuumschmelze [12] The material shows low losses are high frequencies, typical example: at 100 kHz, 0.2 T, approximately 40 mW/g.

TABLE 4. DESIGN PARAMETERS OF MAGNETIC COMPONENTS:
DC CHOKE, AC INDUCTOR, TRANSFORMER, P=1500W, 50KHZ, MATERIAL N87

Component		Core type	d_{chosen} [mm]	P_{cu} [W]	P_{fe} [W]	P_{tot} [W]
DC Choke		E 42/21/20	225x0.071mm	2.74	0.091	2.831
AC Inductor		E 42/21/20	630x0.071	1.922	2.213	4.135
Transformer	primary	E 65/32/27	(4+4)x0.63mm	1.309	5.293	8.501
	secondary		5x1.12mm	1.898		

The nanocrystalline materials are offered mainly in toriodal and UU core forms and it is known they are very concurrent in realization of DC chokes. Thus, in the paper an alternative design of the DC choke will be calculated based on a Vitroperm 500F meterial.

2) *Design methodology*

The designs are realized by a 15 steps methodology suitable for practical calculations including eddy current losses in windings [13], [14]. The first step is calculating the core size using:

$$a_{ch}=\left(\frac{S_{tot}}{A}\right)^{1/\gamma},\quad S_{tot}=\sum_{\text{all windings}} V_{rms}\, I_{rms} \tag{9}$$

where a_{ch} is the largest dimension of the component, used as a scaling parameter;
A is a coefficient, for ferrites, $A = (5–25) \times 10^6$ if a_{ch} is in (m), [13];
γ is an exponent, characterizing the material and shape of the core, $\gamma = 3$;
S_{tot} is the total volt-amp rating of the component;
V_{rms} and I_{rms} are the voltage and current of the corresponding winding.

The allowable power losses of the component are obtained and equally assigned to the core and the windings. Using allowable core losses B_{peak} is found from manufacturer's graphs, the necessary turns for the primary and secondary windings are calculated, followed by choosing the appropriate conductors' diameters and winding arrangements. A final check is provided by the values of introduced coefficients k_{eddy}, k_{cu}, and if necessary a next available (smaller or bigger) core size is chosen and the algorithm is proceeded with that core. The coefficient k_{eddy} gives the ratio between eddy current losses and ohmic losses and k_{cu} is copper filling factor.

3) Specifications of the designed magnetic components

Main specifications of the designed magnetic components based on ferrite material (N87) are:

- DC choke: 44 turns, 3 layers; Litz wire 225x0.071mm, P_{tot}=2.831W;
- AC inductor: 26 turns, Litz wire 630x0.071mm, P_{tot}=4.135W;
- Transformer: 13 turns primary and 5 turns secondary winding, PSP arrangement - primary winding is realized as two parallel layers, each layer 4x0,63mm parallel wires for each turn, all turns' wound in one layer; secondary - 5x1.12mm parallel wires for each turn, all turns wound in one layer, P_{tot}=8.501W.

Remarks:

- Using Litz wire provides reducing eddy current losses, a drawback - deteriorated heat transfer;
- Arrangement PSP (primary, secondary, primary winding) is used to reduce proximity effect in the wires of the transformer.
- Best results of the interleaving are obtained when each of the primary and secondary windings fit within a single physical layer and the whole winding width is filled.

The obtained design results are summarized in Table 4.

The described designs are based on ferrite material N87 as its price is better compared to material Vitroperm 500F. If the design goals are widened with low volume and weight, then using nanocystalline materials (Vitroperm 500F) gives the best results.

IV. TOTAL LOSS ESTIMATION

The total losses include also losses in the control circuits of the converters, in the DC link capacitors and in the snubber circuits. The sum of these loss components is less than 10% of the total losses, thus it will be considered, but not investigated.

The total calculated losses in the switches and magnetic components of the battery charging system are summarized in Table 5. The results are confirmed by simulations.

The total investigated losses are calculated as 80.66W for using Si MOSFETs and 54.659W for using SiC MOSFETs.

TABLE 5. TOTAL LOSSES IN THE SWITCHES AND IN THE MAGNETIC COMPONENTS OF THE BATTERY CHARGING SYSTEM
INPUT RECTIFIER, PFC, DC-DC CONVERTER, P=1500W

Switch type	Input rectifier, switches			PFC, switch+diode				DC-DC, switches			Battery charging system		
	Thyristors	Diodes	Total	Sw. Loss	Con. Loss	Diode	Total	Sw. Loss	Con. Loss	Total	Switches	Magnetics	Total
-	W	W	W	W	W	W	W	W	W	W	W	W	W
Si	5.20	3.60	**8.80**	7.622	1.445	6.853	**15.92**	2.714	37.759	**40.473**	65.193	**15.467**	**80.66**
SiC	5.20	3.60	**8.80**	3.000	1.314	6.853	**11.167**	2.658	16.567	**19.225**	39.192	**15.467**	**54.659**

Estimated efficiency is about 94% with Si MOSFETs and an improvement to about 96% is obtained using SiC MOSFETs. Both cases are calculated with improved designs of the magnetic components used.

V. CONCLUSIONS

The paper presents loss analysis and improvements of a battery charging system for light electrical vehicles (1500W), consisting of rectifier with inrush current limiting, PFC and DC/DC converter.

Analytical presentation of the switching and conduction losses analyses leads to selection of proper switches (SiC) to minimize the total losses.

Comparative study designs based on different magnetic materials, wires and winding arrangements is presented.

Based on the obtained results, design conclusions and recommendations are derived to optimize the charger parameters:

- Using power switches based on SiC technology provides lower total losses in the power switches, efficiency improved from 94% to 96% of the whole charging system;
- Resonant DC-DC converter is recommended when reduction of the switching losses is dominant target in the design;
- Arrangement PSP (primary, secondary, primary winding) is an effective approach to reduce proximity effect in the wires of the transformer;
- Best results of the interleaving are obtained when each of the primary and secondary windings fit within a single physical layer and the whole winding width is filled;
- Using nanocystalline materials (Vitroperm 500F) gives the best results is respect low volume and weight.

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A Power Electronic Smart Load Controller for Nanogrids and Autonomous Power Systems

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Abstract –**This article presents a new power electronic smart load controller which enables improved usage of the energy provided by the distributed generators (DG) present in comprehensive nanogrids. A typical nanogrid configuration is considered and analyzed. The analysis shows that significant part of the energy generated in the present nanogrids is lost due to limited or absent distribution networks and/or storage capacities. A smart power electronic converter for flexible loads control is presented as a promising solution for better utilization of the generated photovoltaic energy. A simulation of the proposed device is realized. The results witness very good adequacy and high potential for implementation in existing micro and nanogrids with solar and other renewable generation.**

Keywords – **nanogrids, microgrids, power converters, control of energy flows, smart load, solar power, flexible load, demand side management**

I. INTRODUCTION

The growing decentralized renewable generation during the recent decade stimulates novel structure of the future electrical power systems. Significant elements of this structure are the microgrids and nanogrids [1-10].

The microgrids consist of energy consumers, producers and networks at a small scale which are able to manage themselves providing significant advantages for both the grid and the prosumers. Such typical examples are neighborhood, villages, or campus networks.

The nanogrids represent small microgrids, typically serving a single building or a single load. Various nanogrid definitions are present. Some organizations have developed their own definition based on the installed power being 100 kW for grid-tied systems and 5 kW for remote systems not interconnected to the utility grid [4].

Some of the main nanogrid operation advantages are [13]:

- Increased power quality and reliability;
- Reduced peak load considered by the grid;
- Reduced peak energy costs;
- Reduced transmission and distribution (T&D) losses by having on-site generation and energy storage;
- Supply of ancillary services to the grid;
- Accelerated adoption of distributed and renewable energy sources;
- Reduced fossil fuel use/carbon emissions.

The typical configuration of a nanogrid consists of flexible and nonflexible loads, energy storage devices, network connections and local distributed generation such as photovoltaic (PV), wind, hydro, combined heat and power (CHP), fuel cell or other generators.

Currently the photovoltaic systems represents the most promising part of the distributed nanogrid generation due to its wide applicability, admissible investment cost, predictive and safe energy production.

One of the significant problems in front of the nanogrid operation is that the energy generated by the distributed generation within the nanogrids is lost when the battery is full and load is not present.

One option to overcome this drawback is to feed the excessive energy into the grid if present [1, 3, 14]. However a majority of nanogrids operate in autonomous mode where grid feeding is not possible. Network congestions and reduced power transfer capability represent other significant barrier which limits the surplus power network injection.

This article presents a new smart power electronic load controller for dispatchable loads which enable significantly improved energy usage and efficiency of the generation.

II. NANOGRID CONFIGURATION

One of the most widely used nanogrid configurations is presented on Fig.1. It consists of the following system components [18]:

1. PV generator;

2. Connection box which forms PV arrays with appropriate voltage and power and hosts the necessary protection equipment.

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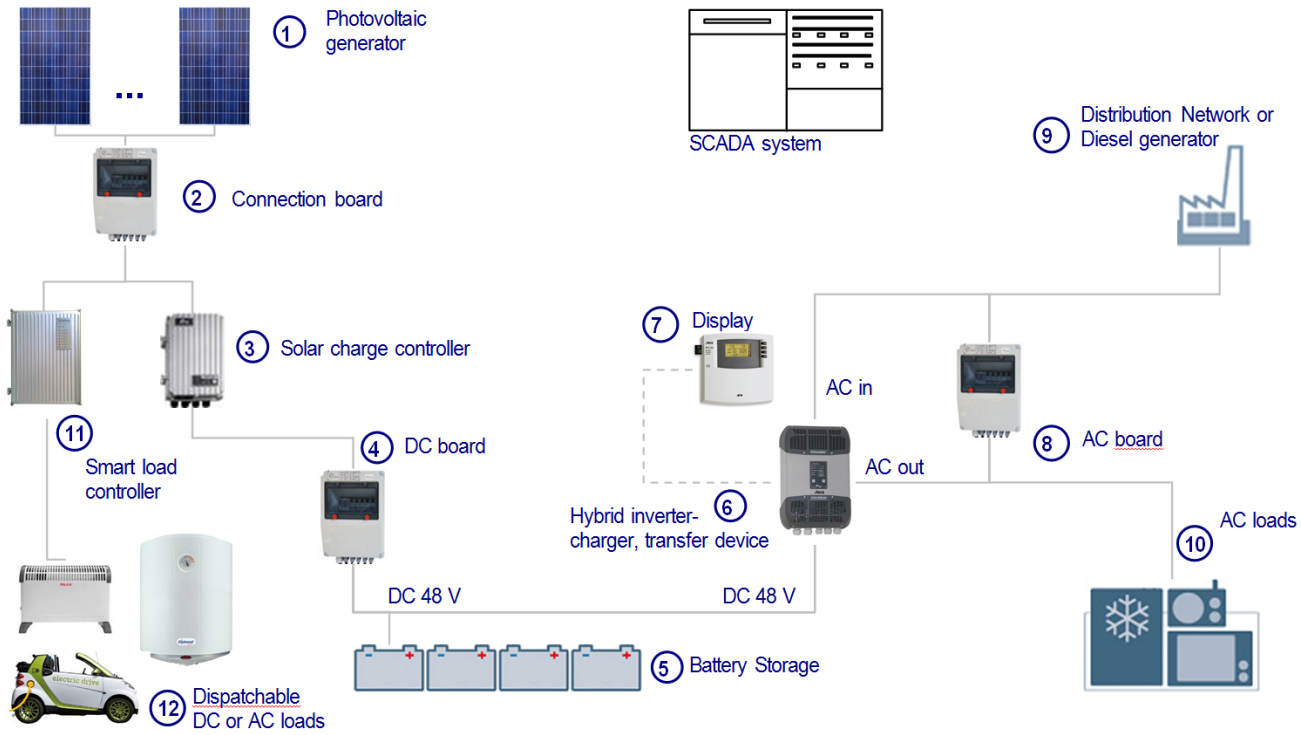

Fig. 1. Typical nanogrid configuration

3. Solar charge controller with MPP tracking. It converts the DC output of the photovoltaic generator in DC with appropriate parameters for charging the battery. The charge controller is typically equipped with external communication channel through which information about the charging process is shared with the other charge controllers and hybrid inverters in order to coordinate the charging process and to avoid damage of the battery.

4. DC box equipped with the necessary protections;

5. Battery block;

6. Hybrid inverter, charger and transfer switching device which operates as programmable energy manager with communication interface and ability to integrate information flows to a SCADA system;

7. Display for the key operating parameters of the system.

8. AC box equipped with the necessary protections.

9. Diesel generator or AC grid;

10. Non flexible AC loads which cannot be dispatched or shifted;

Figure 2 depicts the theoretically available and the practically generated daily power production of an existing household nanogrid near Sofia, Bulgaria which is based on the configuration described above. It is evident that significant amount of the photovoltaic energy is lost due to limited battery storage and grid feeding restrictions.

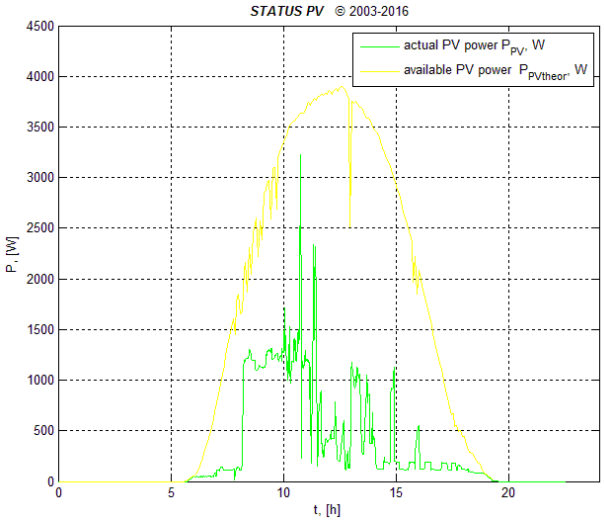

Fig. 2. Measured and theoretically available daily power yield

III. Proposed Nanogrid Controller

A new smart power electronic converter is proposed to overcome the drawback mentioned above. Elements 11 and 12 are added in the configuration on Fig. 1 in order to enable better energy usage of the generated energy by supplying flexible, accumulating DC and compatible AC loads. The newly added elements are:

11. Intelligent power electronic controller. It converts the power of the photovoltaic generator in power with appropriate parameters for supply of active loads, DC charging etc.;

12. Flexible DC and / or compatible AC loads:

- Heating appliances such as convectors, storage water heaters, infrared heaters, electric underfloor heating etc.;
- Electric charging devices such as electric vehicles, hybrid vehicles, e-bikes, etc.;

When the power available from the photovoltaic modules cannot be absorbed by the battery and / or the inverter, the automatic controller directs the free power capacity to the connected devices thru the converter.

IV. Proposed Controller Scheme

The power electronic part of the controller developed is based on proportional Pulse Width Modulation (PWM), voltage controller and voltage sensor (Fig. 3) [17,18]. Due to the easy voltage reference setting a priority to each of the controlled loads is possible.

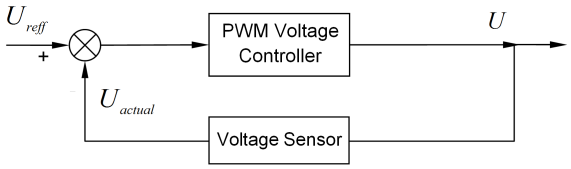

Fig.3. Control scheme

Other controller types such as current hysteresis control, H_∞, artificial neural network, fuzzy logic and predictive control can also be used [19].

The converter (Fig. 4), consists of solid state switch SW such as MOSFET or IGBT with gate driver circuit, reverse diodes D1 and D2, input capacitor C_F, predominantly active load Z_T, voltage controlled PWM controller and voltage sensor. The resistor-capacitor group R and C is used to snub the fast overvoltage transients arising in case of inductance in the circuit.

Unlike the typical DC/DC converter applications the output filter is avoided. The pulsed DC output voltage allows easy and unproblematic connection of standard and inexpensive AC dispatchable loads without any special upgrades of the control and commutation apparatus.

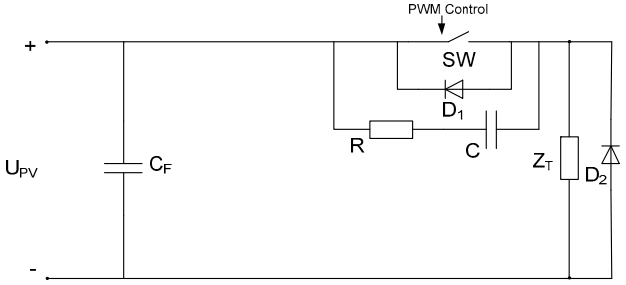

Fig.4. DC/DC converter scheme

The buck converter scheme is used since it is characterized by stable work, good energy conversion performance and wide control range. The proposed converter is simulated in Matlab Simulink environment.

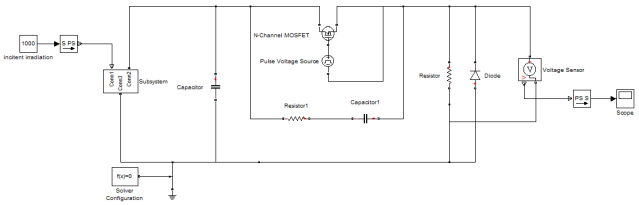

Fig.5. Converter simulation model

A Simscape dynamic simulation model is realized. The photovoltaic generator model consists of 6 modules totaling 360 PV cells connected in series. The PWM control is simulated using a standard pulse voltage source block. The output voltage is depicted by the voltage sensor block.

V. Simulation Results

Fig. 6 depicts the initial transient process with duty cycle value of D= 0,9 until the output voltage is stabilized.

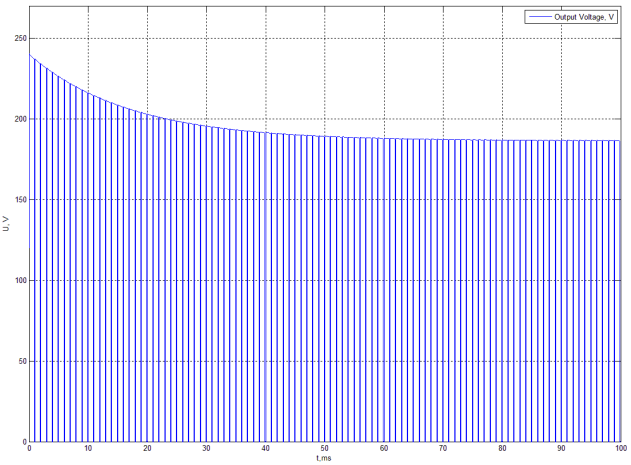

Fig.6. Output voltage, D=0,9, t=0-100ms

Fig. 7 and Fig. 8 show the smart controller output voltage with duty cycle value of D= 0,9 and D= 0,1 correspondingly in steady state operation after the capacitors have been charged.

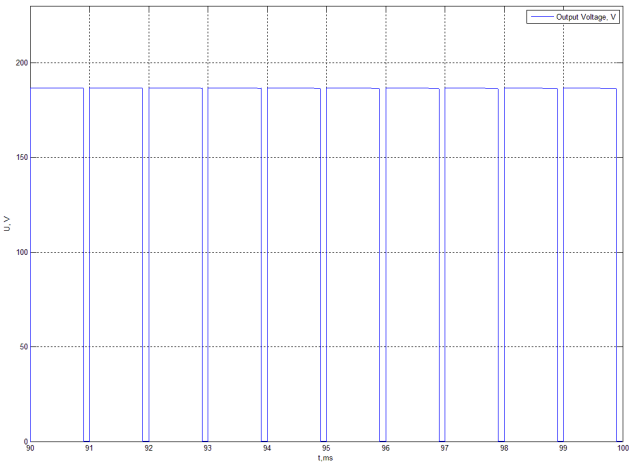

Fig.7. Output voltage, D=0,9, t=90-100ms

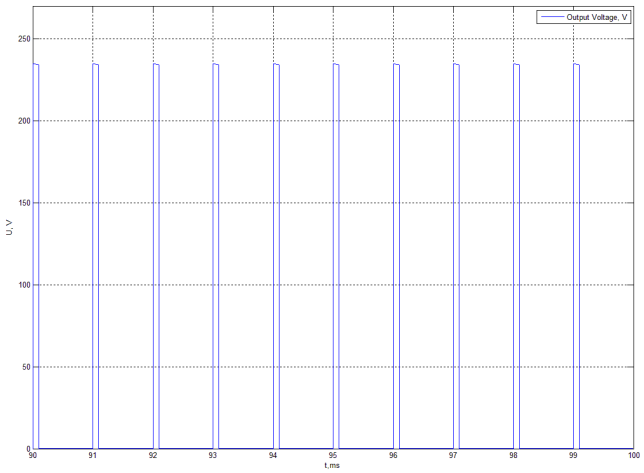

Fig.8. Output voltage, D=0,1, t=90-100ms

With frequency of approximately 1000 Hz, the commutation loses in the scheme elements are minimum and thus high efficiency of the generated power conversion is achieved.

The regulation and stabilization of the smart controller output voltage is achieved by variation of the duty cycle coefficient. A supply of three-phase loads can be achieved using three single phase converters.

Overcurrent protection is realized by monitoring the load current. In case its nominal value is exceeded the control pulses towards the transistor are limited.

Higher voltages can be reached if necessary with the utilization of other known scheme variations of DC/DC converters with or without galvanic isolation.

The life cycle of the battery storage can be further extended using ultracapacitor or other additional storage resources, such as the electric vehicle battery.

VI. Conclusion

A new smart power electronic smart load converter is proposed. The solution provides new opportunities for better and more efficient use of the renewable energy sources in micro- and nanogrid systems.

The hardware solution presented is simple, offers fast interaction and is based on well proven, reliable and inexpensive components. Thus it is cost efficient and widely applicable in distributed systems with multiple load controllers.

Similar approach is also widely applicable for other generation sources in micro and nanogrids.

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Performance Comparison of Active and Passive Converters for Wind Driven Generators

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Abstract – **The paper presents a comparison of the power output of wind driven generators coupled to active and passive converter circuits at certain site in Bulgaria. A table compares the power output difference expressed in percent. Actual wind resource data gives the opportunity to have evaluation and analysis at three different heights. Advantages of active and passive control are derived and summarized. Practical recommendations are made for the dominant application of the compared control approches.**

Keywords – **Passive converter, Simulation, Wind turbine, Wind resource assessment**

I. Introduction

Wind turbines are one of the most spread technology for renewable energy production. The power output of single device rises over the years up to several megawatts at the current moment. Their efficiency is with high significance as the investment of building wind farm becomes larger and larger. Most efficient electrical machines used in wind turbines at the moment are permanent magnet synchronous generators (PMSG). Their peak efficiency is around 95% and therefore the overall efficiency of the system is above 90% for all of the nominal operation range [1]. Variable wind speed operation is crucial for improving the annual power output of modern wind turbines. The investigated topology, which includes PMSG is shown on figure 1. The generator is connected to a rectifier circuit. The DC link is connected to an inverter circuit, which injects the electrical energy into the grid. All the energy harvested from the generator passes through the power electronic converters, which enables full control of the injected energy into the electrical grid. In other words the frequency of the electric generator is completely decoupled from electrical grid frequency by a DC link.

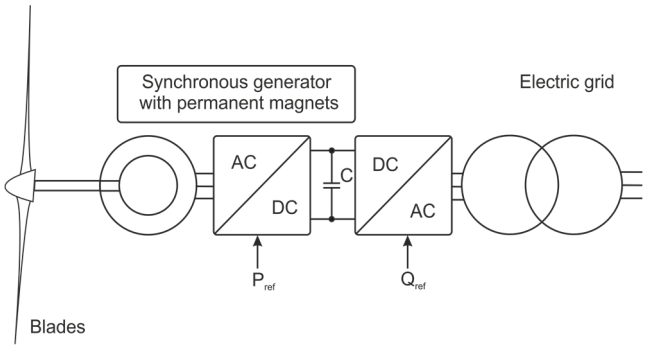

Fig. 1. Wind turbine basic topology with PMSG

Active rectifier circuits, which include fully controlled power electronic switches, provide accurate electrical loading on the electric generator at every moment. This leads to an output power/frequency curve that follows exactly the ideal cubic dependence of power and wind speed almost up to the saturation of the electrical generator.
Disadvantages are sophisticated electronics of the control modules, reliability issues and higher final cost. Figure 2 depicts this and the expected theoretical power from the kinetic energy of the wind can be expressed as:

$$P = \frac{1}{2}\rho A V^3 \qquad (1)$$

, where P - is the output power, ρ – density of the air, A – swept area of the blades, V - wind speed.

An alternative solution can be the use of passive converter circuits proposed in patent PTC/EP2010/055637. The use of the proposed schematics improves robustness and reliability, because there is no control unit with low voltage/low current electronics. It performs better than conventional three phase uncontrolled full wave rectifier at lower wind speeds, which means variable speed operation is possible [2].

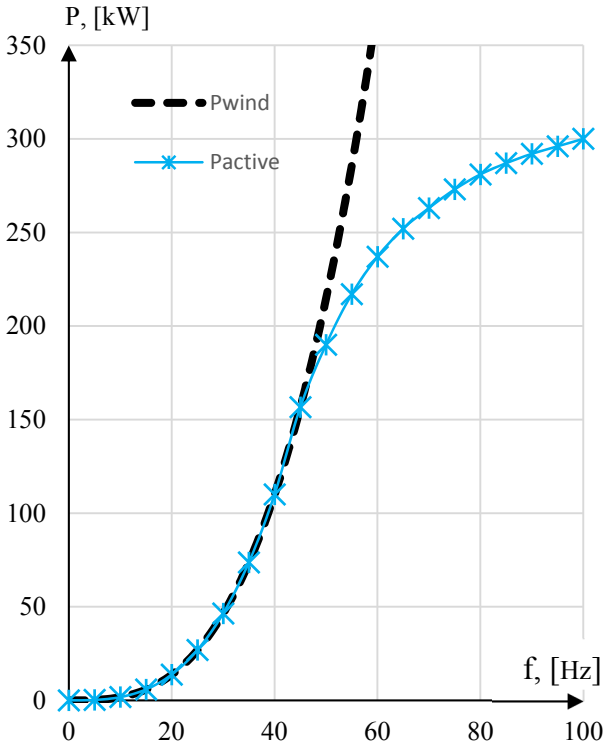

Fig. 2. Power/frequency curve with use of active rectifier circuit

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II. Wind Assessment Data

Effective use of wind renewable energy resource requires precise assessment of the energy potential based on real measurements for an extended period of basic parameters such as, speed and wind direction. Therefore, a scientific consortium of Technical University - Varna, the Association of Producers of Ecological Energy and Pro Eco Energy Ltd. Have prepared maps of solar and wind potential of the North Bulgaria through measurements for at least one year [3]. Measurements are conducted with meteorological masts located in certain places in accordance with the chosen methodology [4, 5, 6].

The meteorological masts are type XHD with a length of 60 m, production of company "NRG Systems". Assembly of the masts meet specific requirements. They are also equipped with sensors to measure wind speed (anemometers) and direction (wind vanes) of the wind. Anemometers NRG #40C and wind vanes NRG #200P are located at 4 different levels of heights 60, 50, 40 and 10 m.

All anemometers are calibrated individually. The technical parameters of the used sensors are presented in the following table 1.

TABLE 1. SENSORS TECHNICAL INFORMATION

Specification	Anemometer	Wind vane
Measurement range	*0÷50 m/s*	*0°÷360°*
Initial threshold	*≤ 1.0 m/s*	*≤ 1.0m/s*
Measurement distance	*< 4.0 m*	-
Temp. range	*-40°C÷60°C*	*-40°C÷60°C*
Humidity range	*0%÷100%*	*0%÷100%*
System error	*≤ 3%*	*≤ 5°*
Tolerance	*≤ 0.1 m/s*	*≤ 1°*

The masts are equipped with a data logger and GSM communicators, through which data from the sensors is sent to e-mail address. The type of the data logger is "Symphonie" and records values every two seconds, which are then averaged in 10 minutes intervals. Records include minimum and maximum value for the interval and standard deviation. The system has an autonomous power supply, including battery and solar module.

As an example on figure 3 are presented results from average monthly wind speed measurement from one of the sites installed near Tutrakan with ID 6053.

An object-oriented software "WindPro" is used then to create digital models that assess the wind potential. Necessary input data include topography and roughness of the terrain, location of the mast and data measurements.

To determine the average speed for each point of the area a model have been used: LINCOM (LINearized COMputation). LINCOM is based on linear equations describing perturbations that relief and roughness of terrain induced air flow.

Processing of the results is a series of calculations in a network of points for consideration area. The advantage of the software is the possibility of using statistics data from poles adjacent to the issue, so wind speed changes smoothly in various points in the network.

Based on the results a wind potential maps are prepared for every area, where individual mast persists. On figure 4 is shown final map at area of mast 6053. The input data and the profile of wind include digital terrain roughness of the terrain and data measured from the meteorological mast. The measured data are for a maximum height of 60 m and is graduated in colors from 4 to 8 m/s.

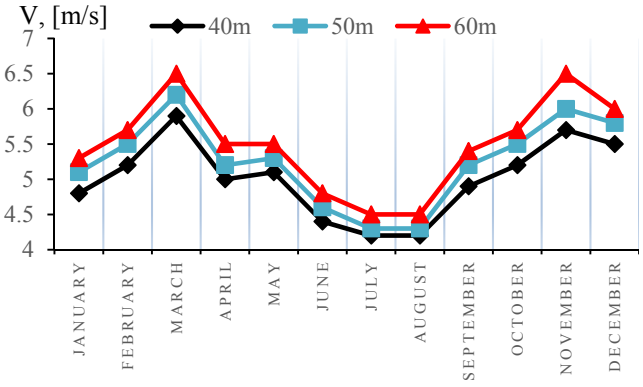

Fig. 3. Average wind speed data

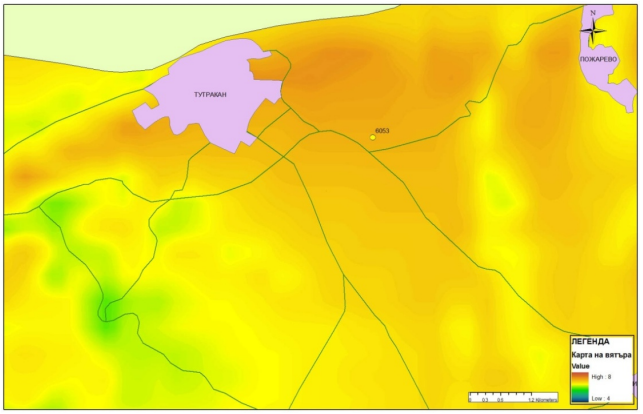

Fig. 4. Wind potential map at area of mast 6053, [3]

III. Passive Converter Basis

A. Operation of passive converter circuit

Basic passive converter circuit is shown on figure 5. It has simplified model of PMSG, consisting of voltage sources Vac1, Vac2, Vac3 and inductors L1, L2, L3.

The specific stricture of full wave rectification of every phase is patented by number PTC/EP2010/055637 and it has 12 variations. The crucial improvement of the performance at low wind speed is due to the influence of the external inductances L4, L5 and L6.

Based on the simple reactive resistance equation 2,

$$X_L = \omega L_{ext.} \tag{2}$$

, where $L_{ext.}$ are substituted with L4,L5 and L6, the circuit becomes with emphasized frequency dependent behavior. At low frequencies $X_{L4,\ L5,\ L6}$ value is low and therefore the three externally connected inductors connect the three phases of the generator acting like middle point connection. This determines topology similar to “star”, which has an advantage of higher line to line voltage and start at lower rpm compared to “delta” topology. When wind speed reaches nominal frequency of the electrical machine (around 40Hz), $X_{L4,\ L5,\ L6}$ values are higher and at this stage the topology is changed to behave similar to “delta”.

Through scanning method with variable step size, shown on figure 6, it is performed parametric optimization of values of components L1 ÷ L6. Then the simulations of the circuit gives output power/frequency curve, i.e. the change in the electrical load of the generator. For the analysis of the result it is carried out a comparison of the resulting curve with a theoretical cubic dependence of the maximum value of the power at different wind speeds shown on figure 7.

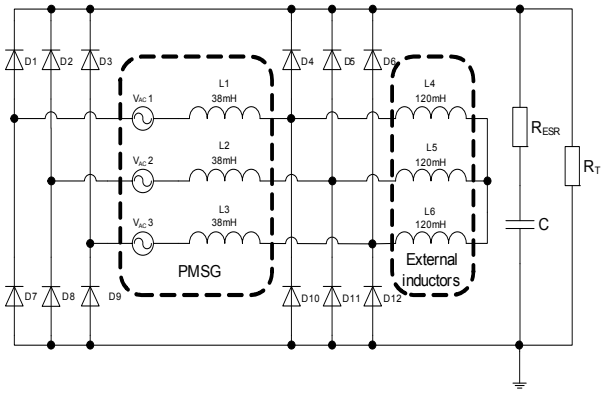

Fig. 5. Basic passive converter circuit

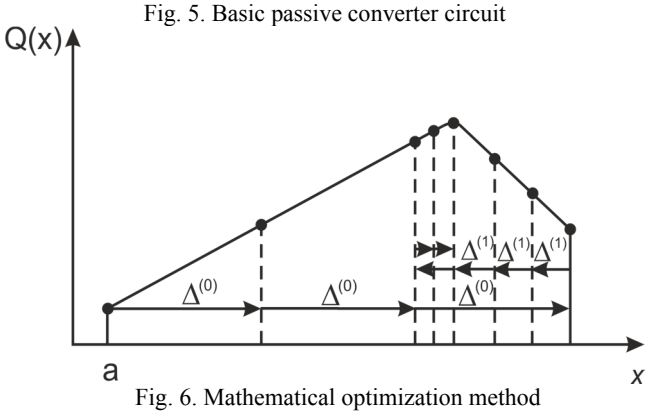

Fig. 6. Mathematical optimization method

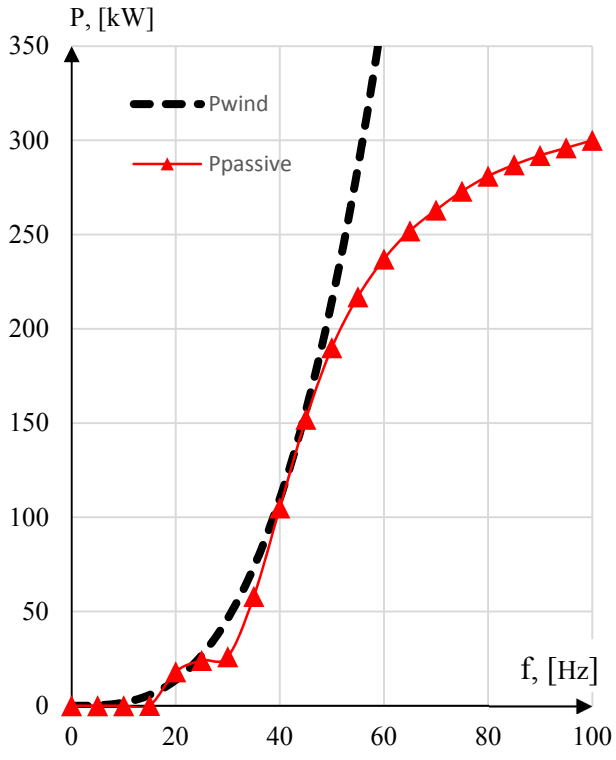

Fig. 7. Power/frequency curve with use of passive converter

The study of the schematic involves multiple iterations to perform the comparison using three computer software products (OrCAD Capture CIS, OrCAD Pspice, MathCAD).

As an example a simulation of mid-sized wind turbine with nominal output power of 100kW, has the following values and simulation parameters:

- Generator inductors value – 38mH;
- External inductors value – 120mH;
- EMF constant 40V/Hz;
- DC link voltage 1000V;
- Coarse step size generator inductors 10mH;
- Fine step size generator inductors 1mH;
- Coarse step size external inductors 20mH;
- Fine step size external inductors 10mH.

Some conclusions from the passive converter simulation can be classified as follows:

- The high frequency area in figure 7 is determined by the generator windings inductance value;
- The external inductance influences mainly the lower frequency area on the power-frequency curve;
- Lower EMF values lead to higher inception point.

Analysis of the achieved results of application of passive converter show small deviation from the ideal cubic dependence. So, it is worthwhile to compare the annual output of this configuration of converters and the system with use of actively controlled rectifier.

B. Design of AC inductors

The parameters of included AC inductors are decisive for the total efficiency and performance of the passive converter. An advanced design algorithm is applied including precise eddy current losses calculation in copper. The algorithm consists of 15 steps [7]. The eddy current losses in windings are found as:

$$P_{eddy} = (R_0 . I_{ac}^2) . k_c \qquad (3)$$

, where k_c is eddy current loss factor; I_{ac} is the AC current component; R_0 is the ohmic resistance of the winding.

The coefficient k_c is given as:

$$k_c = \frac{1}{48} . \zeta^4 . {m_E}^2 . \eta^2 . \frac{\pi^2}{4} . k_F . \frac{1}{\sqrt{\frac{1+G_T}{1024}}} \qquad (4)$$

Where ζ is the ratio between wire diameter and penetration depth; m_E is an equivalent number of winding's layers; η is a copper fill factor in the direction of the layer; G_T is a quantity introduced to realize approximation of the exact analytical solution of the losses in a transverse field; here we use the expression $G_T = (\zeta+0{,}37)^6$ found by comparison with FEM calculations; k_F is a field factor coefficient.

The field factor coefficient k_F represents the magnetic field pattern over the winding. Full analytical and geometric presentation is given in [7] as a function of d_{wg}- distance between the winding and the leg, t_w- thickness of the winding , w- winding width and K - field symmetry factor.

Included AC inductors are design with ferrite materials and alternative nanocrystalline materials: Ferrite N87 (EPCOS) and Vitroperm 500F (Vacuumschmelze). Vitroperm 500F shows low losses and high saturation induction. The calculated designs show significant improvement of size, volume (up to two times reduction) and losses when nanocrystalline cores are used.

IV. Performance Comparison Results

For this comparison we accept that the active rectifier performs at maximum theoretical power and its control unit follows strictly the ideal cubic dependence. The passive one is tested at its worst case - 28÷38Hz area of the curve. The conversion from Hz to m/s and vice versa is done for nominal wind speed of 6 m/s at 40Hz and power output of 110kW. There are 10% losses to be considered due to mechanical losses. Three tables are presented with results of the comparison and the difference in the performance expressed in percent. A graphical comparison is also shown on figure 8 for ease of data analysis.

Table 2. Performance comparison at 40 meters

Months	V_{avg}, [m/s]	P_{active}, [kW]	$P_{passive}$, [kW]	Diff, [%]
January	4,8	56,32	35,82	36,40
February	5,2	71,61	56,98	20,43
March	5,9	104,59	100,93	3,50
April	5,0	63,66	45,75	28,13
May	5,1	67,55	51,25	24,13
June	4,4	43,38	25,26	41,77
July	4,2	37,73	25,05	33,61
August	4,2	37,73	25,05	33,61
September	4,9	59,91	40,64	32,17
October	5,2	71,61	56,98	20,43
November	5,7	94,31	87,94	6,76
December	5,5	84,73	75,20	11,25

Table 3. Performance comparison at 50 meters

Months	V_{avg}, [m/s]	P_{active}, [kW]	$P_{passive}$, [kW]	Diff, [%]
January	5,1	67,55	51,25	24,13
February	5,5	84,73	75,20	11,25
March	6,2	121,37	120,46	0,75
April	5,2	71,61	56,98	20,43
May	5,3	75,82	62,84	17,12
June	4,6	49,57	27,68	44,16
July	4,3	40,49	25,13	37,93
August	4,3	40,49	25,13	37,93
September	5,2	71,61	56,98	20,43
October	5,5	84,73	75,20	11,25
November	6,0	110,00	105,00	4,55
December	5,8	99,36	94,37	5,02

Table 4. Performance comparison at 60 meters

Months	V_{avg}, [m/s]	P_{active}, [kW]	$P_{passive}$, [kW]	Diff, [%]
January	5,3	75,82	62,84	17,12
February	5,7	94,31	87,94	6,76
March	6,5	139,86	134,00	4,19
April	5,5	84,73	75,20	11,25
May	5,5	84,73	75,20	11,25
June	4,8	56,32	35,82	36,40
July	4,5	46,41	26,00	43,97
August	4,5	46,41	26,00	43,97
September	5,4	80,19	68,95	14,02
October	5,7	94,31	87,94	6,76
November	6,5	139,86	134,00	4,19
December	6,0	110,00	105,00	4,55

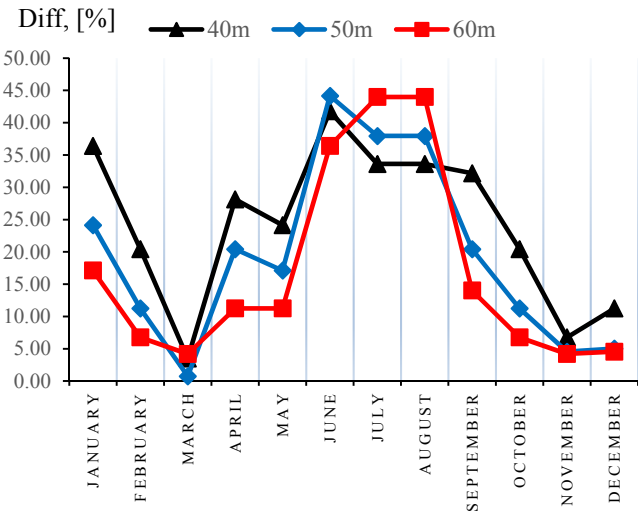

Fig. 8. Graphical comparison of difference in performance of active rectifier and passive converter circuit in a year period

V. Conclusion

Comparison of the power output difference with active and passive control is made and expressed in percent in tables. An actual wind resource data gives the opportunity to have evaluation at three different heights and as a result graphical comparison as well.

The following conclusions are derived based on the carried out comparative study:

- Active control circuits are preferred in cases when the quantity of generated energy is the dominant factor;
- Passive converter circuit performs better at and around the preset production nominal wind speed. So it is important to have accurate assessment data at the site of wind turbine installation;
- Passive control circuits are recommended when the initial investment, reliability and maintenance costs are important for the final estimation of the economic and technical performance of the system.

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Industrial Application of Induction Brazing Systems

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Abstract – **Induction heating systems have wide range of applications. Brazing process - joining two metal parts using filler material, is important part of these. Focus of this article is on the induction heating process implemented in brazing solutions. A brief review of the process is given at the first part. General classification of induction heating systems is described for quick reference. Theoretical and experimental guide lines are included to help during proper system selection and solution implementation.**

Keywords – **Induction heating systems, Brazing, Induction Brazing.**

I. BRAZING PROCESS

Brazing is a joining process, which produces coalescence of materials by heating to a suitable temperature and by using a filler metal (often referred to as braze) having a liquidus temperature above 450ºC and below the solidus temperature of the base material. The filler metal is drawn into the gap between the closely fitted surfaces of the joint by capillary action. To achieve a perfect joint, the filler and the parent materials should be metallurgically compatible and the design of the joint should incorporate a minimum gap into which the braze filler metal will be drawn. The joints must be properly cleaned and protected by the flux or protective atmosphere during the heating process to prevent excessive oxidation. There are many ways of brazing, and they all differ in the method of applying heat to the braze assembly, in particular, the joint area. These include torch brazing, furnace brazing, induction brazing, dip brazing, and resistance brazing.

Soldering is a joining process, which produce coalescence of material by heating them to the soldering temperature and by using a filler metal (solder) having liquidus temperature not exceeding 450ºC and below the solidus temperature of the base metals. Similar to brazing the filler metal is drawn into the gap between the closely fitted surfaces of the joint by capillary action. Usually, a nonferrous alloy is used as solder material. There are many ways of soldering, and alike brazing, they also differ in the method of applying heat to the solder assembly, in particular, the joint area. The main soldering variants include soldering iron, torch soldering, dip soldering, wave and cascade soldering, induction soldering, resistance soldering.

II. ADVANTAGES OF INDUCTION SYSTEMS

Induction heating lends itself to brazing and soldering because of its ability to heat selectively, rapidly and consistently. The induction process reduces part distortion, annealing and damage to the metal surface. Induction heating can also be applied to a wide variety of materials including ceramics, plastics and composite materials. For ceramics and plastics, it is necessary to apply a surface metallization before joining.

Induction heating systems can be easily integrated into series production lines because of their high grade of automatization capabilities. This allows quick and easy implementation of complex processes and technologies. Amount of energy applied to joining parts can be quite precise controlled by using of induction systems. A temperature profile can be easily defined to fulfill process requirements in closest shape possible.

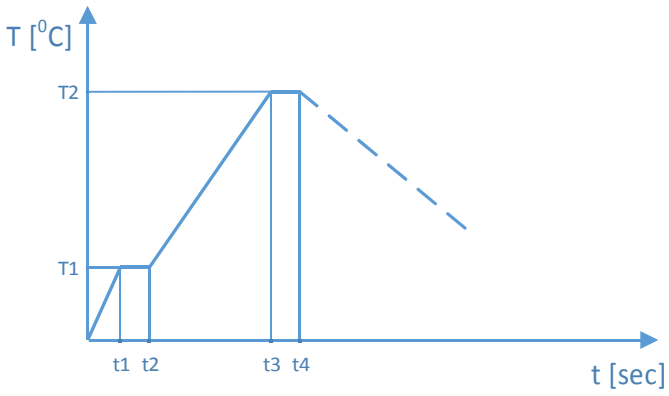

Fig. 1. Temperature profile

Two step temperature profile is shown on fig.1. Characteristic of this profile is temperature T1 presence, where the heating process is hold to constant value. This appears to be necessary when brazing paste is used because there is significant part of dissolvent (usually water) into it. Time interval t1 – t2 is determined by brazing paste quantity used and flux content. Need of this time is related to dissolvent evaporation, which would have boiled up otherwise and would spill the paste out of the joining area. Main heating appears to be in t2 – t3 time interval. The actual brazing process is shown in t3 – t4 time interval, where temperature T2 is kept constant due to equal distribution of brazing alloy into the joining area between parts.

Created once, such profile can be repeated multiple times. Collecting of the induction system parameters, which are easily acceptable, quality of the process can be guaranteed by implementing of monitoring systems. Following the power applied to the brazed parts during process cycle and total energy transferred, monitoring system estimates quality of the joint and report when discrepancy appears.

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III. INDUCTION SYSTEMS TYPES

Induction heating systems are classified by two main parameters:

- Power – this is a maximum achievable power of induction generator. It defines system capability to reach referred temperature and time needed. In general, induction heating systems used in brazing process are in 3kW to 20kW range. To achieve higher production rates systems up to 50kW may take place.

- Frequency – this is working frequency range where the induction generator operates at predefined power. According to this parameter, the following main frequency ranges can be defined [4]:

  - o L – 10kHz – 50kHz – low frequency;
  - o M – 50kHz – 150kHz – medium frequency;
  - o H – 150kHz – 400kHz – high frequency;
  - o SB – 700kHz – 1200kHz – very high frequency;

Systems used in induction brazing process are usually in medium frequency range (M) and in very high frequency range (SB).

IV. INDUCTION HEATING SYSTEM SELECT

Depending on selected target such as material of the joining parts, size of the assembly, brazing alloy and production rate of the process, a different requirement to induction heating systems are set. Use of classical equations can define the energy parameters of the system:

$$P_w = \frac{mc(T_{final} - T_{initial})}{t} \quad (1)$$

where:

- P_w is the workpiece power.
- m is mass of the workpiece.
- T_{final} and $T_{initial}$ are the average values of initial and final temperatures.
- c is the average value of the specific heat of the material.
- t is the required heating time.

Considering that Pw represents the power needed to heat the piece, the power the converter has to provide is bigger due to the losses. Thus, the effective power of the converter is [2, p. 143]:

$$P_c = \frac{P_w}{\eta_T} \quad (2)$$

where

$$\eta_T = \eta_{Thermal}\eta_{electrical} \quad (3)$$

which considers the thermal and electrical efficiency.

For cylindrical coils with concrete as a refractory, the following formulas can be used [2, p. 144]:

$$\eta_{Thermal} = \frac{P_w}{P_w + P_{thermallosses}} \quad (4)$$

and:

$$P_{thermallosses} = 3{,}74.10^{-7}.\frac{l_c}{\log_{10}\left(\frac{d_c}{d_w}\right)} \quad (5)$$

- $P_{Thermallosses}$ are thermal losses through the surface.
- d_c and d_w are the inside coil diameter and workpiece diameter, respectively.
- l_c is the coil length.

Electrical efficiency:

$$\eta_{electrical} = \frac{1}{1 + \frac{d_c + \delta_c}{d_w - \delta_w}.\sqrt{\frac{\rho_c}{\mu_r \rho_w}}} \quad (6)$$

where,

- δ_c and δ_w are coil and workpiece's penetration depth, respectively.
- ρ_c and ρ_w are coil and workpiece's electrical resistivity, respectively.
- μ_r is the relative magnetic permeability of the workpiece.

Penetration equation is given below:

$$\delta = \sqrt{\frac{2\rho}{\mu\omega}} = 503\sqrt{\frac{\rho}{\mu_r f}} \quad (7)$$

where

- δ is the penetration depth.
- f is the frequency of the current, that is the same as the original one, and ω is the angular frequency with $\omega = 2\pi f$.
- ρ is the resistivity of the material.
- μ_r is the relative magnetic permeability of the material, which is adimensional ($\mu = \mu_r\mu_0$, where $\mu_0 = 4\pi \cdot 10^{-7} H/m$ for vacuum).

When choosing induction heating system, a maximum effective and efficient process is targeted to be selected. This means that minimum required power has to be chosen and minimum time for heating, allowed by the temperature process. When very fast heating rate is used (high power level respectively) surface melting of the parts is possible which is not acceptable. On the other hand, maximum temperature has to be closely observed and it must not reach

critical value i.e. has to be kept below the melting point of the parts. If joining parts are made of different materials, then lower melting point temperature has to be taken.

Usually during brazing process, not the whole mass of the assembly is going to be heated. Coil is concentrated on the joining area. This is relatively complex estimation which is highly related to the time for heating and the thermal conductivity of the materials as well. Difficulties sometimes come from complex shapes of the joining parts too. Often computer simulation and application tests are used for process definition and estimation.

Coil Design

As in torch brazing, the parts to be joined must reach the same temperature at the same time to provide capillary action. Hotter areas will cause the alloy to move toward the hottest part of the assembly. This is further complicated not only by the largest mass in the assembly but by the material as well. Because of the differences in resistivity of materials and the fact that heating with a high frequency current is based on I2R, different materials will heat differently in an induction field. The same current that flows in a steel part may not bring a similar piece, made of copper, to the equivalent temperature in the same interval of time. Therefore, the coil must be designed to deliver more current to the greater mass/ lower resistivity material, while still bringing the mating part to temperature at the same time. This change in design of the coil requires placing either more turns at the greatest mass, or decreasing the coupling distance to the larger part so it receives more magnetic flux from the coil.

Efficiency of energy transfer to workpiece can vary in wide ranges from 15% to 85% depending on coil shape. Although induction heating method remains around two times more efficient in energy aspect. This comes from the fact that magnetic field heats workpiece directly.

V. GUIDELINES TO INDUCTION HEATING SYSTEMS FOR METAL PARTS BRAZING PROCESS.

Here is an example of classical induction brazing of cylindrical assembly – outside and inside located coil. [7]

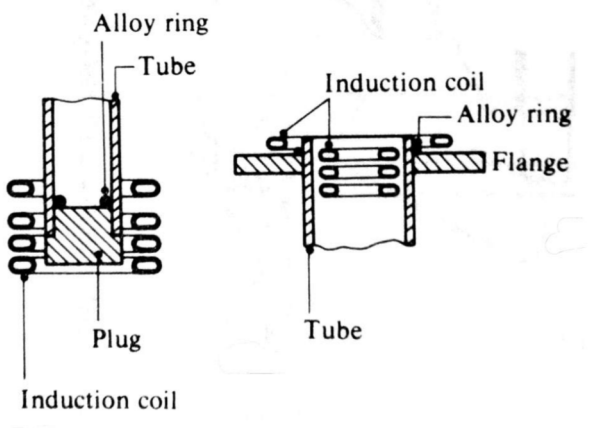

Fig. 2. Induction brazing.

Example of real working coils are given on fig.3 [7]

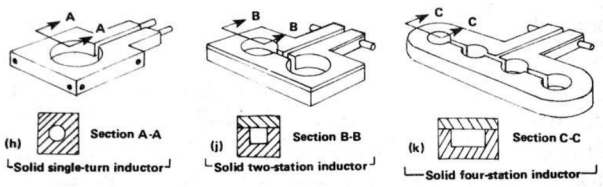

Fig. 3. Induction brazing coils.

In real applications a complex shape coils have to be used quite often in order to achieve equality of heating.

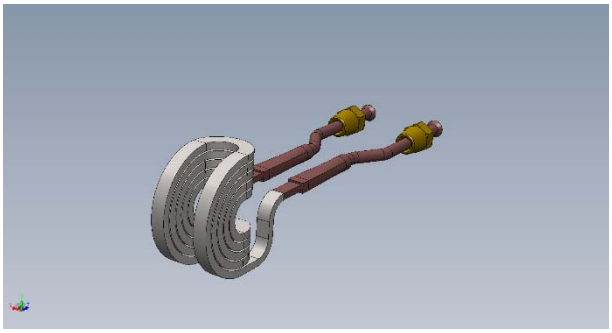

Fig .4. Complex shape coil – open type

Complete outlet system in shape of portable gun for induction brazing:

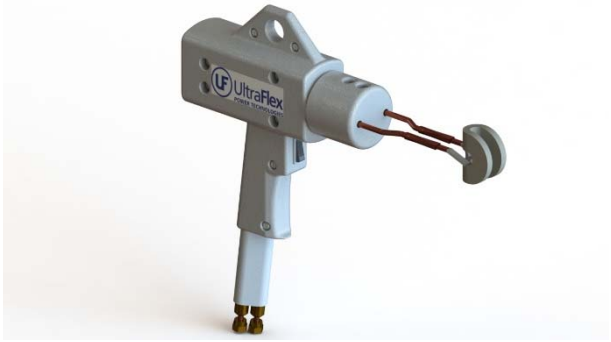

Fig. 5. Induction brazing gun

Real example about implementation of this system is reported by UltraFlex Power Technologies [4].

Induction brazing of refrigerator system pipes. A complex shape type coil (open type) has to be used because the final product cannot be disassembled. In this case is used "C – type" shape.

Difficulty during implementation of given task is the small size and the material of the joining parts. Copper is a non-magnetic material but has got very good electrical and thermal conductivity at the same time. As it can be seen from (6) these properties lower the electrical efficiency. This leads to a coil with more turns (in this case 5) and relatively large operating current.

TABLE 1 APPLICATION TEST DATA

Diameter of brazing parts (pipes):	6mm – 8mm
Material:	Copper
Temperature of brazing:	800^0C
Time for brazing:	4 sec
Power used:	12kW
Working frequency:	134kHz

Fig. 6. Brazing area of the assembly

When using a flame torch the same process takes 20 seconds per joint and it is highly dependable on torch operator assessment. By using of induction method, time for brazing is set by induction generator and it is constantly fixed.

Using (1) and entering the data about copper and size of heating area – 50mm respectively:

$$\boldsymbol{m} = 12.7g,\ \boldsymbol{c} = 0.384\ kJ/kg.^0C,\ \boldsymbol{t} = 4\ sec,$$
$$\boldsymbol{T_{initial}} = 25^0C,\ \boldsymbol{T_{final}} = 800^0C$$

Get the needed heating power: Pw = 0.947kW.

Table data of laboratory application tests of the company [4] shows that current coil used has 15% (ηe = 0.15) efficiency when copper is heated. This includes all power losses into the coil related to the conductivity and the magnetic flux leakage. Energy losses related to the thermal conductivity are around 50% (ηT=0.65). Than according to (2) the power of the generator is:

$$P_c = \frac{P_w}{\eta_e \eta_T} = \frac{0.947}{0.15 \times 0.65} = 9.712kW$$

It can be seen that there is a difference between calculated and measured values which comes from power losses into induction generator and output circuit. In this case the declared system efficiency is 85% [4] which relays to the real measurement given in Table 1.

Choosing a working frequency is not critical in this case. Chosen value is adapted to the operating frequency range of the system.

VI. CONCLUSION

Target of this article was to uncover the potential of induction heating in brazing processes. In short terms were reviewed main steps of process implementation.

Using combination of computer simulated calculations, based on induction heating theory and application data, gives powerful method for determination of induction system parameters. Using systems with large wide frequency range and power flexibility makes implementation of the induction brazing process easier and reliable. Such systems are available at present time. Induction brazing is not just modern process, it solves many process issues and gives new opportunities in almost every assembling area.

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Considerations for Components Selection of Inverter for Induction Heating

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Abstract – **The paper presents study and selection of components (power switches and inductor) of an inverter for induction heating. Power losses in the switches and inductor windings are considered. The comparative study is realized based on using three different types of power switches (IGBT's, MOSFET's and SiC-MOSFET's). Presented loss analyses leads to design requirements for selection of proper switches (SiC) and winding arrangements. Possible solutions and design approaches are presented for reducing losses in the coil of the inductor. Design conclusions and recommendations are derived to optimize the induction heating system.**

Keywords – **Power electronic converters, switching losses, Winding arrangements**

I. INTRODUCTION

Requirements to power invertors for induction heating of fluids are increased as the challenges for low energy consumption are more and more important. An induction heating system consists basically of one or several inductors and feromagnitic pipes to be heated. Design and losses in the inductor is decisive for the total efficiency of the system. Induction heating of fluids is widely used in industrial and in domestic appliances because of possibility for faster heating and avoiding scale [1], [2]. The reliability and protection methods for power circuits of induction heating systems are presented in [3]. Numerical and FEM modelling of induction heating is presented in [4],[5].

Considering the relatively high power of the induction boiler, usually bridge topologies are applied for the power stage. Power switches are MOSFET's or IGBT's.

The purpose of the paper is to investigate losses in the switches and in the inductor in order to improve the selection of proper switches and winding arrangements.

The total losses in the power stage are given as:

$$P_{tot} = P_{rec} + P_{sw} + P_{ind} \quad (1)$$

where: P_{tot} – total losses in the power stage;
P_{rec} – losses in the input rectifier;
P_{sw} – losses in the switches of the inverter;
P_{ind} – losses in the inductor.

The analyzed resonant inverter used in the system is shown in fig.1

II. ANALYSIS OF POWER LOSSES IN SWITCHES

The nominal parameters of the inverter at output power of Po=6kW are: V1=300V, R1=0.1Ω; Lk1=18μH; RL1=3,5Ω; Lk2=26μH; RL2=4Ω; Ck=0,67μF; fnom=50kHz [1]

The inductor is split in two parts: serial inductance (Lk1), and parallel inductance (Lk2). These two parts are assembled on the same pipe. The resistances RL1 and RL2 represent the heat generated in the pipe. Both inductances Lk1 and Lk2 and the capacitor Ck define the resonant frequency of the inverter. The resistor R1 represents the power losses in the wires and the DC supply.

The current research is targeted at comparison of the use of MOSTET's, IGBT's and SiC MOSTET's to realize and operate the inverter at different frequencies.

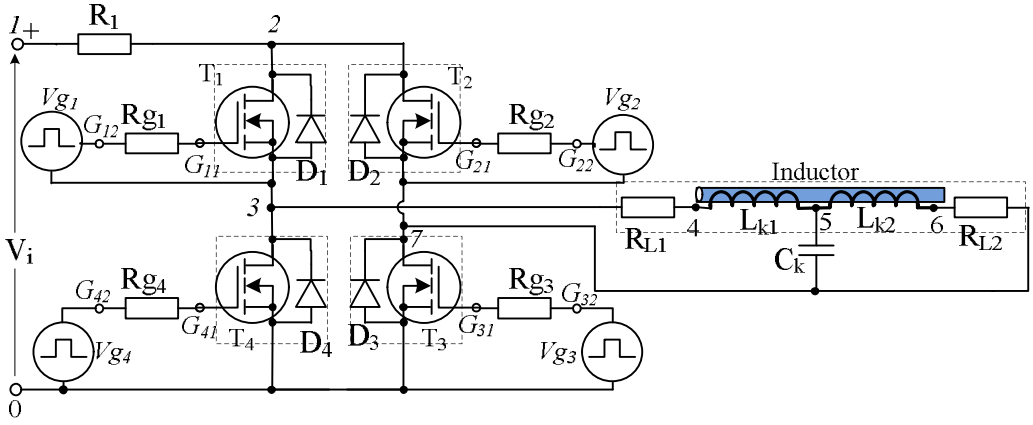

Fig.1. PSpice model scheme of the resonant LCL inverter used in the induction heating system.

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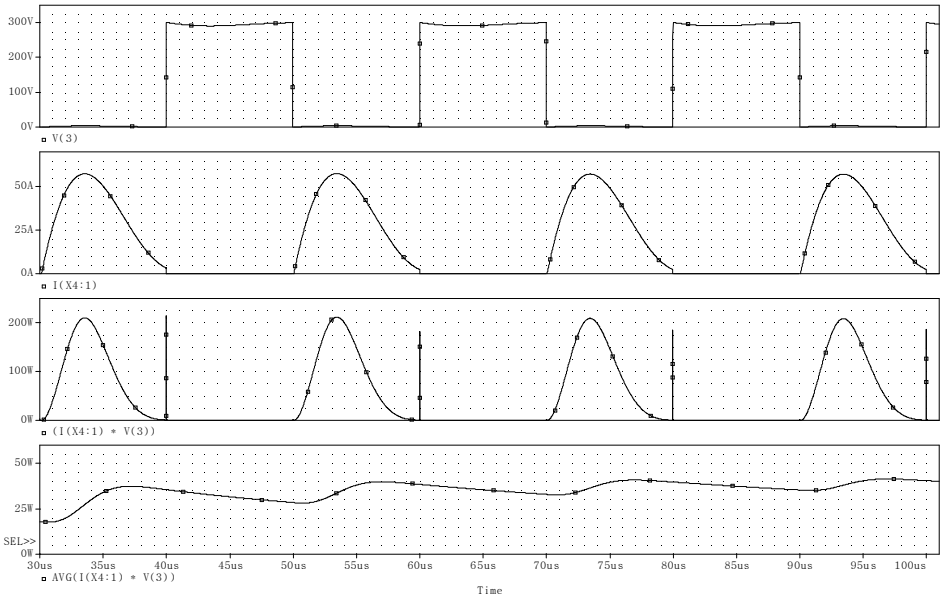

Fig. 2. Voltage, current and power loss of a MOSFET switch of the investigated resonant inverter

The simulations are realized using PSpice analysis based on models of the switches under study.

Two different studies are carried out:

- comparison of performance of switches with different operating parameters (the same type);
- comparison of performance of switches with almost the same operating parameters, but different types: MOSTET's, IGBT's and SiC MOSTET's.

Finally design considerations are derived concerning winding arrangement and used wires of the inductor, based on the eddy current losses analysis.

A. Analysis of power losses in switches with different operating parameters (MOSFET's)

The operation of the resonant inverter in nominal mode using MOSFET's is shown in Fig.2. Soft switching (ZVS and ZCS) is obtained, thus reducing the switching losses.

The losses in two different MOSFETs are obtained by the simulations and shown in Table 1 (parameters of the switches correspond to the calculated voltages and currents) and in Table 2 (switches with higher nominal parameters).

TABLE 1. LOSSES IN THE SWITCHES, MOSFET'S

MOSFETs- IRFP 460N										
f	kHz	20	30	40	50	60	70	80	90	100
Po	kW	7,2	5,4	5,3	8,3	10,8	8,2	5,2	3,9	3
Pz	W	95	56	49	140	275	224	135	100	75
η		0,91	0,92	0,91	0,89	0,86	0,86	0,87	0,88	0,88

TABLE 2. LOSSES IN THE SWITCHES, MOSFET'S WITH HIGHER NOMINAL PARAMETERS

MOSFETs- IXFN 64N60P										
f	kHz	20	30	40	50	60	70	80	90	100
Po	kW	7,8	5,7	5,5	9	11,9	9,1	5,5	4,2	3,1
Pz	W	25	14	13	40	100	70	40	31	23
η		0,95	0,95	0,94	0,91	0,87	0,89	0,90	0,87	0,9

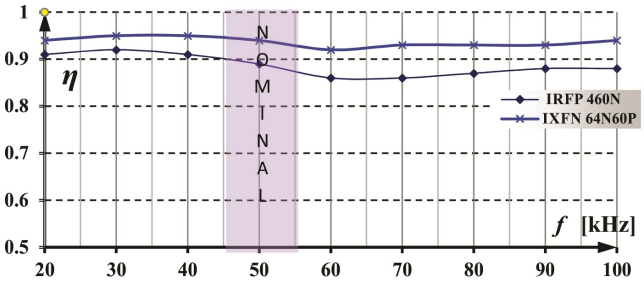

Fig. 3. Efficiency of the inverter power stage realized by MOSFET's

B. Analysis of power losses in IGBT's with different operating parameters

The same approach: comparing performance of the power stage with IGBT's with parameters corresponding to calculated voltages and currents and with switches with higher nominal parameters is realized and shown in Fig.4.

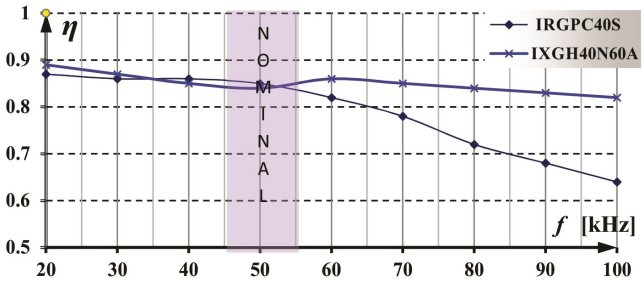

Fig. 4. Efficiency of the inverter power stage realized by IGBT's

TABLE 3. MAIN OPERATING PARAMETERS OF THE SWITCHES USED FOR COMPARATIVE STUDY

Device	Parameter	Vdss/ces	Ic40	Rds(on)	Vce(sat)	trr/tri	Ciss/Cies	Coss/Coes	Crss/Cres	Qg
	Unit	V	A	mΩ	V	ns	nF	pF	pF	nC
SiC MOSFET	SCT30N120	1200	45	90		20	1,7	130	25	105
MOSFET	IXFN 64N60P	600	65	96		200	12	1150	80	200
IGBT	IXGH 40 N60	600	75		2,5(≈89mΩ)	200	4,5	300	60	200

C. Analysis of power losses in switches with the same operating parameters, but different types: MOSTET's, IGBT's and SiC MOSTET's.

This study is most important as it includes switches with the same operating parameters, but different types: MOSTET's, IGBT's and SiC MOSTET's. Main operating paramets of the switches used for the comparative study are shown in Table 3.

The results for the power losses and the efficiency obtained when using SiC MOSFETs are shown in Table 4.

TABLE 4. LOSSES IN THE SWITCHES, SIC MOSFET'S

MOSFET- SiC- SCT30N120_V3										
f	kHz	20	30	40	50	60	70	80	90	100
Po	kW	7,1	6	6,8	8,9	9,5	8,1	5,5	4,3	3,3
Pz	W	19	14	19	39	80	56	33	26	19
η		0,94	0,95	0,95	0,94	0,92	0,93	0,93	0,93	0,94

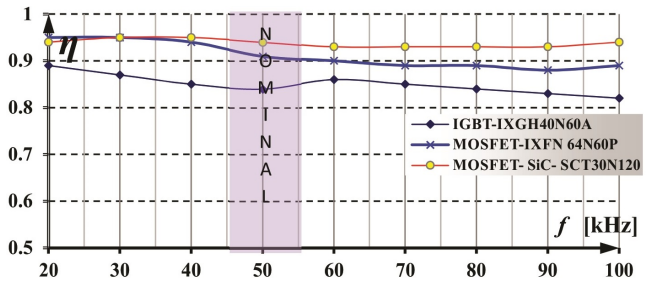

Fig.5. Efficiency of the inverter power stage realized by different types: MOSTET's, IGBT's and SiC MOSTET's.

Final comparison of the efficiency is shown in Fig.5. Power losses in the switches are a function of the operating frequency are shown in Fig.6

III. DESIGN AND LOSS ANALYSIS OF THE INDUCTOR WINDINGS

An improved design methodology for dimensioning inductors for induction heating is presented in [6]. Two different constructions are considered: cylindrical one, Fig.7, and improved one with higher efficiency. The main sources of losses in such an inductor are eddy currents in wires of the inductor.

In a general case, the eddy current losses in windings are given as [7]:

$$P_{eddy} = (R_0 I_{ac}^2)\, k_c \qquad (2)$$

where k_c is eddy current loss factor;
I_{ac} is the AC current component;
R_0 is the ohmic resistance of the winding.

In the inductor cases, for inductors with turns consisting of a few conductors in parallel or Litz wire, the coefficient k_c is given as:

$$k_c = \left(\frac{p\, N\, d_p}{\omega}\right)^2 k_F\, k_{in} \qquad (3)$$

where k_F is a field factor coefficient represents the magnetic field pattern over the coil;
p is the number of wires in parallel, or conductors in a Litz wire;
N is the turns number; d_p is the wire diameter;
k_{in} is used to simplify geometric parameters and it is given as a graphical presentation in [7].

A few possible winding arrangements of the inductor coil for the investigated induction heating system are analyzed and compared. Based on the loss analysis the following recommendations are derived: one layer design shows best efficiency, possible use of Litz wire results in further loss reduction, designs with a few in parallel are also recommended to reduce skin effect and thus, total eddy current losses.

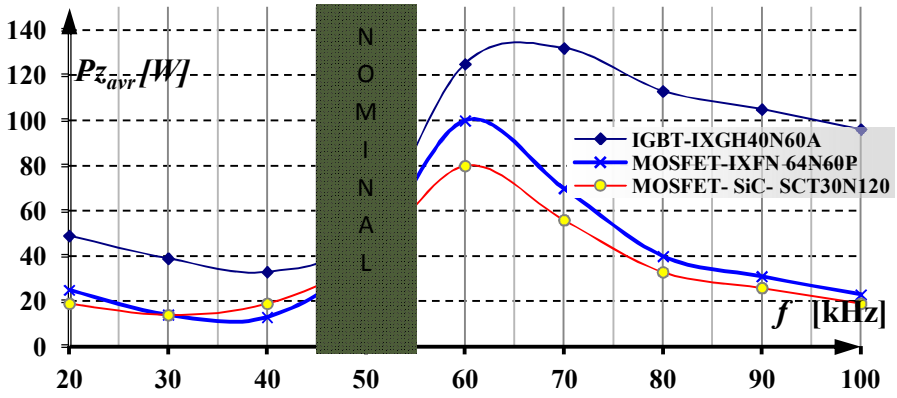

Fig. 6. Power losses in the switches are a function of the operating frequency

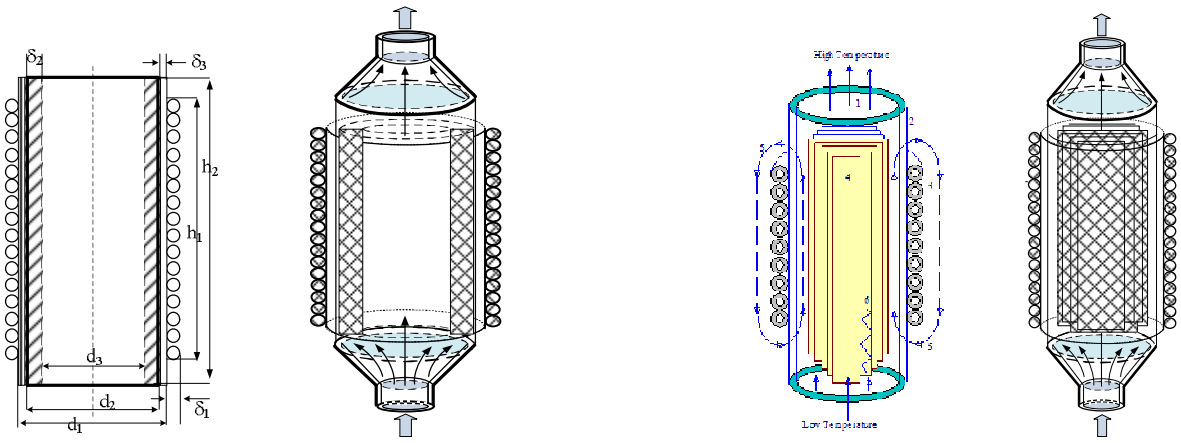

Fig. 7. Cylindrical inductor, a); improved inductor, b).

IV. Conclusion

Based on the carried out simulations and analysis the following conclusions are made in respect to power switches:

- Reduction of losses is possible using switches with higher parameters than the calculated based on voltages and currents through the switches.
- If the efficiency of the power stage is the dominant target of the design, then the selected switches are to have current limits at least one and a half of the RMS values of currents through them in the corresponding power stage.
- The values of the capacitances of the switches influence the operation of resonant converters and have to be considered in the design to maintain the optimal operating conditions in respect to power losses.
- Power losses in the switches depend strongly on the current waveforms and type of switching process.
- The comparative study of the efficiency performance of the resonant full bridge converter for induction heating under different types of switches shows the best results are obtained using SiC MOSFET's.

To reduce the losses in windings of the inductor of induction heating systems using Litz wire is recommended. Another approach is using a few wires in parallel. Coil arrangement with one layer is the recommended approach.

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Current Fed Inverter Application as a Controllable DC Load

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Abstract – **High precision electronic DC loads are necessary for testing the characteristics of switching power supplies, DC power sources such as photovoltaics, fuel cells. Variable electronic loads can be controlled from a remote computer for testing equipment in remote areas and other specific research & development or educational purposes. Electronic loads can also be used in distant control of the test equipment. This paper presents an application of a current fed inverter as controllable DC load. The studied topology is a parallel full bridge inverter with thyristors. The control loop is based on a PI regulator and is realized by variable switching frequency and constant duty ratio.**

Keywords – **Power electronic, Controllable DC load, Current fed inverter, Energy recycling**

I. INTRODUCTION

Electronic DC loads have a range of applications in applied engineering and R&D, which include testing of power supplies and DC power sources such as fuel cells and PV generators (fig.1). They are also used for testing steady-state or transient characteristics of generators, including also student laboratory assignments.

The main requirements for DC loads are [1-6]:

- Compact volume and weight
- Wide range of control of the load input impedance
- Precision in the control of current and power drawn from the DC source
- Scalability - parallel connection of several loads for increasing input power range

The simplest usual way of testing batteries, obtaining their polarization curves or photovoltaic generator I-V curves is through series connection of variable resistors. But this is impractical for a powers superior than few hundred watts because it is related with high losses and doesn't provide the necessary precision, because of the resistance temperature dependence and the absence of a current control loop [1-3]. Also the large volume of such equipment can be considered another disadvantage.

Another relatively simple method is the use of a MOSFET transistor and an operational amplifier as a variable load (fig.1) [4]: the resistance between drain and source is modulated through the gate-source voltage. The MOSFET in this method operates in three operation modes (cut-off, active and ohmic region). As a result, most of the power delivered by the source has to be dissipated by the transistor, which limits its application to a relatively low power.

For the convenience of broader power range and better input current accuracy, PWM switching circuits have been studied and tested in the recent years [2-5]. Subject of most of the studies and researches on this subject are DC-DC converters application as electronic load. Different topologies are examined: the Buck converter is not applicable for this purpose, because of the discontinuous input current [3]. The most often used topology is the Boost converter (fig.2). This is mainly because the circuit sizing methodology for Sepic or Ćuk converters is more complex than the Boost and in general they do not possess considerable advantages in this particular application, compared to the boost converter circuit. By the use of an electronic converter, the power is dissipated in the load resistance and in the switching elements (fig.2).

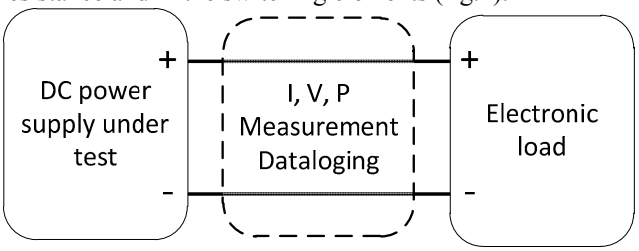

Fig. 1. Test bench for DC power sources

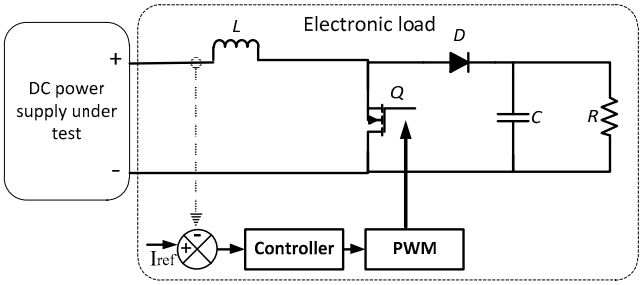

Fig. 2. Boost chopper as electronic load

For testing DC and three-phase AC sources with power greater than several kW energy recycling devices have been developed (fig.3) [3-5]. These consist of a DC chopper (or rectifier when testing AC generators) and a grid-connected single- or three-phase inverter. This configuration raises the maximum power that the load can consume as most of the power drawn from the source is injected to the grid. In this way the energy is "recycled", instead of being dissipated in heat sinks. This allows testing of sources with rated power up to hundreds of kilowatts.

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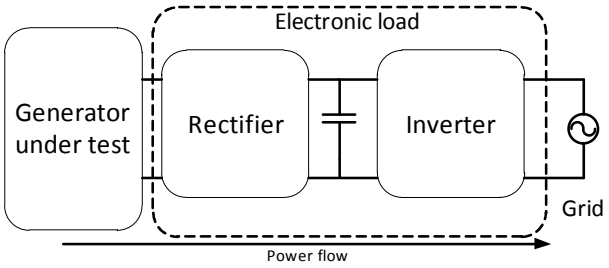

Fig. 3. Testing power sources by energy recycling

II. CURRENT FED INVERTER APPLICATION AS ELECTRONIC LOAD

In this paper a current fed bridge inverter circuit (fig.4) is used as a controllable DC load. The characteristics required for this appliance are enumerated in table 1. The switching devices are thyristors, but bipolar or MOSFET transistors can be used as well. The inverter equivalent circuit is presented on fig. 5. The current drawn from the source can be considered constant and with zero ripple if the inductance L_d is high enough. The values of the RC branch are constant. If the duty ratio is also fixed, then the current drawn from the source is a function of the switching frequency *f*. In other words, the circuit equivalent impedance is proportional to the switching period *T*.

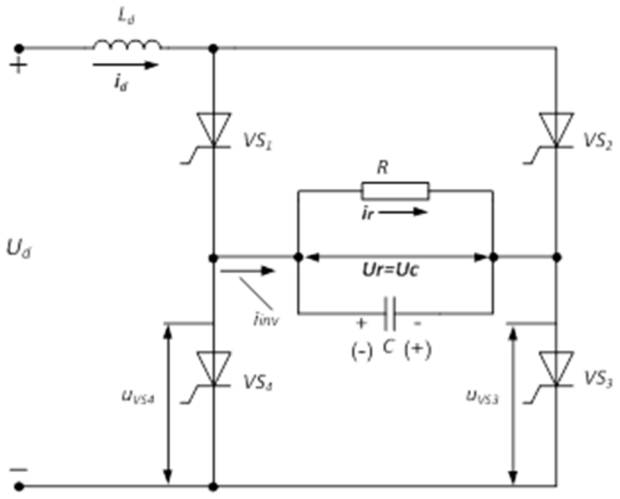

Fig. 4. Current fed inverter circuit

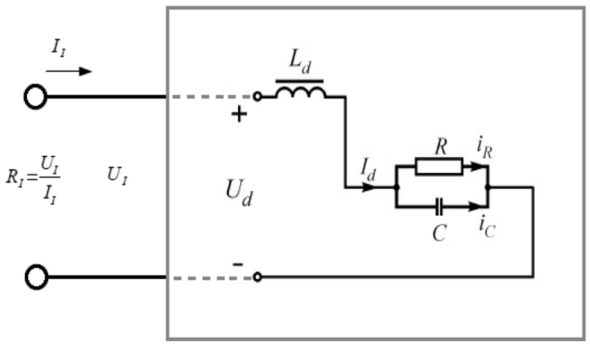

Fig. 5. Equivalent circuit

The circuit analysis is performed under the following adoptions:

- The DC source under study is idealized
- The switching devices, thyristors in this study, are idealized (the voltage drop by conduction is zero).
- The resistance of the input inductor is zero.

These adoptions do not add a considerable loss of precision in the results [6]. The duty ratio of the inverter is 0,5. The value of the input current is controlled by variation of the switching frequency. The circuit operates with switching frequencies in range from 1000 to 19500 Hz to achieve the required range of equivalent impedance. The requirement for the current control loop is a resolution of 500mA or less and the ripple less than 150-200 mA.

TABLE 1. CHARACTERISTICS OF THE DC LOAD

Input voltage range	3÷25 V
Equivalent impedance range	1÷200 Ω
Dissipated power range	0÷525 W
Switching frequency range	1000 ÷20000 Hz

III. CIRCUIT ANALYSIS

The inverter equivalent circuit can be represented as an idealized current source connected in series to a parallel RC load. The equation describing the circuit is [6-8]:

$$I_d = \frac{u_C}{R} + C\frac{du_C}{dt} \Rightarrow \frac{du_C}{dt} + \frac{1}{RC}u_C - \frac{I_d}{C} = 0 \quad (1)$$

Where I_d is the current drawn from the source, U_c is the capacitor voltage, R and C are the capacitance and the resistance of the RC branch. U_c is be expressed with the following equation:

$$u_C(t) = I_d R\left(1 + Ae^{\frac{-t}{RC}}\right) \quad (2)$$

The value of the constant A can be found, from the periodic capacitor voltage in both switching states:

$$u_C\left(t = -\frac{T}{4}\right) = -u_C\left(t = \frac{T}{4}\right) \quad (3)$$

This can be rewritten as:

$$I_d R\left(1 + Ae^{\frac{T}{4RC}}\right) = -I_d R\left(1 + Ae^{-\frac{T}{4RC}}\right) \quad (4)$$

Then the integration constant A is equal to:

$$A = -\frac{e^{\frac{T}{4RC}} + e^{-\frac{T}{4RC}}}{2} = -\frac{1}{\cosh\left(\frac{T}{4RC}\right)} \quad (5)$$

The switching period T is expressed from the switching frequency f and taking into account that the capacitor voltage U_c is equal to the voltage U_r is obtained the expression of the inverter input current I_d:

The current drawn from the DC source is:

$$I_d = \frac{U_d}{R\left(1 - 4fRC\tanh\left(\frac{1}{4fRC}\right)\right)} \quad (6)$$

The relation of the voltage applied on the load at the inverter output and the DC source voltage U_d is:

$$u_R(t) = \frac{U_d}{1 - \frac{4}{k}\tanh\left(\frac{k}{4}\right)}\left(1 - \frac{e^{-k\frac{t}{T}}}{\cosh\left(\frac{k}{4}\right)}\right) \quad (7)$$

Where k is the load coefficient, whose value is a function of switching frequency and the impedance of the RC branch:

$$k = \frac{1}{fRC} \quad (8)$$

The ratio of the equivalent input and output resistance of the studied circuit is expressed by:

$$\frac{R_i}{R_T} = 1 - \frac{4}{k}\tanh\left(\frac{k}{4}\right) \quad (9)$$

The relation between the DC source voltage (U_d) and the voltage across the RC load at the inverter output (U_r) is:

$$\frac{U_R}{U_d} = \frac{1}{\sqrt{1-\frac{4}{k}\tanh\left(\frac{k}{4}\right)}} \quad (10)$$

The circuit parameters are calculated once for F_{min}=1000 Hz the equivalent impedance of the circuit equals 200 Ω. After that, the maximum switching frequency is found by solving the equation for circuit equivalent impedance 1 Ω. The maximum frequency is 19346 Hz. Most of the modern thyristors are capable of operating with switching frequency up to 20 kHz.

For the input inductor L_d is chosen a value of 250mH in order to minimize the ripple current. In theory larger values of this inductance are better, but they tend to add inertia in the system response to profound changes in current reference.

The turn-off time required for restoring the thyristor valve properties should to be considered: on fig. 6 is plotted the relative turn off time t_q/T expressed in P.U. of the switching period T. Its value for this circuit at the maximum frequency of 19346 Hz is 0,24T or 12,43 µs.

The maximum instantaneous bias voltage applied on the switches also has to be taken into account in order to avoid malfunctions. It is equal to the maximum instantaneous value of the load capacitor U_c. The capacitor voltage has a peak in the switching instants: $t=0$, $t=T/2$, $t=T$ etc. The maximum DC source voltage of 25V and the maximal switching frequency are replaced in equation (7) and the value obtained is U_{VSmax}= -997 V.

TABLE 2. SPECIFICATION OF THE CIRCUIT ELEMENTS

R	510 Ω
C	330 nF
L_d	250 mH
Requirements for the switching thyristors:	
t_q	≤12 µs
U_{VSmax}	≥1000 V

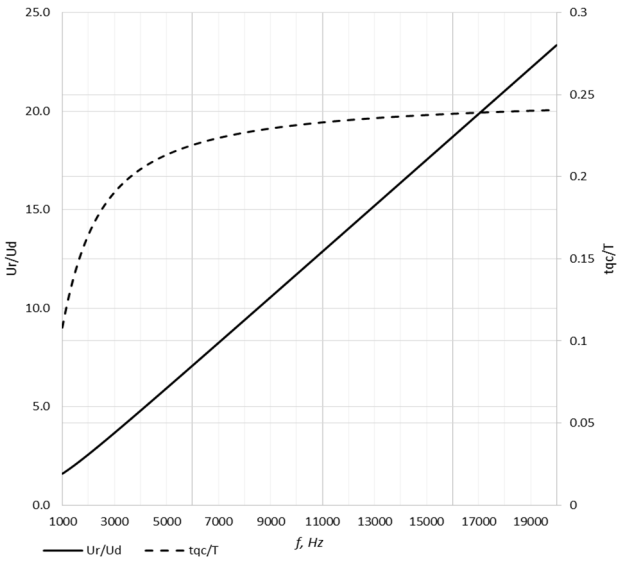

Fig. 6. Frequency analysis of *tq/T* and *Ur/Ud* of the inverter circuit.

IV. SYSTEM MODEL AND SIMULATION RESULTS

The system is modeled and simulated in MATLAB/Simulink environment (fig.7). The inverter is modeled by its switching equations [6-9]. A signal controlled oscillator drives rectangular pulses for gate signals of the switching thyristors. The switching frequency is controlled by PI regulator with current feedback loop, the integral constants *Kp* and *Ki* are tuned according to the Ziegler-Nichols method [7-9]. On fig. 8 and fig. 9 respectively are presented the test current reference signal I_{dref} and as result the current I_d drawn from the DC source. The system is following correctly the current reference ramp. Fig. 10 presents a more detailed view on the input current ripple. The bias voltage of one of the switching thyristors is shown on fig.11. It is in the boundaries determined by the circuit analysis.

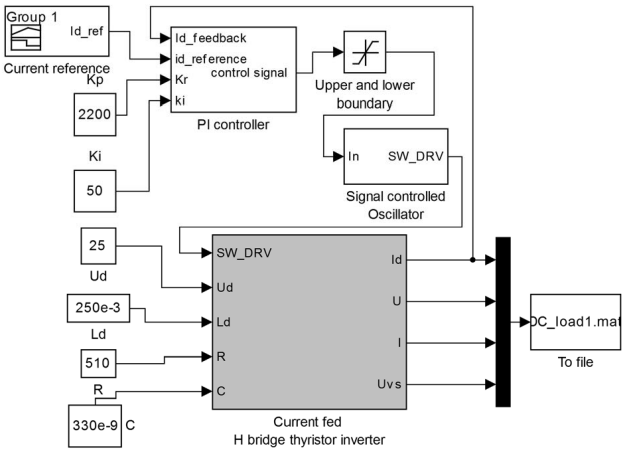

Fig. 7. MATLAB/Simulink model diagram

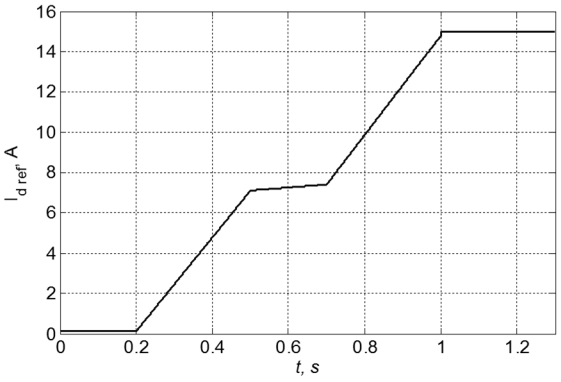

Fig. 8. Reference signal for the DC current I_{d_ref} (A)

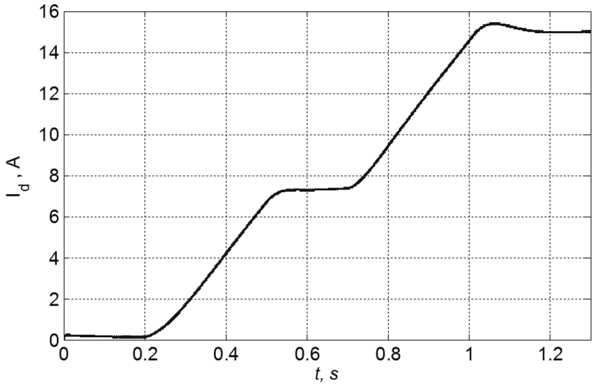

Fig. 9. Current drawn from the source I_d (A)

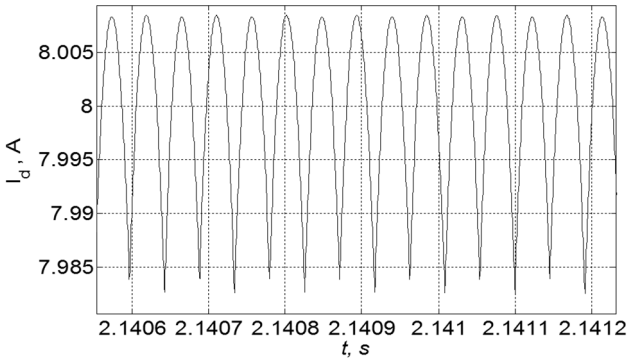

Fig. 10. I_d current ripple (A)

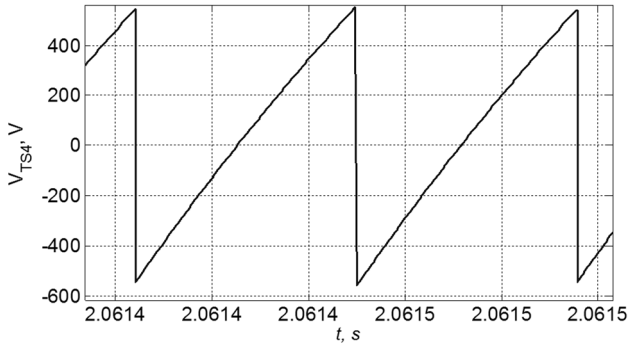

Fig. 11. Bias voltage on the thyristors: V_{TS4}, V

V. Conclusion

A current fed inverter application as controllable DC load is presented in this paper. The circuit synthesis and equations are presented and the elements are calculated to obtain the required characteristics: input voltage of up to 25V, load equivalent impedance from 1 to 200 Ω and switching frequency less than 20 kHz which allows the use of thyristors as switching elements. The inverter operates with constant duty ratio and variable switching frequency controlled by a closed current loop. The required characteristics of the switching thyristors: restoration time t_{qc} and maximum bias voltage V_{TS} are considered.

The MATLAB/Simulink system model is based on the inverter switching equations. Simulation results demonstrate correct system operation under step changes in the current reference, although the PI controller gives some overshoot. The voltage drop on the switching elements is in the specified range and the thyristor restoration time is as expected. The so synthetized inverter circuit is fully operational and a prototype circuit board can be created for a real test.

In future works advanced control methods, such as Fuzzy Logic, Model predictive control etc. can be experimented for a more robust, rapid and precise system control [10], [11].

Acknowledgement

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Load Characteristics of a Series Resonant DC-DC Converter with an Symmetrical Controlled Rectifier

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Abstract – **This paper considers a series resonant DC-DC converter operating above the resonant frequency. In order to control its output power, a symmetrical controlled rectifier is used, which allows bidirectional energy transfer. On the base of well-known analytical modelling of the resonant tank processes, a series for determination of the main converter quantities is proposed. As a result, the converter normalized load characteristics are built.**

Keywords – **Series Resonant DC-DC Converter, Controlled Rectifier, Operation above resonant frequency**

I. INTRODUCTION

The utilization of series-resonant DC-DC converters operation at frequencies higher than the resonant frequency provides a number of advantages [1÷3]: small size and low weight, low commutation losses, natural short-circuit safety. A significant disadvantage of this type of converters is the disruption in the conditions for natural turn-on switching of the controllable switches at zero voltage (ZVS) as a result of a decrease in the current flow through the resonant circuit. This event is observed at close to no-load operating modes, when the control is carried out by changing the operating frequency of the converter [4].

This disadvantage can be avoided by applying phase-shift control technique [1, 5]. Another resolution, which is gaining more and more popularity recently, is the utilization of a controlled rectifier [2, 3]. When this rectifier is symmetrical, another important advantage appears – the converter becomes bidirectional [1].

The existing analyses correspond mainly to series resonant DC-DC converters with asymmetrical rectifier [2, 3]. Usually, authors adhere only to the output and control characteristics, which is not enough for complete investigation and design. For this purpose, it is important the dependencies for the converter circuit elements stress to be obtained as well.

In [6], a time-domain analysis of bidirectional series resonant DC-DC converter operating above the resonant frequency is presented. Essentially, this is a resonant converter with symmetrical controlled rectifier. As a result from the analysis, modeling of the converter resonant tank circuit processes is accomplished and expressions for the model coefficients are obtained.

This paper presents sequel of the theoretical examinations achieved in [6]. Its purpose is load characteristics of a series resonant DC-DC converter with symmetrical controlled rectifier to be obtained for operation at constant frequency above the resonant one.

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II. PRINCIPLE OF THE CONVERTER OPERATION

Circuit of the examined converter is presented in Fig. 1. It consists of two identical bridge inverter stages, resonant tank circuit (L, C), matching transformer Tr, capacitive input and output filters (C_d and C_0). Fig. 1 also presents the snubber capacitors $C_1 \div C_8$ by which a zero voltage switching is obtained.

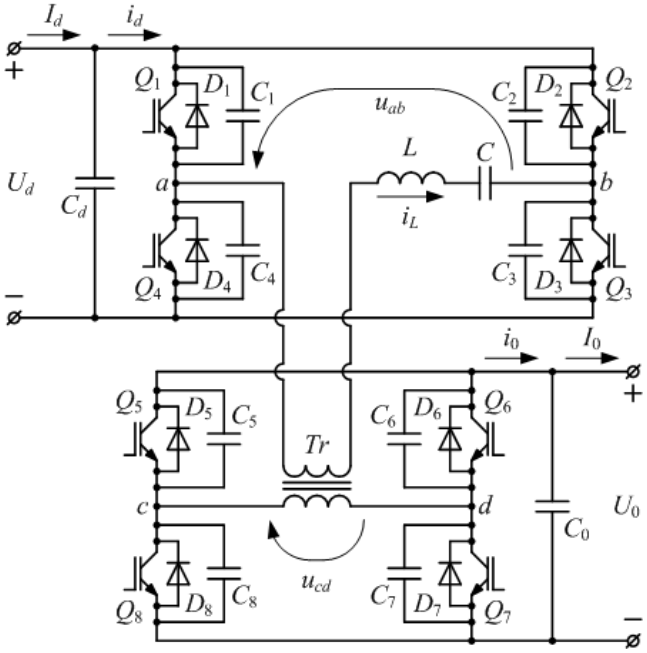

Fig. 1. Circuit of the Examined Resonant DC/DC Converter

The „input" stage (transistors $Q_1 \div Q_4$ with freewheeling diodes $D_1 \div D_4$) operate as an inverter and the „output" stage (transistors $Q_5 \div Q_8$ with freewheeling diodes $D_5 \div D_8$) – as a rectifier. A voltage U_d is applied to the DC terminals of the „inverter". Because the converter is bidirectional, a voltage source U_0 is applied to the DC terminals of the „rectifier".

Depending on the energy transfer direction, two operating modes are possible for the converter. The first of them is called ***DIRECT MODE***. In this mode, it is assumed that energy flows from the „inverter" to the „rectifier", i.e. from the source of voltage U_d to the one of voltage U_0. The second is ***REVERCE MODE***. In this mode, the energy flows from the „rectifier" to the „inverter" (from U_0 to U_d).

The waveforms shown in Fig. 2 illustrate the converter operation in ***DIRECT MODE***, and those in Fig. 3 – in ***REVERCE MODE***.

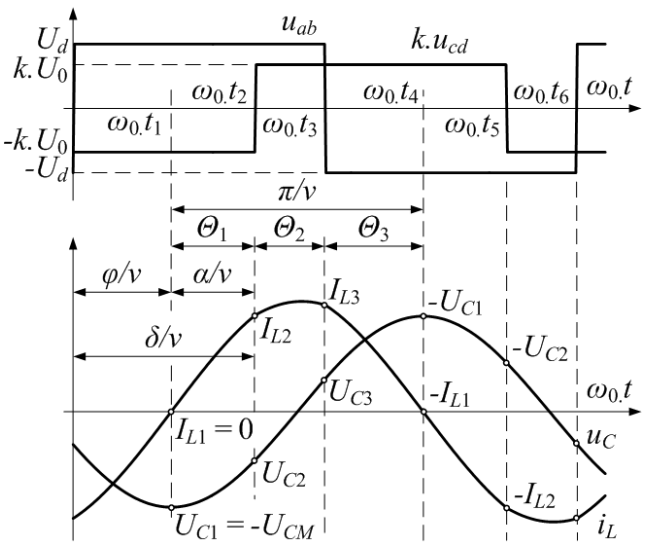

Fig. 2. Waveforms at ***DIRECT MODE***

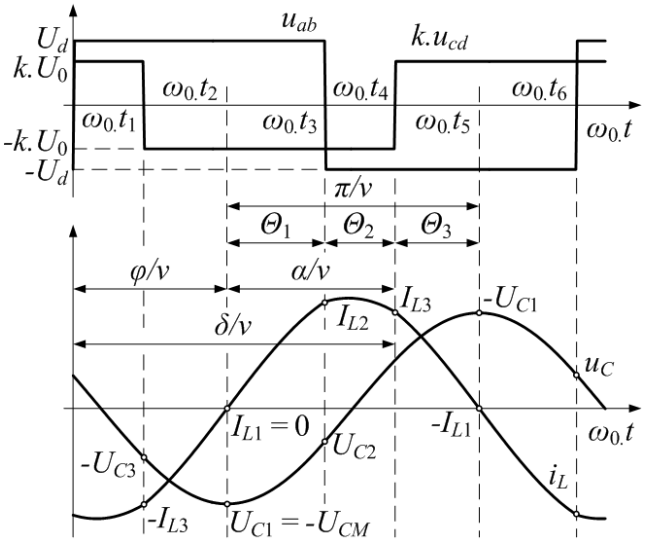

Fig. 3. Waveforms at ***REVERCE MODE***

Independently from the mode, the converter operates at constant frequency ω_S, which is higher than the resonant ω0. Therefore, the transistor pairs of the „inverter" (Q_1, Q_3 or Q_2, Q_4) operate at ZVS. They are controlled in such a way that the voltage u_{ab} has almost square-wave form and amplitude U_d. Along with this, the resonant current i_L falls behind the voltage u_{ab} at an angle φ. The transistors of the „rectifier" also operate at ZVS. Therefore, when the current i_L passes through zero, the corresponding pair (Q_5, Q_7 or Q_6, Q_8) begins conducting. This pair switches off after time, corresponding to an angle α. The voltage u_{cd}, which also has almost square-wave form and amplitude U_0, is shifted in time from u_{ab}. The output power can be controlled by the well-known phase-shifting technique, scilicet the variation of the angle α.

Angle φ corresponds to the conduction time of the „inverter" stage freewheeling diodes, and angle α – to the conduction time of the „rectifier" stage transistors. Obviously, when $\varphi < \pi/2$ and $\alpha < \pi/2$, energy is transferred in „forward" direction, and when $\varphi > \pi/2$ and $\alpha > \pi/2$ – in „reverse" direction. From Figs. 2 and 3, it can be observed that the following equation is valid: $\varphi + \alpha = \delta$. Therefore, when $\delta > \pi$, ***REVERCE MODE*** is observed, and when $\delta < \pi$ – ***DIRECT MODE***.

By means of the waveforms (figs. 2 and 3), the converter ZVS operating range can be determined. From one side, it is limited by the short circuit mode ($U'_0 = 0$). This is possible at $\varphi = \pi/2$. The other limitation for the ***DIRECT MODE*** is $\varphi = 0$, and for the ***REVERCE MODE*** – $\varphi = \pi$.

III. MODELING OF THE CONVERTER OPERATION

For the purposes of the analysis, the following assumptions are made: all the circuit elements are ideal, the transformer *Tr* has a transformation ratio *k*, the commutations are instantaneous, and the ripples of the voltages U_d and U_0 are negligible.

The waveforms (figs. 2 and 3) show that any of the half cycles can be divided into three intervals. For each of them, an equivalent DC voltage U_{EQ} is applied to the resonant tank circuit.

In accordance with the assumptions made, the resonant frequency, the characteristic impedance and the frequency detuning are:

$$\omega_0 = 1/\sqrt{LC}\ ; \quad \rho_0 = \sqrt{L/C}; \quad \nu = \omega_S / \omega_0 \qquad (1)$$

In order to obtain generalized results, all the quantities are normalized as follows: the voltages according to U_d; and the currents – according to U_d/ρ_0. For each of the mentioned intervals, the normalized values of the current i_L through the inductor *L* and the voltage u_C across the capacitor *C* are determined as follows:

$$\begin{aligned} i'_{L\,j}(\theta) &= I'_{L\,j}\cos\theta - \left(U'_{C\,j} - U'_{EQ\,j}\right)\sin\theta \\ u'_{C\,j}(\theta) &= I'_{L\,j}\sin\theta + \left(U'_{C\,j} - U'_{EQ_j}\right)\cos\theta + U'_{EQ\,j} \end{aligned} \qquad (2)$$

where *j* is the interval number; I'_{Lj} and U'_{Cj} are normalized values of the inductor current and the capacitor voltage at the beginning of the interval; $\theta = 0 \div \Theta_j$; Θ_j – angle of the interval for the resonant frequency ω0; U'_{EQj} – normalized value of the voltage applied to the resonant tank circuit during the interval.

From figs.2 and 3, it is observed that the value of i'_L at the end of given interval appears to be initial value for the following one. The same applies to the voltage u'_C. Therefore:

$$\begin{aligned} I'_{L\,j+1} &= I'_{L\,j}\cos\Theta_j - \left(U'_{C\,j} - U'_{EQ\,j}\right)\sin\Theta_j \\ U'_{C\,j+1} &= I'_{L\,j}\sin\Theta_j + \left(U'_{C\,j} - U'_{EQ_j}\right)\cos\Theta_j + U'_{EQ\,j} \end{aligned} \qquad (3)$$

TABLE 1. MODEL PARAMETERS

MODE	Parameter	Number of interval		
		1	2	3
DIRECT	Θ_j	$\frac{\alpha}{\nu}$	$\frac{\pi-\alpha-\varphi}{\nu}$	$\frac{\varphi}{\nu}$
	U'_{EQj}	$1+kU'_0$	$1-kU'_0$	$-1-kU'_0$
REVERCE	Θ_j	$\frac{\pi-\varphi}{\nu}$	$\frac{\alpha+\varphi-\pi}{\nu}$	$\frac{\pi-\alpha}{\nu}$
	U'_{EQj}	$1+kU'_0$	$-1+kU'_0$	$-1-kU'_0$

It is convenient the interval at which the initial values are $I'_{L1} = 0$ and $U'_{C1} = -U'_{CM}$ to be chosen as first. Then, for the second and the third intervals the initial values of the current (I'_{L2} and I'_{L3}) and the voltage (U'_{C2} and U'_{C3}) are

calculated on the base of eqs. (3). For one half cycle, the necessary for the purpose parameters Θ_j and U'_{EQj} are pointed out in Table I.

In [3], analytical expressions for determination of the normalized values of the voltages U'_0 and U'_{CM} are obtained. Like the initial values of the current i'_L and the voltage u'_C, they also represent function of the control parameter α and the angle φ:

$$U'_0 = \frac{1}{k}\frac{\sin\left(\frac{\pi-\varphi}{\nu}\right)-\sin\left(\frac{\varphi}{\nu}\right)}{\sin\left(\frac{\pi-\alpha}{\nu}\right)-\sin\left(\frac{\alpha}{\nu}\right)} \tag{4}$$

$$U'_{CM} = 2\frac{\sin\left(\frac{\varphi}{\nu}\right)+kU'_0\sin\left(\frac{\pi-\alpha}{\nu}\right)}{\sin\left(\frac{\pi}{\nu}\right)}-\left(1+kU'_0\right)$$

(5)

IV. LOAD CHARACTERISTICS OF THE CONVERTER

For determination of the converter capabilities and for the purposes of its design, it is necessary the average values of the currents through the particular elements to be determined. For convenience, the following substitution is used:

$$I'_{AV\,j} = \frac{\nu}{2\pi}\int_0^{\Theta_j} i'_{L\,j}(\theta)d\theta = \frac{\nu}{2\pi}\left[I'_{L\,j}\sin\Theta_j-\left(U'_{C\,j}-U'_{EQ\,j}\right)\left(1-\cos\Theta_j\right)\right] \tag{6}$$

The converter power devices conduct only within a single half cycle. The normalized average values of the currents through them for the ***DIRECT MODE*** are determined by expressions (7a) and (8a), and for the ***REVERCE MODE*** – by expressions (7b) and (8b):

$$I'_{QI} = I'_{AV1} + I'_{AV2};\quad I'_{DI} = I'_{AV3} \tag{7a}$$

$$I'_{QI} = I'_{AV1};\quad I'_{DI} = I'_{AV2} + I'_{AV3} \tag{7b}$$

$$I'_{QR} = kI'_{AV1};\quad I'_{DR} = k\left(I'_{AV2} + I'_{AV3}\right) \tag{8a}$$

$$I'_{QR} = k\left(I'_{AV1} + I'_{AV2}\right);\quad I'_{DR} = kI'_{AV3} \tag{8b}$$

where I'_{QI} and I'_{DI} are the normalized average values of the currents through the transistors and the freewheeling diodes of the „inverter"; I'_{QR} and I'_{DR} – through the transistors and the freewheeling diodes of the „rectifier".

Independently from the operating mode, the normalized average values of the „input" current I'_d and the „output" current I'_0 are determined as follows:

$$I'_d = 2\left(I'_{QI} - I'_{DI}\right) \tag{9}$$

$$I'_0 = 2\left(I'_{DR} - I'_{QR}\right) \tag{10}$$

By means of expressions (3) ÷ (10), for a fixed value of the control parameter α and with variation of the angle φ, values for the important quantities U'_0, U'_{CM}, I'_{QI}, I'_{DI}, I'_{QR}, I'_{DR} and I'_0 can be calculated. On the base of these values, different load characteristics of the converter are easily built. For the purposes of the analytical examination, such characteristics are obtained at frequency detuning ν=1,15 and transformation ratio k=1. The ZVS operating range boundaries are pointed out in dotted lines. These are the curves ***A*** (for $\varphi = 0$), ***B*** (for $\varphi = \pi$) and ***C*** (for $\varphi = \pi/2$). All the characteristics are built for values of the control parameter in the range $0 \le \alpha \le \pi$. These values are chosen in a way to be couples symmetrical to $\pi/2$.

Fig. 4 presents the normalized output characteristics of the converter. In this case, the boundary curve ***C*** falls with the abscise axis. The dependencies of the output voltage U'_0 from the output current I'_0 are shown with thick lines.

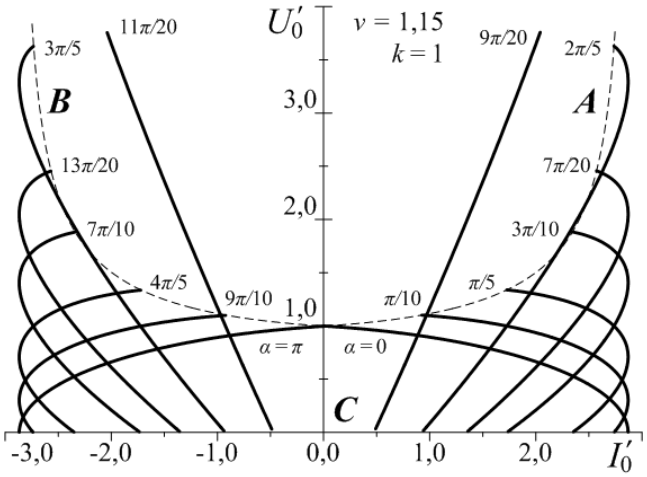

Fig. 4. Normalized output characteristics at $0 \le \alpha \le \pi$

The output characteristics show that the output voltage does not change its polarity and, independently from the energy transfer direction, can significantly exceed the input one. Moreover, the output current I'_0 cannot exceed the value at the output short circuit for $\alpha = 0$ or $\alpha = \pi$ respectively.

Fig.5 presents the normalized dependencies of the average value of the current I'_{QR} through the „rectifier" stage transistors from the output current I'_0. The conducted theoretical analyses show that the characteristics for the average value of the "rectifier" reverse diodes current I'_{DR} have the same form as those from Fig. 5 but are mirrored with respect to the ordinate. This results in the conclusion that obtaining higher output voltage leads to an increase in all the "rectifier" devices stress.

The dependencies of the average value of the current I'_{QI} through the „inverter" stage transistors from the output current I'_0 are shown in Fig. 6. Now the boundary ***B*** falls with the abscise axis and other boundary ***C*** is parallel to that. This is another case when the characteristics for the average value of the "inverter" reverse diodes current I'_{DI} have the same form as those from Fig. 6. However, they are mirrored with respect to the ordinate. This results in the conclusion that at ***DIRECT MODE*** the stress is mainly on the "inverter" transistors, and at ***REVERCE MODE*** – on its reverse diodes.

Fig.7 presents the normalized dependencies of the peak value of the capacitor voltage U'_{CM} from the output current I'_0. The boundary ***C*** is parallel to the abscissa. Like the output characteristics, these are also symmetrical with respect to the ordinate. Therefore, independently from the energy flow direction, the resonant tank elements are similarly loaded for on and the same energy quantity. Moreover, it can be observed that for a random characteristics the capacitor voltage is always greater than the output one.

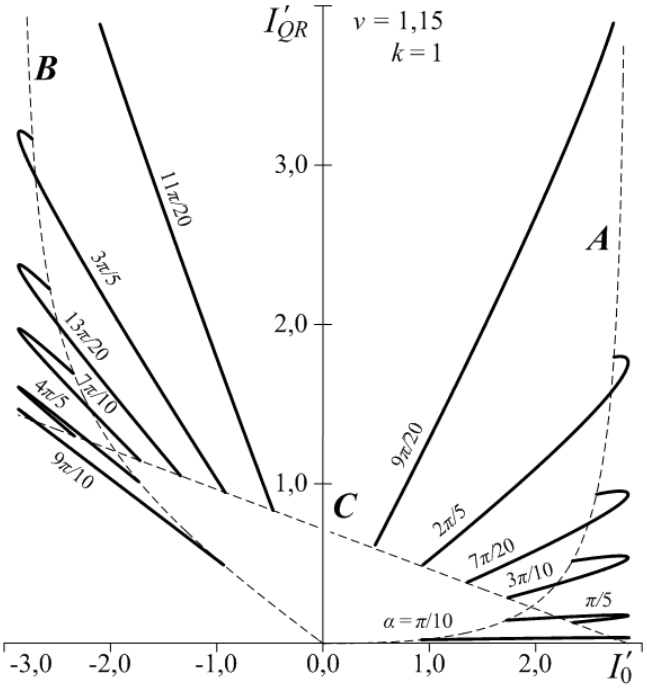

Fig. 5. Normalized average current through the „rectifier" transistors – I'_{QR}

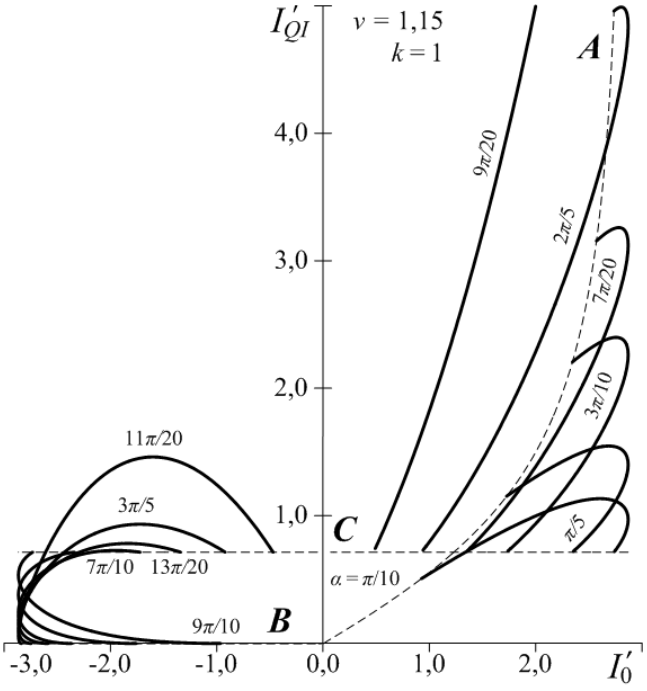

Fig. 6. Normalized average current through the „inverter" transistors – I'_{QI}

V. CONCLUSION

A series resonant DC-DC converter, operating above the resonant frequency, is examined. A symmetrical controlled rectifier is used. As a consequence, its normalized load characteristics are built. On the base of the obtained results, the following can be concluded:

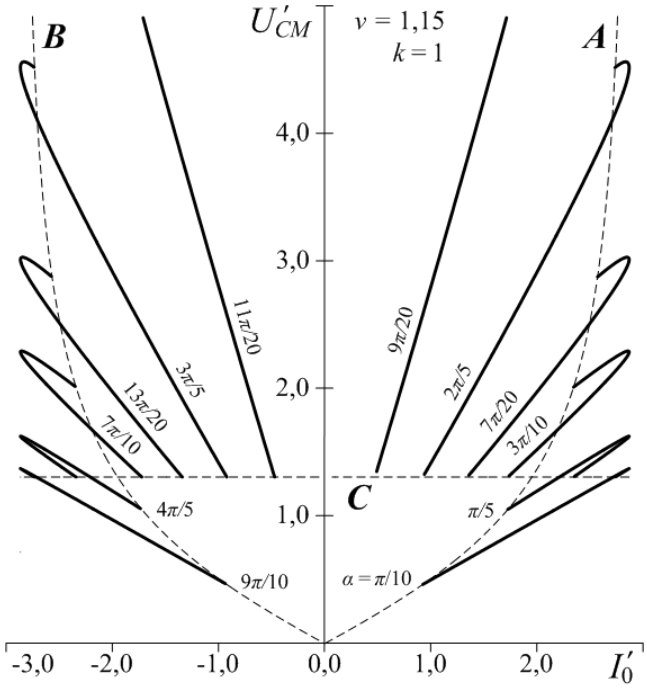

Fig. 7. Normalized resonant capacitor pick voltage – U'_{CM}

- The considered converter is bidirectional and it can operate without violation of the ZVS conditions in wide range of variation of the control parameter.
- The converter output voltage can exceed the input one independently from the energy transfer direction.
- The converter power devices stress grows up with the output voltage increase.

The obtained results can be used for further examination and design of such converters.

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Gate Driver Circuit for ZVS Mode

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Abstract – **This paper considers problems related with the switching losses in the power supply units, based on a high frequency inverters. Different ways to overcome some of the problems are discussed. A ZVS gate driver circuit for transistors in resonant DC/DC converter is proposed. The influence of the snubber capacitors value is studied. Experimental results to demonstrate the effectiveness of the driver are presented.**

Keywords – **ZVS, resonant DC/DC converter, switching losses**

I. Introduction

The requirements for gaining the efficiency of electrical devices have become considerably larger in the last decade. Fortunately, the contemporary semiconductors submit the possibility to work at significantly increased operating frequency, thereby reducing simultaneously volume, weight and the cost of power supply modules. This is of great importance especially when used for applications with relatively large power demands such as: electric vehicles fast chargers, electrostatic precipitators for wastewater treatment, arc welding and X-ray devices etc. In addition, problems with static losses in the conduction mode of the semiconductors are overcame because of their improved characteristics. However, the problem with switching losses remains unresolved. Of great importance is to pay special attention exactly on them, because these losses are proportional to the frequency. An appropriate topology and suitable control mode has to be chosen during the design of such power supplies.

Various types of inverter circuits are widespread. Disadvantage of these with so-called "hard commutation" is the lack of potential for considerable reduction of the switching losses. This sets limitation on their usage. In fact, more common are the converters with resonant tank. Their main advantage is that they provide the possibility for "soft commutation" of the main switches. The essence of the soft commutation is that the power switches could be turned on or off at zero voltage (Zero Voltage Switching - ZVS) or at zero current (Zero Current Switching - ZCS). In this way, some of the switching losses are reduced or almost completely eliminated.

There are plenty of publications, which analyze such kind of convertors and provide design guidelines [1, 2]. However, publications that have practical focus on the control system and formation of impulses to the switching elements in the inverter are not so common.

Most of the papers, which describe problems in the control of the power transistors in the inverter, give specific guidelines for loss reduction and offer solutions to some common problems [3, 4]. However, the proposed solutions are often quite complex like double stage turn-off control [5]. Therefore, in this article are presented directions for the realization of the driver circuit for inverter bridge which considerably eliminate the control problems, without unnecessary complication of the scheme.

II. Resonant DC/DC converter circuit

An LCC resonant DC/DC converter operating above resonant frequency is used for the present study. Variable switching frequency control method is used. The circuit is shown on Fig. 1. It consists of full-bridge inverter (transistors $Q_1 \div Q_4$ and reverse diodes $D_1 \div D_4$), resonant circuit (L_S, C_S and C_P), rectifier ($D_5 \div D_8$), output filter (C_0) and load resistance (R_0). The snubber capacitors ($C_1 \div C_4$), which provide the zero voltage switching (ZVS), are connected in parallel with the transistors.

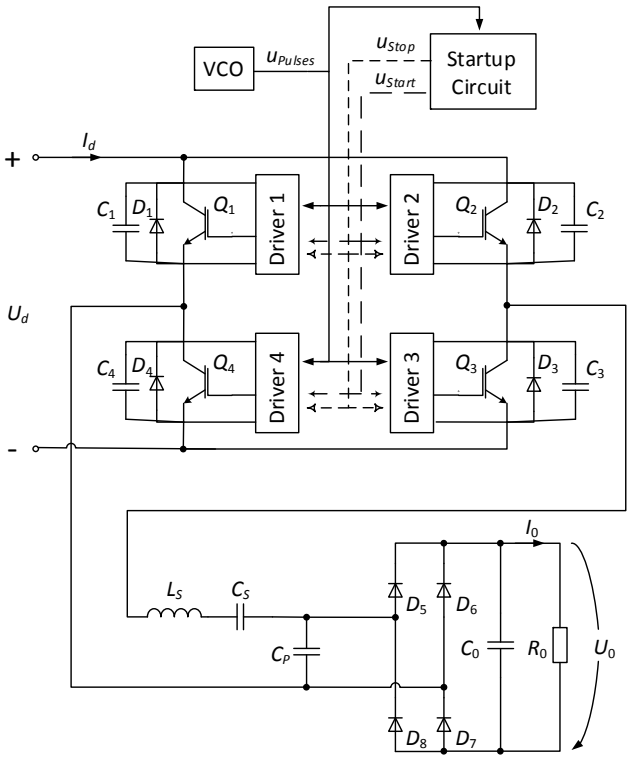

Fig. 1. LCC resonant DC/DC converter

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Each transistor is controlled by an individual driver circuit, which provides its spontaneous turn-on at zero voltage and forced turn-off. A voltage-controlled oscillator (VCO) supplies bipolar square-wave pulses with an appropriate frequency. The Startup Circuit ensures correct start and stop of the inverter, synchronized with the switching pulses.

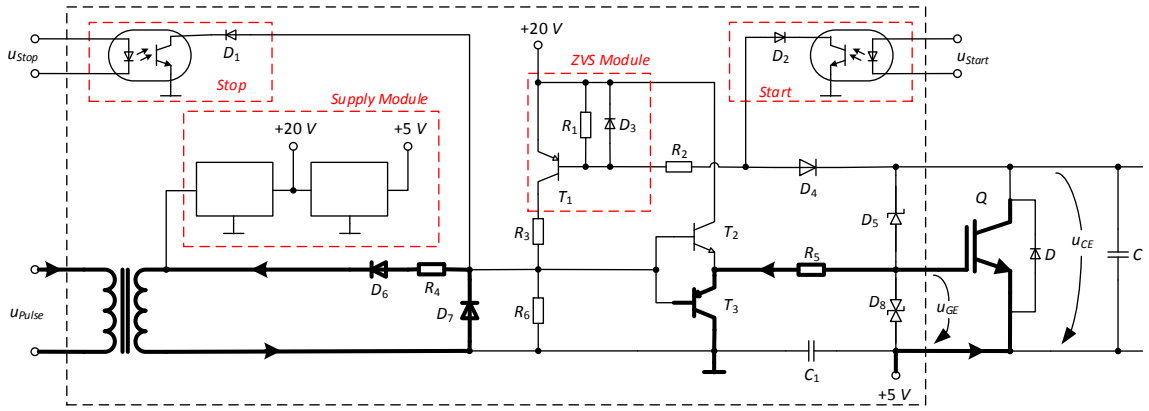
III. DRIVER CIRCUIT

All the driver modules must be galvanic separated. For this purpose, the driver circuits receive the impulses trough pulse transformers, which serve also to amplify the voltage u_{pulse} from ±12 *V* to ±30 *V*. The Start and Stop control signals are fed by high-speed optocouplers. Fig. 2 shows a simplified diagram of the driver circuit for one of the transistors in the inverter in different operating modes.

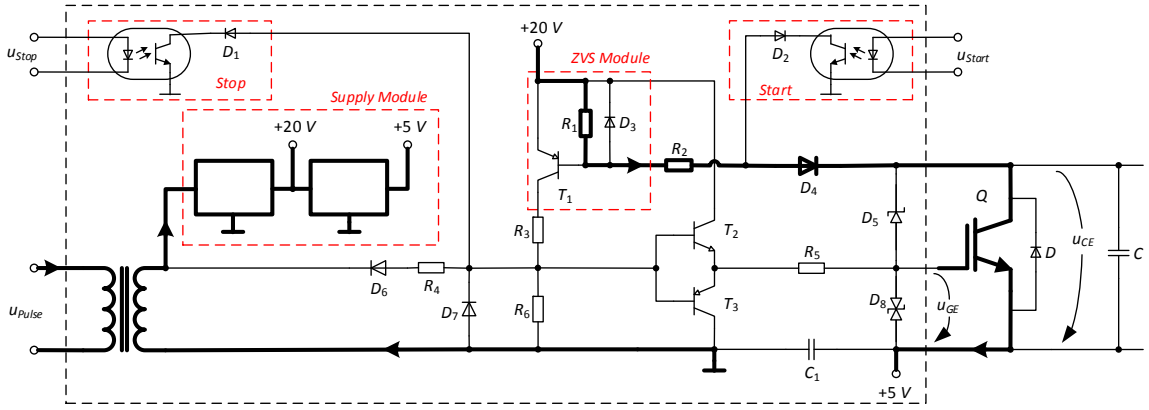
A. ZVS turn-on commutation

If transistors' turn-on is controlled only by the impulses from VCO, ZVS cannot be guaranteed. Appropriate fixed "dead time" between the turn-off of one couple and the turn-on of the other can be provided. This solution is suitable for fixed loads. Voltage u_{CE} has to be observed and turn-on impulse to be applied only when reaches zero.

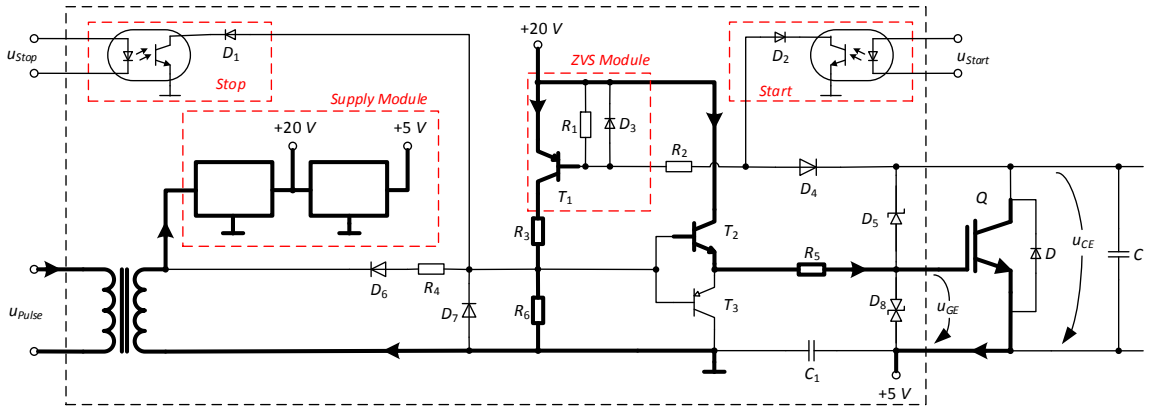
There are different design solutions, which determine the system behavior if this voltage doesn't reach zero. One possible solution is dead time to be defined, for the case in which the requirement $u_{CE} = 0$ *V* is not fulfilled. After this



a) Turn-off



b) ZVS Detection



c) Turn-on

Fig. 2. ZVS gate driver circuit operating modes

period a forced turn-on impulse is applied [6]. In this implementation, some problems in the operation of the inverter could remain hidden. In the circuit we propose, if turn-on at zero voltage could not be achieved, inverter switches off. This is realized by the ZVS Module, with elements R_1, D_3, T_1. It provides turn-on synchronization of transistors T_2 and T_3 in the moment $u_{CE} = 0$ *V*.

B. Reducing switching losses on turn-off commutation

The turn-off commutation is not lossless. However, the use of snubber capacitors significantly reduces them, because when the device is turned-off most of the current flows through the capacitor.

In order to reduce even more these losses the turn-off must be done at negative gate voltage. In this way, the effect of "Miller" capacity between the collector and gate is reduced. The resulting voltage u_{GE} can be sufficient to turn the IGBT on again with possible shoot-through and damage [7]. By selecting appropriate value of resistor R_5 both the length and the level of the Miller's plateau can be adjusted.

C. Driver power supply

One of the common options to form the supply voltage of the driver circuit is by external sources. Disadvantage is the need of additional components, providing galvanic isolation between the particular gate drivers. In this paper, the variant in which the formation of the supply voltages is from the control impulses is proposed. One advantage in this case is when the impulses are absent driver voltages drop out and transistors are immediately turned-off. This provides additional protection in emergency situations.

The formation of the circuit supply is on two levels. First, the pulses are rectified and stabilized at 20 *V*, and 5 *V* formed from them. In this way the IGBT transistor turns-on with $u_{GE} = 15$ *V* and turns-off with $u_{GE} = -5$ *V*.

D. Start/Stop realization

The chosen method of supply voltage formation requires the switching process to be independent from the control impulse submission. The synchronization of the turn-on process of the inverter is provided from the Startup Circuit as shown with the waveforms on Fig. 3.

When the device is powered, VCO submits control impulses to the driver circuit, and driver's supply voltages are formed. The inverter itself does not start yet. The Startup Circuit, via u_{Stop}, feeds active level to the optocoupler of Stop Module and fixes T_2-T_3 bases to ground. Hence, only T_3 is turned-on and $u_{GE} = -5$ *V*.

When startup command is applied *uStop* = 0 and an impulse with quarter of the switching period (T_S/4) is fed to the Start Module. This simulates $u_{CE} = 0$ *V* and turns-on T_1 and IGBT receives $u_{GE} = 15$ *V*. through T_2-T_3. This happens simultaneously for both transistors in one diagonal.

When u_{Pulse} becomes negative, T_2 turns-off and T_3 turns-on by diode D_7, which implements forced turn-off commutation of the IGBT transistor, as shown on Fig. 2a. This relates to the submission of positive half period of u_{Pulse} to the transistors' drivers in the other diagonal of the inverter and creates conditions to open the relevant IGBT transistors. It is not enough, because their voltage u_{CE} has to reach zero and is realized with the ZVS Module circuit, as shown on Fig. 2b. Then T_1 in the corresponding driver module opens, which results in closing of the circuit in a manner shown in Fig. 2c. In this way, turn-on commutation is achieved at a voltage close to zero. In practice, the minimum value is limited to a few volts.

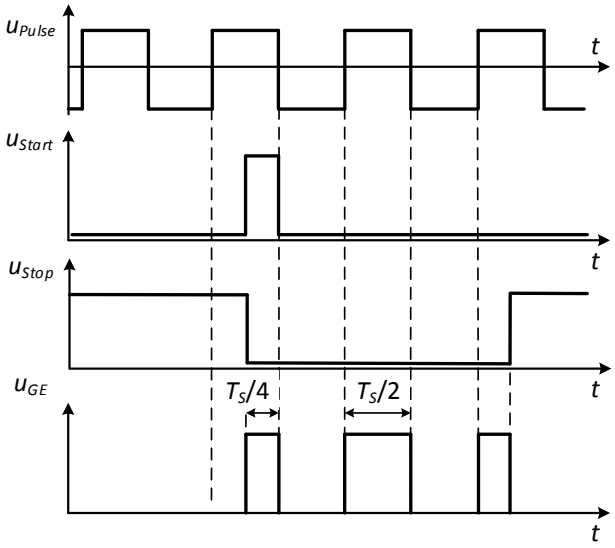


Fig. 3. Waveforms of starting and stopping of the inverter

IV. EXPERIMENTAL RESULTS

An experimental prototype of the proposed ZVS gate driver circuit is made. It is used for controlling the inverter of LCC resonant DC/DC converter. IGBT modules SKM100GB125DN by Semikron are used for power semiconductors. The values of resonant tank elements are: L_S = 416 μH, C_S = 35 *nF*, C_P = 56 *nF*. This results to resonant frequency of 41,7 *kHz*. The switching frequency of the inverter is 49,3 *kHz*.

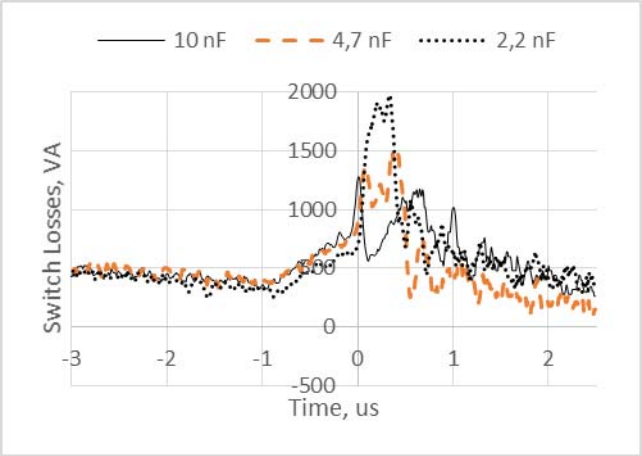


Fig. 4. Switch losses (u_{CE} x i_Q) with different snubber capacitors

Comparison between turn-off losses with different snubber capacitors is presented on Fig. 4. Increase of it narrows the spontaneous commutation region and the snubbers cannot recharge. This, in a driver circuit with fixed dead time, will lead to non-ZVS and hence higher losses. In this situation the proposed circuit, stops operation

and goes to emergency regime without negative consequences. The chosen snubbers' value is 10 *nF*.

Fig. 5 shows ZVS turn-on commutation of IGBT transistor. The turn-on impulse u_{GE} starts only when u_{CE} is close to zero, as seen from the waveform.

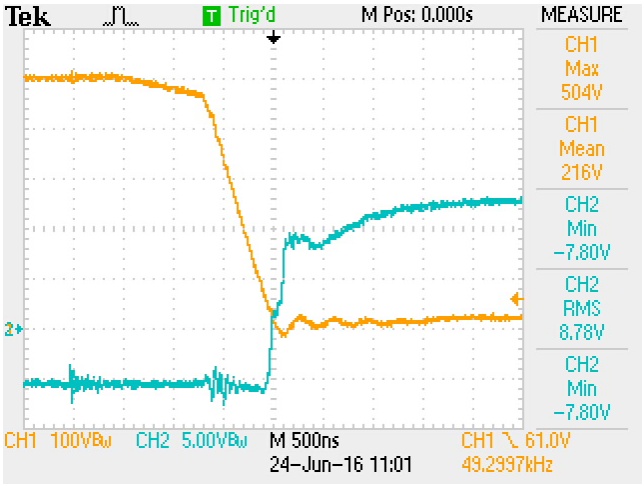


Fig. 5. ZVS turn-on of IGBT (CH1: u_{CE}; CH2: u_{GE})

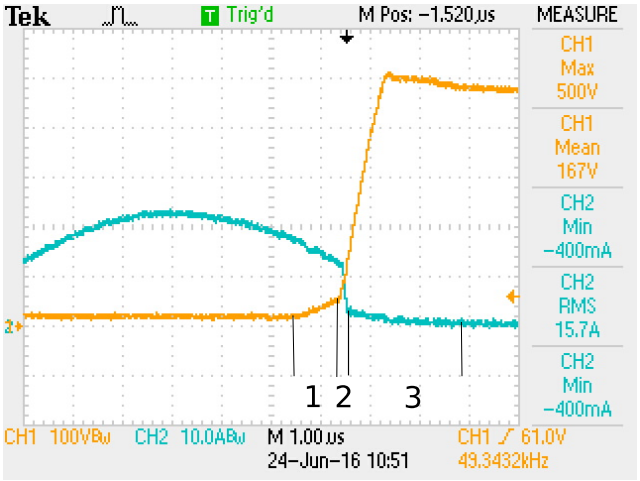


Fig. 6. Loss reducing during turn-off (CH1: u_{CE}; CH2: i_Q)

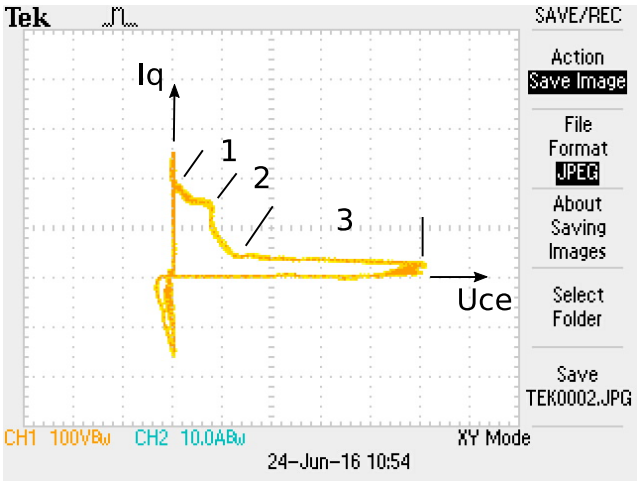


Fig. 7. Operating trajectory of IGBT (CH1: u_{CE}; CH2: i_Q)

The turn-off commutation could be divided on three intervals, as shown on Fig. 6. The first one is when u_{CE} increases but the i_Q follows its resonant form. This interval duration and also the losses are determined by the Miller's plateau size. During the second transistor's current sharply decrease when IGBT begins to turn-off, because most of i_Q flows through the snubber. The third interval is described with so-called "current tail", which is responsible for major losses and is dependent to the device technology. Its effects cannot be reduced by means of the driving circuit.

Fig. 7 describes the operating trajectory of the IGBT. The current and the voltage, during the turn-on, are following the axes without encloses significant area. The mentioned intervals of turning-off are also indicated.

V. Conclusion

In this paper, a driver circuit for inverter's power transistors of resonant DC/DC converter is proposed. The converter is operating above the resonant frequency, so a ZVS commutation is achieved. Problems related with the reduction of the switching losses and different ways to overcoming are discussed. A simplified electrical circuit with denoted operating modes is presented. The driver's supply voltages are formed from the control signal without any additional power sources. This solution guaranteed the inverter switching off during absence of control impulses. Negative gate-emitter voltage is used to turn-off the power switches. This way the losses during this commutation are reduced. Rapid optocouplers are used for the simultaneously turning-off of all the transistors in order to protect them in emergency situations.

Experimental results with a working prototype are presented. The switching losses with different snubber capacitors value are shown, as well as the ZVS turn-on and the turn-off with reduced losses. The operating trajectory of the transistors is presented and the different turn-off intervals are explained.

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DSP Based Induction Motor Drive with Parallel Quasi-Resonant Converter

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Abstract – **A DSP based induction motor drive with parallel quasi-resonant converter is developed. The three-phase inverter bridge and resonant circuit switches are used for powering an induction motor drive. The „TMS320C2000™ Experimenter Kit" board built around the TMS320F2808 DSP controller is used to control the resonant circuit, inverter and motor. This platform is compatible with Simulink®, and includes six dual pulse PWM channels, 16 ADCs, and a speed encoder input. The control program is implemented in Simulink® and the switching signals are transferred to the inverter through an interface board. The experimental results show that a smaller switching loss and higher conversion efficiency are obtained by the proposed system.**

Keywords – **Induction motor drive, Quasi-resonant converter**

I. Introduction

Inverters have many applications in power electronic devices. The performance of a pulse-width modulated inverter-fed system can be much improved by increasing the switching frequency. In hard switching inverters, a higher switching frequency leads to increased switching losses which consequently increases the size of the snubber circuits [1, 2]. This will suffer by giving large switching stresses of the power devices. In addition, electromagnetic interference increases and efficiency decreases. To overcome these problems, the application of soft switching techniques is essential [1-5].

The resonant DC-link inverter is the most commonly used one for induction motor drives, owing to its simplicity, but it possesses the disadvantage of having a high resonant link voltage, which is equal to or greater than twice the supply voltage [1].

Quasi-resonant (QR) inverters offer several advantages compared with resonant DC-link inverters with regard to resonant link design and control, device rating requirements and use of pulse width modulation (PWM) [6]. The QR inverter schemes generate zero-voltage instants in the DC link at controllable instants that can be synchronised with any PWM transition command, thus ensuring a zero-voltage switching condition of inverter devices. As a result, these inverters can be operated at high switching frequencies with high efficiency [6].

The passively clamped QR inverter is reported in [7]. This topology satisfying most of the essential requirements, such as low clamp factor, simple resonance control, guaranteed zero-link voltage condition, PWM capability, use of only one auxiliary switch and recycling of resonant energy. The only drawback of this scheme was the high reverse voltage requirement of the clamp diode. This problem can be solved by use of a separate, low-voltage DC source [5, 6]. Another possible solution could be to use a simple R-C parallel circuit to maintain low voltage [6].

One of the main QR inverter research goals is to achieve soft switching conditions with a minimum number of auxiliary circuit elements [2]. Reducing the number of auxiliary switches simplifies the control circuit and decreases the inverter cost.

The object of this work is to develop and investigate a DSP based induction motor drive with parallel quasi-resonant converter. It is necessary to investigate a efficiency and performance of proposed drive system.

II. Structure and Function of Motor Drive System

The circuit diagram of the induction motor drive with parallel quasi-resonant converter is illustrated in Fig. 1.

Usually the small power variable speed drives are powered from single phase AC mains u_s through a diode bridge rectifier with smoothening DC capacitor and a voltage source inverter. The diode bridge rectifies the AC input voltage and the *C*-filters smoothes out the resulting voltage to make it an almost pure DC waveform.

The converter topology is similar to the classic converter, plus an auxiliary circuit consists of switch S_{a2}, antiparallel diode D_{a2} and the coupled inductors L_{r1} and L_{r2}., the dc-link switch is S_{a1}, antiparallel diode D_{a1} and the dc-link resonant capacitor is C_r.

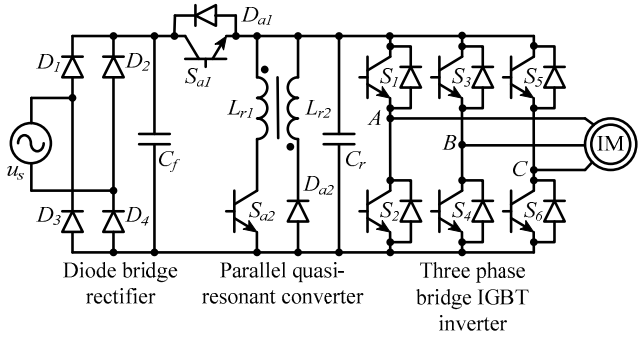

Fig. 1. Parallel Quasi-Resonant Converter

The induction machine is fed by a three phase bridge IGBT inverter ($S_1 \div S_6$) connected to a rectifier. The „TMS320C2000™ Experimenter Kit" board work as the control and estimation platform. This board is built around the TMS320F2808 DSP. This platform is compatible with

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Simulink®, and includes six dual pulse PWM channels (12 channels total), 16 ADCs, and a speed encoder input. The processor is a 32-bit DSP with fixed-point arithmetic; thus, discrete and fixed-point math blocks of Simulink® can be used in the block diagrams.

To achieve the desired feedbacks, the control and estimation algorithms use information from sensors. Current and voltage measurements are used in the control and estimation process (Fig. 2).

The Hall Effect based current transducer LTS 15-NP was used in the current measurement circuits. The accuracy of the current transducer used in the circuit is better than ±0.2 % at 25 °C and has a bandwidth of 100 kHz [8]. This transducer requires a unipolar power supply of +5V, and can measure DC and AC currents. The reference point of the transducer with zero primary current is 2.5 V, which is equal to the half of the supply rail voltage. The maximum gain of $(0.625/I_{PN})$V/A (I_{PN}=15A) can be achieved and the output voltage of the current transducer can be given by $V_{out}=(0.625/I_{PN})I_P+2.5$.

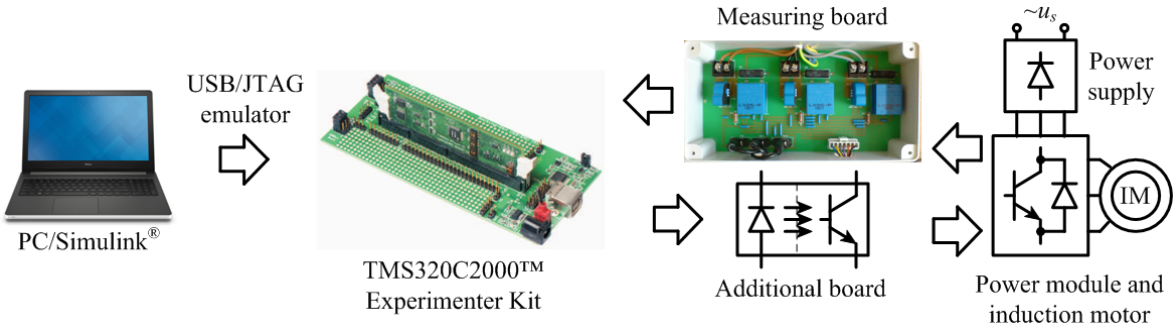

Fig. 2. Block-diagram of the developed system

The Hall Effect based voltage transducer LV 25-P was used in the voltage measurement circuits. The accuracy of the voltage transducer used in the circuit is better than ±0.9 % at 25 °C [9]. This transducer requires a ±15V power supply, and can measure DC, AC and pulsed voltage. The maximum gain of can be achieved and the output voltage of the voltage transducer can be given by $V_{out}=0.01V_P$ (V_{PN}=400V).

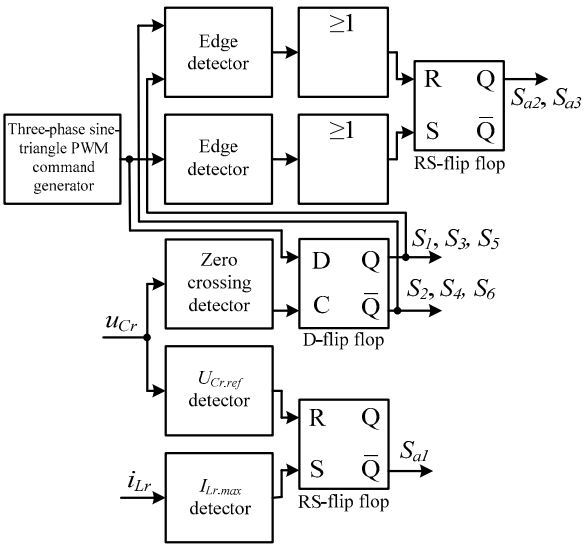

Fig. 3. Block-diagram of the control algorithm

The „TMS320C2000™ Experimenter Kit" requires all ADC inputs to be between 0 and 3 V. The ADC output is a 12-bit fixed-point integer with full scale of 4095 at an actual current of ±12 A and voltage ±400V.

To achieve the best decimal accuracy, fixed-point math is used on the DSP. The "Target for TI C2000" Simulink library has the "C28x IQmath" module in which basic accurate math operations can be found. The Q value of an IQ number is the bit before which the decimal point is placed.

Since the F2808 DSP is a 32-bit fixed point processor the data type mainly used in the Simulink® model below is fixdt(1,32,19) in Matlab nomenclature, which corresponds to a fixed point data type. The range of the data type specified above is -4096 to 4095.9999980926514 and the precision is $1.9073486328125\times10^{-6}$. This range should be more than enough for this implementation where the highest possible number is 4095 and comes from the 12-bit analog to digital converter (ADC). The precision should also be more than enough since it is also limited by the 12-bit ADC.

The DSP clock frequency is 100MHz but the control and estimation run at sampling frequencies 1,5KHz.

A three-phase sine-triangle PWM command generator was implemented to control the six inverter switches. The frequency of the carrier wave is maintained at 1,5 kHz. Inverter control is implemented based on the link operation requirements, whenever a switching signal is generate, the auxiliary circuit must first be turned on to initiate a resonant transient. The inverter switches, when the link voltage reaches zero. A block diagram for a control scheme is shown in fig. 3. The edge detector locates the desired state change before the switching command is passed to the inverter switches. The detected edges are used as an input of a RS-flip flop to turn on of the auxiliary circuit. The auxiliary switch turns off, when the state of the inverter switches was changed. When i_{L1} reaches $I_{Lr.max}$, the pulse is used as an input of a RS-flip flop to turn off of the link circuit. The link switch turns on, when the C_r reaches $U_{Cr.ref}$.

To synchronize the change in the conducting state of the inverter devices with the zero link voltage instant, D-type flip-flop is used (fig. 3). The switching signals generated by PWM generator drive the D-input pins of the flip-flop,

and the output pins drive the corresponding top (S_1, S_3, S_5) and bottom (S_2, S_4, S_6) switches of the PWM inverter. When the link voltage reaches zero, the zero-voltage detector outputs a signal that is used to clock the D-type flip-flop. Thus the conducting state is changed only at zero-voltage condition.

The presented in fig. 3 control schemes was developed in Matlab/Simulink®. The program is compiled in "TMS320C2000™ Experimenter Kit" via USB/JTAG emulator built into the board "TMS320C2000™ Experimenter Kit". The additional board (Fig. 2) is used for galvanic isolation of the control board and power supply.

III. Received Results

The developed DSP based induction motor drive with parallel quasi-resonant converter is experimental investigate with induction motor type 4AO-80B-4D having ratings as 0,75 kW, 380 V, 50 Hz which is connected to drive the load (DC generator). The technical data of the electric motor are given in Appendix.

The design of the proposed inverter involves the selection of parameters C_r, L_{r1}, L_{r2} to satisfy the desired link waveform specifications such as *du/dt, di/dt* and peak currents [6]. The design expressions are derived from the differential equations of each mode of the resonant cycle [1-7]. A set of parameters has been chosen as L_{r1}=220μH, L_{r2}=880μH, C_r=100nF.

Studies were performed in U_{DC}=140V. Current probe is used for the measurement of the currents with a coefficient of 10mV/A.

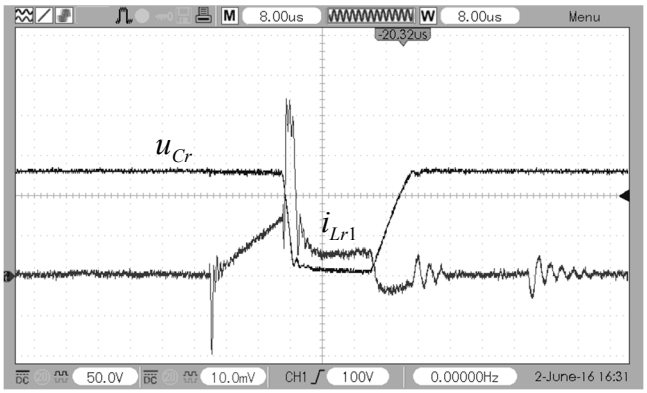

Fig. 4. Dependencies u_{Cr}, i_{Lr1}=*f(t)*

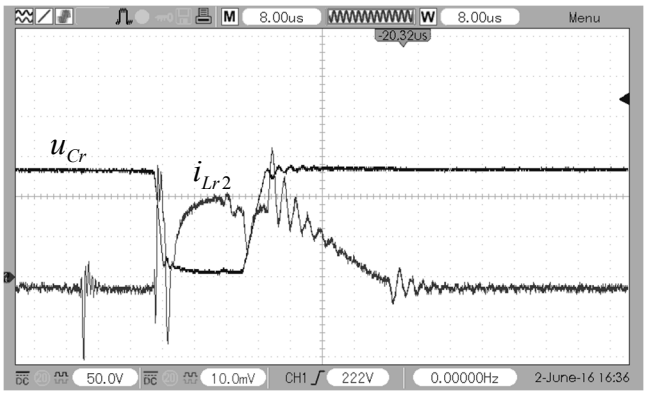

Fig. 5. Dependencies u_{Cr}, i_{Lr2}=*f(t)*

The voltage and currents of the resonant inductor L_{r1} and capacitor C_r are illustrated in Fig. 4 and resonant inductor L_{r2} and capacitor C_r are illustrated in Fig. 5.

From the basic waveforms shown, it is seen that some limitations still exist. The control circuit must drive the auxiliary switch at the proper time. It can be observed, that the state of the inverter switches can be changed Δt_S after turning S_{a2} on. The duration of the energy storage interval is Δt_{ES}; the duration of the falling for the link voltage is Δt_F; the duration of the zero voltage intervals is Δt_{ZV}; the duration of the rising for the link voltage is Δt_R; the duration of one switching cycle is ΔT. The delay values were summarized in Table 1.

Table 1. The Delay Values for the Parallel Quasi-Resonant Converter

Parameter	*Duration, μs*
Δt_S	36,27
Δt_{ES}	17,6
Δt_F	3,2
Δt_{ZV}	19,2
Δt_R	10,13
ΔT	50,13

The duration of the zero voltage intervals Δt_{ZV} is enough to switch the power switches at zero voltage.

The voltage and current waveforms of the dc-link switch is S_{a1} and antiparallel diode D_{a1} are shown in Fig. 6. The voltage and current waveforms of the auxiliary circuit consists of switch S_{a2}, antiparallel diode D_{a2} are shown in Fig. 7 and Fig. 8.

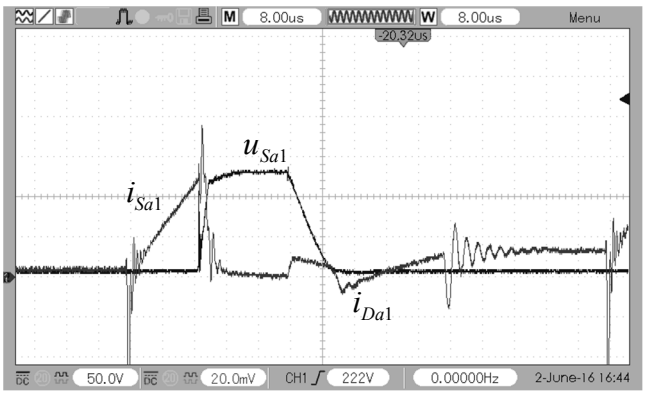

Fig. 6. Dependencies u_{Sa1}, i_{Sa1}, i_{Da1}=*f(t)*

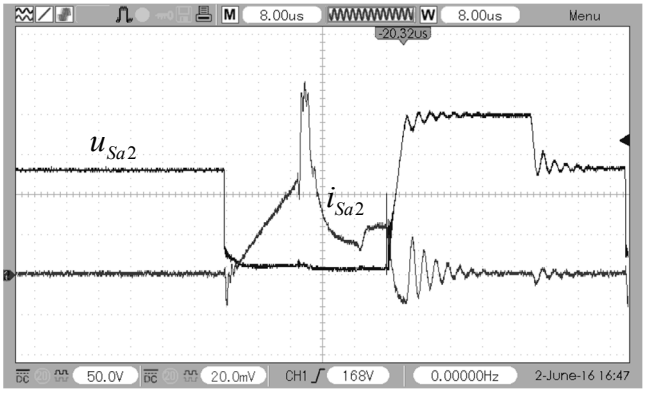

Fig. 7. Dependencies u_{Sa2}, i_{Sa2}=*f(t)*

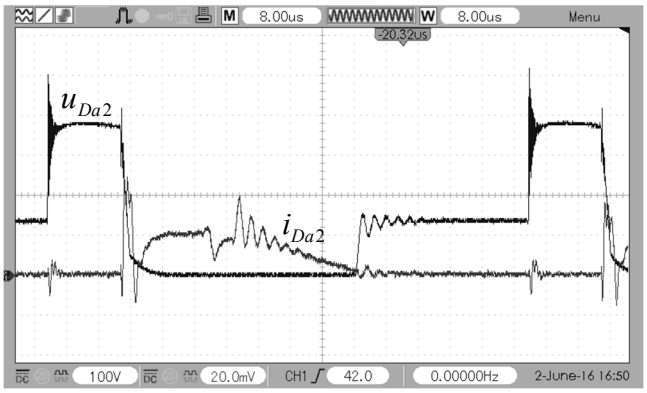

Fig. 8. Dependencies u_{Da2}, $i_{Da2}=f(t)$

The voltage and current waveforms of the inverter main switch S_1 are shown in Fig. 9.

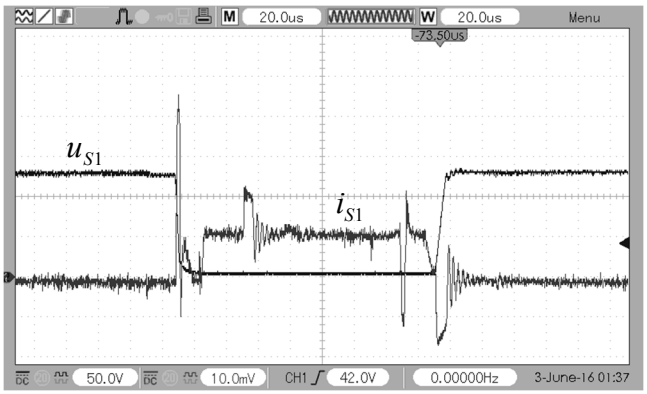

Fig. 9. Dependencies u_{S1}, $i_{S1}=f(t)$

From fig. 6 – fig. 9 is seen that the current through transistors S_{a1}, S_{a2}, S_1 and diode D_{a2} begins to flow in the reset voltage on it. This led to a significant reduction in switching losses.

Amplitude values of the current and voltages of the resonant elements, power switches and diodes are summarized in Table 2.

TABLE 2. AMPLITUDE VALUES OF THE CURRENT AND VOLTAGES

Element	*Voltage, V*	*Current, A*
L_{r1}	-	4,33
L_{r2}	-	3,48
C_r	135,19	-
S_{a1}	130,68	3,79
D_{a1}	130,68	0,42
S_{a2}	201,13	9,55
D_{a2}	377,44	4,89
S_1	134,47	4,70
S_2	138,26	4,58

The greatest value of the current is obtained through the switch S_{a2}. The current i_{Sa2} is 8,135 times greater than the current flowing to the inverter during the switching period I_0 (I_0=1,174A). The greatest value of the voltage is obtained through the diode D_{a2}. The voltage u_{Da2} is 2,696 times greater than the DC link voltage U_{DC} (U_{DC}=140V).

Fig. 10 shows the induction motor line-to-line voltage u_{AB} and phase current i_A.

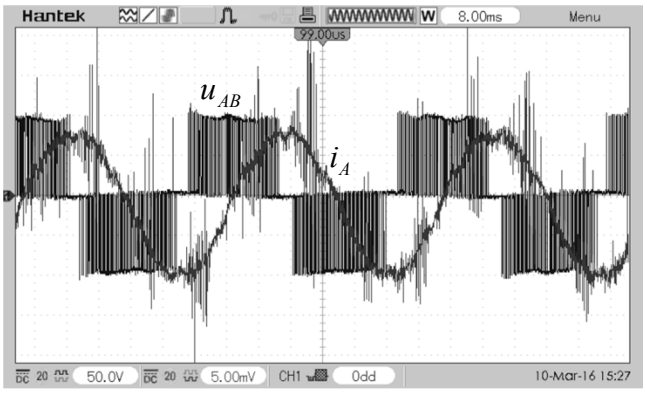

Fig. 10. Dependencies u_{AB}, $i_A=f(t)$

From the figure it is seen that phase current have sinusoidal form with minimal distortion.

IV. CONCLUSION

A DSP based induction motor drive with parallel quasi-resonant converter is developed. The three-phase inverter bridge and resonant circuit switches are used for powering an induction motor drive. The „TMS320C2000™ Experimenter Kit" board built around the TMS320F2808 DSP controller is used to control the resonant circuit, inverter and motor. This platform is compatible with Simulink®, and includes six dual pulse PWM channels, 16 ADCs, and a speed encoder input. The control program is implemented in Simulink® and the switching signals are transferred to the inverter through an interface board. The experimental results show that a smaller switching loss and higher conversion efficiency are obtained by the proposed system.

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APPENDIX

Induction motor type 4AO-80B-4D
P_N=0,75kW; U_N=380V; I_N=2,1A; n_N=1400min^{-1}; η_N=71%; $cos\varphi_N$=0,70; J_m=0,00154kgm^2.

Comparative Study of Winding Arrangements for Power Electronic Transformers

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Abstract – **The paper presents comparative study of winding arrangements for power electronic transformers. The designs are based on an improved design algorithm consisting of 15 steps. Four different winding arrangements are considered for a transformer design, 1200W, 25kHz. The approaches applied are interleaved windings, fully wound winding layers and using Litz wire. The material used is ferrite (N87). A set of operating and construction parameters is defined to compare the obtained designs. Design conclusions and recommendations are derived based on the comparison of the studied winding arrangements of transformers for power electronics.**

Keywords – **Power electronic transformers, Winding arrangements, Power losses**

I. Introduction

The current improvement of power switches provides the opportunities to design power electronics devices with better operating and size parameters. Magnetic components as parts of the power equipment are among the most decisive components when targeting volume, losses and price of a device. High frequency losses in windings are one of the main constraints for the designs based on increasing the operating frequency. Different winding arrangements and using different wires provide approaches to deal with eddy currents in windings. Discussions on winding arrangements and effects of the design, including interleaving and half-layer may be found in [1], [2], [3]. High frequency design, including optimization of the winding layout is presented in [4].

The paper compares four different winding arrangements (cases) for a transformer, 1200W, 25kHz:

- The first arrangement (Case 1) is based on using solid round wires with diameters, equal to the next available sizes in respect to calculated by the methodology;
- The second arrangement (Case 2) is based on solid wires, but both primary and secondary winding diameters are increased as much as the whole winding width of the coil former to be filled with the respective winding layers;
- The third arrangement (Case 3) considers a solid wire for the primary with a diameter chosen to fill the winding width and a Litz wire for the secondary winding;
- In the fourth arrangement (Case 4) the primary and secondary windings are interleaved. The suggested interleaving has an arrangement PSP, i.e. the secondary winding is located between two primary winding layers.

II. Design Approach including Eddy Current Losses in Windings

The called Non-Saturated Thermally Limited Design Approach, 15 steps [5], is used to calculate the four different transformers according to their winding arrangements. Firstly a proper core size is derived according to which the heat transfer capability and respective allowable overall power losses of the component are obtained. Afterwards, for best heat transfer, the total losses are equally divided and subsequently assigned to the core and the windings. Therefore, the losses in the core are predetermined. Then, having their values, we determine what is the peak induction using the P_{loss} vs $B_{ac,peak}$ graphs provided by the manufacturer. Once having the Bac, peak value we proceed with calculating of the necessary turns for the primary and secondary winding followed by choosing the appropriate conductors' diameters and winding arrangements. Here is the biggest challenge of the design.

Four different winding arrangements are calculated for the considered transformer: $V_{prim,rms} = 300\ V$, $V_{sec,rms} = 100\ V$, $I_{sec.rms} = 12\ A$, $f_{op} = 25kHz$. Calculating eddy current losses in wires is essential in the estimation and study of these different winding arrangements. Well known approach using area-product method presented by McLyman [4] does not consider sufficiently eddy current losses in windings. Eddy current losses, including skin and proximity effects in transformers are thoroughly discussed in [6], [7], [8]. These methods are based to some extent to Dowell's interpretation and results [9]. A total loss comparison in the designs of high frequency transformers, including losses in windings is presented in [10], [11].

To calculate the eddy current losses in wires a novel approach is developed in [12], suitable for fast and practical engineering designs. The approach includes a global loss factor k_c, which represents the ratio between the eddy current losses compared to the losses in the ohmic resistance of a transformer:

$$P_{eddy} = (R_0\ I_{ac}^2)\ k_c \quad (1)$$

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where I_{ac} is the AC current component, R_0 is the ohmic resistance of the winding.

The loss factor k_c depends on the operating frequency f_{op}, the wire diameter d_p and the distance between the conductors, presented by the parameter η, and the distance between the layers presented by the parameter λ.

The exact calculation of k_c includes a few parameters, thus the design procedure is fastened by derived set of graphs presenting dependence of k_c on an aggregate coefficient K_{tf}:

$$k_c \approx m_E^2 \cdot K_{tf} \tag{2}$$

where m_E is an equivalent layer [11].

Fig. 1. presents a typical dependence of K_{tf}.

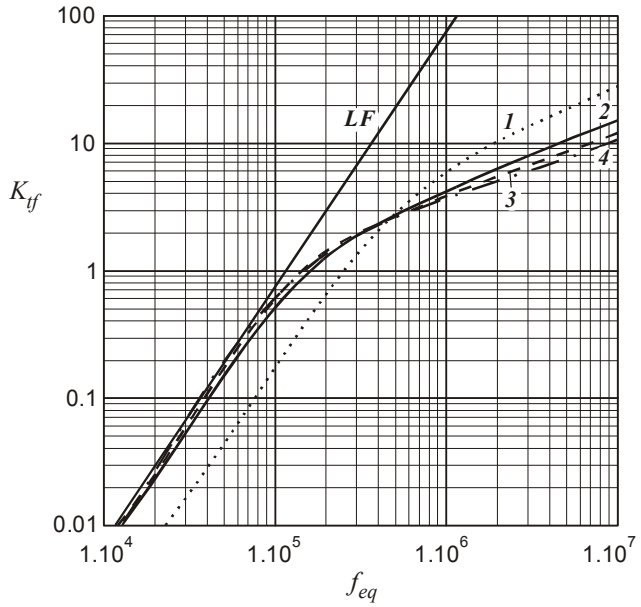

Fig. 1. Typical transformer factor K_{tf} for d = 0.5 mm, $\rho_c = 23 \cdot 10^{-9}$ Ω.m and λ = 0.5 at η = 0.9; 1) dotted line: half layer, m_E = 0.5; 2) solid line: single layer, m_E = 1; 3) dashed: two layers, m_E = 2; 4) dash-dot: three or more layers, m_E > 2. LF– low frequency approximation [12].

The parameter equivalent frequency f_{eq}, Fig.1, is given as:

$$f_{eq} \approx f_{op}\left(\frac{d_p}{0.5\ mm}\right)\left(\frac{d_p}{0.5\ mm}\right)\left(\frac{23\cdot10^{-9}\Omega.\mathrm{m}}{0.5\ mm}\right) \tag{3}$$

where f_{op} is the apparent frequency, d_p is the practical wire diameter and ρ_c is the conductor resistivity.

III. Comparative Study of Winding Arrangements

For the designs we consider ferrite material which is today the most common choice for power transformers in high-frequency switching power supplies. The material chosen is N87 made by EPCOS [13]. It is MnZn ferrite for use up to 500kHz, which in terms of eddy current losses is highly recommended. Other materials like TP4, DMR40, 3C94 are very close to it as properties.

Here we investigate four different cases (Fig.2) of conductors' diameters and winding arrangements, stated in section I:

1. Case 1, Fig.2, solid round wires with diameters, equal to the next available sizes in respect to the calculated by the methodology;
2. Case 2, Fig.3, solid round wires, increased diameter and whole winding width of the coil former is filled;
3. Case 3, Fig.4, solid wire for the primary at full winding width and a Litz wire for the secondary winding [14];
4. Case 4, Fig.5, solid wires, primary and secondary windings are interleaved, PSP type.

Remarks:

- The designs are made without additional spaces for creepage and clearance distances.
- For best results of the interleaving, each of the primary and secondary windings fit within a single physical layer and the whole winding width is filled.
- Having PSP arrangement and primary winding within a single layer means that the two primary winding layers are connected in parallel each of which carry the half of the primary current.

The obtained design results are summarized in Table 1.

The images of Fig.2, Fig.3, Fig.4, Fig.5 represent different realizations of a designed power transformer with input parameters $V_{prim,rms} = 300$ V, $V_{sec,rms} = 100$ V, $I_{sec.rms} = 12$ A, $f_{op} = 25$kHz.

TABLE 1. DESIGN PARAMETERS OF FOUR WINDINGS ARRANGEMENTS, P=1200W, 25KHZ, N87, EE65/32/27, 27 TURNS PRIMARY AND 9 TURNS SECONDARY

Winding arrangements		d_{calc} [mm]	d_{chosen} [mm]	k_c [−]	$P_{allowed}$ [W]	P_{calc} [W]
Case 1	primary	0,847	0,9	0,177	2,467	2,758
	secondary	1,467	1,6	0,462	2,467	3,251
Case 2	primary	0,847	1,25	0,88	2,467	2,283
	secondary	1,467	4,00	5,632	2,467	2,36
Case 3	primary	0,847	1,25	0,88	2,467	2,283
	secondary	1,467	1,565 (245x0,1)	0,003	2,467	2,331
Case 4	primary	0,847	1,25	0,88	2,467	1,142
	secondary	1,467	4	2,186	2,467	1,134

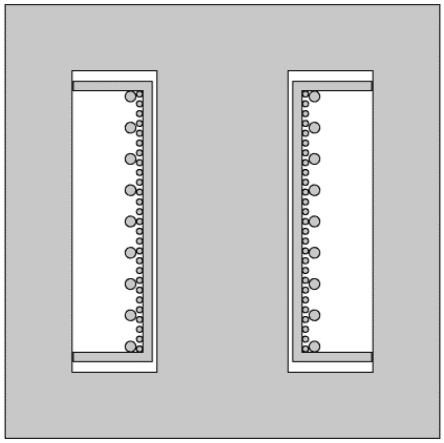

Fig.2. Case 1, solid round wires with diameters, equal to the next available sizes in respect to calculated.

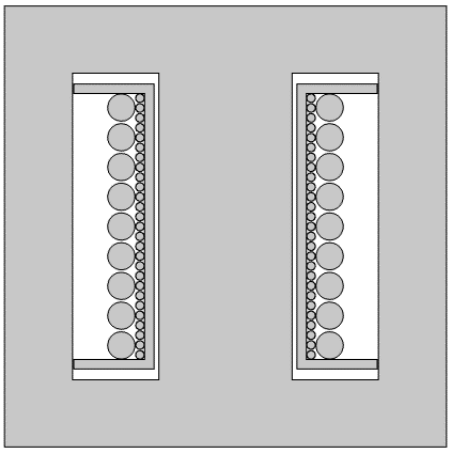

Fig.3. Case 2, solid round wires, increased diameter and whole winding width of the coil former is filled.

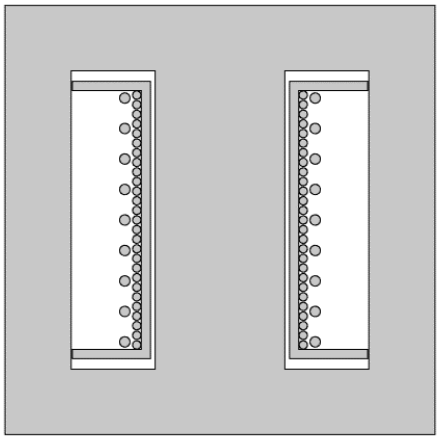

Fig.4. Case 3, solid wire for the primary at full winding width and a Litz wire for the secondary winding.

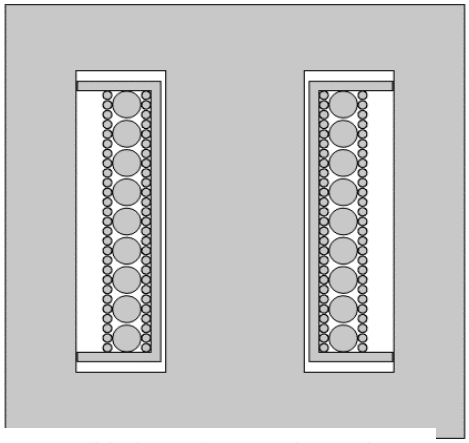

Fig.5. Case 4, solid wires, primary and secondary windings are interleaved, PSP type.

The design is realized by N87, EE65/32/27 core and the turns for primary and secondary winding are 27 and 9 respectively. In table 1, results are given which compare what diameter is needed (d_{calc}) and what diameter is chosen to be used (d_{chosen}).

Table 1 also contains information about the derived power losses for the four cases and the value of the coefficient k_c. For Case 1, the losses are too high. A way to reduce the losses is to increase the diameters, Case 2. In that case eddy current coefficient is still high, even much higher, but the ohmic copper resistance is greatly reduced and the total losses are under the critical values.

For the observed frequency it is evident that in Case 3 although the eddy currents are low the use of Litz wire in the secondary does not decrease much the losses when compared with Case 2. This is because the equivalent diameter of the wire used is almost as needed. If the Litz wire has a larger effective area, than the losses would become smaller but the heat transfer is deteriorated as a great portion of the Litz wire cross-sectional area is not copper.

The least power losses are obtained when interleaving is used, Case 4. The conductors' diameters are the same as in the Case 2 but there are some differences: the primary winding is made of two identical layers connected in parallel, thus the resistance that the primary current sees is two times less. The secondary winding is still the same as in Case 2, but the interleaving creates so called half-layer, thus the effective cross-sectional area of the conductor, which is effectively occupied by the current, is enlarged more than two times, i.e. the AC resistance is decreased by factor of two and a half.

The drawbacks of the design arrangement with interleaving, Case 4, are that more wires have to be stripped, and also that the capacitance between primary and secondary did almost double. Also the leakage inductance decreases with about a factor two. If these properties can be accepted, interleaving is an interesting alternative to Litz wire solutions. For a single layer or half layer the diameters can be increased to fill the whole layer to lower the losses, this is not true for 2 and more layers.

IV. CONCLUSIONS

The purpose of the paper is realization of comparative study of winding arrangements for power electronics transformers. The designs are based on an improved design algorithm consisting of 15 steps. Calculation of the eddy current losses in wires is made by a novel approach, suitable for fast and practical engineering designs. Four different winding arrangements are calculated and compared for the considered transformer: $V_{prim,rms} = 300\ V$, $V_{sec,rms} = 100\ V$, $I_{sec.rms} = 12\ A$, $f_{op} = 25kHz$.

The approaches compared are interleaving windings, fully wound winding layers and using Litz wire.

The comparison of the four Cases yields the following results:

- Using Litz wire, Case 3 does not decrease much the losses when compared with Case 2 (only round wires, completely filled the winding width of the coil former) layers). This is because the equivalent diameter of the wire used is almost as needed.
- If the Litz wire, Case 3, has a larger effective area, than the total losses would become smaller but the heat transfer is deteriorated.
- Interleaving windings, Case 4, provides the lowest total losses. A proper arrangement leads to AC resistance decrease by factor of two and a half.
- Interleaving windings is an alternative of Litz wire, if the design accepts increasing the capacitance between primary and secondary (almost double) and increasing the leakage inductance (about a factor two).

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Analysis of Reliability on the Electronic Circuit for LED Lamp

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Abstract – **Reliability prediction for a system of elements functioning jointly concerns identification of causes for failures in this system and also detecting the elements that can cause failures. This type of prediction is known as fault tree analysis and involves identification of the failure rate at a lower level of the system examined. Such type of analysis will be applied in the reliability study of driver circuit for LED Lamp**

Keywords – **LED driver, LED lamp, Failure Rate, Fault tree analysis, Reliability of electronic equipment.**

I. INTRODUCTION

The application of complex technical systems often requires solution of problems which are related to their reliability and maintenance, e.g. what kind of failures or combinations of them produce a defined reliability of the system and which is the lowest-price recovery of electronic equipment [1, 3].

The subject of the present article is electronic driver circuit for LED's lamp – figure 1. The main parameters are: LED Lamp type – UltraLUX, Fitting/Cap: E27, Output power – 15W, Input current – 100mA, lifetime of lamp bulb - 10000h or 10 years; Lifetime is based on the average usage of 2.7 hr. per day or 1000 hrs a year. This average is influenced by the usage during different seasons (dark winter vs. light summer), the weather conditions (sunny vs. rainy dark day) and on the room where the lamp is used (short usage in bathroom vs. long usage in living room).

II. PRESENTATION

A. Basic of electronic driver circuit for LED's lamp

Electronic driver circuits for LED's lamps are basically switching power supplies with an integrated high frequency inverter/switcher. Current limiting is then done by a very small inductor, which has sufficient impedance at the high frequency. Properly designed driver circuit should be very reliable. Their reliability depends on their location with respect to the heat produced by the lamps as well as many other factors, such as temperature stresses. Since these electronic drivers include rectification, filtering, and operate the LED's lamp at a high frequency, they also usually eliminate or greatly reduce the mains (220/240V, 50Hz) flicker.

The aim of the present paper can be formulated as follows: Analysis of quantitative parameters of reliability of electronic driver circuit for LED's lamp.

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Reliability of electronic circuits for LED's lamp depends on constituent components reliability. Elements of various reliability parameters are used and it is possible for sudden or continuous failures to occur during operation [4]. Failures are incidental and are distributed throughout time according to the law of distribution of random quantities throughout time. The greater the correspondence between actual distribution and the law which underlies its modeling, the greater the accuracy of calculation results will be [2, 5].

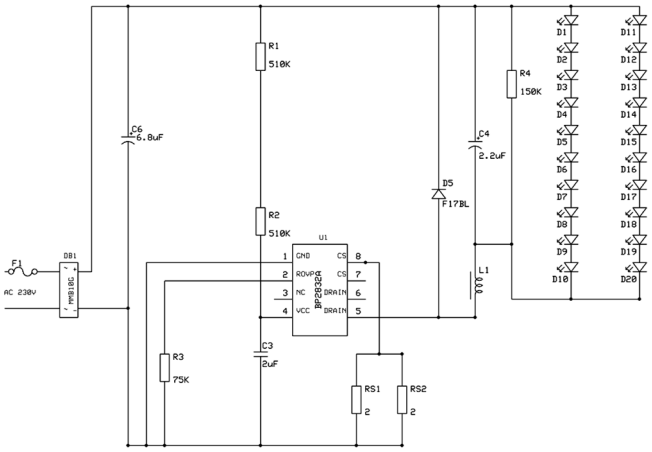


Fig. 1. Circuit diagram of electronic circuit of UltraLUX 15W LED's lamp.

B. Basic of electronic equipment and products reliability.

For the purpose of analyzing and calculation of operational reliability the following approaches are employed: generating of data base for the number and type of failures found in production batches of the same kind or applying established methods for calculation of quantitative parameters for reliability [2, 6].

According to [6] the generalized formula for calculation of failure rates is rendered by:

$$\Lambda = \sum_{i=1}^{n} \lambda_{EEi} = \sum_{i=1}^{n} \lambda_{bi} \pi_i, \ F.I.T. \qquad (1)$$

where: Λ is the failure rate of the investigated product (electronic driver circuits); n – the number of elements used; λEEi – failure rate of i-th element; λbi – reference failure rate of the i-th element which is defined under normal operating conditions, πi – factors describing operation modes and conditions that are classified in the corresponding sets of methods.

The main equation for failure rates (1) can be regarded as:

$$\Lambda = \sum_{i=1}^{n} \lambda_{EEi} = \pi_E . \pi_Q . \sum_{i=1}^{n} \lambda_{bi} . \pi_{Ti} . \pi_{Si}, \quad F.I.T. \qquad (2)$$

where: πE is corrective coefficient according to the operational conditions of respective product; πQ – is corrective coefficient concerning the quality of components used in the product; πTi – corrective coefficient concerning temperature of respective component in the product and πSi – corrective coefficient concerning electrical charge of the component.

From equation (2) it is possible to determine the basic directions by which the rate of failures is calculated – reference failure rate, heat modes, electrical load, quality of components and the impact of environment.

C. Reliability of electronic components in LED lamp.

To analyze the overall reliability of electronic circuits for LED lamp it is required to set up an equivalent substitution reliability circuit. The latter is connected with each element that is used in the electronic circuit. With this type of electronic products, the reliability connection between individual elements is in series: in case of failure of any electronic component the whole circuit will fail.

For electronic circuits for LED's lamp, which are in routine operational period, there should be applied the exponential law of random values distribution in time. By means of it and taking into account equation (2) it is possible to calculate the probability for failure free operation of the investigated product. In serial substitution circuit the following equation is applied:

$$P(t) = \exp(-\Lambda . t) = \exp\left[-\left(\pi_E . \pi_Q . \sum_{i=1}^{n} \lambda_{bi} . \pi_{Ti} . \pi_{Si} \right) . t \right]. \qquad (3)$$

where P(t) – is the probability for failure free operation of the power source, t – is the operational time of the LED's lamp.

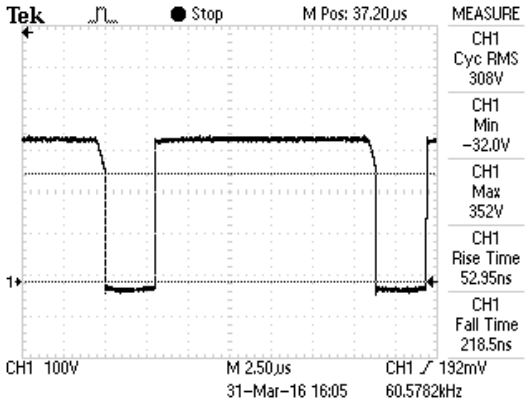


Fig. 2. Voltage U_{DSmax} of transistor in IC BP2832A.

Table 1 contains summarized electric modes of employed electronic components. Measurements have been made of the temperature of the electronic circuit during operation of LED lamp for the mean operation period of the lamp for one day-night period; the results being generalized in fig.4. Measurements have been made also of the electrical modes of the electronic circuits during operation of LED's lamp.

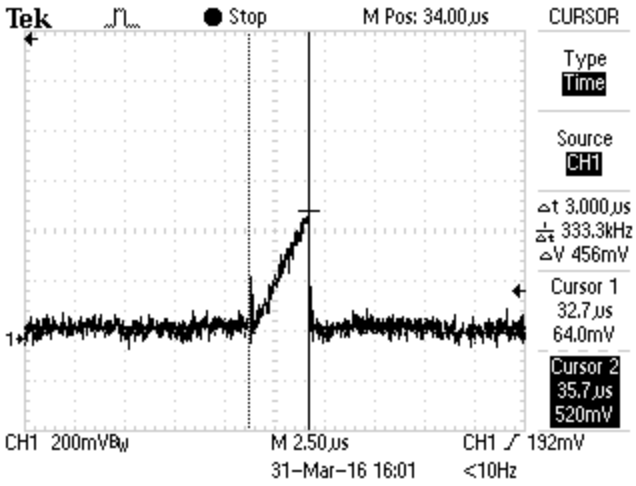


Fig. 3. Current I_{Dmax} of transistor in BP2832A (1A/1V div).

TABLE I
ELECTRIC MODES OF ELECTRONIC COMPONENTS OF LED'S LAMP 1

components	Nominal parameters			Operation parameters		
Diodes DB1 MCC20G	$U_{nom.}$	$I_{nom.}$	$P_{nom.}$	$U_{op.}$	$I_{op.}$	$P_{op.}$
	1000V	*1A*	*1W*	*340V*	*100mA*	*400mW*
Lamp	$U_{nom.}$	$I_{nom.}$	$P_{nom.}$	$U_{op.}$	$I_{op.}$	$P_{op.}$
	240V	*100mA*	*15W*	*230V*	*95mA*	*10W*
Resistors RS1, RS2	$P_{nom.}$			$P_{op.}$		
	0,125W			*0,090W*		
Resistors R1, R2, R3	$P_{nom.}$			$P_{op.}$		
	0,125W			*0,040W*		
Resistor R4	$P_{nom.}$			$P_{op.}$		
	0,125W			*0,024W*		
Capacitor C3 = 2uF	$U_{nom.}$			$U_{op.}$		
	35V			*15V*		
Capacitor C4 = 2,2uF	$U_{nom.}$			$U_{op.}$		
	400V			*65V*		
Capacitor C6 = 6,8uF	$U_{nom.}$			$U_{op.}$		
	400V			*340V*		
Choke L1	P_{nom}, *W*			P_{op}, *W*		
	12			*10*		
IC U1 BP2832A	$U_{nom.}$	$I_{nom.eff}$	$P_{nom.}$	$U_{op.}$	$I_{op.eff}$	$P_{op.}$
	600V	*200mA*	*400mW*	*336V*	*120mA*	*188mW*
LED's	$P_{nom.}$			$P_{op.}$		
	0,7W			*0,5W*		

Parameters of reliability of electronic areas have been analyzed following measurements made.

1. Failure rate of the rectifier module MCC10G.

$$\lambda_{DB1}(t) = 4.\lambda_{b\_diode}.\pi_T.\pi_V.\pi_C.\pi_Q.\pi_E \qquad (4)$$

where:

- λ_{b_diode} – base diode failure rate according MIL-HDBK-217F, where for mains rectifier diodes λ_{b_diode} = 3,8FIT .
- π_T - corrective coefficient concerning crystal temperature.

$$- \quad \pi_T = \ell^{-3091\left(\frac{1}{T_j + 273} - \frac{1}{298} \right)} \qquad (5)$$

where: T_J - crystal temperature – calculated from:

$$T_J = T_A + R_{th}.P_{DISS} \qquad (6)$$

where: T_A – ambient temperature (temperature in LED lamps); $R_{th} = 85^0$C/W –diode „crystal – case" thermal resistivity, P_{DISS}- diode dissipative power - $P_{DISS} = U_{AK}.I_{AK}$ = 500mW – from table 1.

$T_J = T_C + R_{th}.P_{DISS} = 35 + 85.0,5 = 35 + 42,5 = 77,5^0$C

For corrective coefficient π_T equals: $\pi_T = 4,88$

- π_V voltage corrective coefficient – nominal and operate diode voltage are measurement and from (4) equals:

$$\pi_V = \left(\frac{U_{APPL}}{U_{NOM}}\right)^{2,43} = \left(\frac{620}{1000}\right)^{2,43} = 0,31 \quad (7)$$

- π_C = 1 – corrective coefficient concerning diode pin design;

- π_Q = 8 – corrective coefficient concerning the quality of components cases;

- π_E = 1 – corrective coefficient concerning the component application area.

Failure rate of the rectifier module equals:

$\lambda_{DB1} = 4.\lambda_{b\_diode}.\pi_T.\pi_V.\pi_C.\pi_Q.\pi_E = 4.3,8.4,88.0,31.1.8.1 = 183,95FIT$ (8)

2. Failure rate of the resistors RS1 and RS2.

Failure rate of the resistors equals:

$$\lambda_{RS1}(t) = 2.\lambda_{bR}.\pi_T.\pi_P.\pi_S.\pi_Q.\pi_E \quad (9)$$

- where: λ_{bR} - base resistors failure rate according MIL-HDBK-217F, where for composition resistors λ_{b1} = 1,7FIT.

- π_T - temperature coefficient of resistors, which for 35^{0}C equals to 1,30, from MIL-HDBK-217F.

- $\pi_P = (P_{DISS})^{0,39}$ – nominal power coefficient. For RS1 and RS2 resistors with nominal power - 125mW, this coefficient equals to π_P = 0,44

- π_S power corrective coefficient:

$$\pi_S = 0,54.\ell^{2,04.\frac{Actual\ Power}{Rated\ Power}} \quad (10)$$

$$\pi_S = 0,54.\ell^{2,04.\left(\frac{0,090}{0,125}\right)} = 2,344$$

- π_Q - corrective coefficient concerning the quality of resistors, π_Q = 3,00

- π_E - corrective coefficient according to the operational conditions. For industrial operational conditions π_E = 1.

Failure rate of the resistors RS1 and RS2 equals:

$$\lambda_{R1}(t) = 2.1,7.1,30.0,44.2,345.3.1 = 14,14FIT \quad (11)$$

3. Failure rate of the resistors R1, R2 and R3

Failure rate of the resistors equals:

$$\lambda_{R1}(t) = 3.\lambda_{bR}.\pi_T.\pi_P.\pi_S.\pi_Q.\pi_E \quad (12)$$

- where: λ_{bR} - base resistors failure rate according MIL-HDBK-217F, where for composition resistors λ_{b1} = 1,7FIT.

- π_T - temperature coefficient of resistors, which for 35^{0}C equals to 1,30, from MIL-HDBK-217F.

- $\pi_P = (P_{DISS})^{0,39}$ - nominal power coefficient $\pi_P = (P_{DISS})^{0,39}$. For R1, R2 and R3resistors with nominal power-125mW, this coefficient equals to π_P = 0,44

- power corrective coefficient:

$$\pi_S = 0,54.\ell^{2,04.\frac{Actual\ Power}{Rated\ Power}} \quad (13)$$

$$\pi_S = 0,54.\ell^{2,04.\left(\frac{0,040}{0,125}\right)} = 1,04$$

- π_Q - corrective coefficient concerning the quality of components cases π_Q = 3,00;

- π_E - corrective coefficient according to the operational conditions. For industrial operational conditions π_E = 1.

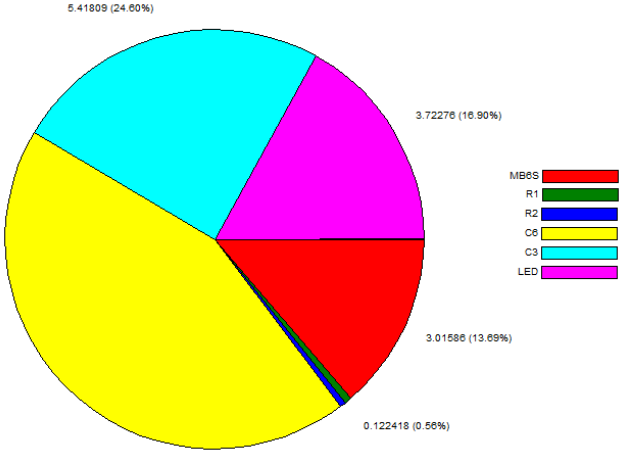
Failure rate of the resistors R1, R2 and R3:

$$\lambda_{R1}(t) = 3.1,7.1,30.0,44.1,04.3.1 = 9,01FIT \quad (14)$$

Results are summarized in table 2.

TABLE II
FAILURE RATES OF ELECTRONIC COMPONENTS OF LED'S LAMP 1

Elements	λ_{bi}, FIT	$\pi_{Ti°C}$ (T_A=78^{0}C)	π_{Si}	π_Q	π_E	$\lambda_{EEi°C}$, FIT
Diodes MCC20G	30	10,42	0,072	8	6	1080
Resistors RS1, RS2	10	1,6	0,696	6	4	535
Resistors R1, R2, R3	10	1,6	0,45	6	4	518
Resistors R4	10	1,6	0,39	6	4	150
Capacitor C3 = 2uF	3,6	7,83	1,42	10	10	4000
Capacitor C4 = 2,2uF	3,6	7,83	1,20	10	10	3382
Capacitor C6 = 6,8uF	3,6	7,83	10,42	10	10	27372
Diode D5	30	10	0,09	8	6	1296
Choke L1	2,7	2,37	1,03	3	6	119
IC BP2832A	25	7,244	4,945	8	6	42986
LED's 20pcs	3,50	3,62	1,53	8	2	6203



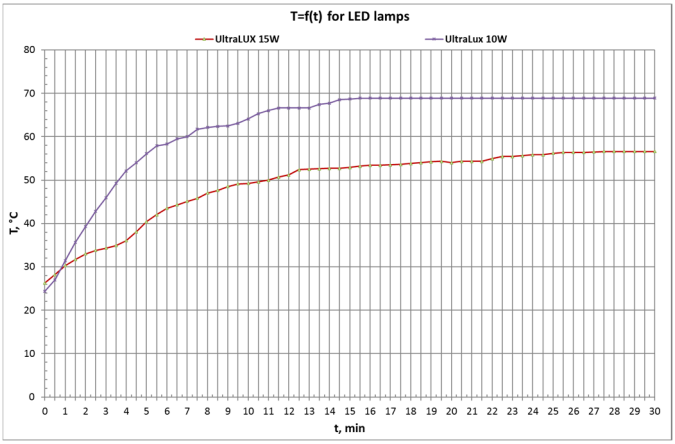


Fig. 4. Heat modes of investigated electronic areas.

The following analysis has been drawn concerning obtained results. General failure rate Λ_1 for LED's lamp1, at operating temperature T_A = 40^{0}C, equals:

$$\Lambda_1 = \sum_{i=1}^{n} \lambda_{EEi} = 87641\, F.I.T. \quad (15)$$

The probability of failure free operation P1(t) of LED's lamp1 for a period of one calendar year (t = 8760 hours) is:

$$P_1(t) = \exp(-\Lambda_1 .t) = \exp\left[-87641.10^{-9}.8760\right] = 0{,}464. \quad (16)$$

Mean time to failure with continuous use of LED1 equals:

$$MTTF_1 = \frac{1}{\Lambda_1}.\frac{1}{8760} = \frac{1}{87641.10^{-9}}.\frac{1}{8760} = 1{,}03\, years \quad (17)$$

Mean time to failure MTTF'1, at defined mean load of LED1 which is set by the manufacturer and equals 2.7 hours a day:

$$MTTF_1^{'} = \frac{1}{\Lambda_1}.\frac{1}{8760}.\left(\frac{24}{t_{on}}\right) = \frac{1}{84778{,}34.10^{-9}}.\frac{1}{8760}.\left(\frac{24}{2{,}7}\right) = 9{,}15\, years \quad (18)$$

Obtained results and their analysis indicate that within a period of one calendar year of continual work there should be expected 53.6% of the components to become defective. The obtained MTTF of the LED lamp1 = 12years and exceeds by 14% the warranty time of 8 years assured by the manufacturer.

For the second LED lamp2 the results are as follows:

The rate of failure for LED lamp2 at operating temperature $T_A = 60^0$C equals:

$$\Lambda_2 = \sum_{i=1}^{n} \lambda_{EEi} = 126327{,}9\ F.I.T. \quad (19)$$

The probability for failure free operation P2(t) of LED lamp2 for a period of one calendar year (t = 8760 hours) is:

$$P_2(t) = \exp(-\Lambda_2 .t) = \exp\left[-126327.10^{-9}.8760\right] = 0{,}33. \quad (20)$$

Mean time to failure MTTF2, with continual use of electronic lamp equals:

$$MTTF_2 = \frac{1}{\Lambda_2}.\frac{1}{8760} = \frac{1}{126327{,}9.10^{-9}}.\frac{1}{8760} = 0{,}90\, years \quad (21)$$

For mean time to failure MTTF'2, with defined use of electronic lamp of 2.7 hours per day we get:

$$MTTF_2^{'} = \frac{1}{\Lambda_2}.\frac{1}{8760}.\left(\frac{24}{t_{on}}\right) = \frac{1}{126327{,}9.10^{-9}}.\frac{1}{8760}.\left(\frac{24}{2{,}7}\right) = 8\, years \quad (22)$$

Results obtained for this LED lamp2 indicate reduced time for operation amounting to 20% of the overall warranty time of the manufacturer and 33% concerning the other LED lamp1. Fig. 4 presents the curves of the probability for failure free operation of both investigated LED lamps. Referring to both curves it is possible to determine the permissible operation times at a certain reliability level for household consumers $P_{NORM}(t)=0{,}80$.

Obtained time references are MTTF1=2500h for LED1 and MTTF2=10000h for LED2.

With these values the mean time to failure MTTF1 at a predefined use of the electronic lamp of 2.7 hours per day:

- for LED1:

$$MTTF_{1_{years}} = \frac{MTTF_1}{8760}.\frac{24}{2{,}7} = 2{,}54\, years \quad (23)$$

- for LED2:

$$MTTF_{2_{years}} = \frac{MTTF_2}{8760}.\frac{24}{2{,}7} = 10{,}15\, years \quad (24)$$

Figure 5 presents the percentile of failure rates of individual components. It is evident that components which could cause failures are: choke L1, capacitor C4 and capacitor C5. Their resizing according to electrical parameters is requireable.

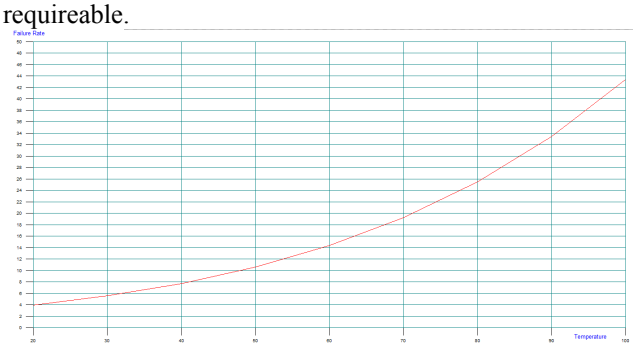
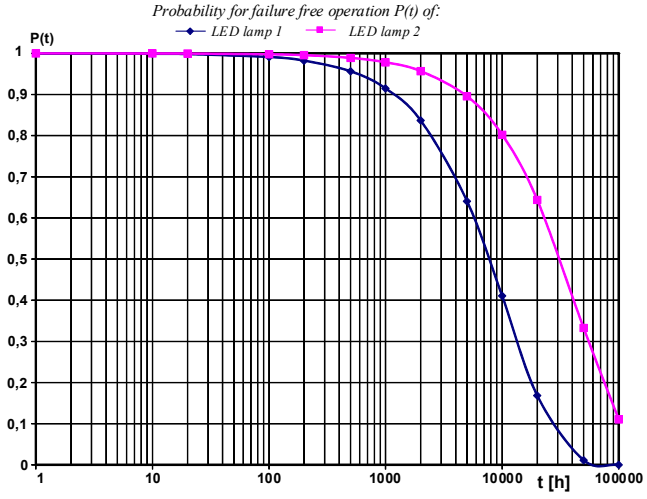


Fig. 5 presents the curves of the probability for failure free operation of both investigated LED lamps. Referring to both curves it is possible to determine the permissible operation times at a certain reliability level for household consumers $P_{NORM}(t)=0{,}80$.



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A Picosecond-resolution Hybrid Method of TDC Implementation in FPGAs, Based on Differential Time Delays

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Abstract – **Time-to-digital converters (TDCs) are useful and required building blocks in the field of fast measurement of small time intervals. When they are implemented through the use of time delays, there are three basic approaches for that, each with its benefits and downsides. However, trade-offs between speed, accuracy and precision are always present between them, which necessitates fine tuning of each created TDC for a specific purpose. This article proposes a new approach to a delay-based TDC implementation – a hybrid between the aforementioned basic approaches with an added external differential delay. This avoids some downsides of the hybrid constituents at the cost of prolonged and more complex system start-up sequence.**

Keywords – **Time-to-digital converters, delays**

I. Introduction

In order to implement fast measurements of short time intervals, with accuracy ranging from 1 ps[1] to 17 ps[2], time-to-digital converters are most often used. A rather large subset of those utilize gate delays as a base of Delay lines[1],[3] and DLLs (delay-locked loops).[4],[1],[3],[5] The advancement of micro- and nanoelectronic technology allows for accurate prediction of those gate timing parameters, however propagation delays are heavily dependent on environmental conditions – such as voltage and temperature shifts, which always call for different types of compensations.

TDC-based time measurement equipment is a subset of measuring devices and as such is subjected to the same analysis methodologies. In terms of measurement specifics there are three basic criteria, on which measuring equipment is being judged:

- speed – it is defined as the delay between receiving the event to be measured and producing a quantized result of some of the events properties;
- accuracy – this property represents how close the measurement result is to the actual measured event property;
- precision – represents the definition with which the result is being measured.

In the majority of cases there is an emphasis on one or two of those properties at the expense of the rest. So far in order to achieve a high enough rate of all three, the approach is to elaborate the measuring equipment in various ways, most of them are either too expensive, or proprietary, or both.

In the current paper it is being proposed a new approach to time interval measuring equipment implementation, based on:

- in terms of methodologies – time delays and advanced preparation algorithm;
- in terms of equipment – programmable logic devices (CPLD and FPGA), as well as a possibility for ASIC implementation; external to the logic device time delay introduction

II. Theoretical Description of the Hybrid Method

A. Basic mode of operation

At the core of the equipment is a constant running loop, whose nodes are delayed from each other by a certain time Δt_D (fig.1).

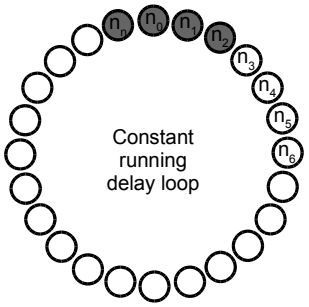

Fig. 1. Rough presentation of the constant running delay loop with nodes n_0 to n_n

The state of the loop is being stored on every "Start" and "Stop" event. The difference in the stored "Start" and "Stop" states of the loop gives the result as a multiple of Δt_D. Fig 2 shows an example of a measurement for two states, the result of which is three time delays Δt_D.

It can be seen, that the result is taken as a difference only between the leading active (colored) nodes. The difference between the total number of active nodes represents a shift in the state of the measuring system between "Start' and "Stop" events, and will be examined later on.

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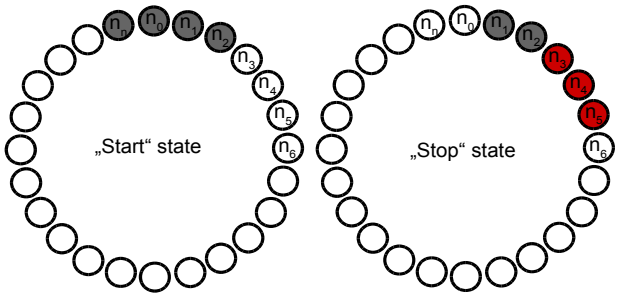

Fig. 2. Rough presentation of a measurement result between “Start” and “Stop” events

In fig. 3 is shown the basic functional diagram of a measuring device, using the proposed methodology.

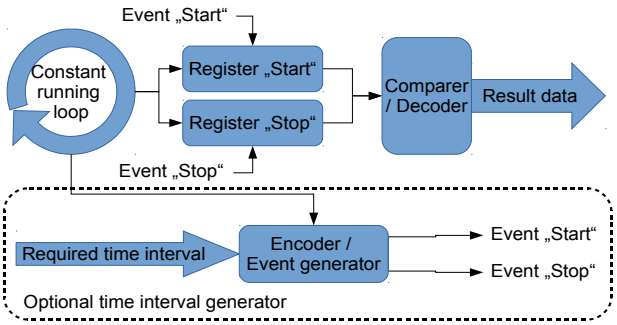

Fig. 3. Functional diagram of the proposed hybrid methodology

B. Constant running delay loop.

The constant running delay loop consists of a number of nodes, delayed from one another by a time delay, equal to Δt_D. This delay specifies the equipment’s precision. Each node consists of a frequency generator, with a period of T_N, as shown on fig. 4.

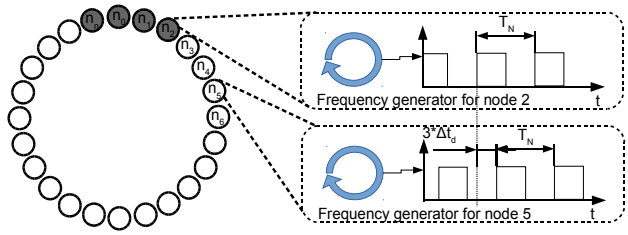

Fig. 4. Functional representation of a delay loop node

An important requirement for T_N of the generated frequencies is that

$$T_N \square n \square \Delta t_D \quad (2.1)$$

C. Registers for the “Start” and “Stop” signals.

Given the function of the nodes for the constant running delay loop, the registers for “Start” and “Stop” event must store the current value for each node on each corresponding signal. For example, from fig. 2, the stored values for the registers are as follows:

“Start” - nodes n through 2 “active”, rest “inactive”

“Stop” - nodes 1 through 5 “active”, rest “inactive”

D. Comparer and decoder of the stored states

This block’s function is to define the leading node for both “Start” and “Stop” states and determine the difference between them, as well as show the result in a representative matter. For example, from fig. 2, the function is as follows:

1. Leading node for “Start” state is n_2.
2. Leading node for “Stop” state is n_5.
3. Their difference is three nodes – the result is 3 [Δt_D].

E. (Optional) Encoder for generation of specific time intervals

Given that there is a constant running loop, there is a possibility of generating time intervals with a precision of Δt_D.

The logic to follow is the same as the decoder, described above, only in reverse order, as shown below:

1. Receive the required time interval as a natural real number N_E;
2. Define a leading node for the generated “Start” event;
3. Define a leading node for the generated “Stop” event as a sum between the leading node for “Start” and N_E;
4. Connect the output for event “Start” to the leading node for “Start”;
5. Connect the output for event “Stop” to the leading node for “Stop”;

III. Implementation of the Hybrid Method

The described above method is implemented in a MAX10 FPGA device (10M08DAF484), produced by Altera.

For practical purposes, there have been introduced some specifics in the process of implementation.

The number of nodes used is 256, as it is a high enough number for measurements, but low enough to be manageable inside the FPGA, and the result is an 8-bit number.

A. Node and registers implementation

In order to minimize noise and error, due to signal propagation in the FPGA, the frequency generators and “Start” and “Stop” registers are implemented in two Logic array blocks (LABs) for each node.

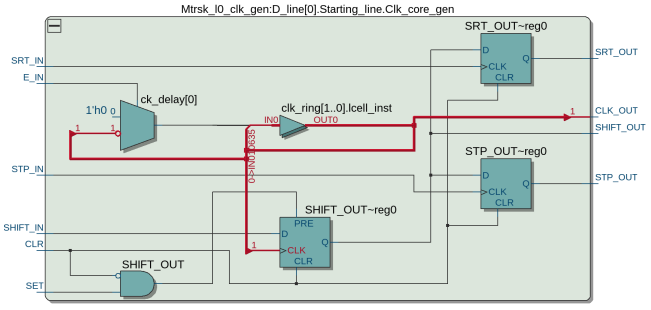

Fig. 5. Implementation of a delay loop node

- The red marked chain is the frequency generator, based on a buffer delay chain loop. The multiplexer serves as a control for the loop, defined by the state of input E_IN.

- D Flip-Flops SRT_OUT and STP_OUT are the state registers for “Start” and “Stop” events. Signals SRT_IN and STP_IN represent those events, and are global clocking signals.
- The SHIFT system, consisting of signals SHIFT_IN and SHIFT_OUT, as well as the SHIFT_OUT Flip-Flop and logic is used for synchronization. Since the SHIFT_OUT Flip-Flop is being driven by the generated frequency, its input (signal SHIFT_IN) comes from a corresponding node, spaced a number of time delays, equal to or greater than the propagation delay of a D Flip-Flop in the FPGA. This connection is shown in fig. 6

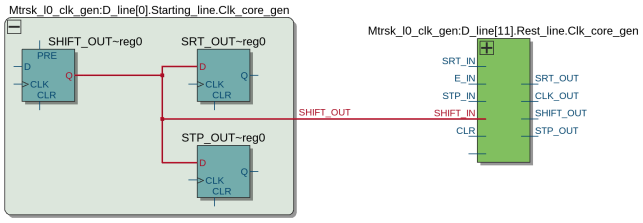

Fig. 6. Shifting connection

B. Constant running delay loop generation algorithm

In order to create the loop in a monolithic device as an FPGA, an external delay line has been introduced. This approach requires the use of an algorithm to generate the constant running delay loop.

1. All nodes are turned on, and are running chaotically.
2. All their outputs are being multiplexed to a single output for the FPGA, which is being used by the delay generator as:
   1) a base signal (considered non-delayed)
   2) delayed signal, with a delay of Δt_D
3. In the beginning of the algorithm, the base signal is being used
4. Starting from the last node, its generated frequency output is used to turn of, and then on the second to last node. This way, the generated frequency has been turned on after a delay of t_{Apd} in respect to the last node. The delay is a sum of all propagation delays, which are on the way of the base signal.
5. When the second to last node frequency generation is complete, its output is used to synchronize the node before it. Now this node is delayed by $2*t_{Apd}$ times in respect to the last node. This process is repeated until node n_0 is reached.

(3.1) $$n_0(delay) = n \cdot t_{Apd}$$

6. When node n_0 is reached, it has been delayed $n*t_{Apd}$ times in respect to the last node (in this case, n is 256).
7. The source of the signal is switched to the delayed one.
8. The whole process is repeated, but in reverse order – n_0 output synchronizes n_1 generated frequency, and so on.
9. When node n_1 is synchronized by n_0, it has been additionally delayed by an amount of time, equal to $t_{Apd} + \Delta t_D$, in respect to the last node. When added to its current delay of $(n-1)* t_{Apd}$, the cumulative delay is:

(3.2) $$n_1(delay) = (n-1) \cdot t_{Apd} + t_{Apd} + \Delta t_D$$
$$n_1(delay) = n \cdot t_{Apd} + \Delta t_D$$

10. When the last node is reached in this way, the state of a number of SHIFT_OUT Flip-Flops is set to “active”, while the rest are inactive. This number is equal to:

(3.3) $$N_{FFs} = \frac{t_{PDFF}}{\Delta t_D}$$, where

- N_{FFs} is the number of SHIFT_OUT Flip-Flops to be set;
- t_{PDFF} is the propagation delay of a single D Flip-Flop (defined by the manufacturer)
- Δt_D – the introduced time delay between the base and delayed signals from the delay generator.

11. After the SHIFT_OUT Flip-Flops are set, the algorithm is complete, and the constant running delay loop is created.

This algorithm is being completed by the circuitry, shown in fig. 7

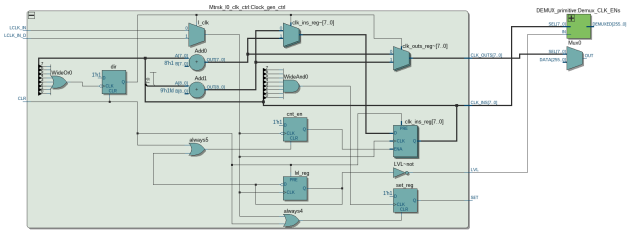

Fig. 7. Algorithm circuitry

In the above figure, the signals are as follows:

- LCLK_IN – the base (non-delayed) clocking input signal
- LCLK_IN_D – the delayed clocking input signal
- CLK_INS – used as a select for the demultiplexer, which in turn controls the E_IN signals for each node. Only one E_IN is active at any moment.
- LVL – used to toggle the output of the CLK_INS demultiplexer
- CLK_OUTS – used to control the selection of an output clock from the nodes
- SET – used to set the SHIFT_OUT Flip-Flops.

C. Definition of time delay difference (Δt_D)

From (3.1) and (3.2) can be deducted, that for node nn, the delay will be

(3.4) $$n_n(delay) = n\square t_{Apd} + n\square\Delta t_D$$

This means that for any couple of nodes, the difference between them is equal to:

(3.5) $$n_p - n_q = (n\square t_{Apd} + p\square\Delta t_D) - (n\square t_{Apd} + q\square\Delta t_D)$$

$$n_p - n_q = (p - q)\square\Delta t_D$$

Theoretically, Δt_D, can be any arbitrary value. It is however, is constrained by the physical capabilities of the delay generator and integrated circuit in terms of timing definition.

Current experimentation is being conducted with:

(3.6) $$\Delta t_D = 78{,}125\, pS$$

Its value was chosen as a result of a measured time interval equal to 20 ns, divided by the number of nodes used for the constant running delay loop, which is 256.

The delay generator in turn is implemented as two different PCB traces, possessing different time propagation delays.

In the case of positive results from the experiments, the time interval and time delay difference will be incrementally reduced as much as possible.

D. Comparer and decoder of the stored states

The decoder is implemented as a logic relation between the two "Start" and "Stop" registers. Since its size for 256 input elements is too large to display, for convenience, fig.8 shows its principle for 8 input elements.

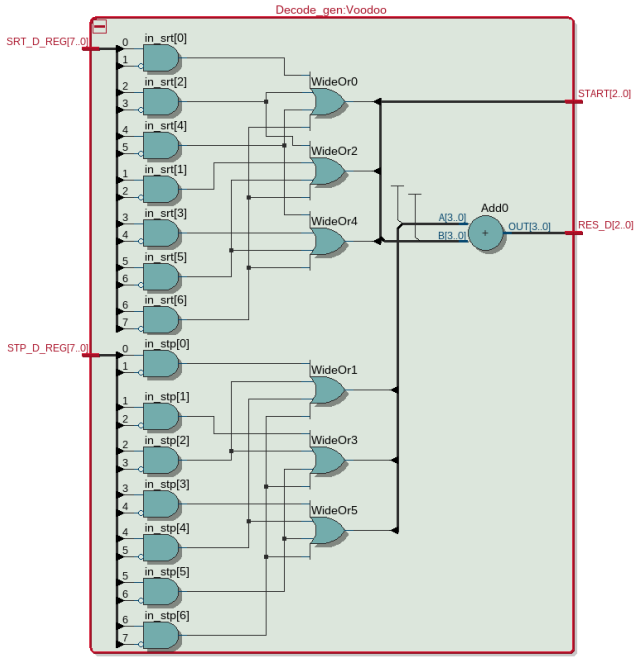

Fig. 8.Decoder/comparer circuitry

The AND logic gates determine the leading node for each register. The OR gates convert the result in binary numbers, which are then subtracted to produce the result in a binary format.

E. (Optional) Encoder for generation of specific time intervals

Given the stored "Start" register as a base point for a "Start" event generation, the "Stop" generation is reduced to simple addition. The resulting binary numbers are then used to control multiplexers, analogously to the one for the node generated frequencies outputs.

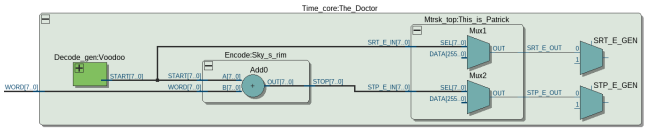

Fig. 9.Encoder/event generator circuitry

IV. Conclusion

The suggested approach in this paper is new and promising in its performance. It is possible to implement it in a variety of devices and theoretically can provide substantial improvement in speed, accuracy and precision in time measurement without added complexity in equipment manufacture. However further and more in-depth analysis and experiments must be carried out, in order to back up these claims.

Acknowledgments

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Light Pulse Generator for Multi-Element scintillation detectors testing

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Abstract – **This paper discusses the key characteristics and the specific requirements for light pulse generators for testing multi-element scintillation detectors. A prototype of such a generator has been built and studied. The block diagrams and the schematics of the LED amplitude drivers of its individual channels are presented. Some key signals obtained with the light pulse generator are also shown.**

Keywords – **Light Pulse Generator, Multi-Element scintillation detectors testing**

I. Introduction

Multi-element scintillation detector systems have been intensively designed and used in the recent years. They consist of many scintillators in a specific setup, oftentimes arranged in several layers. These detectors are mainly used for track reconstruction of high energy particles or for image reconstruction in medical diagnostic tools.

Organic scintillators are commonly used in the form of a square or triangular prism with cross section area of 0.5-1.0 cm^2 and length of several tens of centimeters to 2-3m [2]. Signals are picked up from the side area by coupling suitable photo detectors. Another possibility which has become popular in the last years is gluing an optically transparent fiber in a side groove along the scintillator. The fiber's material usually contains a wavelength shifting substance (WLS), most often from the UV or blue to the blue and green part of the optical spectrum. This construction allows for better collection and transfer of the photons produced in the scintillator, as well as for a simple and effective coupling to different photo detectors. The fibers also make possible the easy optical coupling of several elements to a common photo receiver.

The optical signal is traditionally picked up by vacuum photomultiplier tubes (PMT), avalanche photodiodes (APD) (only for time measurements) or p-i-n photodiodes. Lately semiconductor photomultipliers (SiPM) and multi-anode vacuum photomultipliers (MA PMT) have become widely used alternatives [1],[3].

Some of the key goals when building a multi-element scintillation detector are the testing and the control of the performance of its elements (mechanical integrity, photon flux collection etc.), the photo sensors and the pulse shaping electronics. Thus the requirement for building specialized test equipment which would allow testing the performance and the quality of the individual scintillators, and also the collection and transfer of the photons produced in their volume arises. To accomplish this it is necessary to have the means to generate short light pulses with the closest possible characteristics to the real ones arising from the ionizing radiation. [4].

The design requirements for such test generators include (but are not limited to): their spectral distribution, the length and the intensity of the light pulses, which have to vary within certain intervals, and a good temperature and long term stability. When testing complex multi-element detectors, test pulses must be generated simultaneously for a considerably large number of channels [4],[6].

In order to simulate the response of different types of scintillators (non-organic or organic), the light pulse duration has to vary within a wide range - from several ns to few µs. Though, it is usually sufficient to control the pulse intensity in as few as 16 to 32 amplitude levels.

II. Hardware Design

The light pulse generator, described below, is designed to meet the above-mentioned requirements for complex scintillation detectors systems testing.

A. General setup and structure

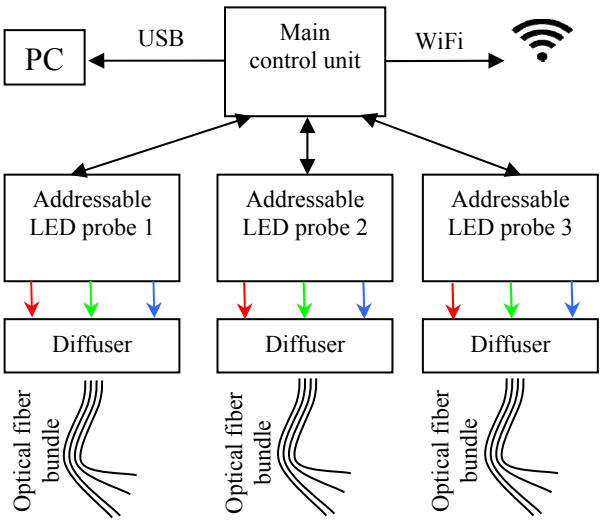

Fig.1. Test generator block diagram

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The block diagram of the generator is shown in Fig.1. It consists of a main controller which also acts as a master oscillator for the addressable remote probes. It can produce three timing signals. Each timing signal drives all three LEDs of a single probe on/off simultaneously. The light intensity of each LED is set individually by the controller.

Each probe has an optical diffuser and an optical fiber bundle attached to it. This allows cloning the light pulse to many channels. It is also possible to use different fiber lengths to assure a preset delay between the output pulses.

B. System modules

Main Control Unit

The main control unit is based on dsPIC33EP64GS504 digital signal processor (Fig.2). It generates two independent pulse series PULSE1 and PULSE2 with adjustable pulse length and phase (time delay).

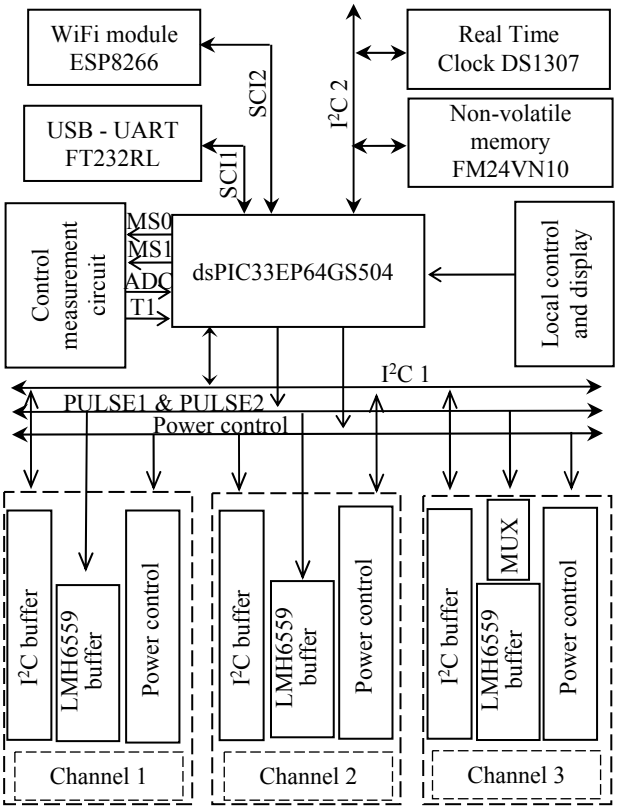

Fig.2. Main control unit block diagram

Three buffer modules are used to transmit the timing pulses and the control signals to the remote LED probes. The first two are driven by pulse series PULSE1 and PULSE2, respectively, and the third buffer can be connected to either of the pulse series (operator controlled).

The individual probes are controlled via an I^{2}C interface. The power supply to each probe can be switched on/off by the controller. To ensure the equal arrival time of the timing pulse to each probe the coaxial cables transferring the pulses have to be of equal length.

There is a reconfigurable control measurement circuit available, which can be used for the evaluation of some static and dynamic parameters of the individual light channels. It can be configured to work with different types of external photon detectors – p-i-n diodes, PMT or SiPM.

The system has a real time clock and calendar and some non-volatile memory for recording parameters and results.

Some parameters and operation modes can be controlled directly by buttons, which is convenient when working *in-situ*, with the detector system. The local LED indicators can be switched off for work in 'dark' rooms to avoid their influence on the data acquisition process.

The generator has an onboard USB-to-Serial Interface convertor and a WiFi module for connection to the upper hierarchical level system (e.g. a computer).

Addressable LED probe

The block diagram of the addressable LED probe is shown in Fig.3. A 16 bit I/O expander converts the I^{2}C signals into a parallel code. Three 5-bit groups are used to keep the DACs' settings. Their output is synchronized with the timing pulse from the master oscillator. The output voltages are converted to currents. The currents are fed to fast current mirrors which in turn drive the LEDs. This guarantees that different types of LEDs will have the same driving current, independent of the LED voltage, and makes possible the adjustment of the output current, allowing for equal light output.

The timing pulse input is buffered by a level translator to match the impedance of the pulse transmission line.

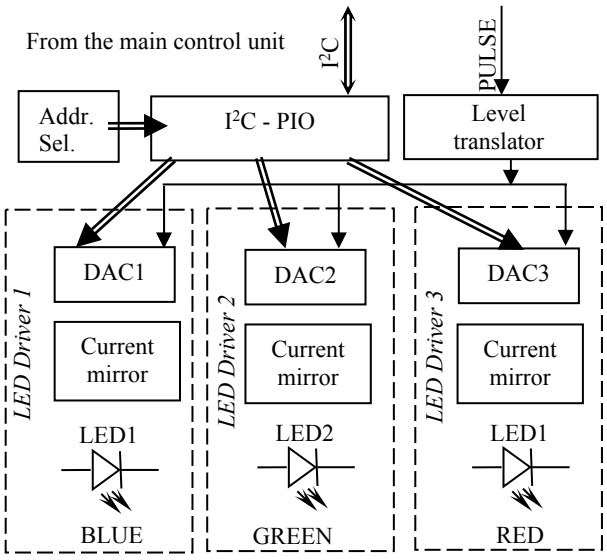

Fig.3. Remote LED probe block diagram

C. Novel schematics and solutions

Due to the limited space of this article it is impossible to present the whole schematic of the system. Hence, we discuss in detail only some unconventional circuits and solutions.

The LED driver

The LED driver schematic is shown in Fig.4.

In its core is a current summing DAC based on three-state output buffers (U1-U5). The inactive bits of the control word bring the corresponding buffer into a high-impedance state; so, it does not contribute to the common current formation. The performance of the module relies on the 74LVC1G126 high-speed, high-current output buffers.

In order to ensure a precise and stable output current, all used resistors have 1% tolerance and under 100 ppm/K thermal instability. The currents are summed by the Q2 transistor, connected in a common base circuit. Care has been taken to avoid its saturation and ensure the module performance.

The current pulse, already shaped in amplitude and length, is reflected by a current mirror based on the 5 GHz wideband transistors BFT93. The mirror coefficient can be fine-tuned within certain limits and allows equalization of the LEDs' light intensity despite their different light yield. The proposed schematic guarantees the same current through the LED independent of its type and forward voltage drop.

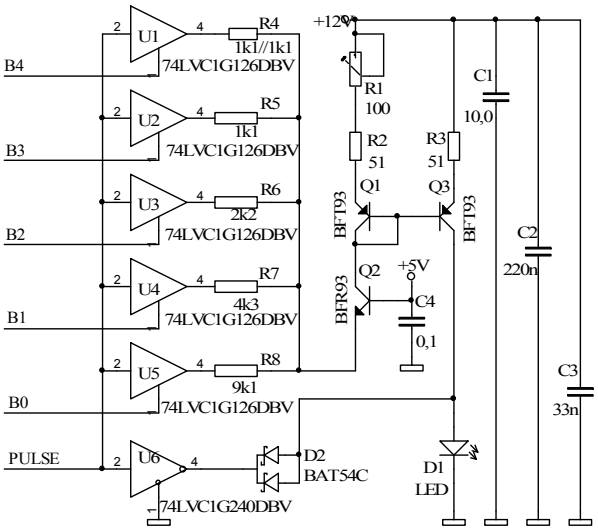

Fig.4. Schematic of the LED drivers

The buffer U6 and the diode D2 produce a blanking pulse that quickly dissipates the charge accumulated in the diffused capacitance of the LED. This guarantees a fast and precise shutdown of the light pulse.

Reconfigurable control measurement system

The schematic of the control measurement circuit is shown in Fig.5. It is based on AD7817-1 FastFET operational amplifiers. Its configuration is determined by the state of the analog switches U12 and U14.

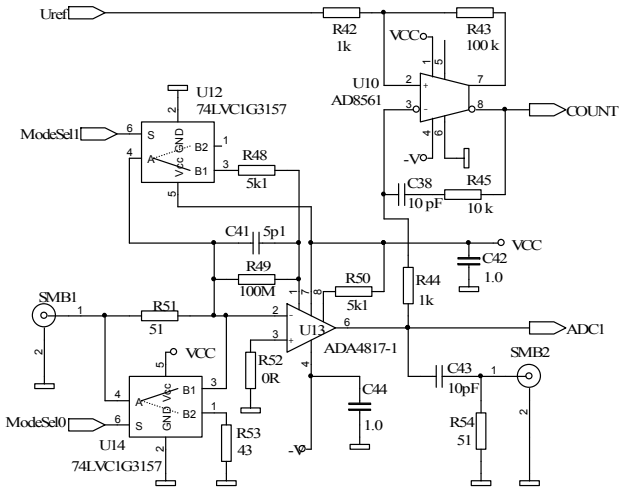

Fig.5. Reconfigurable test measurements system

The possible states are:

- ModeSel 0 = 0 and ModeSel 1 = 0 – the analog switches pass in the direction A-B1, so the input current flows directly to the amplifier input. The circuit behavior is dominated by the 5.1kΩ resistance. The system acts as a trans-impedance amplifier with 5 mV/μA sensitivity.

This allows measuring a photodetector's output current and calculating the light intensity for a given LED current.

- ModeSel 0 = 1 and ModeSel 1 = 0. The circuit is configured as a pulse amplifier with 50 Ω input impedance and voltage amplification $K_U \approx 100$.

If a photodetector is connected to SMB1 and the generator is in pulse mode, the output pulses have shape and length corresponding to the light pulses. In this mode it is possible to connect an oscilloscope on SMB2 and check the shape of the light output signals in the individual fibers.

In this mode it is also possible to configure the DSP for an external trigger input, and connect SMB1 to an external trigger source.

- ModeSel 0 = 0 and ModeSel 1 = 1. In this case the circuit works as a charge-sensitive amplifier. This configuration is suitable for small amplitude signal readout.

The amplifier's output is connected to one of the ADC inputs of the digital signal processor. This gives the possibility to implement additional procedures for the evaluation of the amplitude of the light pulses.

An integral amplitude discriminator is also added to the reconfigurable control system, realized by U10. The threshold is set by the built-in DAC of the DSP. The amplitude of the selected pulses is normalized and they are counted by the DSP for further analyses.

D. Technical parameters of the generator

The main characteristics of the light pulse generator are:

- Control via USB and/or WiFi connection;
- Connection of up to 4 external I^2C interface devices;
- Output pulse channels – 3;
- Minimum pulse duration – 8 ns, 1 ns increments;
- Output amplitude - 32 discrete levels, step size can be adjusted with a trimmer potentiometer;
- Reconfigurable pulse control channel with programmatically selectable configurations: charge-sensitive amplifier, trans impedance amplifier, voltage amplifier (K_U=100);
- Local control panel - 4 buttons + 4 LEDs;
- Power supply - unipolar, +12V, less than 1A.

III. Test Results

The next figures show oscillograms of the wave forms in some key points of the light pulse generator.

In Figure 6 channels C1 and C2 are the two individual timing pulse outputs, with separately controlled pulse lengths and phases. C2 has been configured to produce a minimal length pulse fed to a remote LED probe. Channel C3 shows the timing pulse input to the DACs, and channel C4 shows the LED blanking pulse.

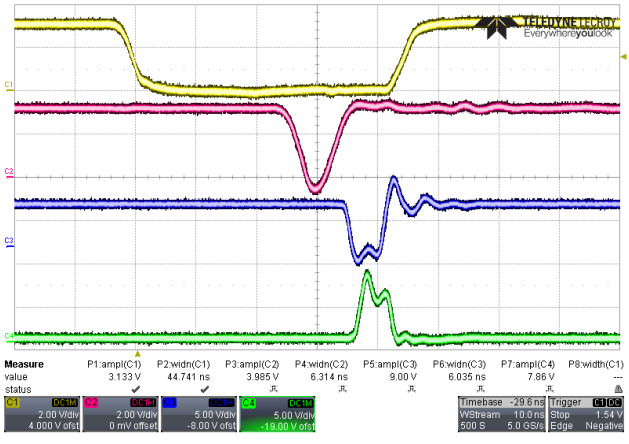

Fig.6. Timing pulse shapes at different points of the LPG

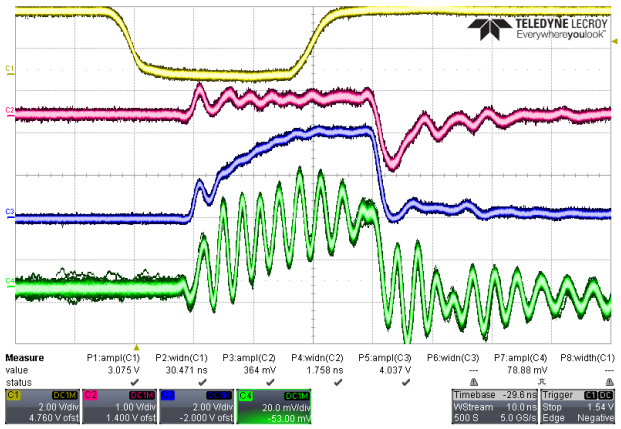

Fig.7. LPG electrical and optical output

Figure 7 shows the LPG output. Channel C1 shows the 30ns timing pulse, C2 and C3 the current and the voltage across the LED. Channel C4 shows the light output, observed with a Hamamatsu S5973 high speed p-i-n photo diode across a 200k Ohm resistance. Due to the high impedance of the circuit a lot of switching noise is induced.

Figure 8 shows the response of an S12571-025C Hamamatsu SiPM to a 16ns pulse with maximum light intensity. The pulses observed correspond to 15 to 40 registered photoelectrons. The used setup is typical for many different tests: the LED was coupled to one of the ends of a scintillating slab with an embedded s-shaped WLS fiber and the SiPM was coupled to the other end of the fiber.

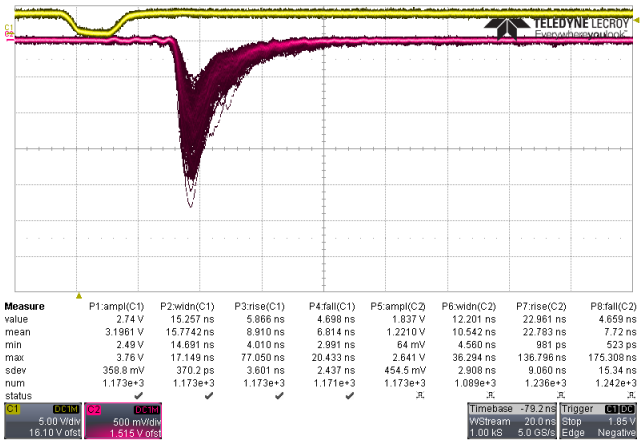

Fig.8. SiPM response to a 16ns pulse

IV. Conclusion

The light pulse generator is well suited for studying and testing of multi-element scintillation detectors. Different detector components can be studied like scintillator bars or slabs, whole scintillator modules, the front-end electronics as well as the control and data acquisition software.

The LED probes produce light pulses with up to three different wavelengths with independent amplitude control for each wavelength. The light pulse from each probe is split optically into 100 channels using a bundle of optical fibers. This allows for the easy coupling and studying of multiple detector elements at once.

Different detector parameters can be studied like: the light attenuation in the individual bars, optical crosstalk, frontend electronics response and software behavior. Studying some of those parameters/characteristics is only possible with such a test system. For others usually high-energy cosmic particles can be used, which is a lengthy process. The latter can greatly benefit in terms of speed (by orders of magnitude) when using the described test system instead. In the case of a multi-plane detector the generator allows separate control of all pulse parameters for each plane. This allows studying the coincidence behavior of the detector and the plane cross-talk.

The onboard reconfigurable test measurements circuit allows for the detailed study and tuning of a single optical channel. Scintillators and photo detectors (SiPM, PMT, MA PMT, p-i-n photodiodes etc.) can be evaluated independently of the frontend electronics.

Fig. 9. A photo of the generator

Acknowledgement

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LED Lamp for Dairy Barns – Design and Thermal Management

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Abstract – **Investigations in this work are connected with the design and thermal management of LED lamp with spectral characteristics suitable for dairy barns. Spectral power distribution (SPD), optimal for dairy cows is achieved by combinations of LEDs with different spectral characteristics and the control of the LEDs' operation. The thermal management theoretical calculations and the heat sink choice are experimentally tested at various ambient conditions (air temperatures from 20ºC to 45ºC) and at different currents through the LEDs. Infrared thermography is used for evaluation of temperature distribution at the LEDs' solder points and the heat sink. Thermal management investigations allow the determination of safe operating conditions for the LEDs at various ambient conditions.**

Keywords – **LED thermal management, illumination dairy barns.**

I. Introduction

It is known that lighting costs form a considerable part of the price of products. Thus replacing the existing lighting equipment with new, energy efficient based on high power LEDs and LED modules is highly relevant task. In the last few years development of energy efficient light sources for application in dairy barns is a very active research field [1 - 4]. Criteria for animal welfare in developed countries are elaborated in detail and include strict regulations in terms of animals' housing and conditions in them. The necessary light conditions for dairy cows include access to daylight during the day or artificial light, corresponding to the specifics sight of cows and during the night must be provided additional dimmable lighting. It is well known that the duration of the light and the spectral composition of light reflected on the milk production. At daylight (presence of blue light) melatonin levels decrease, but increase production of another hormone - IGF-I. The function of the IGF-I hormone is to stimulate the activity of the animal and therefore, its milk production [2]. It is assumed that in a 24-hour cycle for 16 hours daylight of 100 ÷ 200 lux brightness (measured one meter height) and 8 hours of darkness is empirically shown to give the best results. Maintaining brightness 150 ÷ 200 lux in whole dairy farm is very expensive and economically unprofitable. Therefore lighting systems in livestock farms should allow dimming the light output over a wide range; the spectral composition of the radiation to be consistent with the time of day and phase of development of animals. The required light levels can be achieved only in the dining areas around the heads of animals.

II. Problem Statement

Besides specific lighting requirements of livestock farms, mentioned above, must take into account several important features that have a significant impact on milk production. In dairy cows, like all mammals, the circadian rhythm depends on changes in light, temperature, food and water. It is assumed that the greatest influence on the circadian rhythm have the intensity and spectral composition of light [1-4]. It is known that the cows have a dichromatic vision, as their receptors are most sensitive in the spectral region between 440 and 480 nm, preferably between 455 and 475 nm and between 500 and 600 nm [1, 2] – Fig. 1.

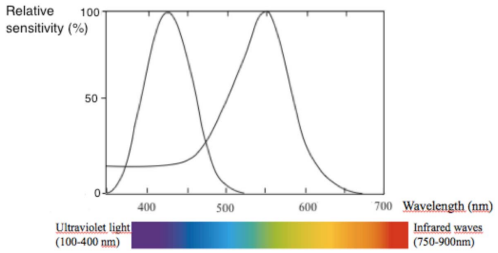

Fig. 1. Cows two cones sensitivity at different wavelengths.

Radiation in the blue region (440 ÷ 480 nm) suppress melatonin production, stimulates the hormone IGF-I production and increases the yield of milk. This includes the use of blue LEDs in luminaires for dairy farms and the use of white LEDs - neutral or cool white – Fig.2 [2].

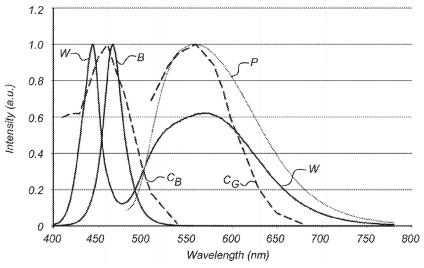

Fig. 2. Examples of LEDs' spectral characteristics suitable for dairy farming illumination C_B – blue part eye sensitivity curve, C_G – green part eye sensitivity curve, W – white LED, B – blue LED [2].

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Cow's vision isn't sensitive in the spectral region over 620 nm and it is accepted that artificial night lighting should be only in the red part of the spectrum to allow service in the barn without disturbing cows [1 - 4].

At realization of night lighting on the farm a very important feature of red LEDs must be considered - their light output decreases strongly with increasing junction temperature of LEDs – Fig. 3.

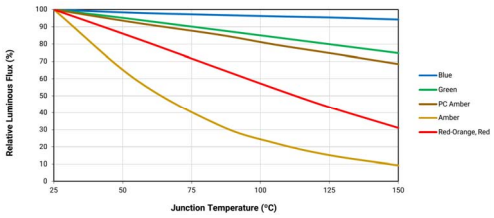

Fig. 3. Temperature dependence of relative flux vs. junction temperature (IF = 350 mA) [5].

This fact should be considered in thermal management – it is desirable to ensure operating of red LEDs at low junction temperatures even at relatively high ambient temperatures.

III. Experimental

Achieving the lamp's desired spectral power distribution demands combination of LEDs with different thermal properties and the need for proper thermal management. Comprehensive comparative analysis of the properties of the available LEDs with suitable characteristics is made with respect to the goals being set: proper spectral distribution and power, light (and energy) efficiency, lamp price etc. The LED operational parameters' differences in the magnitude of the input current, market availability and supply are considered also.

Analysis on the possibility of obtaining the desired spectral composition (fulfilling the criteria set above) is done by combining different types of LEDs based on the data specified by the manufacturer. A mixture of LEDs suitable for achieving the desired SPD is chosen -LEDs XLamp CXA and XPE family, CREE Inc (Fig. 4). The combination of one CXA 1816 module, four XPE blue and four XPE red LEDs is used in the design of the experimental lighting equipment.

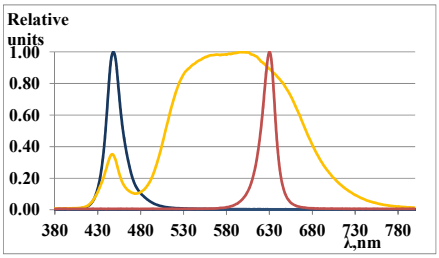

Fig. 4: Spectral characteristics of used LEDs; CXA1816 – yellow line; XPE blue and red – blue and red lines.

IV. Results

A. Luminous flux spectral power distribution

Radiation in the blue region is necessary for proper illumination in dairy barns [2], but it is well known, that sharp changes in the spectral characteristics of light reflected adversely on animal health. That is why LED with worm light is chosen for general illumination – CXA 1816. Its luminous flux is over 1800 lm (I_F = 450 mA, Tj = 85 °C = T_C) and it is sufficient for illumination of two to four cows housing (illumination over 200 lx at area near cows' heads). Equipment for spectral measurement of Stellar Net Inc. is used. Experimentally obtained spectral characteristic of used LED CXA are shown in Fig.5. By dimming the light of the blue LEDs it is possible to achieve the desired spectral composition of light in the barn smoothly, imitating the sunlight, without stress for cows. Exemplary spectral characteristics of light under different conditions are shown in Fig.6 – Fig.8.

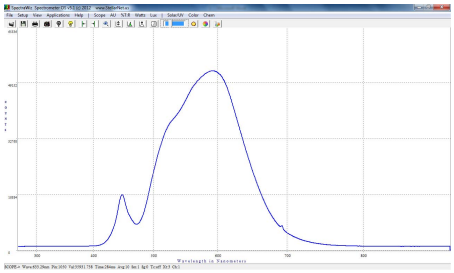

Fig. 5. Experimental spectral characteristics of used LED module CXA1816; forward current I_F = 450 mA; CCT = 3200K.

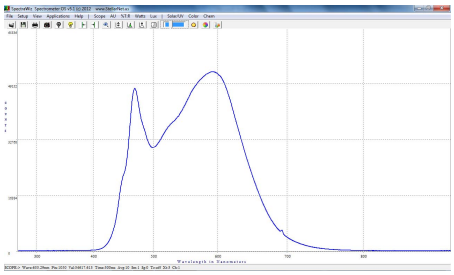

Fig. 6: Experimental spectral characteristics of used LED module CXA1816, forward current I_F = 450 mA and four blue XPE LEDs, I_F = 250 mA; CCT = 4200K.

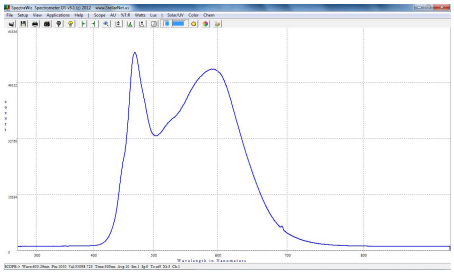

Fig. 7: Experimental spectral characteristics of used LED module CXA1816, forward current I_F = 450 mA and four blue XPE LEDs, I_F = 350 mA; CCT = 4400K.

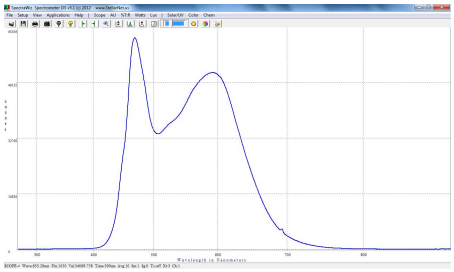

Fig. 8: Experimental spectral characteristics of used LED module CXA1816, forward current I_F = 450 mA and four blue XPE LEDs, I_F = 450 mA; CCT = 4600K.

B. Thermal management

Thermal resistance model, described in [1], is used – Fig. 9.

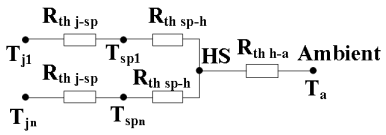

Fig. 9. Thermal resistance model [5-7].
Thermal resistances $R_{th\ j\text{-}sp}$ denotes from junction to solder point; $R_{th\ sp\text{-}h}$- thermal resistance from solder point to heat sink; $R_{th\ h\text{-}a}$- thermal resistance from heat sink to ambient; T_{j1}, T_{jn} and T_{sp1}, T_{spn} are junction and solder point temperatures corresponding.

Equation (1) is used for estimation LEDs' thermal loading [5, 6] and choice of the proper heat sink.

$$T_{jMAX}=T_{a\text{-}max}+(R_{thj\text{-}sp}+R_{thsp\text{-}h})*P_{LED}+R_{thh\text{-}a}*P_{tot} \quad (1)$$

where: $R_{th\ j\text{-}sp}$- thermal resistance from junction to solder point; $R_{th\ sp\text{-}h}$- thermal resistance from solder point to heat sink; $R_{th\ h\text{-}a}$- thermal resistance from heat sinks to ambient.

Some of electrical and thermal characteristics of used LEDs are presented below:

- Thermal resistance between junction and solder point Rth j-sp:
  for blue XPE LEDs Rth j-sp = 9°C/W;
  for red XPE LEDs Rth j-sp = 5°C/W [1].
- Forward voltage at rated current:
  U_F = 2.1V for red LEDs; U_F = 3.1V for blue LEDs; U_F = 3.3V for blue LEDs (ат 450 mA); for blue LEDs I_F – up to 1000 mA; for red LEDs I_F – up to 700 mA. [5, 6].

A proper thermal resistance of the heat sink can be evaluated using (1). P_{LED} is the power of one LED chip:

$$P_{LED} = I_F * U_F; \quad (2)$$

At maximum load of LEDs:
$P_{BLUE} = I_F * U_F = 0.45*3.3 = 1.49$ W for blue LED;
$P_{RED} = I_F * U_F = 0.35*2.2 = 0.77$ W for red LED;
$P_{CXA\_LED} = 0.45*36.4 = 16.38$ W.
Ptot is the power of all LEDs:

$$Ptot = P_{CXA\_LED} + 4P_{BLUE} = 22.34 \text{ W} \quad (3)$$

Estimations using equation (1) show that thermal resistance from heat sinks to ambient Rth h-a should be less than 1.1 °C/W (maximum ambient temperature Ta max = 45°C; TjMAX = 85°C). A heat sink with thermal resistance Rth h-a = 1°C/W is chosen.

All CXA family LEDs are rated for their nominal lumen output at a Tc of 85°C. Temperature change from this point inversely affects the lumen output of the CX family LED. In Fig.10 is shown place for measuring temperature Tc.

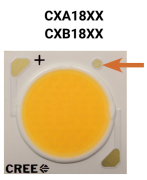

Fig. 10: Place for measuring T_C [5].

Experimental investigations of temperature distributions at different ambient conditions are made in thermal chamber by thermocuples and infrared camera FLIR 350. Some results are show below.

Experimental investigations of LEDs' thermal loading

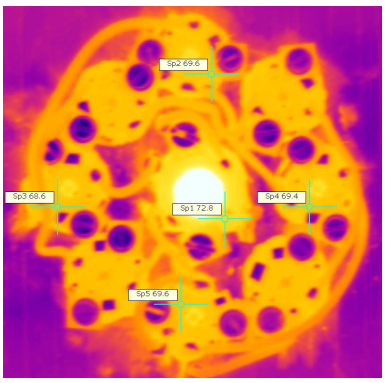

Fig. 11. Infrared photo: solder points' temperatures distributions: LED module CXA1816 and 4 XPE blue LEDs. Ambient temperature is 45ºC.

Temperature dependences of T_C for CXA LED and T_{SP} and T_J for blue LEDs are shown in Fig 12. As it can be seen thermal load of all LEDs is far enough away from danger zones which ensures safety operation and long life of lighting equipment.

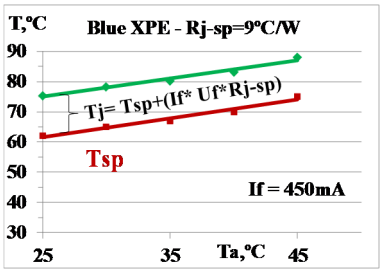

Fig.12. Blue LEDs solder point temperature T_{SP} (measured) and junction temperature T_J (calculated) dependences on ambient temperature T_a.

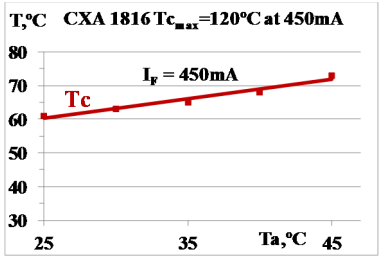

Fig.13. Case temperature T_C (for CXA LED - measured) dependences on ambient temperature T_a.

Night lighting of the dairy farm - requirements and features

The characteristics of lighting in barns at night are determined by the requirement that cows can sleep peacefully, and the staff can serve premises. Taking into account the specificities of cows' vision mentioned above, night lighting is realized by application of red LEDs XPE – CREE Inc. Spectral characteristics of the night light are shown in Fig. 14.

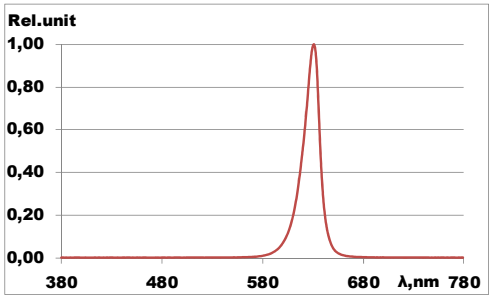

Fig.14. Spectral characteristics of the LED Module's night light.

In the realized LED module 6 red LEDs ensure illumination about 6 – 10 lx for two to four cows' housing, which is practically enough to enable staff to perform their duties.

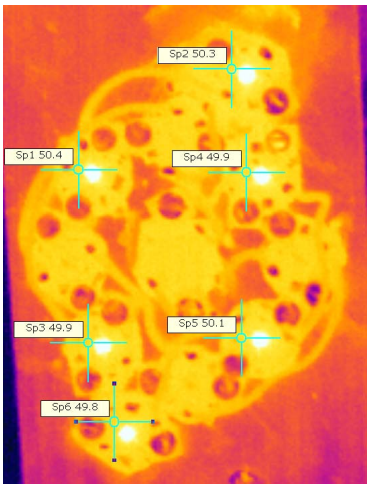

Fig.15. Infrared photo: red LEDs solder points' temperatures distributions: Ambient temperature is 35ºC.

As it is mentioned above – Fig.3, thermal management results are very important for proper operation of night lighting because of strong dependence of red LEDs luminous flux by junction temperature.

Total power of red LEDs in the developed LED module is about 5 W; the heat sink thermal resistance is $R_{th\ h\text{-}a} = 1°C/W$. Theoretical (eq.1) and experimental investigations of red LEDs thermal loading are made using infrared thermography and conventional measuring – by thermocouples. Some results are shown in Fig. 15 and Fig. 16.

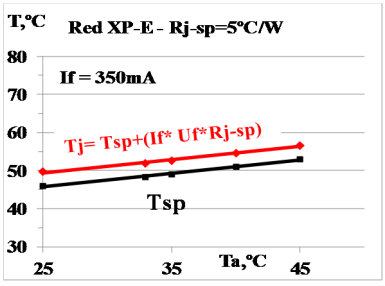

Fig.16. Red LEDs solder point temperature T_{SP} (measured) and junction temperature T_J (calculated) dependences on ambient temperature T_a.

As it can be seen from Fig.16, junction temperature T_J of red LEDs remains below 60ºC and relative luminous efficiency is over 80% (Fig.3) even under the most severe operating conditions. This is a precondition for reliable operation and long life of the developed lighting equipment.

V. Conclusion

LED module for illumination of dairy barns is designed and produced. Luminous flux' spectral power distribution of the designed luminaire for day and night illumination is very close to the optimal spectrum, recommended in literature.

Proper choice of LEDs ensures good energy efficiency of the luminaire and allows easy dimming.

Acknowledgement

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Comparative Study on Data Error Detection Techniques in Embedded Systems

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Abstract –**This paper presents a theoretical comparison of different existing data error detection techniques. The techniques are compared by fault coverage, memory overhead and performance overhead. For this comparison, ten different data error detection techniques are taken into account. In general, the best error detection technique always has the highest fault coverage with low performance and memory overhead. After performing the theoretical comparison, we conclude that GA (genetic algorithm) and SWIFT (software implemented fault tolerance) techniques are the best techniques for data error detection.**

Keywords – **data error detection, fault coverage, embedded systems, duplication**

I. INTRODUCTION

The usage of embedded systems in safety critical and general purpose applications is growing rapidly day by day. It is proved that decreasing the size of the features in circuits and increasing their complexity leads to a less reliable system [1]. Transient faults in embedded systems can cause strange behavior and degrade the data integrity and system reliability [2,3]. Transient faults occur due to electromagnetic interference, glitches and heavy radiation [4]. These external disturbances cause bit – flips into memory locations or CPU registers, also known as soft errors. This may affect the system during program execution. The effect can be either a data flow or a control flow error. Generally data flow errors lead to corruption of variables. Literature states that 33% to 77% of the transient faults are converted to control flow errors and remaining percentage of errors lead to the data flow errors [1,5,6]. Transient faults refer to faults that are no longer present if the system restarts. This paper focuses on different data flow error detection techniques, other work focuses on control flow error detection [7].

In order to improve system reliability, fault tolerance should be included in the system. This allows to detect an error and recover. However, fault tolerance needs redundancy: software or hardware redundancy [3]. Hardware redundancy is an expensive process cost wise, since it needs to include extra hardware in every device. Whereas software redundancy is about duplicating the instructions and data [3,8]. Mark that redundant software can cause memory overhead, extra execution time and more power consumption.

In order to choose the best technique, one must know which technique provides the best trade – off between detection ratio and overheads. Duplication mechanisms take counter measures on data flow errors. This paper describes and performs a theoretical comparison with different existing data error detection techniques. We compare the techniques on memory overhead, performance overhead and fault coverage. Most of the data error detection techniques are based on a duplication mechanism, either full duplication, critical block duplication or critical path duplication [2,5,8,9]. Full duplication methods cover more faults but their drawback is that they impose an overhead of about 255% to the system [10]. To make a better trade-off between the reliability and overheads in the software based techniques, selective duplication methods such as [5,9] are introduced.

In this paper ten different data error detection techniques are taken into account for theoretical comparison and analysis of each technique with other techniques based upon three different parameters: fault detection, performance overhead and memory overhead [2,5,8,9,11–13]. It is obvious that some techniques have more fault coverage with more overheads and other techniques have less overheads with reduction in fault coverage. Comparison and analysis will be performed in Section 3. The ideal technique has a high fault coverage with minor overhead.

The rest of the paper is organized as follows. Section 2 describes the different data error detection techniques. Section 3 presents a theoretical comparison of different data error detection techniques. Section 4 provides future work plans and Section 5 concludes this paper.

II. DATA ERROR DETECTION TECHNIQUES

This Section presents various existing data error detection techniques and explains each techniques procedure in a few sentences. All of the presented data error detection techniques are software based. Their represented results will be compared in Section 3.

A. Error detection by critical block duplication

This technique is named CBD (critical block duplication). It particularly focuses on the detection of data errors during the normal system operation [5]. The authors of the proposed CBD technique also proposed a simple way for critical block detection. A block that has the most number of fan outs in the CFG (control flow graph) is considered as a critical block. It has the greatest number of connections with the other blocks in CFG [1,5]. By finding

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the critical block and duplicating it, low performance and memory overhead, but high fault coverage can be achieved. The critical block will be duplicated and compared to the original block. If any mismatch occurs, an error has occurred. It will be reported and the program will halt.

B. *Error detection by critical path duplication*

This technique is named CPD (critical path duplication) and can be used to detect data flow errors. In this method the DFG (data flow graph) is used instead of the CFG. In the proposed CPD, nodes represent the operands and vertices represent the variables of the program [9]. The main intention of this method is to duplicate the critical path. First step is to find the critical path and then duplicate it. The authors of [9,14] who proposed the CPD method also proposed a simple way for critical path detection. The longest path in the DFG is considered as a critical path because of the great possibility of error occurrence on that long path. Then the critical path will be duplicated and comparison instructions will be placed after each write operation in the final variables. If the final variables are not equal to each other, an error will be reported. The authors also estimate the performance overhead, memory overhead and fault coverage.

C. *Error detection by diverse data and duplicated instructions*

To detect both transient and permanent errors, ED^{4}I has been proposed. Error Detection by Diverse Data and Duplicated Instructions is a SIHFT (software implemented hardware fault tolerance) based technique and does not need any hardware modifications. This makes ED^{4}I a good alternative for hardware fault tolerance. ED^{4}I detects both transient and permanent errors by executing two different programs (original program and its replica) and comparing their results. The transformation of ED^{4}I representation is $\boldsymbol{x' = k.x}$ for integer numbers, where k is the fault detection probability and data integrity of the program, $\boldsymbol{x}$ is the original program and $\boldsymbol{x'}$ is the transformed program [2]. This technique will be calculated the optimum value for k which can maximize the fault detection probability under the condition that data integrity is high.

D. *Error detection by duplicated instructions*

EDDI (error detection by duplicated instructions) is a full duplication technique like ED^{4}I and detects data errors during the system operation. Unlike the other error detection techniques that use the hardware, EDDI does not need any hardware modifications in the system to add the error detection capability to the original program [8]. EDDI contains three different instructions for execution: a master instruction, a shadow instruction and a comparison instruction [8]. The master instruction is the original instruction of the source code, while the shadow instruction is the duplicated instruction added to the source code. A requirement is that registers and memory for master instructions should always have the same values as the registers and memory of shadow instructions, comparison for this can be done with a comparison instruction. If there is any mismatch between the master and shadow instructions, the comparison instruction invokes an error handler. EDDI duplicates the instructions in the assembly source code to achieve error detection capability [8,13]. There is an alternative way that might be duplicating the instructions in high level language.

E. *Soft error detection using software redundancy*

The technique that proposes detection of soft errors using software redundancy is named SEDSR. In the proposed technique the critical block is duplicated at compile-time. As in [1,5] the critical block is the block with the most fan outs. At this time, critical block variables are divided into two categories: (1) middle variables: important in computing the other variables and (2) final variables: they don't perform any computations [1]. In the critical block a redundant instruction is placed after the final variables to compare these variables in original and duplicated blocks. If any mismatch between these variables during comparison, an error will be reported. The EF (Evaluation Factor) is introduced in this paper which considers performance and memory overhead, fault coverage simultaneously.

F. *Detecting soft errors by a purely software approach*

The error detection mechanism in the proposed technique is mainly based on set of transformation rules. The rules are classified in three basic groups, (1) error affecting data, (2) error affecting basic instructions and (3) error affecting control instructions [15] to detect the errors. This technique is also a full duplication technique as in [2,8] it also duplicates the original program for the transformation rules. Since it is duplicating the entire program, this method may have more performance and memory overhead but the positive side is better fault coverage. By applying the different transformation rules, this technique is able to detect errors that occur in data, basic instructions and control instructions.

G. *Shoestring : Probabilistic soft error reliability*

This technique mainly focuses on the soft error detection to make the system as reliable as possible by detecting the faults [11,12]. Any instruction that can potentially impact global memory is considered a high value instruction. If it consumes a corrupted input, they are likely to produce outputs that result in user visible program corruption [10]. The main contributions of this technique are: (1) a transparent software solution for addressing soft errors, (2) a new reliability aware compiler analysis and (3) a selective instruction duplication: the code duplication begins by selecting a single high value instruction, from the set of all high value instructions. Since high value instructions are likely to have more impact on program output, the selected single high value instruction then proceeds to duplicate all instructions that produces values for single high value instructions [10]. The duplication is terminated when no more producers exist or the producer is already duplicated. Then comparison instructions are inserted for checking the errors. This technique focuses on possible ways to make shoestring

code duplication for error detection. The reader is encouraged to refer the prior work for detailed description [10].

H. Software implemented fault tolerance

Error detection technique to prevent systems from soft errors is SWIFT (software implemented fault tolerance). Advantage of SWIFT is that, it can provide high level protection and performance with high level control flow checking mechanism [6,13]. SWIFT is a compiler based transformation which duplicates instructions in a program and also inserts the comparison instructions during code generation. During the program execution, values are computed twice and compared for the mismatch before any differences due to transient faults can affect the output of the program [11]. The proposed technique provides some improvements prior to the result are: no hardware required, reduced performance overhead by eliminating branch validation code, dealings with exception and interrupt handling [13]. SWIFT techniques mainly focuses on both fault coverage and overheads.

I. Overhead reduction in data- flow software based fault tolerance techniques

This technique provides a different implementation alternative of software based techniques. The alternative overcomes the drawback of the massive overhead introduced by other techniques, while keeping the reliability. A set of rules for the data protection is presented such as, (1) global rules: each register used in the program should have its replica, (2) duplication rules: (a) duplicating all instructions except branches, (b) duplicating all instructions except branches and stores and (3) checking rules: to compare the values of a register with its replica at different positions [12]. By applying these rules to various techniques presented in [12] we can detect the errors. Focus of this technique mainly is on overhead with stable reliability.

J. Method for hardening a program against soft error using genetic algorithm

As we know that quite often system failures occur due to soft errors. A software based technique proposed here to tolerate these soft errors, is selective replication, which identifies the most unsafe blocks of the program by using a method called GA (genetic algorithm) [10]. Proposed technique mainly follows three different steps to fulfill the purpose. Those are (1) preprocessing: This step include a method called program slicing [16] to eliminate the irrelevant and ineffective instructions of a program to reduce the size of the program, (2) identifying the unsafe blocks: GA is proposed, which takes source code of the program as a input to find out the smallest subset of the basic blocks which are more vulnerable, have the highest impact on the program and (3) strengthening the identified unsafe blocks: based on the required level of reliability, a small number of most vulnerable basic blocks are strengthened against errors [10].

III. THEORETICAL COMPARISON

This theoretical comparative study will allow to decide which data error detection technique is best, according to their trade - off between the fault coverage and overheads, since each technique is presuming the best. In Section 2, we described different data error detection techniques and their procedures to check for fault coverage. In this Section, a theoretical comparison for all of the above mentioned techniques has been performed. Our theoretical comparison is based on the numbers provided in the literature of the discussed data flow error detection techniques. The authors of the corresponding literature have presented these values by performing fault injection experiments for different case studies [2,3,5,8–13,15]. Most of the techniques for error detection use common case studies such as: matrix multiplication, quick sort and bubble sort.

The main aim of this paper is to compare the different existing data error detection techniques and their results to analyze which technique is performing better than other techniques based upon the fault detection capabilities and overheads for safety critical applications. The EF is defined in this Section, which considers fault coverage, memory and performance overhead simultaneously [1]. The technique which has a higher EF is a better technique because it considers the trade – off between the various parameters.

Table 1: FAULT COVERAGE, MEMORY AND PERFORMANCE OVERHEADS OF DIFFERENT DATA ERROR DETECTION TECHNIQUES

S.no	Technique	Avg. Fault coverage	Avg. Performance overhead	Avg. Memory overhead	EF
A	CBD	70%	41%	63%	2.71
B	CPD	73.32%	48%	75%	2.03
C	ED^{4}I	96%	110%	130%	0.67
D	EDDI	98.7%	100%	125%	0.78
E	SEDSR	96.3%	68%	78%	2.14
F	Software approach	99%	200%	250%	0.198
G	Shoestring	82%	35%	70%	3.34
H	SWIFT	88%	41%	50%	4.40
I	Checking rules	95%	74%	82%	1.56
J	GA	82%	24%	50%	6.83

$$Evaluation\ Factor = \frac{Fault\ coverage}{Memory\ Overhead \times Performance\ overhead}$$

In embedded systems the major concern is to detect as many errors as possible without consuming more processing time, particularly for safety critical applications. In Table 1, the second column contains all of the existing data error detection techniques. Third, fourth and fifth columns contain average of fault coverage, average of performance overhead and average of memory overhead obtained from execution of different case study programs. Sixth column presents calculated EF of the presented techniques

From the comparative study analysis presented in Table 1, EDDI and software approach techniques showed a very good fault coverage with a higher performance and memory overhead. Other techniques: Shoestring, CBD and CPD showed less performance and memory overhead but fault coverage is reduced. It is very important to keep in mind that, for safety critical applications in embedded systems, we need to have best fault coverage with less performance and memory overhead. In this comparative study from Table 1, GA and SWIFT techniques are the best techniques for both fault coverage and overheads compared to the other data error detection techniques.

From Table 1, we can see most of the techniques are having either best fault coverage or low overheads. Only a couple of techniques, GA and SWIFT are having best trade – off between the fault coverage and overheads.

IV. FUTURE WORK

To compare the listed techniques theoretically, we used fault coverage and overheads numbers provided in literature. However, not all techniques were validated with the same case studies or fault injection process.

Therefore, we will perform our own validation experiments. This will allow us to implement the techniques for the same case studies and inject faults with the same injection process. This will allow us to make a better comparison between the techniques.

V. CONCLUSION

This paper listen different data error detection techniques and performs a theoretical comparison based upon their fault coverage, memory and performance overhead. From the theoretical comparison we have seen from Table 1, EDDI and Software approach techniques are having best fault coverage but with more overheads, GA and SWIFT techniques are having good fault coverage with low overheads. We conclude that, GA and SWIFT techniques are the best data error detection techniques among the other data error detection techniques for the general purpose, real time and safety critical applications of embedded systems.

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Inter-block Jump Detection Techniques: a study

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Abstract – **This paper presents a study of inter-block jump detection techniques. The CFCSS, RSCFC, SEDSR, SCFC, ECCA, YACCA and SIED techniques were considered. The conducted experiments measure criteria such as detection ratio, run-time and code-size overhead. Next, those criteria are combined and evaluated to determine the best technique. Finally, our results reveal that CFCSS makes the best trade-off between fault detection and overhead for the implemented case studies.**

Keywords – **Embedded Systems, Fault Tolerance, Control Flow Errors.**

I. Introduction

Embedded systems today are becoming more vulnerable to external disturbances. Examples of external disturbances are high-energy neutrons [1], electromagnetic interference [2] or temperature fluctuations [3].

The external disturbances introduce erroneous bit-flips into the memory locations of embedded systems. The erroneous bit-flips can have varying effects on the system. If the bit-flip occurs in a memory mapped I/O register, it could illegally drive an actuator. For some applications, this could create vary dangerous situations. If the bit-flip occurs in a memory location or a CPU register, the software in execution could be affected. The effect is either a data flow error or a control flow error. A data flow error corrupts input, output or intermediate values. A control flow error disrupts the execution order of instructions.

While these effects on the system might be acceptable for non-critical systems such as infotainment systems, they are unacceptable for safety critical systems. To protect embedded systems against erroneous bit-flips and their effect, fault tolerance measures have to be implemented. Fault tolerance measures can be implemented in hardware, such as Triple Modular Redundancy [4] or ECC [5]. Although effective, hardware implemented fault tolerance measures do require extra hardware to be implemented for every device. This requirement makes these measures expensive.

To overcome that drawback, fault tolerance measures can be implemented in software [6]. Examples are Duplication [7] and Signature Monitoring [8].

In this paper, we will conduct a comparative study of seven different existing Signature Monitoring techniques. More techniques are still being developed in active research such as [9]. This study will allow us to decide which technique is the best to use based on a number of case studies we implemented. The study will compare the techniques on criteria such as detection ratio, run-time overhead and code-size overhead.

The rest of the paper is organized as follows. Section 2 introduces the concept of Signature Monitoring. The experiment results are presented in Section 3. Section 4 discusses the results. Finally, future work is presented in Section 5 and conclusions are drawn in Section 6.

II. Signature Monitoring

Signature Monitoring is a software implemented fault tolerance technique to detect control flow errors. A control flow error corrupts the execution order of instructions. A possible effect is an illegal jump to a random location in the code memory.

In other words, a control flow error can be thought of as an error against the control flow graph of the program. The control flow graph (CFG) of a program is a representation of the program divided into basic blocks and legal edges, as shown in Fig. 1. Basic blocks consist out of a consecutive list of instructions, without branch-in or branch-out instructions. Of course, only the first or last instruction of a basic block can be a branch-in or branch-out instruction. The edges of the CFG represent the legal paths between such basic blocks.

A control flow error can corrupt the execution order of instructions in three ways:

a. Intra-block jump: an illegal jump that originates from and lands in the same basic block.
b. Inter-block jump: an illegal jump that originates in one basic block and lands in another.
c. Outside jump: an illegal jump that jumps outside the code region.

Each jump has its own detection technique.

An intra-block jump is detected by an instruction counter. First, at the beginning of a basic block, the counter is

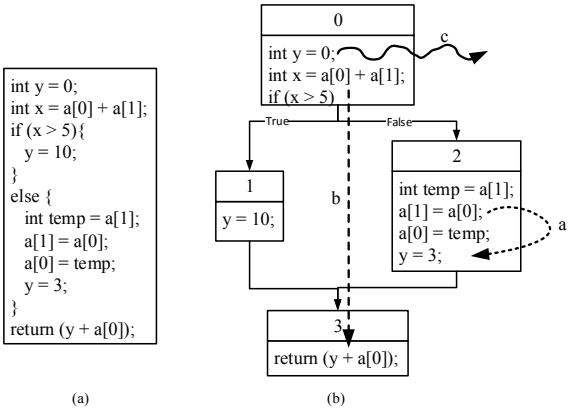

Fig. 1. A control flow graph with the tree possible control flow errors.

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initialized to hold the number of instructions to be executed in the basic block. For example, if in the current basic block 3 instructions must be executed, the counter will be initialized to hold the value 3. Next the counter is decremented after each executed instruction. Finally, at the end of the basic block, it is verified that the counter has reached 0. The 0 indicates exactly the right amount of instructions have been executed.

An outside jump is detected by filling up the unused code memory. The unused memory can either be filled with *no operation* or NOP instructions or with jumps to a fault handler.

In this paper, we focus on Signature Monitoring techniques which take counter measures against inter-block jumps. Signature Monitoring detects an inter-block jump by adding a signature, a variable, to each basic block at compile-time. Next, instructions are inserted into the program to recalculate the signature at run-time. The run-time signature is compared to the compile-time signature. If these signatures are not equal, a control flow error occurred.

There exist different ways to calculate the signature. For instance the location of the basic block in the CFG can be used to calculate the signature. Other parameters to calculate the CFG could be the legal incoming branches or the legal outgoing branches. Due to this wide variety of possibilities, a lot of Signature Monitoring techniques exist, each claiming to be the best. For the study in this paper, we selected seven techniques to compare with one another. The selected techniques are CFCSS [8], RSCFC [10], SEDSR [11], SCFC [12], ECCA [13], YACCA [14] and SIED [15]. These techniques were selected because these were the ones we knew of at the start of the study.

Some of the selected techniques can offer protection against data flow errors or intra-block jumps. To be able to really compare the techniques with one another, only the Signature Monitoring part of the techniques will be implemented and tested.

III. EXPERIMENTS

A. Case studies

We selected four case studies to implement and test the selected techniques. We selected the same case studies as the ones used to validate the Signature Monitoring techniques in the corresponding literature [8-15]. The case studies are (1) an implementation of the bubble sort algorithm (255 elements), (2) an implementation of the quick sort algorithm (255 elements), (3) an implementation of the matrix multiplication algorithm (10*10 elements) and (4) the bit count algorithm of the automotive section of the MiBench [16] suite.

The techniques are inserted in the implementation of the case studies in Assembler using our GCC plugin. Since the techniques highly-depend on the correct CFG, they must be implemented in Assembler. They simply have no effect when implemented in C++. More information about this topic can be found in [17].

B. Hardware

The case studies were executed on a NXP LPC1768, an ARM Cortex-M3 driven microcontroller executing at 96 MHz. It includes 512 kB FLASH, 32 kB RAM with interfaces for different communications busses, such as Ethernet, CAN, I2C and SPI. This microcontroller was chosen because the ARM Cortex-M3 is an industry-leading 32-bit processor used in many different domains.

C. Results

Per case study, the techniques were submitted to 2000 inter-block jump control flow errors. Table I presents the measured detection ratio of each technique. The detection ratio is calculated using formula 1. To get the correct detection ratio, we discard the faults that had no effect on the outcome of the program. Typically such faults are errone-

TABLE I. DETECTION RATIO PER CASE STUDY (IN %)

Case study	CFCSS	RSCFC	SEDSR	SCFC	ECCA	YACCA	SIED
Bubble sort	88.3	52.5	67.3	70.8	99.9	99.6	67.4
Quick sort	98.2	80.3	63.8	85.2	86.9	97.1	72.3
Matrix multiplication	90.2	32.2	36.4	64.5	73.8	92.2	50.2
Bit count	56.9	34.4	45.0	36.3	52.5	64.4	36.8

TABLE II. RUN-TIME OVERHEAD PER CASE STUDY (IN %)

Case study	CFCSS	RSCFC	SEDSR	SCFC	ECCA	YACCA	SIED
Bubble sort	60.3	60.4	60.0	110.0	241.0	201.2	70.3
Quick sort	129.6	182.4	115.6	203.2	433.5	353.6	143.5
Matrix multiplication	60.0	60.4	44.8	95.0	209.1	179.0	61.2
Bit count	154.7	159.4	128.1	215.6	440.6	370.3	165.6

TABLE III. CODE-SIZE OVERHEAD PER CASE STUDY (IN %)

Case study	CFCSS	RSCFC	SEDSR	SCFC	ECCA	YACCA	SIED
Bubble sort	6.8	7.1	5.5	10.2	18.2	15.0	6.6
Quick sort	20.5	26.9	18.5	31.7	48.7	39.4	20.3
Matrix multiplication	15.8	19.9	13.8	24.9	41.6	33.7	17.6
Bit count	8.7	10.4	8.3	13.5	24.3	19.8	9.7

ous jumps over code that was not to be executed or erroneous jumps that re-executes a compare statement which result in the same outcome. What constitutes as a fault without effect is dependent on the algorithm.

$$detection\_ratio = \frac{\#signature\_monitoring\_detected}{2000 - \#no\_effect\_faults} \quad (1)$$

In reality, the actual illegal inter-block jump detection ratio can even be higher than the numbers presented in Table I. Mark that we did not consider the faults that were detected by a processor fault handler. The Cortex-M3 has internal fault handlers that are able to detect specific hardware faults, such as improper bus usage. Injected faults that were detected by such a mechanism are not part of Table I. The table shows the number of malicious faults detected by Signature Monitoring only.

Note that no technique reaches a 100% detection rate, although some techniques, such as ECCA, YACCA and CFCSS come close for some case studies. A detection ratio of 100% is impossible for Signature Monitoring. Erroneous jumps such as premature exits out of the algorithm are undetectable for Signature Monitoring.

Erroneous bit-flip detection does not come cheap. Each technique introduces both run-time and code-size overhead. Run-time overhead expresses how much longer the algorithm takes to execute. Code-size overhead expresses how much more memory the compiled code needs. Table II and Table III present the overhead costs per technique per case study.

IV. Discussion

If only the detection ratio is considered, then Table I shows that YACCA is the best technique for most case studies. However, based on the detection ratio, the techniques can be divided into two groups. On the one hand CFCSS, ECCA and YACCA which have an average detection ratio of 83% and on the other hand the rest of the techniques which have an average detection ratio of 56%. The difference in the detection ratio can be traced back to the way the techniques update the signature. CFCSS, ECCA and YACCA update the signature incrementally. This leads to a high detection ratio. Once an increment is skipped, the signature cannot hold the correct value. The next validation instruction will detect the incorrect value and report a control flow error.

The other techniques update the signature locally, with a *move* instruction. This leaves room for undetected control flow errors. If an illegal jump skips the validation instruction, but lands before the update instruction, the control flow error will remain undetected. Once the update instruction has been executed, the signature will have the correct value and the illegal jump is masked. This process is presented by Fig. 2.

However, for many embedded applications there are run-time and/or code-size restrictions. To determine if a detection technique is good or usable, both the run-time and code-size overhead introduced by that technique should be considered. SEDSR has the lowest overhead for both criteria, as shown in Table II and III.

Code-size overhead is determined by how many extra assembly instructions there are inserted per basic block. For CFCSS, RSCFC, SEDSR, SCFC and SIED an average of 6 instructions are inserted per basic block. However, YACCA inserts 12 extra instructions and ECCA 14 per basic block. This explains the numbers of Table III.

Run-time overhead is not only determined by the number of extra assembly instructions. It is also determined by the type of the extra instructions. CFCSS, RSCFC, SEDSR, SCFC and SIED only insert instructions that need 1 clock cycle to execute. To implement ECCA and YACCA however, two unsigned divisions must be performed per basic block. Although the Cortex-M3 has a hardware divisor and an UDIV instruction, it can take up to 12 clock cycles to perform the division [18]. This is the main reason for the large run-time overhead generated by ECCA and YACCA.

To really compare the techniques to each other, we use the Evaluation Factor (EF) described by [11]. The EF is calculated using formula 2. The overheads used in formula 2 are relative overheads. The results are given in Table IV. The higher the EF, the better the technique.

$$EF = \frac{detection\ ratio}{run\_time\_overhead \times code\_size\_overhead} \quad (2)$$

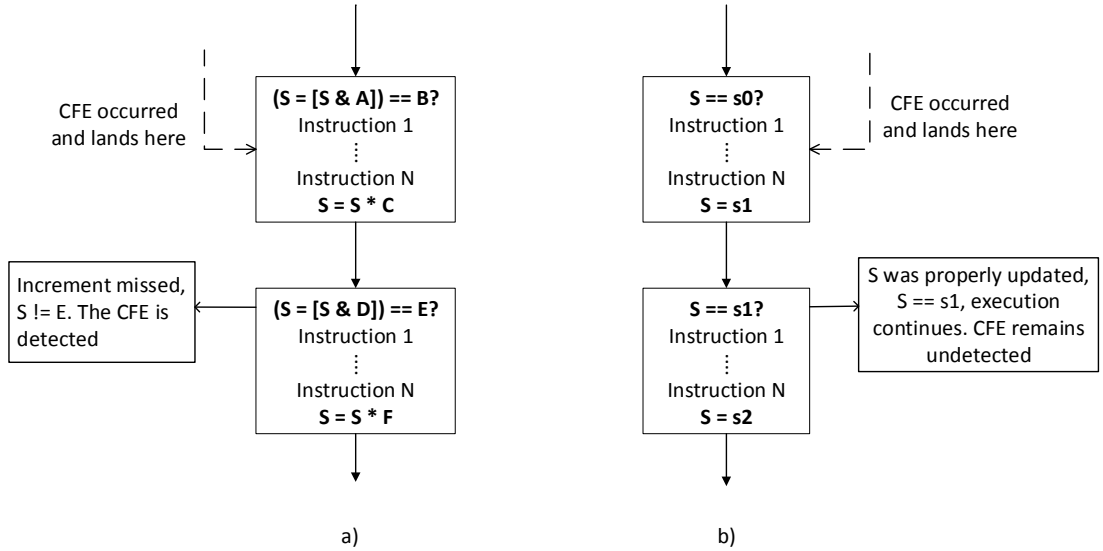

Fig. 2. The difference between incremental signature update (a) and local signature update (b).

TABLE IV. EVALUATION FACTOR PER CASE STUDY

Case study	CFCSS	RSCFC	SEDSR	SCFC	ECCA	YACCA	SIED
Bubble sort	51.6	30.6	39.9	30.6	24.8	28.8	37.1
Quick sort	35.5	22.4	25.0	21.3	11.0	15.4	24.7
Matrix multi-plication	48.7	16.7	22.1	26.5	16.9	24.7	26.5
Bit count	20.6	12.0	18.2	10.1	7.8	11.4	12.6

Regarding the Evaluation Factor, Table IV shows CFCSS is the best overall technique for all case studies, not YACCA or SEDSR. This means that CFCSS makes the best trade-off between detection ratio and overhead. The next best techniques are SEDSR and SIED. Both SEDSR and SIED have a medium to low detection ratio in most case studies. They do however have a very low overhead, both run-time and code-size. This results in a good trade-off between detection ratio and overhead, leading to a good EF.

V. FUTURE WORK

During the study, new Signature Monitoring techniques were developed, such as [9,19]. By using the selective implementation principle, the new techniques claim to have the same or a better detection ratio, with a lot less overhead. We will perform the same experiments with these new techniques and compare the results to the results of this paper. If the selective approach does indeed maintain the detection ratio, we will apply it to the seven selected techniques of this paper and rerun the experiments.

VI. CONCLUSION

This paper selected a number of Signature Monitoring techniques and determined the best technique for a number of representative case studies. We performed experiments for seven selected techniques. The selected techniques were CFCSS, RSCFC, SEDSR, SCFC, ECCA, YACCA and SIED. The experiments measured three criteria, namely detection ratio, run-time overhead and code-size overhead. The three criteria were then combined into the evaluation factor. The evaluation factor enabled us to compare the techniques with each other. The result of the study was that CFCSS is the best overall technique. If overhead was of no concern for the application or the embedded system, than YACCA would be the best technique. YACCA detected the most inter-block jump control flow errors for most case studies.

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Programmable Setup for Peltier Element Control with Fine Smooth Regulation of the Temperature about Testing of Semiconductor Structures

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Abstract – **This article presents the design of non-standard equipment for obtaining experimental data about defects in thin film semiconductor structures. The idea of using low-powered Peltier element programmed to cause small temperature changes in semiconductor structures is scanning of the energy bandgap and thermal stimulation of the trapped charge carriers for defects analysis. Block diagram, control algorithm and PCB layout of the testing stand are given. Samples consisting of organic semiconductor and aluminum electrodes are examined for demonstration of the device working capacity. Energy distribution and concentration of the existing defects are determined.**

Keywords – **Peltier element control, testing of semiconductor structures, smooth adjustment of the temperature, defects analysis.**

I. Introduction

In the last years thin film electronics have been of great interest for its low power consumption, portability and low-cost manufacturing, which make it promising for many micro- and nanoelectronic applications, such as sensors, optoelectronic devices, energy harvesters, etc [1,2]. For these applications fluent charge carrier transport in the film is required for high device efficiency. Variety of defects arises in the films according to the deposition method, such as damaged bonds (dangling bonds) and/or impurities. They capture the charge carriers and prevent their contribution to the conduction process in the device, resulting in low conversion efficiency. The information about the traps' energy level in the band gap of the functional material is important for their identification and for optimization of the deposition conditions [3]. A popular technique for trap energy determination is thermally stimulated luminescence (TSL) [4], but it can be used only for light-emitting materials. Another method, giving information for the traps is photo-induced absorption [5], but the absorption spectrum is related only to the degree of traps filling, but not to their energy state. Space charge limited current method (SCLC) has been developed [6], where information from the slope of current-voltage characteristic can be extracted, but it works at preliminary assumption about the type and distribution of the traps, which is unknown in most of the cases. Pulse transient method has been developed for detrapping of charge carriers from all trap levels at the same time by linear rising temperature applied to the sample [7]. Such approach also seems to be inapplicable for exact energy position of the traps. However, filling the traps at temperatures lower than the room temperature, followed by their controllable releasing with multiple cycles of step temperature increasing, will make possible determination of the traps concentration and energy distribution in the same time. This modification of the linear heating method is useful for defect analysis in organic and inorganic films applied in any kind of micro- or nanoelectronic device. The setup, necessary for realization of this method is not standard and should be especially designed in the meaning of temperature range, frequency and magnitude of the step intervals, and precision of temperature maintaining, according to the deposition methods and the nature of the films implemented in the semiconductor device.

Usually the required control devices serve to provide the necessary parameters and output signals to a single component or group of components, performing any function or manipulating certain environmental parameters. In the most general case, a control unit may include a power supply unit, a computing unit (CPU), a block indication (light, alphanumeric or graphic), block data input device, input-output unit (combining all input or output connections), executive power block, feedback (to set output parameter or input), filters and other blocks [9-11].

This article aims to present a control device, applicable in microelectronics research behavior of specific semiconductor structures, changing the ambient temperature over an extended temperature range. The device controls Peltier element with temperature feedback and information about defects in thin semiconductor films is extracted based on multiple cooling-heating cycles. To demonstrate the device potential, organic optoelectronic samples are tested for traps identification at minimum temperature of 10 ^{o}C, maximum temperature of 45 ^{o}C and precision of the temperature control of +/- 0.5^{o}C.

II. Design of the Control Device for Peltier Element

Regarding the reasons, mentioned above, Peltier element was chosen to control the temperature in the semiconductor testing chamber. When changing the magnitude of the current flowing through the Peltier, its

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temperature is changing. Respectively, when changing the current direction, the direction of the heat transfer is also changed. The selected Peltier element model is TEC1-12726 [8]. This thermoelectric module covers the temperature range, needed for the semiconductor defects investigation, it has dimensions - 50x50x3.3 mm, Umax - 15.4V, Imax - 26A, $\Delta T_{max} \geq 66\ ^{o}C$.

Another reason to use Peltier element is the ability for fine temperature control by the operator through generation of appropriate electrical signals, because in this way the negative effect of condensation on the test sample is eliminated. According to this, a specific control device was developed and its functional block diagram is shown in figure 1.

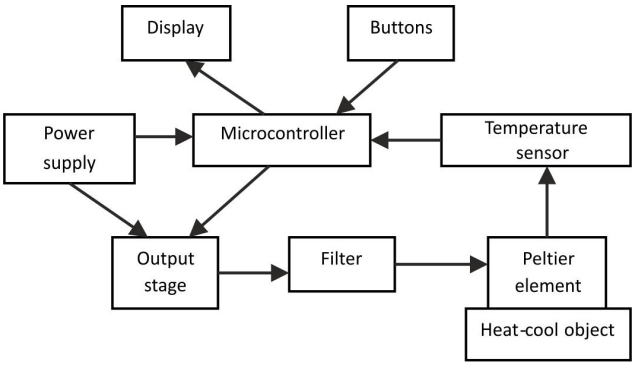

Fig. 1. Block diagram of the designed equipment

Briefly, the selected operating principle is as follows: As mentioned temperature variation on the surface of the Peltier element in its mounting to a suitable heat sink is a function of the magnitude of the current flowing through it. If the voltage is adjusted accordingly changes the current through elements. Since the voltage regulation can be implemented more easily, so it is elected this approach. This function is performed by adjusting duty cycle of a pulse signal with a frequency of 10 kHz from 0 to 100% in two steps, click on the corresponding 1% and 5% (fine and coarse). Since Peltier elements can not work with a pulse signal, for this purpose, take the average of the received pulse signal after output of LC filter.

According to the block diagram presented in figure 1, the purpose of each of the blocks and their structure is as follows:

1. Power Supply - its function is to produce two output voltages. The first one is + 5V upright and stabilized, and the other one is + 12V, only standing power output stage.

2. Microcontroller – the selected microprocessor is PIC18F4550. It has 8 bit RISC microprocessor architecture. According to the chosen principle of management by pulse width modulation, the resulting requirement is to have a microcontroller hardware realized PWM output. The selected microcontroller has two such outputs [12].

3. Output Stage – the part of circuit, which represents a driver stage amplified current PWM signal, generated by the microcontroller.

4. Filter - the idea of this unit is to smooth the output PWM signal by removing its average value.

Figure 2 represents the wiring diagram of the output stage and the filter. Since the output of the microcontroller does not have the load-bearing capacity to be able to manage voltage, MOSFET transistor is put instep boosting current (realized by Q2). The larger is the current unclog the final transistor faster recharging becomes junction its capacities and thus improve key operation.

The relay scheme is used for reversing the polarity of the voltage to the Peltier element, which is a condition to change the direction of heat transfer. The relay switches when the temperature, set by the operator, changes its sign versus the value of the current temperature.

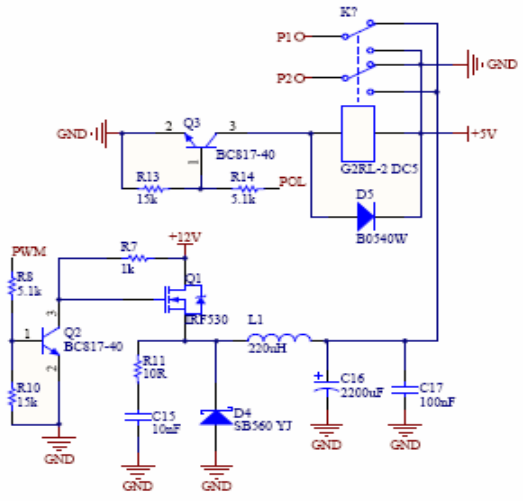

Fig. 2. Output stage and filter

5. Temperature sensor – this is the implemented sensor in the device, which gives the feedback between output and input. The temperature, set by the operator, is achieved by full-time tracking at any time by the CPU on the current Peltier elements while reaching and triggering algorithm and maintenance. The selected sensor DS1820 has an accuracy of 0.5% and temperature range (in degrees) from - 55 to + 125 °C. Its management is serial interface 1-wire, which is a characteristic that has good noise immunity within a few meters away. Since this sensor is exported outside of the control device box and mounted directly on the Peltier elements (sample), an important condition is to be noise resistant. Another characteristic of the DS1820 is his relative inertia, but for the required purposes, this is not critical.

6. Display – the operator will see on this block the current value of Peltier element temperature and a rear value that must be achieved / maintained. The chosen LCD is standard alphanumeric, rippling 16x2. Its management is in four bit interface in order to save wires between the processor and display.

7. Buttons - they are two and serve to increment or decrement of the temperature set. While simultaneously pressing them both, the current step could be changed in rough or fine.

8. Peltier elements – the so called managed object. 18W is selected at an operating voltage up to 11V.

III. PCB LAYOUT AND MANAGEMENT PROCEDURES

The developed printed circuit board, shown in figure 3, includes all the blocks of the functional diagram, presented in figure 1, with exception of the power transformer from the power supply unit and the managed object (Peltier element). They are connected to the circuit board by wires with a suitable cross-section. The Peltier element is located outside the control box model, installed on a suitable heat sink and on the free hand side of the test sample.

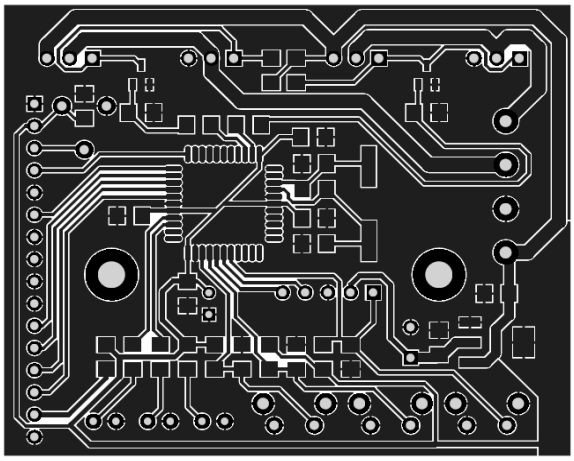

Fig. 3. PCB layout – top layer

The display is also located outside and is attached to the board by a ribbon cable and rack. The PCB is designed as one-sided layer board, but contains elements, combining the surface-mount and through-hole assembly. The selected carrier is FR4 laminate one-sided foil with a 35µm thickness of the copper foil.

The control algorithm, presented in figure 4, reflects the basic setup operations, carried out by the microcontroller. The specific condition of the microcontroller's logical operation here is to reach the average temperature target setup, and not the set temperature itself. Thus is accelerated the rapid stabilization of the demanded degrees on the Peltier device, as there is limited volatility over the necessary degrees. The reason here is the inertia of the device.

The following lines represent the specific base fragment of the software, associated with the extraction of the average temperature if necessary (if the current is aligned with the average). The controller then finds the difference between the two and determines how frequently to change the occupancy of the PWM signal. The value of the filling is from -100 to +100 by changing with step 1 in seconds, so as the difference between the two temperatures, with a minimum of 2 sec., and 20 sec. maximum.

```
 //if current temp meets the current mid desired
//then recalculate mid desired
if (currentTemp==midDesiredTemp)
   midDesiredTemp = calcMidTemp(currentTemp,
desiredTemp);
diff=abs(midDesiredTemp – currentTemp);
diff=20-diff;
if (diff<2)
   diff=2;
//timer for pwm control
uac_timer++;
// increment or decrement duty cycle
//if timer exceeds the required value
if (uac_timer >TICK_SECOND*diff)
{
   if (currentTemp<midDesiredTemp)
      pwmVal++;
   else if (currentTemp>midDesiredTemp)
      pwmVal--;
   timer=0;
   if (pwmVal<-100)
      pwmVal=-100;
if (pwmVal>100)
      pwmVal=100;
   update=TRUE;
      }
```

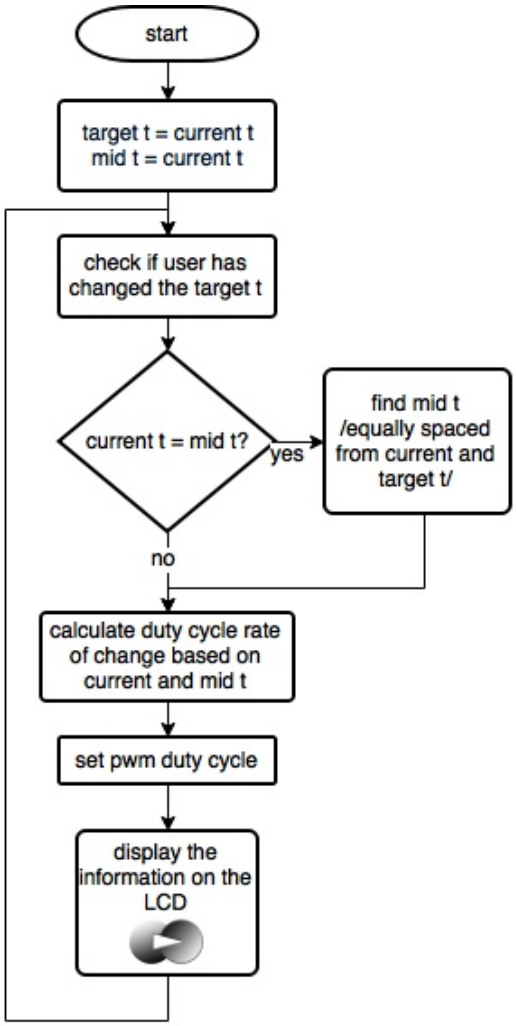

Fig. 4. Control algorithm for heating-cooling cycles generation.

The rest of the software of the microcontroller includes an initialization of the driver for use with LCD and control logic buttons.

IV. Experimental results

In this section data about temperature dependence of the thermally stimulated current and the traps energy distribution of spray deposited polyphenilene vinylene (PPV) based electroluminescent device are given (Fig. 5 and Fig. 6). The measurement procedure is as follows: first the sample is cooled down to 10°C (but not lower to avoid low temperature damage in the organic semiconductor). Suitable turn-on voltage is supplied for current flow formation. In the case of PPV/aluminum junction it is 3.8V. The sample is then linearly heated up to a temperature (T_{stop}) higher than the initial one (T_{start}), taking into account the current formed. Afterward, it is cooled back to a temperature T_{start}. The entire procedure is repeated by setting higher temperature T_{stop} during the next iteration. The incremental temperature step in this case is 5 °C and it depends on the band gap width and the current flow magnitude. Scanning of as wide as possible temperature range is done until temperature above the ambient is reached (in this case it is only 45 °C, due to possible thermal degradation of the organic film). In the temperature range lower than the room temperature information about the shallow traps is derived, respectively the current change in the high temperature range is ascribed to the deep traps behavior. The relation between the thermally stimulated current, the traps concentration and their energy position is described elsewhere [13].

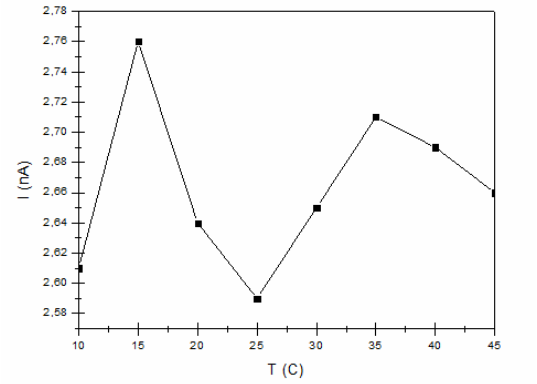

Fig. 5. Thermally stimulated current of organic PPV based electroluminescent sample, measured by the designed setup.

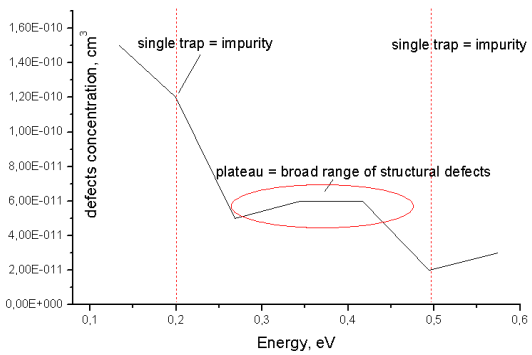

Fig. 6. Concentration and energy distribution of the defects in PPV film, determined from the thermally stimulated current.

It can be noted that in the middle range of the energy spectrum current plateau was formed. This means that the defects revealed in this range are structural. The abrupt change in the concentration of traps for 200 meV and 500 meV can be related to single traps due to impurities implanted probably with the film deposition. In general, the trap activation energy is low, which is proof for easy activation of traps, or they can be identified as shallow traps. Based on the results achieved, we can conclude that the origin of the defects is caused by the deposition method – particles from the ambient environment probably fall on the film surface due to lack of vacuum in the deposition chamber. The structural defects can be caused by the pressure of the aerosol stream. In this way, feedback about the deposition conditions can be got and they can be optimized.

V. Conclusion

Taking into account the performed measurements and the experimental results, it can be deduced, that the designed laboratory device for managing the Peltier element has adequate performance and functionality, as planned in advance. Moreover, the device allows other functions to be added, due to the capabilities of the microcontroler.

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AUTHOR INDEX