Testing of digital filters for power-line interference removal from ECG signals

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Abstract – **A procedure for testing digital filters for power line interference removal from ECG signals is proposed in this article. The testing procedure is developed in a MatLab environment. It allows different filters to be tested and compared based on the residual error from the filtration. A procedure for measurement the frequency and the amplitude of the power line interference is also developed.**

Keywords – **ECG signals, Digital filters, Subtraction procedure.**

I. Introduction

The electrocardiographic (ECG) signals are often affected by electrical disturbances. The most typical for standard electrocardiography are power-line interferences (brume) – (Huhta & Webster, J 1973) [1], (Ziarani & Konrad, 2002) [2], (Lee & Lee, 2005) [3].

In the practice, different digital filters for interference subtraction form ECG signals are used: averaging filters – (Taylor & McFarlane, 1974) [4]; band-stop (notch) filters – (Ma et al., 1999) [5]; adaptive filters – (Zia-Ur-Rahman et al., 2011) [6]; genetic algorithms – (Kumaravel & Nithiyanandam, 1998) [7]; regression subtraction – (Baratta et al., 1998) [8]; subtraction procedure – (Levkov et al., 2005) [9] and others

A comparative test of five different digital filters for interference suppression in ECG signals is done in (Christov, 2005) [10]. The performance of the filters is estimated by Mean Square Error and Mean Absolute Error.

II. Methodology for Testing Digital Filters for Power Line Interference Removal

The following test procedure for digital filters for interference removal from ECG signals has been established (Georgieva et al., 2002) [11], which is illustrated in Fig. 1. It consists of following steps:

Step 1 – a synthesized power-line interference is added to a conditionally clean from interference ECG signal. The interference is generated with constant or variable amplitude and frequency;

Step 2 – The contaminated with interference ECG signal is subjected to filtering for interference removal in purpose of the digital filter testing;

Step 3 – An error is calculated as an absolute difference between the conditionally clean ECG signal and the signal after the digital filtration.

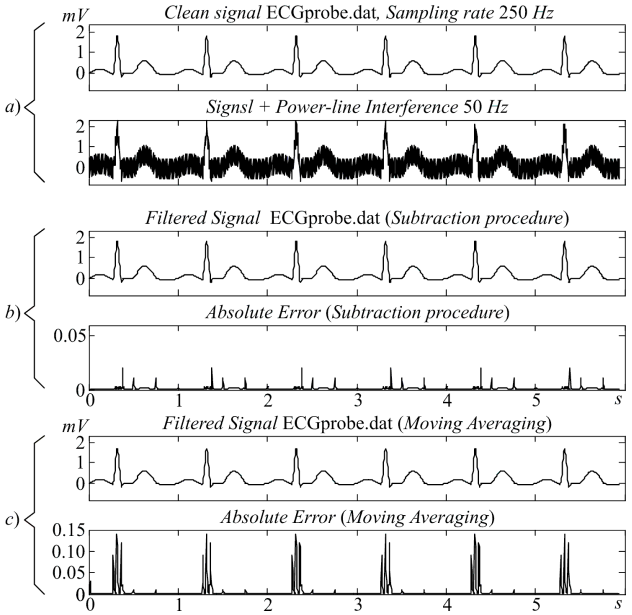

Fig. 1. Test experiments: a) – input signal; b) – subtraction procedure application; c) – moving averaging application.

III. Program Implementation of the Digital Filter Testing Procedure

The testing procedure for digital filters for interference removal from ECG signals is implemented in MatLab environment and consists of two modules. The first module is shown on Fig. 2.

```
%%% Load ECG probe %%%
name1='ECGprobe.dta'; Q=250; res=0.02; name2='ECGprobe.tes';
% name1='R0012.dta'; Q=200; res=0.00488; name2='R0012.tes';
% name1='AHA_7009.dta'; Q=250; res=0.005; name2='AHA_7009.tes';
% name1='N0039.dta'; Q=400; res=0.00488; name2='N0039.tes';
% name1='D0145.dta'; Q=16000; res=0.02; name2='D0145.tes';

fid=fopen(name1,'r'); x=fread(fid,'float'); fclose(fid);
LX=length(x); if LX>16*Q; LX=16*Q; end
```

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```
10 x=(x(1:LX)); % Signal length
11
12 t = 1/Q;
13 a=zeros(1,LX); am=1; %%% Amplitude deviation %%%
14 for i=1: 1: LX;
15 %     a(i) = am; % constant
16 %     a(i) = am/LX*i; % linear low
17     a(i) = abs(am*cos(2*pi*0.06*i*t)-am)/2; % sinusoidal low
18 %     if i<LX/2; a(i)=am; else a(i)=0; end % abrupt change
19 end
20 dPL=zeros(1,LX);  %%% Frequency deviation %%%
21 F=50; dF=F*0.015;
22 for i=1: 1: LX;
23 %     dPL(i)=dF; % constant
24     dPL(i)=i*t*dF/8-dF; % linear low
25 %     dPL(i)=dF*sin(2*pi*0.0625*i*t); % sinusoidal low
26 %     if i<LX/2; dPL(i)=+dF; else dPL(i)=-dF; end % abrupt change
27 end
28 %%% Interference composing %%%
29 PL=x*0; iF=0;
30 for i=1: 1: LX;
31     iF=iF+dPL(i)*t;
32     PL(i) = a(i)*sin(2*pi*(F+iF/i/t)*i*t);
33 end
34 X = x+PL;       % Add mains interference
35 fid=fopen(name2,'w'); fwrite(fid,X,'float'); fclose(fid);
36
37 %%% Call Subtraction procedure for Power-Line Interference removing
38 M=0.1; r=5; [Y]=PLI_removal_Vd1(X,res,Q,F,M,r);
39 %%% Errors calculating %%%
40 Err = abs(Y-x);
41 Err_max=0; Err_ms=0; m=0;
42 for i=Q: 1: LX-Q;
43     m=m+1; Err_ms=Err_ms+(Err(i)*1000)^2;
44     if Err(i)>Err_max; Err_max=Err(i); end
45 end
46 Err_max=Err_max*1000
47 Err_ms=sqrt(Err_ms/m)
48 %%% Visualization %%%
49 tt = 0: 1/Q: LX/Q;
50 axe=1:LX;
51 Hh1=[0 LX*t min(x)-max(a) max(x)+max(a)];
52 Hh2=[0 LX*t 0 .06];
53 figure(1);
54 subplot(4,1,1)
55 plot(tt(axe),x(axe),'k'),title('Original conditionally clean signal'); axis(Hh1);
56 subplot(4,1,2)
57 plot(tt(axe),X(axe),'k',tt(axe),a(axe),'r',tt(axe),dPL(axe),'g'),
58 title('Signal+interference, amplitude & frequency deviation'); axis(Hh1);
59 subplot(4,1,3)
60 plot(tt(axe),Y(axe),'k'), title('Processed signal'); axis(Hh1);
61 subplot(4,1,4)
62 plot(tt(axe),Err(axe),'k'), title('Zoomed absolute error'); axis(Hh2);
```

Fig. 2. Program module for test signal synthesis, ECG signal filtration and error calculation.

The power-line interference is estimated as a difference $B = X - Y$ between the input and the filtered signal (line 12). Then, used buffers, parameters and coefficients for the processing are declared and defined (lines 14-32). The treatment includes a calculation of the frequency (lines 36-44) and the amplitude (lines 46-52) of the power-line interference, as well as result visualization (lines 54-68).

A. Step 1

The conditionally clean ECG signal is loaded from file (line 2). The file name **.dta** , the sampling rate **Q** and the resolution **res** are specified before the test (lines 2-6).

Then the amplitude **am** of the power-line interference is specified (line 13). The way of the amplitude variation of the power-line interference can be selected between constant, linear law, sinusoidal law or abrupt change in the middle of epoch (lines 14-19).

The frequency of the power-line interference is specified with a rated value **F** and a deviation **dF** (line 21). The tapes of frequency deviation in the time are also chosen between constant, linear law, sinusoidal law, or abrupt change (lines 22-27).

The synthesized power line interference is then added to the original signal (line 34), after that the signal is recorded in a test file **.tes** (line 35).

B. Step 2

The signal with added interference is processed by the digital filter which is being tested. In this example, the subtraction procedure for interference removal from ECG signals is use as a digital filter. The subtraction procedure is organized as a MatLab function (Mihov et al., 2006) [12]. The input parameters for the function are:

X – Original ECG signal, *mV* (row vector or column vector);

Res – Resolution, *mV*;

Q – Sampling rate, *Hz*;

F – Frequency of the power-line interference, *Hz*;

M – Threshold for the linearity criterion, *mV*;

r – Number of averaging samples in the period of the power-line interference, *integer*.

The output parameter of the functions is:

Y – Filtered (processed) ECG signal, *mV* (the same dimension as **X**).

C. Step 3

The error is formed as an absolute difference between the conditionally clean ECG signal and the resultant signal after the digital filtration (line 42). The absolute maximal **Err_max**, μV and the mean square error **Err_ms**, μV are estimated (lines 42-47).

On Fig. 3 is visualised the testing of the subtraction procedure. Synthesised ECG signal ECGprobe.dta is used as a conditionally clean ECG signal.

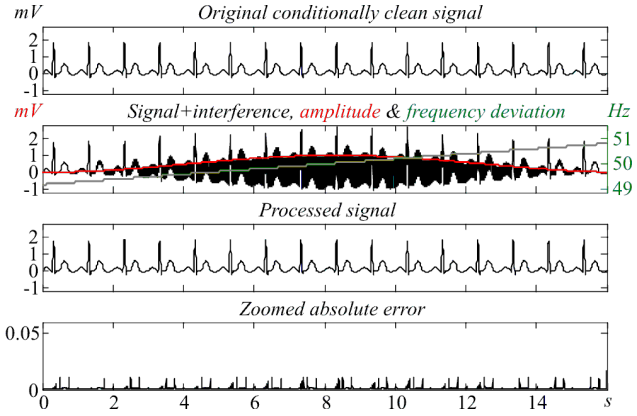


Fig. 3. Experiments with the subtraction procedure with signal ECGprobe.dta : Err_max = 11,35; Err_ms = 1,77

The second program module is shown on Fig. 4. Firstly, the contaminated with the synthesized interference ECG signal is loaded from a file. The sampling rate **Q**, the resolution **res**, the interference frequency **F** and the number of averaged samples **r** are also defined (lines 2-5). Then the signal is filtered (in this case with the subtraction procedure – line 11).

```
1   %%% Load ECG Test probe
2   % name='R0012.tst'; Q=200; res=0.00488; F=50;
3   % name='AHA_7009.tst'; Q=250; res=0.005; F=60;
4   name='N0039.tst'; Q=400; res=0.00488; F=60;
5   % name='D0145.tst'; Q=16000; res=0.02; F=50;
6
7   fid=fopen(name,'r'); X=fread(fid,'float'); fclose(fid);
8   LX=16*Q; X=(X(1:LX)); % Signal length
9                         %%% Input Parameters %%%
10  %%% Call Subtraction procedure for Power-Line Interference removing
11  M=0.1; r=3; [Y] = PLI_removal_Vd1(X,res,Q,F,M,r);
12  B = X-Y;              % Interference estimation
13                            %%% Buffers definition %%%
14  B2 = zeros(1,LX);     % Interference buffer_2 definition
15  A = zeros(1,LX);      % Amplitude buffer definition
16  dFPL = zeros(1,LX); % Power-line frequency buffer definition
17                            %%% Parameters calculating %%%
18  U2=0; U2new=0; dFmax=F*0.025; Bmin=0.02;
19  n = floor(Q/F);     % Floor 'Multiplicity'
20  m = floor(Q/F/2);   % Floor 'Semi-multiplicity'
21  q = floor(Q/F/4);   % Floor 'Quoted-multiplicity'
22  Cm = 2*m+1-n;
23                            %%% Coefficients calculating %%%
24  KF0 = cos(2*pi*q*F/Q); KFnew=KF0; KF=KF0; % Initial value of KF
25  KFmin = cos(2*pi*q*(F+dFmax)/Q);
26  KFmax = cos(2*pi*q*(F-dFmax)/Q);
27  KFspd = (KFmax-KFmin)/(Q/(2*n));
28  kf=2*dFmax/(KFmin-KFmax);
29  K2F0 = (sin(n*pi*2*F/Q)/sin(pi*2*F/Q))/n; % Initial value of K2F
30  K2Fbeg = (sin(n*pi*2*(F-dFmax)/Q)/sin(pi*2*(F-dFmax)/Q))/n;
31  K2Fend = (sin(n*pi*2*(F+dFmax)/Q)/sin(pi*2*(F+dFmax)/Q))/n;
32  R2k = (K2Fbeg-K2Fend)/(KFmax-KFmin);
33                                %%              % Processing %%%
34  for i=1+n+1: 1: LX;           % Start of Main Loop
35                  %%% Frequency Deviation Estimation %%%
36      if abs(B(i-q)-B(i-3*q))>Bmin;           % Division zero protection
37          KFnew=(B(i)-B(i-4*q))/(2*(B(i-q)-B(i-3*q)));
38      end
```

```
    if KFnew-KF>KFspd; KFnew=KF+KFspd; end  % KF speed protection (rising)
    if KFnew-KF<-KFspd; KFnew=KF-KFspd; end % KF speed protection (falling)
    if KFnew>KFmax; KFnew=KFmax; end        % KF maximum protection
    if KFnew<KFmin; KFnew=KFmin; end        % KF minimum protection
    KF=KF*(1-20/Q)+KFnew*20/Q;
    dFPL(i)=F+(KF-KF0)*kf;
                %%% Amplitude Deviation Estimation %%%
    B2(i)= B(i)^2;                          % Second Interference buffer
    K2F = K2F0+R2k*(KF-KF0);                % K2F approximation
    U2=U2+((2-Cm)*(B2(i)-B2(i-2*m-1))+Cm*(B2(i-1)-B2(i-2*m)))/n/2; % Averaging
    A(i)=1.41*sqrt(abs((U2-B2(i-m)*K2F)/(1-K2F))); % Amplitude estimation
    A(i)=A(i)*0.1+A(i-1)*0.9;               % Amplitude filtration
    if abs(A(i))<Bmin; KF=KF0; end;         % Zero amplitude protection
end                                         % End of Main Loop
                          %%% Visualization %%%
tt = 0: 1/Q: LX/Q;
axe=1:LX;
Hh1=[0 LX/Q min(X)*1.1 max(X)*1.1];
Hh2=[0 LX/Q min(B)*1.2-0.1 max(B)*1.2+0.1];
Hh3=[0 LX/Q F-dFmax F+dFmax];
figure(2);
subplot(4,1,1)
plot(tt(axe),X(axe),'k'),title('Tested Signal'); axis(Hh1);
subplot(4,1,2)
plot(tt(axe),Y(axe),'k'), title('Processed Signal'); axis(Hh1);
subplot(4,1,3)
plot(tt(axe),B(axe),'k',tt(axe),A(axe),'r') ,title('Interference & Amplitude');
axis(Hh2);
subplot(4,1,4)
plot(tt(axe),dFPL(axe),'g'), title('Frequency Deviation'); axis(Hh3);
```

Fig. 4. Program module for testing digital filters for power-line interference removal from ECG signals, including frequency and amplitude of the interference calculation.

D. Frequency estimation of the power-line interference

The frequency deviation of the power-line interference is determined by estimation the transfer coefficient $K(f)$ of an averaging filter which has a zero for the rated value of the power-line interference frequency – (Mihov, 2012) [13].

The transfer coefficient of the averaging filter can be represented as a linear function of the current value of the power-line frequency by the Descartes equation $K(f) = K(F) + \tan\alpha.(f - F)$, as illustrated on Fig. 5.

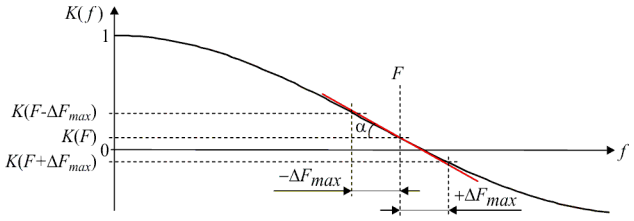


Fig. 5. Linear approximation of the transfer coefficient of an averaging filter within the range of the frequency deviation.

The tangents of the angle α, which the approximating line makes with the frequency axis is expressed with the first derivative of the transfer coefficient of the averaging filter for the rated value of the frequency F of the power-line interference $\tan\alpha = K^I(f)\Big|_{f=F}$. For the new value of the coefficient K_{Fnew} of the averaging filter can be written:

$$K_{Fnew} \equiv K(F_{new}) \approx K_B(F) + K^I(f)\Big|_{f=F}.(F_{new} - F) \quad (1)$$

from where:

$$F_{new} \approx F + \frac{K_{Fnew} - K_F}{K^I(f)\Big|_{f=F}}, \quad K_F \equiv K(F) \quad (2)$$

Representing the first derivative of $K(f)$ as a finite difference:

$$K^I(f)\Big|_{f=F} \approx \frac{K_{(+\Delta F\max)} - K_{(-\Delta F\max)}}{2.\Delta F_{\max}} \quad (3)$$

where $K_{(-\Delta F\max)} \equiv K(F - \Delta F_{\max})$ and $K_{(+\Delta F\max)} \equiv K(F + \Delta F_{\max})$, for F_{new} is resulting:

$$F_{new} \approx F + k_f.(K_{Fnew} - K_F),$$
$$k_f = \frac{2.\Delta F_{\max}}{K_{(+\Delta F\max)} - K_{(-\Delta F\max)}}. \quad (4)$$

When using so called 'two point' averaging filter the transfer coefficient is determined by the equation:

$$K_F \equiv K(F) = \sin\frac{2\pi qF}{Q}, \quad (5)$$

where q is the rounded to a lesser or to an equal integer number of samples in a quarter period of the power-line interference: `n=floor(Q/F/4)`. The new value of the transfer coefficient is re-calculated for every loop of the procedure from the extracted values B_i of the power-line interference – Eq. (7) from (Mihov, 2012) [13]:

$$K_{Fnew(i)} = \frac{B_i - B_{i-4q}}{2.(B_{i-q} - B_{i-3q})}. \quad (6)$$

Before including in Eq. (4) the new value of the transfer coefficient is subjected to a low-pass filtering:

$$K_{F(i)} = a.K_{Fnew(i)} + b.K_{Fnew(i-1)}, \quad (7)$$

where coefficients $a = 20/Q$ and $b = (1 - 20)/Q$ are experimentally chosen according numinous of tests.

After substitution in Eq. (4) the current value of the power-line interference is estimated by:

$$F_{new(i)} \approx F + k_f.\left(K_{Fnew(i)} - K_F\right), \quad (8)$$

E. Amplitude estimation of the power-line interference

The amplitude A of the power-line interference is estimated using its effective value U.

When the number of samples $n = Q/F$ within the period of the power line interference is odd ($n = 2m + 1$), the quadrature value of the mains interference is calculated from extracted samples B_i of the power-line interference:

$$U_i^2 = \frac{1}{n}\sum_{j=-m}^{m} B_{i+j}^2, \quad n = 2m+1 \quad (9)$$

This formula represents a symmetrical averaging filter. When n is an even number ($n = 2m$), the similar averaging filter is used:

$$U_i^2 = \frac{1}{n}\left(\sum_{j=-m+1}^{m-1} B_{i+j}^2 + \frac{B_{i-m}^2 + B_{i+m}^2}{2}\right), \quad n = 2m \quad (10)$$

The two Eqs. (9) and (10) can be combined in:

$$U_i^2 = \frac{1}{n}\left[\sum_{j=-m}^{m} B_{i+j}^2 - \frac{c_m}{2}\left(B_{i-m}^2 + B_{i+m}^2\right)\right], \quad (11)$$

$$c_m = 2m + 1 - n.$$

When the sampling rate is not multiple to the power-line frequency, for the parameter n is used the rounded to a lesser or to an equal integer `n=floor(Q/F)`. Similarly, for the number of samples m in the half-period of the power line interference is used the rounded to a lesser or to an equal integer `m=floor(Q/F/2)`. In this case the calculated quadrature value U_i^2 contains a component with a double higher frequency of the power-line interference. The compensation of this component successfully can be used the method for recurrent filter modification, similarly to the Eq. (21) from (Levkov et al., 2005) [9], applied for the doubled frequency of the power-line interference:

$$U^*_i = \sqrt{U_i^2 - \left(B_i^2 - U_i^2\right)\frac{K_{2F}}{1 - K_{2F}}}, \quad (12)$$

where U^*_i is the calculated current effective value of the power-line interference, K_{2F} is the transfer coefficient of the filter from the combined Eq. (9) for the doubled frequency of the interference:

$$K_{2F} \equiv K\left(2.F\right) = \frac{1}{n}\cdot\frac{\sin\frac{n\pi 2F}{Q}}{\sin\frac{\pi 2F}{Q}} S_{C2Fm}, \quad (13)$$

$$S_{C2Fm} \equiv S_{Cm}\left(2.F\right) = \cos\frac{c_m \pi 2F}{Q}$$

If there is a deviation of the power-line interference frequency the coefficient K_{2F} is also changed. Therefore it should be modified dynamically.

The coefficient $K_{2Fnew} \equiv K_{2F}\left(2.F_{new}\right)$, similarly to Eq. (1), also can be represented as a linear function:

$$K_{2Fnew} \approx K_2\left(F\right) + K_2^I\left(f\right)\Big|_{f=2.F}.\left(2F_{new} - 2F\right) \quad (14)$$

Substituting K_{Fnew} from (1) in (12), the new value of K_{2Fnew} is calculated by:

$$K_{2Fnew} \approx K_2\left(F\right) + \frac{K_2^I\left(f\right)\Big|_{f=2.F}}{K^I\left(f\right)\Big|_{f=F}}.2.\left[K_{Fnew} - K_F\right] \quad (15)$$

Representing the first derivative $K_2^I\left(f\right)\Big|_{f=2F} \approx \frac{K_{2(+2\Delta F\max)} - K_{2(-2\Delta F\max)}}{2.2\Delta F_{\max}}$ as a finite difference, where $K_{2(-2\Delta F\max)} \equiv K_2\left(2F - 2\Delta F_{\max}\right)$ and $K_{2(+2\Delta F\max)} \equiv K_2\left(2F + 2\Delta F_{\max}\right)$, the new value of K_{2Fnew} can be calculated by:

$$K_{2Fnew} \approx K_{2F} + R_{2K}.\left(K_{BFnew} - K_F\right),$$

$$R_{2K} = \frac{K_{2(+2\Delta F\max)} - K_{2(-2\Delta F\max)}}{K_{B(+\Delta F\max)} - K_{B(-\Delta F\max)}}. \quad (16)$$

The calculated by the Eq. (14) the new value K_{2Fnew} substitutes the value K_{2F} in the Eq. (10) and the current amplitude A of the power-line interference is estimated by:

$$A_i = \sqrt{2}.U^*_i. \quad (17)$$

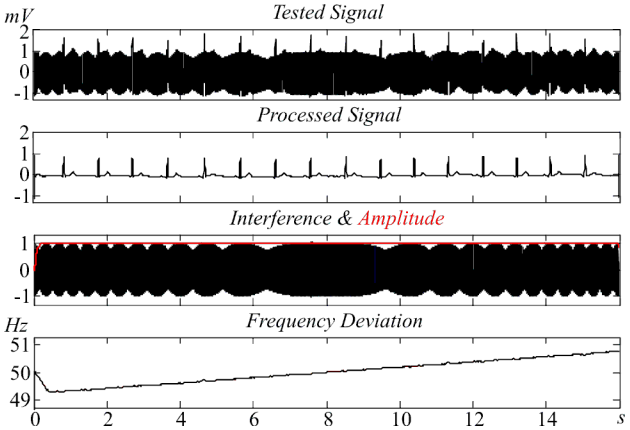
Similarity to the Eq (7) the new value of the amplitude is low-pass filtered by:

$$A_i = 0{,}1.A_i + 0{,}9.A_{i-1} \quad (18)$$

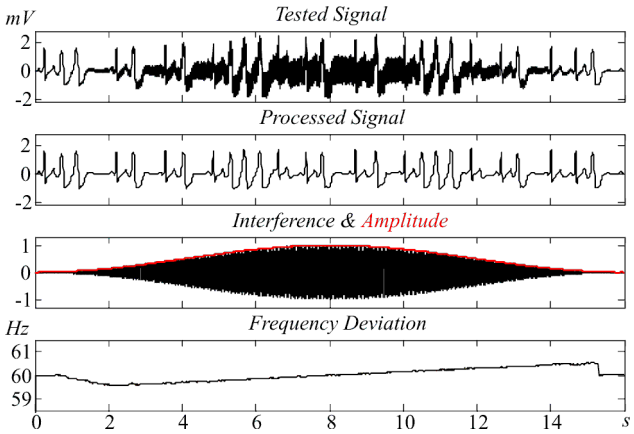
IV. EXPERIMENTS

On Fig. 6 are shown results from experiments with several different ECG signals with added synthesized power-line interference of different frequency deviation. The amplitude of the interference is varied with different ways in the range from 0 to 1 *mV*.

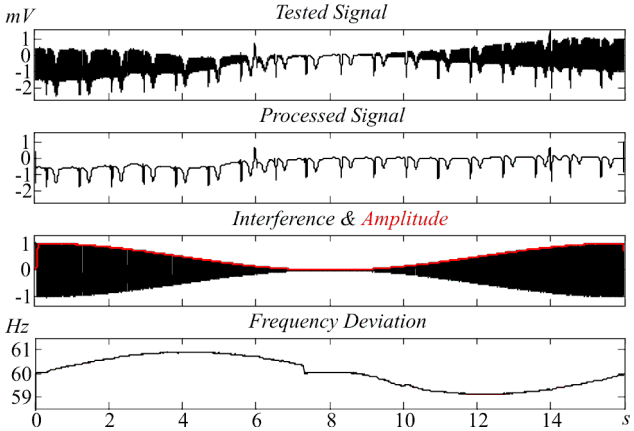
The first subplot shows the tested signal, the second subplot – the filtered from an interference ECG signal. On the third subplot is shown the extracted mains interference together with the estimated amplitude. The fourth subplot shows the calculated frequency of the power-line interference.



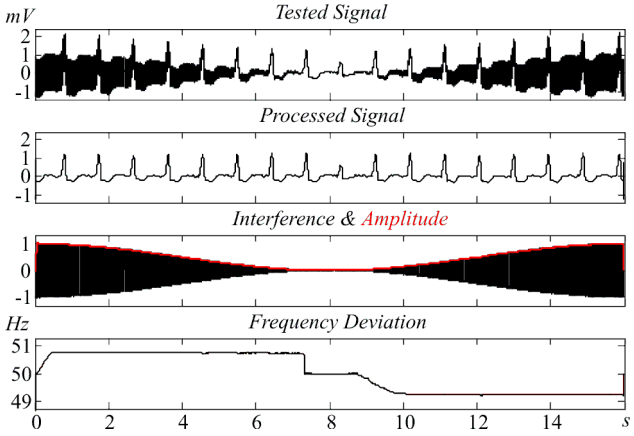
Test No 1: Signal R0012.tst , $Q = 200$ *Hz*, $F = 50{\pm}0{,}75$ *Hz*.



Test No 2: Signal AHA_7009.tst , Q = 400 *Hz*, F = 60±0,9 *Hz*.



Test No 3: Signal N0039.tst , Q = 400 *Hz*, F = 60±0,9 Hz.



Test No 4: Signal D0145.tst , Q = 16 *kHz*, F = 50±0,75 *Hz*.

Fig. 6. Tests for power-line interference removal from ECG signals with interference amplitude and frequency estimation.

V. Conclusion

A testing system for power-line interference removal from ECG using digital filters is proposed. The system is developed in MatLab environment and consists of two modules: a module for synthesis of test signals with added power line interference, ECG signal filtration and error calculation; a module for power-line interference filtration with amplitude and frequency estimation.

The first module can be used for testing and comparison of different digital filters according to the residual error.

The second module can work with real contaminating ECG signals. The offered methodology for interference amplitude estimation offers higher precision in comparison with ones, used at ECG signals filtration.

The proposed testing system can be used in the analysis and the evaluation of digital filters for power-line interference removal from ECG signals. It can be used also in the teaching process for students studying the field of the digital filtration.

References

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Telemetry of patients with pacemaker applying ECG sonification

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***Abstract* – Modern communication technologies allow significant extension of the ambulatory monitoring of risk patients. The practice shows that one of the most common causes for remote monitoring compromise is the lack of skills for use of the equipment. An alternative representation of ECG is investigated in this paper. The aim is to provide an innovative approach for ECG transmission on long distance using a simple GSM module working in standard voice communication mode. The proposed procedure - "sonification" is tested with signals recorded from patients with cardiostimulator. Our experiments confirmed reliability of data processing and signal presentation with quality guarantying the correctness of medical conclusions.**

Keywords –**Patients telemetry, ECG monitoring, ECG sonification,**

I. INTRODUCTION

The telemedicine has been introduced about 35 years ago during the time when the telephones and fax machines were the main telecommunication tools. In the recent years, several telemedicine applications have been successfully implemented using wired communication technologies like POTS and ISDN. However, the wireless communication technologies and data transfer standards like GSM, GPRS, 3G, 4G, allow the operation of wireless telemedicine systems considerably improving the diagnostic process.

In 2002, *F Gouaux et al* [1] proposed a portable device for telemedicine. However, it was still insufficient due to the lack of processing of the raw ECG signals. *E Kyriacou et al* [2] designed a telemedicine framework but it did not discuss the issue of processing raw ECG signals on the mobile device. Guidelines for designing telemedicine for the future applications were given by B. *Woodard et al* [3] and *P Rubel et al* [4].

The ECG signal recorded from a patient with cardiac pacemaker consists of autonomous ECG signal, pacemaker pulses and noises. The informative part of the ECG signal lies in the frequency band 0.05 – 150Hz and its dynamic range is usually up to 5mV. The pacing pulse on the body surface usually have very fast rising edges from less than 10 µs to 100 µs and could be as small as few hundreds µV. The pacing "artefacts" detection is important since they indicate the presence of pacemaker and help to evaluate the heart reaction. All pertinent medical standards require the pacing artefacts to be captured and indicated on the device screen.

There are different medical standards with variable requirements regarding the height and width of the pace pulse, that has to be identified and marked on the record. According to *ANSI/AAMI EC11* [12] the pacemaker pulses that should be obligatory detected are with the parameters:

- duration - 0,1ms to 2ms
- amplitude - 2mV to 250mV
- frequency - up to 100 pulses per minute
- rising edge - less than 100µs

The *IEC60601-2-27* [13] standard states different requirements relating to the duration (0.5 ms to 2.0 ms) and the amplitude (2mV to 700 mV) of the pulses.
Additionally the modern pacemakers could generate smaller pacing pulse amplitudes that could fall below the requirements fixed in the standards and lead to complications in the detection algorithms (*Woodward* [5]).

In Kramer's "Sonification Report" (*Kramer* [9]), the following definitions of sonification are presented: *"Sonification is defined as the use of nonspeech audio to convey information. More specifically, sonification is the transformation of data relations into perceived relations in an acoustic signal for the purposes of facilitating communication or interpretation."* The most recognizable, and one of the earliest applications is the Geiger counter. A Geiger counter uses audible clicks, with intensity and frequency depending on the level of radiation around the device. Sonification is used in a vast range of applications in the field of biomedical signals registration and processing. Auscultation of the Doppler frequency in ultrasound medical devices is another sample for medical interpretation of physiological processes using sound. *Hermann et al* [7] presented three parametric sonification techniques for human electroencephalogram (EEG) data. *Hermann with Baier and Stephani* [6], developed a sonification technique for EEG data aimed at detecting and categorizing epilepsy. *Ballora et al* [8] utilized sonification as a method to analyze electrocardiogram (ECG) data of patients. *Avbeji* [11] made sonifications of ECG and EEG recordings to demonstrate the processing capabilities of the auditory system for these types of signals. *Kather et al* [10] introduced a method for polyphonic sonification of ECG data, whereby different ECG channels are simultaneously represented by sound of different pitch.

An approach considerably extending applicability of ambulatory monitoring of patients with pacemakers is presented in this paper. Its specific features are:

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- High-frequency ECG registration and pace pulses identification;
- ECG sonification;
- Data transmission using GSM module in standard mode (voice communication).
- Absence of specialized interfaces and complicated procedures for connection between ECG device and GSM.

II. Method

The main steps of signal processing are presented on fig. 1. The paced ECG signal has to be digitally converted with high sample rate (> 10kHz) taking into account the pace pulse duration. A sampling frequency 18 kHz and resolution 10 bits are applied in the our case.

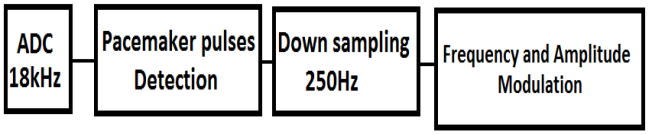

Fig. 1. Paced ECG sonification

The algorithm for pace pulse detection has been described in details in previous our work *Tabakov* [14]. The digital procedure is based on the calculation of the signal slope in time interval - 500 µs. The following equation is applied:

$$S_j = \left[\sum_{i=1}^{4}(X_j - X_{j-i}) + \sum_{i=1}^{4}(X_j - X_{j+i})\right]^2$$

If the current slope (S_j) is higher than an adjustable threshold, the threshold becomes equal to the current slope and pacemaker pulse detection mark (PPM_j) juxtaposes with the current sample j. The next step is "down sampling" resulting in considerably reduction of data buffer size - corresponding to the sample rate of 250 Hz. The final step is digital modulation. Frequency modulation of the signal is with parameters: carrying frequency - 700 Hz, sampling frequency - 10000 Hz and the frequency deviation - 100 Hz. Amplitude modulation is applied only in the regions with duration of 200 µs where the pace pulses were detected. The correctness of the procedure was tested in MATLAB, using a paced ECG signal recorded from patient with cardiostimulator working in VOO mode (Ventricle stimulation – No chamber sensed - No response). A fragment of the program for frequency+amplitude modulation is presented below.

```
fp=fopen('D:\Paients\Patient_24.DAT','r');
% Open file and create file pointer, Fs=18000Hz,
V=5uV/bit
RecLen=200000;
d=fread(fp,RecLen,'int16');
%Read 1500 discrets from file
d = upsample(d,32);
%Upsampling  Fs_new=Fs*25;  Inserting of N-1 (31)
zeros in signal
d=d*0.005; % digits to millivolts
Time=0:1/18750:(RecLen-1)/18750;
% Time vector %x=zeros([RecLen 2]);
x(1:RecLen*32,1)=d;
x(1:RecLen*32,2)=d;
xy=fmmod(x,700,10000,100);
%…….  Amplitude modulation procedure……..
for i=1:RecLen-size(sin2000)
   if mark(i)>100
      for j=1:size(sin2000)
        endsignal(i+j,1)=endsignal(i+j,1)*1.04;
      end
      i=i+size(sin2000);
   end
end
```

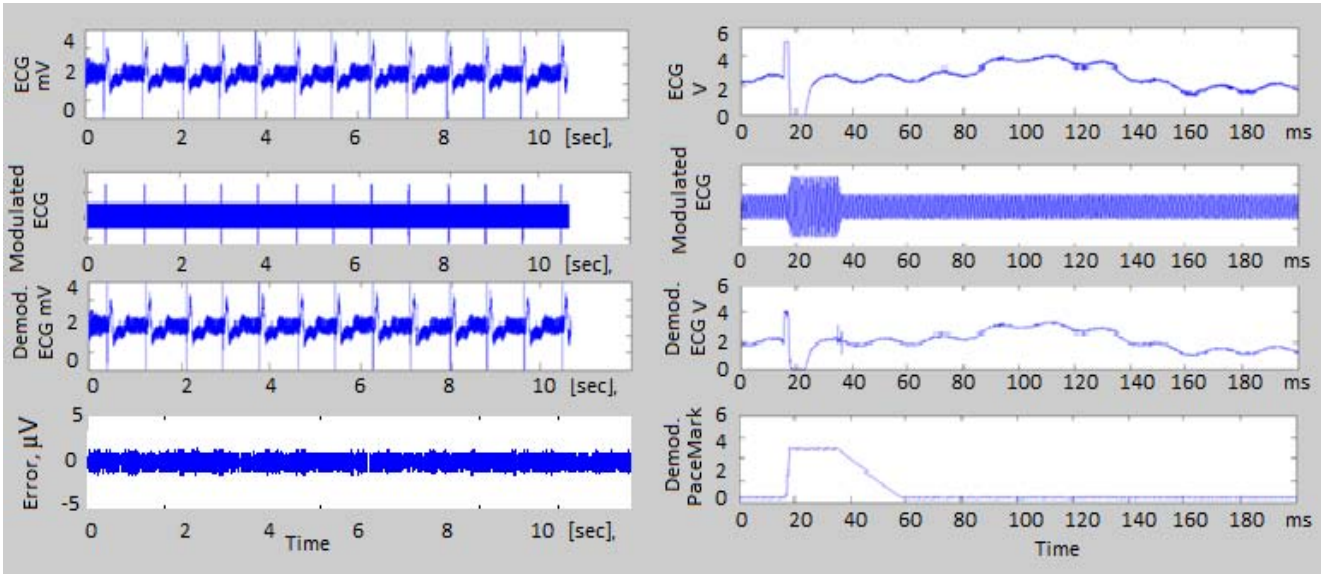

Fig. 2. Sonification procedure realized by digital modulation in MATLAB. Left subplots: 1)-epoch from paced ECG signal, 2)-modulated ECG+detected pace-pulses, 3)-signal after modulation/demodulation procedures; 4)-The difference between 1) and 3). Right upper subplots – extended time scale of the same signal visualizing one pace-pulse. The subplot 4) – demodulated pace mark

As can be seen in Fig.2 the described digital procedure doesn't influence on the signal. The error (last subplots) calculated as a difference between the input ECG signal and the ECG signal after modulation/demodulation is in the range of the digital signal resolution. The subplots on the right side of fig. 2 show the modulation/demodulation procedures in the pace-pulse region. The amplitude of the pace-pulse after frequency demodulation (subplot 3) is slightly decreased because of the limited number of samples describing its flat part. This could be a premise for impossibility for pace-pulse transfer in some cases (e.g. very short pulse). The result after amplitude demodulation in the pace-mark region (applying peak detection procedure) is presented on subplot 4. The prolonged peak's plateau is sonificated with a specific beep (1 kHz) superimposed on the sonificated ECG signal. In this manner the transfer of peak-mark is reliable and independent on the pace-pulse parameters.

III. Results

The applicability of the sonification procedure for ambulatory tele-monitoring was tested using system configuration presented in Fig. 3.

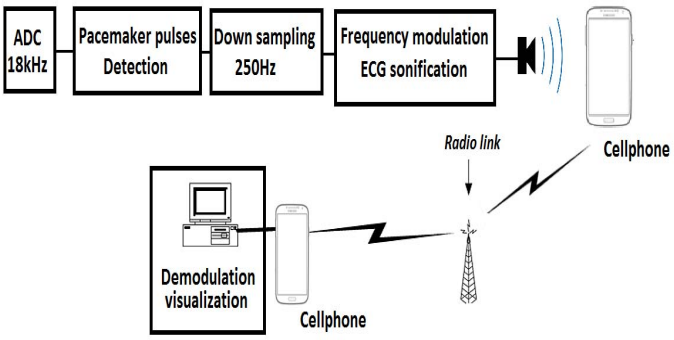

Fig. 3. System configuration of the sonification procedure test

The ECG signal from patient with cardiostimulator is converted to audio signal and reproduced in sound by audio speaker of personal computer. A low class GSM, placed close to the speaker, receives and transmits audio signal to the remote GSM module connected to the second computer via serial interface. The modulated and demodulated ECG signals and corresponding pace marks in the receiving computer are presented in fig. 4.

IV. Conclusion

An approach for telemetry of high-risk patients with pacemakers using GSM for data transfer has been presented. Unlike previous approaches, in this case the high-frequency ECG with detected pace-pulses is converted into audio format (sonificated). In this manner the GSM device is used in standard mode – voice communication. An advantage of this approach is absence of specialized interfaces between ECG device and GSM, resulting in considerably facilitation of the process of telemetry. Our first in-hospital tests with 10 patients (at Clinic of cardiology, Department. of Propaedeutic of Internal Diseases - University hospital "Aleksandrovska") confirmed applicability of sonification procedure for monitoring of patients with cardiostimulators. The analyzed ECG signal after modulation/demodulation transformations is with quality guaranteeing correctness of the medical conclusions. One of the advantages of the proposed approach is the convenience of manipulation, particularly for patients having not enough skills relating to the contemporary devices and interfaces for data transfer.

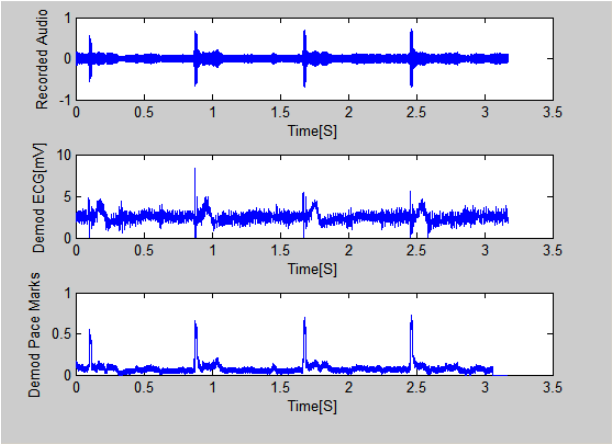

Fig. 4. Received ECG signal – before and after demodulation

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Arduino Based Module for Return Electrode Contact Quality Monitoring in the Electrosurgical Instruments

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Abstract – **The paper describes the development and realization of an Arduino based module for monitoring the contact quality of the patient returned electrode in the electrosurgical instrument. The module is designed in accordance with the requirements of the standard IEC 60601-2-2:209 for protection against electrical hazards from medical equipment. The experimental results of performed tests with 3 patients are presented and discussed.**

Keywords– **Electrosurgery, Patient return electrode, Contact quality monitoring.**

I. Introduction

Electrosurgery employs application of high radio frequency electrical current to a surgical site to cut, coagulate, ablate or seal tissue. In monopolar electrosurgery, the active electrode as part of electrosurgical instrument (ESI) is held by the surgeon and applied to the patient surface to be treated. Usually it has very small surface area as compared to the passive electrode. The smaller the electrode, the higher the current density around it, and the more localized the heating effect. In contrast, the passive electrode has a large contact surface area with patient to minimize heating at that site. The passive electrode is placed remotely from the active electrode to carry back the electrical current to the high frequency generator and safely disperse current applied by the active electrode [1].

The isolated electrosurgical instruments used in today practice eliminate many of hazards inherent in grounded systems, most importantly current division and alternative site burns. As shown on Fig. 1, the isolated generator does not include ground in the circuit, thus the high frequency (therapeutic) current can only flow through the passive electrode, called patient return electrode (PRE) [2].

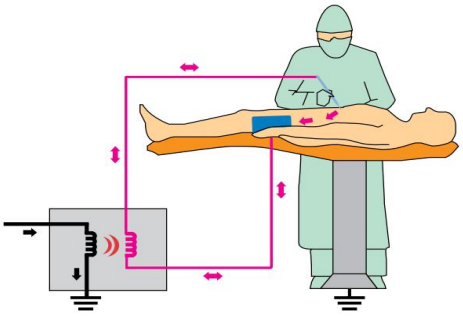

Fig. 1. Isolated electrosurgical instrument [2].

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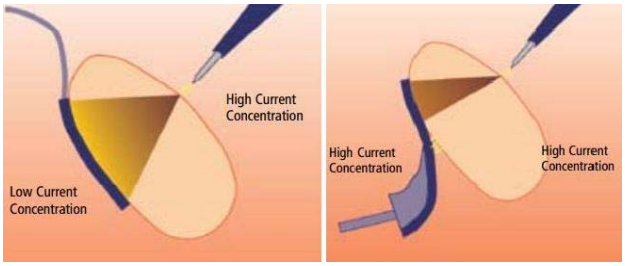
However, isolation does not take care of pad site burns due to loss of contact with the patient return electrode, which leads to the problem with loss of electrical contact at patient return electrode. Even though the patient return electrode is made of highly conductive material, it needs to maintain good electrical contact, as shown on Fig. 2a, with the patient's body during the whole surgical operation in order to avoid pad site burns. If the PRE shifts or peels off, the impedance in the circuit increases, generating enough current density even at the return electrode site as it is shown on Fig. 2b [2]. Heating and burns are caused by high current densities which directly depend on the surface area.



a) b)

Fig. 2. Current concentration at the PRE site.

According to the requirements of sub-clause 201.8.4.101 of the standard EN 60601-2-2:209 for protection against electrical hazards from medical equipment, the electrosurgical equipment should be provided with Contact Quality Monitor (CQM) of PRE. The Contact Quality Monitoring Systems work by inactivating the high-frequency generator of ESI if dangerously high impedance is detected at the return electrode/patient interface. High impedance implies the surface area in contact with the patient has decreased. In order to measure this impedance the patient return electrode is included in a separate, impedance monitoring circuit (REM), shown on Fig. 3, by dividing the electrode in two plates and measuring the voltage generated across the two parts. Such PRE, also known as 'split plate return electrode', is composed from conductive layer, usually metallic foil, split into two areas and covered in a conductive adhesive. A conductive tab provides a separate means of connection from the two areas to the high frequency generator of ESI – Fig. 4 [3].

Several REM systems based on US patents have been developed and incorporated in the commercial ESI which monitor if the measured impedance is within the predefined upper and lower limits range [4, 5]. However, the

physiological characteristics can vary significantly from patient to patient and from one location site for the PRE to another. Even for a particular patient, one location site could be more fatty or hairy than another. So, in order to monitor the quality of the contact of PRE with patient during ESI operation, it is necessary to measure the initial value of contact impedance and monitor continuously relative changes in respect to the initial value.

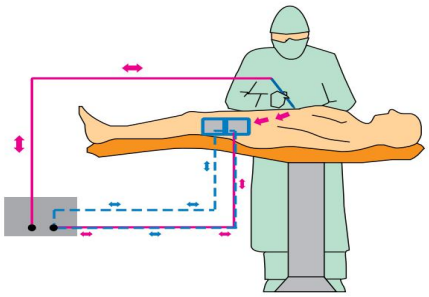


Fig. 3. Patient returned electrode monitoring circuit.

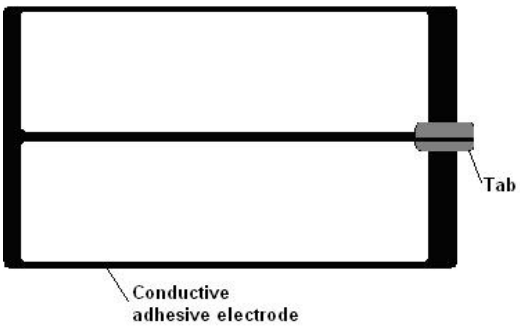


Fig. 4. Split plate return electrode.

The main goal of this paper is to describe the development of an autonomous module, based on Arduino open source hardware platform, for monitoring the quality of electrical contact between the patient returned electrode and the patient in the electrosurgical instruments.

II. PRE Contact Quality Monitoring Module

A. Technical Requirements

Considering the patient safety standard EN 60601-2-2:209, the developed module for patient return electrode contact quality monitoring (PRE CQM) should comply with the following requirements:

- Isolated power supply of PRE CQM module;
- Isolation between ESI and the patient in the PRE monitoring circuit;
- Continuous measurement of the contact impedance between the patient and the return electrode and comparing the value to the standard range of safe impedance (between 5 and 135Ω);
- The PRE CQM module should adapt to individual patient by measuring the initial contact impedance;
- The PRE CQM module should activate audio and visual alarms when either of the following events occur:

- The measured impedance of PRE is outside the limits of the standard range of safe impedance;
- An increase in the contact impedance of PRE is greater than 40% from the initial value.

B. Equivalent electrical circuit of the contact impedance between the patient and the PRE

The equivalent electrical circuit of the contact impedance (***Zx***) of the patient's body and a split plate return electrode is shown in Fig. 5, where:

- ***Zbody*** is the impedance of that part of the patient's body which is in contact with the return electrode;
- ***Re1*** and ***Re2*** are the resistances of the two plates of return electrode;
- ***C*** is the capacitance between the two plates of return electrode;

The value of ***Zx*** is a measure of the quality of the contact.

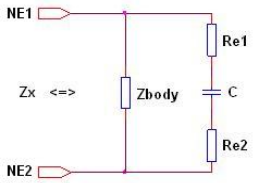


Fig. 5. Equivalent electrical circuit of the contact impedance between the patient and the PRE.

C. Block diagram of PRE CQM module

Block diagram of the developed PRE CQM module is present on Fig. 6. It is based on ARDUINO platform with four additional blocks. The first one is responsible for detection of contact impedance between the patient's body and the split plate return electrode. The second block is rectifier which generates a voltage proportional to the value of the detected contact impedance. The initial and current values of the continuously measured contact impedance are displayed on the integrated LCD display. The last block comprises the audio and visual alarms.

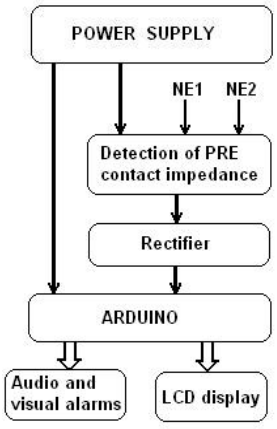


Fig. 6. Block diagram of PRE CQM module.

D. Detection of PRE contact impedance

The purpose of the circuit for detection of PRE contact impedance is to produce a voltage which is a function of the PRE contact impedance. It is realized as a blocking generator circuit shown on Fig. 7 with the patient return electrode connected to the secondary winding of the isolation transformer through connector J2. The

electrosurgical current is returned to the ESI via a lead connected between capacitors C3 and C4. These capacitors are connected across the second winding of the isolating transformer (TRAF NEMSY). This transformer has been developed by Kentamed Ltd. and has been used in their electrosurgical instruments.

The inductance of the primary winding of the transformer together with the capacitor C1 provide the required operating frequency of the generator across the operating range (from open loop to short circuit in the patient loop). In this way the frequency of the voltage at the output of the generator (the collector of the transistor Q1) is ≈65kHz for open loop situation. The third winding of the transformer provides positive feedback for starting-up generations. The peak-to-peak current flowing through the measured contact impedance (Zx) is 4,8mA which is in accordance with the medical standard for allowable values of safe currents flowing through the patients.

Through the capacitor C2 the output voltage of the generator is fed to the block "Rectifier". The output of the rectifier is connected to the input of the ADC integrated in ARDUINO module.

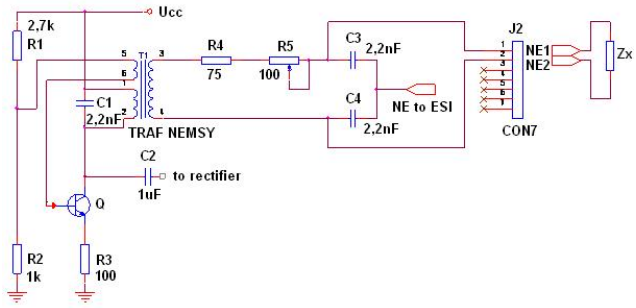


Fig. 7. Electrical circuit for detection of the contact impedance.

The block "Audio and visual alarms" comprises three LEDs and a buzzer. The green LED illuminates when the measured initial value of contact impedance is in the range from 0Ω to 135Ω. The yellow LED illuminates when the value of measured impedance is increased with 25% of the initially measured value (if it does not exceed 135Ω). The red LED illuminates when the measured value is raised by 40% of the initial value or if it exceeds 135Ω. The buzzer tones correspond to the yellow and red LEDs conditions.

III. Results

First, the developed module has been tested with an equivalent electrical circuit of the contact impedance composed by connected in parallel resistor and capacitor. Ten measurements have been made for every value of the contact impedances specified in Table 1. Then the average value, standard deviation and percentage deviation for each of the nominal values have been calculated. The verification shows that the maximum deviation in impedance measurement does not exceed 2,9%, which is considered to be acceptable in practical application of the module. Although no fixed recommendation by the standard is given, based on the information provided by ESIs producer Kentamed Ltd., the maximally tolerated measured impedance variation should be within 5%.

TABLE 1. RESULTS FROM VERIFICATION OF THE DEVELOPED MODULE

Zx (Ω)	average value	standard deviation	percentage deviation
5	5	0,00	0,0%
7	7	0,42	-2,9%
10	10	0,00	0,0%
30	30	0,42	-2,1%
50	50	0,42	-1,6%
70	70	0,32	-0,1%
90	90	0,00	0,0%
108	108	0,00	0,0%
130	130	0,00	-1,5%
135	135	0,48	-2,0%

The PRE CQM module has been tested with three patients. The experimental set-up is shown on Fig. 8. Single-use self-adhesive electrodes are used in the measurements. The initial value results strongly depend on the patient tissue impedance, the pressure from the patient body part on the electrode, the conductive adhesive covering the electrode, the skin condition.

The experimental results from the validation of the PRE CQM module with three patients for different contact areas between the patient and the split plate return electrode are present in Table 2. First, the initial value of contact impedance and the contact area between the patient and the return electrode are measured during the validation of the module. Then starting to peeling-off the return electrode from the patient skin when the yellow LED switch on the current value of contact impedance is measured and the corresponding contact area is determined. Similarly, continuing with peeling-off the return electrode from the patient skin when the red LED switch on the current value of contact impedance is measured and the corresponding contact area is determined.

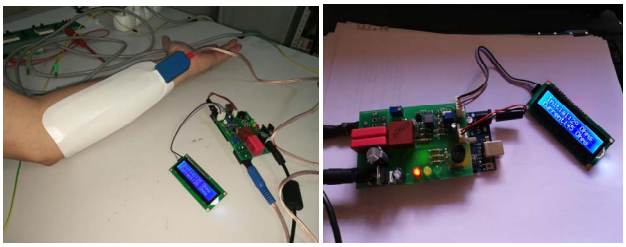


Fig. 8. Set-up for testing the PRE CQM module with patient.

Also, in the last column of Table 2 the maximum value of electrosurgical current which could pass through the return electrode and is safe for the patient is calculated for particular test conditions. These results show that the selected upper limit value of 135Ω for the contact impedance is adequate in terms of the actual values of the high frequency electrosurgical current. The experiment shows that this upper limit value provides safe use of the electrosurgical instrument with output power up to 170W, which are quite sufficient in most clinical applications. The upper limit value of 135 ohms for PRE contact impedance greatly reduces the risk of burning in the site of the return electrode area.

TABLE 2. RESULTS FROM VALIDATION OF THE PRE COM MODULE WITH THREE PATIENTS

Patient	PRE area [cm^2]	Contact impedance – initial value [Ω]	PRE area with Yellow LED indication [cm^2]	Measured contact impedance [Ω]	PRE area with Red LED indication [cm^2]	Measured contact impedance [Ω]	Safe value of HF electrosurgical current [A]
1	122,5	28	95,9	36	80,5	40	1,61
	122,5	28	94,5	36	77	40	1,54
	122,5	29	93,8	37	80,5	41	1,61
	122,5	29	98	37	78,4	41	1,57
	122,5	32	77	41	66,5	45	1,33
	122,5				29,2	135	0,58
2	122,5	49	89,6	62	74,9	69	1,50
	122,5	32	98	41	84	45	1,68
	122,5	35	88,9	44	77	50	1,54
	122,5				33,6	135	0,67
3	122,5	64	98	81	81,9	90	1,64
	122,5				63	135	1,26

However, for patients with very low tissue impedance, the upper limit value of 135Ω of PRE contact impedance is too high to assure the patient safety. Although these cases would be extremely rare, in the spirit of the risk management standards they need to be further considered. In the developed PRE CQM module, this risk is minimized by monitoring the current value deviation of the contact impedance from its initial value. For example, in patient number 1, it can be seen that when the value of the measured contact impedance reaches 135Ω the corresponding contact area is about 30 cm^2. We must note that the reason for this situation is the low tissue impedance of this patient, which is also the reason for the low initial impedance value of 28÷32 Ω. In this case, alarming the increase in the contact impedance of PRE with 40% from the initial value provides a contact area of 80 to 66 cm^2 and minimizes the risk of burning.

The indication with the yellow LED of changes with 25% in the value of measured contact impedance in respect to the initial value is considered to be very useful for the operator to show that a change of the contact area of the return electrode has began.

Although, this is preliminary validation of the module, the results presented in Table 2 show high correlation between the measured contact impedance value and the contact area between the patient return electrode and the patient body.

IV. CONCLUSION

In this paper the development and validation of an autonomous module, based on Arduino open source hardware platform, for monitoring the quality of electrical contact between the patient returned electrode and the patient in the electrosurgical instruments is presented. The PRE CQM module is developed complying with the requirements of the patient safety standard EN 60601-2-2:209.

The validation results show that the module can be successfully implemented in electrosurgical instruments.

ACKNOWLEDGMENTS

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Frequency Compensation in a Two-Integrator Loop Gm-C Biquad When Realized With Single Stage OTAs

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Abstract – **The paper considers the design of a two-integrator loop Gm-C second order filter, realized by single stage operational transconductance amplifiers (OTA). Two major problems are discussed: equalizing the maxima of OTA input voltages and unfavorable effect of OTA input capacitances. It is shown OTA input capacitances cause increasing of pole *Q*-factor and may turn the circuit to unstable. A method for avoiding of this problem is proposed, which could be applied for the other circuits of this class.**

Keywords – **active filters, Gm-C filters, operational transconductance amplifiers, stability.**

I. Introduction

Despite the permanent efforts of the researchers to propose new active filter architectures, the Gm-C filters are still most often used for implementation in the integrated circuits. Their basic structures are known and well described in the literature [1] and the difficulties, with which struggle the designers, relate mainly to their applications. These filters are used in very wide frequency range – starting from sub-1-Hertz range up to several hundreds of MHz. Other problems are: permanent demand for low-voltage operation and low power consumption, extension of the dynamic range, independence from the external influences. All they create challenges basically in the design of the operational transconductance amplifiers (OTA).

One option for realizing of fully differential OTA is to use two identical CMOS inverters – one inverter per each wire of the differential line [2]. This approach suggests several benefits – simplicity and small number of transistors allowing low voltage operation and small noise generation. There is no internal node on the signal path in the OTA, which makes the OTA to be without poles and zeros and extends the frequency range of its application [2]. These benefits make the circuit attractive for applications in HF filters and in other types of amplifiers [3-6]. Of course this way has its specific problems too – for example the tuning of OTA's G_m is more difficult.

Often band-pass and low-pass Gm-C second order filters (biquads) are based on gyrator structures due to their simplicity and less sensitive to OTA input and output impedances. However realization of more complicated biquads with complex zeros is difficult and requires extra elements [7]. Good opportunities in this case are the circuits based on two-integrator loop [1,2,7]. Filter poles in these circuits are created by the loop and then, by applying the input signal at different points of the loop, it is possible to receive a circuit with arbitrary placed transmission zeros.

A realization of such circuit with OTA created by inverters is considered in this paper. The main focus is on the investigation of the unfavorable effect of OTA input capacitances and on a way for compensating of this effect. The use of inverters for OTA is for specificity only and the received results can be applied in all cases when single stage fully differential OTA are used in the filter. The amplifier has no internal nodes on the signal path and only its external capacitances (input, output, transition) deteriorate the filter frequency response.

II. The Circuit of the Considered Biquad and some Design Outlines

The filter circuit considered here is a current-mode biquad proposed in [1] and shown in Fig. 1(a). It has several inputs and outputs. The most interesting case is when the output current is I_{o3} – then by proper choice of the magnitudes of the input currents I_{i1}, I_{i2} and I_{i3} is possible to achieve every combination of numerator coefficients. This case is used for creating the fully differential version of the circuit in Fig. 1(b). There is no second copy of OTA output currents in the fully differential version and the output current I_{o3} should be created by extra OTA, which input is in parallel to the input of OTA g_3. The conductor g_5 in Fig. 1(b) is also realized by OTA similarly to Fig. 1(a). For simplification of the next considerations, the fully differential circuit is considered as voltage-mode. Its output voltage is the voltage at the input of g_3 and the input currents I_{i1}, I_{i2} and I_{i3} are created by three extra OTAs g_{i1}, g_{i2} and g_{i3} excited by the input voltage V_i.

The transfer function of the fully differential circuit is

$$H(s) = \frac{V_o}{V_i} = k_{45}\frac{g_{i3}s^2 - \frac{\tau_1}{\tau_2}g_{i2}s - \frac{g_{i1}}{\tau_1\tau_2}}{s^2 + \frac{\omega_p}{Q_p}s + \omega_p^2}, \quad (1)$$

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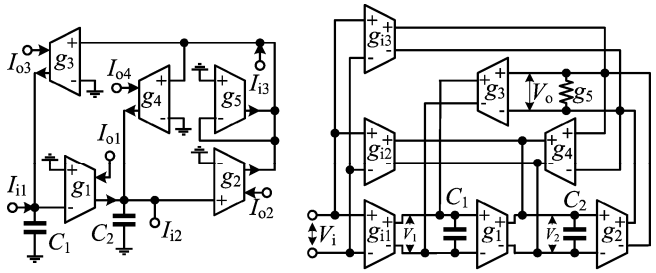
where

$$\tau_1 = \frac{C_1}{g_1};\ \ \tau_2 = \frac{C_2}{g_2};\ \ k_{45} = \frac{g_4}{g_5};\ \ k_{35} = \frac{g_3}{g_5}; \qquad (2a)$$

$$\omega_p = \sqrt{\frac{k_{35}}{\tau_1\tau_2}};\ \ Q_p = \frac{\sqrt{k_{35}}}{k_{45}}\sqrt{\frac{\tau_2}{\tau_1}}. \qquad (2b)$$

In these formulas g_{i1}-g_{i3}, and g_1–g_5 are the transconductances of the corresponding OTAs. Evidently g_{i1}, g_{i2} and g_{i3} control effectively the coefficients in the numerator. The other voltages of the circuit can be taken as output voltages too, however it is not possible to realize all classes of second-order transfer functions in these cases.



(a) (b)

Fig. 1. (a) Original single-ended circuit of the biquad. (b) Its fully differential counterpart.

There are many degrees of freedom during the circuit design – circuit elements are 9, while the coefficients of the transfer function defining the design equations are 5. Additional limitation can be introduced from the requirement for equal maxima of all OTA input voltages. It maximizes the maximum undistorted output signal and improves the filter dynamic range. Nonzero coefficient at s^2 in the numerator, i.e. $g_{i3} \neq 0$, is assumed for deriving of this condition. Then the desired transfer function can be written in the following way

$$H(s) = \frac{V_o}{V_i} = h\frac{s^2+a_1 s+a_0}{s^2+\frac{\omega_p}{Q_p}s+\omega_p^2} = -\frac{g_{i3}}{g_5}f_o(s). \qquad (3)$$

where all the parameters h, a_1, a_0 , ω_p and Q_p are defined by filter specifications. The analysis of the circuit in Fig. 1(b) gives the following expressions for the internal voltages:

$$V_1 = \frac{g_{i3}}{g_1}f_1(s)V_i;\ \ V_2 = \frac{g_{i3}}{g_2}f_2(s)V_i\ . \qquad (4)$$

The functions $f_1(s)$ and $f_2(s)$ are

$$f_1(s) = k_{45}\frac{\left(a_0\frac{Q_p}{\omega_p}-\omega_p Q_p\right)s+a_0-a_1\omega_p Q_p}{D(s)}; \qquad (5a)$$

$$f_2(s) = \frac{\left(a_1-\frac{Q_p}{\omega_p}\right)s+a_0-\omega_p}{D(s)}, \qquad (5b)$$

where $D(s)$ is the denominator of the transfer function. Evidently f_0, f_1 and f_2 depend only on the specified parameters of the transfer function and on the ratio k_{45}. Thus it is possible to find the maxima of these functions $f_{o\,\max}$, $f_{1\,\max}$ and $f_{2\,\max}$ from transfer function parameters (of course k_{45} should be chosen). Then the requirement $V_{o\,\max} = V_{1\,\max} = V_{2\,\max}$ gives two additional conditions for filter elements:

$$\frac{g_1}{g_5} = \frac{f_{1\,\max}}{f_{o\,\max}};\ \ \frac{g_2}{g_5} = \frac{f_{2\,\max}}{f_{o\,\max}}. \qquad (6)$$

These conditions together with equations (2) allow to propose the following steps for calculation the transconductances g_1-g_5 and capacitances C_1 and C_2:

1) Choice of the ratios k_{35} and k_{45}.

2) Frequency analysis of the functions $f_o(j\omega)$, $f_1(j\omega)$ and $f_2(j\omega)$ and determining of their maxima. Calculation the ratios $k_{15} = g_1/g_5$ and $k_{25} = g_2/g_5$ using formulas (6).

3) From formulas (2b): $\tau_2 = \frac{k_{45}Q_p}{\omega_p};\ \ \tau_1 = \frac{k_{35}}{k_{45}\omega_p Q_p}$.

4) Choice of C_1 and $g_1 = C_1/\tau_1$.

5) $g_5 = g_1/k_{15}$.

6) $g_2 = k_{25}g_5$ and $C_2 = g_2\tau_2$.

7) $g_3 = k_{35}g_5$ and $g_4 = k_{45}g_5$.

III. Inverter Based Fully Differential OTA

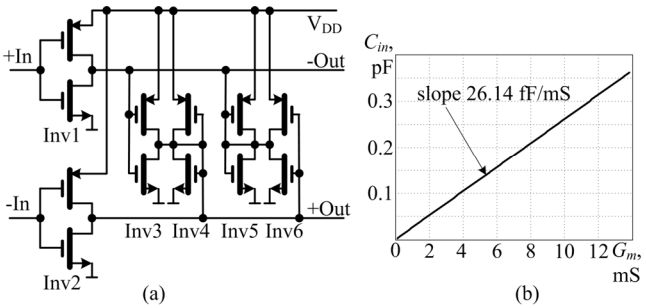
The circuit of fully differential inverter-based OTA is shown in Fig. 2(a) [2]. The amplifier is formed by inverters Inv1 and Inv2. The other four inverters Inv3–Inv6 are necessary for controlling and keeping the output common-mode voltages at the transistor drains of Inv1 and Inv2 and for reducing the common-mode gain of the circuit. The differential transconductance is [2]

$$g_{m\,\mathrm{diff}} = \left(V_{DD} - V_{th\,n} + V_{th\,p}\right)C_{ox}\sqrt{\frac{\mu_n W_n \mu_p W_p}{L_n L_p}}, \qquad (7)$$

where V_{th} is the threshold voltage, C_{ox} is the gate oxide capacitance per unit area, μ is the carrier mobility, W and L – channel width and length and the subscripts n and p relate to NMOS and PMOS respectively. The formula shows that $g_{m\,\mathrm{diff}}$ can be controlled by the ratio W/L. However the increasing of W and L increases also the gate-source capacitances C_{GS} of the transistors, as it follows from the formula [8]

$$C_{GS} = \frac{2}{3}WLC_{ox} + WC_{ov}\ , \qquad (8)$$

where C_{ov} is the capacitance due to overlapping between the gate-source and gate–drain areas. The OTA input capacitance is defined basically by C_{GS}. It follows from (7) and (8) that OTA input capacitance C_{in} and its g_m are proportional if only the channel width is varied. This is illustrated in Fig. 2(b), where the function $C_{in}(g_m)$ for the amplifier in Fig. 2(a) is shown if it is realized on AMS 0.35 µm process [9]. The simulation is done by Spectre from Cadence IC software and the transistor cannel length is assumed 1µm.



(a) (b)

Fig. 2. (a) Fully differential OTA realized with two inverters; (b) Mutual dependence between OTA g_m and its input capacitance when the transistor widths are changed simultaneously and proportionally.

The other parasitic OTA capacitances, caused by gate-drain and drain-source MOS capacitances, are much less and their effect is neglected here.

IV. Biquad Imperfection Due to OTA Input Capacitances and Its Compensation

The inspection of Fig. 1(b) shows that some of OTA input capacitances, those of g_1 and g_2, are in parallel to the capacitors C_1 and C_2 and can be considered as parts of them. Unfortunately there are several parasitic OTA input capacitances connected in parallel to g_5: those of OTA g_3 and g_4; OTA realizing g_5 itself; and input OTAs of the next stage. All these capacitances form relatively large parasitic capacitance C_5 in parallel to g_5 (Fig. 3), which may affect significantly the transfer function at higher frequencies. The filter transfer function with included effect of C_5 can be derived easily from formulas (1) and (2) if replace there g_5 by $g_5 + sC_5 = g_5(1+s\tau_5)$, where $\tau_5 = C_5/g_5$. Then the transfer function is

$$H(s) = \frac{V_o}{V_i} = k_{45}\frac{\frac{g_{i3}}{}s^2 - \frac{\tau_1}{\tau_2}g_{i2}s - \frac{g_{i1}}{\tau_1\tau_2}}{s^2(1+s\tau_5) + \frac{\omega_{p0}}{Q_{p0}}s + \omega_{p0}^2}, \qquad (9)$$

where ω_{p0} and Q_{p0} are the pole frequency and Q-factor without parasitic capacitance ($C_5 = 0$).

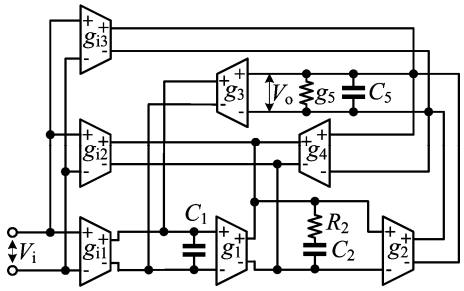


Fig. 3. The circuits of the biquad with included total parasitic capacitance C_5 and compensating resistor R_2.

The term $(1+s\tau_5)$ in the denominator represents the effect of parasitic capacitance on the circuit. It multiplies s^2 in the denominator, increasing the denominator degree by one, and the result evidently is change of the complex poles and appearance of one real pole. The influence of this term can be seen easily if calculate the changed poles at different values of τ_5 and Fig. 4 illustrates the variations of the pole parameters. It is done for normalized transfer function when the normalizing frequency is equal to initial pole frequency ω_{p0}.

Several conclusion follow from Fig. 4. The most important is concerning the circuit stability: when normalized value of τ_5 increases, Q of the complex poles increases too going to infinity at certain τ_5 and then becomes negative (Fig. 4(a)). Thus there is a maximum value for τ_5, above which the circuit is unstable. The normalized value of τ_5 is in fact the product $\omega_{p0}\tau_5$ (not normalized) and Fig. 4(a) shows existence of a limit for the frequency range of operation of this circuit. Higher pole frequency usually requires larger g_ms, which means larger OTA input capacitances – i.e. the increasing of ω_{p0} leads to increasing of τ_5.

The other conclusions are about the frequency of the complex poles ω_p and of the real pole – practically τ_5 has no effect over them. Fig. 4(b) shows that ω_p does not change for the whole range of τ_5 where the circuit is stable. The frequency of the additional real pole is approximately equal to $1/\tau_5$ and it is much larger than ω_{p0} (Fig. 4(c)) in the area of the stable circuit – thus the effect of the real pole can be neglected.

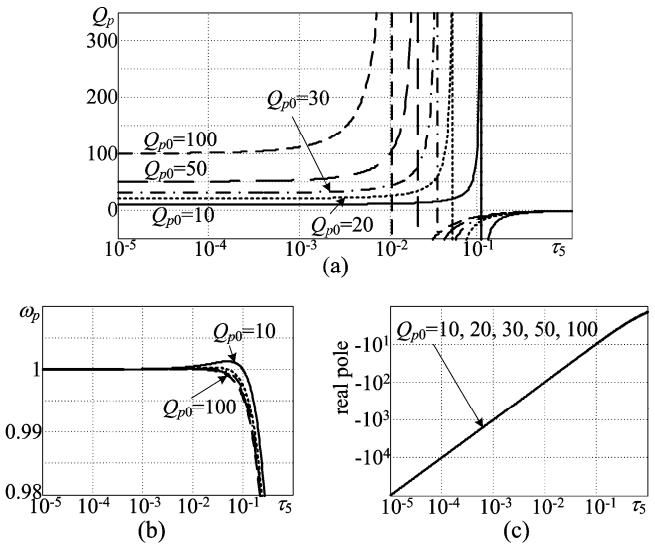


Fig. 4. Variation the pole parameters depending on normalized value of τ_5. (a) Q-factor of the complex poles; (b) pole frequency of the complex poles; (c) value of the real pole.

Fortunately there is a simple way for compensation the instability due to parasitic capacitance C_5. The voltage V_o over g_5 is defined by the output current I_2 of OTA g_2 and V_o and I_2 are in phase if $C_5 = 0$. The capacitor C_5 introduces negative phase shift of V_o. It can be compensated by introducing an opposite phase shift in I_2. This can be done by placing a resistor R_2 in series with the capacitor C_2, as it is shown in Fig. 3. Evidently the time-constants of both groups R_2, C_2 and g_5, C_5 must be equal

$$R_2C_2 = \frac{C_5}{g_5} = \tau_5. \qquad (10)$$

The transfer function of the complete circuit in Fig. 2, derived having in mind this condition, is:

$$H(s) = \frac{\frac{g_{i3}}{g_5}s^2 - \frac{g_{i2}}{g_5}\frac{1}{\tau_2}(1+s\tau_5)s - \frac{g_{i1}}{g_5}\frac{1}{\tau_1\tau_2}(1+s\tau_5)}{(1+s\tau_5)\left(s^2+\frac{\omega_{p0}}{Q_{p0}}s+\omega_{p0}^2\right)}. \qquad (11)$$

The formula indicates the instability is removed – the frequency and the Q-factor of the complex poles are returned to their initial values ω_{p0} and Q_{p0}. However the real pole still exists in the general case and the zeros of the transfer function are changed. Though the compensation is full in two important particular cases – low-pass and band-pass biquads. Then the terms $(1+s\tau_5)$ in numerator and denominator cancel themselves.

When the coefficient before s^2 in the numerator is nonzero then the desired zeros of the transfer function can be achieved by proper choice of the transcondictances g_{i1}, g_{i2} and g_{i3}. Let the specified numerator has the general form $a_2s^2 + a_1s + a_0$. The equalizing of the coefficients a_2, a_1 and a_0 to the corresponding coefficients before s^2, s and s^0 in (11) gives the following expressions for the transconductances:

$$g_{i1} = -a_0 g_5 \tau_1 \tau_2; \quad g_{i2} = -\left(a_1 g_5 \tau_2 + g_{i1}\frac{\tau_5}{\tau_1}\right); \quad (12a)$$

$$g_{i3} = a_2 g_5 + g_{i2}\frac{\tau_5}{\tau_2}. \quad (12b)$$

In these formulas is included the time constant τ_5. It is necessary to know the parasitic capacitances of OTAs g_3, g_4 and g_5 to determine τ_5, i.e. these OTAs should be designed already. Thus the design of the circuit in this case should be in three steps: 1) Calculation the values of g_1 to g_5, C_1 and C_2 based on the desired poles of the transfer function; 2) Electrical design and simulation of g_1 to g_5 and determining of their parasitic capacitances; 3) Calculation of C_5 and τ_5 and from them – R_2, g_{i1}, g_{i2} and g_{i3}. Of course this design does not remove the multiplier $(1+s\tau_5)$ in the denominator, however its effect is negligible if $\omega_{p0}\tau_5 >$ 4-5.

V. Numerical Example

The proposed design considerations are confirmed by a numerical example designing the following transfer function

$$H(s) = \frac{s^2+1.21}{s^2+0.025s+1}, \quad (13)$$

normalized to frequency of 50MHz. Its normalized parameters are: $\omega_p = 1$; $Q_p = 40$; $a_2 = 1$; $a_1 = 0$; $a_0 = 1.21$. Following the steps in Section II first are chosen $k_{35} = k_{45} = 1$. Then the calculation of the functions $f_o(j\omega)$, $f_1(j\omega)$ and $f_2(j\omega)$ by MATLAB gives $f_{o\,\max} = 8.4724$, $f_{1\,\max} = 339.47$ and $f_{2\,\max} = 8.4598$. These values give $k_{15} = 40.068$; $k_{25} = 0.99852$. The normalized time constants are $\tau_1 = 0.025$; $\tau_2 = 40$. The capacitor C_1 is chosen equal to 1 (normalized value) and for the other elements is received: $g_1 = 40$; $g_5 = 0.99831$; $g_2 = 0.99683$; $C_2 = 39.873$; $g_3 = g_4 = 0.99831$. Then the real (denormalized) value of C_1 is chosen to be 250fF, which allows to calculate the normalizing resistance $R_n = 12.732\text{k}\Omega$ and the real values of the other circuit components are: $C_2 =$ 9.9683pF; $g_1 = 3.1416$mS; $g_2 = 78.291\mu$S; $g_3 = g_4 = g_5 =$ 78.407 μS.

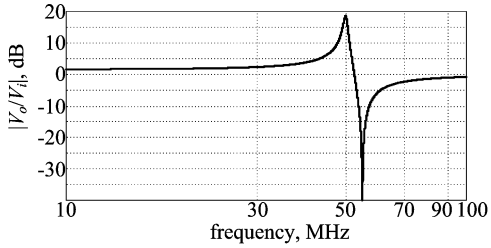


Fig. 5. Frequency response of the circuit designed in the numerical example.

Now is necessary to design the OTAs g_1–g_5 and to determine their input capacitances. Instead, here is used a simplified slightly artificial approach. The OTA input capacitances are calculated by multiplying OTA g_ms by the slope of the dependence $C_{in}(g_m)$, shown in Fig. 2(b), and the result is: $C_{in3} = C_{in4} = C_{in5} = 2.05$fF. The load capacitance is assumed 10fF and then $C_5 = 16.15$fF. The time constant τ_5 is equal to 0.206ns and its normalized value is 0.064709. The normalized poles of the transfer function without compensating resistor R_2 are -15.493; 0.19722 ± j0.99853 – i.e. the transfer function is unstable. This makes the resistor R_2 obligatory and its value, calculated from (10), is 20.663Ω. Finally are calculated $g_{i1} = -94.873\mu$S; $g_{i2} = 245.57\mu$S and $g_{i3} = 78.804\mu$S. The filter block diagram with calculated element values and included parasitic capacitance and compensating resistor is simulated by PSpice. Its frequency response is given in Fig. 5. It coincides completely with the frequency response of the specified transfer function (13) simulated by MATLAB.

VI. Conclusion

The considerations in the paper concern two problems, which appear in the design of a particular Gm-C filter. First of them is equalizing the maxima of the OTA input voltages and improving the circuit dynamic range in this way. The second problem is due to some OTA input capacitances when single stage OTA are used. Then the frequency response deteriorates at higher frequencies of operation and the circuit can be even instable, when the pole frequency is high enough. This effect exists always in this class of Gm-C filters, however it is partly masked by frequency dependences of OTA g_ms if multistage OTAs are used. A method for compensation of the effect is proposed for filters with single stage OTAs.

The filter circuit considered here belongs to the wider class of two-integrator loop second order Gm-C filters and the influence of OTA input capacitances is similar. The proposed way for its compensation is applicable for the other circuits too, of course after some modification.

Acknowledgement

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In-plane magnetosensitive double Hall device

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Abstract – **A novel in-plane magnetosensitive double Hall sensor, consisting of power supply and two identical three-contact *n*-Si cross-coupled architectures, realized in common technology process, is presented. High magnetosensitivity as well as increased metrological accuracy is achieved. The residual offset is about 160 times smaller than the internal ones. The obtained output voltage-to-residual offset ratio at magnetosensitivity of 98 V/AT (*T* = 300 K) is very promising, reaching 7.5x10^3 at magnetic induction 1T.**

Keywords – **In-plane sensitive double Hall devices, Offset and temperature drift compensation, Hall elements**

I. INTRODUCTION

Both the high accuracy and high sensitivity of magnetic-field sensors are critical in many fields of applications, like robotics, mechatronics, industrial controls, automation, etc. Unfortunately, many of the existing magnetometers do not match such high metrological requirements. For example, the presented in [1-8] magnetic-field sensors have decreased sensitivity, as only a half of the supply current is used for generating the output Hall voltage. Moreover, these devises have reduced metrological accuracy due to the both small sensitivity and the relatively high offset. The last is due to: the electrical asymmetry, caused by the geometrical imperfections in the device design; inevitable technological imprecision; mechanical and temperature, strain and stress, etc. This paper suggests a novel silicon in-plane magnetosensitive Hall microsensor, ensuring both high magnetosensitivity and increased metrological accuracy.

II. SENSOR DESIGN AND PRINCIPLE OF OPERATION

The schematic view of the *n*-Si in-plane sensitive Hall transducer is shown in Fig.1. The top-view of the double Hall device is presented in Fig.2.

The sensor consists of power supply E_s and two identical *n*-Si substrates, labelled as "1" and "2" in Fig. 1. They are established parallel to one another. On the top surface of each of the substrates, from left to right, sequentially and at distances from one another, three identical rectangular ohmic contacts are formed – C_1, C_2, C_3 on substrate 1, and C_4, C_5, C_6 on substrate 2 respectively, Figures 1, 2. The contacts C_2 and C_5 are central; the contacts C_1, C_3 and C_4, C_6 respectively are located symmetrically relative to C_2 and C_5. The power source E_s is connected to both middle contacts C_2 and C_5, Fig. 1. The first contact C_1 of the substrate (1) is connected to the third contact C_6 of the second substrate (2); the third contact C_3 of the substrate (1) is connected to the first contact C_4 of the substrate (2). The differential output of the Hall transducer is between the contacts C_1 and C_3 of the first substrate (1), or between the contacts C_4 and C_6 of the second substrate (2). The measured magnetic field $\boldsymbol{B}$ is parallel to the long sides of the ohmic contacts.

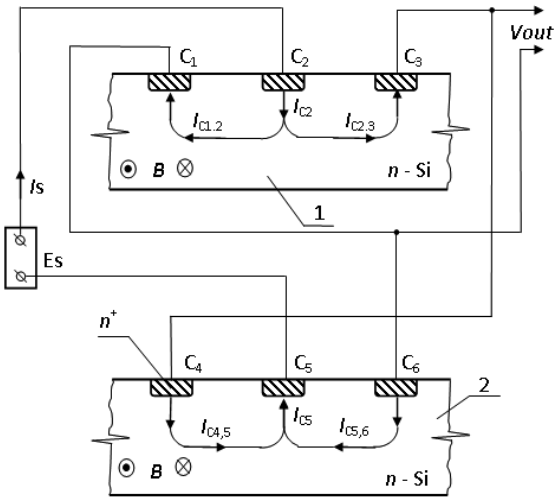

Fig. 1. Schematic presentation of the novel double Hall arrangement containing two identical three-contact cross-coupled devices.

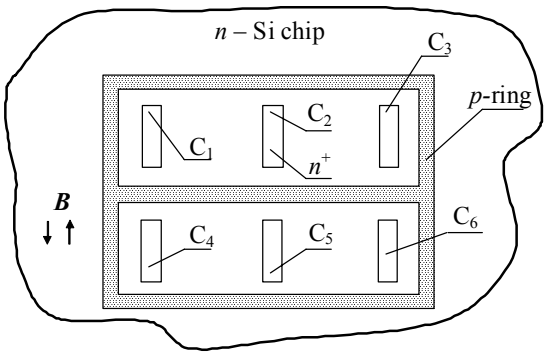

Fig. 2. Arrangement of the double Hall device. The deep p-ring enhances the sensitivity and reduces the parasitic surface current influence.

The principle of operation of the device is as follows. When power supply E_s switched on, in the bulks of both substrates (1) and (2), two equal and oppositely directed currents I_{C2} and – I_{C5} begin to flow, $I_{C2} = |- I_{C5}| = |Is|$, where I_s is the whole current, generated by the supply E_s, Fig. 1. In the absence of magnetic field, $\boldsymbol{B} = 0$, initially the current paths $I_{C1,2}$, $I_{C2,3}$, $I_{C4,5}$, $I_{C5,6}$ under equipotential highly doped n^+ contacts C_1, C_2, C_3 and C_4, C_5, C_6 are vertical,

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further they are parallel to the upper surface. It's obvious that $I_{C2} = I_{C1,2} + I_{C2,3}$, and $I_{C5} = I_{C4,5} + I_{C5,6}$. The substrates construction allows a deep current flow (about 30 ÷ 40 μm at doping concentration $N_D \approx 10^{15}$ cm^{-3}). Generally, in the absence of magnetic field $\boldsymbol{B}$ ($\boldsymbol{B} = 0$), sensor output gives a parasitic voltage (offset) V_{out} (0) ≠ 0. The last is due to: the electrical asymmetry, caused by the geometrical asymmetry in the device design; inevitable technological imperfection; mechanical and temperature stress, etc. In the suggested solution, the offset minimization (or cancellation) is achieved by the direct connection of the contacts C_1 and C_6, and C_3 and C_4 respectively, Fig. 1. This coupling causes compensating current flowing between both identical Hall structures in the absence of magnetic field $\boldsymbol{B}$ ($\boldsymbol{B} = 0$). In the presence of field $\boldsymbol{B}$ ($\boldsymbol{B} \neq 0$), parallel to the substrate plane, a Lorentz force acting on all charge carriers appears: $\boldsymbol{F}_L = q.\boldsymbol{V}_{dr}$ x $\boldsymbol{B}$, q being electron charge, $\boldsymbol{V}_{dr}$ means drift carrier velocity. The impact on the components $I_{C2} = I_{C1,2} + I_{C2,3}$, and $I_{C5} = I_{C4,5} + I_{C5,6}$, in the vicinity of the middle contacts C_2 and C_5, is crucial. The action of the Lorentz force $\boldsymbol{F}_L$ on the vertical and lateral components of drift velocity $\boldsymbol{V}_{dr}$ depends on the directions of $\boldsymbol{B}$, and currents $I_{C1,2}$, $I_{C2,3}$, $I_{C4,5}$ and $I_{C5,6}$. Due to the force $\boldsymbol{F}_L$, the trajectory of the carriers either shrinks towards the upper surface with ohmic contacts, or expands to the bulk of the n-Si substrate. As a result, on the top surfaces of both structures, additional negative or positive charges are generated. This way, the differential output of the transducer gives Hall voltage V_{out} ($\boldsymbol{B} \neq 0$), resulting from the all supply current, i.e. $|V_{out}$ ($\boldsymbol{B} \neq 0$)| ~ $\left|I_S\right| = |I_{C2}| = \left|-I_{C5}\right|$. In the known solutions [1-6], the supply current is split into two equal parts. They generate twice lower potentials on the corresponding Hall contacts (compared to the case when all supply current generates Hall voltage). This circumstance leads to reduced sensitivity as opposed to the presented in Fig. 1 solution. On the connected contacts C_1 and C_6, and C_3 and C_4 respectively, Hall potentials with the same sign and value are generated. In common case, the offset V_{out} (0) is indistinguishable from the Hall voltage. The presented solution allows reducing the offset drastically.

III. SAMPLES

3C Hall devices prototype is fabricated by means of a bipolar integrated process with four masks [9, 10]. The first mask was used to define the p-well for device isolation and parasitic surface current restriction. The second one defines the n^+ inplants for the supply current and sense contacts, to obtain a low-ohmic electrical electrode with the n-Si substrate. Masks 3 and 4 are used for the contact opening in the surface of SiO_2 layer and the metallization layer to connect electrodes with bonding pads. The n-Si low-doped wafers resistivity is $\rho \approx 7.5$ Ω.cm ($n \sim 10^{15}$ cm^{-3}). The width of the rectangular p-well surrounding rings is about 30 μm. The inner n-Si zones are of the sizes 70 x 100 μm^2, dimensions of ohmic n^+- n regions are 10 x 50 μm^2 and distance between them is 25 μm (on the mask). The overall experimental error exceeds no more than 2 %.

IV. EXPERIMENTAL RESULTS

The output characteristics of the new Hall device are shown in Fig. 3. The dependences are linear and odd. The non-linearity NL in the range $B \leq \pm$ 1.0 T reaches no more 1.3 %. The magnetosensitivity is about $S_R \approx 98$ V/AT. For the purposes of low field magnetometry, some experiments at liquid nitrogen temperatures (T = 77 K) were accomplished, using appropriate cryostat. On Fig. 4, some obtained output dependences are shown. Te sensitivity at T = 77K grew about 5 times reaching $S_I \approx 500$ V/AT.

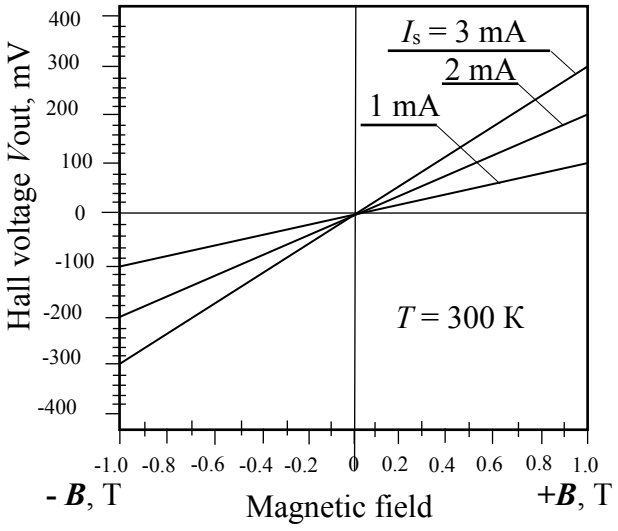

Fig. 3. The output characteristics $V_{out}(\boldsymbol{B})$.The obtained relative magnetosensitivity of the device is S_I = 98 V/AT at T = 300 K.

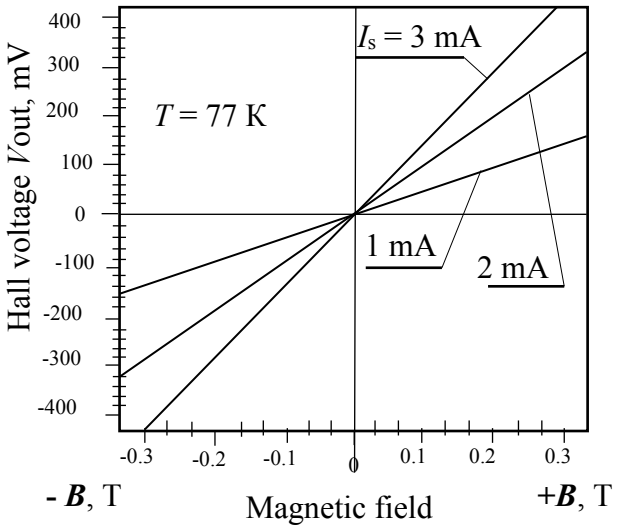

Fig. 4. The output characteristics V_{out} ($\boldsymbol{B}$), obtained at liquid nitrogen temperatures. The sensitivity is S_I = 500 V/AT

The single substrate offset temperature behavior $V_{C1,3}(0,T)$, as well as the residual offset V_{out} $(0,T)$ in temperature range -10 ≤ T ≤ 80 °C are shown in Fig. 5. The ratio K = V_{out} $(B)/V_{out}(0)$ at T = 300 K and a supply current $I_{C2} = I_{C5}$ = 2 mA is about 7.5x10^3. The offset V_{out} (0) is about 160 times less than the internal ones.

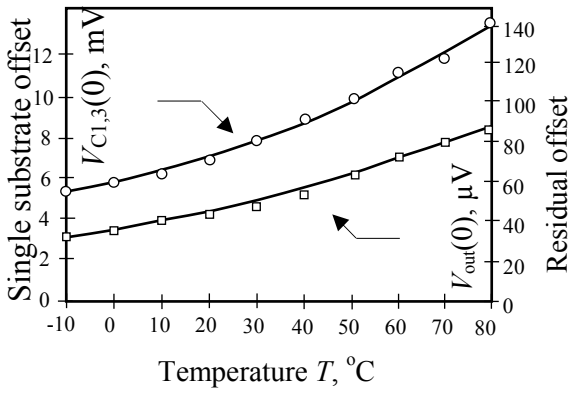

Fig. 5. Temperature dependences of the single substrate offset V_{ss} (0) and residual offset $V_{out}(0)$ of the arrangement, at a supply I_s = 2 mA.

The behaviour of internal noise is presented in Fig. 6. The noise spectral density at induction B = 0 is of the 1/f type. With the increase of bias current I_S the level of internal noise grows too. The mean lowest detected magnetic field induction B_{min} at a supply current 2 mA over the frequency range $f \leq 100$ Hz at a signal to noise ratio S/N = 1 is $B_{min} \approx 10$ μT.

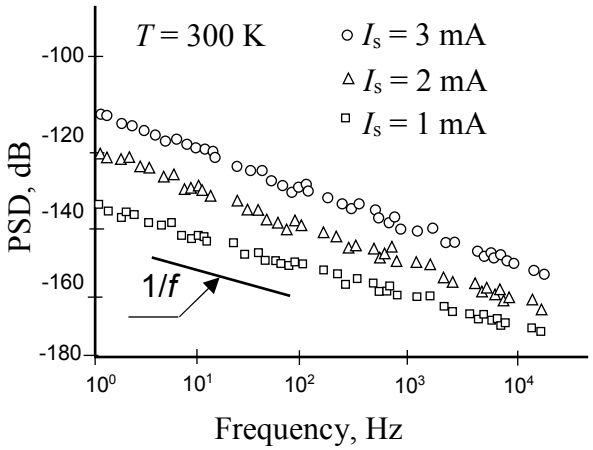

Fig. 6. Power spectral density of the internal noise of the double Hall device.

V. Conclusion

The presented in-plane magnetosensitive double Hall sensor reveals a new possibility for both additional offset reduction and transducer efficiency increase. High magnetosensitivity is achieved, due to the using of all supply current through the both central contacts for generating of Hall voltages. Also, increased metrological accuracy is realized, due to the reduced parasitic offset by the direct connection of the outside sensor contacts. The simplicity and reliability of the proposed offset cancelation technique, as well as the promising experimental results show that it may be suitable for many industrial applications. Among many others – car lock sensors for whether doors are closed, coffee machine transducers able to detect the position of the component, CPU fan sensors responsible for the fan rotation speed, washing machine detectors for the rotation of the laundry drum, level position sensor for chemistry industry plant, navigation systems for satellites, aircrafts and submarines etc.

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COMSOL Modeling of Hall Sensors Efficiency

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Abstract – **In this paper we present a finite element analysis routine for modeling of semiconductor Hall sensors. Their efficiency is studied varying the base semiconductor material. More specifically, 2D COMSOL semi-conductor model is initially employed to extract the properties of the conductive channel. Subsequently a 3D COMSOL DC model is used to perform the studies regarding the Hall sensor efficiency. Hall sensors of identical topology and doping levels are studied in a comparative manner.**

Keywords –**Hall sensors, Efficiency, Germanium, Gallium Arsenide, Indium Arsenide, COMSOL**

I. Introduction

The Hall elements are the most widespread and well technologically developed magnetic sensors. These transducers, which register magnetic fields in an extremely wide range (15-16 orders) are very universal in their applications and are in a constant development process. Their advantages are the miniature size, low price, low supply and very good technical-performance characteristics. The Hall transducers differ in structure, technology and semiconductor materials, package, number of outputs, etc. They can be orthogonal or parallel-field Hall sensors. The variety of applications imposes the development of new solutions in order to increase either the efficiency, or the reliability of such class electronic systems. The requirements to these systems are constantly increasing, regarding their versatility, functionality and compactness, as well as the quality of the magnetic sensors' characteristics and the front end electronics. Despite the enormous progress of the sensor-microelectronics, the there is still need for improvement of the parameters of magnetic sensors. Hence, researchers incessantly try to improve the sensors' topologies, materials and characteristics.

The Hall effect based sensors typically employs the well-known device topology with parallelepiped construction of very thin conducting material with two supply contacts and two output contacts. This is the geometry used by E. Hall in his experiments in 1879. The design flow of Hall sensors includes:

- Geometry optimization;
- Correct choice of materials;
- Fabrication technology

The Hall element acts as good magnetic transducer if it is manufactured from a material with low concentration of doping impurities and high carrier mobility. The only materials that meet these requirements are the semiconductors. The selected materials should respond to the following concerns [1-6]:

- Materials with low concentration of doping impurities are preferred;
- Hall voltage strongly depends on the carrier mobility, which thus need to be as high as possible;
- Carrier concentration and carrier mobility are also important for power dissipation.

Here we develop and demonstrate an analytical scheme employing finite element methods for simulation of semiconductor Hall effect sensors. Sensor performance is simulated as function of both the material properties and the device topology.

II. COMSOL Model

In order to perform the studies regarding this paper, a 2D COMSOL semiconductor model was initially employed. The purpose of this model is to extract some specific parameters for the Hall effect sensor stemming from the semiconductor properties. Figure 1 presents cross-section presentation of the studied Hall sensor topology.

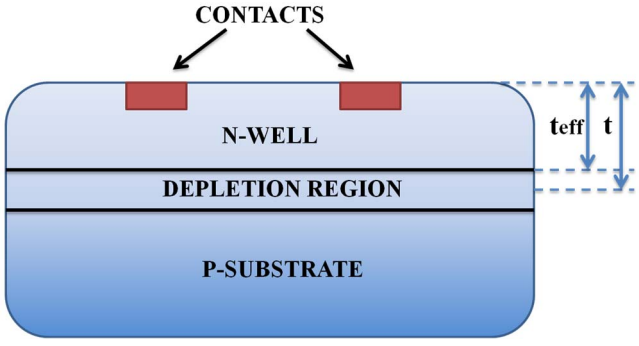

Fig. 1. Cross section view of the Hall sensor. Presented are the effective thickness of sensitive area, the depletion region and the bulk substrate

The Hall sensor is comprised of p-epitaxial layer, n-well, which serves as an active sensor area and n+ contacts. The doping levels used in the COMSOL simulations are practically relevant for the CMOS technology. 2D COMSOL semiconductor model is used to determine the electron concentration values, the conductivity of the n-

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well and the Hall coefficient for three base semiconductor materials, respectively. 3.0 V supply voltage is applied on the contacts. Simulation results are shown on Figure 2. Concentration of the electron carriers is shown with color from blue (zero) to red and dark red (maximum). The thickness of the depletion region can be considered constant in the region between the electrodes.

Fig. 2. 2D COMSOL semiconductor model of the Hall sensor. Simulation results

In Table 1 the determined parameters are presented for three base semiconductor materials, germanium (Ge), gallium arsenide (GaAs) and indium antimonide (InSb).

TABLE 1. PARAMETERS OBTAINED FROM THE 2D COMSOL MODEL

Param. / Material	N-well conductivity σ [S/m]	Electrons concentration n [1/m^3]	Hall coefficient R_H [m^3/(s.A)]
Ge	3725	5.96E22	1.05E-4
GaAs	8116	6.00E22	1.04E-4
InSb	76180	6.5E22	0.96E-4

These simulations can readily be employed in determination of the basic Hall effect parameters. The Hall voltage depends on both the Hall coefficient and the N-well conductivity. The Hall coefficient R_H is determined using Eq. 1.

$$R_H = \frac{1}{qn}, \tag{1}$$

where, q is the elementary charge and n is the carrier concentration. It is positive if the charge carriers are positive and negative if the carriers are negative. In practice, the polarity of the Hall voltage determines the sign of the main carriers. The N-well conductivity is determined through the current density per unit electric field amplitude, predicted by the model.

The above two parameters are then incorporated into a 3D COMSOL technologically constructive model (Fig. 3) of Hall microsensor, to perform the studies regarding the Hall sensor efficiency with respect to its 3D topology.

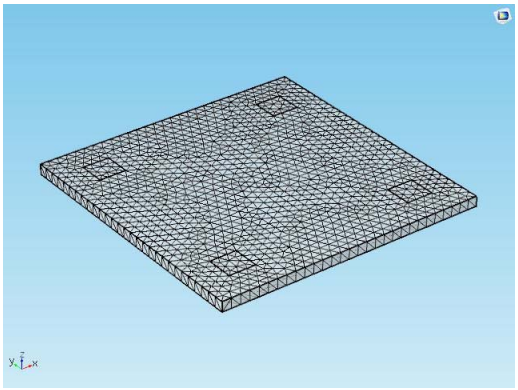


Fig. 3. 3D COMSOL DC Meshed Model of the Hall Sensor

The bias voltage is applied to two of the diagonal contacts, while the Hall voltage (output signal) is measured to the opposite diagonal contacts. The Hall device model is reduced to a square plate (see Fig. 3) with microscopic dimensions (40µmx40µm) corresponding to the N-well surface and thickness determined from the effective thickness of the N-well as determined from the 2D semiconductor model. Contacts are represented by a 6µm x 6µm contact pads ordered in a square with 4µm characteristic side. A 3V bias voltage V_{DD} is applied to the device through two of the diagonal contacts, called the input contacts. The other two diagonal contacts are placed at two equipotential points at the plate boundary and are called the output contacts or the sense contacts. The bias voltage creates an electric field E and forces a current I. If the plate is exposed to a perpendicular magnetic induction $\boldsymbol{B}$, the Hall electric field E_H occurs in the plate. The Hall electric field leads to the generation of the Hall voltage V_H between the two sense contacts.

Current flow obeys the Ohm's law in its general vector – matrix form. More specifically, the current density J and the electric field E are related through the anisotropic conductivity tensor σ represented as a 3x3 matrix.

$$\begin{bmatrix} J_X \\ J_Y \\ J_Z \end{bmatrix} = \begin{pmatrix} \sigma_{XX}\sigma_{XY}\sigma_{XZ} \\ \sigma_{YX}\sigma_{YY}\sigma_{YZ} \\ \sigma_{ZX}\sigma_{ZY}\sigma_{ZZ} \end{pmatrix} \begin{bmatrix} E_X \\ E_Y \\ E_Z \end{bmatrix} \tag{2}$$

The anisotropy in conductivity in this case is due to the Hall effect. The applied magnetic field $\boldsymbol{B}$ produces the Lorentz force on the moving electrons, and the described tensor is in this manner anisotropic. The following matrix elements are produced when B is experienced in the z direction according to Fermi gas theory of free elements [7]:

$$\sigma_{XX} = \sigma_{YY} = \frac{\sigma_0}{1+(\sigma_0 R_H B_Z)^2} \tag{3}$$

$$\sigma_{XY} = -\sigma_{YX} = \frac{\sigma_0}{1+(\sigma_0 R_H B_Z)^2}(\sigma_0 R_H B_Z) \tag{4}$$

$$\sigma_{XZ} = \sigma_{YZ} = \sigma_{ZX} = \sigma_{ZY} = 0 \tag{5}$$

$$\sigma_{ZZ} = \sigma_0 \tag{6}$$

where σ_0 is the n-well conductivity, R_H is the Hall coefficient and $\boldsymbol{B_Z}$ is the magnetic induction.

The effective thickness of the n-well is determined from our 2D semiconductor model. It represents the actual thickness of the sensitive region of the n-well narrowed by the depletion region occurring at the PN-junction (see Fig. 1 and Fig. 2) [8].

The calculated value for the effective depth of the n-well of our structure is 1.49 µm. The depth of the n-well without considering the depletion region is 1.5 µm. The effective thickness of the active area of the sensor is reduced by 0.66% because of the junction effect which is increased by the bias current.

III. Hall Sensor Efficiency

A. Materials Characteristics

The diversity of Hall sensors is enormous as well as their use. The latter imposes a large variation of specifications for these transducers, depending on the specific application. There is no universal material or topology which can be used for all of the different applications. However, a basic requirement to the Hall sensors is to posses high output voltage at low output resistance, as well as low temperature drift. With regard to these rules, the material should have high values for the Hall coefficient and carrier mobility. Metals do not manifest such properties and that is the reason why Hall effect sensors employ semiconductor materials. $A^{III}B^{V}$ materials are preferred for higher values of the Hall angle, but because of their high temperature sensitivity of the Hall coefficient, they can be used only within small temperature ranges. Another parameter which should be taken into account is bandgap width E_g, and in this respect the silicon (Si) and the gallium arsenide (GaAs) are unique materials [1].

In this paper Hall sensors of identical topology and doping levels are studied in a comparative manner with respect to the chosen semiconductor substrate. Three models with different base substrates but identical topology have been developed. Namely Hall sensors with germanium structure (Ge structure), gallium arsenide structure (GaAs structure) and indium antimonite structure (InSb structure) have been studied. The three materials are chosen in order to achieve higher sensor's efficiency. Some important material parameters are presented in Table 2.

TABLE 2. MATERIAL PARAMETERS OF SELECTED SEMICONDUCTORS FOR GALVANOMAGNETIC SENSORS AT T = 300 K.

Material	E_g (eV)	μ_n ($m^2V^{-1}s^{-1}$)	μ_p ($m^2V^{-1}s^{-1}$)	ρ (Ωcm)
Ge	0.67	0.39	0.19	45
GaAs intrinsic	1.42	0.85	0.045	7.8E7
InSb intrinsic	0.17	7.5	0.075	0.005

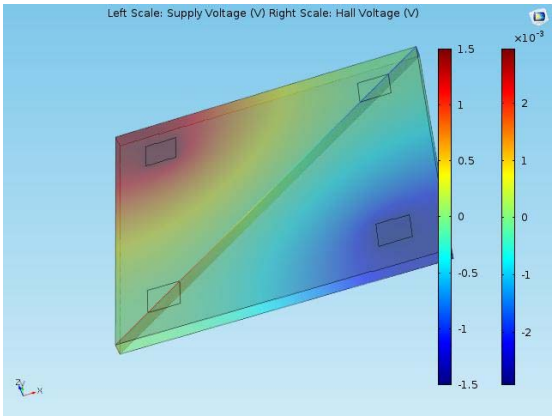
Germanium is an indirect bandgap semiconductor with a room temperature bandgap E_g = 0.67 eV. The germanium Hall element provides increased mobility as compared to its Silicon counterpart, and therefore, a more sensitive Hall effect platform.

Gallium arsenide is a very perspective material. Sensors manufactured from such base material posses linear output characteristics, wide temperature range and higher Hall voltage, because of the higher carriers mobility.

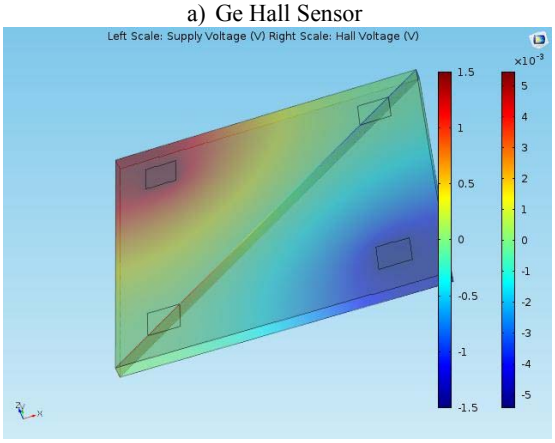
Indium antimonite gives highest output voltage because of the increased carrier mobility compared to the other materials. This material is appropriate for applications which require high sensitivity at low magnetic fields. The disadvantages of InSb element are the higher temperature dependency of its parameters and the nonlinearity of the output characteristics due to the resistivity variations as a function of the magnetic field.

B. Sensors Efficiency

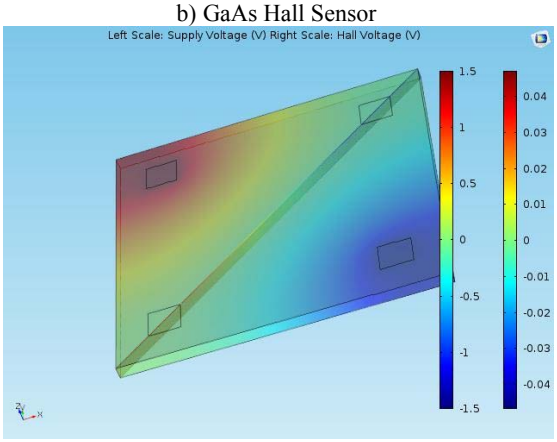
For the vast majority of applications, the key characteristics that need to be analyzed are the output signal (Hall voltage) and the magnetic sensitivity of the element. The Hall voltage is examined at supply voltage V_{DD} = 3.00 V and at magnetic field $\boldsymbol{B}$ = 8 mT. Fig. 4 illustrates the output signal as a function of V_{DD} and $\boldsymbol{B}$ for the examined materials.



a) Ge Hall Sensor



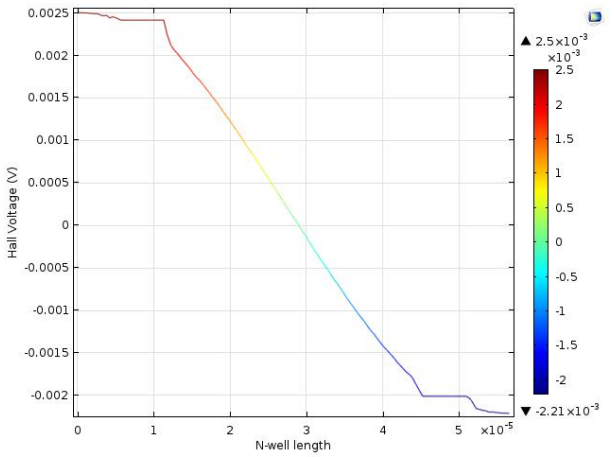
b) GaAs Hall Sensor



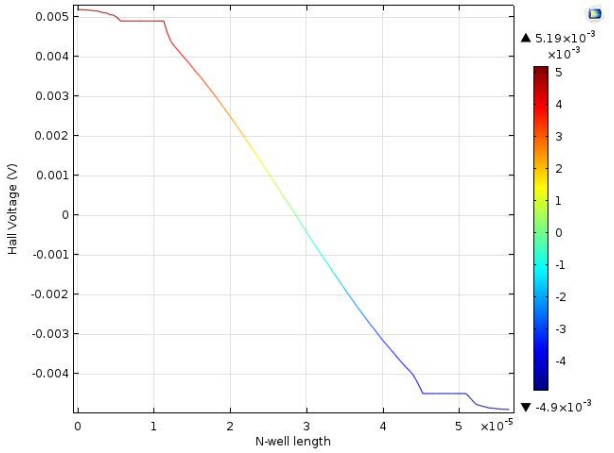
c) InSb Hall Sensor

Fig. 4. Hall Voltage for the three structures

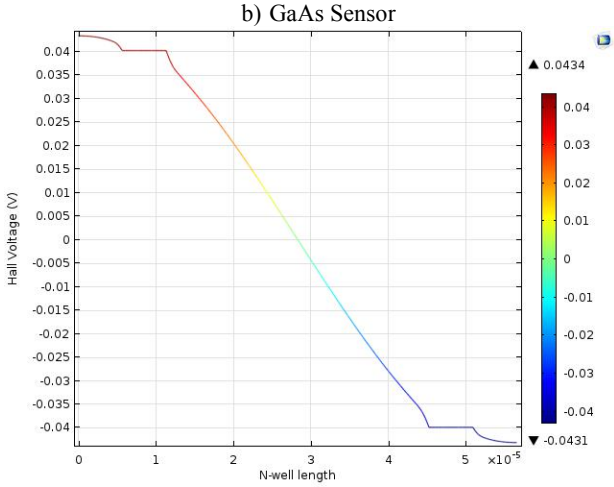
Graphical results for the Hall voltage as a function of the bias voltage and magnetic field are presented in Fig. 5.



a) Ge Sensor



b) GaAs Sensor



c) InSb Sensor

Fig. 5. Output potential for the three structures

Then, the sensitivity is calculated using (8):

$$S_V = \frac{V_H}{V_{DD} B}, T^{-1} \quad (8)$$

S_V is the voltage related sensitivity, V_H is the Hall voltage, V_{DD} is the supply voltage and B is the applied magnetic field. The sensitivity or the transduction efficiency is the most important figure of merit of solid-state magnetosensitive devices and other types of sensors. This parameter can be defined as a ratio of the output signal variation to the variation of the external magnetic field at constant environment. The calculated sensitivity (using Eq. 8) is given in Table 3.

TABLE 3. VOLTAGE RELATED SENSITIVITY FOR THE THREE BASE MATERIALS.

Material	V_{HALL} (mV)	S_V (T^{-1})
Ge	4.43	0.185
GaAs intrinsic	9.39	0.391
InSb intrinsic	80.08	3.336

The obtained results are in good agreement with data from literature. The ratio between the input parameters and the achieved output signals is proven and the developed models are adequate to the real behavior of the Hall effect transducers.

IV. CONCLUSION

In this work, a 2D COMSOL Semiconductor model and a 3D COMSOL DC model are developed and subsequently employed in a complementary manner towards the analysis of Hall micro sensors. The results for three different base semiconductor materials (germanium, galium arsenide and indium antimonide) prove that the analytical scheme proposed here is efficient and can be successfully implemented for the analysis of wide variety of Hall sensors.

ACKNOWLEDGEMENT

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Design of Cascode Current Mirror OTA in Ultra-Deep Submicron CMOS Technology

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Abstract – **The paper proposes a sizing procedure for design of cascode current mirror OTA in 45nm CMOS ultra-deep submicron technology. To this aim the basic relations in the discussed circuit are presented and a short characterization of the 45nm CMOS technology is made. The main considerations for the design of the circuit in subthreshold region of operation of transistors are pointed out and a semi-empirical sizing procedure is developed. It is applied in the design of three variants of the studied cascode current mirror OTA. The results from the simulations confirm the effectiveness of the proposed sizing procedure.**

Keywords – **Cascode Current Mirror OTA, CMOS Ultra-Deep Submicron Technology, Weak Inversion, Moderate Inversion, Subthreshold Region of Operation**

I. INTRODUCTION

The reduction of the channel length of the transistors is a leading trend in the modern CMOS technologies. Currently, the ultra-deep submicron technologies with a channel length of less than 100nm and a power supply below 1.2V are at the top of the researches. These technologies are optimized for the design of digital circuits, but pose serious problems when it is necessary to add analog and mixed circuits on the chip. This is a motive to carry out intensive researches and analyzes of the features of the ultra-deep submicron technologies, especially in the subthreshold region of operation of the transistors [1], [2], [3], [4].

The specifics of the new CMOS technologies require the search and the application of new approaches in the design of analog functional modules for large integrated circuits. The difficulties in the adequate analytical description of the operation of modern transistors are the reason for the development of experimental design approaches. For dimensioning, they use particular graphical or tabular representations, obtained by measuring of experimental samples or by simulation of the real factory models [5], [6].

Operational transconductance amplifiers (OTAs) are one of the main analog functional blocks used in the implementation of amplifiers, filters, comparators and regulators. Fig. 1 shows the current mirror OTA [7]. Its advantages are the lack of a direct connection between the output and the input of the circuit, as well as the absence of an internal high impedance node. Consequently, the output voltage swing and the frequency characteristic depend mainly on the parameters of the output stage of the circuit. The disadvantage of the circuit is the small value of the voltage gain when it is implemented in deep or ultra-deep submicron technology. The reason for this is the low output resistance of the circuit due to the relatively large channel-length modulation factor λ in short channel CMOS transistors. That's why, in case of application of ultra-deep submicron technologies, the more appropriate for use is the cascode current mirror OTA [8], shown in Fig. 2. This circuit is analyzed and tested in [9] for 1.5μm CMOS technology with power supply voltage ±3V. It demonstrates excellent amplification and bandwidth performances when the transistors operate in strong inversion (U_{GS}-U_{th}>0.1V). The imperfection in this case is the high value of the DC power dissipation P_{DISS}≈1.1mW.

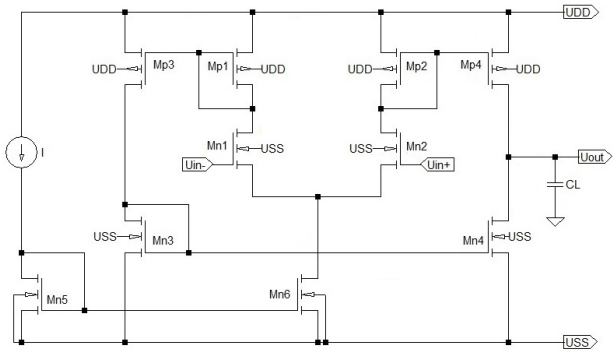

Fig. 1. Current Mirror OTA.

The formulas and design approaches used in [9] are inapplicable when ultra-deep submicron technologies are used. The low power supply voltages determine the operation of the transistors in weak or moderate inversion. This means that the values of the gate-source voltages U_{GS} are below the threshold voltages U_{th}, wherefore the transistors operate at low currents. As a result, the bandwidth and the slew rate of the amplifier are limited, but the circuit is characterized with a low power consumption.

The paper proposes a semi-empirical sizing procedure for design of cascode current mirror OTA in 45nm CMOS ultra-deep submicron technology.

For this purpose, Section II examines the operation and the main relations in the discussed OTA circuit. Section III presents important graphical dependencies between the characteristics of 45nm CMOS ultra-deep submicron technology. Section IV describes the main considerations in the design of the circuit and the proposed semi-empirical sizing procedure. Section V shows the results from sizing and simulation of three variants of the studied cascode current mirror OTA. The conclusion summarizes the obtained results.

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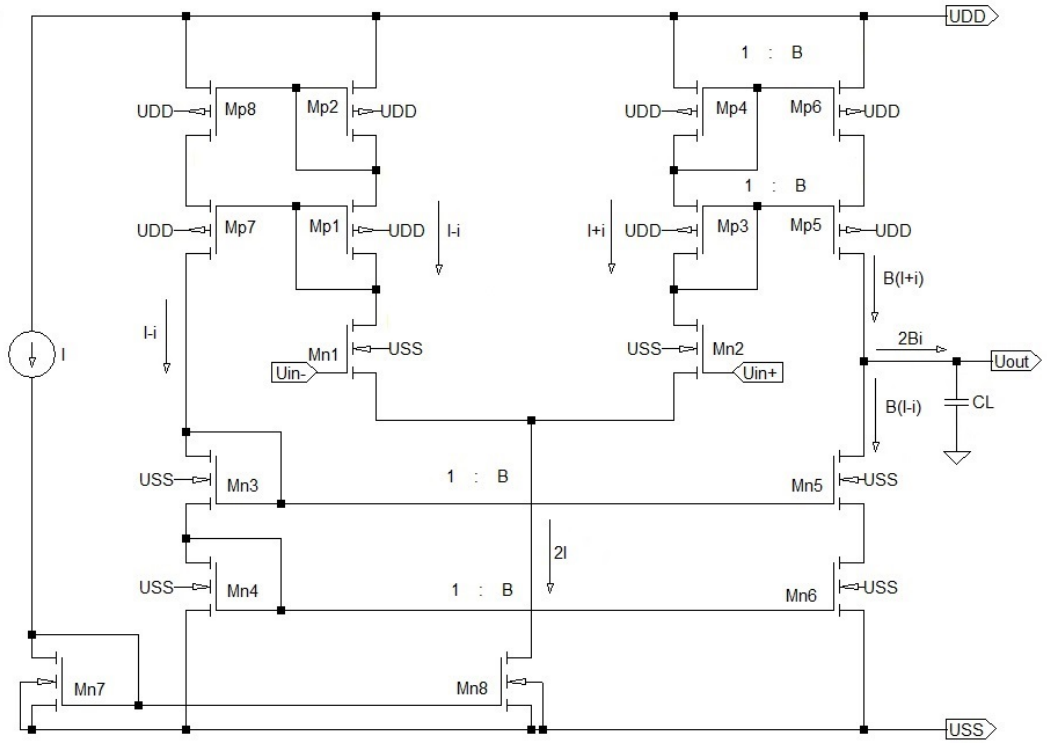

Fig. 2. Cascode current mirror OTA.

II. Basic Dependencies in the Circuit

The discussed circuit consists of two stages. The input stage (transistors Mn1-Mn2, Mp1-Mp4 and Mn8) is a differential amplifier with symmetrical output and diode-connected load for better suppression of common mode signals. The output stage is a push-pull amplifier implemented by transistors Mn5-Mn6 and Mp5-Mp6. The currents at the output stage are B times higher than the currents through Mn1 and Mn2, where B is the transfer ratio of the cascode current mirrors (Mp3, Mp4) – (Mp5, Mp6) and (Mn3, Mn4) – (Mn5, Mn6). The transfer ratio of the (Mp1, Mp2) – (Mp7, Mp8) cascode current mirror is 1.

Hence, the *ac* output current i_{out} is:

$$i_{out} = 2Bi, \tag{1}$$

where i is caused by differential *ac* input voltage u_{in}:

$$i = g_{mn}\frac{u_{in}}{2}. \tag{2}$$

In the above equation g_{mn} is the transconductance of the input transistors Mn1 and Mn2.

The voltage gain A_u of the OTA can be presented by the formula [8, 11]:

$$A_u = \frac{i_{out}r_{out}}{u_{in}} = Bg_{mn}r_{out} = \frac{Bg_{mn}}{g_{on5-6} + g_{op5-6}}, \tag{3}$$

where g_{on5-6} and g_{op5-6} are the corresponding equivalent output conductance of the series connected transistors Mn5-Mn6 and Mp5-Mp6:

$$g_{on5-6} = \frac{g_{on5}g_{on6}}{g_{mn5}};\quad g_{op5-6} = \frac{g_{op5}g_{op6}}{g_{mp5}}. \tag{4}$$

The bandwidth BW of the circuit is [8,11]:

$$BW = \frac{g_{on5-6} + g_{op5-6}}{2\pi C_L}. \tag{5}$$

The gain-bandwidth product (GBW) is:

$$GBW = A_u \cdot BW = \frac{Bg_{mn}}{2\pi C_L}. \tag{6}$$

The power dissipation P_{DISS} can be estimated by:

$$P_{DISS} = (4+B)\cdot I\cdot(U_{DD} - U_{SS}), \tag{7}$$

where I is the reference current.

III. Short Characterization of 45nm CMOS Technology

The basic characteristics of the 45nm ultra-deep submicron CMOS technology, used in this paper, are presented in [10] and examined and elaborated in [11]. The basic parameters of the technology are as follow:

nMOS: U_{thn}=0.4V; $\mu_n C_{ox}$=390μA/V^2; λ(L=90nm)=0.26V^{-1}

pMOS: U_{thp}=-0.38V; $\mu_p C_{ox}$=57μA/V^2; λ(L=90nm)=0.32V^{-1}

The power supply voltage is $\pm 0.6V$.

The condition for the common mode voltage range U_{ICM} of the circuit, when the transistors operate in a strong inversion, in a saturation, is given in [8]:

$$\begin{aligned} &U_{SS} + U_{DSn8(sat)} + U_{thn} + U_{DSn1(sat)} \le U_{ICM} \le \\ &\le U_{DD} - U_{SDp1(sat)} - U_{SDp2(sat)} - 2\left|U_{thp}\right| + U_{thn} \end{aligned}. \tag{8}$$

From (8), by replacing U_{thn}=0.4V, U_{thp}=-0.38V, $|U_{DS(sat)}|$=0.1V and taking into account the corrections of the threshold voltage of Mn1 and Mp1 (about ±0.15V), is obtained:

$$0.15V < U_{ICM} < 0.04V, \tag{9}$$

i.e. in the discussed case the fulfillment of the inequity (8) is impossible and the operation of the circuit when transistors are in a strong inversion is not feasible.

To guarantee the operation of the circuit in 45nm technology, the transistors will need to operate at gates-source voltages, lower than transistor's threshold voltages, i.e. in subthreshold region (moderate or weak inversion). In this region the transistors operate with small drain currents at comparatively large values of the width of the channels.

Fig. 3 shows the drain current I_D (the lower chart) and the transconductance efficiency g_m/I_D (the above chart) of 45nm nMOS transistor (W=1µm, L=90nm), when U_{GS} is varying between 0V and 0.4V (subthreshold region) and U_{DS}=0.3V. The dependency of the current from the gate-source voltage is exponential. In the considered range of the gate-source voltage the drain current changes between 0.5nA and 6µA. To obtain higher currents at a fixed gate-source voltage value, the width of the transistor channel needs to increase in a direct proportion to the desired current augmentation.

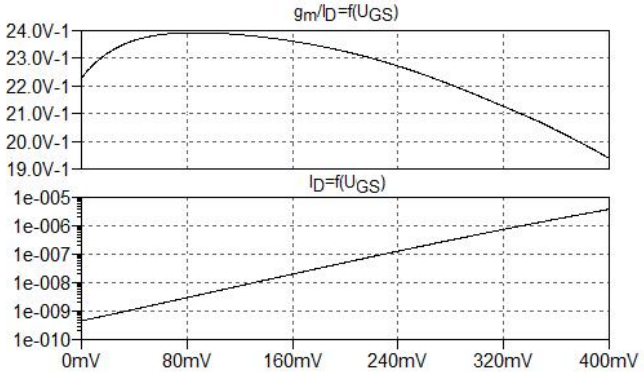

Fig. 3. The drain current I_D (the lower chart) and the transconductance efficiency g_m/I_D (the above chart) vs gate-source voltage for nMOST in subthreshold region of operation.

For the examined gate-source voltage range, the transconductance efficiency g_m/I_D changes in relatively narrow limits between $24V^{-1}$ and $19V^{-1}$. This gives the reason, in case of practical calculations in the subthreshold area, to apply the following empirical equation:

$$g_m \approx 20 I_D . \tag{10}$$

IV. Design Considerations

The sizing of the circuit can be done in several steps, based on the presented dependencies, charts and empirical equation.

Usually the design of OTA is based on the specified bandwidth GBW at a fixed maximum of the load capacity C_L. For this purpose from (6) and (10) is obtained:

$$I \geq \frac{0.1 \cdot \pi \cdot GBW \cdot C_L}{B}, \tag{11}$$

and from (7) and (11) follows:

$$P_{DISS\min} \approx (4+B)\frac{0.1 \cdot \pi \cdot GBW \cdot C_L}{B}(U_{DD} - U_{SS}) . \tag{12}$$

Below is proposed an interactive procedure for the design of the discussed cascode current mirror OTA.

1st step. Choosing the value of the current mirrors ratio.

From eq. (12) follows that when the ratio B of the current mirrors is high, the value of the power dissipation is small. Due to the hyperbolic nature of the relationship, values of the coefficient B over 8 will have low impact on the degree of reduction in dissipated power.

2nd step. Determination of a minimal value of the current I by using equation (11).

3rd step. Sizing of nMOS transistors.

In order to ensure high voltage gain at relatively wide bandwidth, the channel length of the 45nm CMOS transistors should be minimum twice large as the allowed minimum, i.e. $L=2L_{\min}$ [6].

The width W_n of the transistors Mn1-Mn4 and Mn7 can be determined by using the lower chart of Fig. 3. For this purpose, a suitable area in the subthreshold region has to be selected, for example with U_{GS} voltage values between 0.2V and 0.3V. In this area, an appropriate value of $U_{GS(sub)}$, which guarantees the operation in a weak or moderate inversion, has to be chosen. This value of the gate-source voltage $U_{GS(sub)}$ determines the current $I_{D(sub)}$. The width of the channel can be calculated by the formula:

$$W_n = I / I_{D(sub)} . \tag{13}$$

The width of the channel of Mn5 and Mn6 is B times higher than the width W_n of Mn1. The width of Mn8 is twice the width of the Mn1.

4th step. Sizing of pMOS transistors.

The sizing of the pMOS transistors can be accomplished in a similar manner as the sizing of the nMOS transistors. The channel lengths L are again selected equal to $2L_{\min}$=90nm. In the range of 0V to -0.4V the subthreshold currents $I_{D(sub)}$ vary between 70pA and 0.7µA (see Fig. 4). Depending on the selected value of $I_{D(sub)}$, the channel width may vary from several µm to several tens of µm.

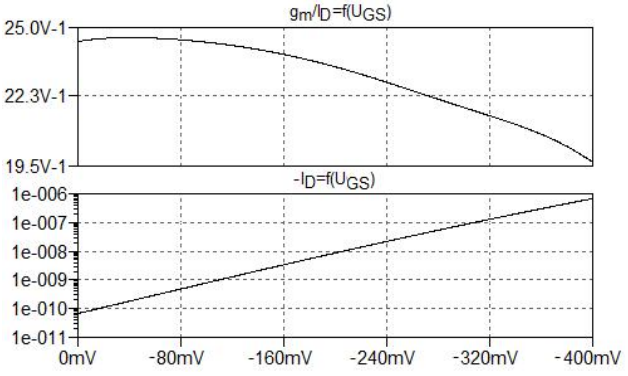

Fig. 4. The drain current I_D (the lower chart) and the transconductance efficiency g_m/I_D (the above chart) vs gate-source voltage for pMOST in subthreshold region of operation.

The advantage of the larger channel width is the low U_{GS} voltage of the pMOS transistors, which increases the allowable range of the input common mode signal U_{ICM}. The disadvantage is the increasing the value of the equivalent parasitic capacitance C_P at the output of the OTA, which is summed up with the load capacity C_L and introduces an additional bandwidth limitation.

The final choice of the channel width W_p of the Mp1-Mp4 and Mp7-Mp8 transistors is a compromise between the achievement of large input common mode voltage

swing U_{ICM} or the obtaining of low parasitic capacitance C_P at the output. The channel width of Mp5 and Mp6 is B times larger than W_p.

5th step. AC simulation of the circuit and correction of the current I.

The next step is the simulation of the dimensioned circuit and the analysis of the results for GBW product and the voltage gain A_u. Due to the parasitic capacitance C_P at the output of the OTA, the simulated bandwidth GBW′ will be narrower than desired. To achieve the requirement of the assignment, it is necessary to increase the value of current I (calculated in 2nd step) in proportion to the ratio of the desired GBW and the obtained frequency band GBW′, i.e.

$$I' = \frac{GBW}{GBW'} I \tag{14}$$

V. Design Example

In order to verify the efficiency of the proposed procedure, we will determine the sizes of the transistors of the cascode current mirror OTA circuit at values of GBW=10MHz and C_L=1pF.

1st step. In order to ensure a good geometrical matching between transistors and a relatively small value of the parasitic capacitance C_P, we choose that the value of the current mirror ratio B equals 4.

2nd step. From (11) we obtain I=785nA ≈ 800nA.

3rd step. In Fig. 3 at $U_{GSn(sub)}$=240mV the corresponding value of the current is $I_{D(sub)}$=128.68nA. Consequently, according to (13) the width W_n of Mn1÷Mn4 and Mn7 is 6.3µm, the width of Mn8 is 12.6µm and the widths of Mn5 and Mn6 are 25.2µm. All channel lengths are 90nm.

4th step. In Fig. 4 at $U_{GSp(sub)}$=-240mV, $I_{D(sub)}$ is 22nA. The channel width W_p of the Mp1-Mp4 and Mp7-Mp8 is 37µm, the channel widths of Mp5 and Mp6 are 148µm.

5th step. The simulation of the circuit with the above values of the transistor dimensions, at a common mode input voltage U_{ICM}=0V, gives the following results: GBW′=6.63MHz, A_u=62.3dB. To expand the bandwidth we increase the reference current I proportionally to the ratio of the desired and the obtained bandwidth – eq. (14). The adjusted value of the reference current is I'=(10MHz/6.63MHz)·800nA≈1.25µA. The new simulation gives GBW=10MHz, A_u=63.1dB, current consumption I_{CONS}=10µA, power dissipation P_{DISS}=12µW.

By increasing the reference current up to 1.5µA we can expand the performance of the circuit for the values of the common mode input voltage U_{ICM} up to ±0.25V (Fig. 5).

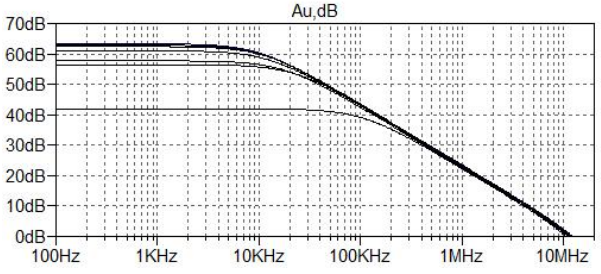

Fig. 5. The frequency response of the circuit for different values of U_{ICM} between ±0.25V.

The above procedure is used to size the circuit when B=2. The obtained results are: W_n=12.6µm, W_p=74µm, I'=2.25µA, GBW=10MHz, A_u=63dB, I_{CONS}=13.55µA, P_{DISS}=16.26µW at U_{ICM}=0V. To ensure the operation at the input common mode voltage U_{ICM}=±0.25V the reference current needs to be increased up to 2.5µA.

When B=8 the results are: Wn=3.15µm, Wp=18.5µm, I'=0.75µm, GBW=10MHz, A_u=63.3dB, I_{CONS}=9µA, P_{DISS}=10.8µW at U_{ICM}=0V. To ensure the operation at the input common mode voltage U_{ICM}=±0.25V the reference current needs to be increased up to 0.9µA.

VI. Conclusion

The paper proposes a semi-empirical procedure for sizing of cascode current mirror OTA.

To this aim cascode current mirror OTA circuit is discussed and the basic dependencies between design and circuit parameters are presented. A short characterization of the 45nm CMOS ultra-deep submicron technology is carried out and an empirical equation (10) that simplifies the sizing is proposed to be used. The design considerations for sizing the circuit at specified values of gain-bandwidth product GBW and the load capacitor C_L are dealt with in detail. A design procedure, that compensates the influence of the parasitic capacitance at the output of the circuit, is developed. The procedure has been applied in designing of three variants of the studied cascode current mirror OTA. The obtained results confirm its effectiveness.

The presented approaches can be used in the design of low-voltage CMOS circuits with ultra-deep submicron transistors operating in weak and moderate inversion.

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Replica biased complementary CMOS comparator

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Abstract - **A novel comparator based on popular self-biased complementary CMOS solution is presented and examined. Its current consumption does not depend on the process variations, the supply voltage and the temperature. This is achieved by using a replica biasing. It can provide output currents during switching, which are larger than its quiescent current, like the adaptive-biasing solutions. Simulations of schematic example confirm the proper operation of the presented comparator.**

Keywords - **comparator, replica biasing, CMOS**

I. INTRODUCTION

The analog comparators are essential building blocks in the mixed signal electronic circuits. The typical one has a differential input and a single-ended digital output. The general requirements for the analog comparators are low offset, high sensitivity and small delay*power consumption product. Insensibility to changes of the input common mode voltage is often required too. Last but not least, comparators implemented in the digital CMOS technologies need topologies able to work with low supply voltage.

The circuit presented in [1] and called by its author complementary self-biased differential amplifier (CSDA) satisfies all these requirements. The CSDA was intended originally for TTL-to-CMOS-level input buffer, but it is very popular as a comparator core [2-4]. The current consumption of the CSDA depends considerably from the process corners, the supply voltage and the temperature. This may prevent its use in applications, where low-power operation is desired. The proposed solution keeps the advantages of the CSDA and has well controlled current consumption, which is practically independent from the process corners, supply voltage and the temperature.

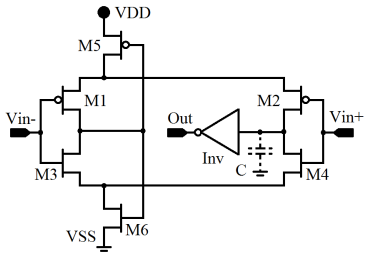

Fig. 1. CSDA based comparator

The circuit of a CSDA based comparator is shown in Fig.1. The CSDA is built with transistors M1 to M6. The inverter Inv produces a rail-to-rail voltage signal on its output and increases the load capability of the circuit. The bias current of the CSDA and hence its current consumption is determined by the dimensions of M5 and M6. In slow process corner, when the threshold voltages of the transistors are higher, the bias current decreases. The same happens when the supply voltage decreases. In the opposite case, when the threshold voltages of the transistors are lower or the supply voltage is higher, the current consumption increases. The speed of operation of the CSDA depends on how fast the parasitic capacitance C can be charged. When the bias current decreases, C is charged with less current and therefore the speed of the comparator decreases. If the bias current of the circuit in slow corner and with low supply voltage is high enough to ensure the desired speed, the current consumption will be much larger than needed in fast corner and with high supply voltage. This property of the CSDA increases its delay*power consumption product.

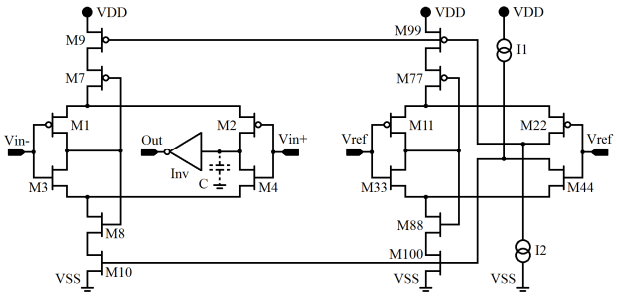

Fig. 2. Proposed comparator

II. PROPOSED COMPARATOR

The proposed circuit is shown in Fig. 2. The transistors M1 to M4 have the same dimensions like those in Fig.1. Therefore, the offset and the sensitivity of the both comparators are equal. M7 and M8 have much less overdrive voltage for the same current compared to M5 and M6 from Fig.1. This guarantees some voltage drop on M9 and M10. The transistors M11 to M100 form a replica circuit of the CSDA, which means that M1and M2 match M11 and M22, M3 and M4 match M33 and M44 and so on. The equal current sources I1 and I2 determine the current consumption of the replica circuit. Therefore, as far as these current can be kept stable, the current consumption of the circuit is independent from the other conditions. The inputs V*ref* can be connected to the input common mode voltage or to VDD/2 voltage, if the first one is not available.

The circuit operates as follows: M33, M44, M100 and I1 form differential amplifier, whose tail current is self-adjusted

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to be two times I1. M11, M22, M99 and I2 form other differential amplifier. Its tail current is self-adjusted to be two times I2. I1 and I2 are chosen identical and therefore M99 and M100 have equal currents. The mismatches between I1 and I2, M11 and M22, M33 and M44 do not affect the proper operation of the replica circuit, because of the self-adjusting tail currents. M7 and M8 control the currents of M9 and M10 to be equal by changing their drain-source voltages. Thus, the effect of the mismatches between M9 and M99, M10 and M100 is eliminated. M9, M10, M99 and M100 are dimensioned to work in triode region, which firstly makes this control easier. Secondly, it preserves the capability of the CSDA of supplying large current pulses for faster charging of the parasitic capacitance C [1]. M77 and M88 keep equal drain source voltages of M99 and M9, and M100 and M10 respectively.

III. Simulation Results

Two comparators like these from Fig.1 and Fig.2 were designed in 1.8V TSMC 180nm digital CMOS technology. The width and the length of transistors are shown in Table1 and Table2.

TABLE 1. TRANSISTORS OF THE COMPARATOR FROM FIG. 1

Name	M1, M2	M3, M4	M5	M6
Width(μm)	60	20	1	0.4
Length(μm)	0.3	0.3	0.3	0.4

TABLE 2. TRANSISTORS OF THE COMPARATOR FROM FIG. 2

Name	M1, M2	M11, M22	M3, M4	M33, M44	M7	M77
Width (μm)	60	6	20	2	6	0.6
Length (μm)	0,3	0,3	0,3	0,3	0.3	0.3
Name	**M8**	**M88**	**M9**	**M99**	**M10**	**M100**
Width (μm)	3	0.3	8	0.8	6	0.6
Length (μm)	0.5	0.5	3	3	7	7

The used minimum channel length is 300nm in order to have higher output resistance and better matching of the transistors. The bias currents in the proposed circuit I1 and I2 are 1μA each. The voltage on V*ref* is equal to the half of the supply voltage VDD. The parasitic capacitances C are set to relatively high value of 100fF. Therefore, the comparison of the circuits is at load conditions, when the CSDA uses its capability to provide currents during switching, which are larger than the quiescent current. The current consumption of the proposed circuit is smaller for bigger ratio between the currents of the comparator (through M9 and M10) and the replica (through M99 and M100). However, M11, M22, M33 and M44 have to be small devices in this cease. Therefore, the mismatch between them and M1, M2, M3 and M4 increases, which causes deviation of the comparator current from its desired value. The ratio between the currents of the comparator and the replica is chosen to be 10, which is a trade-off between these effects.

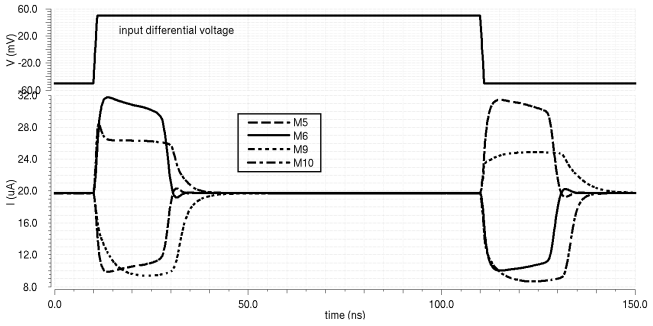

Fig. 3. Currents of M5, M6, M9 and M10

Fig.3 shows the currents of M5, M6, M9 and M10, when a differential square wave signal with amplitude +/- 50mV is applied at the input of the comparators. It can be seen from these simulation results, that the CSDA can supply larger current pulses for charging of the parasitic capacitance C. But the proposed solution has still this feature, despite it uses constant bias current.

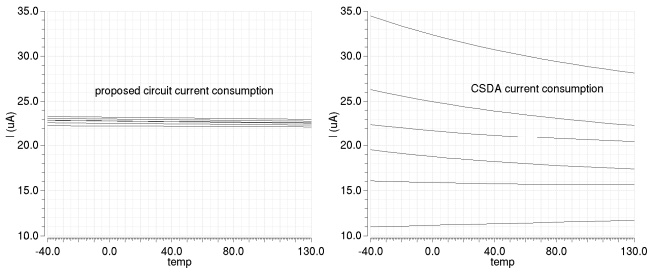

Fig. 4. DC current consumption of the comparators

Fig.4 shows the DC current consumption of the comparators (without the invertors) for three process corners (nominal, slow, fast) and two supply voltages (1.7 and 1.9V) when the temperature changes from -40 to 130°C. The current consumptions are between 11 and 34μA for the CSDA and between 22 and 23μA for the proposed circuit.

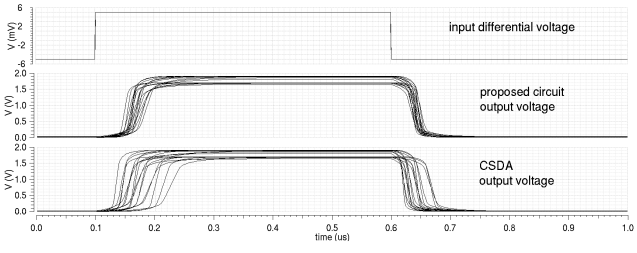

Fig. 5. Delay of the comparators

Fig.5 shows the switching speed of the comparators for three process corners (nominal, slow, fast), two supply voltages (1.7 and 1.9V) and three temperatures (-40, 30, 130°C). The amplitude of the input square wave signal is +/- 5mV. The delays are between 20 and 123ns for the CSDA and between 35 and 86ns for the proposed circuit.

It can be seen from these simulation results, that first the variation of the DC current consumption of the proposed circuit is about 20 times smaller. Second, for a given maximum DC current consumption the proposed circuit will has less delay in worst case (slow process corner and low VDD). The worst case delay*power consumption product of the CSDA and the proposed circuits is 123ns*1.9V*34µA = 8pJ and 86ns*1.9V*23µA = 4pJ

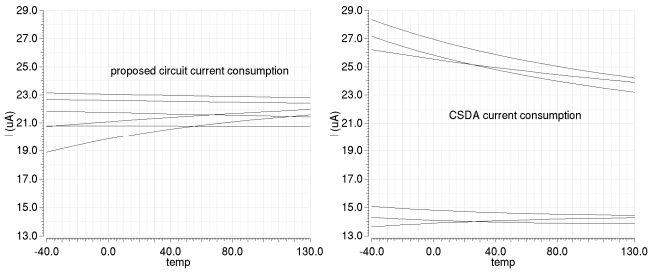

Fig. 6. DC current consumption of the comparators with different input common mode voltages

Fig.6 shows the DC current consumption of the comparators (without the invertors) for two process corners (slow and fast) and three input common mode voltages (750, 900, 1050mV) when the temperature changes from -40 to 130°C. The current consumption is between 13 and 15µA at slow corner and between 23 and 29µA at fast corner for the CSDA. It is between 19 and 23µA for the proposed circuit.

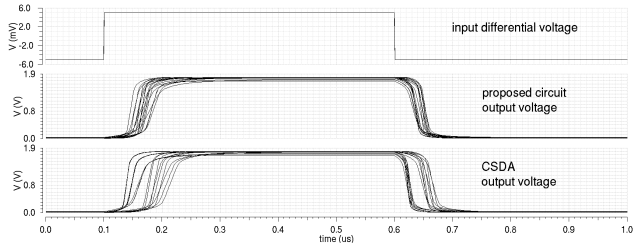

Fig. 7. Delay of the comparators with different input common mode voltages

Fig.7 shows the switching speed of the comparators for two process corners (slow and fast), three input common mode voltages (750, 900, 1050mV) and three temperatures (-40, 30, 130°C). The amplitude of the input square wave signal is +/- 5mV. The delays are between 20 and 115ns for the CSDA and between 31 and 86ns for the proposed circuit.

It can be seen from the simulation results that the proposed circuit keeps the good insensibility to changes of the input common mode voltage of the CSDA. This insensibility can be further improved, if the input common mode voltage is available and V*ref* is connected to it.

IV. Conclusion

An alternative of the CSDA based comparator using replica bias is proposed and compared with. Lower worst case delay*power consumption product is achieved by keeping the current consumption of the circuit almost constant by the replica biasing. The offset, the sensitivity and the insensibility to changes of the common mode input voltage of the comparator are identical to these of the CSDA based solution. The proposed circuit can provide large current pulses during switching like the CSDA, as well. Simulations of implementation in 180nm CMOS technology confirms the concept and shows two times improvement of the worst case delay*power consumption product of the comparator.

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A Fast Comparator with Integrated Small Dual Hysteresis and Offset Control

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Abstract – **This paper presents the design of a fast comparator, where the dual hysteresis and the digital offset control are integrated in a source degenerated preamplifier stage. The selected architecture of the preamplifier stage, followed by a differential symmetrical OTA allowed easily to be achieved design requirements as 8mV hysteresis, 1σ input random offset of 0.58mV, range of ±35mV additional digital offset control with 5mV step, 30ns propagation delay, while the power dissipation is 90µW and the block area is 0.015mm^2 at 0.18µm CMOS technology. The source degenerating resistors in the preamplifier stage can be used to create dual or single, digitally programmed hysteretic comparators.**

Keywords – **comparator, hysteresis, source degeneration, low offset**

I. Introduction

Comparators are widely used in almost all electronics circuit, at the place where the analog signal – voltage or current, has to be converted to a logical level (‘1’ or ‘0’), which to be used in the circuit’s functional control. The comparators are considered as a 1-bit analog-to digital converter and are an important part of every ADC. The application of the voltage comparators varies from those in the ADCs, to be part of integrated circuits (IC) input-output (I/O) interfacing modules, power levels detection and control, sensor interfaces, clock generation and extraction from an analog and/or a noisy signal and others.

The comparator circuit, presented in this paper, is designed to extract a clock signal from differential sinewave signal. Due to specific application requirements, the output clock signal shall have minimum delay in respect to the input signal. This respectively defines the need of fast, low noise, a low offset and low hysteresis comparator. In addition, there should also be considered the typical for the business requirements of having minimum physical size and current consumption, which is usually achieved by selecting the simplest and minimal as number of transistors structure.

II. Preliminary Work

The input signal can be unipolar - referred to ground or supply, or differential, when is floating in respect to supply lines or analog ground. The input signal is compared to the reference signal and when the difference between input signal and reference is higher than the comparator intrinsic offset and minimum overdrive comparator input voltage, the comparator output is set to a logic level ‘1’, or ‘0’ if it is inverting. The comparators have to compare the input signal as quick as possible and to give at the output the sign of the change. They are usually built from high gain open loop amplifiers, which do not have miller compensation, in order to have as fast reaction as possible. Therefore, they are sensitive to noisy spikes through power lines, coupled disturbance, slow input signal change and any non-filtered noise in the input signal. To decrease or remove the unwanted switching at the comparator output, in the comparator circuit is added hysteresis. The changing reference level can be built by a positive feedback, where the reference switching point is the resistor divider proportion of output signal or supply voltage. There are many examples given in [2] and [3], frequently used in the practice due to the process and temperature independent hysteresis, which is a function of the resistors ratio and reference (or supply) voltage. However, no one of these solutions is in the same time with a high impedance input and for a differential signal.

One of the most popular used in practice IC comparator circuit is the symmetrical OTA with small positive feedback in current load of the first stage that forms the hysteresis [1], [5]. The benefit of this circuit is the simplicity of the circuit, leading to an easy design and a good scalability in respect to the layout size, speed and current consumption. This circuit has also symmetrical rise and fall propagation delay time, which is a key requirement for comparators used for extraction of time related parameters. The drawback of using this circuit is the small gain of the first stage, which respectively leads to more noise and offset contributors. The other limitation for some applications might be that the hysteresis is process and temperature dependent [5]. In some solutions is used unbalanced differential pair [6] to create the necessary hysteresis, but the performance of these circuits is again sensible to process variations. The proposed in [5] solution shows a good linearity and possible programing of the hysteresis in a wide range, but requires an additional circuit in order to provide the hysteresis control reference voltage. There are many comparators solutions, where for making a scalable and process independent hysteresis is used a two-differential pairs input amplifier [4], where at one of the input differential pairs is applied the processed differential signal, and at the other - the differential signal equal to the hysteresis voltage. However, these solutions can result to an increased area, current consumption, an offset and noise.

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III. Design of The Proposed Circuit

The simplified view and the principle of operation of the proposed circuit is presented at Fig.1. The ideal comparator output will change from '0' to '1' when the signal difference at the comparator inputs has a positive sign ($V_{INP} - V_{INN} > 0$), and respectively from '1' to '0' when it has negative sign. If the comparator has an internal offset, this will change the moment of switching of the comparator output – see Fig.1(a). In the hysteretic comparator, the wanted output change from '0' to '1' is when the input differential signal is positive and bigger than V_{hyst+} ($V_{INP} - V_{INN} > V_{hyst+}$). It is equivalent of having VDC source creating an offset with the same value ($V_{OS} = V_{hyst}$), and with a negative sign if it is connected to the positive input, or a positive sign if it is connected at the negative input. At '1' to '0' transition, the input differential signal has to be negative and with an amplitude higher than V_{hyst-}, which makes the comparator a dual hysteresis type. To make V_{hyst-} can be used a negative offset at V_{INP} or a positive offset at V_{INN}. In the proposed circuit are used two positive offset shifts to make the V_{hyst+} and V_{hyst-}. The selection of a positive or a negative hysteresis is controlled by the last comparator output state (Fig. 1(b)).

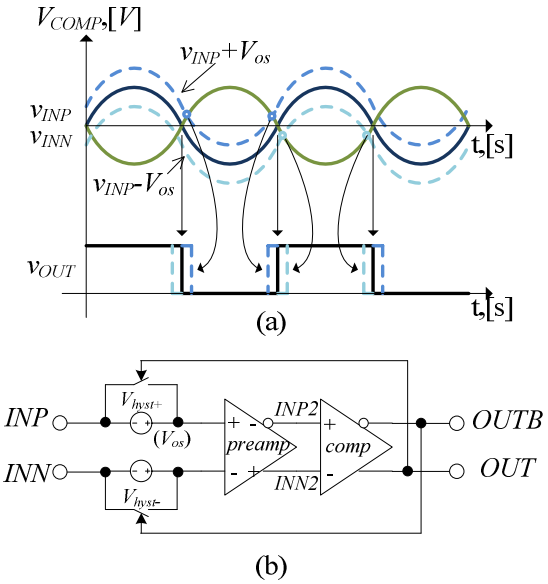

Fig. 1. (a) A base idea of the operation and (b) a simplified view of the dual hysteresis comparator.

The presented comparator consists of a pre-amplifying differential input, differential output stage, a differential to a single ended stage, invertors and a feedback to control the hysteresis. The pre-amplifying stage is a CMOS common source with a resistive load and degenerating resistors at the sources, whose structure has decreased gain, but offers a wider linear range compared to the traditional transistors only gain stage. The degenerating resistors are used for hysteresis creation and for the programmed offset. The second stage is implemented as a two-stage differential-to-single-ended OTA. The function of this stage is to amplify the shaped input signal and to make the conversion from an analog to a digital signal. The inverters function is to increase additionally the driving strength of the comparator output and to provide signals for hysteresis control. The circuit integrates the hysteresis reference, which is in function of a resistor and the input bias current of the comparator. To achieve process, voltage and temperature (PVT) independent hysteresis, the bias current generator has to be based on a PVT independent voltage reference (like bandgap) and a resistor of the same type, which is used in the preamplifier stage.

A. Common Source Amplifier with Degenerating Resistors

The hysteresis can be considered as an offset, which is added at the positive or at the negative input of the amplifier where the selection of the offset is being controlled by the last output state of the comparator – Fig.1 (b). Instead of using an external voltage reference, where to be selected the right offset at the right moment, it can be considered of moving the offset at the transistors source – see Fig.2.

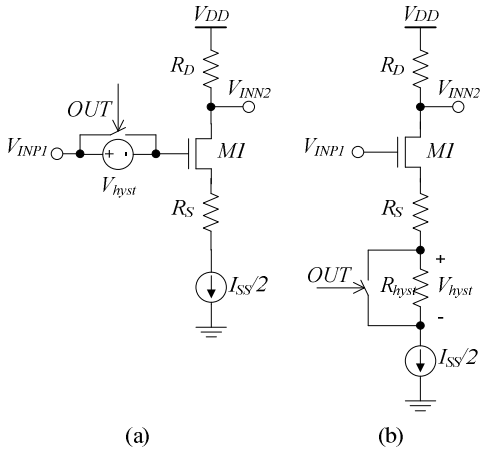

Fig. 2. (a) A common source with a degenerating resistor with external and (b) integrated hysteresis – a half of differential pair.

The offset is integrated into the comparator, but it will also appear with an inverted sign. That offset voltage, or the hysteresis, can be created by a resistor (R_{hyst}) and the nominal current ($I_{SS}/2$) biased via the transistor from the differential pair (see Fig. 2). In this way, the hysteresis voltage at the transition moment is calculated by Eq.1:

$$V_{hyst} = R_{hyst}\frac{I_{SS}}{2} \tag{1}$$

The common source and the common emitter differential amplifiers with degenerating resistors are widely used in the practice for operational amplifiers offset trimming. This type of amplifiers, compared to the one without resistors in the source, has an increased ac output resistance and linearity range, with the cost of slightly increased noise and a decreased output swing range. The small signal dc gain of the common source stage with a degenerating resistor A_{dc}, neglecting the effect of the transistors bulk biasing, is given by Eq. 2:

$$A_{v,dc} = -\frac{g_{m1}R_{out}}{1+g_{m1}R_S} \approx -\frac{g_{m1}R_D}{1+g_{m1}R_S} \tag{2}$$

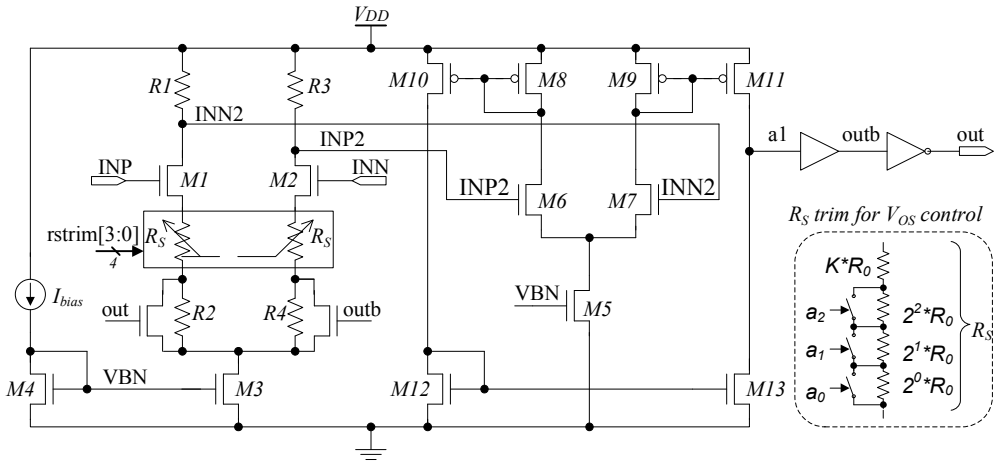

Fig. 3. Final schematic of the comparator

The R_S in Eq.2 represent the sum of the seri-connected resistors in the source, whose value will change when the hysteresis-forming resistor is bypassed by a switch. The R_{out} represents the equivalent output resistance seen at the drain of M1.

The gain of common gate amplifier is with the same as magnitude as the common source, but with a positive sign. This additionally proves that the required offset shift can be added at the gate or at the source of the summing transistor.

As it was mentioned above, the drawback in that circuit is the decreased output range, which has to be known in order to be estimated the gain of the stage, then the respective circuit components to be sized. The maximum output level, due to the resistive load, is the V_{DD} supply voltage. The equilibrium output voltage $V_{OCM,eq}$, when there is no input differential signal, is defined by the half of tail current I_{SS} and R_D - Eq. 3:

$$V_{OCM,eq} = V_{DD} - R_D \frac{I_{SS}}{2} \quad (3)$$

The minimum output voltage has to guarantee that the transistors in the differential pair M1 (M2) and the tail current source transistor M3 stay in saturation. This means that their drain-source voltage is not lower than the overdrive, or effective voltage $V_{eff,M1}$ for M1 and $V_{eff,M3}$ for M3. The minimum output voltage is at the differential pair transistor that is conducting the whole bias current I_{SS}, while the other is fully off. At this case, the overdrive voltage $V_{eff,M1}$ will be increased by a factor of $\sqrt{2}$. Considering also the voltage drop over the R_S resistor, for the minimum output voltage there has to be guaranteed that:

$$V_{O,min} = V_{DD} - R_D I_{SS} > \sqrt{2} V_{eff,M1} + R_S I_{SS} + V_{eff,M3} \quad (4)$$

The minimum input common mode range can give the possible offset trim range and the hysteresis size, also the maximum input differential signal, which can be linearly converted to the output. Considering that due to the hysteresis selection, the equivalent resistance in the source R_S will decrease, when one of the hysteresis forming resistor is shorted, the input linear range will be defined in the same portion from the input transistor, where the input ac signal v_{id} has to be smaller than the effective voltage of the transistor $V_{eff,M1}$. Substituting v_{id} by $V_{eff,M1}$, for the minimum input common mode voltage is calculated:

$$V_{ICM,min} > V_{th} + V_{eff,M1} + R_S \frac{I_{SS}}{2} + V_{eff,M3} \quad (5)$$

The input/output common mode range can be extended if necessary by splitting the tail bias current in two and using the half of the same resistor between the two sources. This will eliminate the decrease of the output voltage swing due to the R_S, but with increase of the noise and offset, as it cannot be considered that both current sources are fully correlated. For the used circuit, the equivalent input voltage noise at low and moderate frequency is given by Eq. 6:

$$V_i^2(f) = \frac{K}{WLC_{oxf}} + \frac{8kT}{3g_{m1}} + 4kTR_S + \frac{4kT}{R_D}\left(\frac{1+g_{m1}R_S}{g_{m1}}\right)^2 \approx \frac{K}{WLC_{oxf}} + \frac{8kT}{3g_{m1}} + 4kTR_S\left(1 + \frac{R_S}{R_D}\right) \quad (6)$$

As can be seen in Eq. 6, for high g_{m1}, the main contributor of the noise is the degenerating resistor R_S.

The input referred random offset voltage is also estimated to be mainly dependent from the transistors in the differential pair, which is given by Eq. 7:

$$\sigma(V_{os}) = \sqrt{\frac{A_{Vth}^2}{WL} + \left(\frac{\Delta R_S}{R_S}\right)^2 \left(\frac{I_{SS}}{2}\right)^2 + \left(\frac{\Delta R_D}{R_D}\right)^2 \left(\frac{1+g_{m1}R_S}{g_{m1}}\right)^2} \quad (7)$$

The trimming of the offset is shown at Fig. 3. By selecting the binary scaled resistors only on the left or only on the right side is achieved a positive or a negative static offset. In the presented case, the programmable offset voltage step is 5mV, and by 4 bits is covered +/-35mV offset voltage range.

B. Final Design of Proposed Circuit

The second stage target is to provide the necessary gain and the minimum propagation delay time. The delay time can be in function of small signal parameters of the gain stages or to be slew rate limited. It can be assumed in case that most of the capacitances are small, the currents are not

so small and the delay is not slew rate limited. Therefore, for evaluating and optimizing the delay, the small signal parameters of the amplifier transfer function will be used. The most high-impedance node can be suggested that is at a differential OTA output. The other high-impedance node with a relatively high load capacitance is at the output of the preamplifier stage. If the time constant of the first node is noted with τ_1 and the other with τ_2, the time dependency of the output voltage $v_{out}(t)$ in function of the input signal V_{in}, the dc gain of the two amplifiers A_0 ($A_0 = A1_{v,dc}A2_{v,dc}$) and the dominant time parameters is given by Eq. 8:

$$v_{out}(t) = V_{in}A_0\left(1 - \frac{\tau_1 e^{-\frac{t}{\tau_1}}}{\tau_1-\tau_2} + \frac{\tau_2 e^{-\frac{t}{\tau_2}}}{\tau_1-\tau_2}\right) \quad (8)$$

To find the delay time for $t = t_d$, the Eq. 8 has to be solved for the output signal equal to the half of the supply ($v_{out}(t) = V_{DD}/2$) or a smaller output swing, considering that the next invertors will provide the necessary output swing to supply.

At Fig. 4 are presented simulation waveforms, where for demonstration purpose the hysteresis was changed from 8mV to 50mV.

After designing the first version of the comparator, the design of the circuit can be optimized additionally by the use of the Eq. 1 to Eq. 8. The final circuit will require adding of a current consumption enabling logic, including a default "off" output sate, which are not shown in the schematics at Fig.3. During the layout design, it has to be considered the potential risk of kick-back noise or current coupling from the fast, digital output buffers back to sensitive analog part, where these high disturbing currents can be passed back through the power supply lines or parasitic wires' capacitances.

IV. Simulation and Experimental Results

The presented comparator architecture is designed at standard 0.18µm CMOS technology, with 1.8V±0.1V supply and temperature range of (-50÷150) °C. The input common voltage is half of the supply – 0.9V±50mV, which for this technology, where V_{th} is about 0.55V, limits the possible linear input signal range to ±100mV. In the designed case, the I_{SS} current is 10µA, R_D is 95kΩ, R_S is programmable in the range of (3÷10) kΩ with 1kΩ step, where R_S is 10kΩ for 0 offset case and 3kΩ is for the 35mV case. The offset control was targeting introducing of a small phase shift, at small steps, positive or negative, in the extracted clock signal. The small input hysteresis voltage is made by the integrated R_{hyst}=1325Ω. The typical gain of the preamplifier stage is about 4.5 and it increases when the selected offset decreases R_S. This behavior was confirmed during the offset step measurement, where for a higher offset step was observed offset drift with temperature and supply. At the minimum offset step, the random offset drift was zero, while at the maximum offset step (35mV), it was rising for some devices up to 2mV. The DC gain of the comparator is above 20kV/V, where 1kV/V is from the preamplifier and differential to single-ended comparator. The simulated 1σ input random offset is 0.58mV and 145 µV 1σ difference between the positive and negative hysteresis. The input voltage noise at 1Hz is below 3µV/sq(Hz). The achieved propagation delay time is 34ns maximum, fully symmetrical for the rise and fall signal. The worst PVT case simulated power dissipation is 90µW for 20kHz input signal. The maximum simulated operating frequency with 1mV input signal (1mV above V_{hyst}) is 7MHz, and for a higher input signal amplitude can be extended to 30MHz. The final block area is 0.015mm2.

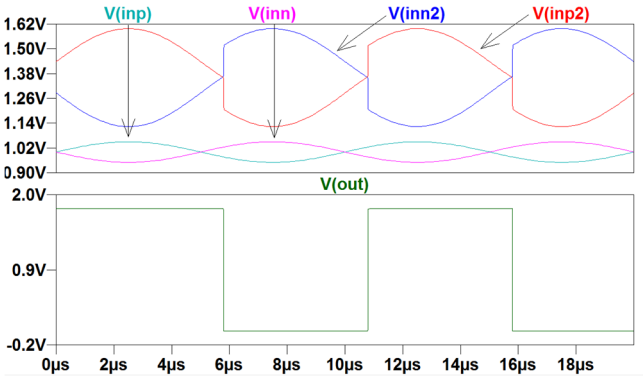

Fig. 4. Simulation waveforms

V. Conclusion

This paper dealt with the design of a fast differential input comparator, with an integrated small hysteresis and a digitally programmed offset, with low noise, an offset and a reasonable small area and power dissipation. The presented architecture provides an easy integration of a digitally programmable offset and/or a hysteresis, which can be quite stable over PVT as their values are based on the input bias current and resistor. The provided equations of the main DC and time comparators parameters can be used for an optimal circuit design.

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Mixed signals technique for offset reductions

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Abstract – **This article, discusses the problem with the influence of offset voltages and their drives generated in the measuring system in the process of forming a digital equivalent to a pre-formed value. A method and a schematic solution are proposed to reduce the total offset voltages in a measuring line, based on the mixed signal technology. Its limitations have been defined in relation to transformation time intervals and generated internal parasitic charges. It's explored a methodology for the construction of a measurement unit, minimizing to the noise level the impact of the offset voltages in the whole measuring system. The sources that cause noise components in the digital output are defined and the guidelines for their minimization are specified.**

Keywords – **mixed sgnals**, **measurement, offset voltage, noise, digital filtering.**

I. INTRODUCTION

In devices for perception of analogue information from objects, errors can be caused by offset voltage at many points in the channel of the circuit in the perception and processing of relatively weak signals. For example, a voltage rise from the temperature. Thermocouple, due to temperature difference, when two different metals are connected - inevitable in real physical realization.
Within even an integrated circuit, such as an ADC with its own internal amplifier and a S & H circuit, there are a number of sources of internal offset errors caused by incoherence between the individual steps, the parasitic charge injection processes on a capacitor in the pass-through sampling process, In memory mode or external interference voltages from electromagnetic processes or radiation.

II. PROBLEM FORMULATION

Increasing resolution results in drift offset problems because applying a zero-time reset is no longer sufficient to eliminate these offset errors by all the factors that cause them in the digital equivalent of the Dig {U} signal.

Particularly difficult is the problem when, as a result of digital conversion monitoring of two analog values, a numerical expression of their ratio should be given as a correction signal for a process as shown by formula (1).

$$K := \frac{Dig\left\{\left[U_{IN}^{A}(+) - U_{IN}^{A}(-)\right] \pm U_{IO}^{A}\right\}}{Dig\left\{\left[U_{IN}^{B}(+) - U_{IN}^{B}(-)\right] \pm U_{IO}^{B}\right\}} \qquad (1)$$

The problem of overlaid offset in the measured values, and especially in relatively weak signals, can lead to generally uncontrollable erroneous results and unpredictable follow-up from them.

The offsets and their drives that occur within the various ADC amplification circuits, can be reseted by "chopping" technology or "auto-zero" technology applied to the amplification circuits [1].

The implementation of the "auto-zero" principle in its two main classical variants is shown on Fig. 1 for an open offset compensation circuit, and in Fig. 2 for offset compensation for an closed circuit [2]. Typically, this is accomplished by interrupting the input process for compensation purposes

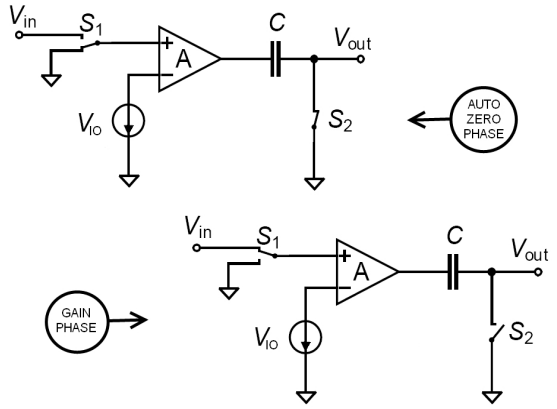

Fig.1. Circuit implementations of the auto-zero with open-loop offset-compensation.

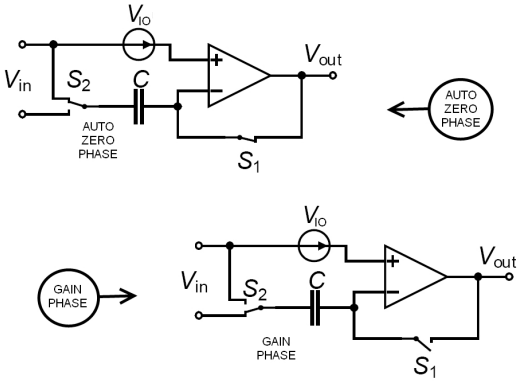

Fig.2. Circuit implementations of the auto-zero with closed-loop offset-compensation

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This approach, in principle, leads to the loss of part of the current information from the signal in the time domain of compensation. This is the "auto -zero" phase, in this phase the offset quantities are compensated subsequently in the normal phase of the signal gain. However, the application of this principle is not particularly problematic if the cumulative effect of the removed effects does not change under the influence of the surrounding factors (for example, by changing the temperature) of the offset interval.

The other approach to dealing with offset parameters and their changes in amplification circuits is the principle of signal modulation, amplification and its subsequent recovery by synchronous detection - known as „chopper stabilization amplification principle" (fig.3) [3] .

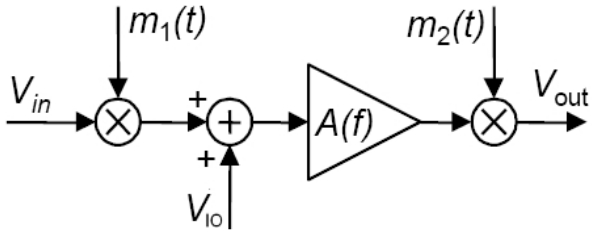

Fig.3. The chopper stabilization amplification principle.

This approach compensates for all offset variations within the amplification tract. In principle, the offsets of the demodulated circuit and those of the subsequent ADC can't be compensated. The greatest advantage of this approach is the ability to achieve high sensitivity of the transformation units.

In both classical methods, all other offset errors occurring outside these circuits from the moment, the signal is received until ADC can't be removed by these means [1].

III. Description Of The Solution

The above effects, require the use of effective compensation methods, combining two classical analogue principles in contemporary use of digital technology.

One proposal for eliminating these events is the co-application of "auto-zero" with "chopping modulation - demodulation technology". The purpose is to include them in a single auto-computational conversion structure, from the source of the analog signal to the final digital infiltrating equivalent for this signal.

Achieving this idea is possible on the basis of the "mixed signal technique". This is achieved by applying the oldest classic "relay chopping technology" for analog signal modulation. It only modulates the polarity of the signal without changing its value. An analog amplification of the received signal and its ADC conversion followed within the modulation signal stroke. Further demodulation processing of the signal is performed in digital form based on the data from the ADC synchronously with the modulation signal.

The application of demodulation and filtration to the information stream from the entire transformation tract in a fully digital format is applied to achieve high-bandwidth and minimize noise components [4].

The block diagram illustrating the idea of "relay chopping technology modulation" with "digital demodulation" is shown in Fig. 4. In this U_{IO} voltage, all possible offset voltages and their drives, which may exist in the circuit related to the differential input of the entire transformation structure, are combined.

The differential input of the S/H chain structure, the amplifier and the ADC are alternatively switched from a CHOP controlled multiplexer circuit. To ensure that the structure works correctly, the S/H signal is doubled in sync and phase shifted frequency to the CHOP signal.

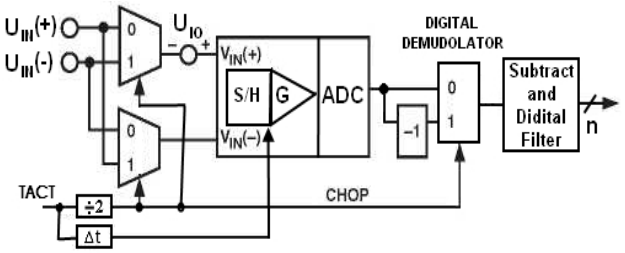

Fig.4. Conversion structure with „relay chopping technology modulation" and "digital demodulation".

The result of the ADC conversion for each CHOP signal level is fed to the digital demodulator with subsequent digital filtering.

The resulting digital value Dig {U} of the ADC covering, contain the input voltage and all offset voltages with their variations. For switching signal value Chop = 1 the output digital value is:

$$N_{DAC}^{1} := Dig\{U_{IN}(+) + U_{IN}(-) + U_{IO}\} \qquad (2)$$

At switching signal value Chop = 0, the output digital value is:

$$N_{DAC}^{0} := Dig\{-U_{IN}(+) + U_{IN}(-) + U_{IO}\} \qquad (3)$$

After receiving two consecutive numerical values from the ADC for CHOP signals 1 and 0 or 0 and 1, the results are subtracted. As a result of this elementary mathematical operation in the final N_{OUT} result, the offset values of the two adjacent transformations are compensated.

$$N_{OUT} = N_{DAC}^{1} - N_{DAC}^{0} = 2.Dig\{U_{IN}(+) - U_{IN}(-)\} \qquad (4)$$

This statement is true if the offset values do not change their values for the switching signal period or their change is below the ADC resolving capability.

Applying this approach, compensates for the temperature deviations of offset voltages as these changes are made for periods many times greater than the switching signal period.

The ultimate effect is that virtually eliminates offset errors occurring in the multiplexer chain, the S/H, the internal signal amplifier, and the ADC itself.

To initiate the ADC compensation process, a conversion for Chop = 1 and Chop = 0 or Chop = 0 and Chop = 1 must be performed.

The first valid output for N_{OUT} appears after two ADC conversion periods (2 * T_{ADC}). This is the time for finding a first result. The following results are now obtained at each conversion period (T_{ADC}).

The result for the phase starting with Chop = 0 is obtained by the formula:

$$N_{OUT} = -N^0_{DAC} + N^1_{DAC} = 2.Dig\{U_{IN}(+) - U_{IN}(-)\} \quad (5)$$

And the result for the phase starting with Chop = 1 is obtained by the formula:

$$N_{OUT} = N^1_{DAC} - N^0_{DAC} = 2.Dig\{U_{IN}(-) - U_{IN}(+)\} \quad (6)$$

The chart of the output results is shown in Fig. 5. The output for the first valid result appears with a delay within the third ADC conversion rate.

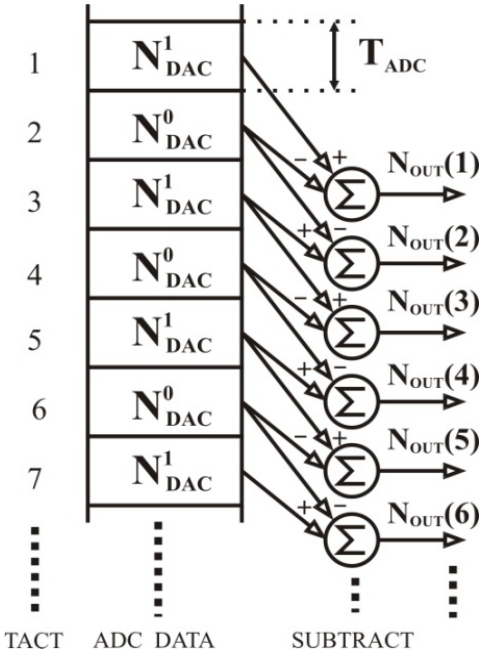

Fig.5 The Output Results Chart

A general problem, limiting the capability of the method is related to the transient processes induced by the injected charges in the commutation of the signals in the input multiplexer circuits as shown in Fig. 6.

Due to the fact that the measurement interval is the same and digitally defined for both normal Chop = 1 and inverse Chop = 0 signal conversion, the effect on the end result of the switching charges is essentially self-canceling. This is possible due to the fact that the input is differential and they have completed less than 1 LSB within the conversion cycle as shown in Fig. 7.

In order to reduce them and to protect the amplification circuits from shock saturation, a digitally calibrated delay of the S/H synchronization is introduced in relation to the "chopper" signal with the interval Δt. In this situation, the initial steep part of the development of the transition process is cut, which can lead to saturation of the chains.

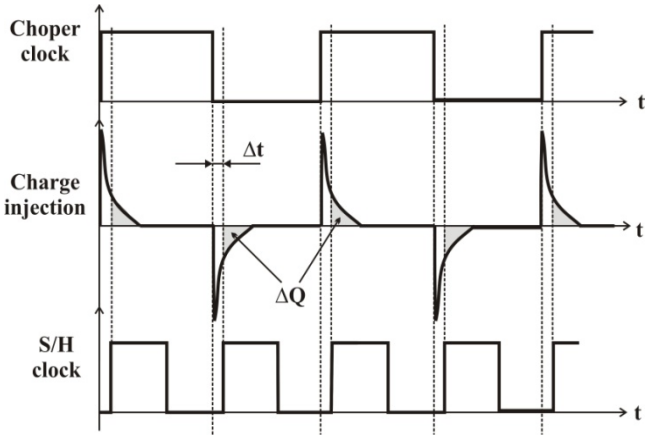

Fig.6 Transitional processes from injected charges in multiplex circuits and S / H synchronization versus "chopper" signal.

The duration of the transient process of this effect ultimately determines the maximum frequency of the switching signal frequency.

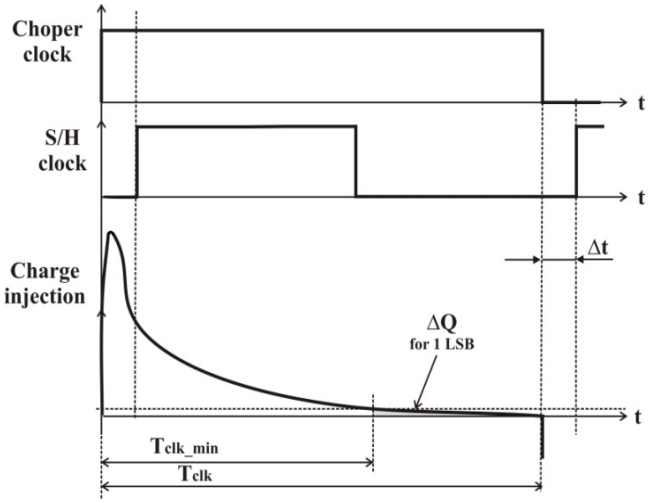

Fig.7 Transitional processes from injected charges in multiplex circuits and synchronization of S / H defining the minimum duration of the "chopper" signal.

Applying the process of summing the digital signal values from two consecutive reports due to their mutual un correlation, generally leads to an increase in the white noise noise type with SQR (2) and the probable increase in type 1 / f noise caused by the “djitter” effect at Commutation of analog circuits.

This requires, after carrying out the numerical subtraction operations, the use of a minimal filtration of the resulting set of numerical values. Recommended are those with an integrative hatcher of the current average type or rearranged by the statistical hysteresis or medial filtration rearrangement.

On the other hand, the application of the principle of "Auto-Zero" generates, in its essence, in the compensating circuit additional noise voltages with spectral density $S_n(f)$

The effect of the automatic reset process on the noise of the amplifier can be described by assuming that the input noise of the amplifier corresponding to the voltage source V_{IN} is described as:

$$S_n(f) = S_{WN} \cdot \left(1 + \frac{f_K}{|f|}\right) \quad (7)$$

where S_{WN} is the PSD (Power Spectral Density) at the input of the amplifier (usually expressed as thermal noise), and f_K Is the angular frequency defined as the frequency for which PSD *1/f* the noise equals the PSD white noise S_{WN}. [3] [5].

As opposed to the compensated voltage, which can be considered constant, the amplifying noise and especially its broadband thermal noise component is a variable and random magnitude.

Therefore, the efficiency of the automatic reset and low noise reduction process depends on the mutual correlation between the signals from two adjacent reports that are subtracted.

The autocorrelation between two samples of noise 1/f is much higher than white noise, assuming they have the same bandwidth. In this way, the automatic reset process is effective to reduce the noise of 1/f. This method is low-efficient for broadband white noise and explosive noises.

Another way to see the effect of auto-resetting is to note that this is equivalent to subtracting noise from the previous sample with the same noise. For a DC or a very low frequency drift, this causes the parasitic values to be canceled.

In addition to this basic filtering process, since automatic resetting is a sampling technique, broadband noise is added to the baseband, increasing the PSD obtained.

Partially, the broadband noise problem is relatively easy to solve by filtering it before it is fed to the ADC. In fact, this noise remains the one with a spectral density of 1/f and 1/f2 that causes unpredictable signal processing.

Upon the occurrence of additional emerging explosive noises in the measurement information whose amplitude density distribution is non-gassive and sometimes even unpredictable, the process of processing the measurement information is preferably performed on the principle of editing values with unlikely information based on criteria set.

III. CONCLUSION

The problem of the impact of offset voltages and their drift generated in the measuring system in the process of forming a digital equivalent for a pre-formed value is examined.

A method and a schematic solution are proposed to reduce the total offset voltages in a measuring line based on the mixed signal technology.

Its limitations have been defined in relation to transformation time intervals and generated internal parasitic charges.

A methodology for the construction of a measuring line minimizing to the noise level the impact of the offset voltages in the whole measuring system.

We define the sources that cause the noise composition in the output digital result and the guidelines for minimizing them.

Upon the occurrence of blasting noises with the distribution of amplitude densities of non-Gaussian nature, it is proposed to process the information processing on the principle of editing improbable values

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Investigation of ADC Using "Sliding Scale" Technique and its Impact on Differential Nonlinearity

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Abstract – The influence of differential nonlinearity on widely used ADCs build into general purpose microcontrollers is investigated in this paper and the possibility to reduce it using the "sliding scale" technique. Experimental data is presented. Simple circuits are presented which offer wide usage of the method.

Keywords – **ADC, "sliding scale", differential nonlinearity**

I. INTRODUCTION

The question about accuracy when transforming analog values into digital has always been the leading one when designing analog to digital systems. The most common way to improve it is based on making the bit size of the ADC bigger. Unfortunately this approach does not solve but circumvents the problems, which are methodologically generated by physical facts like integral and differential nonlinearities of the particular device.

A. Integral and differential nonlinearities

Integral nonlinearity (INL) represents the maximum difference between the real transfer characteristics of ADC and the mathematical dependence (in most cases linear), which describes this characteristics. It gives an idea about the maximum error which can be seen during the measurement within the full scale of the converter.

Differential nonlinearity (DNL) represents the maximum difference between the real width of one discrete value of the ADC versus its nominal value of one LSB. DNL gives information about the ADC's monotonicity. Most often it is caused by deviations of the scaling components in use (resistors or capacitors) and it is seen when switching to the next code. The effect of the DNL error is most obvious when the data is plotted in a histogram.

B. Ways to improve accuracy during conversion

When conversion accuracy improvement is needed the most common practice used is to make the ADC resolution bigger. This solution works only partially because the reason that DNL exists is fundamental and it will exist independently of the specific technical solution applied.

In some cases the averaging method is used – several measurements are done and the average of them is used as a final measured value. This at first look good approach does not lead to good results because the measurements are done around the same point of the ADC's transfer function. Averaging data from several consecutive measurements will help in cases when the measurement accuracy is influenced by external factors (like noise) but it will not lead to correction of internal based inaccuracies.

C. Method of the,,sliding scale" - Gatti method

The "sliding scale" method aims at reducing the differential nonlinearity while determining the amplitude of impulse signals with the help of spectrometric ADCs. It is proposed by d-r Emilio Gatti back in 1964 [1].

The method is expressed in shifting the input signal trough the ADC input range by adding additional input voltage from precise DAC, which value is subtracted digitally from the result. [2]. DAC's output voltage is generated from a random number generator thus the measured value can be offset to a random location of the ADC's transfer curve. After doing multiple measurements of pulses with the same amplitude, correcting the output code based on the added offset voltage and averaging the codes, the differential nonlinearity is reduced. The method is used in nuclear electronics for measuring the amplitude of pulses coming from detectors of ionizing radiation to determine the spectral spread by energy.

D. Purpose of the investigation.

It is beneficial to evaluate the effectiveness of the "sliding scale" method in DC level measurements, using an ADC integrated in cheap general purpose microcontroller. To do this first the DNL and INL must be measured for the specific ADC, in order to compare the results when the Gatti's method is applied.

In modern microcontrollers are embedded more and more analog subsystems with parameters and characteristics that can be controlled by the firmware – ADC, DAC, CTMU, analog amplifiers, programmable voltage sources and others. This is creating possibility for diverse measurement configurations and also making feasible the implementation of the Gatti's method. The performance of which is in the scope of this investigation.

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II. STATEMENT.

A. Description of the experimental setup

In order to conduct the investigation an experimental setup is created, which is shown on fig.1. The investigated object is twelve bit ADC embedded into a Microchip microcontroller PIC18F25K80. For ADC reference a TL431, manufactured by Texas instruments, is used. It has temperature coefficient of 92ppm/°C. The applied input voltage is shifted against the ADC scale by MAX4238ASA configured as summing amplifier. It is an auto-zero amplifier with 10uV input offset and 10nV/°C input offset temperature drift. For offset voltage (used to shift the input voltage) generation a twelve bit DAC is used – MCP47FEB21, it has integrated bandgap voltage reference with temperature coefficient of 15ppm/°C. The readings from the analog to digital conversion and the applied offset code to the DAC are transferred to a PC by a serial communication channel.

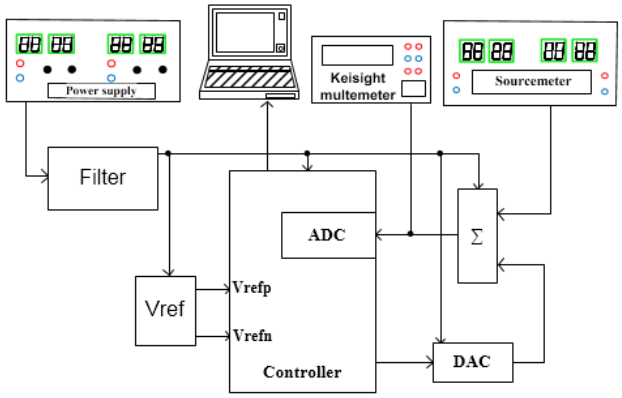

Fig.1 Block diagram of the setup

The system is supplied by universal power supply – Hameg HD7042. The input stimulus for the ADC is generated by programmable source meter – Keithley 2401A. The voltage after the summing amplifier (right at the ADC input pin) is measured by Keisight 34461A multimeter.

B. Sequence of the experiment

After the equipment is powered up, including the system under test, the entire setup is left for one hour to reach normal working temperature. On the PC in running an Excel macro used for control of the ADC input voltage (source meter), logging the ADC conversion results, control of the applied offset voltage (DAC) and logging the multimeter readings. The ADC input voltage step is 1LSB. After doing 4096 measurements with zero input offset voltage (in order to scan the entire ADC span) a random number generator is used to select the DAC code thus generating different values for input offset, limited to 1/16 of the ADC's full scale range. In this way the next measurements are done at different part of ADC's transfer characteristics. The latter input range is "shortened" therefore only 3840 measurements are done (2^{12}-2^8). In total four different measurements are done on different locations of ADC's transfer characteristics.

All data generated during the experiment are saved and processed in Excel. A correction to each measurement is done by subtracting a value equal to the applied input offset voltage. All data from the four measurements are averaged. Integral and differential nonlinearities are calculated before and after using the "sliding scale" technique.

C. RESULTS

Interesting are the results from the experimental setup used to show the properties of the method under investigation.

On figure 2 is represented in graphical form the transfer characteristic of the ADC. It is clear that the measured (based on least square method) dependency can be well approximated using a linear dependency.

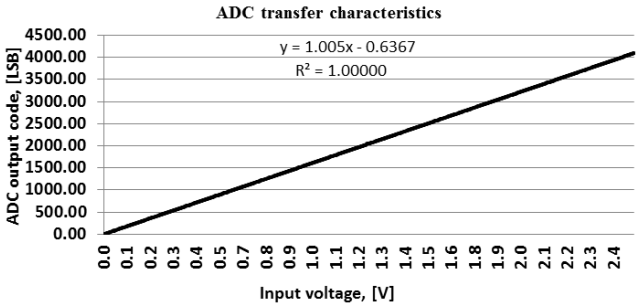

Fig.2 Graphical representation of ADC's measured transfer

It is clear that the generated trend line based on least squares method fits good to the transfer curve. This proves the good characteristics of the ADC and that the noise and nonlinearities of the setup are minimized under 1LSB.

With the gathered data (without using the "sliding scale" technique) INL (fig.3) and DNL (fig.4) are calculated.

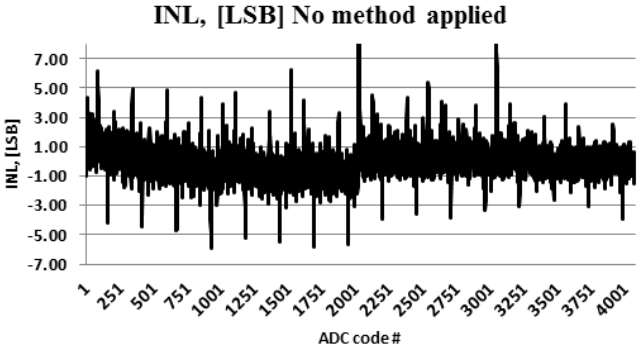

Fig.3 ADC's INL no method applied

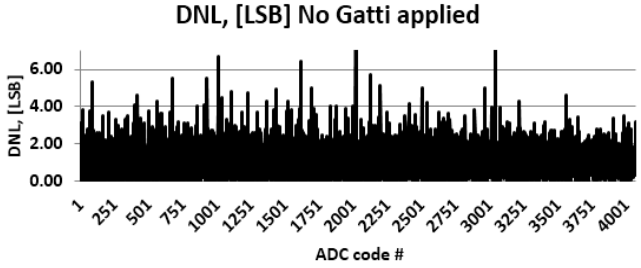

Fig.4 ADC's DNL no method applied

After averaging the results with the four different offset voltages INL and DNL are calculated again. The latter results are presented on fig. 5 and fig. 6.

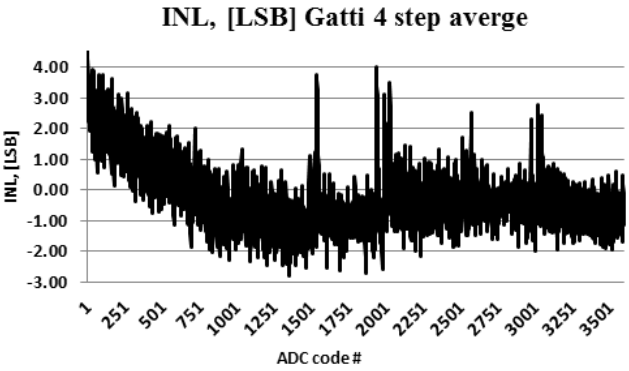

Fig.5 ADC's INL Gatti's method applied

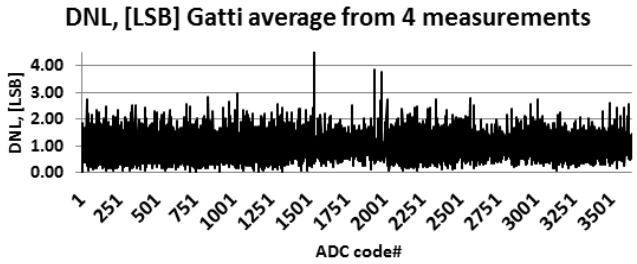

Fig.6 ADC's DNL Gatti's method applied

III. DISCUSSION OF RESULTS

The presented results prove that when using the method of the "sliding" scale differential and integral nonlinearities are improved. With more measurements the results will get better.

If averaging is used when Gatti's method is not applied no improvement of DNL and INL will be observed because the averaged data will be measured only on a specific point from the ADC transfer characteristic. The averaging will work only as an input signal filter but will not "correct" the transfer characteristic of the ADC.

IV. PRACTICAL USE (APPLICATIONS)

The Results prove that it is worth it to develop different hardware and software approaches for ADC non-linarites reduction.

A. Typical schematic used for the method:

One of the possible schematic realizations of the method is using the idea as its first appearance – the input signal is "moved" against the ADC scale, shown on figure 7. The major advantage of the solution is its simplicity and "visibility" of the separate structural blocks. As disadvantages the DAC nonlinearities, the offset voltages of the buffering amplifiers and the summing amplifier can be mentioned. DAC control and result correction are realized by the embedded software into the used microcontroller.

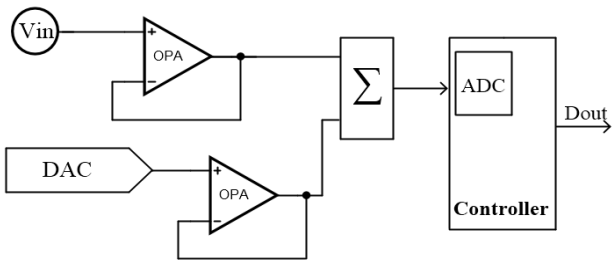

Fig.7 Typical schematic for adding input offset voltage

In this case ADC's top part of the scale is not usable. As the input voltage cannot have values bigger than the full scale of the ADC minus the maximum applied offset voltage.

B. Modified schematic

If the integrated in to the microcontroller ADC have the ability to use external reference voltage the offset can be applied to the reference instead to the signal, schematic shown on figure 8. Here the approach is changed – the scale of the ADC is shifted versus the measured voltage. This requires the input voltage to be shifted up with a voltage equal to the maximum offset voltage applied to the ADC reference. Again the scale of the equivalent converter is reduced.

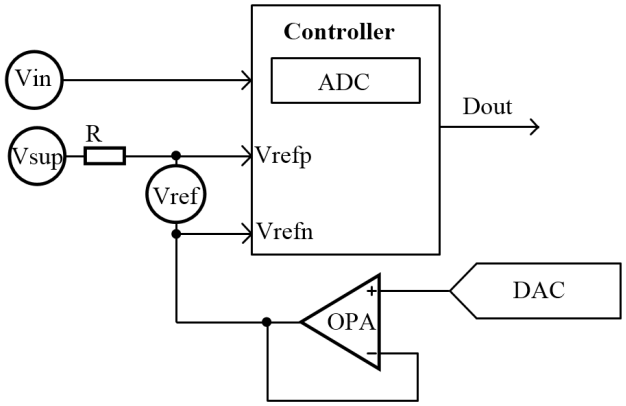

Fig.8 Modified schematic

The advantage of this solution is its simplicity. As disadvantage the input signal minimum value is limited.

C. Schematic using CTMU module for DAC

In some microchip controllers (like PIC18F25K80 and others) there is an embedded CTMU module (Charge Time Measurement Unit), which has programmable current source connected internally with an analog multiplexor to the ADC. This gives the possibility to generate a voltage shift of the ADC input voltage simply by adding a series

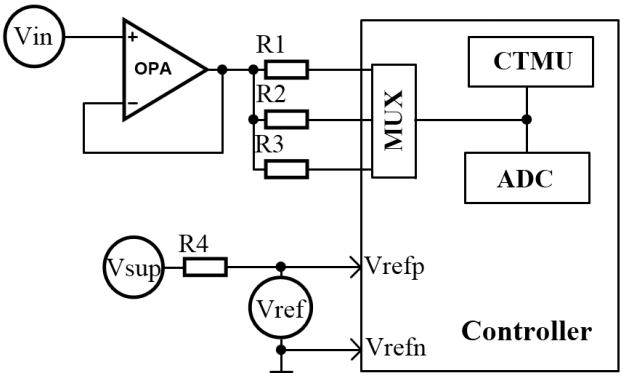

Fig.9 Schematic using CTMU module for DAC

resistor to the corresponding analog input pin. (fig. 9). The possibility of trimming this shift can be extended by using several inputs to which are connected resistors with different values.

The schematic solution allow easily a self-calibration procedure to be implemented – for this purpose an input signal with amplitude of 0V must be applied to the input and all shifts generated by the different values of the current source must be measured. After that the saved values are used for code correction of the separate ADC reading.

As advantage of this solution again is its simplicity. No summing circuits are used (less potential sources of error), no external DAC and additional external components are used. The application of this method is limited to microcontrollers which has embedded CTMU module. The shortening of the scale is "on top" which can be easily corrected by changing the value of the reference voltage.

V. CONCLUSION

The conducted research confirms the effectiveness of the "sliding scale" principle for improving integral and differential nonlinearities of ADCs. This allows the integrated ADC to be used for precision applications.

VI. ACKNOWLEDGEMENTS

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Median technique for noise reductions

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Abstract – **The problem of reducing the low-frequency drift, "flicker" and blasting noise, generated in the measuring tract in the process of forming a digital equivalent for a measured value has been considered. Methods are proposed to further reduce the noise composition in the results obtained. The minimization of noise components of type 1/f, 1/f2 and irregular blast noise in the output digital result is performed by means of digital filtering based on modified "Tukey53H3" algorithm. A one-stage algorithm for "SM9H3" is proposed with floating current fragmentation in signal processing. As an application, the results of the proposed signal processing methodology are shown and described.**
Keywords – **median filtering, noise reduction, digital filtering, Tukey-53H, SM9H3**

I. INTRODUCTION

In devices for the reception of analog information, errors may be caused by unintentional external or internal induced noise voltages at many points in the circuit channel, in the perception and processing of relatively weak signals.

Within even an integrated circuit, such as an ADC with its own internal amplifier and S&H circuit, there are multiple sources of internal noise errors due to incoherence between the individual steps, the parasitic charge injection processes on the capacitor in the pass-through sampling process In memory mode or external interference voltages from electromagnetic processes or radiation.

These problems, in principle, appear to be inevitable problems in building transformational structures and are mainly related to the possibilities for real physical realization, especially in the case of work of extreme sensitivity.

II. PROBLEM FORMULATION

In the attempt to increase the resolving power, noise problems arise because, by applying any method for removing offset errors in the digital equivalent of the Dig (U) signal, additional noise compositions [2] with spectral density $S_n(f)$.

The influence of the noise components can be described by assuming that the spectral density of the input noise relative to the input of the whole transformer tract is described as:

$$S_n(f) = S_{WN}\cdot\left(1+\frac{f_K}{|f|}\right) \tag{1}$$

where S_{WN} represents the spectral density of white noise (PSD -Power Spectral Density) brought to the input of the conversion circuit (usually expressed as thermal noise) and f_K is the angular frequency defined as the frequency at which the PSD of the *1/f* noise becomes equal to the PSD of white noise S_{WN}. [1].

Partially, the broadband noise problem in the conversion devices is solved by filtering it just before feeding to the ADC. In fact, from this noise, it remains to operate at a spectral density of $1/f$ and $1/f^2$. This gives rise to implausible signal processing values.

The classical structural scheme for editing values with unlikely values of measurement information is presented in Fig.1 [5].

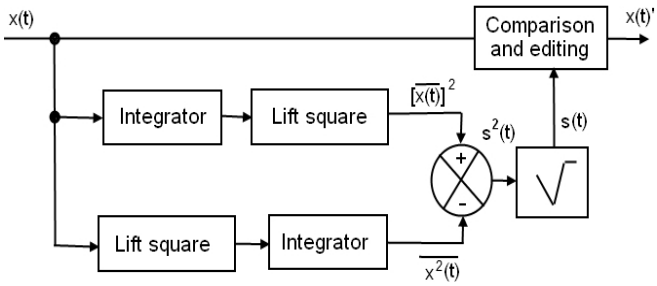

Fig.1 A classical scheme for editing values with unlikely values of measurement information.

An editorial rating criterion is based on a pre-accepted value for the maximum permissible standard deviation s (t) within the set processing time interval. This interval is determined by the built-in transition characteristics of the integrating circuits.

$$x(t)-k.s(t) < x(t-\tau) < x(t)-k.s(t) \tag{2}$$

Depending on the set tolerance k, relative to the value of the current standard deviation s (t) in the comparison and editing unit, the current unlucky value is replaced by another value obtained by the extrapolation method of the adjacent time values prior to the occurrence of the imprecise measurement.

$$x(t_i) = 2.x(t_{i-1}) - x(t_{i-2}) \tag{3}$$

For the correct operation of the described procedure additional limitation criteria should be introduced so that the resulting extrapolation does not lead

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to a new implausible value.

An inconvenience of this method is the limited rate of change in the amplitude of signal data that makes sense to process, as well as the terminal rate of increase in the output signal. The reason is the presence of integrating chains as well as the relationship between s and τ.

III. Description Of The Solution

The problem of further reduction of the noise spectrum in the output, and in particular of the type *1/f* and the explosive noise $1/f^2$, can be achieved by applying a median filtration [3].

This is a method for non-linear processing of data sequences based on the center of gravity method as the most plausible information. Processing is based on an odd number of samples from the signal in current fragmented packets. The idea was initially formulated by John Tukey [6] and concludes that the median in the absence of a priori information on the measurement process is the most likely estimate of the mean value of the magnitude of the interval under consideration, with minimal deviation deviations.

On the other hand, the median estimate is a value of the measured magnitude itself after re-ordering within a given processing interval. This means that the final result after this processing is part of the most probable value of the estimated magnitude obtained from the input data without any computational procedures being performed on them.

Functions describing the behaviour of median processed signals are [5] :

$$Med\{K.f(x)\} = K.Med\{f(x)\} \tag{4}$$

$$Med\{K + f(x)\} = K + Med\{f(x)\} \tag{5}$$

$$Med\{f(x) + g(x)\} \neq Med\{f(x)\} + Med\{g(x)\} \tag{6}$$

It follows from definitions (4) and (5) that the media filters store the information characteristic of the signal in the sense of a modulated noise signal. Any deviations from the most probable centered value for one signal with a duration of less than half of the median processing window are suppressed. Equation (6) shows the impossibility of two centers of gravity or separation by mediated processing of two constituents from one information sequence.

A modified algorithm for applying a current processing to form the values in this procedure uses the following algorithmic order:

$$\begin{cases} .X'(i) = Med\{X(i-5),....,X(i)\} \\ .X''(i) = Med\{X'(i-2), X'(i-1), X'(i)\} \\ .X'''(i) = \{.[X''(i-2) + 2.X''(i-1) + X''(i)]/4\} \end{cases} \tag{7}$$

This is a modification of the famous "Tukey53H3" procedure. The filter window is formed based on information from 9 consecutive reports. The structure is a two-stage nonlinear median treatment with subsequent smoothing of the result with a three-ply window of "Hening". Output data for the current processing is obtained in the eleventh order - i.e. the current time fragment is from ten consecutive reports. A disadvantage of the proposed procedure is the low filtration of subwoofers and fluctuations.

Further reduction of noise components is possible by increasing the length of the fragmentation interval for medial treatment in a one-stage variant with a subsequent Hening quot for three or more results [3][4]. The basic idea behind this procedure is to apply a median processing over a larger range of input data while preserving the processing time and the delay of the current fragment packet from the beginning of the signal processing as the number of clocks.

For this purpose, a nine-point median filtration structure with a three-layer Hening window was applied. The algorithm for operating the proposed procedure under the name "M9H3" is shown in Figure 2.

The results are based on the following algorithm:

$$\begin{cases} .X'(i) = Med\{X(i-9),....,X(i)\} \\ .X'''(i) = \{.[X'(i-2) + 2.X'(i-1) + X'(i)]/4\} \end{cases} \tag{8}$$

From the structural scheme reflecting the movement of the fractional packet in the processing of the information (Fig. 2), it is apparent that the output information is again at the eleventh time as in "Tukey53H3".

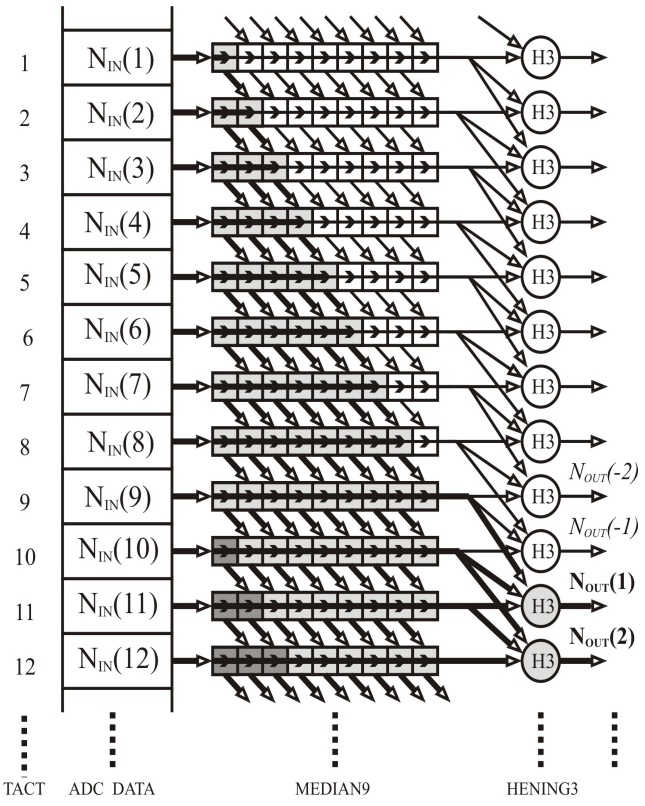

Fig. 2 Structure of processing of information under the procedure "M9H3".

In order to reduce the influence of super low disturbance factors and DC drives, in addition, a mixed signal technique for offset reductions is applied to two adjacent values of alternating polarity.

As opposed to “Tukey53H3”, the proposed algorithm handles almost all of noise component in the flicker and blasting noise signals. The strong reduction of any explosive components of the improbable data type is due to the extended range of medial treatment. Emission abnormalities of less than five consecutive inputs from ADC conversions are eliminated.

The co-implementation of the mixed signals technique for offset reductions also allows a strong reduction of ultra low inter-correlated by two-beat interference, as well as the overloaded DC drives.

To reduce the influence of all the above noise components, the numerical treatment procedure "SM9H3" (Substraction Median 9 Hening 3) was applied, whose structure of fragmentation of the data is shown in Fig. 3

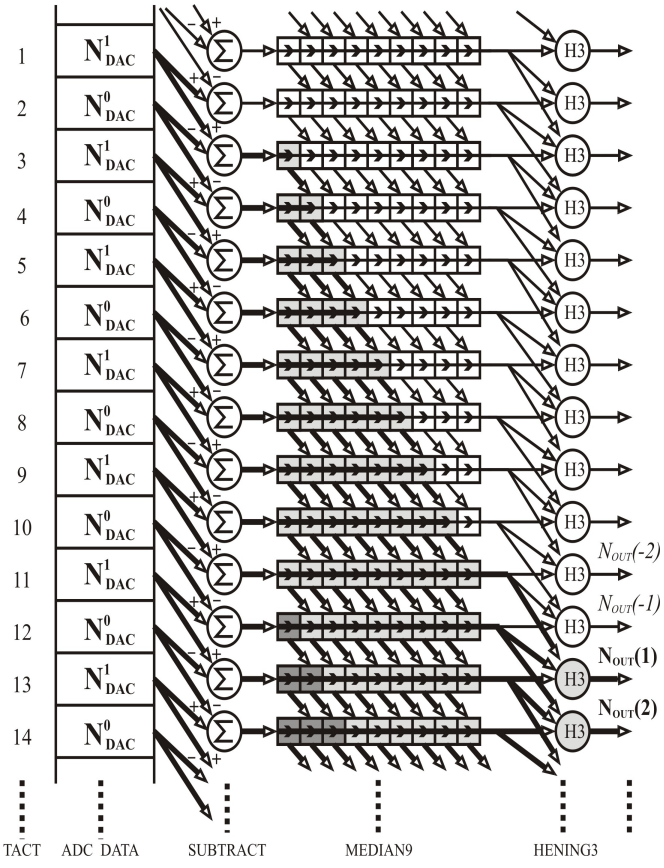

Fig.3 Output Compensation Data Processing Structure and Digital Filtration by Algorithm "SM9H3"

The total time delay from the processing process is twelve feet, which is only two more paces than the classic "Tukey53H3"

The result of the operation of this digital data processing algorithm is applied to the test signal of Fig.4. Fig. 5 shows the effect of the noise components on the spectral distribution of the test signal with the distribution *1/f* and $1/f^2$.

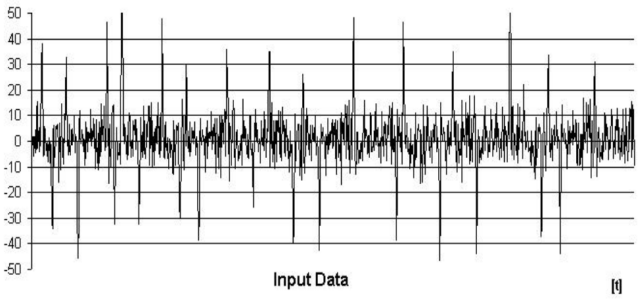

Fig.4 Time-frame of an digitizing test signal with remove DC offset.

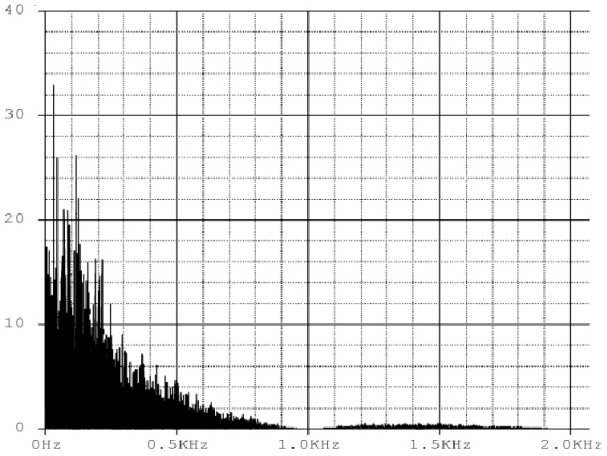

Fig. 5 Spectrum of the signal without digital filtration and offset reduction

The timing of the signal after processing with modified procedure "Tukey53H3" is shown in Fig.6. The signal no longer contains part of the noise components of the base signal. Despite the applied signal processing, strong explosive noise components are still available that penetrate the two-stage processing structure and would mask the useful component of the signal.

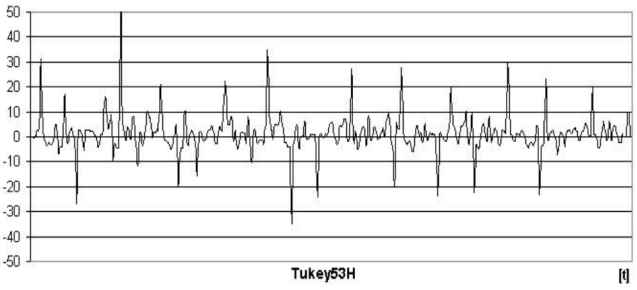

Fig.6 Timeframe of an o-digit signal and after applying a modified digital processing procedure "Tukey53H3"

A processed signal time frame after applying the "SM9H3" digital processing procedures is shown in Fig. 7. At the expense of just two-step increments, but as a combination of two methods, the proposed transformation procedure addresses both offset signals and their drives, and "Flicker noise", "Blasting noise" and "White noise".

Only "LSB noise" remains and those caused by the mutual overlap of the "substracting" process and the medial filtration. This is justified by the fact that there is more than one regular process and that the median of the sum of two sequences is not equal to the sum of the two medians according to (6).

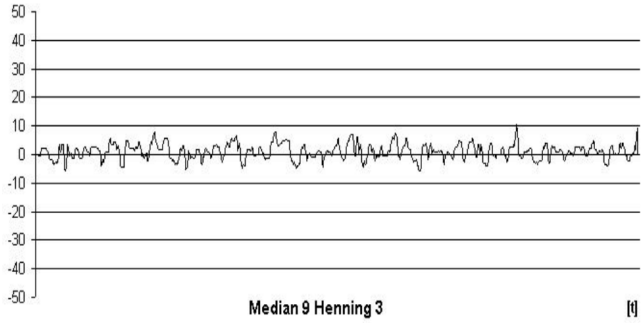

Fig. 7 Timeframe of an OCR signal after application of numerical processing procedures "SM9H3"

The change in the spectrum reflecting the reduction of "fliker," "blasting noise" and offset reduction after processing by "SM9H3" algorithm is shown in Fig.8 and is reduced to several LSB units of ACD resolving power in the field of DC.

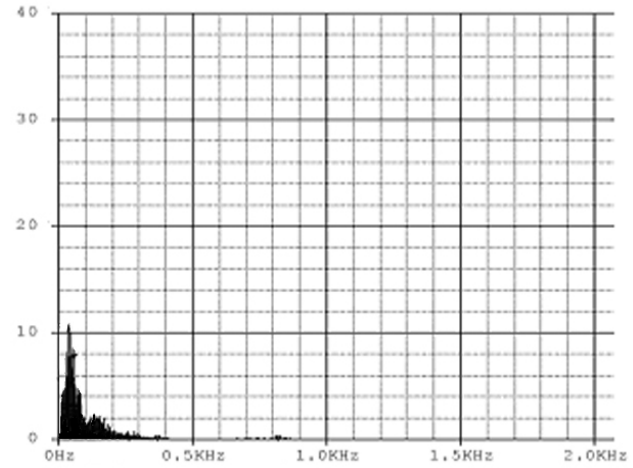

Fig. 8 Spectrum of the signal after applying digital filtration procedure by algorithm "SM9H3"

IV. Conclusion

The problem of reducing low-frequency drives, "flip-flop" and blasting noise generated in the measuring circuit in the process of forming a digital equivalent for a measured value is considered. Methods are proposed for further reduction of the noise components in the results obtained. The minimization of noise components of type *1/f*, $1/f^2$ and irregular blast noise in the output digital result is performed by means of digital filtering based on a modified "Tukey53H3" algorithm. A one-stage algorithm for "SM9H3" is proposed with floating current fragmentation in signal processing.

An advantage of the proposed methodology is to preserve the signal impulse response for times greater than half the duration of the processed data fragment. The development of the proposed method, can be found by compromising prolongation or decrease of the median filtration at the expense of the processing time of the data when increasing the ADC discharge as well as adaptively adjusting its duration.

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Discrete Adaptive Real-Time State Observer Development Using Least-Squares Method

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Abstract –**This paper presents non-recursive algorithm for adaptive observation of linear single-input single-output (SISO) time-invariant discrete systems based on least-squares method. The developed adaptive state observer estimates the parameters, initial and current state vector of the discrete linear system and is suitable for real-time working. Simulations are carried out in Matlab environment and provided in order to prove the algorithm performance.**

Keywords– **adaptive observation, discrete adaptive state observer, non-recursive algorithm, initial and current state vector estimation**

I. Introduction

Design of state feedback control systems often requires state vector reconstruction which could be done by using measurements of input and output signal values of the controlled system.

The algorithm used for state vector reconstruction is referred to as state observer [1,2,3].

The adaptive observation problem is consisted of state observers synthesis, which include parameter estimators. In the adaptive observers synthesis matrices A and b or c (according to the state space canonical representation chosen) are assumed to be unknown. The observation process leads to parameters estimation, unknown matrices determination and state vector calculation [3,4].

In the present paper is presented a non-recurrent algorithm for adaptive observation of SISO linear time invariant (LTI) discrete systems. The algorithm is developed by using the well-known least-squares method (LS method) [4].

The developed adaptive observer uses a parameter estimator which is constructed based on a mathematical procedure which includes inversion of the informative matrix [4].

II. Problem Statement

Let us consider a linear time-invariant SISO discrete system by a state space model of the form:

$$\begin{aligned} &\mathbf{x}(k+1) = \mathbf{A}\mathbf{x}(k) + \mathbf{b}u(k), \quad \mathbf{x}(0) = \mathbf{x}_0, \\ &y(k) = \mathbf{c}^{\mathrm{T}}\mathbf{x}(k) + f(k), \quad k = 0, 1, 2, \cdots \end{aligned} \tag{1}$$

where:

$$\mathbf{A} = \begin{bmatrix} \mathbf{0} & \vdots & \mathbf{I_{n-1}} \\ \cdots & \cdots & \cdots \\ & \mathbf{a}^{\mathrm{T}} & \end{bmatrix} \tag{2}$$

$$\mathbf{a} = \begin{bmatrix} a_1 \\ a_2 \\ \vdots \\ a_n \end{bmatrix}, \ \mathbf{b} = \begin{bmatrix} b_1 \\ b_2 \\ \vdots \\ b_n \end{bmatrix}, \ \mathbf{c} = \begin{bmatrix} 1 \\ 0 \\ \vdots \\ 0 \end{bmatrix}. \tag{3}$$

In the above equations the system order n is a priori known, $(k) \in \mathrm{R}^n$ is the unknown current state vector , $\mathbf{x}(0) \in \mathrm{R}^n$ is the unknown initial state vector, $u(k) \in \mathrm{R}^1$ is a scalar input signal, $y(k) \in \mathrm{R}^1$ is a scalar output signal, $f(k)$ is an additive noise, **a** and **b** are unknown vector parameters.

The following transfer function corresponds to the state-space model (1):

$$W(z) = \frac{h_1 z^{n-1} + h_2 z^{n-2} + \cdots + h_{n-1} z + h_n}{z^n - a_n z^{n-1} - \cdots - a_2 z - a_1}. \tag{4}$$

The relation between the vector **b** elements b_i for the chosen canonical form and the coefficients h_i of the numerator polynomial of the discrete transfer function (4) could be expressed by the following equation[3]:

$$\mathbf{T}\mathbf{b} = \mathbf{h}. \tag{5}$$

where

$$\mathbf{h}^{\mathrm{T}} = \begin{bmatrix} h_1 & h_2 & \cdots & h_n \end{bmatrix},$$

$$\mathbf{T} = \begin{bmatrix} 1 & 0 & \cdots & 0 & 0 \\ -a_n & 1 & \cdots & 0 & 0 \\ -a_{n-1} & -a_n & \cdots & 0 & 0 \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ -a_2 & -a_3 & \cdots & -a_n & 1 \end{bmatrix}$$

The elements a_i of the vector are the coefficients of the denominator polynomial of the discrete transfer function (4), in reversed order and an opposite sign.

It is assumed that the values of the system input signal $u(k)$ are recorder continuously in vector **u**, and the values of the system output signal $y(k)$ are continuously recorder in vector **y**.

In the developed algorithm the last elements of vectors **u** and **y** at each moment are denoted by *end*.

The problem to be considered is to be estimated the unknown vector parameters **a** and **b**, the initial state vector $\mathbf{x}(0)$ and the current state vector $\mathbf{x}(k)$, $k=1, 2, \ldots$

III. Solution Of The Considered Problem

Algorithm For Adaptive Observation Based On Least-Squares (LS) Method [4,5]

The developed algorithm is consisted of the following steps:

Step 1. Input-output data arrays forming:

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$$\mathbf{y_2}=\begin{bmatrix} y(end-N+n+1) & y(end-N+n+2) & \cdots & y(end-n)\end{bmatrix}^{\mathrm{T}},$$

$$\mathbf{y_3}=\begin{bmatrix} y(end-n+1) & y(end-n+2) & \cdots & y(end)\end{bmatrix}^{\mathrm{T}},$$

$$\mathbf{Y_{11}}=\begin{bmatrix} -y(end-2n) & -y(end-2n-1) & \cdots & -y(end-N+1)\\ -y(end-2n+1) & -y(end-2n) & \cdots & -y(end-N+2)\\ -y(end-2n+2) & -y(end-2n+1) & \cdots & -y(end-N+3)\\ \vdots & \vdots & \ddots & \vdots\\ -y(end-(N-2n+1)) & -y(end-(N-2n+2)) & \cdots & -y(end-N+n)\end{bmatrix},$$

$$\mathbf{Y_{21}}=\begin{bmatrix} -y(end-(N-2n)) & -y(end-(N-2n)-1) & \cdots & -y(end-N+n+1)\\ -y(end-(N-2n)+1) & -y(end-(N-2n)) & \cdots & -y(end-N+n+2)\\ -y(end-(N-2n)+2) & -y(end-(N-2n)+1) & \cdots & -y(end-N+n+3)\\ \vdots & \vdots & \ddots & \vdots\\ -y(end-1) & -y(end-2) & \cdots & -y(end-n)\end{bmatrix},$$

$$\mathbf{U_{12}}=\begin{bmatrix} u(end-(2n-1)) & u(end-2n) & \cdots & u(end-N+2)\\ u(end-(2n-2)) & u(end-(2n-1)) & \cdots & u(end-N+3)\\ u(end-(2n-3)) & u(end-(2n-2)) & \cdots & u(end-N+4)\\ \vdots & \vdots & \ddots & \vdots\\ u(end-n) & u(end-n-1) & \cdots & u(end-N+n+1)\end{bmatrix},$$

$$\mathbf{U_{22}}=\begin{bmatrix} u(end-(n-1)) & u(end-n) & \cdots & u(end-N+n+2)\\ u(end-(n-2)) & u(end-(n-1)) & \cdots & u(end-N+n+3)\\ u(end-(n-3)) & u(end-(n-2)) & \cdots & u(end-N+n+4)\\ \vdots & \vdots & \ddots & \vdots\\ u(end) & u(end-1) & \cdots & u(end-N+2n+1)\end{bmatrix},$$

where $\mathbf{Y_{11}}$, $\mathbf{Y_{21}}$, $\mathbf{U_{12}}$ and $\mathbf{U_{22}}$ are Toeplitz matrices, n is the system order and $N\geq 3n$.

Step 2. The submatrices calculations:

$$\mathbf{G_{11}}=\mathbf{Y_{11}^{\mathrm{T}}Y_{11}}+\mathbf{Y_{21}^{\mathrm{T}}Y_{21}},$$

$$\mathbf{G_{12}}=\mathbf{Y_{11}^{\mathrm{T}}U_{12}}+\mathbf{Y_{21}^{\mathrm{T}}U_{22}},$$

$$\mathbf{G_{21}}=\mathbf{U_{12}^{\mathrm{T}}Y_{11}}+\mathbf{U_{22}^{\mathrm{T}}Y_{21}},$$

$$\mathbf{G_{22}}=\mathbf{U_{12}^{\mathrm{T}}U_{12}}+\mathbf{U_{22}^{\mathrm{T}}U_{22}}.$$

Step 3. Calculation of the covariance matrix $\mathbf{C}$:

$$\mathbf{C}=\begin{bmatrix} \mathbf{M_1}+\mathbf{M_1G_{12}M_2G_{21}M_1} & \vdots & -\mathbf{M_1G_{12}M_2}\\ \cdots\cdots\cdots\cdots & \cdots & \cdots\cdots\cdots\cdots\\ -\mathbf{M_2G_{21}M_1} & \vdots & \mathbf{M_2}\end{bmatrix},$$

where

$$\mathbf{M_1}=\mathbf{G_{11}^{-1}},$$

$$\mathbf{M_2}=\left(\mathbf{G_{22}}-\mathbf{G_{21}M_1G_{12}}\right)^{-1}.$$

Step 4. Calculation of vectors $\hat{\mathbf{h}}$ and $\hat{\mathbf{a}}$ by using the following vector-matrix system:

$$\hat{\mathbf{p}}=\mathbf{C}\begin{bmatrix}\mathbf{Y_{11}^{\mathrm{T}}y_2}+\mathbf{Y_{21}^{\mathrm{T}}y_3}\\ \mathbf{U_{12}^{\mathrm{T}}y_2}+\mathbf{U_{22}^{\mathrm{T}}y_3}\end{bmatrix}.$$

$$\hat{\mathbf{h}}=\begin{bmatrix}\hat{h}_1 & \hat{h}_2 & \cdots & \hat{h}_n\end{bmatrix}^{\mathrm{T}}=\begin{bmatrix}\hat{p}_{n+1} & \hat{p}_{n+2} & \cdots & \hat{p}_{2n}\end{bmatrix}^{\mathrm{T}},$$

$$\hat{\mathbf{a}}=\begin{bmatrix}\hat{a}_1 & \hat{a}_2 & \cdots & \hat{a}_n\end{bmatrix}^{\mathrm{T}}=\begin{bmatrix}-\hat{p}_n & -\hat{p}_{n-1} & \cdots & -\hat{p}_1\end{bmatrix}^{\mathrm{T}},$$

$$\hat{\mathbf{A}}=\begin{bmatrix}\mathbf{0} & \vdots & \mathbf{I_{n-1}}\\ \cdots & \cdots & \cdots\\ & \hat{\mathbf{a}}^{\mathrm{T}} & \end{bmatrix}.$$

Step 5. Calculation of vector $\mathbf{b}$ estimation implementing the following linear algebraic system of equations:

$$\mathbf{T}\hat{\mathbf{b}}=\hat{\mathbf{h}},$$

where: $\mathbf{T}=\begin{bmatrix} 1 & 0 & 0 & \cdots & 0 & 0\\ -\hat{a}_n & 1 & 0 & \cdots & 0 & 0\\ -\hat{a}_{n-1} & -\hat{a}_n & 1 & \cdots & 0 & 0\\ \vdots & \vdots & \vdots & \ddots & \vdots & \vdots\\ -\hat{a}_2 & -\hat{a}_3 & -\hat{a}_4 & \cdots & -\hat{a}_n & 1\end{bmatrix}$

is a lower triangular Toeplitz matrix.

Step 6. Estimation of the initial state vector $\mathbf{x_0}$:

$$\hat{\mathbf{x}}_\mathbf{0}=\left(\mathbf{D}^{\mathrm{T}}\mathbf{D}\right)^{-1}\mathbf{D}^{\mathrm{T}}\left(\mathbf{y_1}-\mathbf{Qu_1}\right)=\begin{bmatrix}\hat{x}_{0\,1} & \hat{x}_{0\,2} & \cdots & \hat{x}_{0\,n}\end{bmatrix}^{\mathrm{T}},$$

(applicable only in case that $\det\left(\mathbf{D}^{\mathrm{T}}\mathbf{D}\right)\neq 0$),

where:

$$\mathbf{D}=\begin{bmatrix}\mathbf{c}^{\mathrm{T}}\\ \mathbf{c}^{\mathrm{T}}\hat{\mathbf{A}}\\ \mathbf{c}^{\mathrm{T}}\hat{\mathbf{A}}^2\\ \vdots\\ \mathbf{c}^{\mathrm{T}}\hat{\mathbf{A}}^{(N-1)}\end{bmatrix}_{(N\,x\,n)},$$

$$\mathbf{Q}=\begin{bmatrix} 0 & 0 & \cdots & 0\\ \mathbf{c}^{\mathrm{T}}\hat{\mathbf{b}} & 0 & \cdots & 0\\ \mathbf{c}^{\mathrm{T}}\hat{\mathbf{A}}\hat{\mathbf{b}} & \mathbf{c}^{\mathrm{T}}\hat{\mathbf{b}} & \cdots & 0\\ \vdots & \vdots & \ddots & \vdots\\ \mathbf{c}^{\mathrm{T}}\hat{\mathbf{A}}^{(N-2)}\hat{\mathbf{b}} & \mathbf{c}^{\mathrm{T}}\hat{\mathbf{A}}^{(N-3)}\hat{\mathbf{b}} & \cdots & \mathbf{c}^{\mathrm{T}}\hat{\mathbf{b}}\end{bmatrix}_{(N\,x\,(N-1))}.$$

Step 7. Current state vector $\mathbf{x}(k)$ estimation:

$$\hat{\mathbf{x}}(k+1)=\hat{\mathbf{F}}\hat{\mathbf{x}}(k)+\hat{\mathbf{b}}u(k)+\mathbf{g}y(k),\ \hat{\mathbf{x}}(0)=\hat{\mathbf{x}}_\mathbf{0};$$

$$\hat{\mathbf{F}}=\hat{\mathbf{A}}-\mathbf{gc}^{\mathrm{T}}.$$

Vector $\mathbf{g}$ could be obtained by solving the pole placement problem (PPP) also known as pole assignment problem (PAP). Synthesis of the vector $\mathbf{g}$ should be performed according to the following recommendation: the eigenvalues of the matrix $\hat{\mathbf{F}}$ should be zeros or should be spread into the unit circle closer to the origin than the matrix $\hat{\mathbf{A}}$ eigenvalues. Satisfying this requirement ensures good dynamic characteristic of the observer synthesized.

IV. Simulation Results

Computer simulations are carried out in MATLAB environment taking into account the following assumptions:

- the output signal *y(k)*, the so called system response, is to be simulated for a given system description and an input signal *u(k)*, as known as system reference;
- to the system output is added colored noise *f(k)*;
- the input signal *u(k)* and the noise-corrupted output signal *y(k)* are used as an input data for the observation algorithm;
- the algorithm calculates parameters and state vector estimations by using the input-output data.

The simulations are carried out for a 6th order system which is described by the transfer function given below:

$$W_{об}(z)=\frac{0.6z^{-1}+0.56z^{-2}+0.2125z^{-3}+0.3080z^{-4}+0.5488z^{-5}+0.7221z^{-6}}{1-1.4z^{-1}+0.7875z^{-2}-0.2275z^{-3}+0.035525z^{-4}-0.002835z^{-5}+0.00009z^{-6}}$$

Therefore, the corresponding state space vectors are as follows:

$$\mathbf{a}=\begin{bmatrix}-0.00009\\0.002835\\-0.035525\\0.2275\\-0.7875\\1.4\end{bmatrix};\ \mathbf{b}=\begin{bmatrix}0.6\\0.2\\0.1\\0.3\\0.4\\0.5\end{bmatrix};\ \mathbf{c}=\begin{bmatrix}1\\0\\0\\0\\0\\0\end{bmatrix};\ \mathbf{x}(0)=\begin{bmatrix}1\\1\\1\\1\\1\\1\end{bmatrix}.$$

The matrix **A** eigenvalues are obtained by using *eig(.)* function in Matlab:

$$eig(\mathbf{A})=\begin{bmatrix}0.4 & 0.3 & 0.25 & 0.2 & 0.15 & 0.1\end{bmatrix}^{\mathrm{T}}.$$

As an input signal *u(k)* a pseudo-random binary sequence (PRBS) is used which is generated in Matlab using the following commands u=(sign(randn(127,1)))*10. The output signal *y(k)* is noise-corrupted by adding a color noise *f(k)*. The colored noise is obtained by filtering of white noise through a filter which transfer function could be written as follows:

$$W_{\phi}(z)=\frac{1}{1-1.4z^{-1}+0.7875z^{-2}-0.2275z^{-3}+0.035525z^{-4}-0.002835z^{-5}+0.00009z^{-6}}.$$

The noise level -η,is calculated when dividing the noise standard deviation -σ_f by the output signal standard deviation -σ_y in accordance with the equation:

$$\eta=\frac{\sigma_f}{\sigma_y}100=0\div 10\% \qquad (6)$$

Vector **a** estimation error - e_a, vector **b** estimation error - e_b and state vector **x***(k)* estimation error -e_x are relative mean squared errors (RMSE) and could be determined by the Eq. (7)-(9):

$$e_a(k)=-\sqrt{\frac{\sum_{i=1}^{n}\left(a_i(k)-\hat{a}_i(k)\right)^2}{\sum_{i=1}^{n}a_i(k)}}, \qquad (7)$$

$$e_b(k)=-\sqrt{\frac{\sum_{i=1}^{n}\left(b_i(k)-\hat{b}_i(k)\right)^2}{\sum_{i=1}^{n}b_i(k)}}, \qquad (8)$$

$$e_x(k)=-\sqrt{\frac{\sum_{i=1}^{n}\left(x_i(k)-\hat{x}_i(k)\right)^2}{\sum_{i=1}^{n}x_i(k)}}. \qquad (9)$$

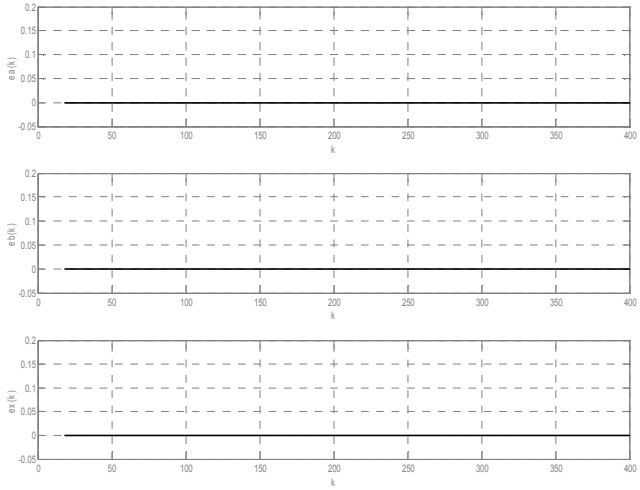

Fig. 1. RMSE for the case of noise-free output signal

In fig.1 are shown the results for the case of noise-free output signal (i.e. *f(k)=0*) and *l=0* (i.e. minimum number of the input-output measurements - *N=3n=18*). It is easily seen that the algorithm starts working at the 18th step of calculations and the observation errors $e_a(k)$, $e_b(k)$ and $e_x(k)$ are zeros.

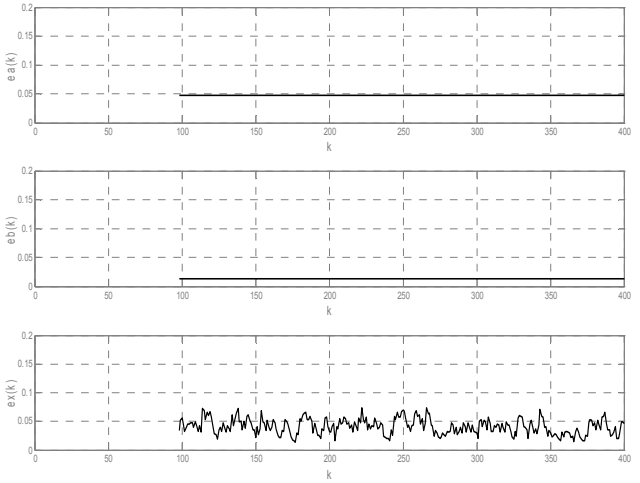

Fig. 2. RMSE for the case of noise-corrupted output signal, N=3n+2l=98

In the case of noise-corrupted output signal experiment is carried out for noise level η=*10.018* and *l=40* (i.e. *N=3n+2l=98*). The results are shown in fig.2. The algorithm starts working at the 98th step of the calculations and the RMSE are as follows: $e_a(k)<0.053$, $e_b(k)<0.014$, $e_x(k)<0.081$.

Another experiment is carried out for the noise-corrupted output signal case for noise level η=*10.018* and *l=100* (i.e. *N=3n+2l=218*). The results are shown in fig.3. The algorithm starts working at the 218th step of the calculations and the RMSE are as follows: $e_a(k)<0.041$, $e_b(k)<0.01$, $e_x(k)<0.055$.

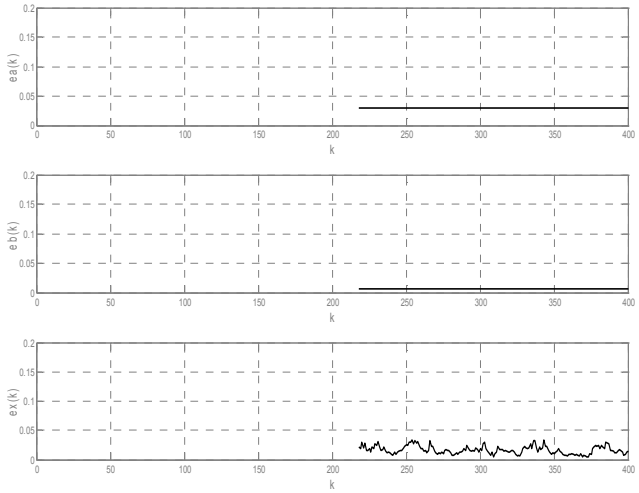

Fig. 3. RMSE for the case of noise-corrupted output signal, N=3n+2l=218

The conclusion that can be drawn from the graphs shown is that the increasing of the number of the input-output measurements (N) increases the algorithm noise resistance (the estimation errors decrease) but the time for initial data collection also increases. In order to remedy the drawback mentioned above the estimation could start when the number of the measurements is minimum, $N=3n$, and further during the calculations (when the number of the input-output measurements increases continuously) the number of the covariance matrix rows to be increased.

The results from such a computer simulation are shown in fig.4. After the 150th step of calculations (i.e. $N>150,l>66$) the estimation errors are as follows: $e_a(k)<0.056$, $e_b(k)<0.015$, $e_x(k)<0.059$. At the end of the estimation process $l=191$.

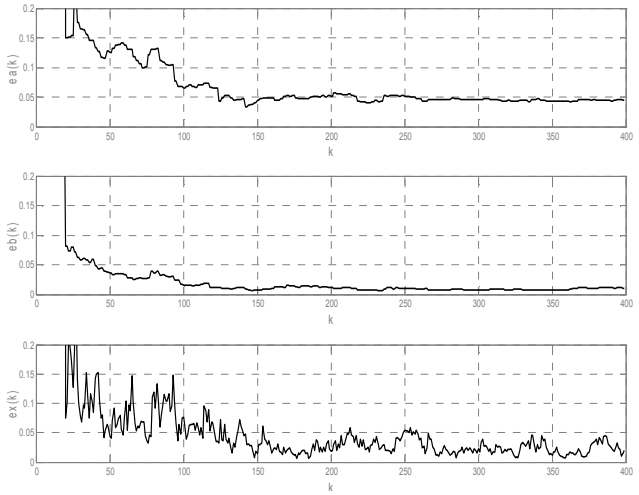

Fig.4. RMSE for the case of noise-corrupted output signal, N>150,l>66

V. Conclusion

From the results shown in fig.2-fig.4 it is easily seen that the number of the input-output measurements (N) is of major importance for the estimation accuracy in case of noise-corrupted output.

However, the greatest advantage of the developed algorithm is in the way the covariance matrix is formed. It is formed by using of the four submatrices $\mathbf{Y}_{11}$, $\mathbf{Y}_{21}$, $\mathbf{U}_{12}$, $\mathbf{U}_{22}$. In this manner the computational complexity of the procedure (due to the inversion of the matrix $\mathbf{G}$, consisted of the matrices $\mathbf{G}_{11}$, $\mathbf{G}_{12}$, $\mathbf{G}_{21}$, $\mathbf{G}_{22}$) is significantly decreased. Regardless of the number -N,of the input-output measurements, for coefficients h_i и a_i estimation only the matrices $\mathbf{G}_{11}$ and $(\mathbf{G}_{22}-\mathbf{G}_{21}\mathbf{M}_1\mathbf{G}_{12})$ are inverted, which are always with dimensions (n x n). At all other cases this procedure includes inversion of a (N-n)x(N-n) - dimension matrix.

The necessary condition for algorithm noise resistance is $l>1$, and the maximum of N should be determined according to the hardware (computer) used for the calculations. Once the maximum N_{max} of the input-output data is reached, the "data window" should start moving to the right at each calculation step when a new measurement is added and the leftmost element is dropped out of the calculations.

The suggested adaptive estimation algorithm is suitable to be used in the case of noise level not more than 5% since the measurement errors values are not greater than 0.005. In the case of high noise levels the LS method should be combined with some other estimation methods in order the estimation accuracy to be increased.

The developed algorithm is based on a direct (non-recurrent) estimation method so there is no danger of a lack of the procedure convergence. It can be used together with the algorithm shown in [6].

VI. Acknowledgment

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A Floating-Gate Array Based Discrete True-Random Stream Generator

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Abstract – **A simple and yet extremely effective digital hardware true-random number generator is presented. It is capable of operating as a memoryless source and as both a Markov chain source and a hidden Markov model source, with flexible switching between these modes. The device has a scalable design and demonstrates a remarkable performance.**

Keywords – **True-Random Number Generation, Random Source Simulation, Floating-Gate Device**

I. Introduction

True random data generation has a decades-long history. A wide variety of solutions have been invented during this time, e.g. [1], and no one can escape the requirement for a physical process at its core. Unfortunately, both practice and recent theory [2] persuade that the ideal true randomness lies in the quantum area and anything else is just a decent (or not so) approximation. However, most real applications are satisfied with the non-quantum alternatives. Each individual application imposes its specific demands – from a highest unpredictability of the next value in cryptography to an intended statistics of a huge amount of random data in stochastic simulations.

This article proposes a kind of generator whose nature is far away from quantum and which utilizes a rather undesirable technical phenomenon – the instability of a non-volatile floating-gate transistor (FGT) memory cell, when put in a proper region of its characteristics. The basic idea is outlined in [3] and this paper presents its further development towards a fully functional device.

The author's thorough search for a solution on a similar basis did not find any, so this one is considered original.

II. Basics

In brief, the idea in [3] is to make use of: 1) the various kinds of noise present in the FGT of a non-volatile memory cell when properly loaded with charge and 2) the unstable behavior of the subsequent threshold circuitry when put in boundary conditions. It is possible to load a precise amount of charge into the floating gate and thus to control the exact probabilistic behavior of each memory cell's digital output. Besides, every modern non-volatile memory device comprises of hundreds of thousands or even millions of cells and each one of them is a standalone randomness generator. These facts not only compensate for the deficit of theoretical guarantee for perfect true randomness, but even contribute to some benefits of practical importance: massive production of random data at high rates; various randomness probability adjustments; complex modes of operation; simple and elegant design; and last but not least – an impressively low cost.

The choice to use EPROM ICs as floating-gate array devices is motivated in [3], too. The follow-up work and newly set goals impose use of ICs with parallel input addresses and parallel output data. Though being an outdated technology, these are mostly the latest generation of EPROMs and as such possess good performance – e.g. ST's M27C512-45XF1 offers "Address Valid to Output Valid" times down to 45ns.

III. EPROM Programming for Randomness

In order to achieve a predetermined probability model (PM) of each cell's output, a sophisticated programming procedure is devised. A required precondition is that the EPROM be in a completely erased state.

Fig.1 depicts the common manufacturer recommended algorithm for reliable programming of a single FGT cell:

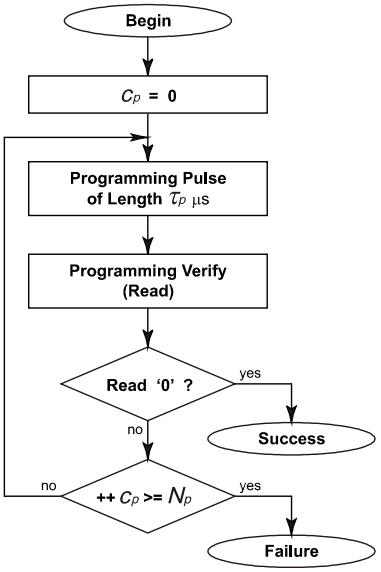

Figure 1. FGT Cell Reliable Programming Flowchart

Here: τ_p and N_p are the manufacturer recommended values for programming pulse duration and maximum allowed number of programming cycles for a cell.

Achieving the goal to pump a very precise amount of charge into the cell's floating gate, in order to get a pre-determined probabilistic behavior at the cell's output, obviously requires the much more complicated Fig.2:

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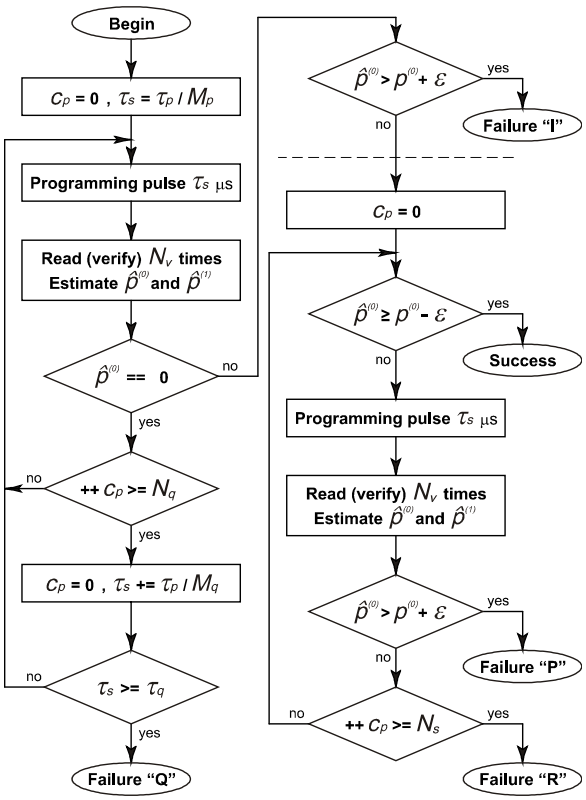

FIGURE 2. FGT CELL PARTIAL PROGRAMMING FLOWCHART

Here are the parameters: $p^{(0)}$ is the target probability that the cell reads as "0" in normal operation; $\boldsymbol{\varepsilon}$ is the acceptable deviation from $p^{(0)}$; $\boldsymbol{M_p}$ and $\boldsymbol{M_q}$ are factors by which to derive (by dramatically scaling down $\boldsymbol{\tau_p}$), respectively, the initial value and the update step (upwards) of the programming pulse duration ($\boldsymbol{\tau_s}$) for partial programming; $\boldsymbol{\tau_q}$ is the upper limit for $\boldsymbol{\tau_s}$; $\boldsymbol{N_q}$ and $\boldsymbol{N_s}$ are the maximum allowed number of programming cycles in, respectively, the initial and the main phase; $\boldsymbol{N_v}$ is the number of times a cell should be read right after every pulse in order to accumulate statistics about "0" and "1" reads and hence to calculate the respective probability estimations $\hat{p}^{(0)}$ and $\hat{p}^{(1)}$. Fig.2 shows how the flowchart can be divided in two phases: the initial one (before the dotted line), where the shortest possible programming pulse that is able to inject charge into the cell's floating gate is determined; the main phase, where the goal is to pump the needed amount of charge as precisely as possible, in order to reach $p^{(0)} - \varepsilon \le \hat{p}^{(0)} \le p^{(0)} + \varepsilon$. The flowchart has several "failure" outcomes for diagnostic purposes.

This procedure is able to achieve any PM $\{p^{(0)}, p^{(1)}\}$ for each cell in the EPROM array. When certain cells make up the parallel bits in a register-like structure at a given address, a proper programming word is used with a single "0" for the corresponding bit while the procedure is performed at the given address. After successful completion, the next cell (bit) in the word at the address is programmed by changing the programming word ("0" shift) and executing the same procedure. This way, it is possible to program completely different behavior in every single bit of the same word at the same address. Even if different cells in a word have to be loaded with the same PM, they must be programmed separately due to the differences in their physical characteristics – gate oxide layer thickness, floating gate volume, control gate area, etc.

IV. HIGH-LEVEL GENERATOR DESIGN

While considered at conceptual level, the idea to have an array of several hundred thousand independent binary true randomness generators with their own distinct PMs on a single chip implies a myriad of opportunities.

But in reality most mass-produced EPROM ICs offer a restrictive interface to the outer world. Fig.3a presents a generalized model of an EPROM "block", based on the common EPROM IC interface – parallel M-bit address input (A), parallel N-bit data output (D), chip select input (CS) and output enable (tri-state control) input (OE) :

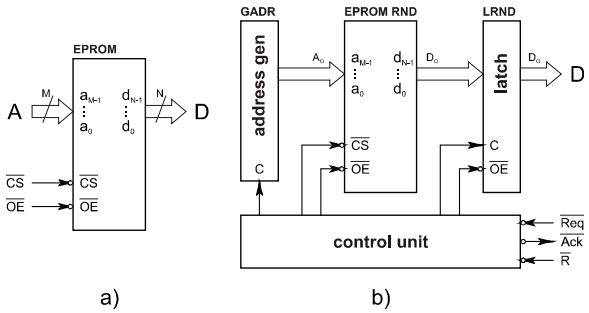

FIGURE 3. STRAIGHTFORWARD EPROM GENERATOR

Fig.3a's EPROM block is helpless without a valid address on A and a proper control of CS and OE. Hence Fig.3b – 1) a hereafter called "control unit" (CU) is introduced, and 2) a level-clocked address generator (AG) appears. The latter needs some clarification – a fixed address will do it, too, but at a given time the N-bit data output gives access to only N of all the above mentioned several hundred thousand cells. Why loose the rest? Any finite-state machine with uniform output timing distribution is suitable for AG, e.g. a high speed M-bit counter.

There is one more problem: even if properly addressed and controlled, the EPROM block will produce unstable data output during a single, but not extremely short reading cycle. This explains the edge-clocked latch, with a tri-state output in order to resemble the EPROM's one.

A few words about the three lines at the right edge of CU – they provide the handshaking, needed to acquire a single N-bit random word from the generator.

A. Memoryless (ML) Source Case

Fig.3b structure is itself a memoryless source of N-bit random binary words, provided all 2^M addresses are programmed with the same PM.

An explicit definition of PM is now necessary. Let $W_q = b_{q,N-1}b_{q,N-2}...b_{q,k}...b_{q,1}b_{q,0}$ be an N-bit binary word and $b_{q,k}$ is its k-th bit. Then $P_q^{(O)} = P(D_O = W_q \mid A_O = A)$ is the probability that W_q is read at the output D_O, if A is applied on the input A_O. So, the set $\mathbf{P^{(O)}}=\{P_q^{(O)}\}$, $q = \overline{0,Q-1}$, $Q = 2^N$, is the PM of D_O at $A_O = A$. Actually, A is of no importance, if all addresses expose the same PM, and so A is from now on missing in the notation.

Further: Let b_k be the k-th bit of D_O, no matter which W_q is read. Then $p_k^{(b)} = P(b_k = b \mid D_O)$, $b \in \{0,1\}$, is the absolute probability that the k-th bit reads as b. Having in

mind that $p_k^{(0)}$ is the target probability of "0" reads when programming the cell behind b_k, so let the set $\mathbf{p^{(0)}}=\{p_k^{(0)}\}$, $k=\overline{0,N-1}$, be the target bitwise PM at address A.

Furthermore: Let $p_{q,k}^{(b_{q,k})}=P(b_k=b\,|\,D_O=W_q, b_{q,k}=b)$ be the partial contribution of $b_{q,k}$ to $p_k^{(b)}$.

Finally, here are some important dependencies:

$$\sum_{q=0}^{Q-1}P_q^{(O)}=1 \quad P_q^{(O)}=\prod_{k=0}^{N-1}p_{q,k}^{(b_{q,k})} \quad p_k^{(b)}=\sum_{q=0}^{Q-1}p_{q,k}^{(b_{q,k})} \quad p_k^{(0)}+p_k^{(1)}=1 \quad (1)$$

a) b) c) d)

Special attention should be paid to (1.b) and (1.c). They are the links that define the mappings $\mathbf{F}:\mathbf{p^{(0)}}\rightarrow\mathbf{P^{(O)}}$ (forward task) and $\mathbf{B}:\mathbf{P^{(O)}}\rightarrow\mathbf{p^{(0)}}$ (backward task). The forward task is, actually, solved by the normal generator operation, and the backward task solution, by calculation, is required in order to program the EPROM block.

And here comes the real trouble: the nature of $\mathbf{F}$ and $\mathbf{B}$ is such, that in general $\mathbf{F}:(\mathbf{B}:\mathbf{P^{(O)}})\neq\mathbf{P^{(O)}}$! The latter is not true only for specific cases of $\mathbf{P^{(O)}}$, that fulfill certain conditions and these grow more complex as N increases. Fortunately, one particular useful case of $\mathbf{P^{(O)}}$ is the uniform one – when $P_u^{(O)}=P_v^{(O)}$, $u,v=\overline{0,Q-1}$.

This makes Fig.3b structure inapplicable. The solution is to divide the generation in two stages – a uniform generator, whose output is then mapped to form the final output codewords, according to their specific PM. This is shown on Fig.4, where two EPROMs implement the stages:

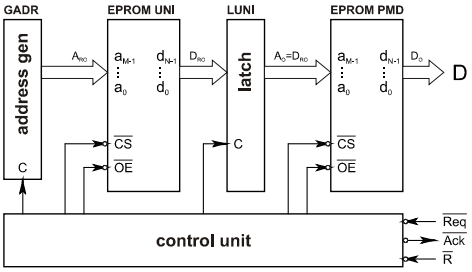

FIGURE 4. CODEWORD MEMORYLESS GENERATOR

Fig.5 shows how the EPROMs are programmed: UNI (a) with a uniformly random PM at each address; PMD (b) with a reliably programmed output codewords $O_q=W_q$, mapped onto the partitioned address space, each partition's size proportional to $P_q^{(O)}$ of the corresponding codeword.

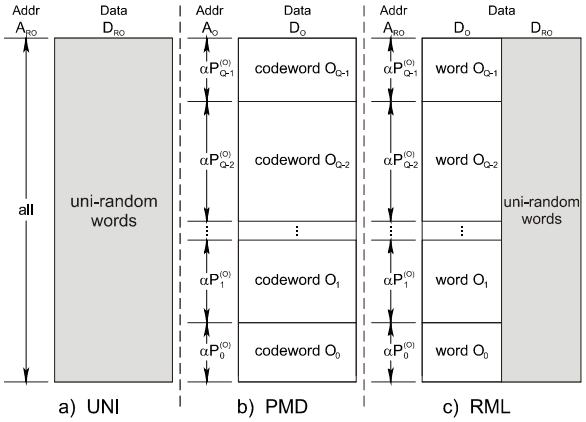

FIGURE 5. EPROM MAPS – MEMORYLESS CASES

Once a uniformly random generator (UNI) is in place, its own output can be used to feed itself with addresses and thus to eliminate the need for AG. This feedback makes UNI a stochastic automation, but the output remains memoryless due to the uniformity. Fig.6 shows the details:

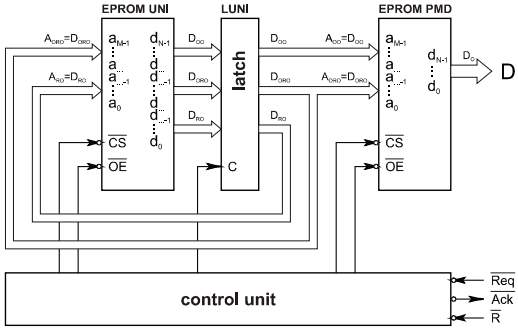

FIGURE 6. ADDRESS LOOPBACK CODEWORD GENERATOR

The idea to have a part of UNI's output, D_{ORO}, as both a feedback and an outer-output producing factor is a bad one, due to the theoretical decrease in output's unpredictability. As such, both the idea and D_{ORO} disappear further.

A little more thinking over and reminding that each distinct cell at the same address can be programmed separately and entirely differently, allow speculation about merging UNI and PMD into a single block, seen on Fig.7:

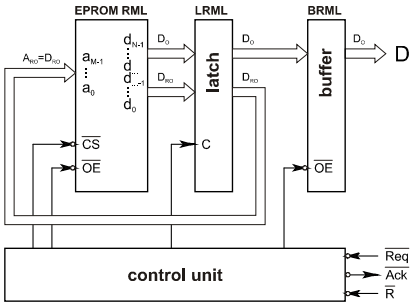

FIGURE 7. SINGLE-EPROM MEMORYLESS GENERATOR

The merged RML is wisely programmed as shown on Fig.5c – at each address part of the bits (D_O) encode the output codeword and the rest (D_{RO}) produce the uniformly random address feedback.

B. *Markov Chain (MC) Source Case*

What if the output of Fig.7 structure is fed back to control the next emission ? Depicted on Fig.8:

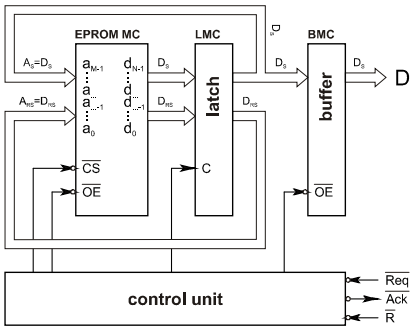

FIGURE 8. SINGLE-EPROM MARKOV CHAIN GENERATOR

If a proper control is embedded in the EPROM, then this becomes, actually, a Markov chain generator.

What does a proper control mean ? First, the output codewords should be considered MC state codewords. Second, the EPROM mapping, shown on Fig.9a, introduces two levels of address space partitioning – the outer one divides the whole space in V (states number) equi-sized

parts, one for each current state S_i, $i=\overline{0,V-1}$, and the inner one, which maps the transition probabilities $P_{ij}^{(S)}$ to the next state S_j, $j=\overline{0,V-1}$.

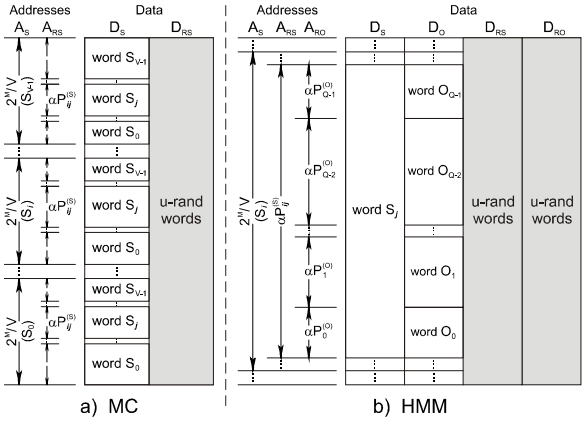

FIGURE 9. EPROM MAPS – MC AND HMM CASES

Every time the EPROM is read, it outputs on D_S the appropriate next state S_j codeword, depending on the current state S_i codeword, applied on A_S, the transition probability $P_{ij}^{(S)}$ and some uni-randomness, applied on A_{RS}.

C. Hidden Markov Model (HMM) Source Case

If there are MC and memoryless generators available, it is possible to cascade them, obtaining a HMM one, Fig.10:

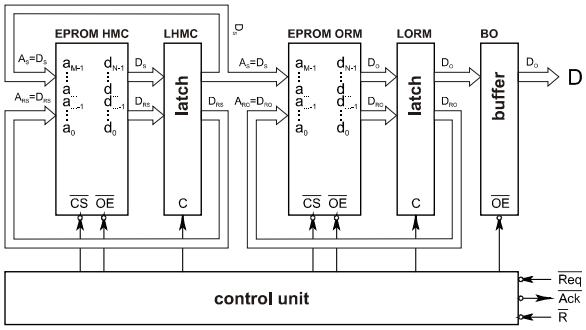

FIGURE 10. HIDDEN MARKOV MODEL GENERATOR

By induction, merging is possible, to Fig.11 structure:

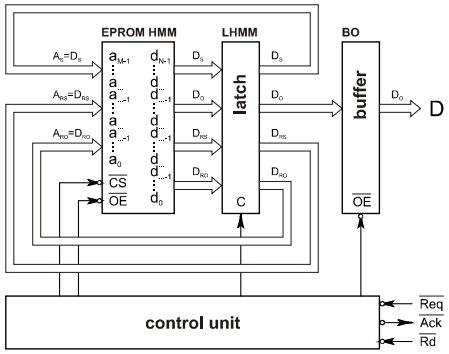

FIGURE 11. SINGLE-EPROM HMM GENERATOR

The EPROM mapping, Fig.9b, is devised by induction, too, with third, the observation, level of partitioning added.

V. MIDDLE-LEVEL GENERATOR DESIGN

High-level design structures from Fig.7, Fig.8 and Fig.11 are integrated and transformed to a middle-level design, presented in Fig.12:

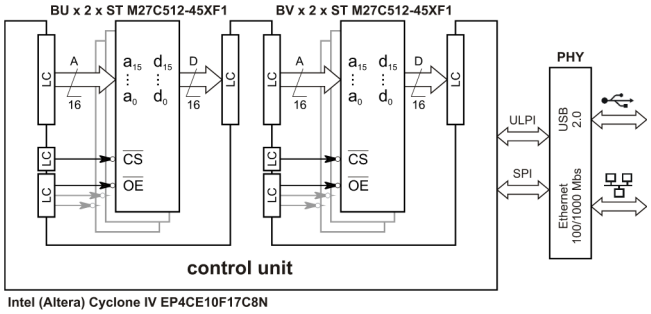

FIGURE 12. MIDDLE-LEVEL PROTOTYPE GENERATOR DESIGN

There are several guiding ideas:

– To this stage, a prototype is in design.

– The control unit is implemented by FPGA. The actual model is chosen for its resourcefulness, large number of GPIOs and development kit availability.

– There are two EPROM block banks, each block consisting of two ICs, with: address inputs connected in parallel, control inputs driven separately, and data outputs in union to form larger output word.

– Level conversion (LC) circuitry is required.

– Outer world communication should be done by popular high-speed interface – USB 2.0 and/or Ethernet.

– Outer world communication is bi-directional, because there is need to choose mode of operation, to set the initial state (for MC and HMM cases), etc.

VI. RESULTS AND FUTURE WORK

Tbl.1 presents some results regarding the performance of several configurations :

Configuration / Output	Blocks		Output Rate
	U	V	
ML uni-random bit-stream, less security		1	267 Mbps
ML uni-random bit-stream with more security	1	1	267 Mbps
ML uni-random bit-stream with more security	1	2	320 Mbps
ML uni-random bit-stream with more security	1	3	342 Mbps
ML uni-random bit-stream with less security	1	1	533 Mbps
ML model codeword stream – 64 codewords		1	17 Mwps
ML model codeword stream – 64K codewords	1	1	17 Mwps
MC state codeword stream – 64 states		1	17 Mwps
HMM observation codeword stream – 8 states , 8 observations		1	17 Mwps

TABLE 1. EXPERIMENTAL CONFIGURATIONS PERFORMANCE

Future work will be focused on even better performance and in control unit firmware improvement, so that if high-speed or high-volume output is not required, the device can take advantage of the high-speed internal generation and yield higher quality uniformity and randomness by utilizing deterministic extraction.

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Further Development of the „E-Management“ Platform for Electronic Management and Control of the Education

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Abstract – This paper presents the new functionalities which have been introduced to the "E-Management" platform for management and control of the educational process. Functions related to facilitation of teachers' tasks and traceability of the process are shown. The results from their application to different subjects at different faculties and year of study are described. Part of the results acquired during the last decade of usage have been statistically processed.

Keywords – **electronic education, Internet control, management of the education, quality of the education**

I. Introduction

As the information technologies became more and more advanced, the electronic means for education became more and more spread. Mobile educational technologies were developed, too [1], as well as flexible platforms for different courses [2], cloud technologies for storage and processing of information [3], etc.

A. Electronic Education and Quality Control

In the sphere of education information technologies and electronic means could be reviewed in two directions.

The first one is the electronic means themselves, which include both virtual instrumentation like simulators, multimedia [4], and electronically constructed courses [5, 6]. Of course, the different means for assessment in the form of electronic tests, etc. are also present here.

The second one is related to the application of informational and electronic technologies for management of the process of education. The typical tasks in this direction are registration of participants and document issuing [7], individual sites of the educational institutions [8], assessment databases, etc.

B. Existing Functionalities of the "E-Management" Platform

The "E-Management" platform is an Internet based module for management and control of the educational process [9]. Functions typical for the educational process and students' activity stimulating bonuses have been gradually implemented in it [10]. Horizontal and vertical integration with platforms of the same kind implemented with other subjects, as well as other systems and databases, including an external administrative control could be performed [11]. The platform is oriented towards a total removal of paper documents related to laboratory exercises reports, results from students' assignments, students' assessment statistics, class attendance and certification for it [12].

A possibility for checking the credibility of different answers (including surveys) via parallel comparison of data from different systems [13] is implemented in the platform. The accumulation of different data from different subjects in the platform makes it possible to study the behavioural assessment of students and teachers [14].

A main advantage of the developed platform is its ability to be integrated with a centralised students' database system, which is used at the students' offices.

B. Aims of the Development

The ability of electronic means to collect, process and present different kinds of information is especially suitable for analysis of the individual and group behaviour in the educational process. That is why new functionalities are added to the "E-Management" platform in this respect. Those functionalities could be aimed at statistical processing of existing data, as well as accumulation of new types of data. For example, the activity in the educational process based on users' logins, which could be analysed in respect to the timely distribution of the logins, completion of the assigned tasks in time, or class attendance, etc.

II. New Functionalities

A. Activity History

The logins to the platform are chosen to be a parameter, which allows to trace back the activity in the educational process. All individual login times are being stored in the database. The history of students' and teachers' logins can be accessed by the main teacher - Figure 1.

A detailed list as well as the total of logins by weeks is available – Figure 2. The weeks are synchronised with the academic calendar of the semester. Holidays are included in the schedule, so the total number of weeks is greater that the number of weeks in the semester.

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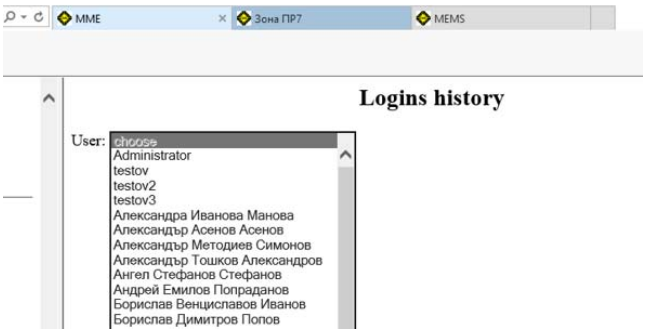

Fig. 1. List of users – teachers and students.

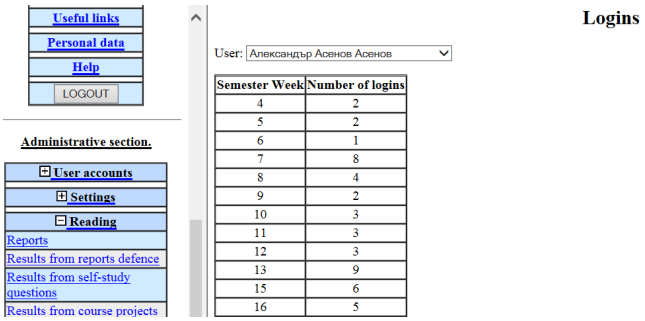

Fig. 2. Table with logins by weeks for a selected user from the site of the subject Materials in Microelectronics – 4th year of study.

B. Participation in the Educational Process

The ability to store the time of task submission related to lectures, laboratory exercises or seminars, self check-in time for different classes, class attendance with groups other than the student's one, etc. was implemented in a previous version of the platform.

A later development of the platform included the ability to send the self check-in keys for lectures and exercises by email or as a personal message – Figure 3. Up to that moment the only way was to print, cut and give the self check-in keys to each student at classes.

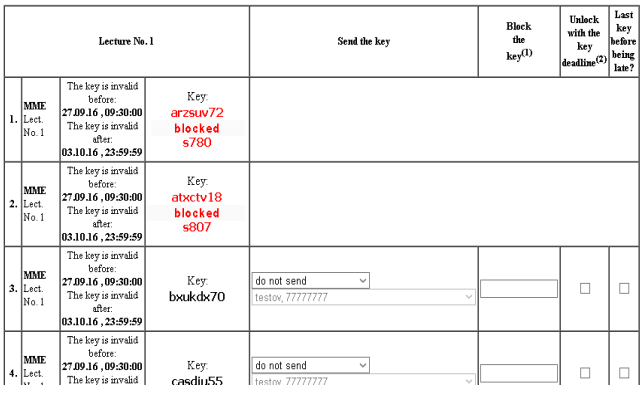

Fig. 3. Table with self check-in keys management from the site of the subject Materials in Microelectronics – 4th year of study.

The teacher starts giving the self check-in keys to the students starting from the first one. The keys are alphabetically ordered. When the first student comes, and he/she is already late for the lecture, the teacher marks that key in the last column. All next keys are automatically marked like the first one. In this way the statistics related to lecture attendance looks like the ones shown in Figures 4 and 5. The yellow cells denote a student who was late for the lecture.

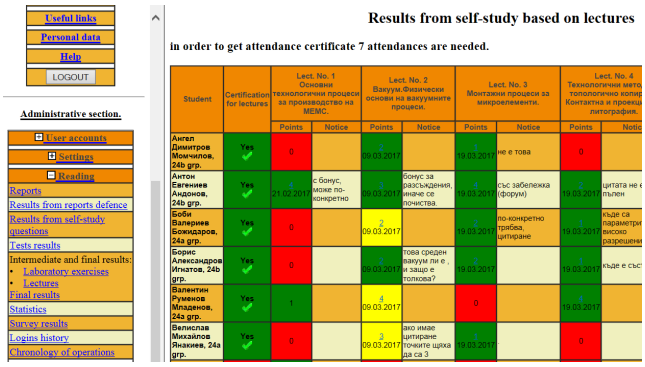

Fig. 4. Table representing lecture attendance and showing late students from the site of the subject Microelectromechanical systems– 3rd year of study.

The absent students are denoted in red (0 points). The red colour could also mean that the student got a key but did not perform a self check-in.

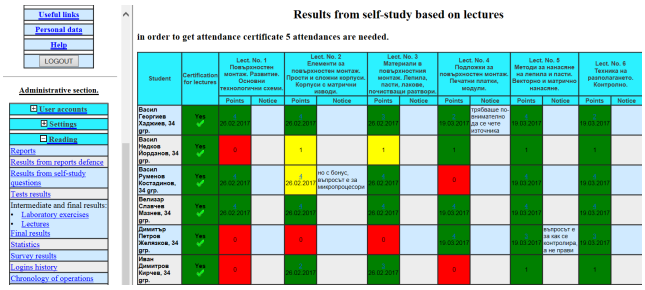

Fig. 5. Table representing lecture attendance and showing late students from the site of the subject SMD technique – 4th year of study.

II. Results and Discussion

A. Activity

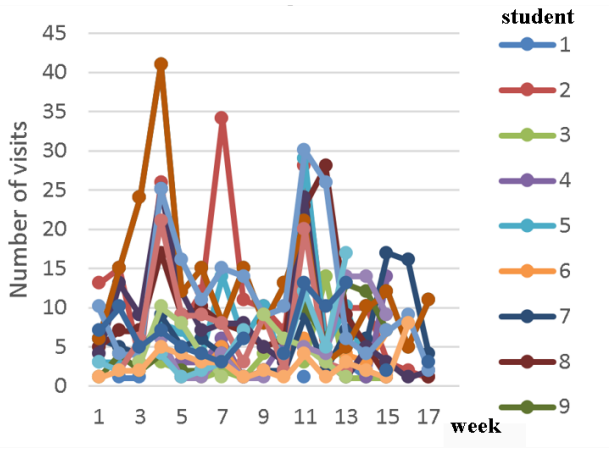

Fig. 6. Logins of 9 students to the site related to the subject SMD technique.

A study of users' logins was carried out, without taking into consideration the duration of work, which was used as a criterion for the activity. 20 students were the subjects of

the study, without taking into account their marks, sex, etc. The study covers their logins during the semester and two weeks after that. The presented results are related to students from the Faculty of Industrial Technologies and the Faculty of Electrical Engineering at the Technical University of Sofia. The students are in their first, third and fourth year of study. The form of assessment of the subjects is examination, ongoing assessment or none – Figures 6, 7 and 8.

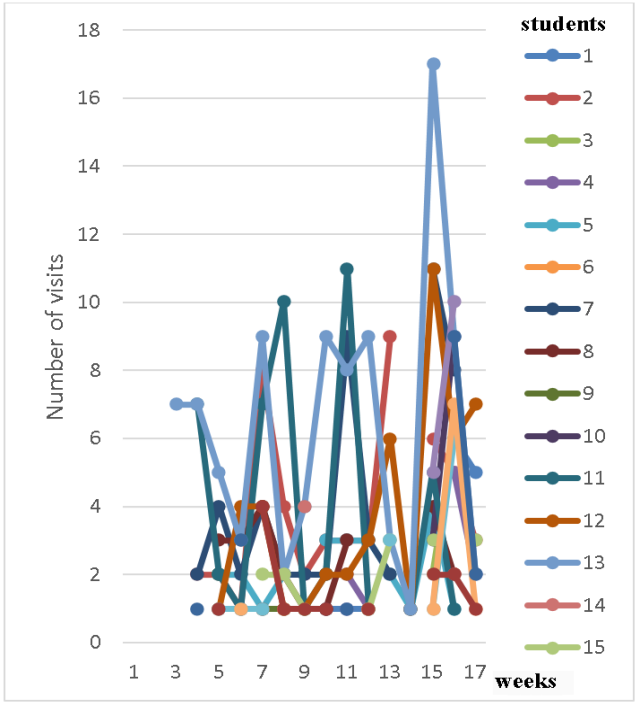

Fig. 7. Logins of 15 students to the site related to the subject Materials in Microelectronics.

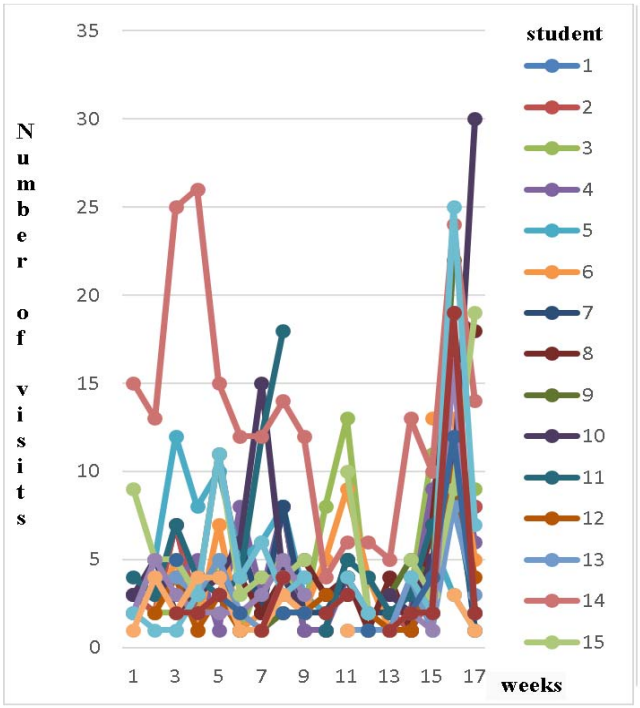

Fig. 8. Logins of 15 students to the site related to the subject Microelectromechanical Systems.

Logins to the sites related to the subjects Microelectromechanical systems and SMD Technique, during the period when tests for the ongoing assessments were performed, are shown in Figure 9.

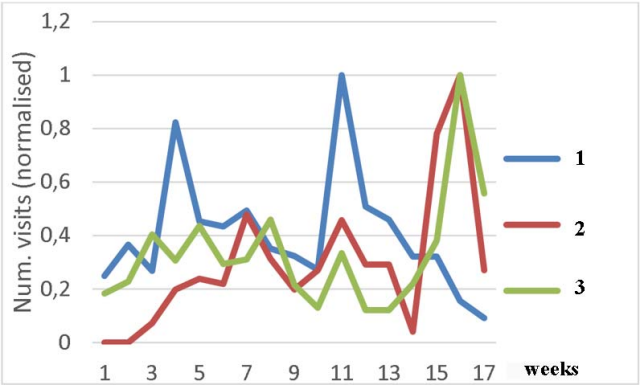

Fig. 9. A summary of the logins to the sites of the three subjects. tpm – SMD Technique, mme – Materials in Microelectronics, mems – Microelectromechanical Systems.

B. Classes

After applying the new function related to distinguishing students who are being late for classes, result similar to the one show in Figure 10 were obtained.

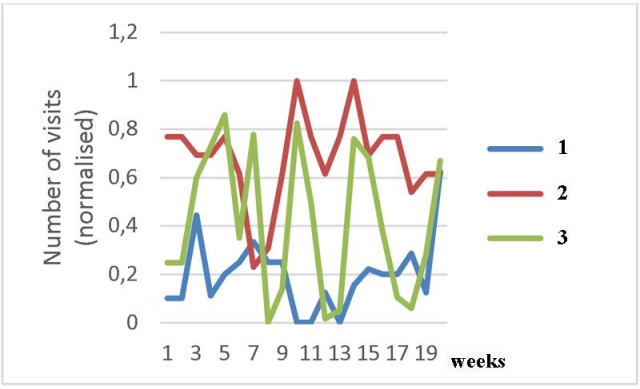

Fig. 10. Late students, students in time and test results in the subject Microelectromechanical Systems. 1 – late students, 2 – class attendance, 3 – tests.

C. Some comments

After reviewing the individual students' data, it is hard to tell any typical dependencies. The region of activity at the different subjects varies with more than one order of magnitude. Depending on the type of the subject's assessment, the average site visits differs several times.

However, the analysis of the summarised parameters shows the expected dependencies. Site visits for ongoing assessments disciplines are two to four times greater in the weeks around the tests. In the subjects with examination and no assessment, visits are concentrated in the last few weeks. This number is again several times greater than the average.

The results of the comparison of the attendance and the students being late during the lectures are interesting. With the exception of the 100% of the students present at lectures, the late students are 20 % at all other subjects' classes, which is about 20% of the number of classes attended.

Again, a dependency exists that there is no exact correlation between the type of assessment and class attendance. Only in the case of a correlation between high attendance and an average score of the assessment it can be said that there is a connection. There are also cases of low attendance but relatively high grades.

III. CONCLUSION

The processing of the results from the function for logging site visits, which was implemented at the "E-Management" platform, shows the ability to define students' commitment to the educational process with respect to the types of assessment – none, examination and ongoing assessment. It can be underlined for sure that there is a more constant commitment to subjects where there is an ongoing assessment.

No unambiguous relation can be established between class attendance and results from ongoing assessment. Maybe it is more suitable to assign tasks in respect to each lecture in addition to unrestricted lecture attendance.

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Implementing University Learning Approaches in Secondary School Education

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Abstract –**The paper considers introduction of collaborative project based learning at the Technology School "Electronic Systems" associated with the Technical University of Sofia. It discusses how the Global Networks course was restructured to apply team work on shared project with using cloud computer technologies. The organisation and outcomes from conducted pilot courses are briefly reviewed. The benefits of introducing new learning approaches and collaborative cloud computing technologies in supporting school students to acquire new competencies and skills are also commented.**

Keywords – **Knowledge work practices, Cloud technologies, Collaborative learning, ICT education, Digital competences**

I. INTRODUCTION

Rapid changes in technology and related innovations stimulate the development of the knowledge economy. This industry changes the requirements of the labour market in terms of new competencies and skills. Teamwork, ability for problem solving, using information and communication technologies (ICT), as well as lifelong learning skills are needed [1].

The emergence of the knowledge-based industry is accompanied with increasing investments in ICTs and the expansion in the use of the Internet. ICT business companies are looking for staff with a mix of technical and management skills, working in multidisciplinary and multicultural teams, with abilities to communicate and networking, capable of solving complex problems and coping with challenges.

Education systems have to respond to the challenge and prepare people with ever-increasing and varied skills for the needs of the changing knowledge economy. Present-day students will be employed in professions that do not exist today, which will require modern knowledge work. To participate effectively in the knowledge economy today's learners have to develop required competences.

New trends in the 21st century require a new learning model. Traditional approaches apply simple procedures and rely on memorizing facts. In the knowledge society such approach is not enough because it does not develop critical thinking and problem solving ability. The predominant lecture model, which is still a widespread instructional approach in education, is highly inefficient for teaching 21st century skills. It typically leads to students' disinterest and apathy. The way young learners from the Internet generation learn is different and continue to change. It is obvious that the way of teaching also has to change as to respond to the growing needs.

Formal education must be transformed to enable new pedagogical practices to cope with complex global challenges [2]. Graduates need a deeper understanding of complex issues and the ability to work in multidisciplinary teams to generate new ideas, new products and new knowledge. In order to achieve adaptation and integration of new knowledge, it is necessary to introduce new pedagogical approaches that give opportunity learners to practice and apply new knowledge in different contexts.

To promote required competences 21st century pedagogy [3] suggests developing pedagogical practices that:

- Create thinking skills;
- Use project based learning;
- Use problem solving;
- Use timely appropriate and comprehensive feedback;
- Use collaboration with appropriate technologies.

In order to meet these challenges, the KNORK (Promoting Knowledge Work Practices in Education) project [4] aims to develop pedagogical models and technologies that support collaborative practices with wide implementation of modern cloud technologies.

The paper discusses efforts done at the Technology School "Electronic Systems" associated with the Technical University of Sofia to reconstruct a course and pedagogical practices in Global Networks education to support collaborative learning with using cloud computer technologies. This approach helps learners in acquiring new competencies and skills to tackle challenges of knowledge economy.

II. GLOBAL NETWORKS COURSE REDESIGNING

The Global Networks course in the Technology School "Electronic Systems" is re-designed to be project oriented. This educational approach, normally used in universities, was chosen for applying at secondary professional school because it:

- Increases students' motivation and engagement;
- Betterment the students' practical abilities;

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- Permits team work on common tasks;
- Forms skills to assign timetable in order to handle specified deadline;
- Develops problem-solving skills;
- Creates abilities of networking and communications

To promote students' knowledge work competencies we have transformed the Global Network course from traditional face-to-face to applying collaborative project based learning. A new trialogical educational approach was introduced. The knowledge creation approach to learning is called 'trialogical' because it emphasizes the role of shared objects produced instead of concentrating on individuals' learning (a monological approach) or just on interactions between people (a dialogical approach) [5].

The details of trialogical design principles [6] and their implementation for introducing collaborative project based practices at secondary Technology School "Electronic Systems" are considered in [7].

Instead of giving 12th grade school students many separate or lightly connected tasks accurately developed by the teacher we provide them with prolonged work on common project within 31 weeks. All team activities are organized around shared objects – development of common project, preparation of shared report, continuous working process, and final presentation in teams. During this process students learnt to manage their work, to distribute tasks between team members, to critic and reflect on others' work. Continuous monitoring and teacher assistance in this process is ensured by applying cloud computing technologies and up-to-date communication tools.

III. Collaborative Environment

During the continuous collaborative project development a significant part of the work (research, design and analysis, consultations, discussions, teachers' comments during design phase, in team communications etc.) is done outside regular class. This requires an environment supporting common work and communications to give students opportunity to work collaboratively in group with clear role of each participant.

Fig.1. Collaborative cloud tools used

Interaction with digital and mobile technologies is a daily life for young people. Despite this trend, mobile technologies have not yet found a place in education. Where appropriately used, technologies can provide tools for continuous monitoring and support and offer many forms of learning. The appearance of new cloud computing technologies enabled introducing of innovative forms of collaboration. The use of cloud capability allows access to networks and provides on-demand connection to available resources, people and tools.

The collaborative environment chosen for project based learning in Global networks course is shown in Fig. 1.

The public cloud based services are organised in a way that support cooperative development of common project between team members. Google Drive, Docs, and Sheets are used for preparation of common shared report. Google calendar facilitates project management and progress monitoring during long term project development. It sets dates for individual homework assignments, deadlines for intermediate stages reporting and final project submission.

For inter team communications students can choose whatever tools they prefer (e-mail, conferences chat, forums). Student-teacher communications are performed through Google applications Calendar, Gmail, Drive and Google+.

All school students had to register individual Google accounts. Projects are developed collaboratively in one semester and during long term period school students prepare shared common report using Google Drive. Google Docs allows creating text, graphics, equations, uploading pictures, screenshots with simulation results and measured data in the shared report etc.

The collaborative learning environment helps students to discuss ideas with colleagues, exchange different view points, ask questions and get answers, manage and organize the work process, make critical analyzes, solve problems and create new knowledge, and deeper understanding.

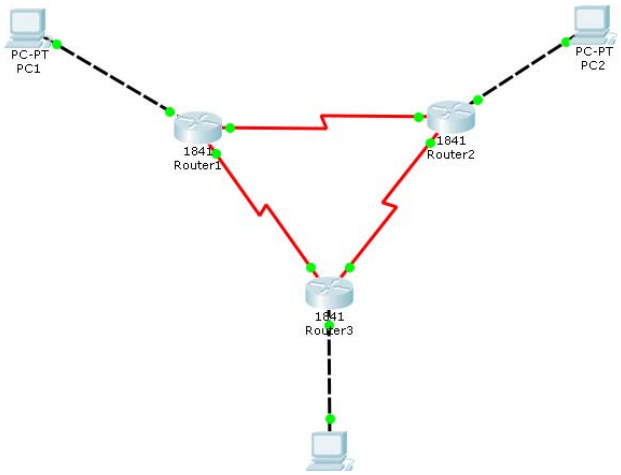
Cloud computing in combination with personal mobiles helps students manage their collaborative work with other team members and easy communicate with educators and industry experts.

IV. Results from Pilots

Secondary school students from 12th grade have to perform collaborative network design (Fig.2). To facilitate learning process along with long-term project development, the school students are provided with several individual homework assignments, which cover the main stones in the project subject area, to be easier for students to understand the particular topics. The students were required to fulfill and submit individual homework assignments.

School students work in teams of two persons. They are required to perform iteratively number of analysis of the designed network, and to refine the network characteristics. During the long term projects development teams have to gather information, discuss the raised problems, analyze and troubleshoot the network topology applying pre-defined networking technologies and protocols – all in collaborative environment.

With project based approach, students learn subject matter by designing and constructing actual solutions to real-life problems in global networks, employing critical thinking, collaboration, communications, creativity and self-management.




```
R1(config)#interface g0/1
R1(config-if)#no shutdown
R1(config)#interface g0/1.2
R1(config-subif)#encapsulation dot1q 2
R1(config-subif)#ip address 157.113.72.1 255.255.252.0
R1(config-subif)#exit
R1(config)#interface g0/1.4
R1(config-subif)#encapsulation dot1q 4
R1(config-subif)#ip address 157.113.64.1 255.255.248.0
R1(config-subif)#exit
R1(config)#interface g0/1.8
R1(config-subif)#encapsulation dot1q 8
R1(config-subif)#ip address 157.113.76.1 255.255.254.0
R1(config-subif)#exit
R1(config)#interface g0/1.15
R1(config-subif)#encapsulation dot1q 15
R1(config-subif)#ip address 157.113.79.1 255.255.255.224
R1(config-subif)#exit
R1(config)#interface g0/1.25
R1(config-subif)#encapsulation dot1q 25
R1(config-subif)#ip address 157.113.78.1 255.255.255.0
R1(config-subif)#exit
R1(config)#
```

Fig.2. Collaborative network design

At every step of the development process the learners have to document their work and to upload solutions in Google Drive project space (Fig.3).

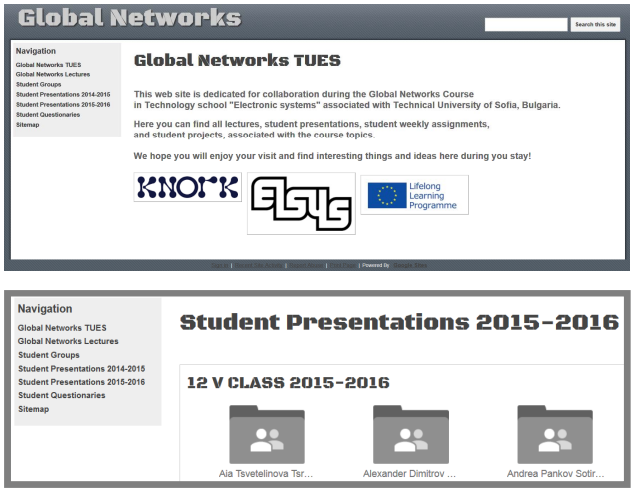


Fig.3. Collaborative Google Site

During continues working process, school students have iteratively to update network configuration, perform numerous analysis of the designed network, refine the network characteristics, write documentation, share drafts, ask teacher and other team members for feedback, improve the project report, submit respective report. At all stages students need support from teachers and industry experts for tasks clarification and help for decisions' correction.

Students submit their questions as in-document comment, which are context related. Teachers and experts answer with reply comments in the same document. The discussion is a part of the shared report as shown in Fig.4.

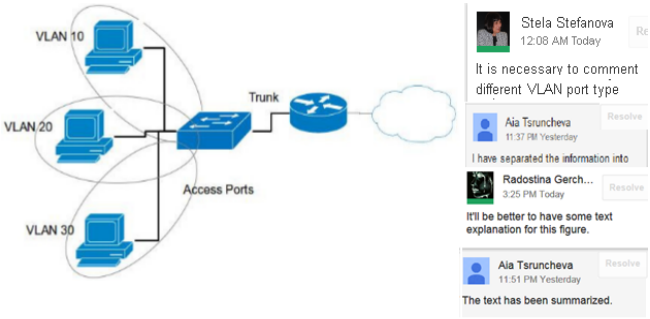


Fig.4. Student-teacher discussion as a part of shared document

Guidance is provided in the cloud environment and students are advised online on demand. This approach permits direct student-teacher contact that is not face-to-face, but is mediated through modern communications technologies. Independently that all players in online dialog are separated by place and time school students obtain help in time without waiting regular classes.

The final stage of project development aims at physical implementation of the designed network. Learning by doing approach is used for deeper understanding. Emphasis is placed on practical application of the developed network. Already designed network is configured in the laboratory by using dedicated networking equipment (Fig.5).

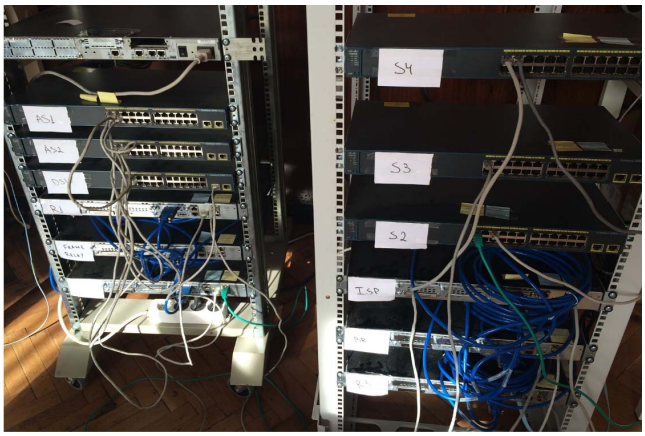


Fig.5. Group practice Lab and exercises

It is important to mention that even well guided during the long-term project work, the school students face difficulties to achieve required results. For this reason the teachers split the project in several parts with intermediate targets and specified deadlines to fulfill these tasks so helping students do not lose interest.

The process of project development is also evaluated in final assessment. Assessment criteria include quality of the shared project, individual contribution of each team member, participation in discussions, and fulfilling all intermediate and final tasks within predefined deadlines.

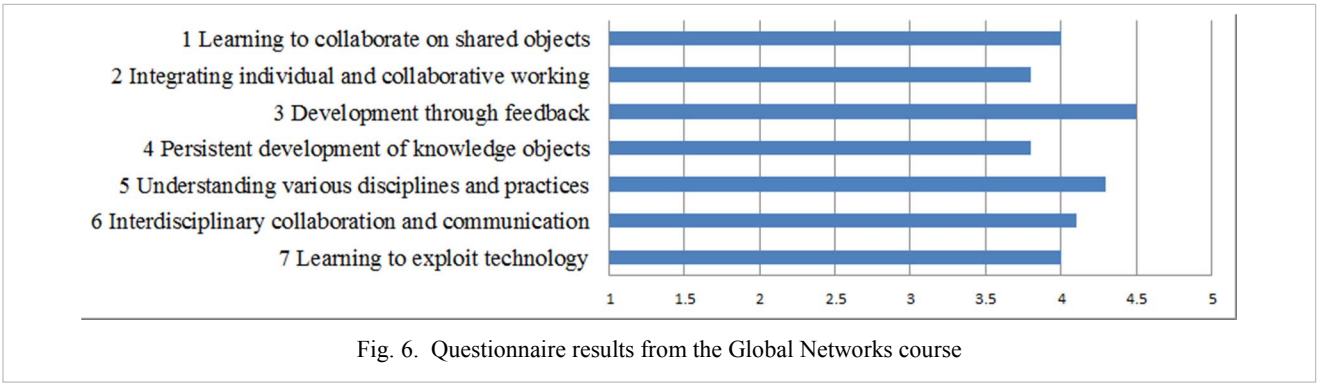


Fig. 6. Questionnaire results from the Global Networks course

School students are more engaged in learning when working collaboratively on authentic real-world contexts, carrying out projects from beginning to end, and solving problems as they arise.

At the end of the course, the questionnaires were used to ask the school students how they had learned collaboration and knowledge work practices during the Global networks course. The goal was to evaluate students' self-assessed competence-development during the project based course. The data were collected by an online form. The scales range from 1 (strongly disagree) to 5 (strongly agree).

Fig. 6 presents results of the questionnaire regarding the parts concerning what students feel that they had learned working collaboratively in teams on shared project. As can be seen the students consider the timely obtained detailed feedback and help from teachers as the most important and useful for their learning and deeper understanding. Opportunity to work on real-world projects helps them to comprehend and apply different disciplines and practices. Collaboration, working on shared projects exploiting cloud computing technologies and communications are very well accepted. They report that feel difficulties in integration of individual and collaborative work.

The questionnaire also includes open questions, which ask what the students consider as positive, challenging or disturbing in the course. Most of the students appreciate the new approach of course delivering and innovative way of team work using modern cloud technologies. They express their satisfaction of ability to learn new tools, to understand how important is the expertise and contribution of others in development of common project with a good quality. The opportunity for students to work at any place and at any time is stated as big advantage, which helps them to manage their time in more effective way.

Some of the students report for difficulties in task distribution especially if some team members are not sufficiently responsible for common work. The fulfilling and submission the project within fixed time are considered as the greatest challenge, since after the deadline projects are locked for editing.

V. Conclusions

The paper considers introduction of collaborative project based learning in computer networking education at secondary school. It discusses how the Global Networks course was restructured to introduce team work on shared project. The use of cloud technology to create learner-centered environment has been described and its advantages for collaborative work practices and deeper learning are also commented.

The results from pilot course in Global Networks in 12th grade classes are highlighted. As most important can be mentioned: deployment project based learning in secondary education; using research and problem solving as educational tools; using contemporary cloud technologies as common environment for cooperation with well-timed, adequate and comprehensive feedback and help; improving motivation, engagement and collaboration skills in students; getting students ready for real life social and job situations;

The greatest benefit was the competences gained by the school students, educated in new collaborative approaches. As a result the students won many prizes in the national and international competitions: Computer Networking, the largest global line trace type robot competition "Renesas MCU Car Rally 2016" in Germany, NASA Apace Apps Challenge 2017, ECER 2017 and other – all requiring strong team work and digital competences.

Acknowledgement

The work reported in this paper was supported by the EU KNORK (Promoting Knowledge Work Practices in Education) project at the Technology School "Electronic Systems" and the TU-Sofia.

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Improving the software quality - an educational approach

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Abstract – **The term "quality software" refers to software that is easy to maintain and evolve. The presence of Anti-Patterns and Patterns is recognized as one of the effective ways to measure the quality of modern software systems. The paper presents an approach which supports the software analysis, development and maintenance, using techniques that generate the structure of Software Design Patterns, find Anti-Patterns in the code and perform Code Refactoring. The proposed approach is implemented in a software tool, which could support the real phases of software development and could be used for educational purposes, to support "Advanced Software Engineering" course.**

Keywords – **Software Engineering, Software Design Patterns, Software Anti-Patterns, Software Refactoring**

I. Introduction

The presence of Anti-Patterns and Patterns is recognized as one of the effective ways to measure the quality of modern software systems. Patterns and Anti-patterns are related [1]. The history of software production shows that Patterns can become Anti-patterns. It depends on the context in which a Pattern is used: when the context become inappropriate or become out of date than the Pattern becomes Anti-pattern. For example, procedural programming, which was Pattern at the beginning of software production activity, with advances in software technology gradually turned into Anti-pattern. When a software solution becomes Anti-pattern, methods are necessary for its evolution into a better one. Refactoring is a general way for software evolution to a better version. This is a process of source code restructuring with the goal to improve its quality characteristics without changing its external behavior. In refactoring we replace one software solution with another one that provides greater benefits: code maintainability and extensibility are improved, code complexity is reduced.

The paper proposes an approach (Fig.1) that improves the software quality. The approach supports software analysis, software implementation and maintenance. It provides techniques that generate the structure of Software Design Patterns (DP), find Anti-Patterns in the code and perform Code Refactoring. As stated in [4] refactoring can be applied in different contexts; "improving the software quality" it is the high level context. This paper focuses on two specific refactoring contexts: "refactoring, to remove bad code constructions" and "refactoring, to implement design patterns".

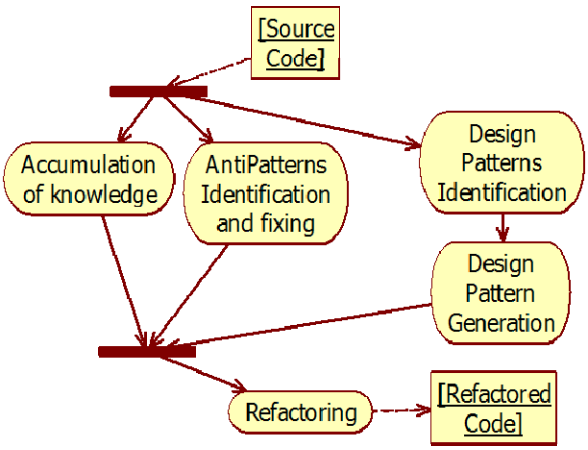

Fig.1 The general structure of the approach

The proposed approach is realized in a software tool that covers real phases of software development (Fig.2) and could be used by software engineers in their real work. The main purpose of the developed tool, however, is - to be an educational Instrument within the disciplines "Software Engineering" and "Software design Patterns" in "Software and Internet technologies" Department of the Technical University in Varna.

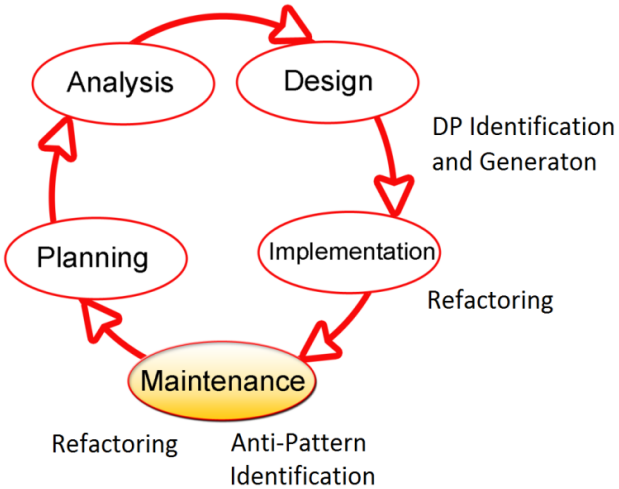

Fig.2 The approach supports real phases of software development

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Recent studies show that the development of refactoring tools is an active research ([1]÷[10]). At the same time, such tools are not enough used in practice. One possible raison is that most existing refactoring tools focus only on improving some quality metrics. Case technology leads to significant improvement of the software process, but not all aspects of software production could be easy automated. It is because software development is creative and team-based activity; large projects waste a lot of time for interaction between participants. These aspects of software production cannot be automated.

II. Our Approach

The general structure of our approach is presented in figure 1. It takes as input the software source code that has to be refactored. The output is refactored code. The approach relies on accumulation of knowledge about the best practices in programming so "Accumulation of Knowledge" is one of the processes that are performed in parallel with other processes. The refactored code is result of "Anti-Patterns Identification and fixing" and "Design Patterns Generation". Before generate Design Patterns it is necessary to analyze the code with the goal to find Design Patterns candidates. The proposed approach comprises the following main components:

- Accumulation of Knowledge: aims to provide information on design pat-terns and anti-patterns. It contains information about creational, behavioral and structural design patterns and software anti-patterns in software development and software architecture. Describe the problems that each design pattern solves, the advantages that it provides and the situations in which it is used. For the anti-patterns - the nature of the problems and possible options for their avoidance are described.
- Design Pattern Generation: provides functionality to generate sample implementations of the design patterns structures; basic elements and relationships between them are generated, it's not implementation of the solution of specific problem. To generate a template user must select appropriate names for key elements. Appropriate names for the key elements must be given by the user, in order to generate a pattern.
- Refactoring Component: provides methods for automatic code refactoring. The code is supplied as input of any method, as for inputs are accepted only properly constructed classes. Each method performs the appropriate changes and returns the modified code as a result.
- Anti-Patterns Identification and fixing: provides methods for code analysis. The code is supplied as input of a particular method and as result of code analysis the poorly constructed sections of code are colored. The colored code should be rewritten in order to increase its readability and maintenance.
- Design Pattern Identification: provides methods to examine source code and to identify candidates for design patterns. This component is still un-der development. Our detection strategy is based on the code inspection. Extensive research has to be conducted to develop techniques to automatically detect candidates of DP in the code.

III. Implementation

Based on the approach proposed a web system was developed. The system architecture is based on Model-View-Controller (MVC) pattern. Block "controllers" (Fig.3) includes five controllers managing the different sections of the application. „HomeController" manages the Main Page; „WikiController" has a function to display the different pages of the educating section Encyclopedia; „IdentificationController" includes methods for code analyzing and detects poorly parts of the analyzed code; „RefactoringController" contains methods and logic for code refactoring. „TemplatesController" includes methods for input data processing and for the construction of various patterns. Block "Views" contains views for each of the controllers and a general view section that contains common pieces of code for the controller's views.

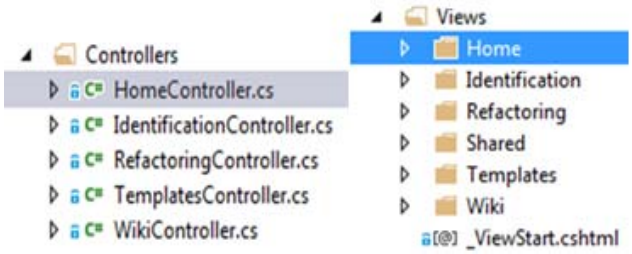

Fig.3 Controllers and Views

All views use Razor technology of Microsoft, which allows insertion of C# code in html pages. Upon receipt of a request for a page, the server compiles C # code and in response sends html content - result of the compilation. The main sections of the web system are presented in Fig.4.

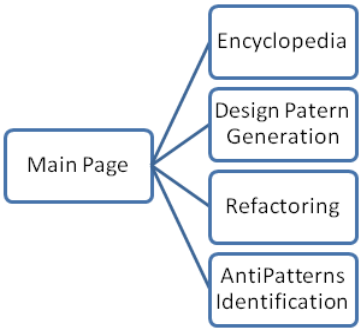

Fig. 4 Basic structural elements of the web system

- Main Page: it aims to present the different sections of the system with a short description and redirect the user to any of them.
- Encyclopedia: it aims to provide information on design patterns and anti-patterns. It consists of two parts: menu type accordion and informative part. The user can select from the menu a concrete DP or anti-pattern. When you choose a concrete pattern then the information about it is dis-played in the informative part. The section describes the problems that each design pattern solves, the advantages it provides and the situations in which it is used. For anti-patterns – their nature and options to be avoided are described. This section is realized as one page

with dynamic content that is changed through asynchronous AJAX requests to the server.

• Design Pattern Generation: this section offers functionality to generate sample implementations of the structure of the design patterns (Fig.5). The user chooses a type of pattern for example “Prototype”, inputs its parameters and click button "Generate". The generated code is displayed below the form.

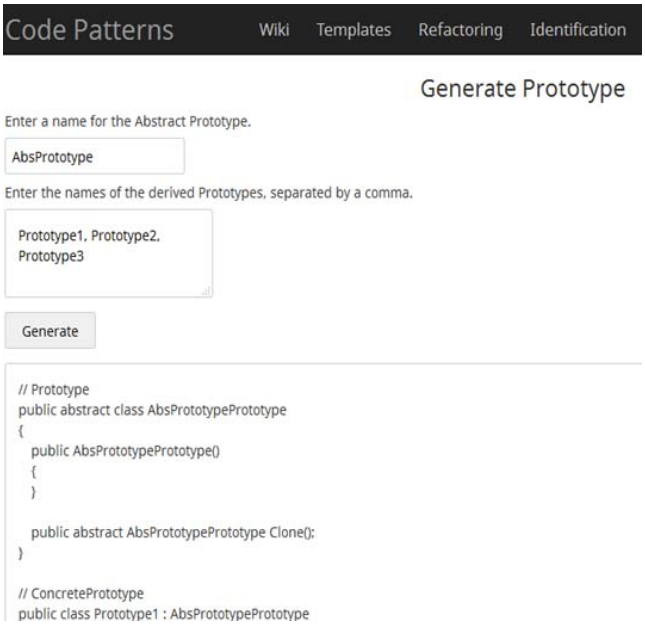

Fig.5 Prototype Design Pattern Generation

Refactoring: this section provides methods for automatic code refactoring. Each method performs the appropriate changes of the code and the modified code is returned as a result. In the left section of the refactoring window, the user puts the code, which must undergo refactoring. After entering the necessary parameters the user has to press button "Refactor". The refactoring code is displayed in the right pane (Fig.6).

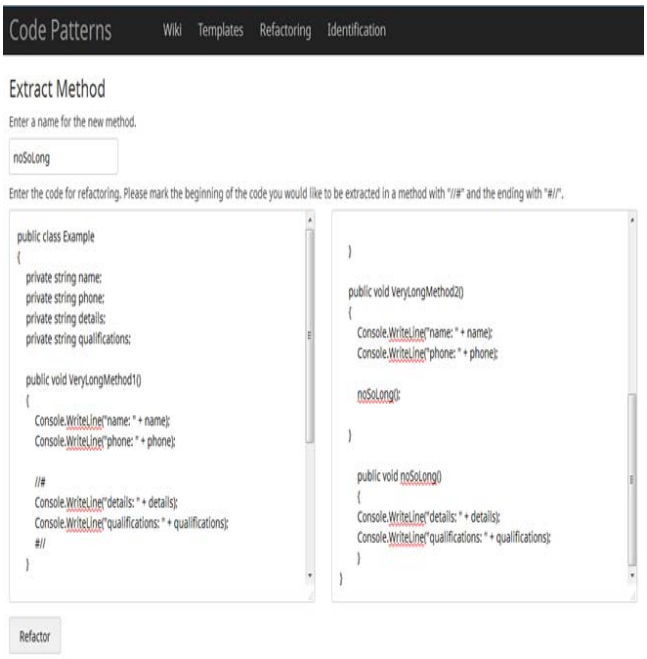

Fig.6 Code Refactoring

• Anti-pattern Identification: this section offers methods for code analysis with the goal to detect anti-patterns. The code is supplied as input to each method, which analyzes and paints the poorly constructed code sections. Then poorly constructed pieces of code must be rewritten to improve code readability and maintenance. Selecting a method (for example “Complicated If’s” – Fig.7) a page for entering the code for analysis is visualized. After entering the necessary input data the user must press the button "Identify". The program will process the code and will paint the problematic code parts in red (the result is shown in the right section): Design of libraries of components for re-use;

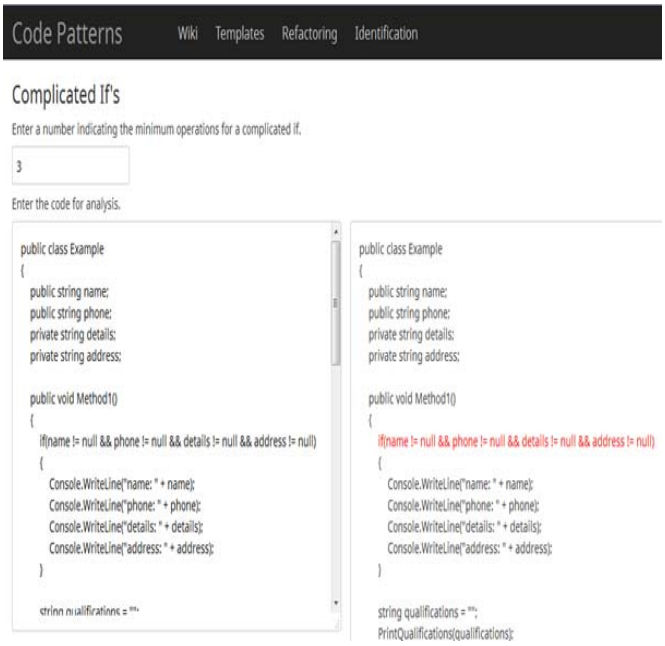

Fig.7 Anti-pattern Identification

IV. Conclusion and Future Progress

An approach that improves the software quality is proposed in the paper (Fig.1). “Refactoring” is the most important module of the approach. It is a general way for software evolution to a better version, i.e. general way to increase the software quality. Two specific contexts of refactoring are addressed by our approach: "refactoring, to remove bad code constructions" and "refactoring, to implement design patterns". The presence of Anti-Patterns and Patterns is recognized as one of the effective ways to measure the quality of modern software systems. In these contexts, the approach focuses on:

• Studying anti-patterns (code smells) to support their identification - module "Anti-pattern Identification".

• Studying patterns, to increase their effective use - module "Design pattern generation".

Actually, refactoring in the contexts addressed improves the quality of the software but more can be done in this direction. Software Refactoring includes many more contexts [5].

• Future work is needed to cover more refactoring contexts.

A Case tool (Fig.4÷Fig.7) is created that implements the approach proposed.

- Currently our DP detection strategy is not automated. Extensive research is necessary to develop techniques to automatically detect candidates of Design Patterns in the code.

We plan further:

- To add new patterns and anti-patterns in encyclopedic part.
- To add new methods for automatic refactoring and Anti-Pattern identification.
- To add support for various programming languages.

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Teaching Methodology for Digital Pulse Width Modulation and Phase Angle Control

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Abstract – **A teaching methodology for digital generation of Pulse Width Modulated signals and phase angle control is proposed in this article. Several different schematics and methods for Pulse Width Modulation and phase angle control are proposed. A sequence of tasks is developed for step-by-step education. The examined logical diagrams are implemented on FPGA device and are tested with USB oscilloscope. The advantages and the limitations of the different schematics are discussed. The use of Pulse Width Modulation and phase angle control for power control as well as for voltage regulation is demonstrated.**

Keywords – **PWM, Phase Angle Control, Pulse Width Modulation, FPGA, Teaching Methodology**

I. Introduction

Digitally generated Pulse Width Modulation (PWM) and phase angle control signals are widely used today. As the PWM and the phase angle control are one of the most common regulation techniques they are frequently used in the microprocessor systems. This requires the students to be familiar with the advantages and the limitations of the different methods for generation of such signals digitally. The proposed schematics are similar to the capture-compare modules of the microcontrollers. Some alternative methods for PWM and phase angle control are proposed also.

The following tasks are developed in order to learn the basic principles:

– A circuit for PWM generation using two parallel loadable counters is built and examined. The dependence of the output signal frequency and pulse width from the values loaded into the two counters is examined. The pulse width step is examined depending on the counters resolution and the loaded values.

– Alternative circuit for PWM generation using one binary counter and digital comparator is built and examined. The pulse width step is examined. The advantages and the limitations of the circuit are discussed.

– A circuit for phase angle control using one parallel loadable counter is built and examined. The relation between the frequency of the internal clock signal and the frequency of the external Zero Crossing signal is discussed. The effect of the frequency relation on the phase angle control step is discussed. The advantages and the limitations of the circuit are discussed.

– Alternative circuit for phase angle control with binary counter and digital comparator is built and examined. The advantages and the limitations of the circuit are discussed.

In all tasks 4 bit counters are used in order to be more simple to examine. In the real applications 8 or 16 bit circuits are used, and the proposed diagrams are scaled directly.

Examples of the usage of PWM for power and voltage regulation is given. A Light Emitting Diode (LED) is connected directly to the PWM output and the dependence of the brightness from the pulse width is examined. A test setup is made where the PWM digital signal is integrated and used for analog voltage generation. This demonstrates the possibility to generate analog voltage without dedicated digital-to-analog converter (DAC) using PWM and one digital output.

II. Structure of the Test Setup

The structural diagram of the test setup is shown on Fig. 1:

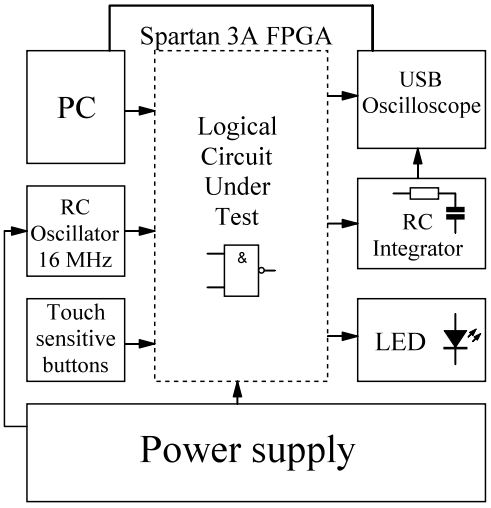

Fig. 1. Structural diagram of the test setup

A development board with Spartan 3A FPGA chip by Xilinx is used for the laboratory trainings. The board contains a power supply, 4 touch sensitive buttons with controller, USB interface for programming from PC, 16 MHz RC oscillator and 5 LED. The developed circuits are implemented into an FPGA chip. The circuits are tested using clock signals from the on-board RC oscillator followed by appropriate frequency dividers and the capacitive touch-sensitive buttons. The output signals are measured with USB oscilloscope that is also connected to the PC and are watched on the LEDs.

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III. DIGITAL PULSE WIDTH MODULATION

The first logical diagram proposed for digital PWM is shown on Fig. 2:

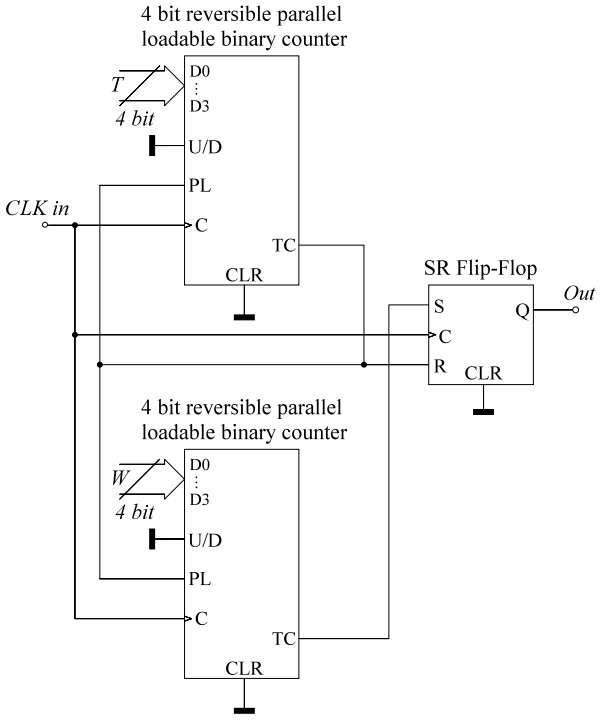

Fig. 2. Digital PWM logical diagram - first version

The circuit consists of two reversible parallel loadable binary counters permanently configured for counting down and an SR-type flip-flop. The circuit receives external clock signal and forms an output square wave signal with variable pulse width from 0 to 100% [1]. The value T loaded into the upper counter is determining the frequency of the output signal. The lower counter is loaded with the value W which is inversely proportional to the pulse width. The two counters are receiving a common clock signal. When the upper counter reaches zero its TC output goes high and resets the SR flip-flop. It also loads the counter with the value T again. The same signal loads the lower counter with the value W. The two counters start counting down from T to zero and from W to zero. When the lower counter reaches zero its TC output goes high and sets the SR flip-flop. The cycle repeats when the upper counter reaches zero and resets the flip-flop. The frequency of the output signal is given by Eq. 1:

$$F_{out} = \frac{F_{in}}{T} \tag{1}$$

Where T is the decimal value of the binary number loaded into the upper counter.

The duty cycle is given in percent by Eq.2:

$$D = \frac{T - W}{T}.100 \tag{2}$$

Where:

D is the duty cycle in percent

T is the decimal value of the binary number loaded into the upper counter

W is the decimal value of the binary number loaded into the lower counter

The timing diagrams of the circuit are represented on Fig. 3:

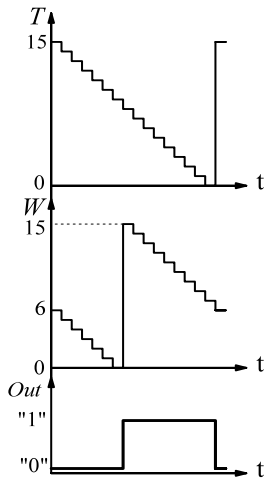

Fig. 3. Digital PWM timing diagrams - first version

The first subplot represents the state of the upper counter. The second subplot represents the state of the lower counter while on the third subplot the state of the flip-flop is represented. In the particular example the upper counter is loaded with T = 15 and the lower counter is loaded with W = 6 resulting in 60% duty cycle.

The circuit is implemented on the FPGA and two auxiliary binary counters are connected with two touch sensitive buttons for clock signal. Their outputs are connected to the parallel load inputs T and W. The values of the two counters are varied and the output signal is observed with the USB oscilloscope. The frequency, period and duty cycle are measured with the oscilloscope and compared to the ones from the equations. The PWM signal is applied to one of the LEDs. The brightness of the LED depending on the duty cycle is observed. The results are discussed.

The second logical diagram for PWM is represented on Fig. 4:

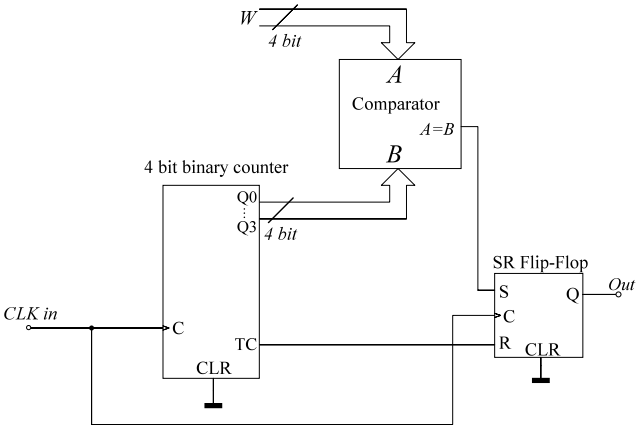

Fig. 4. Digital PWM logical diagram - second version

The diagram contains one binary counter, digital comparator and SR-type flip-flop. The counter is counting up continuously and every time it reaches its maximum value 2^n and overflows the TC output goes high and resets

the SR flip-flop. When the state of the counter equalizes with the value *W* the digital comparator outputs logical one and sets the SR flip-flop [2]. The duty cycle of the output pulses is inversely proportional to the value *W*. The frequency of the output signal depends on the counter resolution and the input clock frequency and is given by Eq. 3:

$$F_{out} = \frac{F_{in}}{2^n} \tag{3}$$

Where *n* is the counter resolution.
The duty cycle of the output pulses is given by Eq. 4:

$$D = \frac{2^n - W}{2^n} \tag{4}$$

Where:

D is the output duty cycle

n is the counter resolution

W is the decimal value of the binary number controlling the duty cycle.

The timing diagrams of the circuit are represented on Fig. 5:

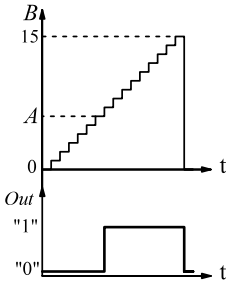

Fig. 5. Digital PWM timing diagrams - second version

The first subplot is showing the state of the counter applied to the *B* input of the comparator. The value *W* applied to the *A* input is marked with a dotted line. On the second subplot the output signal of the flip-flop is shown.

The circuit is implemented onto the FPGA. Clock signal is applied to the *CLK in* from the *16 MHz* on board oscillator after a proper frequency division. One of the touch sensitive buttons is connected to the clock input of auxiliary binary counter which forms the number *W* for the duty cycle control. The circuit is examined with the USB oscilloscope. The frequency and the duty cycle are measured with the oscilloscope for different values of *W* and the results are compared to the equations and are discussed.

IV. Digital Phase Angle Control

The first logical diagram proposed for digital phase angle control is represented on Fig. 6. It includes parallel loadable reversible counter configured permanently in down direction, and an SR-type flip-flop. A zero cross signal *ZC* is used for synchronization with the AC voltage. The counter receives internal clock signal *CLK in* and counts down until it reaches zero. Then the TC output goes high and sets the SR flip-flop. When the *ZC* input receives a pulse the flip-flop is cleared and the counter is loaded with the value *A* and continues to count down until it reaches zero again. This way a triggering pulse is generated *A* number of periods of the *CLK in* signal after the zero crossing. The angle of triggering is proportional of the *A* number [3]. Due to the fact that the parallel load operation of the counter is synchronous *ZC* pulse is required to be with length at least one period of the *CLK in* signal. A pulse stretching circuit with one SR flip-flop is added [4]. The SR flip-flop is cleared immediately with the *ZC* signal and the level to its inverted output drives high the PL input of the counter. As soon as the first rising edge of the *CLK in* is received the counter is loaded with the *A* value and the flip-flop is set to one and its inverted output goes low.

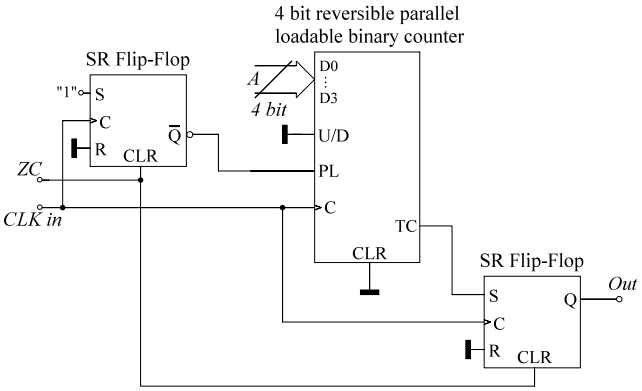

Fig. 6. Digital phase angle control logical diagram - first version

The angle of the triggering pulse is given by Eq. 5:

$$\alpha = \frac{180.A.T_{CLKin}}{T_{ZC}} \tag{5}$$

Where:

α is the angle of the triggering pulse in degrees

A is the decimal value of the binary number loaded into the counter

T_{CLKin} is the period of the *CLK in* signal

T_{ZC} is the period of the *ZC* signal

In the ideal case the frequency of the *CLK in* signal should be slightly less than *ZC* frequency multiplied by 2^n where n is the resolution of the counter. The counter should do less than one full cycle for one period of the *ZC* signal. If it makes more than one cycle the range of phase angle regulation will be limited.

The timing diagrams of the phase angle control circuit are shown on Fig. 7:

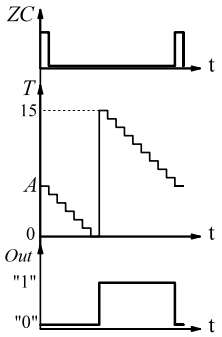

Fig. 7. Digital phase angle control timing diagrams - first version

The *ZC* signal is plotted on the first subplot. On the second subplot the counter state is represented and on the third subplot the output signal is shown.

The circuit is implemented on the FPGA and is tested. One touch button is connected as a clock signal to an

auxiliary binary counter which output is connected to the *A* input of the circuit. By the button the number *A* is varied. The *ZC* signal is formed from the on board RC oscillator by special dividing and forming circuit. The phase angle control circuit is tested with the USB oscilloscope. The phase angle of the triggering pulse is measured for the different values of *A*. The *CLK in* frequency is varied and the phase angle range is tested again. The pulse stretching circuit is bypassed and the circuit is tested again. The results are discussed.

The second circuit for digital phase angle control is represented on Fig. 8:

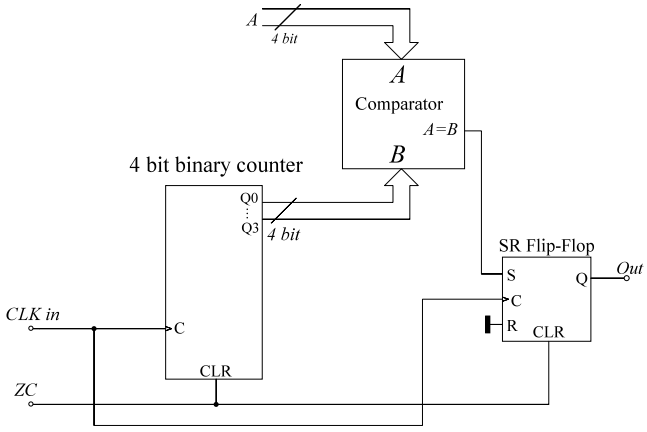

Fig. 8. Digital phase angle control logical diagram - second version

The circuit contains a binary counter, a digital comparator and an SR flip-flop. When the *ZC* pulse is applied the counter and the flip-flop are cleared asynchronously. Due to that the circuit does not require pulse stretching of the *ZC* signal in order to operate correctly. After the *ZC* pulse the counter starts to count up. At some point its output state equalizes with the number *A* and the digital comparator drives high the S input of the flip-flop. The flip flop is loaded with "1" and remains in this state until the next *ZC* pulse when the cycle repeats [5]. Basically the circuit operation and the equations for the phase angle of the triggering pulse are identical to these for the first version. The requirements for the frequency of the *CLK in* are the same.

The timing diagrams of the circuit are represented on Fig. 9:

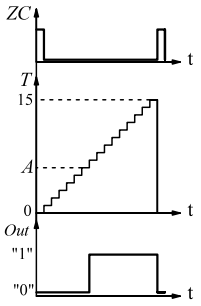

Fig. 9. Digital phase angle control timing diagrams - second version

The first subplot shows the *ZC* pulses. The counter state is plotted onto the second subplot and the output triggering pulse is represented on the third subplot.

The circuit is implemented in the FPGA and is tested with the USB oscilloscope the same way as the first version. The advantages and the limitations of the circuit are discussed.

V. Conclusion

The developed logical diagrams for digital PWM and phase angle control are simple and easy to understand. They are showing the principle of operation of the capture-compare modules of the microcontrollers at hardware level and are suitable for the teaching course of the digital electronics. Different versions of the schematics are developed showing different possible methods to achieve one task each with different limitations and advantages. In the process of circuit implementation some additional logical circuits are needed for example a frequency divider chain or pulse-forming circuit. These circuits are designed as a library modules and are used directly in the laboratory trainings helping the students to focus on the circuit being studied and doing the tasks faster.

All developed logical circuits are the digital analog of the standard analog circuits for PWM and phase angle control. This makes them easier to understand based on the already known analog methods.

The use of 4-bit circuits makes the testing of the circuits more simple. Also the discrete 16-step regulation of the duty cycle and the phase angle is good demonstration of the significance of the circuits resolution for the precision control.

In the circuits for phase angle control the range of the digital code *A* in which the phase angle of the triggering pulse is varied from 0 to 180 degrees depends on the mains frequency. As the mains frequency becomes higher there is more unused code range above 180 degrees. This problem can be avoided if a digital Phase Locked Loop is used for the generation of *CLK in* signal from the *ZC* signal [6]. This is obviously going to increase the complexity of the circuit significantly. If the code-to-phase angle ratio is not critical and the circuit is used only at one mains frequency such complexity is not needed.

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Development of series resonant converter models with output transformer

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Abstract – **The main advantages of the resonant converters are the high efficiencies, low losses and minimal stress over the power semiconductors achievable with the soft-switching capabilities. This improvement over the standard half- and full-bridge converters comes with added complexity but nevertheless offers several performance benefits. The aim of this paper is to presents methodic for the design and verification of the series isolated resonant DC-DC converters.**

Keywords – **Power Electronics, DC-DC converters, Resonant Converters, Modeling**

I. INTRODUCTION

The paper presents investigation of the approach for modeling series resonant converters with output transformers. Essentially model of series resonant inverter is proposed with output current ratio changing via a current transformer and then an output rectifier is connected to the secondary winding, effectively transforming the inverter to a DC-DC voltage converter. The purpose of the model is to take in account the influence of the transformer parameters (primary and secondary inductance, coupling factor and resistive parameters) on the resonant converters. From the literature [1, 2, 9] is known that they affect the operating regime by influencing on the resonant frequency and thus changing the overall operating regime of the converter.

II. THEORY OF OPERATION

The examined circuit of the series resonant inverters is shown on figure 1. It consists of the resonant inductor and capacitor (L_r, C_r) and resistance R connected in series. They form the resonant tank circuit [3 - 7] through which flows the common load current i_L.

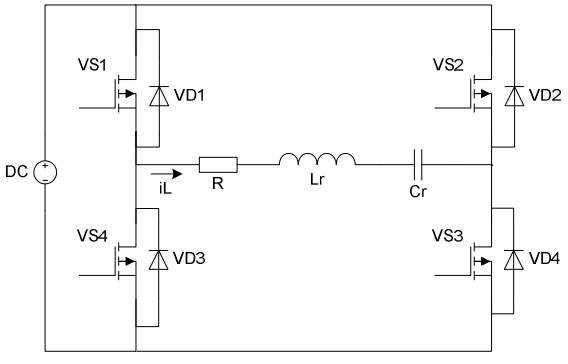

Fig. 1. Series resonant inverter without transformer

The balance of the voltage yields that the sum of all momentary voltages equals the supply voltage $u_L + u_C + u_R = U_d$. If there is a need to lower or rise the current flowing through the load a transformer in series with the resonant elements can be used. It provides not only the necessary current stepping but allows operation in excessive load (like short-circuit), due to the finite value of the primary winding's resistance R_p. Also it provides a galvanic insulation, which is an advantage in some applications.

A. Series resonant inverter with transformer

The circuit of such a device is given on fig. 2. As it can be observed the load is connected on the secondary winding and the current is transferred with a ratio $K_I = w_1/w_2$ which is also equal to $K_I = L_p^2/L_s^2$ according to the electromagnetic laws of Faraday. These values can be found experimentally using various methods [4, 5, 8, 10].

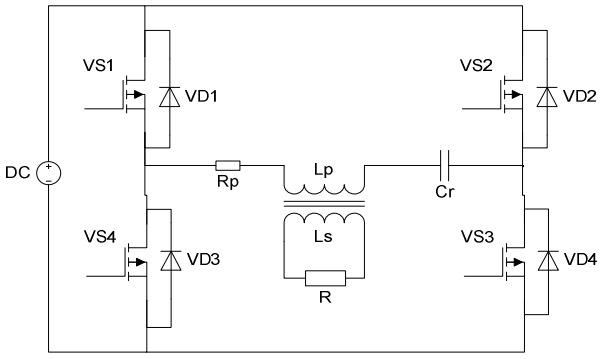

Fig. 2. Series resonant inverter with transformer

However the primary inductance affects the resonant frequency of the converter, because it sums with the series resonant inductance L_r (not shown on the figure) in the differential equation:

$$(L_p + L_r)\frac{di_p}{dt} - M\frac{di_s}{dt} + u_{Cr} + R_p \cdot i_p = U_d \qquad (1)$$

Note that the equation takes into account the effect of the secondary winding circuit through the mutual inductance M and the secondary current i_s. Depending on the load, the effect of the primary inductance is variable; that is the value changes with the load current, thus changing the resonant frequency and the quality factor which all of them

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affect the performance and the operating regime of the converter.

B. Series resonant DC-DC converter with transformer

If a rectifier is added in series of the secondary, the series resonant inverter becomes a DC-DC converter, with an output voltage depending on the turn ratio of the transformer. The schematic is given on figure 3. Another thing to point out for this circuit is that the output capacitor voltage U_o acts as anti-parallel voltage source on the primary circuit.

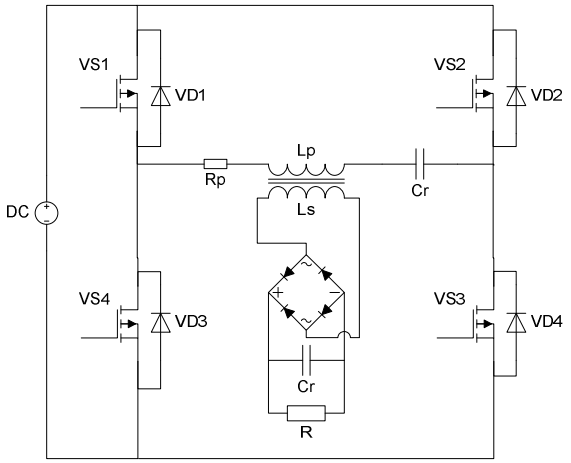

Fig. 3. Series resonant DC-DC converter with output transformer and rectifier

For the modeling purposes is used the output standard full-wave diode bridge rectifier, which is simpler to model than the full wave dual-phase secondary winding diode rectifier.

III. MODELING

The aim of the modeling is to create a description of the circuit, taking into account the effects produced by the transformer and it's coupling parameters. These effects will be used to analyze the operating regime and the conclusions will be used to optimize the control circuit and algorithm. These models can be successfully applied in prototyping test benches. The chosen modeling approach is via mathematical models with system of ordinary differential equations, which are evaluated in computational software.

A. Series resonant inverter with transformer

The differential equation system describing the circuit operation of the series resonant inverter with output transformer is the following:

$$\begin{cases} (L_p + L_r)\dfrac{di_p}{dt} - M\dfrac{di_s}{dt} = U_d - u_{Cr} - R\cdot i_p \\ M\dfrac{di_p}{dt} - L_s\dfrac{di_s}{dt} = R\cdot i_s \\ C_r\dfrac{du_{Cr}}{dt} = i_p \end{cases} \quad (2)$$

Due to the fact that there are three reactive elements the number of the equations is three although there is a mutual inductance between L_p and L_s. The mutual impedance R_m is neglected in this model.

B. Series resonant DC-DC converter

Same rules apply when we create the model of the resonant converter with rectifier – however an extra output filter capacitor equation is added; and the secondary current charges this capacitor always with positive current (due to the rectifier).

$$\begin{cases} (L_p + L_r)\dfrac{di_p}{dt} - M\dfrac{di_s}{dt} = U_d - u_{Cr} - R\cdot i_p \\ M\dfrac{di_p}{dt} - L_s\dfrac{di_s}{dt} = R\cdot i_s - sign(i_s)\cdot u_{Co} \\ C_r\dfrac{du_{Cr}}{dt} = i_p \\ C_o\dfrac{du_{Co}}{dt} = |i_s| - \dfrac{u_{Co}}{R} \end{cases} \quad (3)$$

The changes of signs in the equations are affected by the operational principle because when the circuit is operating the inverted current is changing the direction in the output diagonal of the bridge, where the load circuit is connected. The method of the momentary values states that the state variables must be connected together at the moments of commutation of the semiconductor power switching elements. This designates that the calculated values of the state variables produced in the end of the half period from the circuit operation are involved as the initial conditions for the next half period. In order to do a generalized description of the workings of the circuit in the individual half periods a switching function is used, which serves as a commutator of the power supply to the resonant tank circuit.

IV. RESULTS

The investigated mathematical models with a system of ordinary differential equations are (2) and (3). The evaluation is done by using MATLAB® scripts. This allows more flexible setting of the parameters and also the source can be ported and compiled very easy to embedded systems for further evaluation. The schematic elements for the resonant inverter with transformer are with the following parameters: input voltage U_d = 300 V, output voltage U_{out} = 48V, output power P_{out} = 1 kW, switching frequency f_{sw} = 100 kHz, resonant inductor value L_r = 170 µH and resonant capacitor value C_r = 11.3 nF. A transformer is designed so that the primary inductance doesn't affect the operating regime of the inverter. This is achieved by selecting the primary inductance to be at least 10 times greater than the resonant inductor. For a transformer turns ratio K_{Tp} of 8.62 this yields a primary inductance L_p = 1.7 mH and secondary inductance L_s = 22.73 µH. The load resistance for a 1 kW inverter is R = 1.63 Ω. The modeling method used for the evaluation is finding a solution of system of ODEs using Adams method.

If we compute a numerical solution to this system we will obtain the following waveforms:

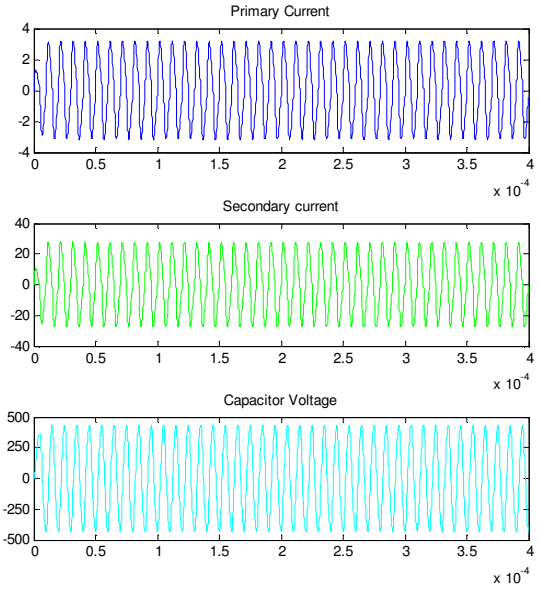

Fig. 4. Produced waveforms of the resonant inverter with transformer

The obtained RMS values of the primary and secondary currents are $I_{p(RMS)}$ = 2.23 A and $I_{s(RMS)}$ = 19,8 A respectively. As it can be observed this yields an output power of 1 killowatt. The resonant capacitor voltage amplitude is around $C_{r(max)}$ = 460 V, which is 50% more than the supply voltage value. The circuit has a very fast settling time, because the load resistance is low and the transformer parameters do not affect the resonant tank network, due to their selection to be a magnitude higher than the elements in the resonant network.

For the evaluation of the model of resonant DC/DC converter with transformer the desired parameters are: input voltage U_d = 110 V, switching frequency f_{sw} = 100 kHz, output power P_{out} = 400W and output voltage U_o = 24 V. The calculated resonant tank elements are: resonant inductor value L_r = 32.4 µH and a resonant capacitor value C_r = 39 nF. The output of the rectifier is connected with output filter capacitor C_o = 10 µF and load resistance R = 2,4 Ω. The transformer is designed so that the turns ratio coefficient is K_{Tp} = 4.79. This yields for a primary inductance L_p = 1.82 mH and secondary inductance L_s = 380 µH.

If we compute a numerical solution to this system we will obtain the waveforms shown on figure 5. It can be observed the primary current with a RMS value of $I_{p(RMS)}$ = 3.93 A and secondary winding current with a RMS value of $I_{s(RMS)}$ = 17,8 A. The voltage across the resonant capacitor is around $C_{r(max)}$ = 360 V, which is a bit higher for this type of applications. The average value of the output voltage in steady-state operation U_o = 24,08 V. The circuit possesses fast transient response and settling time into steady state regime, especially for the resonant tank network and transformer (it settles in just five switching cycles). Also the maximum overshoot at turn-on is no more than 5%, which is good for the operation and selection of the semiconductor devices – they don't need to be oversized by their maximum voltages and currents. The settling of the output voltage is determined only by the output filter capacitor value.

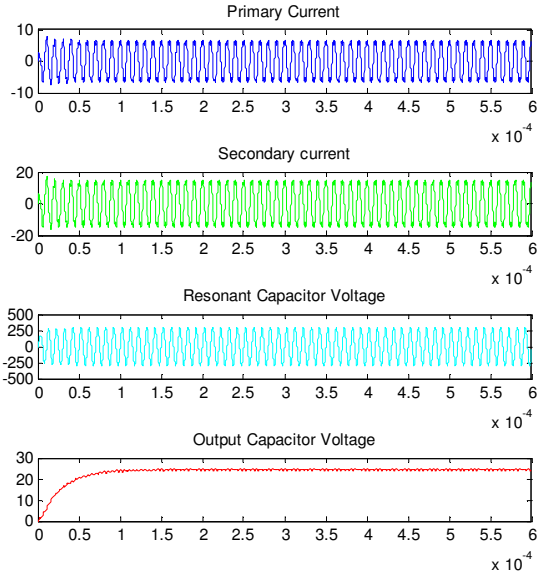

Fig. 5. Produced waveforms of the resonant converter with transformer

The proposed models can be used successfully for verification of design parameters calculations and evaluation in system-level designs, where applicable. If a regulator and/or controller is added the scope of applications can be expanded for power supplies of different loads.

CONCLUSIONS

A review of the most common types of series resonant inverters and converters with their advantages and disadvantages has been made. The paper proposes mathematical models of series resonant converters with transformers. An evaluation of the models is conducted and a brief review of the results is made.

ACKNOWLEDGMENT

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Practical Model for Management, Monitoring and Research of Passive Optical Network

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Abstract – **Passive optical networks are widely used in modern communication networks for broadband access. A major problem in terms of development and operation of these networks is to provide opportunities for management, monitoring and research. The main objective of this work is to implement a practical model of a passive optical network for the delivery of interactive services to perform three main tasks: to allow convenient and easy training of staff; to permit a wide variety of practical research (traffic processing, introducing of new services and optical service modules, etc.); to be a platform for conducting general research in the field of passive optical networks.**

Keywords – **passive optical network, optical power, eye diagram, power budget, wavelength multiplexing**

I. Introduction

Modern passive optical networks are widely used in networking for the delivery of broadband services. They introduce maintenance cost reduction and high data rates.

The typical access architecture uses an optical platform, traditionally located in the Central Office (CO), known as an Optical Line Terminal (OLT) to transmit traffic to large number of residential drop points [1]. Passive optical devices called splitters/combiners are located at fiber distribution hubs situated between the OLTs and subscribers' Optical Network Terminals (ONTs). The passive optical splitters/combiners divide a single downstream transmission into multiple fiber drop streams as well as collect upstream traffic from multiple ONTs on to a common stream transmitted back to the CO.

As fiber gradually penetrates deeper into the access edge, the OLT is slowly shifting out of the CO [1]. The reason for this trend is to better extend network reach to more ONTs, and therefore to more subscribers and subsequently attain higher penetration densities. Higher bandwidths permit the sale of new services including IPTV, video on demand, security surveillance, VoIP, internet, on-line storage and gaming [2,3]. Cost-effective passive optical networks (PONs) utilize passive optical splitters/combiners at this point to distribute the cost of one OLT port and the associated laser transceiver across many drop points. The goal is to provide ever more subscribers with service while containing the cost to reach each additional customer. In such cases, the optical network termination effectively moves all the way to the enterprise office building or customer premises. [1]

The practical concept of PON model is designed to improve the training opportunities for students, trainees and staff, moreover to create a low-cost multi-functional platform for a wide variety of scientific research in the field of passive optical networks and broadband service delivery.

II. Design of Simulation Model of Passive Optical Network

For modeling the concept of the practical model of a PON network is developed a simulation model with OptiSystem design suite, as shown in Fig. 1.

The simulation model consists of three spectral multiplexed channels: two downstream (DS) channels (one for transmission of broadcast services such as TV content and one for IP data download services) and one upstream (US) channel (for IP data uploading services). The two DS channels are at 1550 nm and 1310 nm wavelengths, and the US channel is at 1490 nm. The wavelengths are multiplexed through the power combiner with 0,8 dB loss and demultiplexed through the power splitter with 0,6 dB loss. Optical connectors with internal losses of 0,5 dB are introduced to model the attenuation and the connections.

Various types of visualizers are used to visualize the parameters and characteristics of the input / output optical signals: optical spectrum analyzers, optical time domain visualizers, optical power meters and BER analyzers.

Using this simulation model of the PON concept, its behavior is studied under the following conditions: inserted input power 0 dBm for DS and US channels; NRZ optical modulation type; different optical link distances: from 6 m (as it is predicted for the implemented practical model) to 12 km (for small urban PON networks, for example, for cable television and internet delivery); SMF fiber with α = 0,3 dB/km. The results are summarized in Table 1.

This simulation model can be used, for example, to determine the Q-factor (OSNR respectively) when a required BER value is set (i.e. Q_{BER}), to investigate the BER characteristics of the determined network [5], to investigate the noise parameters of the network [6] or to determine the required OSNR at a given receiver sensitivity [4].

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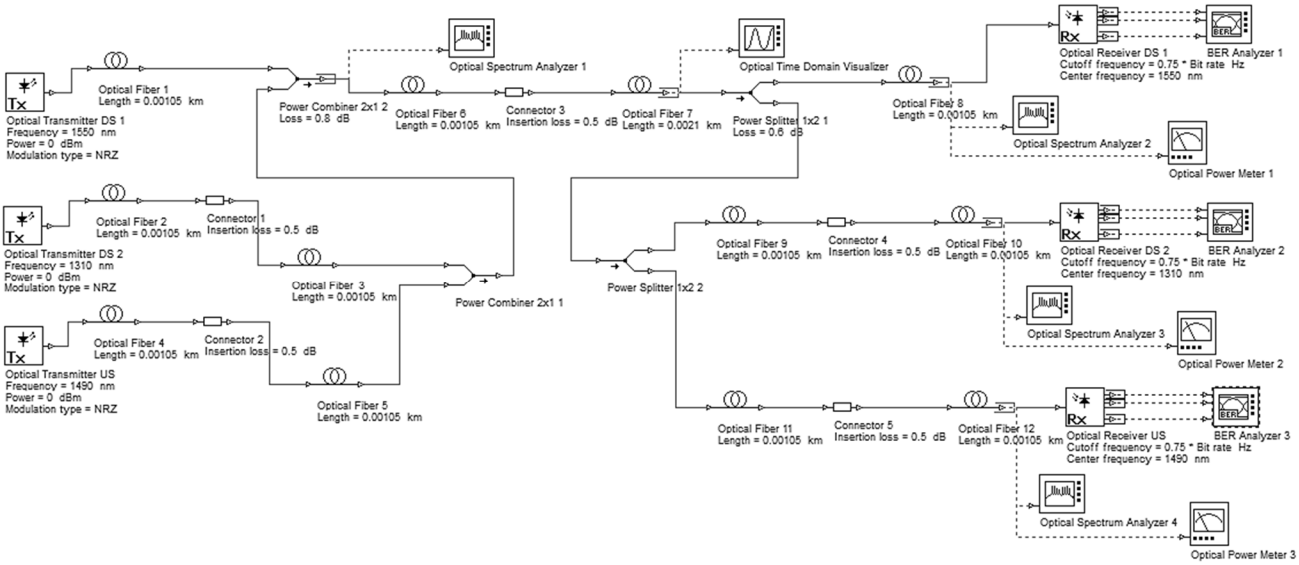


Fig. 1. Simulation model of the passive optical network concept

TABLE 1. PON MODEL SIMULATION STUDY RESULTS

Distance, km		0,006	0,1	1	2	4	6	8	10	12
BER	DS 1550 nm	-	-	-	-	-	$2{,}80.10^{-202}$	$4{,}54..10^{-150}$	$4{,}33.10^{-108}$	$8{,}41.10^{-86}$
	US 1490 nm	$6{,}59.10^{-31}$	$2{,}24.10^{-31}$	$1{,}55.10^{-27}$	$7{,}20.10^{-24}$	$3{,}98.10^{-20}$	$2{,}14.10^{-15}$	$1{,}02.10^{-11}$	$3{,}51.10^{-9}$	$8{,}26.10^{-8}$
	DS 1310 nm	$1{,}13.10^{-31}$	$2{,}45.10^{-31}$	$1{,}15.10^{-28}$	$3{,}95.10^{-24}$	$1{,}08.10^{-19}$	$7{,}74.10^{-15}$	$5{,}20.10^{-12}$	$9{,}69.10^{-10}$	$6{,}56.10^{-8}$
Q	DS 1550 nm	52,14	56,94	53,88	45,32	38,52	30,32	26,24	22,05	19,6
	US 1490 nm	11,5	11,59	10,81	10,01	9,11	7,85	6,7	5,79	5,23
	DS 1310 nm	11,65	11,58	11,05	10,06	9,01	7,68	6,8	6,002	5,22
P_{RX}, dBm	DS 1550 nm	-7,78	-7,81	-8,051	-8,378	-8,978	-9,579	-10,179	-10,778	-11,378
	US 1490 nm	-11,291	-11,319	-11,561	-11,888	-12,489	-13,089	-13,688	-14,288	-14,88
	DS 1310 nm	-11,291	-11,319	-11,561	-11,888	-12,489	-13,089	-13,688	-14,288	-14,88

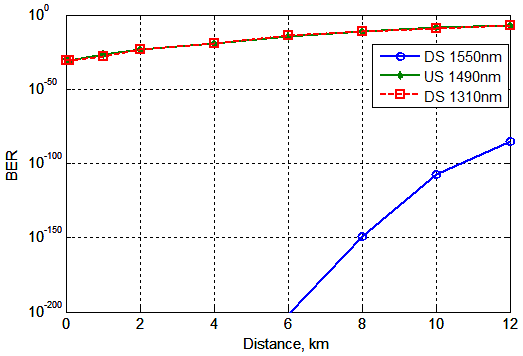


Fig. 2. BER in function of the distance of the simulated PON

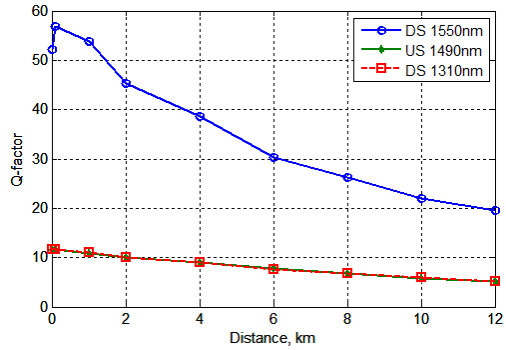


Fig. 3. Q-factor in function of the distance of the simulated PON

On Fig. 2 is shown the resulting graphical dependence of the BER in function of the physical length of the optical line, and on Fig. 3 – the Q-factor of the optical line in function of its physical length.

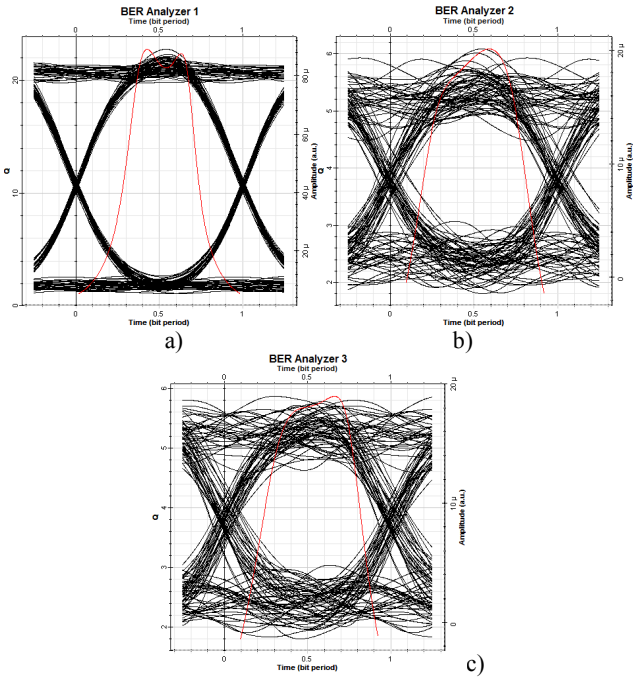
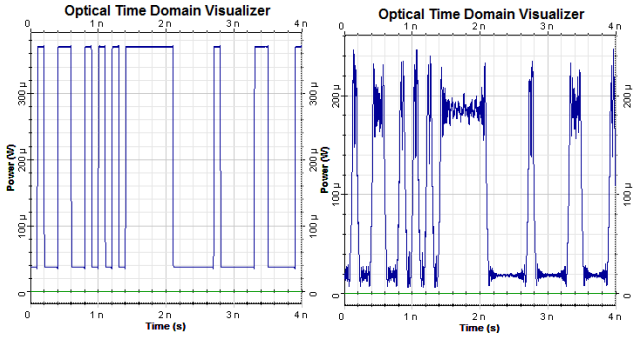


Fig. 4. Eye-diagram and Q-factor at a 10 km distance of simulated PON: a) DS 1550 nm, b) DS 1310 nm and c) US 1490 nm

From the presented table and the graphical dependencies, it is determined that the maximum possible distance where the BER will be better than 1.10^{-9} is 10 km. For this worst-case scenario on Fig. 4 are shown eye-diagrams and Q-factor of the network. It is evident that the worst parameters characterize the upstream channel at a wavelength of 1490 nm (BER = $3{,}51.10^{-9}$).



a) b)

Fig. 5. Optical time domain diagram of the simulated PON: a) for 6 m distance (ideal case), b) for 10 km distance (worst case)

Fig. 5 depicts the optical time domain diagram of the optical wavelength multiplexed signal in the case provided for the practical model (i.e. 6 m distance) and in the worst case (i.e. 10 km distance).

III. Implementation of the Practical Model for Management, Monitoring and Research of Passive Optical Network

After the modeling of PON network, the practical implementation of the proposed model will be considered here. The practical concept of the developed model is shown on the block diagram in Fig. 7.

The model consists of the following modules and elements:

- Galvanic isolator GIP (pos. 1 and 9);
- Optical transmitter module KTS OT-1 at 1550 nm (pos. 8) [7];
- Optical receiver module KTS MOR-01-ALC at 1550 nm (pos. 2) [7];
- Power supply modules KTS DCP 612 (pos. 5, 12 and 13) [7];
- Remote power supply module KTS ACTR 150 230V/48V AC (pos. 15) and safety fuse (pos. 16) [7];
- Switches NMGS4P1F-IS (pos. 3 and 10) with SFP modules (Tx 1310 nm / Rx 1490 nm and Tx 1490 nm / Rx 1310 nm) (pos. 4 and 11);
- CWDM filter (pos. 6);
- Optical splitter (pos. 7);
- Power monitoring system VC IPM-4 (pos. 14).

The selected max. distance of the optical link is 6 m due to the following practical considerations: the model should be small enough for ease of use and the length of the used SC/APC fiber optic patch cables is typically about 1 m.
The developed power monitoring system VC IPM-4 allows remote IP monitoring and control of supply voltage.

The overall look of the implemented model is shown on Fig. 6.

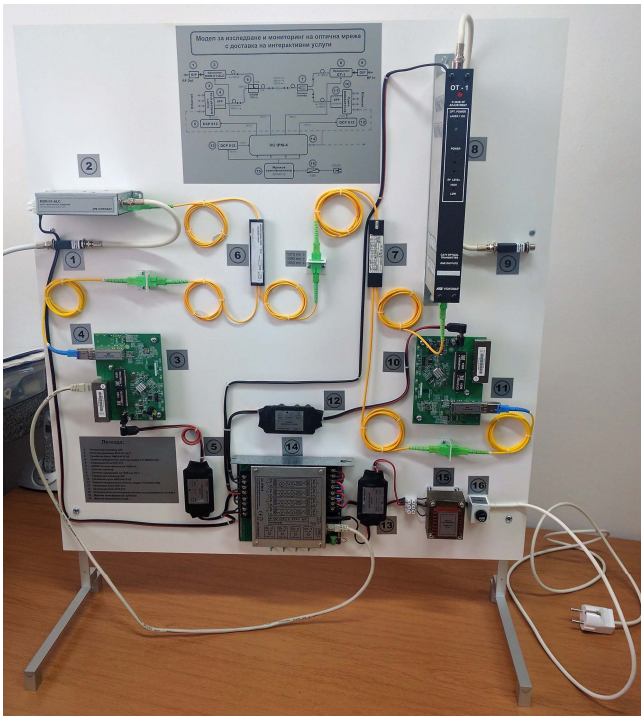


Fig. 6. Overall view of the implemented practical model for management, monitoring and research of passive optical network

The approbation of the model is realized by measuring the optical signal at the designated control points in both directions (upstream and downstream). The results are shown in Table 2. The values in Table 2 may be used for displaying a graph of the energy budget of the passive optical network in both directions – Fig. 8. The drops in the energy budget of the optical line are due to the damping in the optical SC/APC adapters, optical splitter (pos. 7) and CWDM filter (pos. 6).

Table 2. Measured optical signal power in designated control points

Control Point №	Wavelength, nm	Optical Power, dBm
CP 1 (OT) DS	1550	3,5 ±0,5
CP 2.1 DS	1550	0,15
	1310	–8.41
CP 2.2 US	1490	–8.25
CP 3.1 DS	1310	–5.44
CP 3.2 US	1490	–10.11
CP 4.1 (Switch 1) DS	1310	–4.44
CP 4.1 (Switch 1) US	1490	–10.89
CP 5 (OR) DS Sensitivity: -7dBm	1550	–1.03
CP 6.1 DS	1310	–9.61
CP 6.2 US	1490	–6.25
CP 7.1 (Switch 2) DS	1310	–10.27
CP 7.2 (Switch 2) US	1490	–5.7

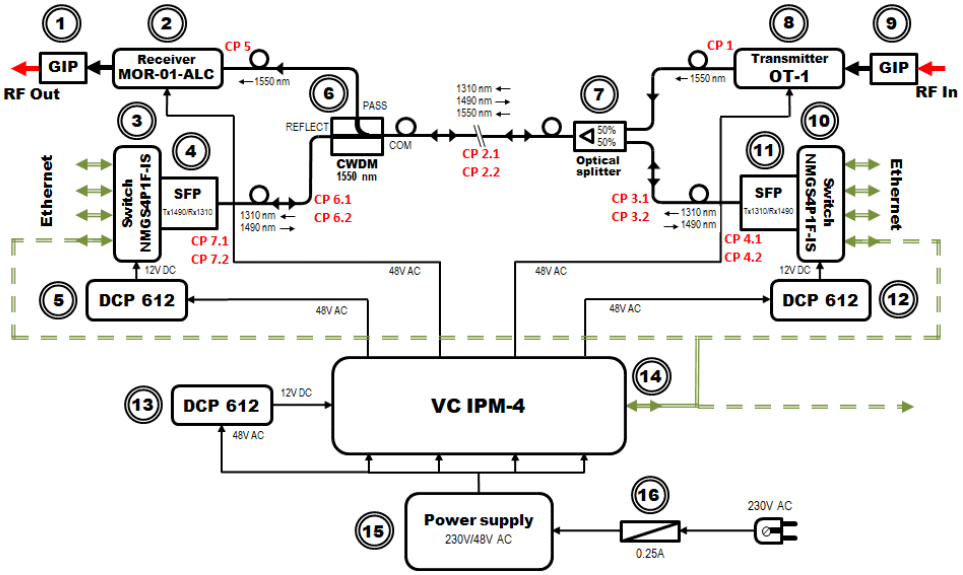


Fig. 7. Block diagram of model for management, monitoring and research of passive optical network (conception)

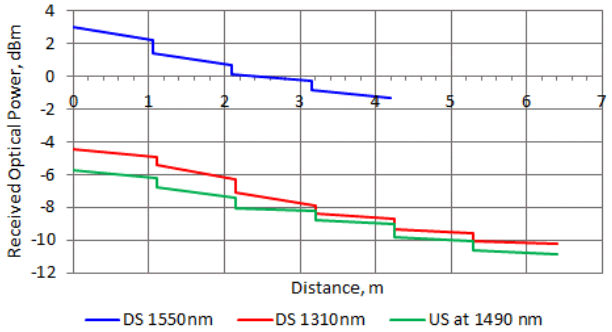


Fig. 8. Optical power budget of the implemented passive optical network model

By comparing the simulation results in Table 1 with the experimental optical power measurements in Table 2 is evident that there is a good correlation between the results. Investigation of various scenarios associated with varying optical power levels may be performed by using optical attenuators and optical fibers of different length coupled at the control points (CPs) to the available optical connectors.

IV. Conclusion

In this paper is simulated, developed and researched practical model of PON network for urban conditions for delivery of wide range of services like TV, VoD, Internet, telephony (VoIP), etc. The model offers flexible options for training of students, trainees and staff, as well as low-cost multi-functional platform for a wide variety of scientific research in the field of passive optical networks and broadband service delivery.

The developed practical model of PON has many advantages such as small size, low cost, wide range of options, flexible and modular structure and could be incorporated into a large-scaled network. The disadvantages are the fixed wavelengths used by the optical transmitter, optical receiver and SFP modules.

There is a wide variety of possibilities for conducting further scientific and practical research on the model: use of different types and lengths of optical fibers; optimization of equipment parameters; investigation of optical non-linear effects in optical transmission networks; emulating signals for different types of services and analyzing the traffic load; emulating a large number of subscribers, etc.

V. Acknowledgements

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Control Flow Aware Software-Implemented Fault Injection for Embedded CPUs

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Abstract – **Fault injection is a highly used technique to test fault-tolerant embedded systems. We present a new software-implemented fault injection process to deterministically inject control flow errors in embedded CPUs. The proposed process analyses the disassembly file of the program acting on the embedded CPUs to construct the correct control flow. Once known, this information is used to deterministically inject intra-block, inter-block and out-of-function errors. To conclude, we discuss how our process can aid in performing a vulnerability analysis for a target algorithm.**

Keywords – **Fault Injection, Soft Errors, Control Flow Aware, Fault Tolerance**

I. Introduction

Today embedded systems are susceptible to erroneous bit-flips caused by external factors, which range from high-energy neutrons to electromagnetic radiation [1-4]. The introduced bit-flips can affect the embedded system by corrupting memory or the software in execution, which in turn can lead to a system crash [5]. To protect (embedded) systems, several fault tolerance techniques have been proposed in literature [6-9]. Fault tolerance is a three step process:

- fault detection, indicating that somewhere in the system a fault occurred;
- fault isolation, pinpointing the exact location of the fault; and
- fault recovery, restoring the system from the fault.

To test and validate the implemented fault tolerance, faults or bit-flips need to occur in the system. Fault tolerance measures can be validated using fault injection tools, which allow testing fault detection, fault isolation and fault recovery strategies both together and separately. Over the years, many fault injection tools have been developed. Although each tool has its advantages, they all suffer from one or more disadvantages. For example, they either require expensive additional hardware or don't allow to inject faults deterministically.

In this paper, we propose a software-implemented fault injection process that allows to deterministically inject control flow errors. Our process can inject inter-block, intra-block and out-of-function errors deterministically using the control flow graph of the target program. Next, we show that this process can also be used to perform a vulnerability analysis to assist in choosing the correct fault tolerance measure.

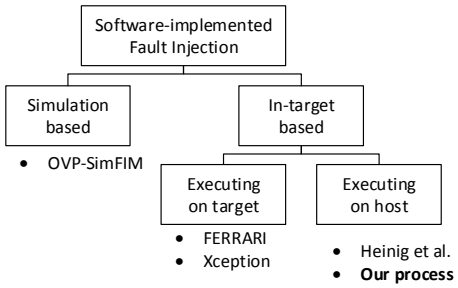

Fig. 1: Overview of software-implemented fault injection categories and tools.

The rest of the paper is organized as follows. Related Work is presented in Section II. The new control flow aware injection process is presented in Section III. Section IV describes the fault injection experiment setup. The results of the performed experiments are presented in Section V. Section VI discusses how the proposed process aids in performing a vulnerability analysis for the target algorithm. Future work is presented and conclusions are drawn in Section VII and VIII respectively.

II. Related Work

This section summarizes different approaches to software-implemented fault injection and provides examples of existing tools. A more extensive overview of fault injection is given by Hsueh et al. [10]. Existing software-implemented fault injection techniques can be divided into two groups, the technique is either simulation based or in-target based, as shown in Fig. 1.

A. Simulation based

Simulation based injection tools use models and simulations of the target hardware and inject faults into those simulations. The advantage of such tools is that a fault can be injected into every hardware location e.g., CPU registers, main memory or Direct Memory Access controller. The disadvantage of these tools is the limited availability towards platforms. Some effort is required to create or extend the tool for a new platform. An example of a simulation based tool is OVPSim-FIM, a fault injection framework built around the OVPSim framework, which provides models and the simulation framework for a variety of microprocessors [11]. OVPSim-FIM is an

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extension that allows fault injection into CPU registers, main memory and interconnection structures [12].

B. In-target based

In-target based tools inject faults into a physical target system through source code modification or by using the on-chip debug capabilities of modern microprocessors. A disadvantage of these tools is that they cannot access hardware areas that are not accessible via source code or the on-chip debugger. An example of a source code modification technique is binary modification. This compile-time technique manipulates the binary before it is loaded onto the target by changing branch destinations or memory addresses. Another example is inserting time-outs. A timer, implemented in hardware or software, expires at a predetermined time which triggers the injection of a fault. This technique is used to inject faults with an unpredictable outcome, such as transients or erroneous bit-flips. FERRARI is a tool that uses timeouts to change the content of registers or memory locations at random times to emulate realistic data corruption [13].

Fault injection tools that use the on-chip debug capabilities either set the debugger to trap certain memory accesses or instructions, or call the debugger from a host system. In both cases, the debugger is used to modify the content of CPU registers or main memory. Xception uses the on-chip debugger to inject both stuck-at and transient faults, when certain addresses are accessed or instructions are executed [14].

III. Control Flow Aware Injection Process

Most of the tools described in Section 2 lack the possibility to deterministically inject both data flow errors and control flow errors. To test and validate software-implemented fault tolerance techniques, such deterministic injection is needed. Heinig et al. proposed a process in order to deterministically inject data flow errors [15] and we propose a process to deterministically inject control flow errors. As depicted by Fig. 1, these processes affect the physical target but execute on a host system such as a PC or another embedded system.

A. Principle

To deterministically inject control flow errors, we propose a new injection process which is capable of corrupting the control flow by analyzing the control flow graph of the target program. The control flow graph is a directed graph based on basic blocks of instructions and edges between those. A basic block is a sequence of instructions with 1 entry and 1 exit point. The edges represent the legal paths between such blocks.

Our process creates the control flow graph in memory by analyzing the disassembly file of the program. As depicted by Fig. 2, the analysis results in Program Counter values mapped to basic blocks and legal edges converted to legal Program Counter jumps. By using the in-memory control flow graph, the correct flow of the target can be corrupted deterministically. An erroneous bit-flip can have one of three possible outcomes on the control flow of the program. The bit-flip either causes an intra-block jump, an inter-block jump or a jump outside the program memory. An intra-block jump is an erroneous jump inside a basic block and an inter-block jump is an erroneous jump between two basic blocks. The third possibility is a jump that originates within the program but lands out of it, into unused memory containing non-specified instructions. We developed processes to deterministically inject the three possible errors.

The following presents the process to deterministically inject an inter-block control flow error. First, the Program Counter of the target is read out and the basic block of the read out value is determined. Based on that information, a new Program Counter value is calculated. This is done by first creating a list of all possible new values, flipping a bit at each bit position. Next, the non-existing Program Counter values in the program and the intra-block jump values are discarded. If the filtered list of possible new Program Counter values contains more than one value, the new Program Counter value is chosen at random. This increases the fault coverage of the fault injection experiments. Finally, the new value is written to the Program Counter.

The same process is used to deterministically inject intra-block jumps. Instead of discarding the intra-block values, the inter-block values are discarded. To inject jumps that land outside the program, both the inter- and intra-block values are discarded.

B. Example

The following is an example of injecting an inter-block control flow error using the described process:

0. Assume the program depicted in Fig. 2, which has Program Counter values between 0x1c8 and 0x1da. An inter-block jump will be injected;
1. The Program Counter is read out: its value is 0x1d2;
2. Create a list of all possible values, by flipping a bit at each position: {0x1d3, 0x1d0, 0x1d6, … 0x9d2};
3. Discard all non-existing values: {0x1d0, 0x1d6, 0x1da};
4. Discard all intra-block values: {0x1da};
5. Write the new value to the Program Counter: the Program Counter now has the value of 0x1da.

IV Experiment Setup

We implemented the described processes as Python scripts that focus on the ARM Cortex-M processor family. The external host, a PC or laptop, connects to the on-chip

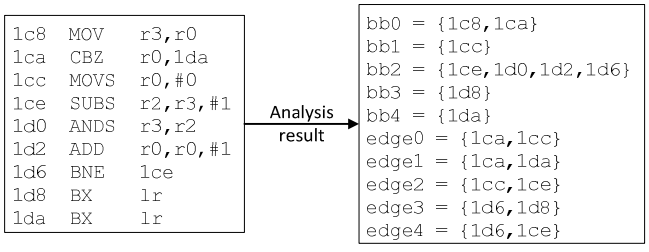

Fig. 2: Example of the Control Flow Graph analysis.

TABLE 1: RANDOM INJECTION RESULTS, WITH 3000 BIT-FLIPS INJECTED [%].

Case study	Intra-block	Inter-block	Out-of-function	Hard Fault	Wrong Result	No Effect
Bubble sort	5.6	6.9	**87.5**	**82.9**	5.0	12.1
Quick sort	3.3	9.6	**87.1**	**82.3**	3.3	14.4
Matrix multiplication	3.9	6.7	**89.2**	**85.3**	10.8	3.9
FFT	10.1	9.5	**80.4**	**80.1**	9.9	10.0

TABLE 2: CONTROL FLOW AWARE INJECTION RESULTS, WITH 3000 BIT-FLIPS INJECTED [%].

Case study	Intra-block	Inter-block	Out-of-function	Hard Fault	Wrong Result	No Effect
Bubble sort	33.3	33.3	33.3	23.3	23.5	**53.2**
Quick sort	33.3	33.3	33.3	25.1	13.4	**61.5**
Matrix multiplication	33.3	33.3	33.3	33.1	**45.0**	21.9
FFT	33.3	33.3	33.3	27.2	33.7	**39.1**

debugger of the processor via USB to inject the requested bit-flips. To validate the fault injection processes, we selected four case studies. The case studies are an implementation of the bubble sort, quick sort, matrix multiplication and FFT algorithms. The implementations of bubble sort, quick sort and matrix multiplication are our own and we used the MiBench 1.0 implementation for the FFT case study [16]. With the selected case studies, a variety of embedded application domains such as robotics, image processing and data compression are covered. To be able to execute the case studies, some setup code such as filling the necessary data structures with values is required. Faults are, however, only injected when the target algorithm is executing.

The case studies are executed on an ARM Cortex-M3 driven microcontroller running at 96 MHz including 512 kB FLASH and 32 kB RAM. This microcontroller was selected because the ARM Cortex-M3 is an industry-leading 32-bit processor used in many different embedded application domains.

By using this target, each injected bit-flip can have one out of three outcomes. It either causes a hard fault, a wrong result or has no effect on the outcome of the algorithm. If an injected error caused a hard fault, it means that is was detected by a fault handler present in the processor. Some processors, such as the ARM Cortex-M3, have internal fault handlers that detect certain types of faults, such as improper bus usage or memory access violation.

V. EXPERIMENT RESULTS

To analyze our control flow aware injection process, we injected 3000 errors at random in the target and 3000 using our process in each of the four case studies.

For the random injection, a random bit of the Program Counter of the target was flipped. Table 1 shows the results of the random injection, with the largest value for each case study indicated in bold. It can be seen that the random injection mainly injects out-of-function jumps. Out-of-function jumps are jumps that originate in the target algorithm but land in either the setup code or outside the program memory. Random injection cannot be used in order to deterministically test against intra-block and inter-block jumps. Analyzing the result of the injected bit-flips, it can be seen that on average 82.7 % of the injected bit-flips resulted in hard faults. The most desired outcome, namely a wrong result, is the smallest category. To validate fault tolerance measures, bit-flips that produce wrong results are needed since only those bit-flips are able to test the fault tolerance measure.

Using our Control Flow aware injection, we can specify to inject 1000 intra-block, 1000 inter-block and 1000 out-of-function jumps. The results of the error injection are shown in Table 2. Although the type of the jump can be specified, the process cannot guarantee the result of the jump. As can be seen, for the bubble sort and quick sort most of the injected jumps had no effect on the algorithm. Only 23.5 % and 13.4 % produced a wrong result respectively. The matrix multiplication proved more vulnerable to control flow errors, with 45.0 % of the injected jumps resulting in a wrong result. For the FFT case study, the outcomes of the injected jumps are more evenly distributed over the three categories.

VI. VULNERABILITY ANALYSIS

Given that our control flow aware injection process is able to deterministically inject the three types of control flow errors, it can be used to analyze the vulnerability of a target algorithm against each type. This analysis can aid in assigning a priority or severity to each type of error, which assists in choosing which fault tolerance measure(s) to implement. The result of such a vulnerability analysis is shown in Table 3. Per error, the largest category of result is represented in bold.

The first result of the analysis is that an out-of-function jump causes either a hard fault or has no effect on the outcome of the algorithm. On average 90 % of the injected out-of-function jumps had no impact on the case study, making this type of error target the least severe on the selected hardware. However, this result is target dependent, because not all processors may have internal fault handlers that detect this type of jump.

TABLE 3: EFFECT OF THE DIFFERENT TYPES OF CONTROL FLOW ERRORS (CFE) ON THE DIFFERENT CASE STUDIES [%].

Case study	CFE type	Hard Fault	Wrong Result	No Effect
Bubble sort	Intra-block	0.1	22.6	**77.3**
	Inter-block	1.9	45.4	**52.7**
	Out-of-function	**67.9**	2.6	29.5
Quick sort	Intra-block	3.9	17.0	**79.1**
	Inter-block	16.2	17.4	**66.4**
	Out-of-function	**55.2**	5.7	39.1
Matrix mult.	Intra-block	7.4	**56.8**	35.8
	Inter-block	41.7	**55.7**	2.6
	Out-of-function	**50.3**	22.5	27.2
FFT	Intra-block	8.0	32.5	**59.5**
	Inter-block	22.9	**59.1**	18.0
	Out-of-function	**50.8**	9.4	39.8

The second result of the analysis is that the selected algorithms already reach a certain level of reliability without any fault tolerance measure implemented. The *No Effect* category is the largest for each intra-block and inter-block injection. An exception is the matrix multiplication case study, which shows to be vulnerable against both intra-block and inter-block jumps. The FFT implementation proved to be vulnerable against inter-block jumps.

Using this analysis, an engineer can decide what type of fault tolerance measures must be implemented and which types of errors can be ignored.

VII. FUTURE WORK

The current architecture in which we implemented the injection process has certain disadvantages. The main issue is that a lot of overhead is introduced by using USB communication. This overhead not only means that injection experiments take a lot of time, but also is the main reason why extensive, detailed reporting of the experiments is not possible. Metrics as time per fault or program coverage can not accurately be measured.

To solve this problem, we'll port the injection process to a simulation based fault injection tool. This will eliminate the communication overhead needed to communicate with a physical target and thus allow faster injection experiments.

VIII. CONCLUSIONS

This paper proposed a new fault injection process, control flow aware injection, which makes it possible to deterministically corrupt the control flow of the target embedded system. By providing the control flow graph of the program running on the target, the tool can use that information to assure the injected fault affects the control flow.

Secondly, we showed how our proposed control flow aware process makes it possible to analyze the vulnerability of a program against control flow errors. A target algorithm can be analyzed for its vulnerability against intra-block, inter-block and out-of-function errors. This analysis aids in prioritizing the implementation of fault tolerance measures.

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Functional Safety Standard's Techniques and Measures in Light of Electromagnetic Interference

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Abstract – **Everyday modern electronic programmable systems are performing more and more safety-critical tasks. Due to electromagnetic interference (EMI), these systems potentially violate their predefined safety goals. Appropriate actions must be taken to ensure the system's integrity. This paper looks at proposed safety standard techniques in the light of EMI. Redundancy and error detection and correction schemes are not only reviewed, but recommendations are provided to increase the EMI-resiliency of the considered system.**

Keywords – **Functional Safety, Electromagnetic Interference, Redundancy, Resilience**

I. Introduction

Embedded systems are fulfilling an ever more prominent role in everyday life, even in safety-related applications such as avionics, medical and automotive. Nowadays, these systems are packed with programmable electronics. The hardware is directly affected by EMI. However, since software uses hardware, the EMI disturbance effects are able to disturb software operation as well. Because of the susceptibility, there is a risk of a system failure. Such failures might lead to severe harm for both humans and the environment. In current functional safety standards, such as IEC 61508 (General) and ISO 26262 (Automotive), many fault-tolerance techniques are proposed to aid in the compliance with these standards. Note that not all fault-tolerance techniques are able to mitigate the effects of EMI. Designers implement these techniques to reach a certain required safety integrity level (SIL), and hence increases the confidence that the device will function as intended without the violation of safety goals.

Three major reasons are responsible for making current devices in operation intrinsically less resilient to EMI:

(1) The decrease of the minimum feature size to reduce heat generation and to increase transistor density;
(2) A continued lowering of supply voltages to reduce power consumption and heat dissipation;
(3) Harsher electromagnetic environments, due to an increase in the number and strength of transmitting (and thus EMI-emitting) devices.

The fault-tolerance techniques selected from the safety standards are classified as mandatory (M) or highly-recommended (HR) for each SIL. Even though some techniques are adequate on their own, others might need some changes to have the ability to mitigate adverse EMI effects. This paper only considers the general safety standard (IEC 61508) and its automotive derivative (ISO 26262).

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This paper is organised as follows. Section II introduces the functional safety concept. In Section III, more details on EMI are presented. The resiliency techniques and their (dis)advantages are assessed in Section IV. Conclusions are drawn in the final Section.

II. Functional Safety Concept

In the general functional safety standard [1], safety is defined as the freedom of unacceptable risk. Risk is the combination of the probability of occurrence of harm and the severity of that harm. Functional safety is defined as the part of the overall safety relating to the Equipment Under Control (EUC) and the EUC control system. It depends on the correct functioning of electrical and/or electronic and/or programmable electronic (E/E/PE) safety related element. An element is a part of a subsystem comprising a single component or any group of components that performs one or more element safety functions. A safety function is a mechanism to achieve and maintain a system's safe state.

IEC 61508 defines multiple levels of safety integrity, referred to as Safety Integrity Level (SIL). SILs are numbered from 1 to 4, whereby SIL4 is the more stringent. These SILs are dependent on the average probability of a failure of the system's safety function. In other words, the failure of a system is not assessed, but the failure of the safety system around it is of utmost importance, since the latter might lead directly to harm or injury.

The failure rates that are specified by the SIL are dependent on the demand mode of the safety-related system. IEC 61508 defines three demand modes:

(1) Low demand mode: the safety function that transitions the system into a safe state is invoked on demand, with a frequency less than once per year. An automotive example is an airbag.
(2) High demand mode: The safety function is also invoked on demand, but is invoked more than once per year. An anti-lock braking system (ABS) or traction control system (TCS) are examples of systems for which the safety function might be needed more than once per year.
(3) Continuous demand mode: the safety function keeps the EUC in a safe state as part of normal operation.

The safety function's maximum failure rate is dependent on the demand mode. For low demand systems, it is expressed in probability of failure on demand (PFD). For the other systems, the probability of failure per hour (PFH) is used. Table 1 summarizes the SILs and their failure rate.

Since one year is 8,760 hours of operation, the factor 10^{-4} is explained.

TABLE 1. SILS AND THEIR FAILURE RATES

SIL	Probability of Failure on Demand (PFD) – Low Demand Systems	Probability of Failures per Hour (PFH) – High and Continuous Demand Systems
D	$\geq 10^{-5}$ to $< 10^{-4}$	$\geq 10^{-9}$ to $< 10^{-8}$
C	$\geq 10^{-4}$ to $< 10^{-3}$	$\geq 10^{-8}$ to $< 10^{-7}$
B	$\geq 10^{-3}$ to $< 10^{-2}$	$\geq 10^{-7}$ to $< 10^{-6}$
A	$\geq 10^{-2}$ to $< 10^{-1}$	$\geq 10^{-6}$ to $< 10^{-5}$

For ISO 26262 [2], ASILs are defined in four Automotive SIL levels: ASIL A/B/C/D, with D being the more stringent. ASILs are composed of three pillars: severity, exposure and controllability. During the risk and hazard analysis, each hazard will be classified according to all three measurements, from which an ASIL level will be defined.

Obviously, systems are not composed solely from safety-related functions. For the elements that do not have any safety-related functions, both standards define that they should be designed, implemented and maintained in accordance with a quality management system, such as ISO 9001.

Safety of a product must be assessed during its entire lifetime. The product undergoes many phases, such as: design, implementation, integration, validation, verification, installation, operation, maintenance, upgrade, repair and decommissioning. Even during the time it's disassembled, e.g. during maintenance or decommissioning, the system cannot pose a direct threat to users, bystanders or the environment.

The risk and hazard analysis requires the assessor to review many different factors that can influence the operation of a device. Some factors to be considered are: temperature, humidity, vibrations, operational limits (and foreseeable misuse) and, as focus of this paper: EMI.

III. ELECTROMAGNETIC INTERFERENCE

In simple terms, EMI can be defined as the disruption of operation of an electronic device when it is in the vicinity of an electromagnetic field. However, the disruption itself and the cause for disruption can be very diverse.

A classification of EMI sources is made in Fig. 1. Five categories are used to distinguish different sources of EMI [3]. The first distinction of EMI sources is that they can be artificial or natural. Artificial EMI is originating from man-made devices and infrastructure. Lightning on the other hand, is an example of natural EMI. Secondly, the difference is made between narrowband and broadband EMI. Broadband disruptions have a greater frequency range than the bandwidth of the device subjected to EMI, whereas narrowband disruptions have a smaller bandwidth. Thirdly, EMI-events can be coherent or incoherent. Coherent EMI is defined as signals with a well-defined relationship between amplitude, frequency and phase. Fourthly, EMI can be conducted or radiated. Conducted EMI propagates through electrical conducting paths such as grounding planes or wires. All non-conductive EMI is classified as radiated. The fifth category is whether or not the device is transmitting intentionally. Intentional radiating devices are emitting devices whose primary function is dependent on radiated emitters, such as communication, navigation and radar systems. Natural EMI events are by definition classified as unintentional. Restricted radiating devices only access the ether for a limited time, such as garage opening systems and wireless microphones.

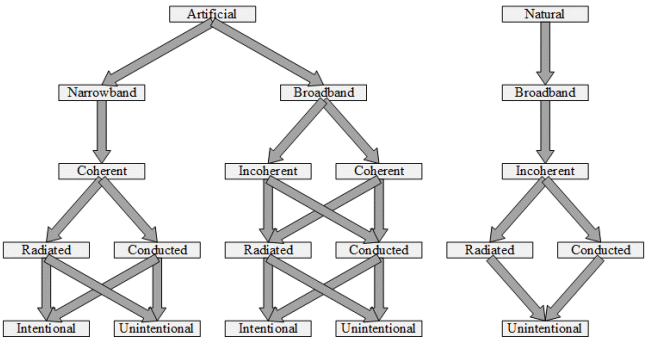

Fig. 1. Classification of EMI Sources [3]

Even though the sources of EMI can be clearly classified, it is impossible to determine which disturbances will occur in the EUC's life-cycle [4]. The techniques used for mitigating the negative effects on a system and its control mechanism should thus protect against as much disruptions as possible.

As mentioned in the introduction, both hardware and software effects are seen. In hardware, EMI can result in noise accumulating on traces which leads to false readings on inputs or distortion on outputs. Transients (bursts), power surges and communication channel corruptions are possible. More EMI phenomena are described in the IEC 61000 series. Software errors due to EMI are classified in data flow and control flow errors, which are elaborated further in [5] and [6].

IV. EVALUATION OF TECHNIQUES

This Section provides a selection of techniques mentioned in the functional safety standards, accompanied by special considerations when used in a harsh electromagnetic environment. It must be noted that each of the techniques is not sufficient on its own, since it will target one specific kind of vulnerability. As mentioned, EMI can strike a system anywhere anytime. The perfect combination of techniques is impossible to determine in this paper, since this is in the largely dependent on the considered application and system.

Since there is an abundant selection of techniques and measures available to be used, this paper attempted to group them in to categories for which the arguments are valid for each of the techniques in that group.

Hardware and software development are mentioned separately in the standards. For the automotive standard, ISO 26262-5 covers the product development at the hardware level, whereas ISO 26262-6 is dedicated to the software development cycle. Each part will have dedicated techniques and measures to be used, so each of the categories is therefore found in hardware as well as software. Depending on the considered techniques, the same arguments pro or anti can be given. Note that some techniques in hardware have an equivalent in software and vice versa.

A. Redundancy

Redundancy is the duplication of critical components or elements in order to increase the resiliency of the system. It is exploited in two possible configurations: backup redundancy and load sharing redundancy. In the first case, the redundant (backup)components do not actively participate in the system's operation. Only when the main (active) component fails, the backup takes over. The backup itself can be in either hot or cold standby mode. Hot standby configurations consume power, but are immediately operational. A cold backup needs initialization time before it can perform its failover function. In load sharing configuration, the backups are actively participating. However, to provide failover, the system should not function to the full capacity.

For example, a four-component system has to process 240 units of work. Each component gets 60 units. Upon failure of one of the nodes, the 240 units are redistributed to the remaining three nodes, which all need to process 80 units. When a limit of 100 units per component is assumed, the system cannot tolerate another component failure without performance loss.

In light of an EMI disturbance, the redundancy mentioned above might not be sufficient. EMI should be seen as a systematic failure, since a specific disturbance will result in specific behaviour of the system. When that system is not adequately equipped to deal with EMI, the disturbance is regarded a common cause failure, where all nodes of the system are affected by the same cause of failure.

To cope with the deterministic and common cause nature of EMI, the redundancy should be expanded with electromagnetic diversity, in order to create different behaviour under the influence of the same EMI disturbance. This diversity is obtained by various methods, such as using different architectures (processors, memories), inversion of data and signals, a different implementation of the same algorithm and desyncing components, both in hardware and software. The following example demonstrates the difference between a normal and diverse communication channel.

The comparison is made between a communication channel that uses two data lines with the same voltage (common mode) and one with differential signalling. Both setups are shown in Fig. 2.

It is assumed that a '0' is sent as 0V on both lines in both cases. In the common mode channel, a '1' is represented by sending 1V on both lines. On the other hand, in the differential mode channel inversion is used. Thus on one data line, 1V is sent whereas on the other line, -1V is transmitted. For common mode, the voltages are added and divided by two. The differential mode receiver will subtract the voltages found on the lines and divide the value by two.

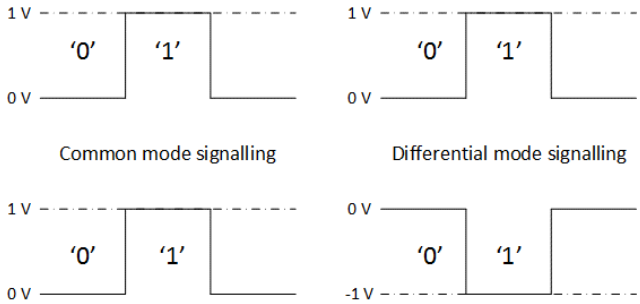

Fig. 2. Common mode and differential mode signalling

Due to an EMI disturbance, 1.5V is superposed onto the data lines. In the common mode case with disturbance when a '0' was sent, the receiver sees the following voltages on the data lines: D1 = 1.5V and D2 = 1.5V, and comes to the conclusion that a '1' has been received. This will translate into a bit error in the system. For the differential signalling, the voltages on the data lines are the same. Due to the subtraction, the common mode error is fully eliminated. The receiver sees two times 1.5V, which are subtracted and divided, leaving the correct decoding of a '0'.

B. Error Detection and Correction (EDC) techniques

Whereas redundancy is considered a fault masking technique, error detection and correction techniques will actively search for and attempt to correct induced faults in the system. Whichever technique is used, the main goal is to assure that the system is aware that faults have occurred and to prevent the faults from inducing any potential harmful event to humans and environment.

The fault tolerance process consists of three distinct phases which must be fulfilled. Firstly the fault must be detected. Without detection, faults can remain within the system and retain the ability to cause failures. When a fault is detected, it must be contained within the part or module of the system where it occurred. At this point, freedom of interference [2] can be reinforced. Freedom of interference is defined in ISO 26262 as the absence of cascading failures between elements: failure of one element cannot cause another element to fail. The third step is the fault correction, for which different techniques can be used to achieve the recovery.

This paper considers two types of EDC techniques: error correcting codes and duplication. The choice for these specific techniques is made based on their appearance in the functional safety standards and popular application into different systems. Another consideration was made in terms of portability, since each of the techniques can be implemented on all aspects of computer systems, such as memories and buses.

Error correcting codes (ECC) themselves are categorized in convolutional codes and block codes. In a convolutional code, the data is processed in a bit-by-bit fashion. Similarly, block codes process the data per block, where the block size

is either dependent on the code itself, or is free of choice. The probably most widely known block codes are Hamming and Reed-Solomon codes.

Each code is design to withstand a certain predefined amount of errors. EMI does have the ability to flip more bits than the code is designed for. In a harsh EMI environment, ECC can reduce the error rate, but cannot guarantee an error free system.

Duplication is closely related to redundancy on a block data level. Whereas redundancy duplicates elements or components, the duplication considers data specifically. The same remark must be made as with redundancy, that the duplication should be performed in an electromagnetically diverse way. One of the most effective ways is to introduce the differential aspect mentioned before. The inverse of a data block can be stored. The common mode EMI disturbance will be detected due to the differential nature of the technique.

Note that a minimum of three diverse data blocks is needed in order to perform a correction. This is called the Hamming distance of a code and will determine the corrective power of the code. A code with a distance of three is called a single-error-correcting (SEC) code.

For bit sequences, SEC codes bear one main dis-advantage: a double bit error can be mistaken for a single bit error and will thus perform a false corrective action. Since EMI is expected to disturb adjacent bits, the SEC codes can be specifically altered to target these errors. Sánchez et al. [7] developed specific codes to correct single errors, with the ability to correctly identify all double errors and triple adjacent errors.

C. Monitoring

When the implementation of a component or subsystem is unknown, it is seen as a black box system. In safety-critical systems, monitoring is used to assure correct behaviour of the component. Commercial Off The Shelf (COTS) are used in this fashion.

Since the system's implementation is unknown (and unchangeable), the only option would be to double or triple the component in order to gain redundancy. Recall that this does not fulfil the electromagnetic diverse requirement.

How the monitor is implemented, depends strongly on the considered application. However, plausibility checking can be grouped in categories, which are illustrated using an example. An electronic throttle control (ETC) is considered. This is an automotive application linking the throttle pedal (input) to the throttle (output), removing the need for a mechanical connection. The ASIL is ignored for this example, because the stress is on the implementation of the control checks. The ECT itself is used by other electronic systems, like cruise control, stability control and traction control. In each of the following situations, the monitor will be implemented in different ways.

Firstly, a range check is used as monitor. For any given output, the value is checked with a static range for correctness. For values that fall without the normal operating range, an error is reported and appropriate action is taken. Exemplary values might be a range between 0 and 100 percent of throttle valve opening.

Secondly, a differential check is implemented. The differential check verifies the difference between the last value and the newly received one. When they differ too much, an error is reported and appropriate action is taken. Note that correct assumptions for the value of the maximum difference must be assessed.

Many other monitoring configurations exist. However, these kinds of checks are never fail-safe for 100%, since there is no fine-grained error detection. The checks are based on logic and specifications of the device.

Special care must be taken to make the monitor as resilient as possible, since it too can fall under the influence of EMI and thus produce false results. Note that these monitoring examples will not cover all possible faults and more protection should be provided.

V. CONCLUSION

Safety-critical application residing in harsh electromagnetic environments must be developed with EMI in mind. The deterministic nature of EMI results in an ability to harden the systems in use, but due to the impossibility of predicting which EMI the system will encounter, one technique will never suffice to gain a 100% coverage of EMI induced faults and must be combined.

This paper reviewed some of the proposed techniques in the functional safety standards, under the light of electromagnetic disturbances. The main topic of consideration was the electromagnetic diversity, so that techniques like redundancy and error detection schemes do not fail because of common cause induced failures. Furthermore was the utilization of inversion reviewed and the reason why it is so effective against EMI.

When COTS systems are used in a safety-critical setup, considerate action must be taken to ensure the freedom of interference expected by functional safety standards.

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Electromagnetic Interference in the Internet of Things: an automotive insight

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Abstract – **This paper reviews the Internet of Things in an automotive setting, complemented by Electromagnetic Interference as a cause of failures. Electromagnetic Interference is, as a common cause failure, able to disturb even redundant systems. Due to the safety-critical nature of automotive applications, different methods in order to reduce the susceptibility and to increase the robustness of automotive IoT are reviewed. Inter-, intra- and extra- vehicle IoT is considered, using a currently used system as a running example.**

Keywords – **Internet of Things, Electromagnetic Interference, Communication, Adaptive Cruise Control**

I. Introduction

Our modern world is evermore dominated by programmable electronics, in every aspect of our lives. Driven by the Industry 4.0 revolution, smart devices are used from Smart Homes over Smart Cities to Smart Factories. By 2025, the Internet of Things is projected to have an $11 trillion impact on companies all around the world [1]. The automotive sector is not escaping this trend; modern cars include fifty or more separate microcontrollers, each responsible for a specific function. More and more, those microcontrollers are used in a safety-critical environment, where a failure might result in injury, and in the worst case, even death.

Many factors influence the correct behavior of programmable electronics, including but not limited to: humidity, temperature, misuse and Electromagnetic Interference (EMI). This paper focusses on the latter, since this topic is still gaining more and more importance for modern electronics. The increased influence of EMI is due to three major trends in present-day systems:

(1) The lowering of internal voltages, allowing reduced power consumption and heat dissipation;
(2) The reduction of the minimum feature size, allowing an increased transistor density and thus increasing performance per area for the electronic device;
(3) The electromagnetic environment is becoming increasingly harsher, due to more and more transmitting devices in use today. This makes the ether more crowded and allowing devices to interfere with each other.

This paper follows the general IoT description given by Xia et al. specify the IoT as the networked interconnection of (everyday) objects, which are often equipped with ubiquitous intelligence [2]. In the following Section, the automotive viewpoint on the Internet of Things is given. In Section III, the concept of EMI is introduced. Section IV provides an example of EMI vulnerabilities in automotive IoT and the protective measures are covered in Section V. Lastly, the conclusions are drawn in Section VI.

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II. Automotive Systems as IoT

Depending on which systems are interconnected in the IoT network, three categories are observed. Firstly, intra-vehicle networks are studied, whereby the communicating systems are all located within the same vehicle. Secondly, inter-vehicle communication is considered. This is the communication between (independent) vehicles. Thirdly, extra-vehicle IoT is mentioned, whereby the vehicle is communicating with either the Cloud or road-side infrastructure. Wired networks are usually used for intra-vehicle communication, whereas wireless is used in inter- and extra-vehicle systems. Naturally, all systems are manufacturer-dependent concerning the implementation.

A. Intra-vehicle IoT

Modern cars carry many different Electronic Control Units (ECUs). Each of them has a specific responsibility and a set of tasks. One is responsible for the interior lighting, another for the Anti-lock Braking System (ABS). For safety-critical applications, functions such as Adaptive Cruise Control (ACC), Electronic Stability Control (ESC) and the Blind-spot Information System (BLIS) can be considered. When the ECUs need to communicate, they use the automotive buses present in the vehicle. Two examples of automotive buses are the Local Interconnect Network (LIN) [3] and Controller Area Network (CAN) [4]. An example is given in Fig. 1, which shows several ECUs used in present-day cars being connected via a CAN bus.

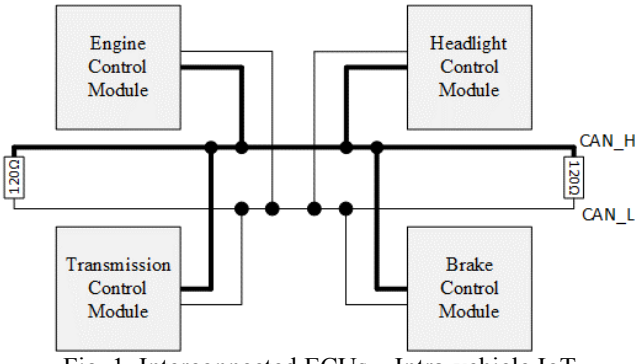

Fig. 1. Interconnected ECUs – Intra-vehicle IoT

The example is an actual CAN network used in the Volvo C30, S40 (2004+), V50 and C70 (2006+) and is extracted from the open-source Volvo wiring diagrams [5].

Note that Fig. 1 is not complete in terms of all components. Only the control modules are displayed and how they are interconnected. Each module itself is connected to sensors and actuators, forming a network of their own.

B. Inter-vehicle IoT

Interest in intelligent transport systems has been shown in recent years. Currently, such systems are able to sense their surroundings and respond appropriately. Research and development, however, is focusing on new more intelligent systems that are able to communicate with each other in order to respond to (external) events. A specific research path is vehicle to vehicle (V2V) communication, which enables vehicles to send messages to each other. V2V is being tested within several project issued by the European Commission [6]. The biggest domain that pushes V2V forward, is autonomous driving. Autonomous vehicles need to be able to communicate with each other, in order to make the correct decision in each situation. To the best of the authors' knowledge, there are no production cars yet that use V2V communications.

Autonomous driving using V2V is expected to massively improve safety. From a survey conducted from 2005 to 2007 by the National Highway Traffic Safety Administration (NHTSA), it seemed that the driver was responsible for the crash in 94% (± 2.2%) of the cases [7]. Errors due to driver's inattention, internal and external distractions and inadequate surveillance were the main reasons for crashes due to driver error. Furthermore, decision errors such as tackling corners too fast, misjudging other's speed and actions and performing illegal manoeuvres were found to account for 33% (± 3.7%) of the driver's errors. Autonomous cars are immune to fatigue and distractions, thus they are expected to be safer. Naturally, further improvements in other technologies such as artificial intelligence and machine learning, are in progress.

C. Extra-vehicle IoT

Next to V2V, extra-vehicle communication such as interfacing with road-side infrastructure, is being researched. This paragraph discusses two distinct systems: a fleet management system and vehicle-to-infrastructure (V2I) communication.

(1) By enabling the vehicles to send the information it can gather about itself to the cloud, the management of a fleet is streamlined and perfected. Mileage, fuel consumption, GPS-location and more are gathered, sent to the cloud and used to plan the mandatory maintenance in advance, in accordance with the vehicle's schedule. The gathered information can also be used as input to optimize routes, known in literature as the Travelling Salesman Problem [8].

(2) V2I communication enables vehicles to communicate with road-side infrastructure, such as traffic lights and road signs. This communication can have a huge impact on many factors of everyday driving, from reducing traffic incidents and increasing traffic flow, to parking space management and eco-driving. An example is given by Lin et al. [9]. They researched how V2I can save fuel when vehicles are enabled to communicate with traffic lights. Due to the communication, braking, stopping and accelerating can be avoided as much as possible, saving fuel for the vehicle. Note that the road's speed limit is taken into account in their algorithm.

III. ELECTROMAGNETIC INTERFERENCE

EMI can be defined as the disruption of operation of an electronic device when it is in the vicinity of an electro-magnetic field.

EMI is found in many forms and a classification is made in Fig. 2. Five categories are used to distinguish different sources of EMI [10].

The first distinction of EMI sources is that they can be artificial or natural. Artificial EMI is originating from man-made devices and infrastructure. Lightning on the other hand, is an example of natural EMI. Secondly, the difference is made between narrowband and broadband EMI. Broadband disruptions have a greater frequency range than the bandwidth of the device subjected to EMI. Thirdly, EMI-events can be coherent or incoherent. Coherent EMI is defined as signals with a well-defined relationship between amplitude, frequency and phase. Fourthly, EMI can be conducted or radiated. Conducted EMI propagates through electrical conducting paths such as grounding planes or wires. All non-conductive EMI is classified as radiated. The fifth category is whether or not the device is transmitting intentionally.

Intentional radiating devices are emitting devices whose primary function is dependent on radiated emitters, such as communication, navigation and radar systems.

Natural EMI events are by definition classified as unintentional. Restricted radiating devices only access the ether for a limited time, such as garage opening systems and wireless microphones.

Effects of EMI corruption are seen in both hardware and software. In hardware, the effects of EMI can result in noise accumulating on traces and leading to false readings on inputs or distortion on outputs. As a result, software effects such as jumps in the program execution and data corruption can be witnessed. Protection techniques for program jumps are more closely studied in [11].

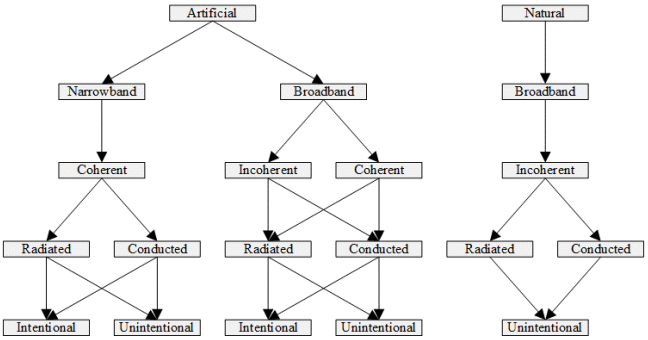

Fig. 2. EMI Source Classification [10].

An overview of data protection techniques is provided in [12]. Both conclusions find that there is no protection without extra code size and execution time overhead. For automotive applications, the choice of the correct technique can prove difficult, since both the real-time aspect (and thus execution time) as program memory (code size) are important factors to consider. Nonetheless, correct operation should be the main concern in each design.

IV. EMI IMPACT ON AUTOMOTIVE IOT

This section takes a closer look at one example system within a modern car. By using this example, the impact of EMI on IoT setups is illustrated. For this purpose, Adaptive Cruise Control (ACC) is considered. ACC automatically adjusts the speed of the car to match the speed of the vehicle in front of it in order to stay at a preset distance. Depending on the movement of the preceding car, the ACC either retains the lower speed, or resumes its former speed when the road is cleared. This paper considers ACC in two possible configurations to assess the impact of EMI: an intra-vehicle and an inter-vehicle setup.

A. Intra-vehicle ACC

An intra-vehicle setup uses different sensors to assess the distance between the car itself and the one in front. Possible implementations are for example lasers, cameras and radars. In Fig. 3a, the setup is provided.

Due to an electromagnetic disturbance, the used sensor can give false readings or the ECU might calculate a wrong value. For example, the car might experience a sudden acceleration based on faulty calculations or values. The driver is still in charge, which allows him to interact with the system and take protective and corrective action. When autonomous driving breaks through, the system will have to be able to fully detect and correct errors, without manual intervention.

Upon failure of the system, the car might behave in three distinct ways: operation where no operation is required, no operation where operation is required or incorrect operation of the system. In each case, the driver should be able to contain the effects of a failure. Note that a failure in this case results in the incorrect behaviour of only one car. Each vehicle makes up its own mind according to its sensors and design logic.

B. Inter-vehicle ACC

In nearly the same configuration as Section A, the system is now implemented as an inter-vehicle setup, as can be seen in Fig. 3b. The main difference is, since the cars are able to communicate, that more and more cars get involved. Three or more cars driving in convoy, can perfectly adopt the speed of the first one, since it is communicated down the line.

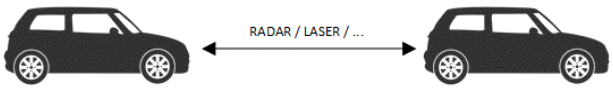

Fig. 3a. ACC as intra-vehicle IoT system

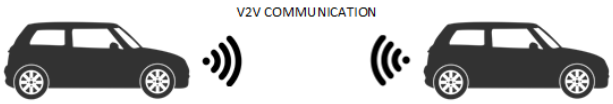

Fig. 3b. ACC as an inter-vehicle IoT system

B. Inter-vehicle ACC

Even further, the communicating cars are able to drive at the same speed in a multi-lane configuration. This would result in less acceleration and deceleration, which improves traffic flow.

However, when one of these cars malfunctions or sends out the wrong speed, multiple cars become affected. When fully autonomous cars are considered, enough fault-tolerance must be built in. Naturally, an intra-vehicle configuration might be used as a backup system.

Deployment on inter-vehicle systems and V2I communication is estimated to commence in 2019 [13].

C. Extra-Vehicle Impact

In the same way that EMI can cause corrupt values within the vehicle, false data can also be sent to the fleet management system. Based on false information, incorrect calculations might be made and wrong decisions taken. These systems usually do not reside in a safety-critical position, but they can have a mission-critical character or function that proves essential for the company.

In the case of infrastructure however, the case might be totally different. A red traffic light emitting the status of being green, can have disastrous consequences when high-speed dense traffic is passing by.

V. DESIGNING AN EMI-RESILIENT AUTOMOTIVE IOT

The most basic step in designing EMI resilient systems, is being aware that EMI exists and that it can and will cause failures when no protective measures are taken. At all appropriate steps in the system's life-cycle, the following should be considered as a result of EMI-induced failures: operation, no operation and faulty operation.

Automotive vehicles and their systems must comply with a large number of standards for a large number of systems. It would be unpractical to list all the standards here in this paper, so a selection has been made and grouped in categories according to systems or phenomena.

A. Functional Safety Standards

These standards hand methods to engineers to create safety-critical or mission-critical systems, which can harm people or the environment upon failure. The proposed methods help ensure that no safety-goal is violated at any stage of the system's life-cycle. For automotive applications, the ISO 26262 [14] standard is widely used. The standard itself does not impose any performance requirements on the system. However, it pushes the design to implement safety and control functions to keep or bring the system into a safe state. Note that functional safety standards only refer to EMI as one of the possible failures.

They leave it up to the expertise of the engineer to know what to do. Therefore, automotive EMC standards are used.

B. Automotive EMC standards.

In the electromagnetic environment, two major fields are studied. The first is the electromagnetic emissions. No electric or electronic device should exceed a certain predefined level of radiation. Secondly, electromagnetic susceptibility is tested and assessed. The combination of those two fields should result in an EMI-immune system. So why isn't EMC engineering sufficient? First of all, the EMC standards are testing-based. For each emission or immunity test, a new device is used, a so called "virgin" device. As mentioned, functional safety requires the device to remain immune to EMI at all stages of the system's life-cycle, even if it incurred earlier EMI events. Furthermore, the system needs to operate at a confidence level of 99.99% or higher. Since electronic systems, especially the ECUs considered here, are non-linear, the testing of a subset of the system and its environment, is insufficient in proving conformance for the other part. Since at this point, every combination of EMI, state of the device and specific foreseeable failure should be tested, this is called "Exploding EMC Test Plan" [15]. Lastly, EMC testing is not included in the design. In other words, the product is developed first, and then the testing phase begins. When vulnerabilities are discovered, the cycle is restarted. This means, that neither functional safety, nor EMC engineering can provide a solid answer to EMI.

C. Communication standards.

In an interconnected system, communication is one of the main aspects to consider. It is imperative that the protocol used for the communication, is one-sided and unbiased, such as LIN and CAN mentioned in Section II.A. Next to the sensors and ECUs, EMI can also corrupt the message being send on the (IoT) network. In order to detect errors induced during transmission, an error detection method must be used. A widely used error detection method is using a Cyclic Redundancy Check. CRC adds extra information to the sent data, based on the data itself. At the receiver, errors can be detected by evaluating the received data and the extra information. The effectiveness of CRC under harsh EMI disturbances has been studied in [16]. The authors found that up to 50% of false positives, wrong data received but no error detected, remain possible when CRC has been implemented.

VI. CONCLUSION

EMI is quickly gaining more and more importance as a contribution factor to failures. For safety- or mission-critical systems, the failures might result in loss of revenue, environmental damage or even injuries to people. It is therefore essential to make those systems as robust as possible against EMI.

This paper presented the IoT in light of critical automotive systems, whereby both intra- and inter-vehicle networks were considered. The communication which make up the networks are susceptible to the interference, having the possibility to result in dangerous situations. As an example of automotive IoT and its implementation, the Adaptive Cruise Control was considered. In the end, robust design and compliance appropriate standards are required to keep cars, and its occupants, safe.

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Implementation of Internet of Things based Solution of Universal Power Transducer

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Abstract – **The paper presents a smart power transducer implementation as IoT based solution. The essentials of IoT concept are outlined. The possibilities for application of cloud computing in the electric power system management are discussed. The block diagram of a smart transducer with extended network capabilities is described. The remote user interface is shown.**

Keywords – **Internet of Things, Cloud computing, Smart metering, SCADA**

I. Introduction

Like most of the new concepts, especially in the technical field, Internet of Things has originated at the Massachusetts Institute of Technology (MIT) in the beginning of the 21st century [1]. It is considered not as a brand new process but as an evolutionary one which development has been in progress. The main goal of Internet of Things is to create smart environments for application in different areas of the industry and social life like e-government, e-learning, e-health, e-business, smart homes, smart cities and etc. A significant impact on the evolution of IoT has been given by the strong progress of electronics, computing and telecommunications. On one hand the people have become able to interact with the surrounding world by use of variety of sensors and actuators. In the same time mobile and wearable computing give them the possibility to be connected anywhere and to consume services at any time [2]. The Internet of Things concept represents the integration of various devices like sensors, actuators and etc. to Internet. The term "thing" is related to people, machines, devices, sensors and data [3]. Nowadays the research trends which concern the field of the pervasive and ubiquitous computing consider IoT as the interconnection between things-embedded computing devices and the existing Internet and web infrastructure. Hence, IoT will be able to offer the users improved connectivity of devices, systems, and services in a way that advances machine-to-machine (M2M) communications, and that stimulates the integration of things not only to the Internet (the network), but also to the web (application layer), allowing the development of things-oriented and service-based applications built upon a large number of networked physical elements [4].

There are a lot of definitions for Internet of Things but they have many common points:

- the ubiquitous nature of connectivity;
- the global identification of every thing;
- the ability of each thing to send and receive data across the Internet or across the private network they are connected into [3].

This paper is organized as follows: section 2 presents the essentials of the Internet of Things. The application of the cloud computing and the probable benefits of the introduction of network-based control in the power system are considered in section 3. The IoT based solution of a smart power transducer and the remote interface are described in section 4. The conclusions and the future work are presented in the last section.

II. IoT Concept Essentials

Two basic acts have enabled the IoT development – the first is to define open standards for communication, and the second is to map the traditional IP-based Internet stack to the IoT. The successful communication model of the Web is regarded as a base for the IoT. The idea of an IP-based IoT has been discussed for years and is realized now. The use of the IP protocol for smart object addressing and data exchange will allow the full interoperability and integration of IoT with the existing Internet. The deployment of two important achievements - IPv6 and Cloud computing, has given a significant impact on the fast development of the Internet of Things. IPv6 gives the possibility to assign a communications address to billions of devices. In addition, it makes the management of networks easier because of the auto configuration capabilities and also offers improved security features. Cisco IBSG predicts that there will be 50 billion devices connected to the Internet by 2020 [1]. Cloud computing is already a building block of the Internet and it is expected that the Internet of Things will be the biggest user of Cloud. The IoT applications are comprised of many detectors and services to manage them and are very dynamic, processing data with rapidly changing volumes and rates. Clouds provide a flexible facility to manage this variability. Certainly a Cloud environment can also provide the services for analysis of the data streams often associated with synchronous simulation to support providing the information to the end consumer in an optimal form. The benefits for the business can be found in applications like environmental monitoring, healthcare monitoring and heavy industries monitoring where the high volumes and rates of data need rapid processing to information for perception. Cloud computing, mobile networks development, wearable and smart devices have

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let the wide expansion of IoT. The main features of this expansion are:

• the cloud has developed an infrastructure providing various services – information storage, communications, security, etc.;

• mobile networks have ensured ubiquitous connectivity;

• wearable and smart devices provide the user interface (and a gateway for some devices) to access, manage, and control the things.

• the Internet means this new infrastructure is accessible anywhere and at any time.

The result of the expansion is the incredible increase of the amount of data available for processing. This, together with the ability of Internet to exchange this data, will allow people to improve the services in most of the fields even further.

The most common cases for the application of Internet of Things are:

• general remote monitoring and control;

• asset tracking;

• process control and automation;

• resource allocation and optimization;

• decision optimization [5].

The common requirements to all of the mentioned above cases include:

• presence of sensing nodes for data collection;

• presence of local embedded processing nodes;

• presence of connectivity nodes for cable and/or wireless communication;

• presence of software for enabling new classes of services;

• presence of remote embedded processing nodes;

• security of information across the signal path [5].

The Internet of Things architecture is organized in layers and it is used to abstract and automate the integration of objects, and to provide smart service solutions to applications. The systems architecture can be divided into three layers [6], perception, transportation, and application, as shown in Fig. 1. The perception layer is responsible for the recognition and control of field devices, and also for the collection of the data provided by these devices. The transportation layer provides the elements of the perception layer with ubiquitous network access.

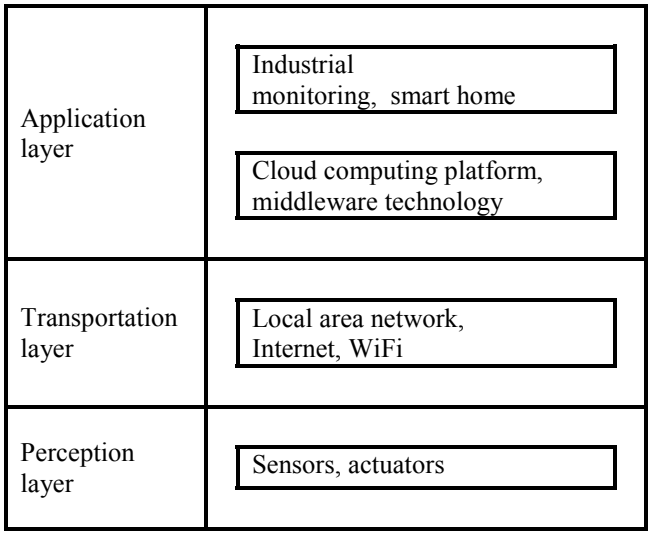


Fig. 1. IoT systems architecture

The application layer concerns the domains where IoT applications can be developed. It is responsible to support the services provision, and in the same time for the realization of intelligent computation and logical resources allocation also. High-level system layers, like the application layer, are comprised of IoT applications and a middleware system, which simplifies the development of applications by supporting services to cope with the interoperability requirement among heterogeneous devices [7].

Internet of Things also can be considered as a network of networks. The Internet is the physical layer or network which is composed of switches, routers, and other communication equipment. Its basic function is to ensure quick, reliable, and secure transport of information from one point to another. The Web itself is an application layer which operates on top of the Internet. Its primary responsibility is to provide an interface which makes usable the information that flows across the Internet [1]. Now it can be supposed that the IoT will be a network of heterogeneous, interconnected devices that will form the infrastructure for the so-called Web of Things (WoT) [2].

III. Expected Benefits from the Introduction of IoT and Cloud Computing in the Power System Control

The European Commission has set the Renewable Energy Directive, which establishes a common policy for the countries in the European Union (EU) for the promotion of renewable energy sources (RESs). The main goals are to achieve a 20% reduction in greenhouse gas emissions, 20% renewable energy consumption, and a 20% reduction in energy consumption by 2020 (compared to the levels in 1990).

This directive sets requirements to the consumers and utility suppliers to implement smart metering units to monitor the power consumption. The consumers will be forced to use the home appliances in low tariffs periods. Furthermore, the increasing availability and usage of smart devices in homes promises future integration in the Internet of Things of intelligent homes. This fact lets the residential electrical power systems to work in cooperation with smart devices in order to achieve smarter, more effective, more sustainable, and cleaner energy systems [8]. For the industrial consumers it is very important to plan the energy delivery quantities and periods of use aiming low prices. The implementation of IoT networks might contribute for significant energy savings. By collecting and monitoring consumption patterns, it is easier to adjust the electricity demand and generation, especially when using RESs such as PV and wind because their generation depends on the weather and it is difficult to be predicted.

In the beginning the Internet of Things networks implementation was intended to connect industrial equipment. Nowadays its application has been expanded to connect everything from industrial equipment to everyday objects. The range of items includes from gas turbines to automobiles to utility meters. The modern application of IoT networks for industrial and home automation means that every device can be connected to energy-management

system (EMS) and to provide information to the consumer. Consumers will be aware of their consumption, and, therefore, they can adjust their behavior to reduce the energy bills because a significant reduction in consumption can be achieved when the user is aware of the cost of the energy that is being consumed [9].

The complexity and the geographical distribution are two important characteristics of the electric power system. The energy-management system is responsible to assure sustainable, effective and safety operation. Increasing transmission capacity is essential to meet an increased demand of electricity, integration of renewable generation and etc. The first approach to satisfy the need for the most economical ways for transferring the bulk power along a desired path might be by building new transmission lines, but it is a long and expensive process. Alternately, to increase the available transfer capacity of the existing transmission lines with the introduction of a smart metering infrastructure including power flow controllers and development of IoT networks may contribute not only to the costs reduction but to the improved operation regarding the reliability and the sustainability. One of the important problems in this area is caused by the different equipment, devices and software from different suppliers which are installed. All these elements must be connected in a proper way so that the entire system can operate reliably. Another problem concerns the system functionality. The electric power system includes different levels (such as generation, transmission, distribution and consumption) and its proper structure can be seen in the way it assures interoperability of control functions on all its component levels. In the last years, new sensors and devices with Internet connectivity and abilities to provide real-time information and access have appeared. The importance of the topic is proved by many research articles in the technical literature which describe the benefits of a sensor-based distributed computing infrastructure [3].

The main requirements for the next-generation SCADA-based applications that can be intended for monitoring and control in the electric power system are [3]:

- real-time;
- scalability;
- connectivity – to allow sensors connectivity to enterprise IT systems;
- support for dynamic environments;
- security.

An Internet of Things oriented solution must take into account all these aspects. Also, it must ensure the autonomy of a various IoT objects and resources, such as sensors, smart devices, sensor networks, etc. Monitoring and control systems in the energy field use the following types of devices:

- dispersed devices – which are spread over a wide area;
- concentrated devices – which are close to each other (e.g. in substations).

These devices can be fixed or mobile. The fixed devices (being in fixed locations) might use cable or wireless Internet connection. The mobile devices can be wirelessly connected to the Internet (e.g., by mobile phone). When the thing itself is connected to the Internet, it is in active mode and is able to send real-time information to the IoT. By now, there are many devices and sensors which are used in the power system monitoring and control, which are not connected to the Internet. These devices could be connected as things to the Internet of Things in a passive mode through the concentrated devices (gateways or mediators) that support sub-networks and are connected to the Internet [10]. In the passive mode, a thing is not connected to the Internet, but can be uniquely identified through the gateway which maintains the network of smart units.

IV. IoT based Power Transducer Description

The block diagram of such transducer is shown in Fig. 2, and the view of the remote HMI – in Fig. 3. The structure is divided into two parts, namely Application processor and Communication processor. Both parts are developed using standard microcontrollers and the data transfer between them is serial using UART. This is a further development of a universal power transducer [11].

The Application processor accepts the input signals and it is connected to the grid by measuring transformers with ratios kV and kI. The main quantities of the three phase power grid – voltage, current, frequency and phase angles are measured, and the derivatives – apparent, active and reactive power, and power factor are calculated. The rated input values are 57,7 V and 5 A and they are standard for the measurement and control systems in the objects of the power grid – power plants, substations and etc.

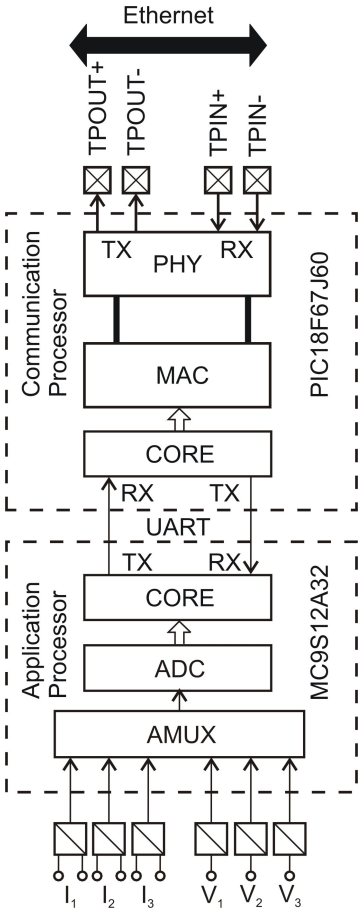
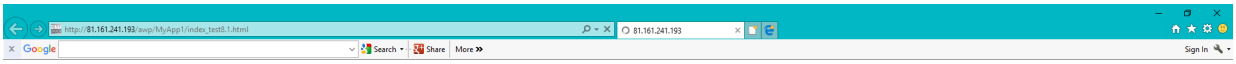


Fig. 2. Smart transducer block diagram



TRANSDUCER address = 43

V1 = **57.8 V**	fi_V1 = **0**	I1 = **1.001 A**	fi_I1 = **0**	P = **173.6 W**	f = **50.02 Hz**
V2 = **57.6 V**	fi_V2 = **241**	I2 = **1 A**	fi_I2 = **241.1**	Q = **0.8 VAr**	
V3 = **57.6 V**	fi_V3 = **121.1**	I3 = **1 A**	fi_I3 = **120.6**	S = **173.6019 VA**	
kV = **1100**		kI = **100**		cos_fi = **0.9999894**	

Fig. 3. Remote user interface

The inputs of the transducer have the flexibility to be adjusted to different rated values. For example the voltage dividers can be set for 230V and the transducer will be able for direct connection in industrial and home supply systems.

The communication processor is responsible for the networking applications and it supports the remote user interface. It is fully compatible with 10/100/1000Base-T Networks. The implementation of networking capabilities makes the transducer possible for inclusion in Internet of Things networks.

V. Conclusion

In this paper the main features of the IoT concept are explained. The expected benefits from the introduction of Internet of Things and Cloud computing are considered. The hardware and software design and possibilities of a smart transducer with extended networking capabilities are presented. The customers are able to access the developed remote HMI from anywhere in anytime using Standard Web browsers. The proposed transducer is intended for Internet based SCADA system development. Laboratory tests using power system simulator have been conducted. The presented results will be used in further investigation of more complex systems for electric power management.

Acknowledgements

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A practical implementation of smart home energy data storage and control application based on cloud services

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Abstract – **This paper presents the development and realization of distributed energy data storage and control application based on cloud technologies. The LAN is built by cloud connected devices and Olinuxino A20 single board computer. The developed application utilizes microservices based architecture which improves code maintenance, enables easier scalability and improves the reliability of the system. The implemented application presents three services: DeviceHive connector, Database and Schedule service. Each of them uses its own instance of a database for storing service related data. This approach enables the performing of local control over the demand response without using cloud control logic. The application is built using mostly open source software modules.**

Keywords – **Smart Homes, Home Energy Management Systems, Cloud-based Smart Homes, Microservices architecture.**

I. INTRODUCTION

The emergence of cloud technology greatly simplifies the creation and subsequently the expansion of infrastructure for communication between different devices and clients (users) in applications such as smart homes [1]. Consequently, some applications for Cloud-based Home Energy Management Systems (HEMS) have appeared where intelligent devices with hardware and software layers can monitor, control and provide feedback on a home‘s energy usage [2]. The main task in HEMS is the realization of Demand Response (DR) optimization programs by means of which to reduce peak loads at consumer-end and improve energy efficiency. The integration of HEMS in Smart Grid Management Systems (SGMS) expands the effect of DR in larger area (regions) [3]. Generally the development of these systems is based on hybrid cloud architecture. In order to increase the reliability, in case of temporary loss of connection, the information from HEMS is stored centralized in cloud environment and also decentralized on the side of the smart home devices. However, independently of the storing location, the information is required to be extracted and processed towards fulfilling any given needs. This approach further enables the performing of local control over the demand response without using cloud control logic.

This paper presents a practical implementation of an application for distributed smart home energy data storage and control [https://github.com/MihailLyaskov/HomeassistApp]. The main goal here is to continue the work done by M.Shopov [4], by developing an application which can perform the tasks of: cloud gateway for different appliances, local energy data storage and device control based on work schedules. This is achieved by using microservices based architecture, which enables: faster development, easier integration of new functionalities, scalability and reliability of the system.

II. SYSTEM INFRASTRUCTURE

In this chapter we will discuss the infrastructure needed to deploy and test the smart home energy data storage and control application. There are a couple of reasons for which DeviceHive [5] framework was chosen for building this system over other frameworks:

- It is an open source project, which can be further extended and developed.
- It can be hosted in privet and public clouds.
- It implements a M2M (Machine-to-Machine) type of communication protocol.
- Presents open source libraries for communication with the cloud server, which can be used on different devices and platforms.

The DeviceHive framework presents REST and WebSocket based application programmable interfaces (APIs) which are consumed by devices and clients in the system and enables them to communicate in real time. Both devices and clients use JWT (JSON Web Token) to authenticate in front of the server. The different type of appliances are grouped together into logical networks based on their location. Each appliance can authenticate as a device with DeviceHive cloud service directly by itself or with the help of a gateway. After authentication devices perform a registration or update by providing “Device Name” and ”NetworkID”. After that they can start polling for commands coming from DeviceHive server and send notifications about their status. On the other side client applications don’t need to to registration or update. They just authenticate with JWT and can start polling for device notifications, send commands and get information about the server.

A server running the DeviceHive framework is currently deployed in Technical University of Sofia, branch Plovdiv as a private sensor cloud infrastructure. Figure 1 shows the overall view of the implemented system. It consists of local area network containing cloud connected appliances and

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Olinoxino A20 [6], DeviceHive server and client applications.

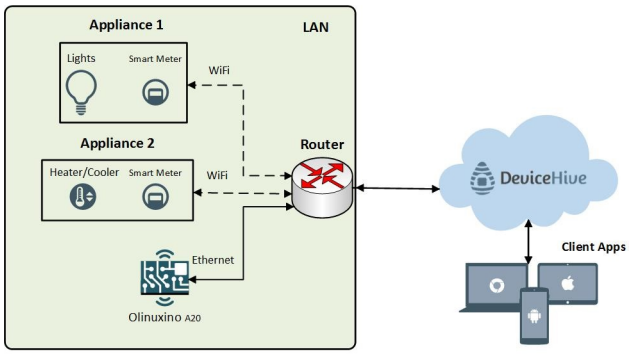

Fig. 1. The developed system infrastructure

Different appliances in LAN are connected to smart meters, which measure their electric power usage, calculate the consumed energy and send regular notifications to DeviceHive. Also they can receive commands and apply direct control over the appliances.

The smart home energy data storage and control application is being deployed on Olinuxino A20 single board computer. Olinuxino is running Armbian - Debian Jessie 8 build for Allwinner A20 SOC. The application uses DeviceHive REST API to communicate with the cloud server and uses JWT for authentication.

The last component in this infrastructure comprises the client applications. The current implementation of a client application is in a very basic state. It can plot time based graphics for consumed energy and can create working schedules for different devices using the services provided by the smart home energy data storage and control application.

III. Application Architecture

The presented application is written with JavaScript on NodeJS [9], which is an event-driven I/O server-side JS environment based on Google's V8 JavaScript engine. Because of its event-driven architecture NodeJS is capable of asynchronous I/O, which proves to be a good choice for real-time applications. By design NodeJS uses a single thread for execution and this could be considered as disadvantage to the system, but with the help of native child processes or JS modules like PM2(Process Manager) [10], many NodeJS processes can be started in parallel and can be monitored and controlled if needed. This led to the choice of using microservices architecture [11] for this application over standard monolithic architecture.

The usage of microservices over monolithic architecture brings some advantages on developing and maintaining such an application. Functionalities are grouped together to form services, which enables easier management over time and the possibility of easier and faster scaling of the application with new functionalities [12,13]. Each service can have its own database which helps in isolating data with different essence and assuring that if one database fails it will not affect the rest of the services. That also introduces a higher level of complexity when deploying the application and requires more memory. Different services can communicate with each other using inter-process communication (IPC), different publish/subscribe message buses or via REST APIs.

The application presents three services (Figure 2): DeviceHive connector, Database and Schedule service. Each of them uses its own instance of a database for storing service related data. They are interconnected by HTTP based IPC module SenecaJS [14]. Each service creates server on a specific port and opens client which can connect to services on other ports. Because of the small size of this application service discovery is not needed, so each client and server configuration is described in configuration file which all services have access to when initializing. SenecaJS provides pattern matching mechanism implemented in the bus driver for every service, so they can differentiate which messages are intended for them. Message patterns are being sent in JSON format and typically begin with service role, functionality and arguments. Each service uses its own database to save service related data. DeviceHive connector service and Schedule service use document-orientated database MongoDB to store respectively notification subscriptions and work schedules. The Database service is using InfluxDB, a time series database, to store power and energy consumption measurements sent from other devices.

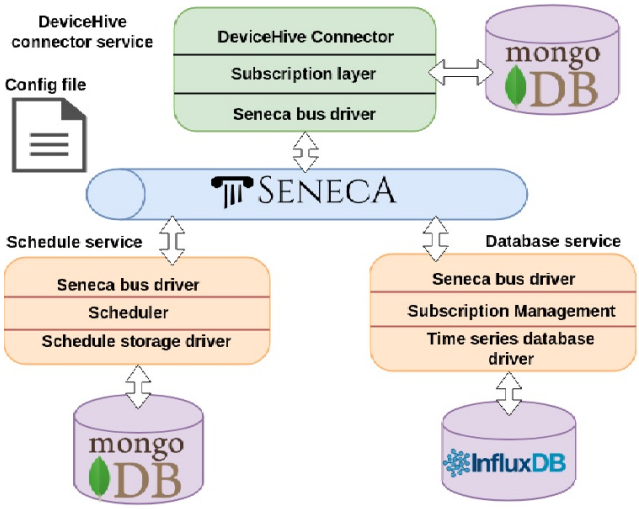

Fig. 2. The developed application architecture

The role of the DeviceHive connector service is to route commands between DeviceHive and the other application services. It registers the application as a device in DeviceHive framework and starts polling the server for commands. The incoming commands are mapped to command endpoints exposed by the other services from SenecaJS bus. The mapping is done in the configuration file. This service exposes its own endpoints on SenecaJS bus, which enables other services to: send commands to other devices, send and subscribe for notifications. Every time a new notification subscription is made, the connector starts polling the server for updates on this specific notification. The configuration of each subscription is saved to MongoDB database as a JSON object so it can be recreated after application restart. This persistent storage

ensures that the application will be able to restore its previous working subscriptions.

The supported functionalities by the schedule service are to: create daily schedules based on a JSON configuration, remove schedules and show all active schedules. On every new schedule the service subscribers, through DeviceHive connector, for notifications from the monitored device. The service uses a NodeJS module called “node-schedule”, which takes care of sending start and stop commands according to the working schedule. It also aggregates the consumed energy value from every notification and sends stop command if the device has reached the threshold energy value. All active schedules are stored in MongoDB database in order to be recreated after application restart or service failure.

Example schedule configuration:

```
{
      "DeviceID": "TestDevice",  // DeviceID
      "start": {              // DeviceHive command to turn
    on the device
          "command":"device/control",
          "parameters":{
            "state":"On"
          }
      },
      "stop": {                       // DeviceHive
    command to turn off the device
          "command":"device/control",
          "parameters":{
            "state":"Off"
           }
      },
      "schedule": [{                  // Array of start and
    stop times
          "beginTime": "13:00:00",
          "endTime": "14:00:00"
      }],
      "maxEnergy": 1500.0,          // Consumed energy
    threshold
      "notification": "device/init"   // Subscribe for this
    notification
  }
```

The database service supports the following functionalities: make notification, subscriptions through DeviceHive connector, remove notification subscriptions,
show all logged devices from database and present power and energy measurements from date to date. All the measurements are saved in a time series database (InfluxDB).

The usage of time series database gives some advantages over the standard relational databases. InfluxDB gives a less complex schema for storing and retrieving time series data. It also gives the possibility for extending the schema without affecting previously stored data. This database also presents two functionalities that give the chance to store data for bigger time intervals without exceeding the memory. They are called “continuous queries” and “retention policies”. The overall idea for using those functionalities is to down-sample the stored data. The continuous queries perform aggregation over the data and can produce one measurement per hour averaging the data from sixty measurements and store them in different database with no retention policy. The retention policies are used to describe for how long data can stay into the database before it is automatically deleted. In the end we can have a smaller database that can have high precision data (one measurement per minute) for the last 24 hours and lower precision but long term data for the last week, month or even a year.

IV. Testing the Application

There are two tests written, that exercise the schedule service and the database service. Both tests are can be found in the github repository for this project in directory /services/Devicehive/tests. The names of the tests are: integration TestDatabase.js and integration TestSchedulde.js. Both tests authenticate with DeviceHive, register a device named “TestDevice” and start sending commands to the application.

Pseudo code is used to represent the basic actions made by both tests.

```
START  integrationTestDatabase.js:
        Authenticate with JWT;
        Register “TestDevice”;
        Get test begin time;
        Send command “database/startLog” for
“TestDevice”;
        Send command “database/showSubs”;
        IF there is no a subscription for “TestDevice”:
                ERROR subscription not made;
                STOP TEST;
        ENDIF
        Send 3 notifications with power and energy from
“TestDevice”:
        Send command “database/stopLog” for
“TestDevice”;
                Send command “database/show Subs”;

        IF there is a subscription for “TestDevice”:
                ERROR subscription not removed;
                STOP TEST;
                ENDIF

                Get test end time;

                Send command “database/get Data” for
    “TestDevice” between begin and end time;

    TEST END


START  integration TestSchedule.js:
        Authenticate with JWT;
        Register “TestDevice”;
        Start polling for commands directed to
“TestDevice”;
        Send command “schedule/create” for
“TestDevice”  with 1 minute length and energy threshold
of 1500 W;
        Send command “schedule/show All”;
        IF there are no schedules:
                ERROR schedule not made;
                STOP TEST;
        ENDIF
```

Send notification from "TestDevice" with energy 1000W;
Send notification from "TestDevice" with energy 1000W;
IF "TestDevice" doesn't receive stop command:
ERROR energy threshold exceeded but application is not stopping "TestDevice";
STOP TEST;
ENDIF
Send command "schedule/remove" for "TestDevice";
Send command "schedule/show All";
IF there are schedules:
ERROR schedule not removed;
STOP TEST;
ENDIF
TEST END

IV. Conclusions And Future Work

The paper presents one practical implementation of distributed energy data storage and control application based on cloud technologies. It utilizes microservices based architecture which improves code maintenance and enables easier scalability of the system. The application is built using mostly open source software modules which makes it easier to run not only on embedded devices such as Olinuxino A20 but also in the cloud. In the future, this architecture will be added to a DeviceHive gateway and more services for connecting with appliances and devices will be provided. This will give the chance to control and monitor those devices even if cloud services go down or connection to WAN is not reachable.

V. Acknowledgements

The presented work is supported by National Science Fund of Bulgaria in the frame of the project "Investigation of methods and tools for application of cloud technologies in the measurement and control in the power system" under contract NSF E02/12 (http://dsnet.tu-plovdiv.bg/energy/).

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Increasing of the Number of the Controllable Axes Using TDM Mode of SPORT Interface Between DSP and FPGA

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Abstract – **The most of known technical solutions for multi-axis control are based on single processor architecture for particular number of axes according of the limited number of embedded PWM channels.**

The method of increasing of this number by using FPGA support of PWM and waveform generations is described in this paper. The interface between DSP processor-calculator and FPGA based PWM-generator are made by using of TDM mode of SPORT interface ordinary used only for audio applications.

Keywords – DSP**, FPGA, multi-axis control**

I. Introduction

The method of digital control of motor activate mechanical axes in most realization is based on singled processor architecture for single axes.

The main tasks of the embedded microprocessor or microcontroller or DSP (Digital Signal Processor) in digital control device can be summarized as: signal generation, data acquisition, control algorithm calculation and data communication.

In case of need of multiple axes control there are two main methods:

- single processor architecture based on more powerful microprocessor (microcontroller) or DSP;
- multi-processor architecture based on microprocessor or DSP.

The availability of free-in-user programmable, high speed digital devices such as FPGA (Field Programmable Gate Array) enable the other method of multiple axes control to be used.

The method of separate signal generation and data acquisition in FPGA device in one side and control algorithm calculation and data communication in DSP device in other side is described in this paper. In this method a multiple axis control algorithm calculation and data communication can be realized in single DSP. The number of FPGA devices will depend from number of axes and the logical capabilities of taken FPGA device.

A. Layout

The main tasks of embedded microprocessor, microcontroller or DSP in classical approach are:

- high speed PWM generation for 3-phase power inverter;
- sin-wave 3-phase numeric law generation for sin-waves in 120 degrees distance between phases;
- speed and position encoder support for speed and position feedback using PID and other sophisticated floating point calculation in real-time;
- set of communication protocols and tasks according particular use.

The basic scheme for proposed approach is shown on Fig.1. The different programmable digital devices DSP and FPGA with different tasks can be seen easy.

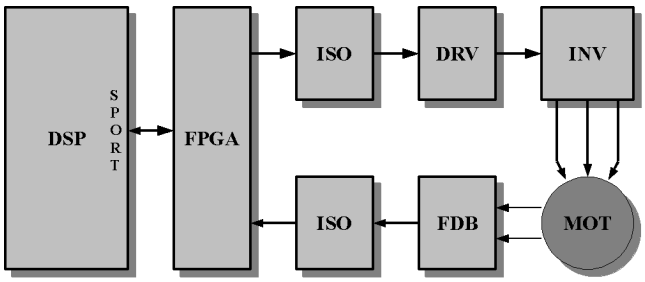

Fig.1. Basic scheme of the DSP-FPGA approach for Motor Control Solutions

The tasks of each part of this method are:

For DSP: PID and other sophisticated floating point calculation in real-time tasks, communication protocols and particular application tasks,

For FPGA: High speed PWM generation for 3-phase power inverter for each axis, sin-wave 3-phase numeric law generation for sin-waves in 120 degrees distance between phases for each axis independently, speed and position encoder support for speed and position feedback.

The common task for both device is to support high-speed data transfer in real-time mode of the control process of the axis. The success of shown method depend from reliability and functionality of interface and protocols for real-time data exchange between two main parts on this architecture DSP and FPGA.

B. Discovery of TDM mode

The Time Division Multiplexed (TDM) [1] mode of data exchange is one of the most useful method for data transfer

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between single (or multiple) Masters and many Slaves. Fig.2. shows the interconnections between two devices over Serial Port interface (SPORT).

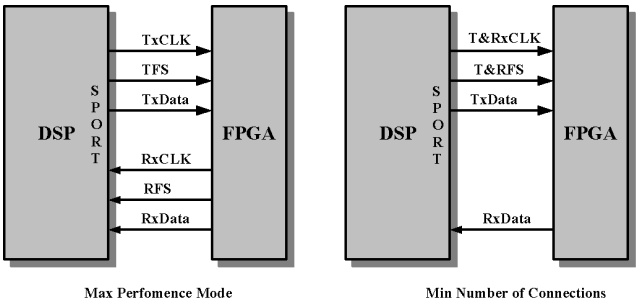

Fig.2. SPORT connections in max performance and min connections modes.

The main features of SPORT interface are:
- synchronous method of data transfer and synchronization;
- one-period-width Start-of-the-Frame signal (Frame Synchronization - FS) for all Slaves;
- Master device generates and Slave devices accepts clock and frame synchronization signals;
- Maximum performance mode using six connections and min numbers of connections mode using four wires-common connections for CLK and FS for receive and transceiver directions.

The TDM method add more properties. The Fig.3. shows the data structure inside of each frame according TDM mode over SPORT interface.

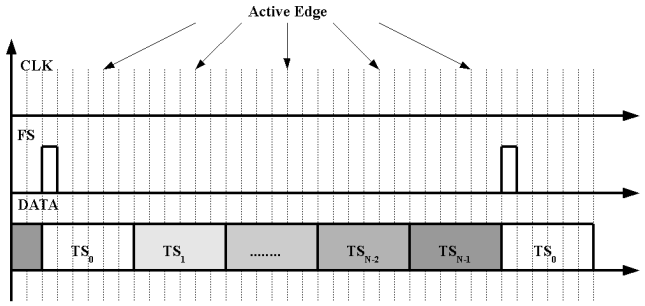

Fig.3. The Internal Structure of TDM Method for Data Transfer

The main features are:
-multi-slave architecture - this is variant of common bus architecture for data transfer over single data wire in given direction;
- byte, 16-bit word or any other data width can be used for data transfer in given TDM realization as a single data portion named Time Slot (TS);
- every particular Slave device can accept every TS but can send data in unique TS according unique Time-slot-number (TSN);
- the length in bits of TDM frame on can be calculate by multiplication of TS-width and number of Slave devices (number of unique TSN).

At now, the main using of TDM mode is in Automatic Digital Exchanges, GSM networks and audio data transfer interface between DSP Serial Port (SPORT) and audio codec.

The additional benefit of using of TDM mode of SPORT in DSP is embedded Direct Memory Access (DMA) between SPORT of DSP in TDM mode and internal of DSP memory. The data to and from this port in this mode are exchanged to and from internal DSP memory with minimal software support.

For most of the DSP devices the maximum of number of time slots in TDM mode are limited to the value of 128. This great feature is ideal for using for data transfer between DSP and FPGA for multiple axis control systems. The additional advantages in case of this are:
- real-time full duplex transfer without wait-states and handshake protocols;
- strict activation option for broadcast commands for multi axis applications.

C. Benefits of using a FPGA device

Using a FPGA as a Slave device in this setup is ideal because of the superior adaptability and flexibility of the FPGA architecture [4]. By tasking the FPGA to work directly with the controlled axes, the DSP can be free from the responsibility to deal with motor specific feedbacks and control signal generation. These tasks are both very time consuming and pin dependent which makes the act of choosing the particular DSP or processor a very difficult task. By allocating these duties to the FPGA, it is allowed the DSP processor to dedicate its' time to algorithm calculations. This separation of responsibilities allows to pick a DSP not based on its interfaces or signal generating capabilities, but based on its computational strength (which is the main strength of the DSP processors). The main advantages of the FPGA devices are:
- the ability to adapt to any motor feedback (hall sensors, quadrature encoder, absolute encoder)
- customizable signal generation (PWM width, PWM frequency, dead time duration)
- fit multiple axes drivers into a single device or implement each axis into a different device (based on the needs of the current situation)
- SPORT interface driver is device independent (does not rely on device specific primitives).

Additionally the FPGA chip can control other devices except motors (such as relays, ADCs, external brakes) which are board-specific for the current slave. This makes the design of the hardware much simpler since we can connect differently designed slave boards to a pre-existing master board without the need to alter it.

D. Custom board specifications

For the testing of the proposed method, a circuit board is made that implements the desired control hierarchy (Fig.4)

The main component parts of this board are:
- FPGA- XC3S50A- Spartan3A [2];
- ADSP BF-592 - lowest cost fixed-point DSP from Blackfin family [1],[3];

The only connection between the two devices is the SPORT interface. There aren't any specific pin requirements from the FPGA side except that, the interface clock signal (RSCLK) needs to be fed into a global clock input pin (for better signal processing). Connectors for the PWM control signals and motor feedback are provided. A connector to the UART interface of the Blackfin processor is also present to facilitate a user control interface to the system. There are no speed requirements for this particular connection due to it being only used to pass time-irrelevant information.

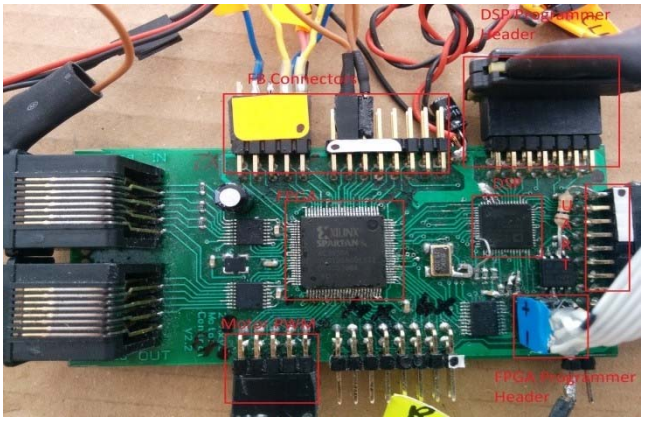

Fig.4. Custom DSP-FPGA board

E. Results

By implementing a custom SPORT driver into the FPGA, can complete the connection between the Master and Slave devices. On Fig.5 is presented a typical data exchange. It is evident from it that the FPGA is capable of conforming to the SPORT interface timing requirements.

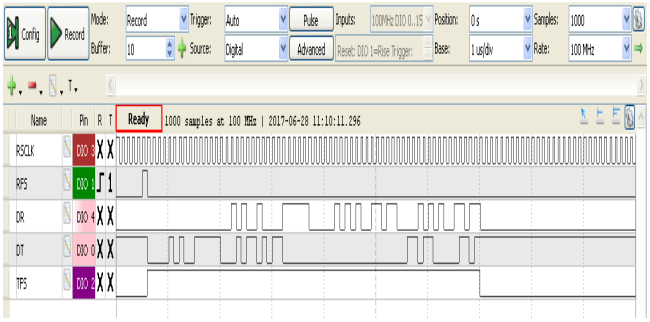

Fig.5. Real-time waveform from SPORT data transfer in TDM mode

The specific interface parameters used are:
- word length - 32 bits
- FS period - 1ms or 500us
- frame length - 128 TDM channels maximum
- frequency of R&TCLK - 10 MHz
- active TX TS channels - 2
- active RX TS channels - 2
- multi-frame delay - 1 period of CLK
- total TDM bits for single axes - 64 bits
- total time-by-period for single axes - 6.4usec
- total additional axes for current TDM - 63

Total view of the custom board is shown on Fig.6.

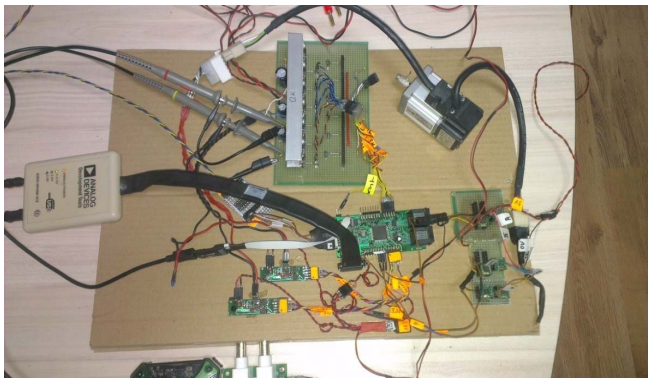

Fig.6. Total view of the custom board include power inverter for single axes

The data exchange between DSP and FPGA contains motion data necessary for the generation of six PWM signals – two for each phase of the test motor.

The parameters used for the waveform generator module are:

- period - 36605 kHz
- width – 12 bit
- duty cycle – sine modulated
- dead time – 120 ns

As a result of these configurations we can observe the following waveforms:

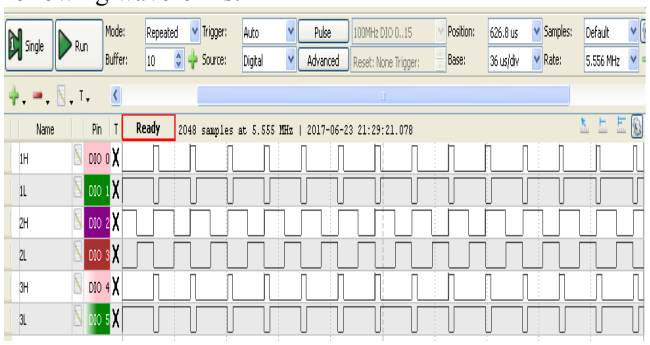

Fig.7. Waveform of the PWM signals from FPGA

II. Conclusion

The proposed method can be used for controlling a large number of axes using only one DSP as a central processing unit. This is enabled by the use of a FPGA chips for waveform synthesis, feedback generation, in-out and more functions.

This solution can be implemented on all different FPGA parts of the same or different vendor and all SHARC and Blackfin DSP devices on Analog Devices company.

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IoT-GSM-Based High-Efficiency LED Street Light Control System (IoT-SLCS)

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Abstract – **Today, population density shifts towards urban centers have resulted in the constant rise of energy consumption in cities. Due to the cost and technical restrictions of strengthening the infrastructure at the same rate, alternative energy sources must be sought in order to meet these increased energy demands. This study presents a street lighting system which consumes minimum energy from the city network by using solar energy to charge the battery during the day. This intelligent charging system will increase battery life and store solar energy. During the night, the battery is used for illumination until it is depleted, and only then is the energy from the city network used. Moreover, with the development of TCP/IP communication with centralized software on the cloud via GSM, the high-efficiency LED lighting is managed and monitored according to the level of daylight and the volume of traffic detected. Thus, with this system, a lead-free environment, lower CO_2 emissions and energy savings can be achieved.**

Keywords – **Wireless street lighting, GSM-based TCP/IP**

I. INTRODUCTION

The aim of long-life street lighting for the smart cities of today necessitates the management and monitoring of a LED-based system. Depending on the light level, street lighting is more easily provided by LEDs, which are available in a wide supply range. In this study, 12 VDC LEDs and 2 × 20 Ah batteries were charged during the day to provide illumination at night. The energy stored during charging was measured, ensuring that the battery level was used within safe limits. To this aim, an integrated hardware was designed with a GSM-based TCP/IP client socket that communicates with the writing on the cloud. By measuring energy consumption, the transition between the battery and the city network is controlled according to the traffic volume and the light level. In this system, an intelligent battery charging and management structure was designed using a Cortex-M3 processor, a GSM data module and a micro SD. It was designed to be cost effective and feasible since it did not require a PLC or any external hardware. Current limitation during battery charging, low charge/high charge checks and approximate battery health measurement were incorporated into the system. Even when the battery is depleted or there are interruptions in the city network, the electronic components of the system were designed to operate for seven days, reporting the traffic volume and light level to the cloud. The choice of which lamps to employ is determined via the cloud according to the intensity of the traffic and the level of light. The IoT Street Light Controller (IoT-SLC) communicates with the cloud software at 3-minute intervals via GSM. The GSM signal in Turkey covers 98% of the country.

Table 1 shows a comparison of different light sources and presents the advantages of LED-based lighting. Although the IoT-SLC was designed to allow for the collection of additional data such as rain gauge measurements of precipitation and rainfall, temperature, humidity, and so on, these will not be discussed in this study.

Much work is being done to develop cable and wireless street lighting. Some types are structured to use cables, some to communicate via fiber and others to perform automatic checks independent of one another. In this study, the assessment of traffic volume and meteorological data (such as fog conditions) is flexible because it operates via the cloud and an additional server is not required. If the scenario on the cloud changes, all IoT-SLCs are capable of changing their controls accordingly in the shortest possible time. This study focuses on the control and monitoring of solar battery levels via the cloud. Because of the increased number of manufacturers of LED street lamps, there are many different types on the market and so MPPT or LED light-control technologies are not addressed in this study.

TABLE 1. LIGHT TECHNOLOGY COMPARED

Light Technology	Average Lamp Life in Hours	Lumens per Watt	Considerations
Incandescent	1000-5000	11-15	Very inefficient, short lifetime
Mercury Vapor	12000-24000	13-48	Very inefficient, radiation and mercury
Metal Halide	10000-15000	60-100	High maintenance, UV radiation, mercury, lead

High Pressure Sodium	12000-24000	45-130	Contains mercury and lead
Low Pressure Sodium	10000-18000	80-180	Contains mercury and lead
Fluorescent	10000-20000	60-100	UV radiation, mercury, prone to break, non-directional light
Compact Fluorescent	12000-20000	50-72	Short life, mercury
Induction	60000-100000	70-90	Higher initial cost, lead, heat problems
LED	50000-100000	70-150	Relatively higher initial cost

The Environmental Security Technology Certification Program (ESTCP) and many manufacturers such as the ON Semiconductor Corporation have carried out detailed studies on price performance ratios and the advantages, disadvantages and depreciation of LED-based lighting. Findings of a few previous works on the topic have been summarized below.

[1] This study describes work on GSM-based energy-saving street lighting with On/Off/Dimming operating capabilities.
[2] Another study on high-power LEDs in street lighting. Low-cost, high-efficiency drivers for high-power LEDs of up to 144 W were discussed, and losses caused by soft-switching and diodes were demonstrated.
[3] This study was concerned with ZigBee-based illumination control and measurement and was aimed at high efficiency and energy saving.
[4] The researchers worked on lighting and controls depending on traffic volume via vehicular ad-hoc networks. The lighting was turned off when the street was empty. However, nowadays, with the population moving from the villages to the cities, the volume of city traffic is increasing daily.
[5] In the concept of the Smart City, WiMAX was applied to street lighting using ZigBee technology. The study cited areas where the GSM signal was inadequate.
[6] This study examined street lighting optimization and high-efficiency street lighting. Similarly, ZigBee mesh topology was used to measure and diagnose faults.
[7] The important role of light poles on energy consumption around the world was discussed. The daylight intensity was shown to be very important for energy savings.
[8] This work emphasized the advantages of the mesh topology provided by the ZigBee network.
[9] The researchers followed a slightly different path. By measuring the vehicle concentrations with sensors placed along the street, lighting control was provided depending on traffic volume.

II. IoT-SLCS METHOD AND SYSTEM

Figure 1 shows the overall structure of the IOT-SLCS system. The system consists of three main components: hardware, embedded software and cloud software

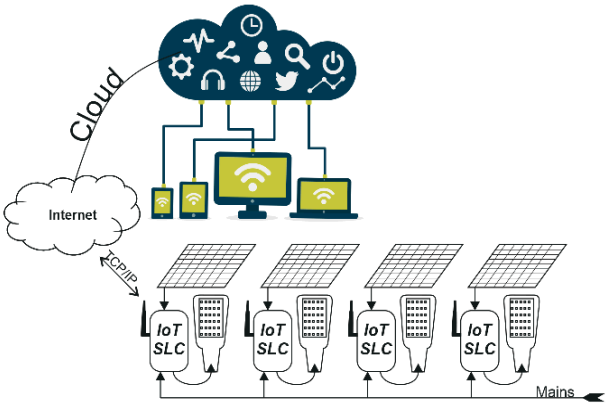

Fig. 1. IoT-SLCS overall system structure

A. Proposed IoT-SLC Hardware Structure

The light poles were equipped with 12-V LED lights with each light source drawing ~ 1.8 A current. In the IoT Street Light Controller hardware (IoT-SLC-H), two 12 V/20 Ah batteries were used for each light pole. These batteries were charged wirelessly, using a 5-W solar panel with a full power output voltage of 21 V. Both batteries were charged using a trickle charger unit containing an 8-bit processor operating independently of the Cortex-M3 processor in the IoT-SLC-H. This was necessary to save the battery when it dropped below 10.5 V during periods when the entire system was completely de-energized, thus enabling the battery to be monitored with minimal energy consumption. The 8-bit ATtiny841 processor was used for this by being wakened from sleep mode in order to complete the measurements. When wakened from sleep mode, it remained active for about 1 ms and then entered sleep mode again, while consuming less than 100 UA of current. Experimentally, when the voltage drops to 11V, all charging related units enter sleep mode. In this case, however, even if the battery operated for nearly one week, the voltage would not fall below 10.5 V. The detailed structure of the charge system designed in the architecture of IoT-SLC-H is shown in Figure 2.

The main processor in the IOT-SLC-H is the Cortex-M3, which performs all measurements and checks. The NXP LPC1769 microcontroller was used with the Cortex-M3 processor. The main processor controls TCP/IP socket communication, lighting and other traffic-related operations via GSM.

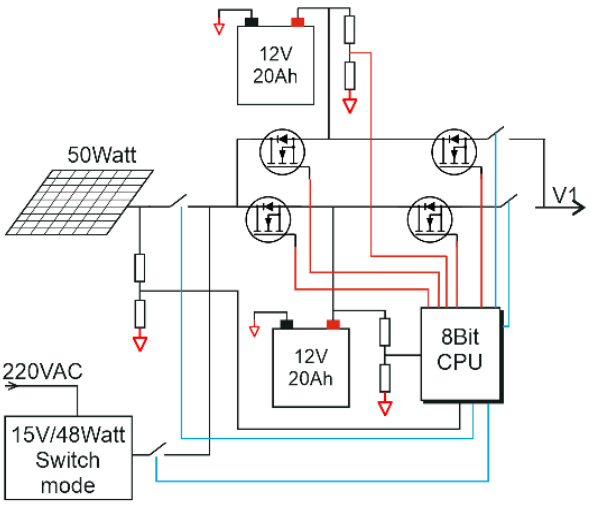

Fig. 2. Trickle charge with load controller

The architecture of the main IoT-SLC-H board is displayed in Figure 3. By driving the IR LED with 38 KHz at 50% duty, the IoT-SLC-H counted the vehicles in traffic from the reflected IR. Although there are many ways to count vehicles very precisely, IR measurement was sufficient for this work. The TSOP32438 IR receiver module was used as the IR detector. The DM009 radiation sensor was selected as the light, LDR and solar radiation sensor. The purpose here was to be able to follow the values of factors such as the falling of square meter energy under cloudy weather conditions using http://www.pvsyst.com. This made it possible to monitor the decrease in performance due to dirt or oil on the solar panel or other influences. Aspects of the dry contact input and output units will be developed in further studies.

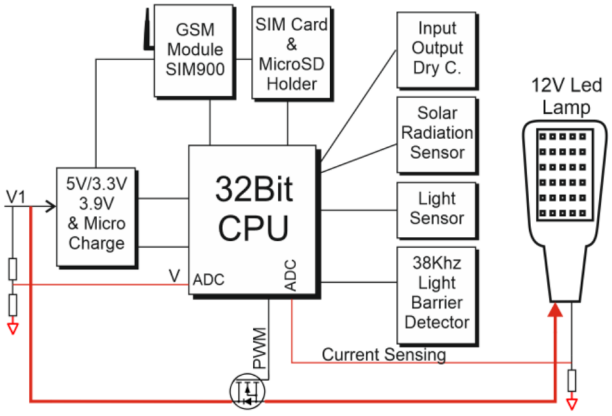

Fig. 3. Main hardware

The PCB design of the main board is illustrated in Figure 4 and the numbered components of the PCB artwork in the figure are listed in Table 2. Figure 5 shows the completed IoT-SLC-H hardware implementation, with a description of the numbered components provided in Table 3.

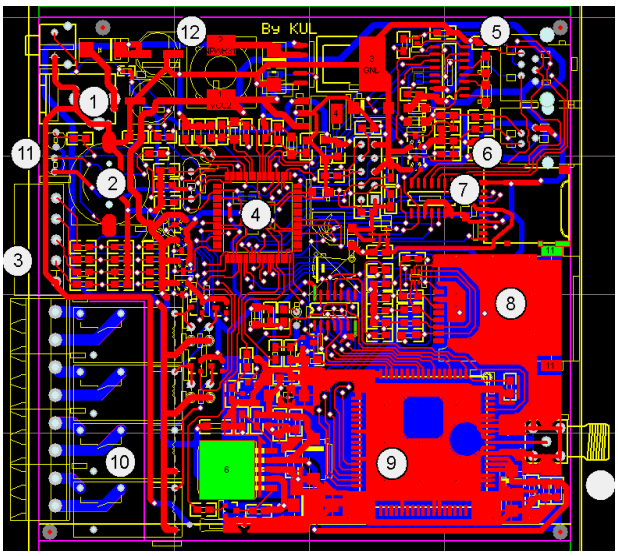

Fig. 4. Main board PCB artwork

TABLE 2. DESCRIPTION OF PCB ARTWORK

No.	Description
1	DC Power Input (V1)
2	RTC
3	Dry Contact Input (from Light Barrier)
4	LPC1769 32-Bit Cortex-M3
5	PWM Output for LED Block
6	Light and Solar Sensor
7	Micro SD Holder
8	SIM Card Holder
9	SIM900R GSM Module
10	Relay Output
11	GSM and Activity LEDs
12	Switch Mode power Supply and Micro Charge

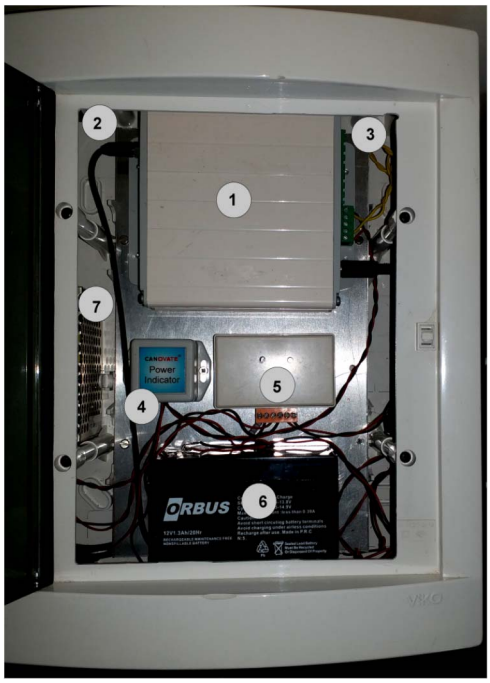

Fig. 5. Finalized IoT-SLC-H

TABLE 3. IoT-SLC-H COMPONENTS

No.	Description
1	IoT-SLC-H Main Board
2	GSM Antenna SMA Connector
3	Digital Inputs and Outputs
4	Main Power Failure Detection Module
5	Battery Charger with Load Controller
6	12 V/20 A Battery or 12V/3A Aux.battery
7	15 V/3.6 A Switch Mode Power Supply

B. IoT-SLC Software Structure

The IoT-SLC system was developed with software components that include embedded software and cloud software. Under the embedded software, sensor measurements (e.g., energy measurements and intensity levels of light) and GSM operations are carried out. The cloud software sets the entire lighting scenario and sends it to the IoT-SLC-H units.

Software algorithm optimizes brightness of the lights according to traffic density, solar energy level, light level that caused by car, sunset time of the light location. In addition, discussed algorithm is not only one light, but also optimizes all lights on a street. In addition, algorithm will be published in another study.

1. Embedded software

The ARM7 Cortex-M3 LPC1769 (LPC) processor used by the IoT-SLC-H is capable of handling the pulse counts coming from the TSOP32438 for the detection of daylight level, solar radiation level and traffic vehicle transit, the TCP/IP client socket communication via GSM, the PWM output for lighting and all other operations. A light source modulated at a 900 nm wavelength with 38 KHz at 50% duty placed on the other side of the street gives a numerical output filtered via the TSOP32438. The modulated IR light is needed to separate out the great amount of IR noise coming from the sun and from the surroundings. In this way an economical vehicle detection system was obtained. In addition, it was extremely easy to install because no under-the-street operations were required. The LPC connects to the cloud every three minutes via TCP / IP, during which time it sends on passing vehicle numbers, battery, solar panel and network status and sensor information. The cloud sends back the level of illumination to the IoT-SLC-Hs according to the information it received in the previous communications from all other IOT-SLC-Hs. Thanks to the RTC in the LPC, the IoT-SLC-H connections and updates are completed in a maximum of 100 ms-1s. The intensity on the GSM network affects the duration of the connection to the cloud, but this does not pose a problem for all the IoT-SLC-H installations along the street. With the lighting controls in software on the cloud, the whole system has got a flexible structure. The software on the cloud will allow a broader lighting strategy to be pursued if the IoT-SLC-H is deployed over a large area. The IoT-SLC-H system has been tested in the field for about two years and has been working continuously under the most extreme conditions. In Kayseri, light operating temperatures have been measured at between -20 °C (in winter) and 70 °C (in summer). However, at temperatures below -10 °C, the batteries are incapable of storing any energy and the charging time is prolonged. On the other hand, at high temperatures, there is a risk of fire. For this reason, the IoT-SLC-H is switched to the mains voltage during adverse conditions. Feed status, whether from the mains or battery, does not affect the operation of the system. However, the cloud software changes the lighting strategy according to the energy source used.

2. Cloud software

According to the information received from the IoT-SLC-H units, the software running on the cloud (IoT-CS) determines the lighting scenario for the entire street and manages the process of sending it to IoT-SLC-H units. The values required to save energy are experimental and new scenarios are defined on the cloud depending on many factors such as climatic conditions and traffic volume.

The IoT-SLC-H is connected to the cloud as a TCP / IP client socket. Through this process, the IoT-SLC-H response is transmitted over the port opened by the IoT-SLC-H units to the IoT-SLC-H unit providing the connection. The connection port opened on the cloud with the client socket connection is closed when data sending and receiving operations are completed. When the number of open ports on the cloud reaches high values in a short period of time, the processing power of the cloud software is greatly affected.

In addition, the client socket connectivity eliminates the need for a static IP and reduces costs. A packet size of 512 bytes was set and maintained for the IoT-SLC-H units. Thus, the information was sent on time in one packet and the communication time was kept short.

III. EXPERIMENTAL STUDIES

The experimental studies are ongoing and it was decided that the work to determine optimum values should be continued for another year. The energy saving with the cloud software, according to the current experimental data, is shown in Table 4. In order to achieve higher efficiency, the ability of the battery to store energy under difficult conditions must be enhanced.

TABLE 4. ENERGY SAVING WİTH CLOUD SOFTWARE

No.	Watt	Amp.	Lumens per Watt	Lumens	Working Time	Saving
1	22	1.8	150	3000	8	~50-66%
2	42	3.5	150	6000	8	52-68%

IV. CONCLUSION

The innovations brought about by technology have resulted in systems that are more economical, longer lasting and more energy efficient than traditional lighting. The price of an LED-based lighting system working with solar energy and the mains voltage at the same time was found to be less than 100 USD, excluding the cost of solar panels and batteries. The cost of a battery amounts to 30 USD, and a 50-Watt solar panel to 47-60 USD. The calculated battery life is accepted as four years. Assuming eight hours of working time during the night, the annual average costs and savings were calculated for battery run-time when charged with solar energy. These values vary according to climate and regional conditions. The system on the whole saves ~ 60%. In addition, maintenance costs are reduced with the provision of remote monitoring, control and energy consumption measurement. Software algorithm

This study has attempted to show the advantages of a smart street light control system and predicts increased application of this technology in the future.

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Energy Saving IoT-Based Advanced Load Limiter

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Abstract – **A load limiter is particularly needed in places like microgrid business centers because the load limit that the microgrid structure can handle must not be exceeded. This study aimed at keeping load variation under control by planning daytime load distribution using IoT-based energy measurement and central management software. By using IP-based smart meters and control methods to perform energy measurements, all loads on the microgrid can be loaded in a balanced manner from the centralized software. Moreover, load balance across the grid can be protected by shutting off the relevant overcurrent devices. By setting the load limits for certain zones at specific times of the day, both the electrical devices and the microgrid are safeguarded. In heating and cooling applications, when all components on the grid are overloading the microgrid, other electrical appliances are prevented from exceeding the permitted current limits. Thus, installation of the system results in energy saving and reduced costs. Details are shown in this study.**

Keywords – **IP-based smart sensors, smart energy, load limiter, microgrid, smart grid,**

I. INTRODUCTION

With the progress of technology a rapid increase in energy demands is emerging. When examining recent statistics, it can be seen that renewable energy sources will not be able to meet energy requirements. This has led us to seek new solutions to save our energy and energy resources from unnecessary consumption. A priority of this concerned research was to prevent unnecessary power consumption of home and office equipment. This led to the idea of a controllable socket and rapid development of these smart sockets has since begun and is ongoing. Furthermore, in order to reduce the microgrid installation costs in microgrid applications, it is necessary to keep the devices on or off at a certain time, so as to monitor the load consumption of electrical appliances online, and to load the system in a balanced manner to prevent overload. It is also necessary to determine total energy policies.

In this study, total energy consumption control was achieved by preventing devices from overloading in the workplace application. The devices were allowed to operate at different times by dividing them into time slots. The sleep mode of the devices was then detected and energy consumption completely eliminated. In addition, integrated energy management software was developed via cloud technology and in this way, energy management access was provided over the Internet.

A number of relevant studies carried out on the subject are briefly summarized here.

[1] Researchers demonstrated a grid structure that can be remotely controlled with real-time communication speed in a smart grid. This system is based on extensive optimization methods of the smart grid over existing network structures. Experimental results on measurement control via the smart grid with different communication protocols were emphasized.

[2] This study dealt with the detection on the grid of voltage, phase, and frequency faults beyond the specified tolerances, and also examined sector-based control methods.

[3] This work explored the use of technologies such as IoT, ZigBee and networking smart things in intelligent sensors and equipment and integration with their web services and cloud services, with emphasis on feasibility and energy savings.

[4] This research was concerned with algorithms and methods for energy measurement via CNP protocol, control of load distributions and automatic implementation of microgrid structures such as those of solar energy and wind energy.

[5] This work involved ZigBee protocol allowing remote energy measurement and control of home appliances. Access was provided via mobile phone using GSM.

[6] Researchers developed mathematical models by Linear Programming and indicated that in this way they had reduced energy consumption by 20% in the simulation model.

[7] This study reported the effects of the total daily consumption of electrical appliances, and emphasized that energy savings could be achieved by raising the awareness of the users.

[8] Efforts were made to further reduce stand-by energy consumption by combining ZigBee-based sensors with environmental monitoring, energy measurements and home automation systems.

[9] This study reported energy savings of ~ 7% as a result of planning the working times and priorities of electrical appliances.

[10] This study attempted to determine energy consumption profiles without a central server by developing intelligent sockets that communicated with each other in order to measure and control energy.

[11] Using ZigBee protocol, researchers developed smart sockets that could measure and control the energy of household

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electrical appliances by gaining access to smart home automation over the cloud. This work is similar to the present work, with a few important differences. The aim of the current study was to reduce energy consumption, especially in factories, business centers or places where local energy can be produced. For this reason, the energy management planning was based on offices or machines. In addition, the high-current and stand-by management, the conditions for the load to be active, and the timings were completely user determined.

[12] This study involved socket-based energy measurement and control and overload warning in smart home systems using Power Line Communication (PLC).

[13] This is another work on IoT-based energy measurement and management.

[14] Researchers presented information on increased energy requirements and traditional measurement methods. In addition, they demonstrated the overall advantages and disadvantages of increasing measurement and control strategies.

[15] This last work is about the provision of a wide range of management support, including centralized management support equipped with an IP-based power distribution unit having energy measurement and control capabilities and configured to eliminate stand-by energy consumption. It points out that savings can be achieved by eliminating stand-by energy consumption, especially in banks and public institutions.

In addition to high-current control and IoT-based energy measurement, the present study aimed to achieve greater energy saving by monitoring the very low stand-by currents. A total energy management plan with cloud integration can provide energy measurement and control and at the same time, achieve savings in business centers having a microgrid or a large amount of electrical equipment.

II. MATERIAL AND METHODS

Electrical appliances exhibit different energy consumption rates according to their different operating modes. The new generation devices using switch-mode power supplies display a sudden increase in high energy consumption when switched on. When a large number of devices with switch-mode power supplies on one network enter the circuit at the same time, this causes a very high current to be drawn on the mains. For this reason, it is necessary for these types of devices, which are located on a microgrid or on a local network, to switch in sequence. Devices with increased energy consumption in different modes will also cause high-current draw on the network when switching to high-current draw modes at the same time. When possible, these should be prevented from overloading the network by not working in these modes at the same time. Thus, in this work, each electric device was provided with an IoT-based energy measurement and control system and is controlled by centralized software via the cloud. Moreover, in this study, power limits and operating times and modes of each designed IoT device controlled by the cloud software are determined, measured and controlled. The IoT- energy meter and control (IoT-MC) measures the active, reactive, Cos-Fi and total energy consumption of each device, and the total energy consumption and energy profiles of the electrical devices on the system are measured and updated. This method could be used in the same way to determine user profiles.

In this study, overcurrent devices are controlled by central software and are prevented from consuming more power than specified for the time slots. When the overcurrent devices begin to draw more current than the specified limit, they are shut down by the system and in this way both the devices and the network are protected from overloading. In addition, in order to determine and eliminate the stand-by energy, the device is disconnected from the central software via the cloud. If the user wants to use a device in stand-by mode again, by using a mobile telephone or the internet to log into the cloud, it is possible to restart any device. Specifically, the use of these applications began in textile factories and microgrid business centers. The textile mills that use this system can calculate unit costs per meter of fabric produced by the factory.

In this study, the ADE7754 integration was used for energy measurements and the current transformer was used to accurately measure low currents, while the Hall-effect sensor was used for measuring high currents. The current transformer used for low currents was connected to one of the ADE7754 di / dt inputs. The Hall-effect sensor was connected to the di / dt input of the other phase input of the ADE7754. Although the ADE7754 energy recovery integration is a 3-phase energy meter, in this study a single phase was applied to two phase inputs. In this way, one made energy measurements of low currents, while the other phase input provided energy measurements of high currents.

In this study, the NXP1769 cortex-m3 32-bit processor having a built-in Ethernet interface was used. The overall structure of the system is shown in Figure 1.

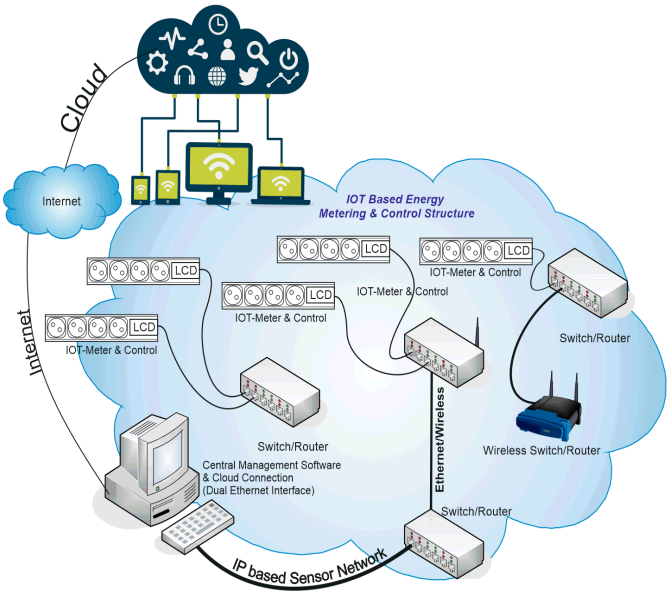

Fig. 1. Structure of IoT-based system

Figure 2 shows the hardware architecture of the designed IoT-MC unit.

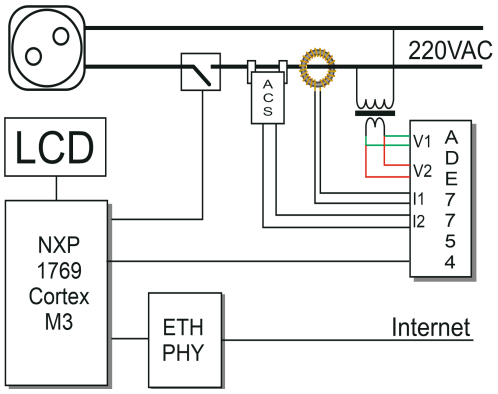

Fig. 2. Hardware design structure

III. Working Algorithm of the System

The NXP LPC1769 with an Ethernet layer was used as the main processor. The developed embedded software included Web server, SNMP, Email, Telnet, SMTP, 320 × 240 16 million color graphics LCD, and communication software with ADE7754. The central server has a dual Ethernet output. One of them continuously scans the IoT-MC network to gather energy metrics with the SNMP protocol and the other opens the TCP / IP socket on the other Ethernet output and sends it to the cloud. In this way, all energy measurements are updated on the cloud. The software on the cloud sends the necessary commands to the central server according to the current energy data. On / off operations are controlled by sending the commands from the cloud to the IoT-MC units on the local IP network via the central server. The software on the cloud manages the energy management policy required for the entire system architecture. The management console and all other user actions are implemented via the cloud. The software on the cloud governs the hierarchical organization of energy distribution, stand-by management, settings of current limits, and operations to be performed when the current limit is exceeded. In this way, energy management of the entire structure is ensured. When a computer is connected to the IoT-MC unit, a WOL protocol is added in order to send a power-on command over the network when the power is re-applied.

Energy calculations made with the ADE7754 integration are provided by a single processor. The IoT-MC consumes up to 0.8W / h of power when the computation and Ethernet protocols are active, and when inactive, they consume a maximum of 0.6W / h of energy.

In order to accurately measure low currents at the hardware level, the SCT-013-005 current transformer with a maximum measurement capacity of 8 A was used. This current transformer measures currents from 3 mA (~ 0.7 Watt) to -5 A with 0.2% measurement accuracy. This is enough to detect the minimum current required for all devices. Current measurements of up to 30 A were carried out by the ACS711. The ADE7754 integrates a three-phase energy measurement with a reference transformer to reduce mains voltage and provide isolation at the same time. The output of the reference transformer was applied to the two voltage inputs of the ADE7754. In this case, instead of three phases, one phase was measured. Since the ADE7754 requires calibration, a separate calibration sequence is required for the ACS711 and the current transformer during calibration. During calibration, one of the current inputs of the ADE7754 was calibrated by short-circuiting. The current sensors used are shown in Figures 3a and 3b.

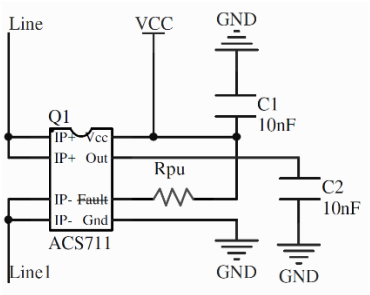

Fig. 3a. ACS711 current connection diagram

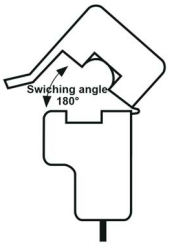

Fig. 3b. SCT-013-005 split core current transformer

The IoT-MC analyzes a sudden current surge as a transient current or continuous current of the other devices in the circuit. For this purpose, as seen in Figure 4, it waits for the surplus increase of the current to reach stability. If the rising current value is continuous, unlike peak current or an increase in current due to the input capacitance of the switching device, and the previously defined current limit has been exceeded, the energy consuming device is then turned off and the user is informed by the overcurrent warning via the web interface.

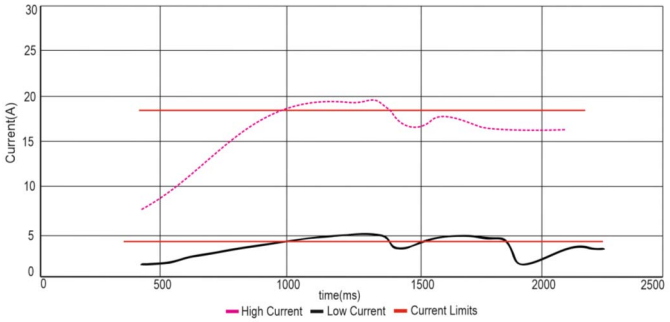

Fig. 4. Current on capacitive loading

Different current limits were set from the management console via the cloud for different times of the day. Accordingly, the software running on the cloud provided total energy management of load limits and energy consumption in other devices,

A part of the schematic belonging to the design is shown in Figure 5 and the PCB artwork is presented in Figure 6.

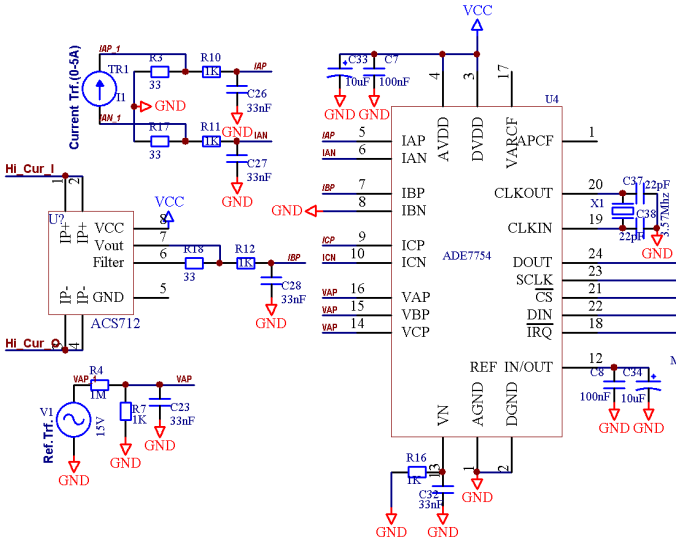

Fig. 5. Part of design schematic

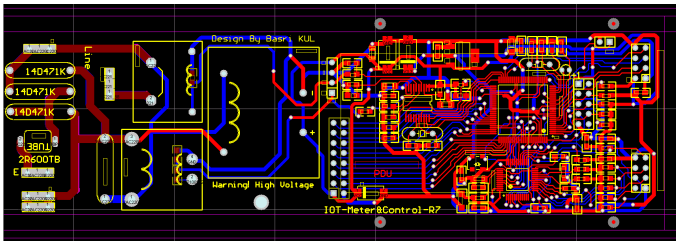

Fig. 6. PCB artwork

Figure 7 shows the application of the IoT-MC.

Fig. 7. Finalized IoT-MC

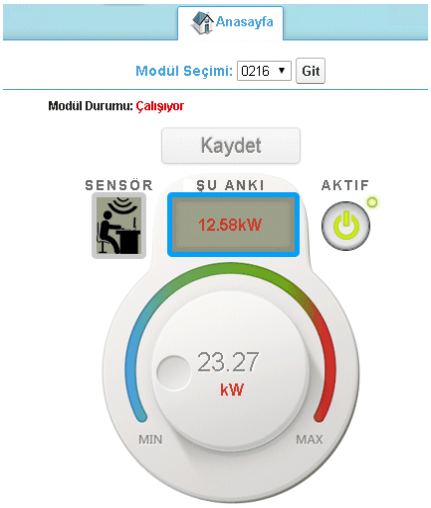

Fig. 8. Responsive web interface

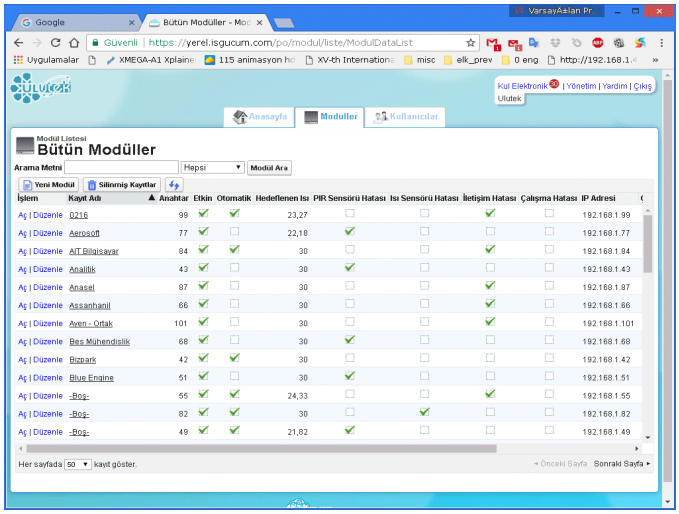

Fig. 9. Management console interface on cloud

As the flow diagram of the script running on the cloud is very extensive, only the screen output is shown in Figures 8 and 9.

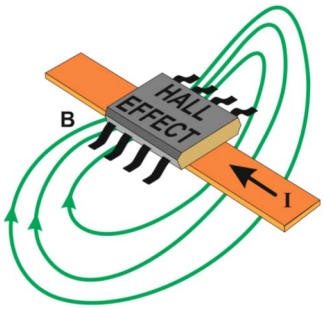

Fig. 10. Hall-effect current sensor implementation on bus bar

IV. EXPERIMENTAL STUDY

In this study, the Hall-effect and current transformer were combined to provide low-power stand-by detection, load limiting and total energy management at higher powers.

The central server scanned the IoT meter and control units on SNMP at approximately 100-ms intervals. It took about 100 ms for the central server to update the data in the cloud. Energy management was achieved with an average interval of 100 ms, and this speed was found to be sufficient to control the load balance.

In a construction with bus bar architecture, even when it is not possible to connect the Hall-effect sensor in series, as shown in Figure 10, a structure that can be placed on the bus bar is needed. The MLX91208 can be used for this purpose.

V. CONCLUSION

In this study, by measuring the energy consumption of 120 textile factory looms in inactive and activated states, the developed system was used to calculate the energy costs of the enterprise according to the product type. In addition, the study was able to determine the operations during which the reactive components of the machines were in effect.

A similar architecture previously developed by the authors [15], has been applied to a building within Uludag University in Bursa, Turkey. The end result of the application was a monthly energy saving of ~ 22%.

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Device for Measuring Parameters of the Meteorological Precipitation

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Abstract – **The operation principle of the optical device for determine the size and velocity of rain drops and measuring the level of meteorological precipitation is described. Cases of application of the slit-type diaphragm and arrays of photodiodes with defined parameters are shown. The design of the device and methods of processing signals to generate calibration coefficients used to determine the droplet size are described. The results of the laboratory tests of the device are presented.**

Keywords– **Meteorological precipitation, optoelectronics, data processing, measuring**

I. INTRODUCTION

An important task of meteorology is to determine the type of precipitation, their intensity and structure. Previously to present time, the rain gauge is used to determine the level of meteorological precipitation. Detailed information about the devices of this type is given in Wikipedia [1] and also in the scientific literature, various technical descriptions of devices and patents. However, modern meteorological station should be composed of instruments that provide accurate and timely information about all the basic parameters of the precipitation. The disdrometers [2] that is an instrument used to measure the drop size distribution and velocity of falling hydrometeors are used for this purpose.

A detailed literature review, the basic formula for calculation statistical parameters for the size distribution of raindrops and other useful information is given in literature [3] and in other works.

Disdrometers differ in principle of operation. One of the classes of disdrometers is optic disdrometer. Despite a wide range of industrial devices (such as [4-6]) until there are no cheap, reliable and efficient methods of solving the tasks. Therefore, the development of these devices is relevant in the present time.

II. BASIC PRINCIPLES OF OPERATION

The principle of operation of the device based on the determination of the parameters of particles crossing a light beam by pulse parameters of the photocurrent arising in the photo receiving device of special design. In the simplest case, that is either two of the sensor with a rectangular photosensitive areas, or a diaphragm with two light transmissive slits [7-8]. The principle of operation is illustrated by diagram shown in the Fig. 1.

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The movement of opaque particles (Fig. 1) is from top to bottom. The minimum value of the photocurrent is achieved at coincidence of center of the spherical particle with the longitudinal axis of the slit (point 2 and 4 in the Fig. 1), the maximum – in the case when the center of the particle coincides with the center between two slits (point 3 in the Fig. 1). The pulse shape of the photocurrent depends on the ratio of the geometric dimensions of the elements of the diaphragm and the diameter of the particles, and the particle velocity. Such pulse parameters as modulation depth and relative width according to the set levels do not depend on the velocity of the particle and can be used to determine the size of particles. If we are using one sensor for determining the speed of the particle is advisable to choose the pulse level 0.5 from the maximum value [9] and introduce a factor correcting the calculated speed value depending on the particle diameter. Transparent spherical particle, in particular a drop of water, is a short throw lens, so the distance of 5 or 10 diameters behind the transparent area is formed a shadow, almost corresponding to the shadow (diffraction pattern) of an opaque disk [7].

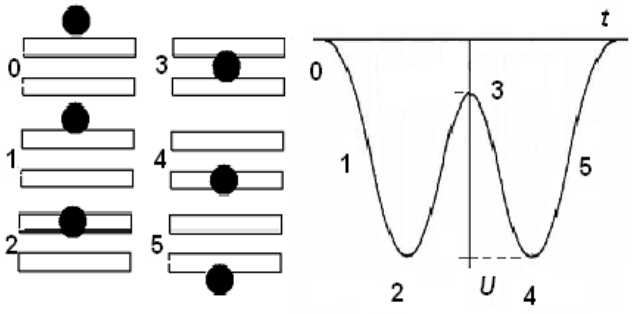

Fig. 1. Diagram explaining the principle of operation of the device: 0 – 5 – phase of motion of the particle relative to the photosensitive areas (marked by rectangles) and the corresponding part of the impulse

The diffraction pattern at a given distance from the particle and the pulse shape can be calculated by numerical methods, as for example in [8]. However, to take in account for the shape of the emitting area, aberration of the lens of the diode and of the collimating lens is a serious difficulty. Moreover, the calculation must be performed for a relatively wide range of wavelengths. So for this installation it is advisable to perform calibration for

particles of a given size, and then to determine the size of rain drops use the obtained calibration dependence.

III. EXPERIMENTAL SETUP

Structural diagram of the device is shown in the Fig. 2. The appearance of the entire device is presented in the Fig. 3. Light emission diode (LED) 1 is the source of optical radiation. LEDs of visible (ARPL-1W-EPL30, red, 630 nm) and infrared (ARPL-1W-EPL IR850, 850 nm) wavelength ranges were used in the device. Unlike a semiconductor laser, light of LEDs is not coherent, so in the receiver does not appear optical noise due to interference. Unit 2 supplies the current to the LED. The modulation frequency was chosen to be 455 kHz for ease of circuit solutions of filtering the signal with the photodetector, as well as to reduce the possible influence of extraneous signals. LED current can be adjusted from 0 to 300 mA. The unit 2 of the modulator is provided with a possibility of including the simulated pulse signal to verify operability of the device and estimate the parameters of the receiving path.

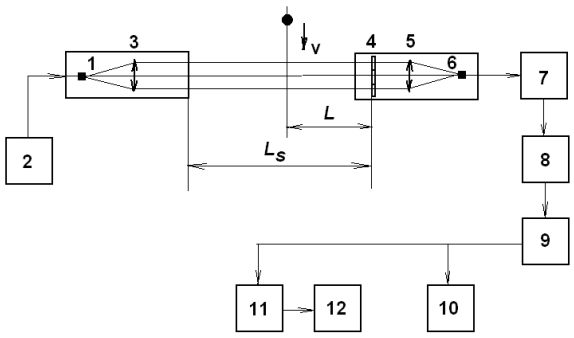

Fig. 2. Structural scheme of the experimental setup: 1 – lED, 2 – current modulator, 3 – collimating lens, 4 – slit type diaphragm 5 – focusing lens, 6 – photodetector, 7 – resonant amplifier of the photocurrent, 8 – detector, 9 – amplifier, 10 – microprocessor, 11 – ADC, 12 – personal computer.

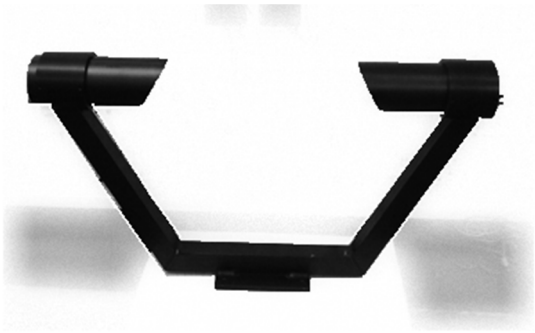

Fig. 3. Photograph of the device for measuring parameters of the meteorological precipitation

LED light was collimated by lens 3 into a parallel beam with the diameter of approximately 65 mm. The chosen focal length lens was 0.1 m. The input diaphragm 4 of photo receiver located at the distance of 0.5 m from the lens 3. The picture of the slit type diaphragm is shown in the Fig. 4a. Used diaphragm has two rectangular windows with dimensions 2x30 mm, located at the distance of 5 mm from each other. The optical radiation passed through the aperture 4 is focused to the photodetector 6 (type BPW34). LED with collimating lens, and the photodetector with the lens and the diaphragm were placed in the waterproof case.

In block 7, the signal of the photodetector is amplified and frequency filtering of the signal using ceramic filter Murata (CFULB455KC2A-B0) with bandwidth of ±12.5 kHz (6 dB) performed. Block 8 is the root mean square (RMS) detector, whose output was, formed the useful signal characterizing the parameters of the particle crossing the light beam, in particular, drops of rain or hail particles. Block 9 used to link the detector with microprocessor 10 and, if necessary, with the analog-to-digital converter (ADC) 11 designed to work with the personal computer 12. The use of a personal computer simplifies the process of calibrating and testing the device before commissioning.

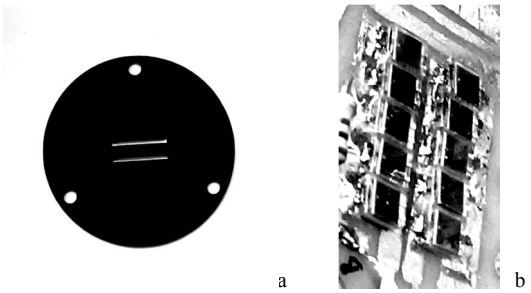

Fig. 4. Photos of the slit type diaphragm (a) and arrays of photodiodes (b).

Another embodiment of the device has two rows of photodetectors BPW34 (2x5) located at the distance 6 mm from each other (Fig. 3b). The side surfaces of the sensor were ground off for a tight mechanical contact with the aim of reducing the gap between the photosensitive areas. The approximate value of the obtained gap was 400 μm.

The presence of optical elements creates the specifics of the testing and determination of parameters of the electronic part of the device. The creation of the modulator of intensity of a LED radiation with a low harmonic distortion of optical power, taking into account the nonlinearity of the watt-ampere characteristics of the LEDs at low pumping significantly complicates the electronic circuit and increases its cost. However, even a significant nonlinearity of the radiation power of the LED relative to the pumping current has virtually no effect on the quality of the measuring device, since the average optical power of the emitter during operation remains constant and higher harmonics of the modulation frequency filter reduced to a level that does not affect measurement accuracy. Important is the linearity of the photodetector tract relative to the power of the optical signal, and the uniformity of sensitivity to the area of overlap of the particle in the window area on the input aperture. The specificity of this measurement is that the useful signal is formed of a relatively high constant level signal. In particular, when the nonlinearity caused by the saturation of the photodetector, the signal from particles even of small size will also are distorted.

The value of this type of nonlinear distortion depends on the size of the focused beam on the photosensitive area of

the photodiode. So the practical purpose of measuring of nonlinear distortions is interesting only for the assembled device. For these purposes, were produced two kinds of measurements: 1 – dependence of DC voltage at the detector output U_d on the area of the slits of the diaphragm 4 (Fig. 1) at the working level of the optical signal and 2 – dependence of the difference between half of the voltage U_d at the working diaphragm 4 and the voltage U_d at shaded one slit of the diaphragm 4 on U_d.

In the first case, part of the area of the slits of the diaphragm was covered by the opaque screen, which was moved along the slits. In the second case either the upper or the lower slit diaphragm was closed. In case of equality of the areas of the slits of the diaphragm in a linear system, the output voltage U_d at case of the one opened slit must be two times less than in the case of two open slits. The deviation from this ΔU_s dependence characterizes the nonlinearity of the opto-electronic system. For example, at the radiation power of the LED 300…500 mW non-linearity (ΔU_s) can approach up to 30%..50%.

The lower limit of the measured dimensions is determined by the diffraction-limited divergence and noise in the electro-optical system. The diffraction divergence can be reduced only by reducing the distance L (Fig. 2). The device with shorter length L_s should be used for this purpose. Improving the signal-to-noise ratio (SNR) can be achieved by the increase of the radiation power of the LED. However, the increase of power can lead to increased nonlinear distortion. Therefore it is necessary to find a compromise between the small value of the nonlinear distortion and high SNR value. It should also take in account that typically, increasing the operating power of the led is achieved by increasing the area of emitting area, and this leads to higher divergence of the radiation, and, perhaps, to disruption-to-one correspondence between the pulse parameters and the size of the particles.

We assume the useful signal is the maximum possible signal level, i.e. the amount of U_d. Experimentally, the magnitude of the U_d and the RMS noise were measured with the voltmeter. An example of the measured SNR at the wavelength of 630 nm at the operating power of LED when using the slit type diaphragm is shown in the Fig. 5.

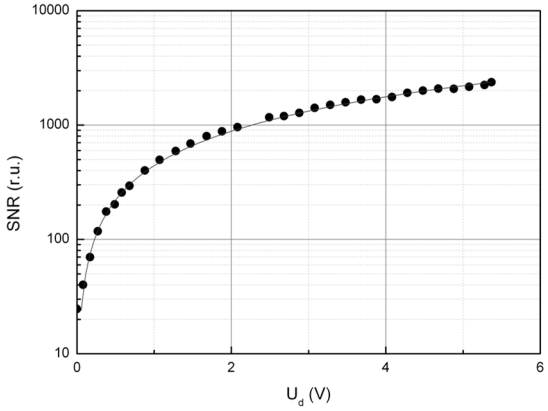

Fig. 5. Dependence of the signal-to-noise ratio on output voltage.

The dependence obtained differs from the classical one, is described for example in [10], may be due to the specificity of signal detection and characteristics of the used photodiode.

IV. DATA PROCESSING

The diameter of the particles and their speed can most accurately determine by optimization method at all points of the pulse, comparing the received pulse with the reference pulse shape from particles of different diameters. However, this method requires time-consuming calculations. Therefore, it cannot be used for microprocessors and personal computers to obtain results in real time. Therefore you need to choose a few characteristic points of the pulse and then use them to determine parameters of the particles.

In this paper, levels of 0.75, 0.5 and 0.25 of the maximum value of the inverted signal pulse were selected. The example of the pulse shape obtained at falling of calibrated ball with the diameter of 4.0 mm through the optical system of the described device and designation of the characteristic points are shown in Fig. 6.

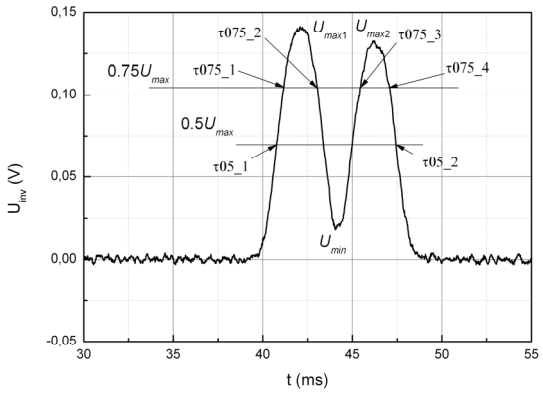

Fig. 6. Inverted pulse of voltage of the photocurrent for particles with the diameter of 4.0 мм (L=150 mm, λ=630 nm).

Following coefficients we used to calculate the size and velocity of particles in the first approximation:

$$k_{md}=((U_{max1}+U_{max2})/2-U_{min})/((U_{max1}+U_{max2})/2) \quad (1)$$

$$k_{075}=(\tau075\_3-\tau075\_2)/(\tau075\_4-\tau075\_1) \quad (2)$$

The coefficients k_{md}, k_{075} as well as some other factors for the calibrated beads was initially identified. Calibrating dependencies were created on the basis of the obtained data. Further, in the measurement process the mentioned above characteristic points of the pulse were searched by the microprocessor or personal compute; the coefficients k_{md}, k_{075} were found, the particle sizes were calculated using the calibrating dependencies. The volume of meteorological precipitation was calculated based on the drop volume (assuming spherical shape) and the cross-section square of the optical beam.

To determine the particle velocity in the first approximation used formula:

$$v=(2w_s+w_g)/(\tau05\_2-\tau05\_1) \quad (3)$$

where w_g – distance between slits of the diaphragm, w_s – width of slits; (for the array of photodiodes it is the distance between the photosensitive areas of the photodiodes plus width of two photodiodes).

Simultaneously measured values for size and velocity allow, in particular, improving the accuracy of meteorological measurements of precipitation, due to the exclusion of the pulses, not associated with rain or hail. If the velocity of the particles differs significantly from the theoretical values, typical for particles of this size, that dimension should be regarded as erroneous. Such errors can be caused by the intersection of the optical beam by flying insects, falling plant seeds and other causes.

The characteristic point related to the definition level 0.25 of the maximum value was used to refine the first approximation. When using two arrays of sensors the particle velocity is determined by the delay between pulses, so the use of clarifying refinements on the size of the particles is not required.

V. CALIBRATING AND TESTING

The simplest and most accurate way of determining the relationship of size of particle with the pulse parameters can be obtained by calibration. Pulses during movement of the calibrated balls diameter from 2 to 6 mm were obtained and processed. The characteristic parameters of the received pulses were obtained on the basis of which were created, in particular, dependences of k_{md}, k_{075} on the diameter. An example of dependencies for the case of using the slit type diaphragm is shown in Fig. 7. The coefficients k_{md}, k_{075} depend on the distance from the particle to the slit type diaphragm or the photosensitive elements of the photodetector. If this dependence is not taken into account, for this model, the measurement accuracy of the sizes will be from 5% to 10%. The instrument error of determining the size may increase to 15%...20% for particles with small diameter – 2.5 mm and less at the edges of the optical gap.

To increase the accuracy of measurements it is expedient to use the calibrating dependences for different distances L.

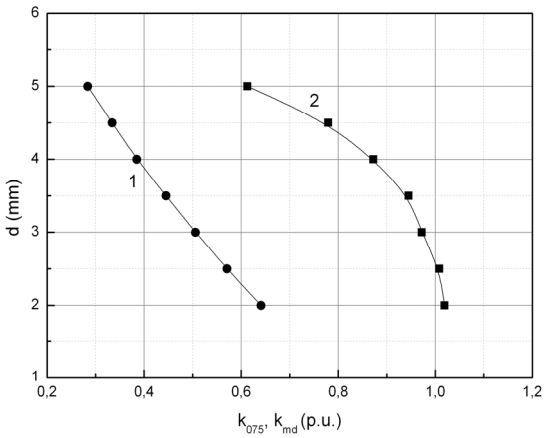

Fig. 7. The calibrating dependences for measuring the diameter of the particles: 1 – k_{075}, 2 – k_{md}.

When performing the calculations, first, the distance L should be estimated based on the pulse parameters, and then should use the appropriate calibration. The tests of operation of the device using calibrated beads of various sizes, the water droplets in the diameter range from 2 to 6 mm were carried out. Comparison of two different designs of the device was fulfilled on the basis of the conducted studies. Both designs showed the possibility of achieving the measurement precision of 5% and better. The results of the work are summarized in the conclusion.

VI. CONCLUSION

The developed design of the instrument is appropriated for measurement of sizes and velocities of rain and hail, as well for the level of meteorological precipitation.

The device uses a single photodetector, slit type diaphrarm and focusing lens has the following advantages: better uniformity of sensitivity relative to the place of intersection of the particle, ability to use of large modulation frequencies, less chance of splashing on the optical elements of the device in real operating conditions. The disadvantage of this type of devices: the large size and greater weight of the receiving side of the device, more complicated and less accurate algorithm to calculate the sizes and velocities of particles, the complexity of the accounting of particles crossing the window of the input aperture only partially.

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Realization and Testing of PC-based Power Quality Signal Generator

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Abstract – **The paper elaborates the design and evaluation aspects of power quality signal generator. The system is capable of reproducing the power quality (PQ) disturbances in accordance with European standard EN50160. The signal generator is divided in two functional parts: LabVIEW virtual instrumentation software, and hardware electronics for signal generation (data acquisition card and signal amplifier). By using the developed signal generator, a number of experimental test signals with various PQ disturbances typical for real power distribution systems are presented. The PQ analyzer Fluke 435 is used as the reference instrument suitable for measurement of PQ parameters from signal generator output. This paper summarizes the software architecture of the PQ generator, and some experimental results obtained with the reference instrument.**

Keywords – **Instrument testing, LabVIEW software, power amplifier, signal generator, virtual instrument**

I. INTRODUCTION

The increased concern for power quality (PQ) disturbances and problems, indicated in the recent years, basically is caused by limitations of natural energy resources for power production, including significant using of the renewable energy resources [1, 2]. Hence, PQ assurance became important and significant topic. In order to provide customer protection, optimal PQ level is defined according to relevant international standards. European standard EN50160 defines voltage characteristics in the public electrical power distribution systems, for normal operating conditions [3]. The required PQ level is determined by reference nominal values and acceptable limits of power quality parameters and typical network disturbances. Relevant data, necessary for proper PQ assessment, can be provided using measurement and software processing of power quality parameters at selected locations within the power distribution network.

Various instruments and equipment for measurement and software supported processing of standard PQ parameters are available in the market. Having in mind the challenges of the modern power distribution smart grids and great importance of PQ problems, special attention is paid to development of sophisticated measurement systems for PQ monitoring and analysis. Virtual instrumentation concept can be successfully implemented for realization of computer-based measurement systems. Various virtual instruments applied for PQ analysis, signal generation and parameter measurement have being published [4-10]. However, very important for the practical implementation of PQ generators is the signal amplification. In order to satisfy the specified level of the measurement accuracy, equipment for measurement of PQ parameters must be followed by appropriate metrological traceability chain. Reference instruments, voltage and current calibrators, are available in the various functional and constructive solutions. Such commercial instruments are relatively expensive and unavailable to the many researchers. Significant limitation of such instruments is closed functional architecture. Due to this limitation, such devices are not flexible and hardly adaptable to the specific requirements. On the other hand, the solution presented in this paper is easily adaptable to various practical requirements, such as: data logging, generation of random PQ sequence and upgrading some recently defined network disturbances [11]. The developed signal generator can be used as a source of reference signals for testing the instruments for measurement of power quality parameters, including various software supported algorithms for detection of standard PQ disturbances. This is PC-based solution, with LabVIEW software application, data acquisition card and power amplifier block. Detailed design and practical implementation of power amplifier are already described in the recently published scientific papers [12], [13]. Here in this paper is presented design of computer-based PQ signal generator and experimental procedure for verification of this signal generator, performed by professional instrumentation.

II. DESIGN OF COMPUTER-BASED POWER QUALITY SIGNAL GENERATOR

The hardware block configuration of the computer-based PQ signal generator is presented in the Fig. 1. The realized solution includes two functional segments. First segment is standard PC computer, supported with LabVIEW application software and data acquisition card NI PCIe 6343 [14]. Second segment of generator is power amplifier for amplification of acquisition card output voltage to the nominal power line level of 230 V. The power amplifier is analyzed in detail in [12], [13] and therefore its realization will not be discussed in this paper.

The virtual instrument developed in LabVIEW environment consists of a graphical user interface (front panel) and program code (block diagram). The basic purpose is generation of reference voltage signals with special functions for simulation of standard PQ disturbances [7, 8]. Generally, the virtual instrument enables generation of three-phase voltages but the realized

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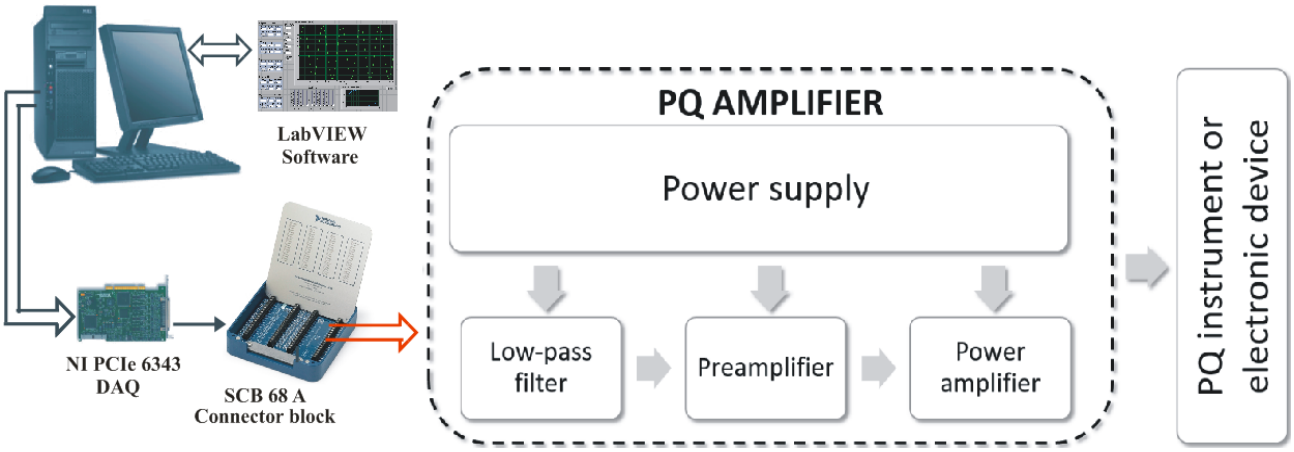

Fig. 1. Hardware block configuration of the computer-based PQ signal generator.

signal amplifier is developed for amplification of single-phase voltage waveform. However, this solution can be simply multiplied in symmetrical manner in order to simulate the three phase distribution systems. Some basic functions provided by virtual instrument for PQ signal generation are: definition of nominal signal amplitude and frequency values, definition of sample rate and duration of final test sequence, generation of Gaussian noise, variation of nominal signal frequency and slow amplitude fluctuations, slow signal amplitude variations with defined frequency of variation, definition of DC offset, voltage swell and voltage sag, definition of high-order signal harmonics with up to 50 individual harmonics, generation of some specific network disturbances (flicker, burst transients, short voltage oscillations). LabVIEW front panel of signal generator for presentation of undisturbed sinusoidal voltage waveform is given in the Fig. 2. Definition and simulation of voltage waveforms, with specified levels of standard PQ disturbances, can be performed directly inside the control panel and block diagram of virtual instrument. Each type of signal disturbances, for example voltage swell, voltage sag or high-order signal harmonics, can be defined and generated using separate segments. Disturbances can be combined and unified in the form of final complex sequence, according to the requirements of European power quality standard EN50160 [3].

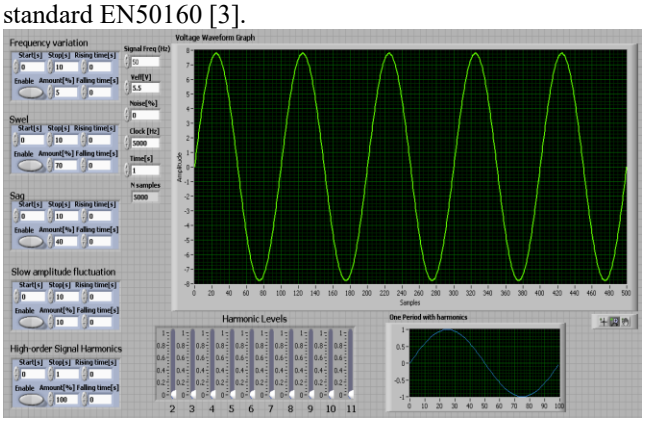

Fig. 2. Front panel of the LabVIEW-based PQ generator

The block-diagram of the virtual for PQ generator is given in Fig. 3 and Fig.4. The Fig. 3 represents the architecture of the system, whereas Fig. 4 contains the main sub-VI for disturbance generation.

The software part of the virtual instrument is organized in a state-machine program architecture. The program contains three states: initialize, generate and stop. In the initialize state, the virtual instruments performs hardware settings and initialization of the front panel controls and indicators. Afterwards, the program enters into the generate state for simulation and generation of the PQ signals. The main part of the generate state is the PQ generator sub-VI given in Fig.4 where the signals with the predefined settings are simulated. This sub-VI simulates the signals according the user control settings and outputs two waveform signals: signal with PQ disturbances, and signal with harmonics. After the signals are simulated, they are being physically reproduced by using the data acquisition card, and occasionally written into file if required by the user. To achieve optimal memory and speed performance, the signal is recorded into binary file, and the user settings are written into ASCII file format. The program enters the stop state on a user exit action or error occurrence when the program is being stopped and all communication ports closed.

III. Experimental Evaluation and Tests

The experimental setup for verification of realized computer-based signal generator is shown in the Fig. 5. The reference test of voltage signals are generated by the PC-based PQ signal generator and amplified with the power amplifier. Such signals have nominal power line voltage levels and they can be directly connected to the voltage inputs of a reference instrument PQ analyzer Fluke 435 [15]. All the time during the experiments the reference instrument is in a logging mode and records all PQ disturbances according the EN50160 standard. The communication between instrument Fluke 435 and computer is provided using the standard Universal Serial Bus (USB) communication interface and transferred to the computer by using a dedicated software tool.

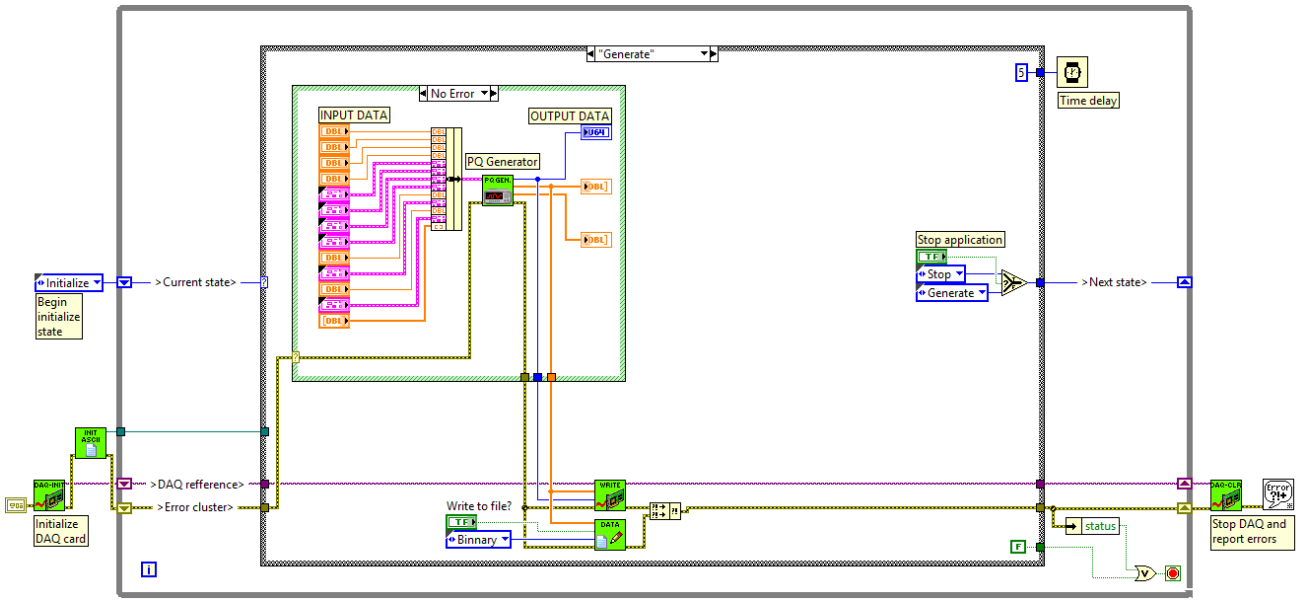

Fig. 3. PQ generator software state machine architecture

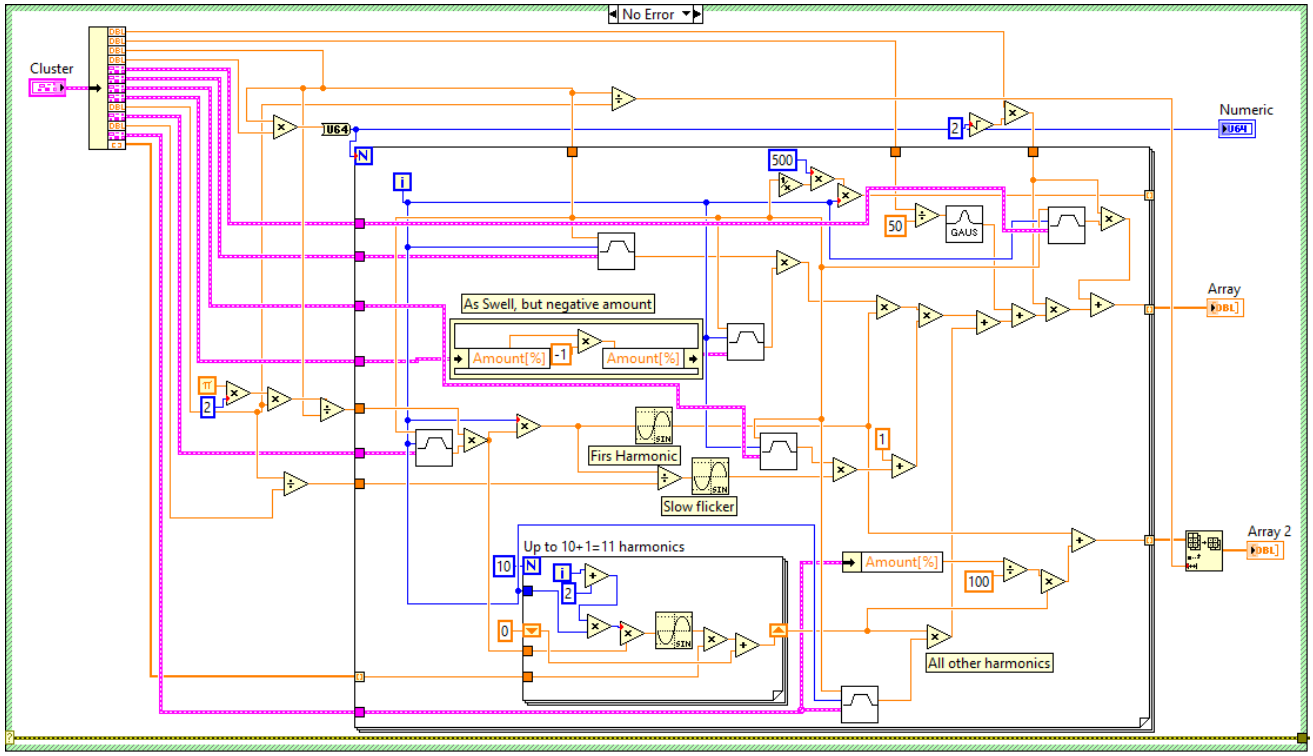

Fig. 4. Detailed view of the main PQ generator sub-VI

Some corresponding experimental waveforms, both generated using the LabVIEW virtual instrument and the amplified signals recorded on the graphical display of reference instrument – PQ analyzer Fluke 435 Series II, are presented in the following set of figures. The experiments are represented with two parts: simulated signal with the PQ amplifier (top) and recorded signal with the reference instrument (down).

Having in mind all different possible types, combinations and levels of the PQ disturbances in the experimental tests we have focused on three main groups of disturbances: harmonics, sags/dips, and transients. These PQ disturbances are often attributed to the industry environment and can cause significant damage to the electrical equipment and/or cause malfunctions in to the industrial process. Nevertheless, the system allows generation of all other types of disturbances which are foreseen to be organized in a disturbance database and distributed through internet [16] in some future publication. The Fig. 6 shows specific voltage signal with 30% level of 3rd harmonic, 20% level of 5th harmonic and 15% level of 7th high-order voltage harmonic generated with the PQ generator (top). The relative percentage levels of signal harmonics are expressed in relation to the nominal voltage amplitude level. The signal recorded with the Fluke 435 PQ analyzer are presented in Fig. 6 (down).

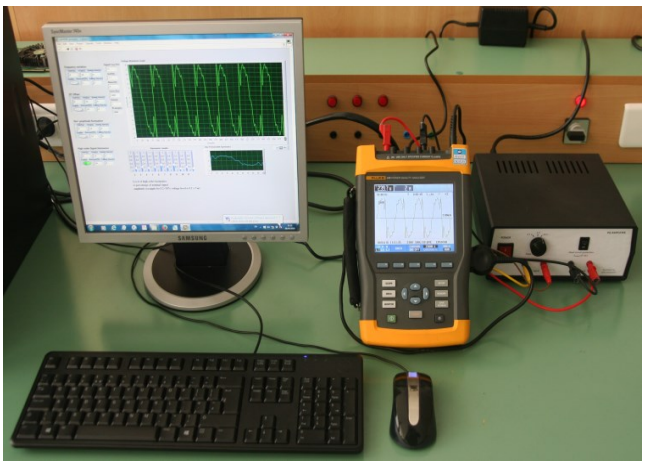

Fig. 5. Experimental system for verification of PC-based signal generator

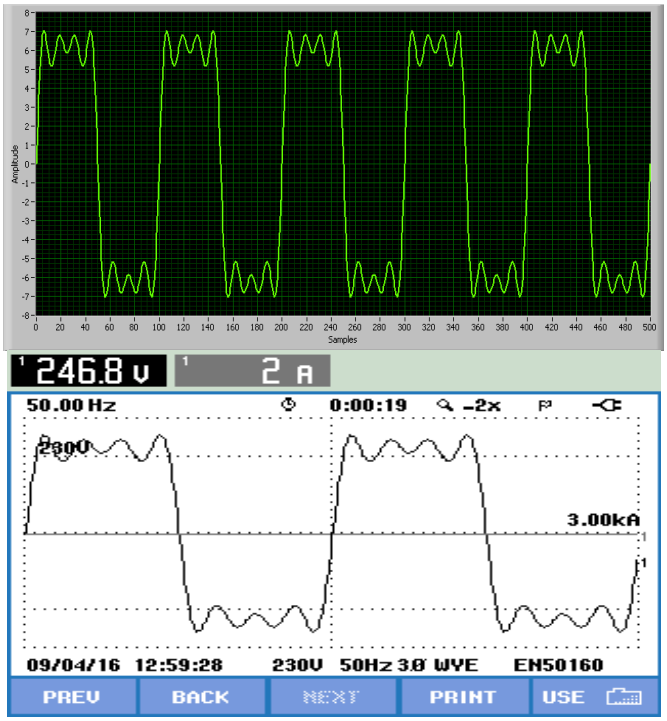

Fig. 6. Simulated highly distorted signal with harmonics with the PQ generator (top) and recorded signal with the reference instrument (down)

Experimental test voltage waveforms, including voltage dip generated by virtual instrument and recorded by Fluke 435 analyzer, are presented in Fig. 7 In this cases voltage dip test signal is generated with 50% amplitude dip level. The voltage dip has trapezoidal shape with duration of about 160 ms. The voltage dip is generated repetitively regarding the settings for the simulated signal and dip duration. Having in mind the longer acquisition period of the instrument, the reference instrument FLUKE 435 recorded two consecutive dip occurrences. The later improvements of the system will be devoted to generation of the PQ disturbances (as with the voltage dip) randomly, i.e. defined by specific probability level in a given time duration. Such behavior of the system will be suitable for realistic power line signal simulation and detection and classification algorithms testing.

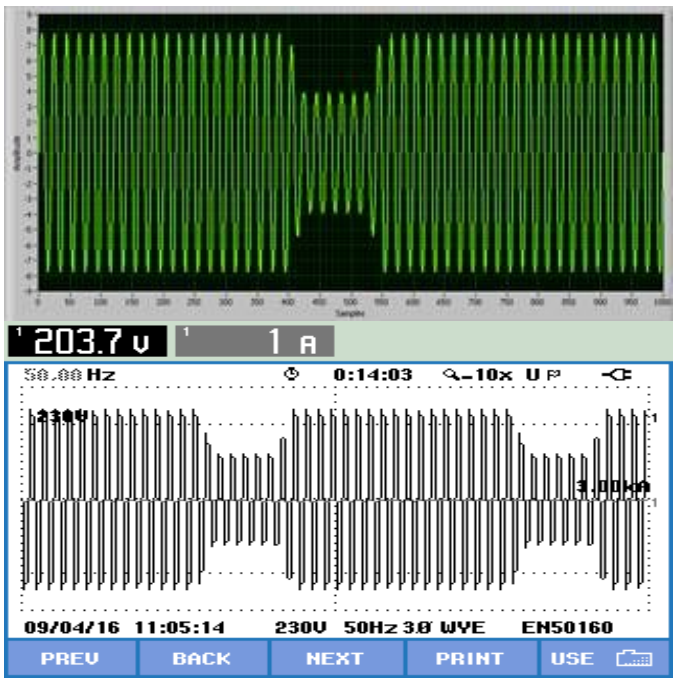

Fig. 7. Simulated voltage dip with the PQ generator (top) and recorded signal with the reference instrument (down)

Test voltage signal generated by virtual PQ generator with characteristic short-time transient (voltage peak), is shown in the Fig. 8. Such transient often appears as a result of lighting discharged in the grounding or in the power distribution grid. The amplitude of the voltage transient is limited by the maximal output voltage level of the power amplifier, which in this case is 400 V.

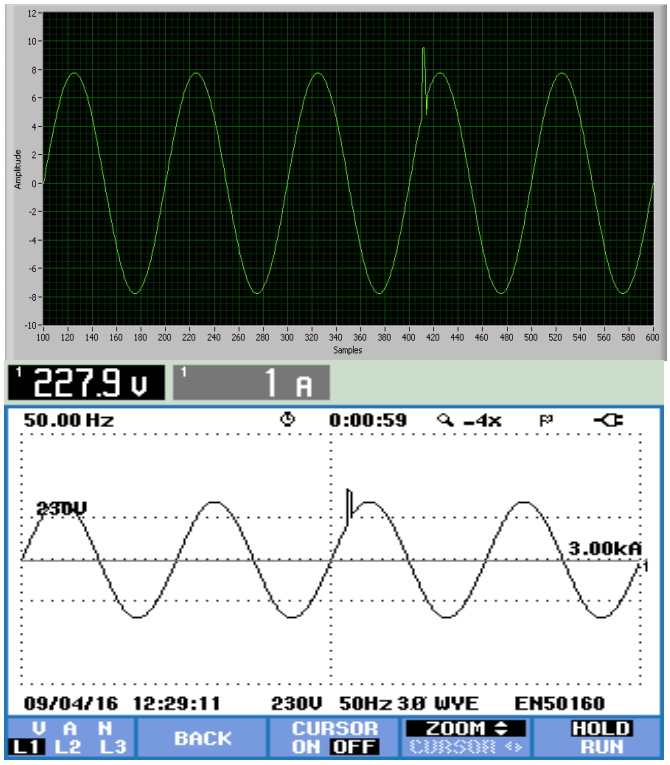

Fig. 8. Transient occurrence generated with the PQ generator (top) and recorded signal with the reference instrument (down)

Finally, the generated and amplified voltage test waveform showing characteristic case of signal with burst transients is illustrated in Fig. 9. Specific simulation of burst transient voltage events is performed using only the certain percentage level of the 11th high-order voltage harmonic component.

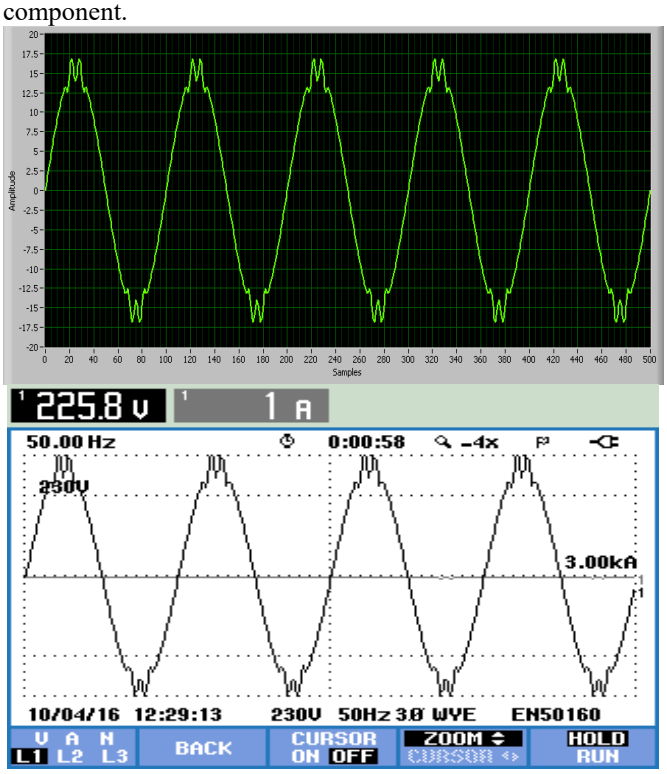

Fig. 8. Generated test voltage signal (top) and corresponding amplified signal recorded by PQ analyzer Fluke 435 – signal with burst transients (down).

CONCLUSIONS

Design and experimental evaluation of computer-based electrical power quality signal generator is presented in this paper. The generator consists of virtual instrument for simulation of standard PQ disturbances and power amplifier for scaling generated signals to the power line voltage level. The definition of basic parameters for output signal generation is enabled using the control panel of virtual instrument developed in LabVIEW environment. Moreover, the paper summarizes the software architecture and realization of the virtual instrument. Realized signal generator is experimentally verified by using the reference instrument – three-phase PQ analyzer Fluke 435. A number of experimental test signals are generated by virtual instrument, amplified and recorded using the reference instrument.

Due to mainly closed functional architecture, developed according to some specific standards, most commercial signal generators are not fully flexible and hardly adaptable to meet some specific demands and user requirements. Therefore, the software and hardware functionality are considered as one of the major advantages of the proposed solution for software supported PQ signal generation. The generator hardware and software architecture enables easy upgrade to three phase solution and very simple implementation of new functional features and capabilities.

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Voltage Source for AC Electroluminescent Measurements

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Abstract – **Alternating high voltage source for measurement of AC electroluminescent panels consisting of microcontroller, digital potentiometer, buffer with signal converter, amplifier with high voltage module, current limiter and power supply unit was developed and tested. The AC source is based on digital sine waveform generation, using the look-up table method. The generated sine waveform is furtherly amplified by AB class amplifier up to 260 Vpp. The voltage source constructed is connected to PC via USB interface. A simple testing program for the PC computer was also written.**

The test of the AC voltage source was performed by measurement of four layer AC electroluminescent panels in a setup consisted of PC computer, the voltage source developed, shunt resistor, optical fiber and spectrophotometer.

The measurement of AC electroluminescent panel shows stable behavior of the source producing sine signal without apparently visible on the oscilloscope distortions of higher harmonics.

The measured sample is of predominant capacitive character which is related to the strong influence of the dielectric layers.

Keywords – computer controlled **AC high voltage source, AC electroluminescent panels, phosphor**

I. Introduction

High AC electroluminescent panels use electric current directly through a phosphor to produce light. They are used as emergency lighting, decorative luminescent clothing, watch illumination, flat wall decorative illumination and large-area, flat-panel displays [1].

These devices are based on the principle that the electrical current is formed by tunneling of electrons from interface states at the dielectric-phosphor boundary into the conduction band of the phosphor [2].

Alternating current electroluminescence (AC-EL) in ZnS powder layers was discovered as early as 1936 [3]. Since that time AC displays are widely optimized, to achieve different color of lighting.

The thick-film AC-EL still is present in the market, since it is the only mature technology for flat and flexible large area light sources, at least as long as organic light emitting diodes (OLEDs) fail to deliver in this respect.

Measurement of dissipative current in AC devices is important not only for the understanding of the device functionality and for developing of theoretical models, but is also used from application point of view, for example to determine the internal luminous efficiency, which is an important device characteristic [4].

For the purpose of measurement an adjustable AC voltage source capable to provide two or three hundred of volts at changeable frequency is needed. Unfortunately such type of devices are not easy to find on the market, moreover they are designed for more extensive and precise measurements in the industry.

The current work aims to develop and test computer controlled voltage source for AC display measurement of adjustable voltage and changeable frequency.

II. Device

A. Hardware

The high voltage source (Fig. 1.) consists of microcontroller (μC), digital potentiometer, buffer with signal converter, amplifier with high voltage module, current limiter, and power supply unit.

The μC (1) gets commands and data from the PC via USB interface. For the digital sine signal formation the build-in timer and the PWM modules are configured and used. SPI interface controls the digital potentiometer (2) MCP4258 which sets the signal amplitude.

The digital potentiometer is set to 5 kΩ, furtherly buffered with OPA376 which facilitates the work of the next stages (4,5). In this module (3) low noise amplifier (LT1007) is used to convert the unipolar signal (5V) to bipolar one within the range of ±5V. Other advantages of this chip is the existence of additional pins for offset correction.

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The power amplifier (4) is based on the chip LT1012 establishes an amplifier of class AB. It provides high input resistance for the next modules and preliminary amplification. The high voltage part of module 4 also fulfills the strategy of AB class amplifier in a way to reach output voltage up to 260 Vpp.

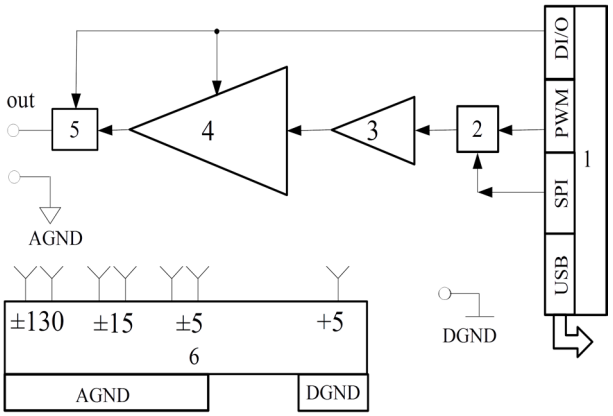

Fig. 1. Block-diagram of the voltage source for AC electroluminescence measurements: 1 – Microcontroller; 2 – Digital potentiometer 3 – Buffer with bipolar signal converter; Amplifier with high voltage module; 5 – Current limiter; 6 – Power supply

In the presented amplifier two negative feedbacks are used – local and global. The local negative feedback improves the amplitude–frequency dependence but the global one stabilizes the amplification coefficient, decreases the nonlinear distortions and improves the temperature stability of the whole amplifier.

The feedback depth could be changed by reed relays, which are controlled by the ditital pins of μC. By switching the feedback two voltage ranges could be selected ±10 V and ±130 V.

The current limiter (5) is designed to provide two ranges of current limitation - 2.5 and 25 mA.

On Fig 2 one shoulder of the current limiter is presented. This modified schematics differs from the commonly used solution for current limitation. It is necessary as the current which activates the limiter is comparable with the total

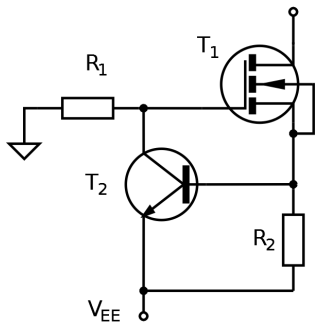

Fig. 2. Simplified schematic of the current limiter

current of the amplifier. Under the increase of the output current the voltage drop on R_2 increases and at about 0.6 V the transistor T_2 is turn on in a way to activate the current limitation by decreasing the gate voltage applied on T_1.

B. Firmware

The firmware was written in C under the MPLAB X IDE, and compiled with C18 compiler [5]. Block-diagram of the μC software is presented on Fig 3. After booting an initialization of μC, setting of the USB and timer interrupt is taking place. Next the peripheral interface is initialized,

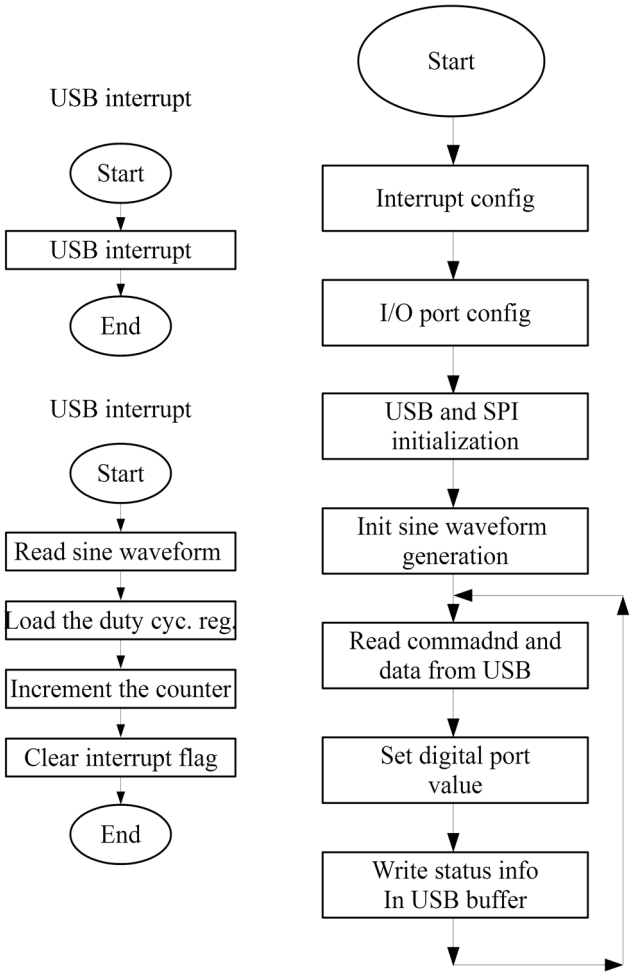

Fig. 3. Block-diagram of the firmware

with the I/O ports. USB and SPI interfaces are furtherly initialized. The USB procedures are based on the code included in Microchip Libraries for Applications (MLA) [6], while the SPI code uses the standard compiler libraries. Finally the sine waveform generator is configured and set. For this purpose the timer and PWM modules were activated and configured in a way to use the look-up table method for digital sine waveform generation [7].

After the initialization the software fulfills an endless loop waiting a command from the PC. Meanwhile the code in the loop checks for incoming package over the USB interface sets the value on the digital potentiometer and writes the status back on the USB package.

When receiving an USB interrupt, the command and data sent through the interface are read and saved for further usage.

Upon the timer interrupt next sine waveform value is red from the look-up table and prepared for the formation of the signal amplitude. Next a loading of the duty cycle register and the counter increment are performed. After

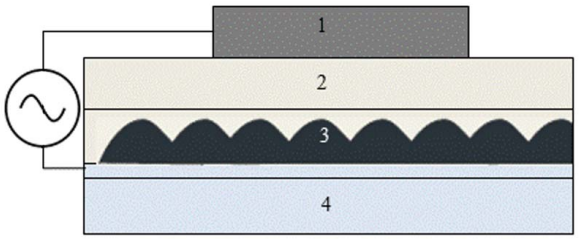

Fig. 4. Architecture of AC electroluminescent device with each specific layer: 1 – silver top electrode, 2 – double dielectric layer, 3 – phosphor, 4 – PET substrate with ITO bottom electrode

finishing the interrupt procedure, the timer interrupt is cleared to prepare the system for the next interrupt request.

A simple testing program for the PC computer was written in C++ under QT 5 IDE to check the correct work of the firmware. Further improvement of the PC software including GUI is under development.

III. Tests and Measurements

A. Samples under test

Our alternating current thick-layer electroluminescent panels consist of four separate layers. Bottom electrode is a transparent indium-tin oxide (ITO), second layer is an active phosphor – doped zinc sulfide (ZnS). The active layer consists of grains, which are preliminary formed in the paste. The third layer is formed by a double layer of strong dielectric material ($BaTiO_3$; $\varepsilon_r \sim$ several thousands) and the upmost layer is a silver electrode system. The structure of the device is drown on Fig. 4

All the layers were prepared by the mean of screen printing technique. Standard screen printing machine

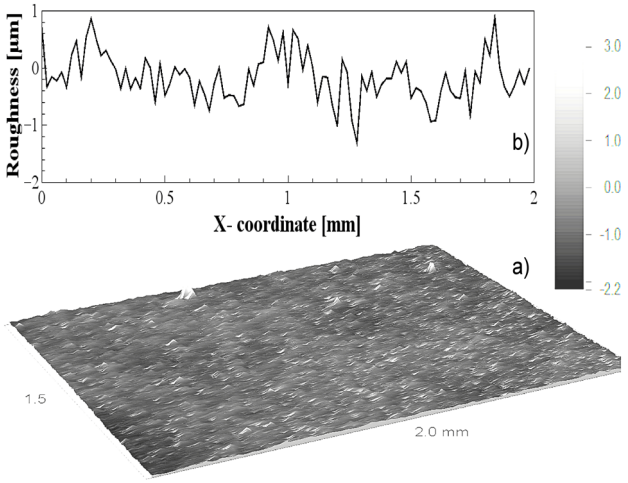

Fig. 5. Surface profile of the active phosphor layer of approximately 35 µm thickness: a) - profile of the surface roughness along the x axis; b) - map depicting the film homogeneity

RokuPrint SD05 was used. Standard screen printing formulations of pastes have been used with significant values of dynamic viscosities. Viscosity of phosphor is up to η = 2,5 cPs, silver paste η = 8,5 cPs and dielectric η = 2,3 cPs. The amount of solid content in the pastes is from 60 up to 80 %. Before the film deposition the substrates have been treated with 5% NaOH solution and isopropanol and all the pastes are soluble in organic solvent 2-ethoxyethanol. Printing parameters such as on-off ratio, printing velocity and force of the print have been optimized.

The thickness and profile of printed layers have been measured by mechanical profilometer Bruker Dektak XT. Fig. 5 presents surface profile of the active phosphor layer of approximately 35 µm thickness. On Fig. 5a a profile of the surface roughness along the x axes is presented. It could be seen from the graph that the roughness measured do not exceed ±1µm.

Fig. 5b presents 3D map depicting the film homogeneity has been measured by the mechanical profilometer. The presented surface is relatively uniform with separate peaks around 3µm which could be related to impurities included in the film during the deposition process.

B. Measurement setup

On Fig 6 block-diagram of the measurement setup is presented. The constructed AC voltage source (2) receives the data from the PC computer (1) over the USB interface and forms sinusoidal signal with a proper frequency and amplitude. The voltage source is disconnected from the ground in a way to implement two channel measurement with the Tektronix TBS2000 digital oscilloscope (5). The generated voltage is applied on the sample (3) which is an AC electroluminescent display.

The voltage applied on the sample is measured by the

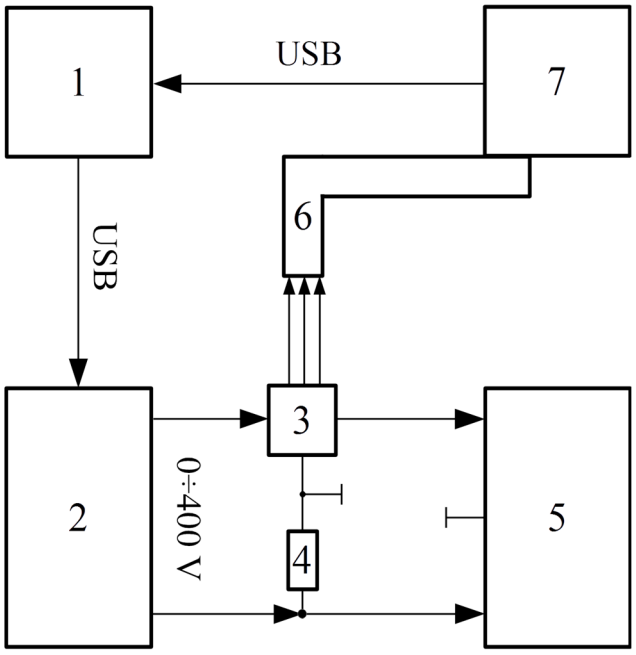

Fig. 6. Block-diagram of the measurement setup: 1 -PC; 2 – Voltage source constructed; 3 - Measured sample; 4 - Shunt resistor; 5 – Oscilloscope; 6 – Optical fiber; 7 – Spectrophotometer

first channel of the oscilloscope. The electrical current flowing trough the sample forms a voltage drop on the shunt resistor (4) which is measured by the second oscilloscope channel. The value of the shunt resistor has to be negligible with respect to the sample impedance in a way to avoid the influence on the measurement. In this way the oscilloscope measured the voltage, applied on the sample, and the voltage drop on the shunt resistor (which is

in fact the AC current flowing trough the sample, and the phase between them. Then the consumed power of the sample is calculated by the equation:

$$P=U_D.cos\ \alpha\ .U_R/R \qquad (1),$$

where U_D is the voltage applied on the display [V], R is the value of the shunt resistor [Ω], U_R is the voltage drop on R [V], and α is the phase angle between U_D and U_R, which is in fact the phase angle between the voltage applied on the sample and the current flowing trough it.

A. Results measured

On Fig. 7 oscillograms measured with the setup described is presented. The upper oscillogram presents the voltage U_D applied on the sample measured by probe x10. The signal of 1 KHz exhibits clear sine waveform which shows an absence of higher harmonics. This oscillograme shows the good performance of the voltage source constructed without apparently visible distortions of higher harmonics. The lower line corresponds to the voltage drop U_R measured on the resistor R by the second oscilloscope channel. The sine signal is more distorted probably due to

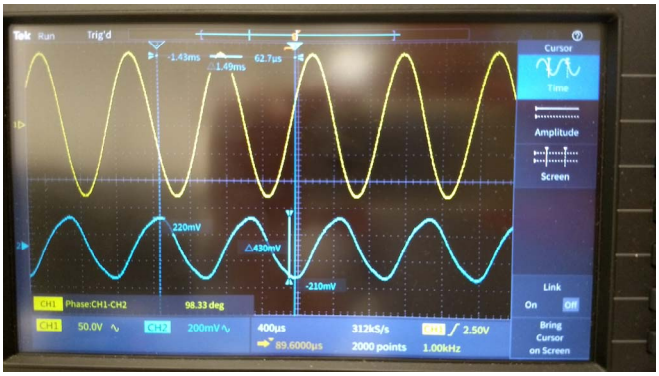

Fig.7. Oscillograms measured with the setup presented on Fig 6; upper line - U_D, lower line - U_R

low amplitude of the signal measured, the noise and the influence of the measurement probes, etc. The value 324 Ω of the resistor is chosen in a way not to disturb the measurement. As a result the voltage drop on the resistor is more than 500 times less than the voltage drop on the sample in a way not to affect the measurement. The phase angle α measured between the signal of the voltage and the current is 98.3 degree. This value shows a predominant capacitive behaviour of the sample. As seen on Fig 3 the main drop of the voltage is expected in the dielectric layer which supports the capacitive feature of the sample. The phase angle value measured shows that the predominant energy applied on the sample is of reactive character, only a few miliwats cause the light shining of the sample. This measurement shows that more precautions could be taken to increase the efficiency of the sample working.

TABLE 1. MEASURED AND CALCULATED VALUES

parameter	dimension	value
U_D	V	257
U_R	mV	440
R	Ω	324
α	°	98.3
P	mW	50.4

The measured values together with the calculated according to eq. (1) power are presented in table 1.

VI. CONCLUSION

AC source producing up to 260 Vpp based on digital sine waveform generation, using the look-up table method was developed and tested by measurement of AC electroluminescent panel based on active phosphor layer.

It was found that

The 1 KHz, 250 Vpp signal produced by the voltage source exhibits good quality without apparently visible distortions of higher harmonics, as observed by the oscilloscope.

The sine voltage drop measured on the shunt resistor is more distorted probably due to the noise and the influence of the measurement probes.

The measured phase angle of 98.3 degrees shows predomenant capacive behaviour of the sample which is explained by the strong influence of the dielectric layers. The predominant energy applied on the sample is of reactive character, only a few miliwats cause the light shining of the sample.

ACKNOWLEDGMENTS

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Long Term Performance of Data Acquisition System for Parameters of the Environment

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Abstract – **In this article are presented the results from one year autonomous working of a data acquisition system located on Livingston island. Also technical problems are presented together with possible solutions.**

Keywords – **DAQ, performance**

I. Introduction

The presented results are from a DAQ system constructed in 2015. The system is collecting measurements of the Earth's magnetic field, acceleration, internal temperature and light intensity. The acquisition period is 30min with enough memory for 13 mount uninterrupted record and battery life of 10+ years.

A. The sensors

In Table 1 are listed all sensors used in the system.

Table 1. Sensors

TAOS TLS260	Light sensor
Microchip TCN75A	Temperature sensor
Honeywell HMC5883L	3-axis magnetometer
Freescale MAG3110	3-axis magnetometer
Freescale MMA8652FC	3-axis accelerometer

More in-depth information about the system architecture (hardware and firmware) is available in a previous article [1].

B. Location

The system was located in in the Bulgarian Antarctic base on Livingston Island. The data covers almost a full year with well distinguished summer and winter periods. During the summer period members of the expedition are inhibiting the base moving the DAQ system to different locations. In the winter period the base is uninhabited, the DAQ system was located near the window of the second floor of the building. There is clear difference between the data from the inhabited and the uninhabited period. The data from the inhabited period is "contaminated" by the human presence. For example the temperature is uncorrelated with the light intensity due to artificial heating and the magnetic field changes are with amplitude far bigger than the expected change from natural sources or sensor instability. A second system was working in Sofia, equipped with the same sensors, firmware and box, but with different power source. It was powered by a pair of alkaline batteries due to relaxed requirements for low temperature operation. In the next chapter are presented and analyzed the results from both systems.

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II. Results

A. Sofia DAQ – data overview

On Figures 1 to 5 are shown the measurement from the DAQ system located in Sofia. On Figure 1 and 2 are shown the calculated Earth's magnetic field vector length from the sensor's XYZ axis data points. The time step of each measurement is 30 minutes. For each of the magnetic sensors is performed simple offset calibration by rotating the DAQ system in all directions. The calibration procedure is performed once, before the data acquisition start. On Figure 1 is shown the data from the Honeywell HMC5883L sensor.

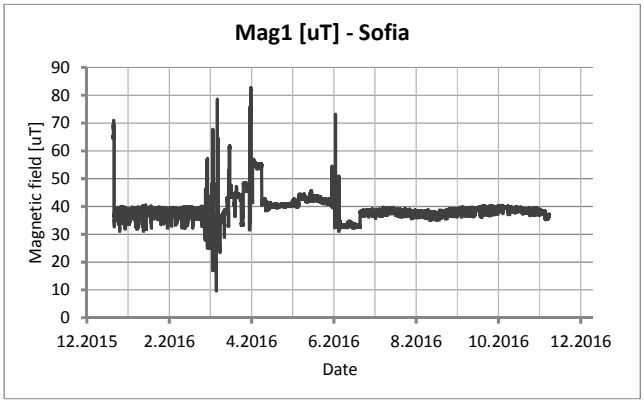

Fig.1 One year data from Honeywell HMC5883L sensor

On Figure 2 is shown the data from the Freescale MAG3110 sensor. The rapid changes in the magnetic field can be explained with human intervention. The system was located in inhabited building, data was downloaded to a PC 2-3 times during the year and overall constant working conditions were not guaranteed. On Figure 3 is shown the internal temperature of the system, measured by the Microchip TCN75A temperature sensor.

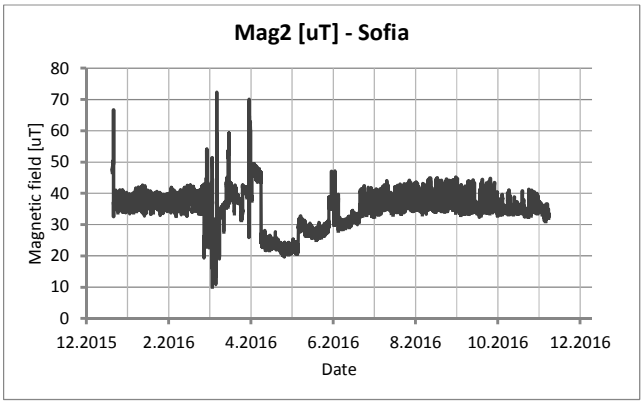

Fig.2 One year data from Freescale MAG3110 sensor

The abnormal daily temperature fluctuation can be explained with the amount of sun light shining on the system, shown of Figure 4. From March 2016 to mid-June 2016 it was located in place not exposed to direct sunlight and the temperature fluctuation are much lower with average value equal to normal room temperature.

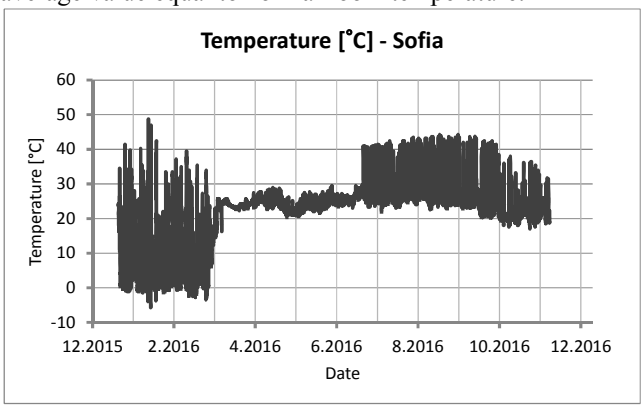

Fig.3 One year data from sensor Microchip TCN75A

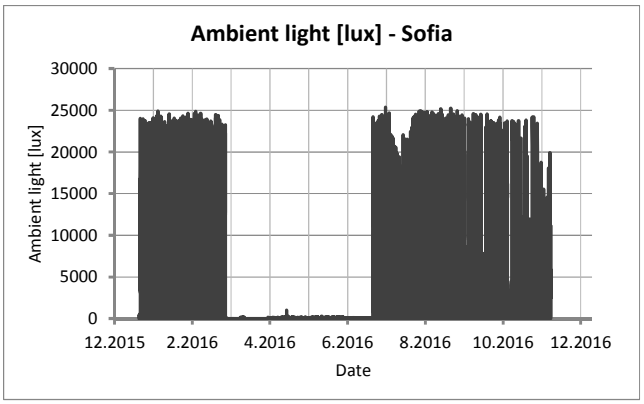

Fig.4 One year data from sensor TAOS TLS260

The battery voltage is shown on Figure 5, expected battery life with alkaline batteries is more than 2 years.

B. Livingston Island DAQ – data overview

On Figures 6 to 10 are shown the measurements from Livingston Island. On Figure 6 and 7 are the Earth's magnetic field measurements. The winter (uninhabited) period is clearly visible on these graphs. The measurements are more stable with less fluctuation in this period. The last members of the expedition left the base on 28.02.2016, leaving the DAQ system near the window of the second of the base.

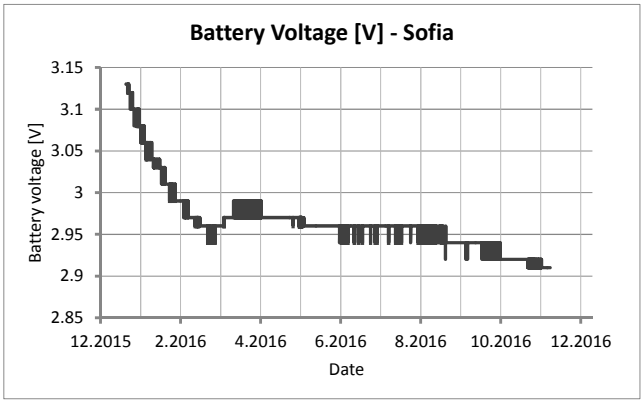

Fig.5 One year data for battery voltage

The first members returned to the base on 26.11.2016. The offset of the magnetic sensors calibrated one, before the start of the data acquisition. Mag1 and Mag2 (Figure 6 and 7) again represent the length of the Earth's magnetic field vector.

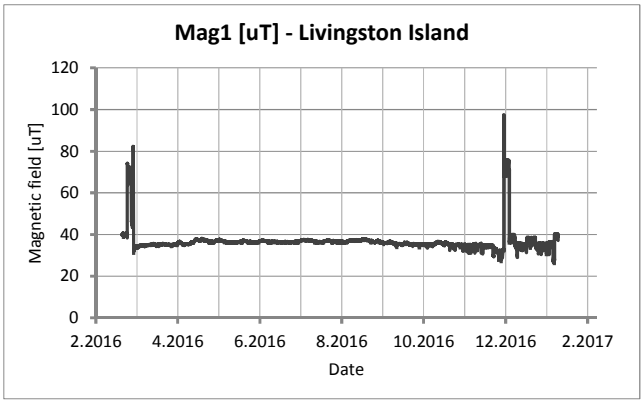

Fig.6 One year data from Honeywell HMC5883L sensor

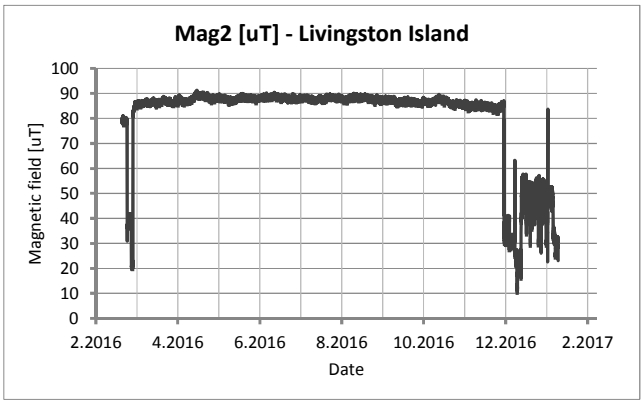

Fig.7 One year data from Freescale MAG3110 sensor

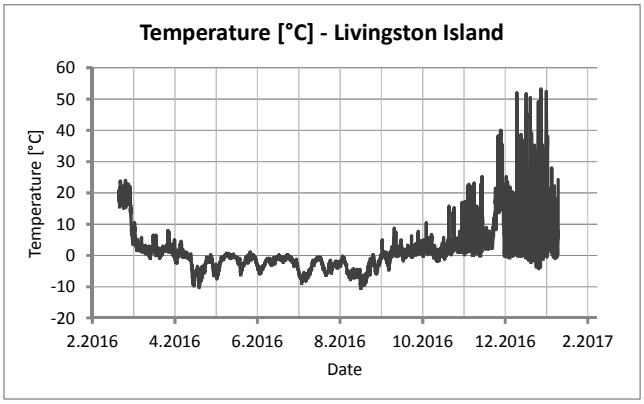

Fig.8 One year data from sensor Microchip TCN75A

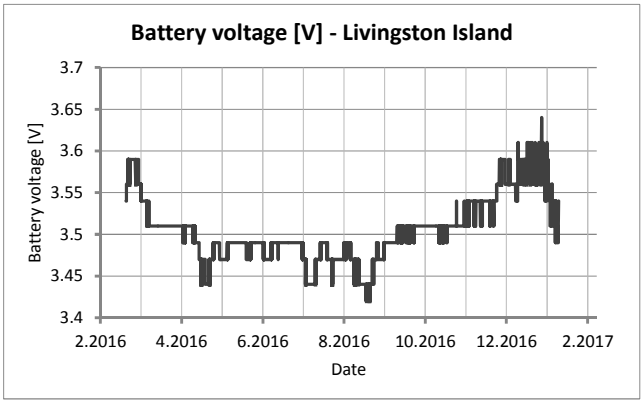

Fig.9 One year data for battery voltage

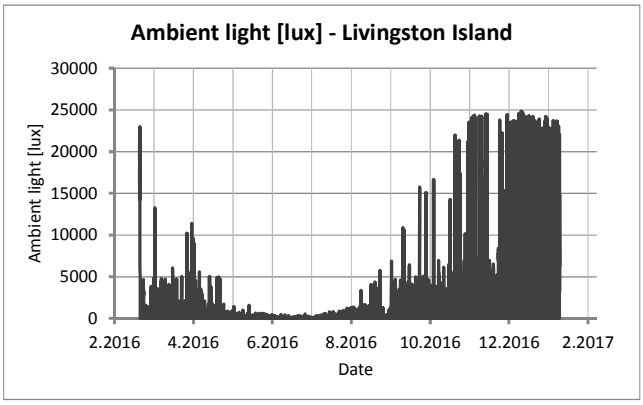

Fig.10 One year data from sensor TAOS TLS260

Since the winter period offers better data, not affected by human presence, the further data processing is focused on this period.

C. Livingston Island DAQ – winter period data

During the data analysis it was clear that there is temperature dependence of the magnetic field measurements, described in the previous article [1]. The same temperature compensation is applied to this data. The effect of the calibration of the Honeywell HMC5883L sensor is shown on Figure 11 and 12. The calibration results for the Freescale MAG3110 sensor are omitted for simplicity, the effect is similar.

The compensation is linear temperature correction (gain correction). It is based on an average magnetic field over long period of time for each temperature. The calibration coefficient is calculated for the temperature range with the most measurements. In this way the changes of the Earth's magnetic field, gain and offset drift errors of the sensors and other types of errors are averaged. On Figure 13 is shown the measurement count for each temperature in the winter period. Most of the measurements were made from -1.5˚C to 0.5˚C therefore -0.5˚C was chosen for intersection point for the linear trend line (Figure 14). The gain coefficient of -0.202μT/˚C was used for the temperature correction (Figure 12). For Mag2 measurements (Freescale MAG3110) the coefficient is -0.1867μT/°C.

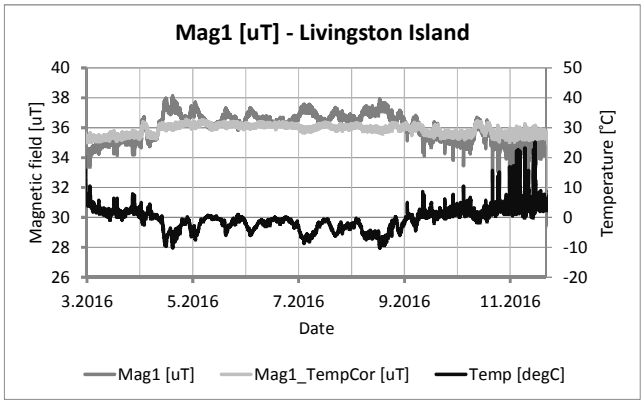

Fig.11 Honeywell HMC5883L winter period, temperature corrected data

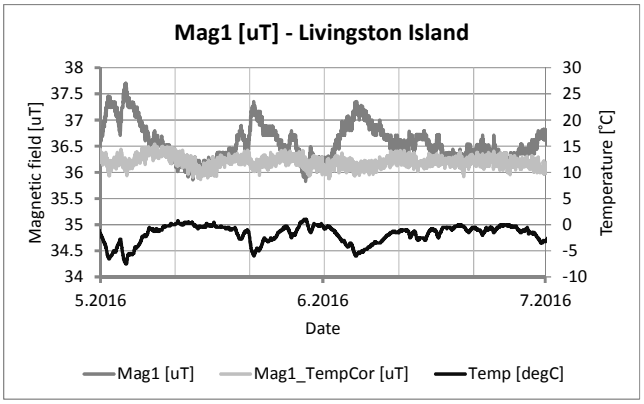

Fig.12 Honeywell HMC5883L winter period, temperature corrected data

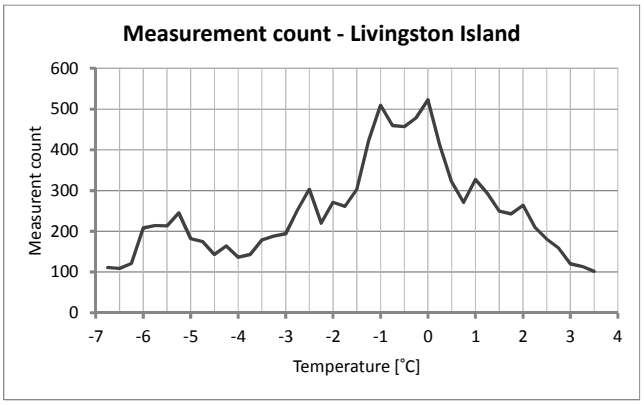

Fig.13 Measurement count over temperature, winter period

Using this type of calibration is resulting ~5 times improvement in the stability of the measurements in the used temperature range (Figure 11 and 12). The temperature dependence of the sensor is only one of the error sources, probably there is also offset and gain instability and offset temperature coefficient which are also contributing to the instability of the magnetic field measurements. The remaining fluctuation of the magnetic field, after the temperature compensation, observed on Figure 12 from May 2016 to July 2016 is in the range of 500nT. After comparing the results with magnetic data from the World Data Centre for Geomagnetism, station LIV [3], from 2014 it can be concluded that the measurements change is most likely due to sensor instability, not changes of the actual Earth's magnetic field.

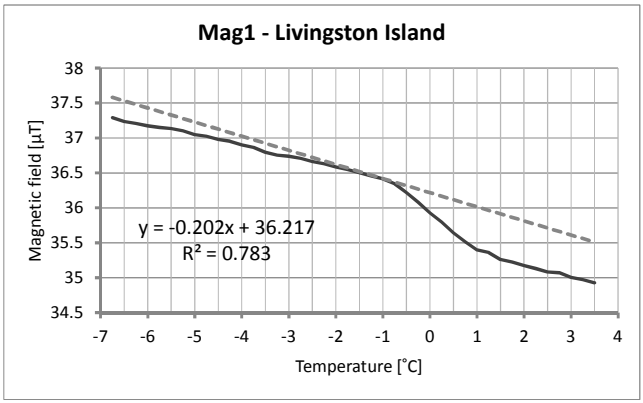

Fig.14 Magnetic field over temperature, including trend line

In the data from LIV station the change in the amplitude of the magnetic field for the full 2014 is less than 100nT.

The data from the light sensor was used to calculate the length of the day during the winter period. The threshold for day/night transition was chosen to be 10lux. This is considered very low amount of light. The result of the calculation is shown on Figure 15.

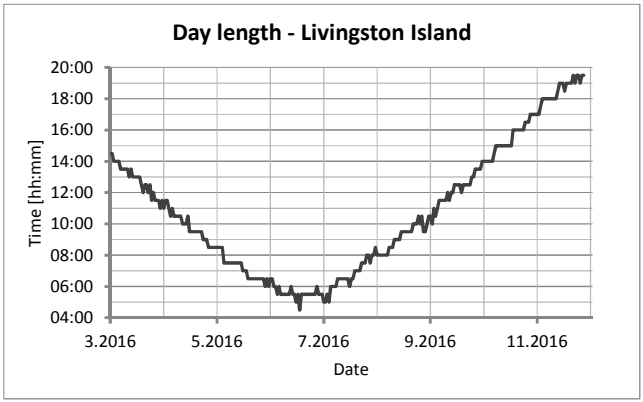

Fig.15 Livingston Island, calculated day length

The shortest day is in June and it is around 5 hours long. According to the web site timeanddate.com the shortest day on Livingston Island in 2016 is 20th of June 4 hours 53 minutes and 24 seconds [3].

III. Problems, Future Improvements and Conclusions

During the use of the 2 DAQ systems only one problem was encountered. The firmware running on the DAQ's have implemented self-diagnostic sub-functions and activated watchdog timer. If one of the self-diagnostic functions detects an unexpected behavior it calls the reset procedure. The same is for the watchdog timeout. The reset procedure is resetting the CPU, clearing the RAM and power-cycling all peripheral chips in order to recover normal operating conditions. The power-cycling is used to reset the peripheral ICs in order to have clear, well-defined reset state for the whole system. This behavior of the system is influencing the battery backed-up real time clock IC. The RTC is reporting wrong time and date when read. The RTC is read only once after reset, after that the time and date is kept in the RAM of the CPU and increased by 1sec on interrupt from the RTC chip. The self-diagnostic reset procedure is breaking the RTC time keeping, at least on the first read. In order to investigate the problem a separate system was build. This debugging system consists on Atmel 328P MCU and Microchip MCP79402 RTC this time a readily available software library for communication with the RTC was used in order to exclude probable bug in the firmware developed by us for the DAQs.

Two theories were investigated, influence of the rise/fall time of the supply voltage and time-dependent data validity of the time keeping register of the chip.

For the first theory the chip was powered from arbitrary waveform generator, used to generate the needed supply slopes. On each power cycle the IC was read and data was compared with the expected values. All combinations of rise and fall times were tested from 5ns to 100ms in 1-2-5 order for each decade. Each combination was repeated 10 times in order guarantee repeatability of the results. The results showed inconsistent fails which were not reproducible and repeatable. The rise/fall time of the supply voltage is not the source of the problem.

For the second theory the chip was power with constant rise/fall time and the time between power-on and first I^2C read was altered. Again delay times between 1μs and 500ms was tested, no fail occurred. The RTC data registers are valid after power-cycle.

A possible and un-investigated source of the problem may be a disturbance on VBAT pin of the chip. In the DAQ system the back-up lithium battery is connected with the chip with 60mm long trace without decoupling capacitor (capacitor is not needed according to the datasheet in Microchip's datasheet). In the debug system the battery was connected directly to the pins of the chip. Influence of the trace length will be a feature experiment.

In every other aspect the DAQ system performed as designed.

The Honeywell HMC5883L sensor includes a test mode which can be used for sensitivity correction of the sensor. In this test mode a known current is creating a magnetic field. This feature is not used in the current firmware, but will be implemented in the feature.

For the RTC a workaround will be implemented, five sequential reads of the time keeping registers will be made and majority voting will be performed on the read values.

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Performance Evaluation of Low-cost Particulate Matter Sensors

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Abstract – ***Increased particulate matter (PM) concentration in big cities and agglomerations is one of the main risk factors for the health of the residents. Conventional systems for PM monitoring have significant limitations, especially with respect to the costs for installation and maintenance. The number of these monitor stations is limited but PM concentration changes fast, non-linearly, within wide limits and depends on various factors. The large gradients in air quality, especially in urban areas, are a significant challenge for conventional measurement technologies. In recent years there has been a rapid development of compact, mobile low-cost measurement systems with better spatial coverage than that of traditional air quality systems.***

The present work is dedicated to the performance evaluation of commercial, off-the-shelf PM sensors. The main error sources in these sensors and the possibilities for their reduction are discussed.

Keywords – **Particulate matter, Air quality, Calibration, Regression, Correlation, Sensor characterization,**

I. Introduction and Motivation

The need to measure basic aerosol parameters has increased dramatically in the last decade. This is due mainly to their harmful effect on the environment and on public health. Legislation requires that particle emissions and ambient levels, workplace particle concentrations and exposure to them are measured to confirm that the defined limits are met and the public is not exposed to harmful concentrations of aerosols.

Recent data shows that between 70–90 % of the population is exposed to average annual PM2.5 concentrations that exceed the World Health Organization Air Quality Guideline for an annual average of 10 $\mu g/m^3$. This exposure leads to between 2.2 and 7 million premature deaths/year worldwide [1]. The spatial representativeness of the measurements used to generate these estimates is a major source of uncertainty. Thus, temporal and spatial resolution is obligatory in order to obtain reliable data to be used for establishing policies and measures for protecting the health of the citizens.

The monitoring networks that are currently in use consist of a restricted number of fixed stations. The cost for the construction of an air quality monitor station is about 200 000 Euro and for its yearly maintenance - about 25 000 Euro [2]. As a result, the stations number of in most world metropolises is limited (Table 1).

Recent research has shown that there is a clear tendency for a shift in the current monitoring paradigm. Building up wireless networks with mobile and cost effective sensors is gaining popularity as an alternative way of monitoring air parameters with a much higher resolution capability. This approach makes it possible to collect personal-specific indicative information that enables people to monitor the quality of the air they breathe [3].

TABLE 1. NUMBER OF PM MEASUREMENT STATIONS AND THE AREA IN SELECTED METROPOLISES [4, 5].

City	# of stations	Area, km^2
Beijing, China	18	~16 000
Berlin, Germany	12	~890
Mumbai, India	7	~440
New York City	13	~1 200
Sofia	**10**	**~1 310**

These facts necessitate the adoption of additional measures in order to acquire more detailed data about the levels of pollution and main emittents. Our research is part of the measures taken in this respect. It studies the accuracy of low-cost PM sensors and proposes approaches for reducing the errors in their measurements. This will make it possible to obtain online and fine-grained PM information throughout a city, by means of mobile low-cost sensor nodes.

II. Related Work

Over the last decade, the number of publications dealing with PM measurement has been rising steadily. In many publications, the use of smartphones and low-cost PM sensors is explored [6].

A lot of companies offer compact PM sensors that could be used in mobile measurement devices. However, different studies show that only few of these sensors are suitable for (near) real-time monitoring applications. As a basis for our work we have chosen the Sharp GP2Y1010 dust sensor, which has been used in many successful PM sensing projects [1, 4, 3, 7].

In previous studies, temperature compensation was attempted to allow for more reliable results under different real-world conditions. The experiments were made under controlled air conditions with constant humidity rather than in environments with temporally varying humidity conditions. The results in other studies showed significant outliers in high humidity conditions, which need to be compensated for by improving accuracy [4].

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This paper presents an experimental set-up for PM low-cost sensors performance evaluation under varying PM concentrations and temperature, relative humidity (RH) and pressure conditions. Alongside the impact of the temperature, RH and pressure changes, we have studied the accuracy, the precision, (especially the uniformity and the repeatability) of the low-cost PM sensors. Some studies do not use those concepts in accordance with their accepted definitions [7]. In the present paper we look at uniformity as a systematic error which refers to the consistency of a measured value, usually compared to another sensor taking the same measurement. Repeatability is similar to uniformity but it deals with the problem how consistent a particular sensor is against itself. It is used to describe the ability of a sensor to provide the same result, under the same conditions again and again.

For the uniformity assessment the normalized Root Mean Square Error (nRMSE) between two sensors ($S1$ and $S2$) of the same type measuring the same PM concentration was used:

$$\text{nRMSE} = \frac{\sqrt{Mean(PM_{S1} - PM_{S2})^2}}{Mean(PM_{S1} + PM_{S2})/2}, \quad (1)$$

where PM_{S1} is the PM concentration detected by sensor $S1$ and PM_{S2} is the concentration detected by sensor $S2$ for a defined time interval. Mean $(PM_{S1} + PM_{S2})$ is the average concentration of both sensors over the all measurements [8].

III. Experimental set-up

A. Test Chamber

An experimental set-up was built for the detailed performance study of the low-cost PM sensors (Fig. 1). The set-up is realized on the basis of the NI USB 6212 data acquisition system of National Instruments [9]. The control of the set-up and the measurement procedures is executed in the LabVIEW environment of graphical programming.

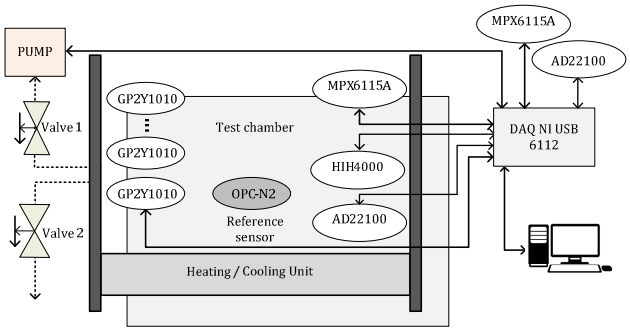

Fig. 1. Experimental set-up.

The studied sensors for PM, the reference PM sensor and the sensors for pressure, temperature and RH are mounted in the test chamber. An external heating/cooling device is used to maintain the needed temperature.

For the initial reduction of humidity we have used silica gel. The desired RH was adjusted by flowing dry air through a deionized water bubbler and then into the chamber before the test. After the RH reached the set values, the feeding of water vapor was discontinued, and PM were introduced into the chamber. The decrease of RH was found to be less than 5% during the test.

Outlets for air pumping in and pumping out are included to keep the pressure within the desired limits.

The RH was measured with a sensor probe HIH-4000 (accuracy: 3% in 0 to 90% RH) [10]. The temperature was measured with AD22100 (accuracy: ± 2°C).

For the atmospheric pressure measurement the MPXA6115A sensor was chosen with accuracy of ±1.5%) [11]. The choice of sensors for physical values is determined mostly by considerations for achieving sufficient levels of accuracy and objective parameter evaluation of the PM sensors.

B. PM Sensors and Reference Sensor

Sharp GP2Y1010AU0F sensors were evaluated in this work. The sensors employ light scattering as their operation principle. IR light is emitted into the measurement chamber. When PM is present the light is refracted by the particles and the scattered light is detected. The GP2Y1010 sensor relies on a hole through the center of the body to allow for the convection of particles [4].

The present research employs the widely used and available Optical Particle Counter OPC-N2 of Alphasense as a reference sensor, which provides reference measurement results to evaluate the performance of the low-cost sensors. Like low-cost sensors, the reference sensor also uses light scattering, while the flow of particles is regulated by a small built-in ventilator [12].

C. Algorithm for controlling the set-up

The main algorithm for conducting the measurements is shown in Fig. 2.

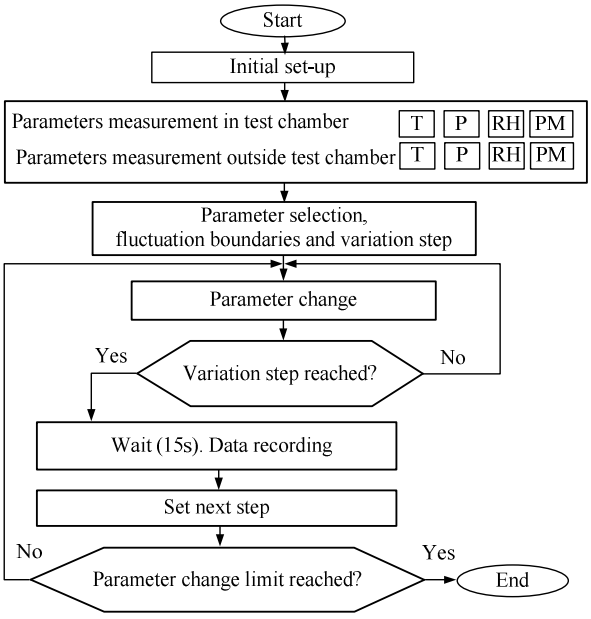

Fig. 2. Flowchart for data collection.

After the initial set-up, the main parameters in the chamber and outside it are measured. A parameter is chosen in order to study its impact on the accuracy, the boundaries of its fluctuation and the step with which it will be done. The parameter changes until it reaches the value set by the step. Then there is a tolerance interval, which depends on the dynamic properties of the studied PM sensor. In this particular case we have chosen a value of 15 seconds (determined primary by the reference sensor OPC-

N2), which guarantees that major dynamic errors are avoided. The measured data is recorded and then there is another cycle of measurements until the upper limit of the studied parameter is reached.

IV. Experimental Results

For the calibration of air quality sensors several protocols have been developed [13, 14, 15]. This section presents the experimental results on assessing the low-cost PM sensors using the revised protocol provided by European Commission JSR Protocol of evaluation and calibration of low-cost gas sensors.

All measurements with the GP2Y1010 sensors are carried out at a regulated air flow rate determined by the flow rate used for measurements with the OPC-N2.

A. The impact of RH, temperature and pressure changes

Relative humidity affected the performance of the particle sensors in different ways. Water molecules absorb the infrared radiation and often cause particle mass concentrations overestimations, due to the reduced light intensity received by the photo receiver [6].

In the tests performed under different RH levels (20, 40, 60 and 80%) and at low PM concentrations near the target values of about 20 µg/m^3 no significant correlation was found between the RH and the sensor responses.

Theoretically light scattering and absorption have no significant temperature and pressure dependence.

The impact of the changes in pressure on the measurements of the sensors has been studied by changing the pressure in the test chamber with a PM concentration of of about $20\mu g/m^3$, at temperature of 20°C and RH of 60% (at a pressure of 950 hPa). The measurements are conducted according to the algorithm in Fig. 2 with a change of the pressure in the chamber with step of 5 hPa. The tests in the range of 85 – 105 hPa show that pressure changes have no major effects on the sensor readings.

The impact of the temperature changes on the sensor outputs has been studied by PM concentration of about $20\mu g/m^3$, at pressure of 950 hPa and RH of 60%. The temperature in the chamber was changed from 15°C to 45°C with a step of 5°C.

As shown on Fig. 3, in comparison with the RH, temperature impacted sensor readings in the range of 15°C – 45 °C. The R^2 values calculated by the least-square regression were higher than 0.9.

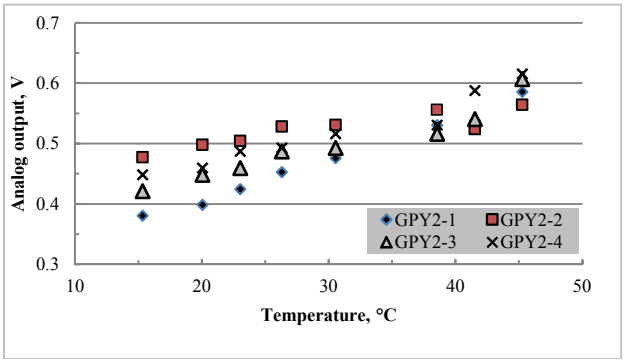

Fig. 3. Performance of 4 PM sensors at concentration $20\mu g/m^3$ and temperature in the range 15°C to 45°C

B. Linearity

When using cigarette smoke or incense smoke as the particle source, the response of the four sensors and the OPC-N2 agreed well in the particle mass concentration range of $0-500\,mg/m^3$. For the purposes of this study, the measurements with the tested low-cost PM sensors were correlated with the OPC-N2 as a reference.

For the tested sensors, a calibration function was computed by assumption of linearity between the PM sensor outputs and the reference measurements. The calibration functions were of the type $y = a + bx$ where y represents the sensor responses and x the corresponding reference PM measurement. The reverse equation (measuring function), $x = (y - a)/b$ was applied to all sensor outputs for the calculation of PM concentration levels. For the calculations a conventional least square regression and Reduced Major Axis (RMA) regression was used. Prior to RMA, the outliers are removed from the data set because they can cause significant changes to the model parameter estimates.

Table 2 shows the result for the linear regression of an averaged value for all four sensors against the OPC-N2 sensor. The averaging is justified by the high correlation values between the single sensor, which is the lowest for sensor two compared to four with a coefficient of determination given to 0.9913. An overview of all correlation coefficients is shown in Fig. 4, where values above 0.995 are rounded to 1.

Table 2. Linear correlations between particle sensor outputs and OPC-N2 measured particle

	Least squares $(0-1000\mu g/m^3)$	RMA $(0-1000\mu g/m^3)$	Least squares $(0-500\mu g/m^3)$
Slope	374.69	384.73	355.05
Intercept	-157.38	-168.78	-149.23
R^2	0.978	0.977	0.98

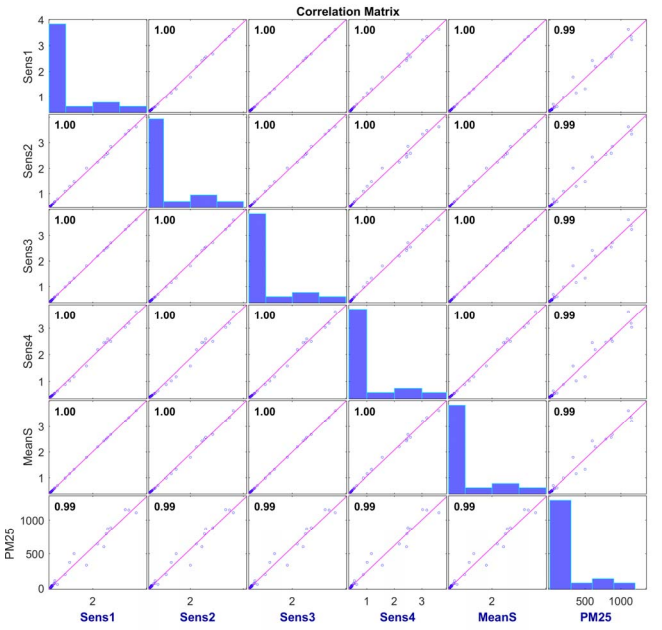

Fig. 4. Correlation matrix with linear regression line (magenta) and normalized correlation coefficient for all single sensors, an averaged value (MeanS) and the OPC-N2 at PM25.

The coefficient of determination between the OPC-N2 and the sensor average is very high with $R^2 \approx 0.98$.

The results in the table are used to assess the accuracy with the help of linear regression. Although the results vary slightly, the very high R^2 value indicates the good performance of the low cost sensors. The small differences between the least-square and RMA regression indicate minor influence of the variation of OPC-N2 measurements.

C. Uniformity and Repeatability

The results of the nRMSE explained in Section 2 indicates a very good uniformity of the 4 sensors. Table 3 shows the results for a low particle concentration of 4.2 $\mu g/m^3$.

TABLE 3. NRMSE VALUES OF THE FOUR EXAMINED SENSORS

Sensor A	Sensor B	nRMSE
1	2	0.079
1	3	0.024
1	4	0.078
2	3	0.088
2	4	0.155
3	4	0.082

Repeatability, the likely difference between two measurements made under repeatability conditions, is computed as $2\sqrt{2}s_{LV}$ where s_{LV} is the standard deviation of repeatability for 50 and 80 % of target level (LV) [13]. We found an s_{LV} of 1.64 $\mu g/m^3$ and relative s_{LV_rel} of 22%.

D. Limit of detection

The limit of detection (LOD) is the minimum concentration of the analyte that reliably can be detected with a specified level of confidence. There are a number of approaches which can be used for LOD evaluation and that is why it is important to state the used approach. Here for the LOD and limit of quantification (LOQ) calculations $3s_{BP}$ and $10s_{BP}$ values are used, where s_{BP} is the standard deviation of repeatability for the blank probe. According to the Kaiser and Specker (1956) method [16]:

$$\text{LOD} = 3s_{BP}/b, \qquad (2)$$

where b is the slope of the fitted line. We calculated an average value of LOD $= 10.93\ \mu g/m^3$ and $LOQ = 36.43\ \mu g/m^3$ for the GP2Y sensors.

VI. CONCLUSION

Increasingly complex and demanding regulations to mitigate particulate matter pollution mean that aerosol measurements are becoming more and more time- and resource-intensive. Latest developments in the field of sensor technologies have enabled the implementation of low-cost sensor systems which are specially designed to be used in urban environments. They provide highly space- and time-specific results and in this way yield important information, which facilitates exposure assessment and hazard mitigation.

The evaluated low-cost PM sensors performed well during this performance evaluation: low intra-model variability and overall good correlation with the reference instruments. Our research indicates that the fluctuation of basic parameters in the environment can results in considerable errors in the sensor readings. The results of the present study prove that the impact of temperature changes is the dominant one, which has been reported in other research too. Regardless of limitations in the accuracy of the GP2Y1010 sensors, their small size and low cost offers the ability assess the aerosols variability in different environments.

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Design of Strain Gauge Anemometer for Work in Antarctic Conditions

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Abstract – **This paper describes the design of anemometric device based on strain gauge sensors. The device relies on an ultra-low power micro architecture and adaptive power distribution mechanism. It is dynamically reconfigurable for working in real time transfer slave mode; and ultra-low power, fully autonomous, self-monitoring, long-term measurement mode. For convenience the collected data of the environmental parameters could be initially analyzed and visualized by specialized master system and end-user software tools.**

Keywords – **Strain Gauge Anemometer, Wind Speed, Wind Direction, Weather Station, Ultra-Low Power Management, Self-Monitoring, Dynamically Reconfigurable, Global Warming, Data Acquisition.**

I. INTRODUCTION

Monitoring of the ambient parameters is important task for a number of activities. This includes, but is not limited to, studying the weather and the climate, preparing whether forecasts, collecting reference data for other studies, for aviation and navigation purposes, etc. Each of those tasks requires specific monitoring and/or logging system.

Usually, to study the climate changes, is necessary to analyze data from long-term measurements of the environment parameters like temperature, barometric pressure, humidity, etc. The data from the daily measurements are then logged into sets of different time frames (in conditions defined by World Meteorological Organization [1]) and analyzed to define the tendencies in the climate changes.

At the same time collecting a reference data for other studies requires measurements to be focused on current weather conditions. In this case is used an equipment allowing real-time monitoring of environmental parameters – measurements are done continuously, and a suitable interface is provided for communication with the user and/or other systems. Data from these measurements can be then used as a reference in order to take into account possible errors in the further processing of data from other measurements taken in parallel or used as an input for other systems.

Wind characteristics are typical example for environmental parameters that could require both long-term and real-time measurements. Tracking the wind speed and direction changes is specific and important task not only for the matter of weather and climate study, but also for a various everyday activities. In cases where conventional anemometers are not applicable, this task could be very challenging. Examples of such cases are places where wide temperature deviation exists and could cause freezing of the moving parts of the anemometer or blocking them due to infestation of small particles from dust and/or ice.

In order to support a research of Bulgarian Antarctic Expedition it was requested to provide anemometric system which should be capable to sustain the work in Antarctic conditions. Specific problems taken into account are the wide amplitude of the wind speed and the specific temperature conditions, namely freezing and thermal shrinkage. Another issue is the high air infestation of small hard particles – primary ice, but also dust picked up during intensive winds.

This task requires development of low-power anemometer without moving parts. Additionally, it should be able to communicate with external systems and provide data on-demand and as per the requirements of the real-time operation.

This particular set of conditions causes conventional cup anemometers to fail during long-term usage. Pitot tubes and sonic anemometers are also not convenient to use due to freezing and clogging risk.

Sphere laser anemometer [2] has shown some promising results, but there is no data for ice protection, air density changes and power requirements.

Due to above constrains, an idea for strain gauge anemometer have appeared with design characteristics described in this paper.

II. MECHANICAL DESIGN

Figure 1 presents the mechanical construction of the sensor, which consists of main pivot and covering coat.

Several considerations are made during mechanical design of the system:

- Measurement range;
- Uniformity of force distribution;
- Diagnostic and Calibration.

Main pivot is built of two pairs of strain gauge sensors with different sensitivity. This approach provides possibility to record wide range of wind speed by changing the resolution of the sensor.

Each pair contains two strain gauge sensors with perpendicular sensing axis, in order to detect wind direction from 360 degrees. Covering coat is designed to

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transfer wind force to pivot evenly despite of the wind direction. It also serves to shields the sensors from the environment.

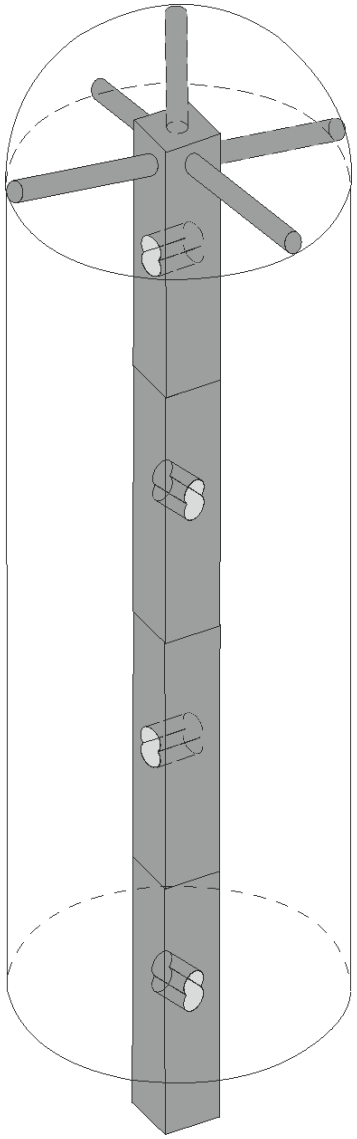

Figure 1 – Model of Strain Gauge Sensor

There are also two critical elements that require special attention during installation of the sensor – orientation of the sensor and mounting precision.

The orientation of the sensor is important for the system, so it gets the correct values for wind direction. In general, this requires some attention from the operator. Considering working conditions, this could be quite an issue, which may lead to incorrect data logging. To avoid such a problem and to ease the task of the operator a tri-axial compass is added to provide the orientation of the sensor to the system on-demand – during calibration or during diagnostic process.

Due to character of the strain gauge sensing, sensors need to be mount absolutely perpendicular to its foundation. Any deviation may cause static errors due to gravitational force, which in that case needs to be included to final calculations. To help covering such an issue, a gyroscopic sensor is used.

In addition to those two sensors a tri-axial accelerometer is added to help detecting wind blasts.

III. HARDWARE DESIGN

The development of the hardware is based on constrains of working conditions and environment:

- Continuous data logging;
- Lack of energy sources;
- Extreme weather conditions;
- Unattended area.

These conditions set requirements for ultra-low power management architecture and self-monitoring mechanisms.

Thus the system is designed on the base of three main subsystems:

- Power and Reset Manager;
- Control subsystem;
- Front-end block and auxiliary sensors.

Figure 2 presents the device block diagram.

A. Power and Reset Manager

The Power and Reset Manager (PRM) is entirely hardware based mechanism which ensures system maintenance on board level. It consists of two main structures – power control module and off-chip reset distributor.

Power control module structure includes accumulator, battery charger, on-board power conditioners, and power switching mechanism.

Power switching mechanism is critical for the system. It provides adaptive power control that ensures the ultra-low power requirements. It also includes over charging and short circuit protection modules.

Specific point in the design is the provision of autonomous power supply for the device. This is critical for two reasons – first, this allows the device to work as a stand-alone system, making it more flexible for usage; and second, because this provide relaxation on power requirements for master system, when device is used in smart-sensor mode.

Off-chip rest distributor is logical-gate based circuit, which propagates different on-board reset sources to MPU. It includes voltage level supervisor, on-board watch-dog timer, temperature supervisor, and manual reset circuit.

B. Control Subsystem

The control subsystem is based on efficient ultra-low-power mixed-signal microcontroller (MSP432P401R [3]) and includes user control interface for direct work with the system, real-time clock, an additional internal watch-dog timer, and data memory.

Control interface subsystem is dedicated slave interface from device point of view. It is based on I2C and RS232, which allows the device to serve as a smart sensor for a larger system such as Adaptive Weather Station [4]. It

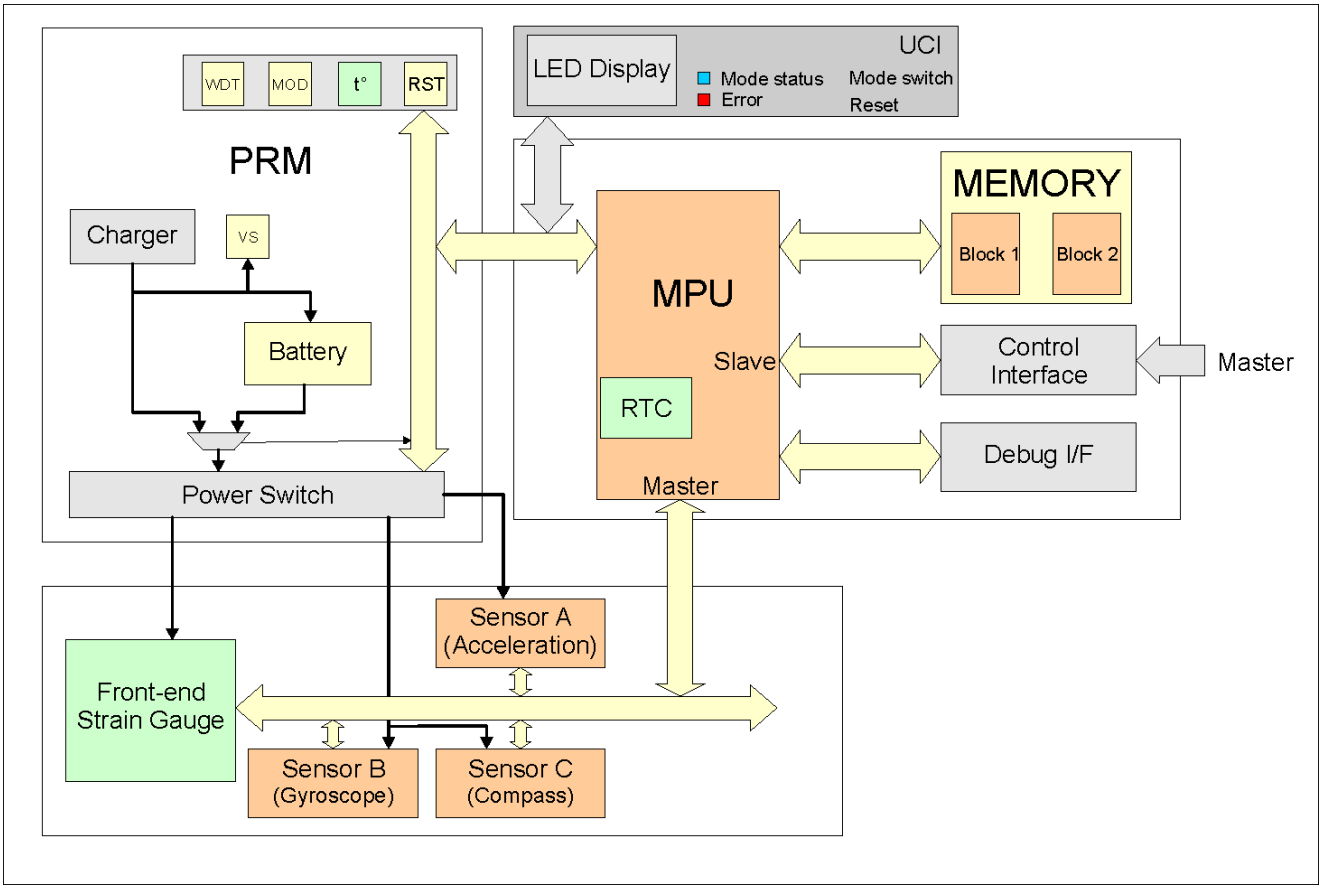

Figure 2 – Block Diagram

provides options for setup, control, and direct read of the memory.

Additionally there is a debug interface, based on JTAG, which allows programing and debugging the device during development and updating the firmware afterword.

Real-time clock and the internal watch-dog timer ensure the continuous operation of the microcontroller and the system. RTC provides time stamp required for the synchronization of the measured parameters with a global database. This is critical for the stand-alone mode, but also very useful for backing up the main system time during smart sensor mode.

User control interface is a simple direct control mechanism, which allows interaction with device on basic level to help setup modes, calibration, and real-time data observation.

C. *Sensor Subsystem*

The sensor subsystem includes front-end electronics, necessary for converting analog signal from strain gauge sensors, and the three auxiliary sensors (tri-axial compass, accelerometer, and gyroscope) described above.

Each subsystem is equipped with controllable power supply in order to cover ultra-low power requirements.

IV. Firmware Design

System management is executed by embedded software, including algorithms for determining the operating modes of the system (stand-alone or smart sensor), powering the sensors, synchronization, error detection, analysis and reconfiguration of the operating modes, the data logging and transmission.

Figure 3 presents the simplified block algorithm of the firmware. There are three main algorithms that build the firmware:

- Self-diagnostic,
- Power Management and
- Data collection.

A. *Self-diagnostic*

Self-diagnostic algorithm is executed during the first (diagnostic) system scan after restart. Its main task is to check the system health status and to configure appropriate working mode. It is executed in two phases.

Component detection – during this phase firmware is scanning all peripherals within the system. Each scan is performed for a predefined period of time (2x sensor's maximum response time); if a response does not appear during this time frame, the program cancels the scanning process, flag the sensor as unusable, and log an error message. Once detection scanning is completed a watch-dog timer (WDT) starts monitoring the system during its normal operation. Component detection is performed only once after restart, as this is high power consuming operation. If sensor fails during normal working mode, WDT will restart the system and the failed sensor is detected during new diagnostic scan.

Error detection – this phase is active during system's normal operation mode. It logs all errors/status that could

appear – mode change, reset, manual scan requests, inappropriate user configurations (invalid input data, syntactic error, invalid command, etc.), data memory overflow, etc.

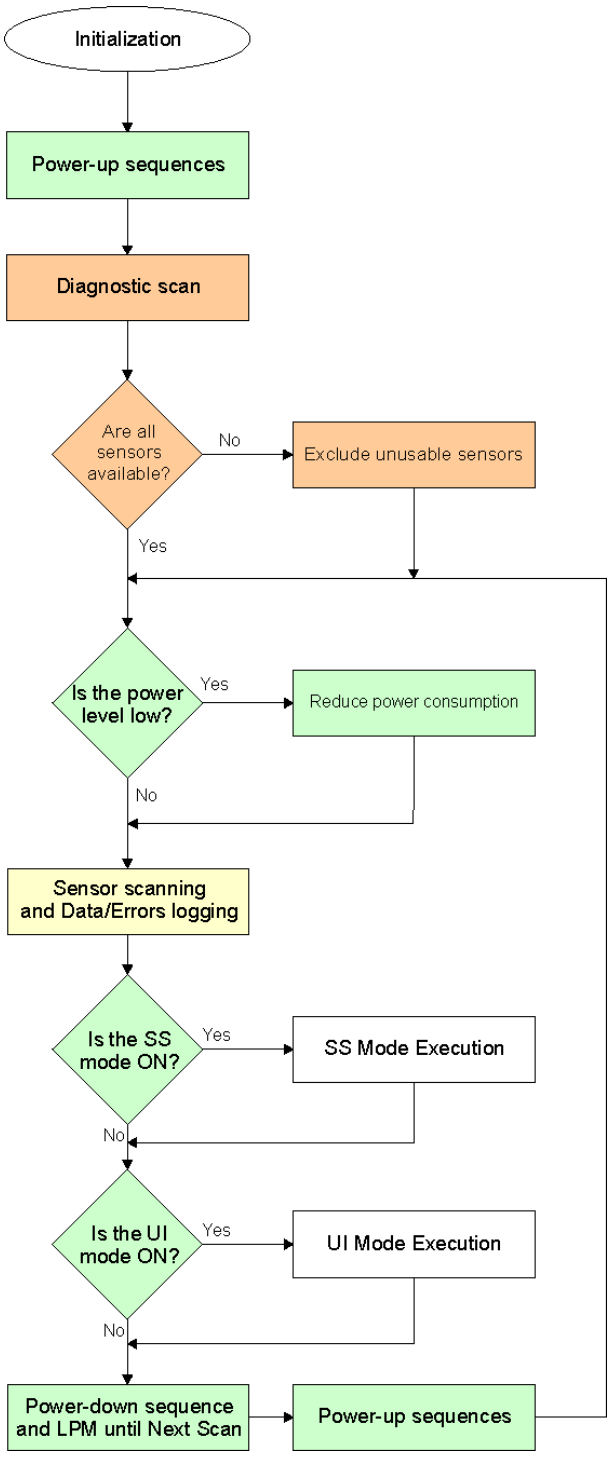

Figure 3 - Block Algorithm

B. *Power Management*

Power Management algorithm is executed immediately after initial initialization and have the responsibilities to perform power-up and power-down sequences necessary to prepare the peripheral devices for work, and to switch them off to save power. This program is in direct service of the data collection algorithm. Additionally, this program monitors the traffic upon the user interfaces and can change the working mode from user-controlled (UI Mode) and smart sensor mode (SS Mode) to stand-alone mode, if defined time of interface inactivity expires. And vice versus - if the user/system request control appears, it changes the modes back.

In cooperation with the Data collection algorithm, the Power Management also monitors the battery status, and can cut down the power exhaustive sensors, if the source drops below predefined thresholds, and keeps the system active for longer periods.

C. *Data collection*

Data collection algorithm is the main program that is running during normal operation mode. Its main task is to collect data from the sensors and record them in the embedded memory. It also provides vital data for Power Management and Self-diagnostic algorithms in order to keep them function properly. It is also responsible for user communication and all data exchange including acceptance of control commands and data conversion for real-time user usage.

V. Conclusion

This device is designed to extend the range of action of Adaptive Weather Station – system designed to support a research of Bulgarian Antarctic Expedition.

First prototype is under development and is expected to be send to Bulgarian Antarctic base on Livingston Island, during 26-th Antarctic expedition in the end of 2017.

VI. Acknowledgement

The present research is supported by the Bulgarian National Science Fund under Contract И02/11/2014.

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Sun Tracker with Sensor – Photovoltaic Cell

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Abstract – **The paper presents a technical solution for one-dimensional (east-west) solar panels managing as two photovoltaic cells are used for the sensor. The photovoltaic cells are placed at an angle of 45 ° to each other on the surface of the panel. If the difference between the measured radiations by the cells is greater than 5%, the corresponding relay is activated and the panel rotates. The proposed solution is simple, its parameters can be easily changed and can be implemented with the Arduino microcontroller. It provides a rapid reaction to increase the effectiveness of the solar panels under fast changing environmental conditions. The implementation and experimental results are also presented.**

Keywords – **maximum power point trackers, microcontroller, sun tracker, photovoltaic cell**

I. INTRODUCTION

As solar power increases in popularity, the need for this power to become more efficient is evident. Renewable clean, energy sources are becoming more desirable throughout the world, and solar power provides this. Unfortunately, solar energy is not as efficient as traditional energy sources, but there is a boom in the development of the solar panel technologies.

Systems with a built-in tracking mechanism for the sun's trajectory aim to maximize electricity production by rotating the solar panels in an optimal position.

The targeting of modules is based on measured values [1, 3, 4] of solar radiation or by a controller configured for the specific geographic location of each tracker. According to system makers, the use of positioning structures increases panel efficiency by about 25% for single-track monitors and about 35-45% for dual-track tracking systems.

The technical solution presented in this article is a one-dimensional (east-west) solar tracking, with two photovoltaic cells being used for sensors. The theoretical foundations of the method, the geometric positioning of the photoreceptors and the equation giving the connection between the azimuth of the sun and the difference between the currents measured by the two cells are shown. The hardware and the software designs of the tracker: the block diagram, the full electrical schematic and the algorithm diagram are also shown in the paper. The device is based on the Arduino microcontroller. The physical implementation is represented too.

This research creates an efficient tracker, easy-to-use, manufacture and setting, adaptable to various power and size panels, and last but not least, with an affordable price [1, 3]. This tracker provides a rapid reaction to increase the effectiveness of the solar panels under fast changing environmental conditions.

II. PRINCIPLE OF OPERATION

A. Theoretical Bases

Altitude angle and azimuth of the sun are changing constantly and are determined by the declination (day of the year), hour angle (hours a day) and latitude of the location in question.

The fundamental principle of the shadow created by an opaque barrier is used for the continuous observation of the azimuth of the sun. Moving the shadow is a linear function of the height of the barrier and the angular displacement of the light source - the sun. The use of this principle is possible in a variation with angled photoreceptors. Figure 1shows the geometric positioning of the sensors.

To shift in east-west direction at an angle Θ, two identical photovoltaic cells are used. They are symmetrically placed of an angle α on both sides compared to the normal N. The photocurrent generated by each of the photovoltaic cells can be described using the equations:

$$I_W(\Theta) = E_{sun}.R_{PV-W}.A_{PV-W}.cos(\Theta + \alpha) \quad (1)$$

$$I_E(\Theta) = E_{sun}.R_{PV-E}.A_{PV-E}.cos(\Theta - \alpha), \quad (2)$$

where E_{sun} is the instantaneous irradiance produced by the sun.

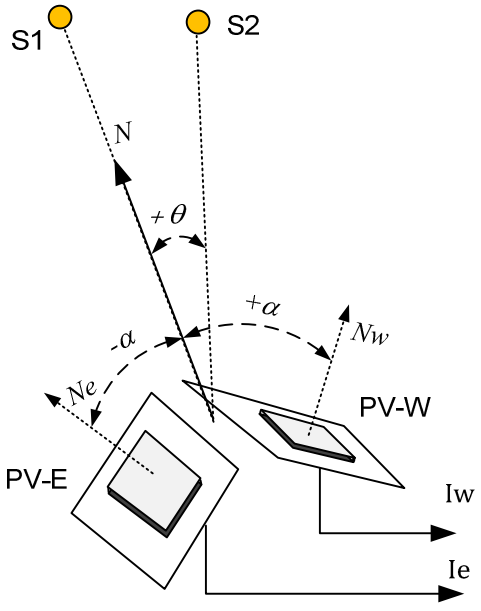

Fig.1. Geometric positioning of the sensors

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R_{PV-W}, R_{PV-E} – sensitivity of the photovoltaic cells, A_{PV-W}, A_{PV-E} is the photosensitive area.

Photovoltaic cells are identical, as a result of which $R_{PV-W} = R_{PV-E}$ and $A_{PV-W} = A_{PV-E}$.

The difference in the generated signals at angular displacement of the sun will be:

$$\Delta(\theta) = I_W - I_E = (+/-)2 \,.\, E_{sun}.Const.\sin(\theta) \,.\, \sin(\alpha),$$

where the sign defines the direction of the offset angle Θ, direction west or east.

The angle α is constant and is determined by the sensor's design. In this case, it is selected to be 45 ° for higher sensitivity of the device.

To determine the moment of turn actuating the panels to the east or west, the difference Δ(θ) compares with a predefined threshold Δ_{Th}:

$$|\Delta(\theta)| > \Delta_{Th}$$

B. Hardware Design

On the basis of the previous subsection a sun tracker is developed. The block diagram of the device is shown on Figure 2 and the electrical schematic is shown on Figure 3.

An important element of this technical solution is the microcontroller. Arduino Uno is chosen because of its simplicity of use, the affordability, the availability of various shapes and sizes to fit the variety of practical needs.

They are positioned at an angle to each other on a board placed on the surface of the control panel. Their maximum current is about 20mA, which also determines the voltage gain of the amplifiers $A_U = 20$.

Through the sensors, the intensity of sunlight is measured; the microcontroller forms the difference between the readings of the two sensors.

The sensors are photovoltaic cells operating in a mode close to that of a short circuit with load resistor R = 10Ω.

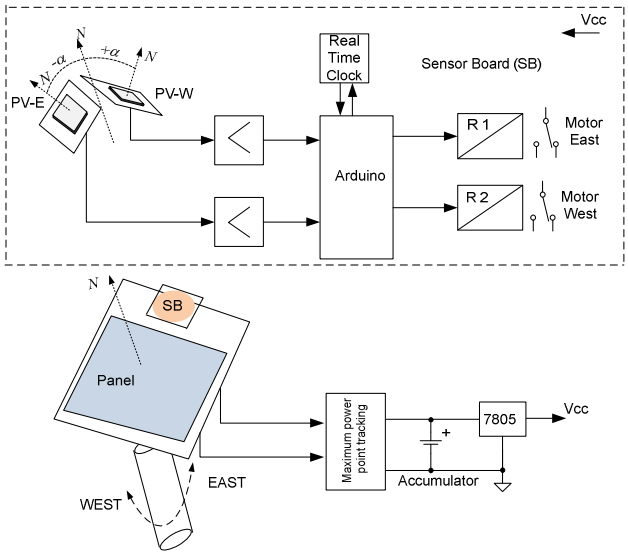

Fig. 2. Block diagram of the sun tracker

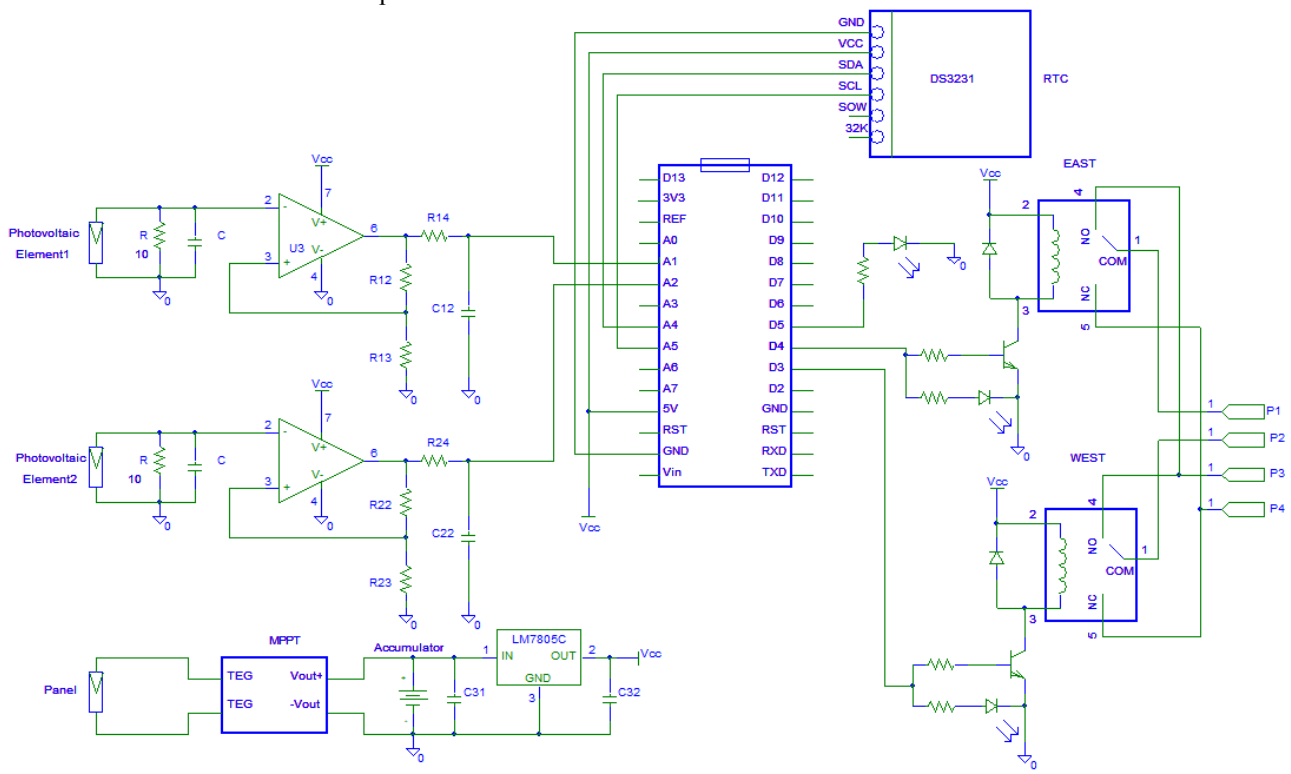

Fig. 3. Electrical schematic

If the difference between the readings is greater than the set value *Δth* (for example 5%), a signal is generated to the relays in the device. The relays control the direction of rotation of the motor in the system, east or west respectively.

The motor rotates the control panel together with the sensor board mounted on it. If the sun is located along the N-axis of the block diagram shown on Figure 1, the difference between the photovoltaic solar energy measured by the two photovoltaic cells will be below the set value *Δth*. The control of the relays is accomplished by the inclusion of additional transistor switches controlled by the microcontroller [7].

The tracker works in the bright part of the day and for this purpose a RTC module, a real-time clock, is included. The sensor readings are processed on the condition that the measured intensity is greater than 100W/m^2.

The tracker must operate autonomously without external power supply. That's why a rechargeable battery is being charged from the sun through the day using the MPP tracking driver.

C. Software Design

Figure 4 shows the algorithm diagram of the tracker software. System parameters that can be varied according to specific needs are the threshold *PVmin* = 100W/m^2 over which the results of the measurements are processed, the difference in readings between the two sensors over which the motor is rotated *Δth* = 5%, as well as the astronomical time through which the device operates. The time slice in which the tracker works can be set automatically using a calendar. The tracer turns east at night to be ready at sunrise.

III. PHYSICAL IMPLEMENTATION

The proposed solution has been tested in its own parts. Figure 5 shows a picture of the tested sensor board. The photovoltaic cells of TRONY type SC25S-3N, microcontroller ATmega168 or ATmega328, MPP tracking driver, type 120ML M902, relays type JQC-3F-1C-5VDC are used.

IV. CONCLUSION

This paper proposes a technical solution of the one-dimensional (east-west) sun tracker. Two photovoltaic cells are used for the sensors. The sensors are positioned at an angle α to each other on the surface of the control panels. Sensors run relays that rotate the motor while the difference between the measured solar energy from the cells becomes less than a set threshold. This means that the panel is oriented perpendicular to the sun and its efficiency is maximum.

The geometric positioning of the photovoltaic cells at an angle of α to each other and the equation for the calculated the sun azimuth using the photocurrents are represented. The design of the device with the block diagram, the full electrical schematic and the algorithm diagram are also shown.

The proposed solution is simple; easy to use and manufacture, its parameters can be easily changed and can be implemented with the Arduino microcontroller. It provides a rapid reaction to increase the effectiveness of the solar panels under fast changing environmental conditions. The physical implementation are also presented.

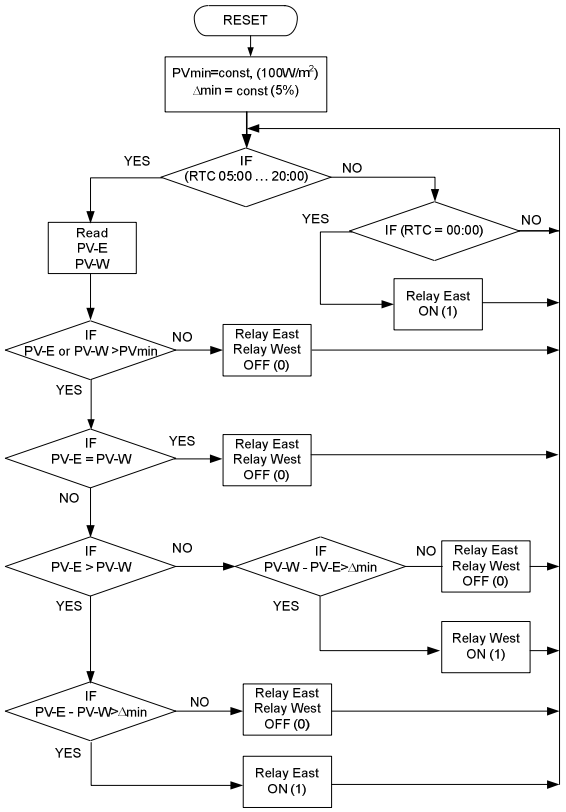

Fig. 4. Software Algorithm

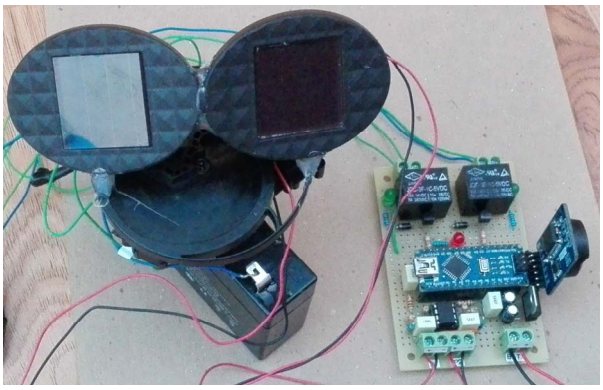

Fig. 5. Physical implementation

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Electronic scoring system - algorithm for microcontroller unit

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Abstract – **This report examines a system for electronic measurement and calculation of the coordinates of an object on a target and subsequent reporting of a certain result on the position of the object. It is a method of locating objects using sound receivers - TDOA (Time Difference of Arrival), a part of multilateration (MLAT) method used to locate mobile phones, civil aviation aircraft, locating military objects, and more. Also is presented a lightweight algorithm for calculating coordinates of the localized object based on measured times by sound sensors. An overview of the problems to be overcome is made. Suggestions for decisions were made allowing the implementation of the system into a real embedded project. A scheme for implementing the system has been proposed. The limitations of the measurement method in terms of practical implementation are defined and some ideas are outlined to minimize these limitations. The application of such systems is a training and training purpose, sports shooting equipment, applicable to other games using targets and requiring electronic reporting of the result.**
Keywords – **measurement, target, shell, bullet, automatic, positioning, coordinate, trajectory.**

I. INTRODUCTION

This report presents a system for measuring the coordinates of a target object based on a sound localization method. The method under consideration has been known since the Second World War. Over the years, this method has been used to locate distant sound generating objects. Their long distance reduces some of the time requirements to the measurement system. This is due to the fact that the sound receivers are located at longer distances, and the pulses generated at reception are vastly different, easy to measure with minimal schematic techniques.

The target can be of different materials. Depending on the accuracy of tracking and the measurement system applied, the material may be a tree (for a dart target or for a target used in archery) or metal (for small caliber - sport shooting, training shooting range and etc.). The only thing that must be known about such a system is the speed of sound propagation in the particular environment (or material) from which the target is composed.

The shape of the target is desirable to be round or square. Correct forms are preferable because of the easier setting of the exact coordinates of the receiving devices in the memory of the measuring system.

When a target object is hit, the sound propagates to the plate at a rate equal to:

$$c = \sqrt{\frac{E}{\rho}} \tag{1}$$

,where :

E = bulk modulus elasticity (Pa),

ρ = density (kg/m3).

In Fig. 1 is a schematic diagram of the ultrasonic measurement method, receivers are placed in points A, B, C and D. The minimum number of receivers required is three. When the bullet falls on the target, depending on the target material, the sound reaches all receivers for a different time.

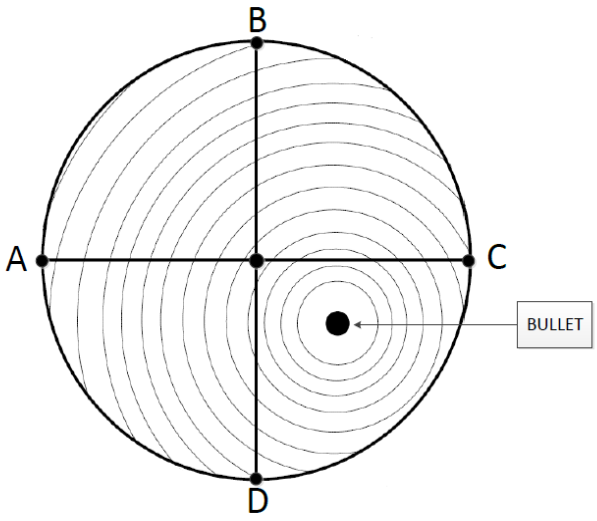

Fig. 1 – Principle diagram for ultrasound measuring system

In the specific case of Fig. 1, the wave will first reach point C, then reach point D, then point B, and finally end at point A. Based on this behavior of the system, it is possible to accurately measure the times between reports at different points and calculate their distances between the point and the points of the sensors according to the material and location of the receivers.

Table 1 lists several environments and the rate of distribution for the specific environment. This speed determines the necessary time quantum required for the calculations and must be consistent with the received signals from the receivers. Based on this velocity and the

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times measured by the system, the distances required for the method of calculating the coordinates are calculated.

Table 1 – Sound speed in different materials

medium	velocity (m/s)
Steel	4880 - 5050
Steel, stainless	5790
Titanium	6070
Wood (hard)	3960
Wood	3300 - 5000

The type of receivers used is determined by the desired sensitivity to wavelength and time-resolving ability in subsequent processing. It is possible to use simple microphones or pick plates based on the piezo effect. In all cases, the input signal must be filtered from low-frequency components and processed in a suitable way so that it can be fed to a discrete system. At different receivers, there are different features in designing system schematics.

At the moment of the object's impact on the target, ultrasound waves propagate into the target material, reaching the receivers for a different time. The time is in direct dependence on the coordinates of the target and the material from which the target is built. By measuring the time intervals between pulses from all receivers, and knowing the target size and velocity of the wave propagation in the target material, a very accurate TDOA (Time difference of arrival) . To solve this problem, the necessary and sufficient number of receivers is three, but for a more accurate measurement, a five-receiver algorithm is recommended.

Fig. 2 shows the timing of the signals generated by the four receivers. The time from targeting the target and the recording of the generated vibrations by the first sensor remains unknown. It is the basis for starting the time readings for the other sensors. The situation is judged on the basis of the remaining times and the known coordinates of the sensors located on the target.

We use the dependence that a plane is defined by three non-right points. The calculations are based on the theoretical equations derived for multilateration (MLAT) and TDOA (Time difference of arrival method). One of the problems of the method under consideration is that computing the exact coordinates of this method requires many calculations that will hamper an embedded system.

Multilateration (MLAT) is a monitoring technique based on the measurement of the time difference of transmission and reception of signals to two reception points with known coordinates. Unlike absolute distance measurements or angles, measurement of the difference in distance between two reception points results in an infinite number of hyperbolic curve reports that satisfy the solution of the measurement equation. To determine the exact location on this curve, multilateration is based on multiple measurements. A second measurement taken from a different pair of receive points will result in a second curve intersecting the first one. The intersections of these curves determine the number of possible places. In this way, a "fix" of the unknown position of the localized object is obtained.

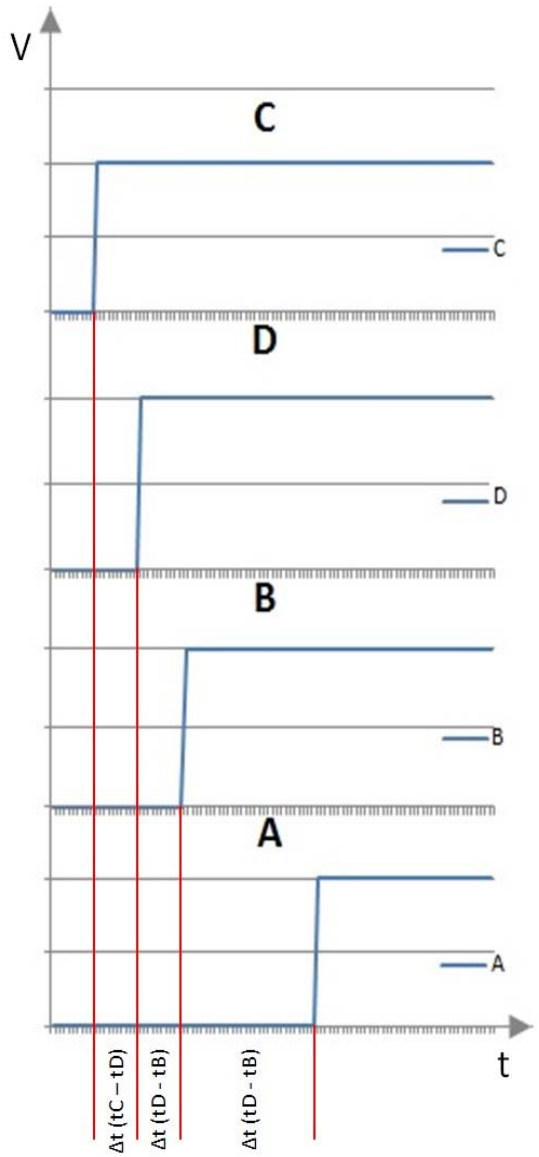

Fig. 2 – Timing diagram for reg. signals from the receivers

Multilateration is a common technique in radionavigation systems, where it is known as hyperbolic navigation. These systems are relatively easy to construct because there is no need for a common timer but for the difference in signal synchronization and is not critical to the synchronization of the measurement procedures of the sensor signals.

This forms the basis of a number of widely used navigation systems starting in the Second World War with the British Gee system and several similar systems introduced over the next few decades. [1]

The coordinates of the point of impact are given by the following expression:

$$\vec{S} = (x, y, z) \tag{2}$$

The coordinates of all receivers can be given as follows:

$$\vec{P}_0, \vec{P}_1, \vec{P}_2, ..., \vec{P}_N \tag{3}$$

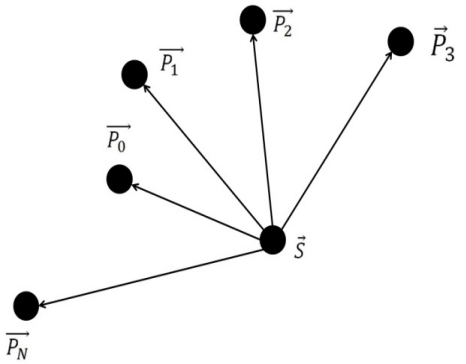

Fig. 3 – The abstract vectors about position calculating

The coordinates of all P points are known to us. The coordinates of the S point are unknown. On the basis of the measured times (the measurements of these times begin after contacting the first sound wave to the nearest receiver) and the dependencies described in the method, a calculation can be made and respectively the assumption of the exact coordinates of the point of attack.

$$R_0 = \sqrt{x^2 + y^2 + z^2} \tag{4}$$

The difference in the coordinates of the individual receivers and the object:

$$R_m = \left|\vec{P}_m - \vec{S}\right| = \sqrt{(x_m - x)^2 + (y_m - y)^2 + (z_m - z)^2} \tag{5}$$

The difference in the start point times (the first receiver is reached by the sound generated at the impact of the object with the shot) and the other receivers:

$$\Delta T_m = T_m - T_0 \tag{6}$$

From 1,2,3,4,5 and 6, the following equations can be derived:

$$\begin{aligned} 0 &= x.A_m + y.B_m + z.C_m \\ A_m &= \frac{2.x_m}{\gamma.\Delta T_m} - \frac{2.x_1}{\gamma.\Delta T_1} \\ B_m &= \frac{2.y_m}{\gamma.\Delta T_m} - \frac{2.y_1}{\gamma.\Delta T_1} \\ C_m &= \frac{2.z_m}{\gamma.\Delta T_m} - \frac{2.z_1}{\gamma.\Delta T_1} \\ D_m &= (\gamma.\Delta T_m - \gamma.\Delta T_1) - \frac{x_m^2 + y_m^2 + z_m^2}{\gamma.\Delta T} + \frac{x_1^2 + y_1^2 + z_1^2}{\gamma.\Delta T} \end{aligned} \tag{7}$$

The basis of the various implementations is the methodology for the rapid solution of all the equations. If all receivers are located in a single plane, the value of the third coordinate will become zero, and this may facilitate the algorithm, but it will only make it unified to calculate a point in the two-dimensional space.

II. Problem Formulation

The problems to be solved for the actual implementation of the project are several.

The first problem to be considered is the small spacing between the receivers and the high speed of sound propagation in dense materials.

The second problem to be solved is the reception of the signal generated by the impact of the object and its subsequent processing. Also a problem is the subsequent reflected sound waves inside the target structure. They should also be ignored and not affect the system. The last problem is the speed of calculation and optimization of the mathematical apparatus used to determine the coordinates. It is necessary to solve linear equations and it is relatively fast with the help of the embedded system. For this purpose, a suitable methodology should be selected and embedded in a MCU.

III. Description Of The Solution

The first problem to be considered is the small spacing between the receivers and the high speed of sound propagation in dense materials. In recent years, electronics have been developing at very fast pace and time measuring systems with operating frequencies above 10MHz are widely marketed. By choosing a suitable microcontroller, a suitable 32-bit timer and a high operating frequency of the system, this problem is practically resolved.

The problem of the speed of calculation and the method of solving the equations to determine the coordinates of the hit can be solved by matrix calculus by the Gaussian elimination method. Since the solution to the task must be implemented in a microcontroller language, with (8) an example of a short extract of a working code:

```
Am=(2*Xm/TMDm)-(2*X1/TMD1)
Bm=(2*Ym/TMDm)-(2*Y1/TMD1)
Cm=(2*Zm/TMDm)-(2*Z1/TMD1)
Dm=TMDm-TMD1-(Xm^2+Ym^2+Zm^2)/TMDm+(X1^2+Y1^2+Z1^2)/TMD1
```
(8)

In the example code, TMD is the product of the measured start time (touch with P0) to the point Pm, with the velocity of the wave propagation in the target medium. For all known coordinates, these coefficients are found (Am, Bm, Cm, Dm) and a matrix is formed with the values so obtained. Then with matrix calculus, we calculate the exact values. Matrixing in the embedded system is done with a library of a language-specific mathematical library.

For the correct operation of the system, it is necessary to solve the problem of receiving the signal generated by the impact of the object and its subsequent processing. Also a problem is the subsequent reflected sound waves inside the target structure. They should also be ignored and not affect the system.

The block diagram of the device is shown in Fig. 4. The first block has the function of filtering the input signal and protecting the whole circuit from high input voltages generated by external factors and/or ESD/EMC interferences. The second block is intended to process the analogue signal received at the input and to transmit a switching signal to the LATCH block. This block is realized with a comparator. The REF reference value sets the level at which to switch the comparator and generate a signal. The LATCH will work and keep its output level in one state until it is reset by the control block. In this way, the subsequent "false" generations are filtered by reflected sound waves inside the target structure. The output of the LATCH block is connected to a microcontroller input with a low-to-high switching function. So, when the controller enters a disruption for the first triggered channel, a timer can be started, and subsequent interrupts (generated by another channel) take the timer value, store it in a certain amount of memory and that is basis to calculate the time between the individual channels.

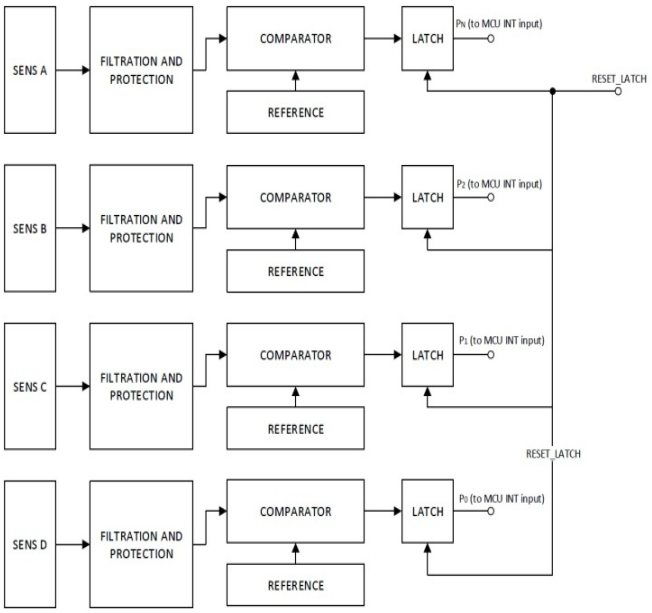

Fig. 4 – Block diagram of the scoring device

The last problem is the speed of computation and optimization of the mathematical apparatus used by us. This is determined by the need to solve comparatively fast equations by embedded system. For this purpose, a suitable methodology should be implemented in embedded MCU.
In recent years, many different and relatively inexpensive microcontroller offerings have come into the market to meet the needs of our system. And if the high operating frequency has been a problem before, then these problems are already solved and a system can be implemented to carry out this process.

III. CONCLUSION

This report examines a system for electronic measurement and calculation of object coordinates that have been targeted and subsequent reporting of a certain result to the position of the object based on the embedded system.

A method for locating objects via sound receivers - TDOA (Time Difference of Arrival), part of multilateration (MLAT) method is discussed. This method is widely used for locating phones, civil aviation aircraft, locating military objects, and more.

Also presented is a lightweight algorithm for calculating coordinates of the localized object based on measured times by sound sensors.

An overview of the problems that need to be addressed is made and suggestions are made to solve these problems.
The suggestions made allow the implementation of the system into a real embedded project.

A scheme for implementing the system has been proposed. The limitations of the measurement method in terms of practical implementation are defined and some ideas are outlined to minimize these limitations.

The application of such systems is a training and training purpose, sports shooting equipment, applicable to other games using targets and requiring electronic reporting of the result. Also, the method itself allows for an extended application range because the algorithm to solve this task is universal for almost all types of localization based on this principle.

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System for Multi-frequency Capacitance-Voltage Characterization

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Abstract – **Capacitance measurement at different DC voltage levels, different signal amplitudes and different frequencies, finds extensive application to qualify semiconductor and multiple-layered structures. Generally, the cost of such type instrumentation is in range of several thousand dollars and they are not very popular in the market. In present paper an approach of combining conventional measuring instruments and high-level programming environment is suggested in order to achieve system with complete functionalities for capacitance measurements.**

Keywords – **C-V measurement, Device characterization, LabVIEW, Virtual measurement system.**

I. Introduction

Capacitance measurements is widely used for semiconductor characterization, particularly in metal-oxide-semiconductor structures, bipolar junction transistors, III-V compound-devices, photovoltaic cells, micro-electro-mechanical systems, photodiodes, carbon nanotubes, and many others. Such measurements are used by semiconductor manufacturers for new materials evaluation, processes and circuits characterization. C-V measurements are extremely important for improving processes and device performance.

Using appropriate methodology, software and instrumentation a lot of material parameters of semiconductor devices can be derived. In wafer processes C-V measurements are used after some process steps as lithography, cleaning, etching, some depositions and metallization. After the full fabrication of the devices, C-V measurements are used for parameters characterization, such as threshold voltage, as well as modeling the performance of such devices. For example, in order to determine electrical characteristics of photo cells, characterization involve measuring the current and capacitance as a function of an applied DC voltage. This way, important parameters can be extracted using current-voltage and capacitance-voltage measurements, such as the maximum power output and the conversion efficiency in the cells.. The electrical characterization is also of great importance in order the losses to be assessed and the devices to be as efficient as possible [1].

Because of their specific application, capacitance measurement systems are not very widespread and are relatively expensive. In present paper is suggested a method that combine three conventional measuring instruments into one system for impedance parameters characterization.

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II. System Design and Mode of Operation

The base architecture of designed system for multi-frequency C-V measurement and analysis is shown in Fig.1.

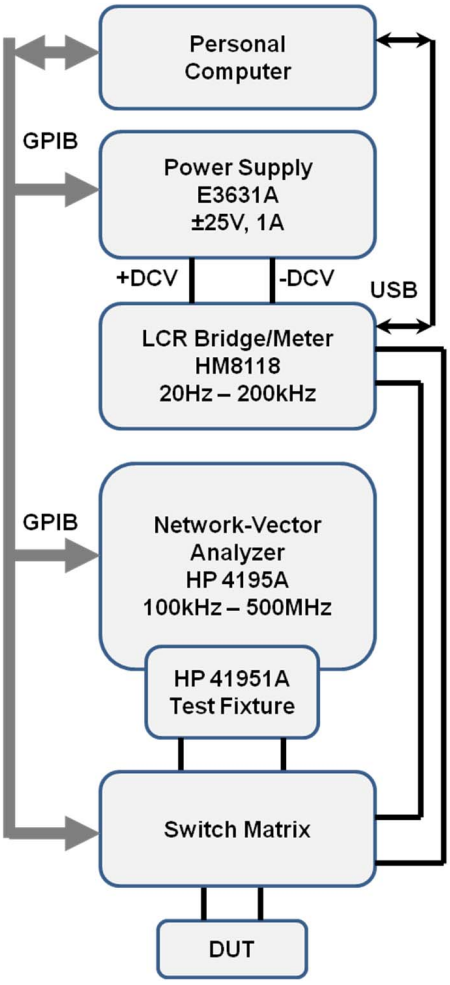

Fig. 1. Architecture of designed system for multi-frequency capacitance-voltage measurements.

The system consists of three autonomous instruments, switch matrix, personal computer and interfaces. For precise voltage and current source is incorporated programmable power supply E3631A from Keysight Technologies [2]. Measurement of impedance parameters in low frequency range (20 Hz - 200kHz) is achieved with LCR meter HM8112 from Rohde & Schwarz [3]. High frequency (up to 500 MHz) characterization of devices and structures is performed with the help of Vector Network Analyzer HP4195A from Keysight Technologies [4]. The system is controlled by personal computer and interfaces Universal Serial Bus (USB) and General Purpose Interface Bus (GPIB).

A key role to achieve system functionality is the graphical programming environment LabVIEW. In addition to control of instrumentation, this graphical environment also provides synchronization between measuring devices, as well as processing and analysis of results.

The designed system can be used in three different operational modes - Capacitance vs. DC Voltage, Capacitance vs. Frequency, and Capacitance vs. AC Voltage.

A. Capacitance vs. DC Voltage measurement

In this operational mode the main sweep is DC Voltage and for nested sweeps can be used frequency or AC Voltage. Many parameters of the semiconductor devices structures and materials can be obtained from the C-V measurements using appropriate tools and equations. For example, the carrier density could be estimated with the most common capacitance (C) measurements. Graphical representation of a $1/C^2$ - V plot is called a Mott-Schottky plot and is widely used to estimate the charge density distribution.

B. Capacitance vs. Frequency measurement

For Capacitance (Impedance) versus Frequency measurement the main sweep is frequency and for nested sweeps can be used DC or AC Voltage. This operational mode is also known as electrochemical impedance spectroscopy (EIS). Due to the fact that resistance and capacitance depend on the frequency, the single-frequency AC method can supply limited information parameters of the structure. When there is a perturbation in the steady-state system, for example an applied AC voltage it gets to a new steady state. The time taken for this relaxation is known as the time constant and when the relaxation process is analyzed, this will provide information for the parameters of the system or the structure. The transfer function is represented by the ratio of the response time to the perturbation.

Frequency response, known also as Nyquist plot can be used to estimate dynamic behavior of device under test. Particularly the Capacitance vs. Frequency characteristics are useful for corrosion studies, battery research, solar cells, bio-materials, ceramics, electronic component development, organic light emitting diodes (OLED), food quality control etc.

C. Capacitance vs. AC Voltage

In this mode of operation, the main sweep is voltage signal level, and for nested sweeps are used DC Voltage or frequency. This method is also known as drive level capacitance profiling (DLCP), and is used for deep defect densities determination by the non-linear response of the capacitor.

Key technical specifications of suggested virtual system for multi-frequency impedance characterization of electronic components and structures are summarized in Table 1.

TABLE 1. KEY TECHNICAL SPECIFICATIONS OF DEVELOPED SYSTEM

Function	Range	Basic accuracy
Frequency	20Hz to 500 MHz 20Hz - 200kHz	1mHz, 100ppm 69 steps 100ppm
DC Voltage bias	-40 V to +40 V -25 V to +25 V	10mV resolution ±(0,05%+20mV)
AC signal level	50m Vrms to 1.5 Vrms	±(5%+5mV)
DC Current level	0 to500mA	±(0.15%+4mA)
Measuring parameters	Cp-G, Cp-D, Cs-Rs, Cs-D, R-jX, Z-θ	-
Interface	USB and GPIB	-
Z measurement	0.01mΩ to 100MΩ 30mΩ to 30kΩ (f>200kHz)	0,1% 2%
C measurement	0.01pF - 100mF 10pF - 30μF (f>200kHz)	0.5% 2%
Sweep types	Linear, Logarithmic, Program, Partial	-

III. SOFTWARE DESIGN

The instrument control and data acquisition are achieved by sending appropriate commands and receiving measured data via serial or parallel interface. In general, all modern measurement devices have LabVIEW Plug and Play instrument drivers, which include all of its functionality [6]. Unfortunately, vector network analyzer HP4195A is relatively old fashioned instrument and hasn't instrument drivers. This necessitated the creation of additional LabVIEW applications for the needs of the presented project. The other problem in process of software development of the system is the difference between interfaces USB (for HM8118) and GPIB - Fig.1. Because there is no hardware synchronization between these two interfaces, in presented work software synchronization is suggested.

The pseudocode or informal description of the operating principle of implemented synchronization is presented in Fig. 2. The instrument drivers of two instruments - power supply E3631A and LCR meter HM8118 are separated in two different software threads. Each thread begins with initiating (Init) and completes with releasing of resources (Close). The drivers which generate commands for sweeping DC Voltage with E3631A and continuous measuring capacitance with HM8118 are placed in *While Loops* and *Case Structures*.

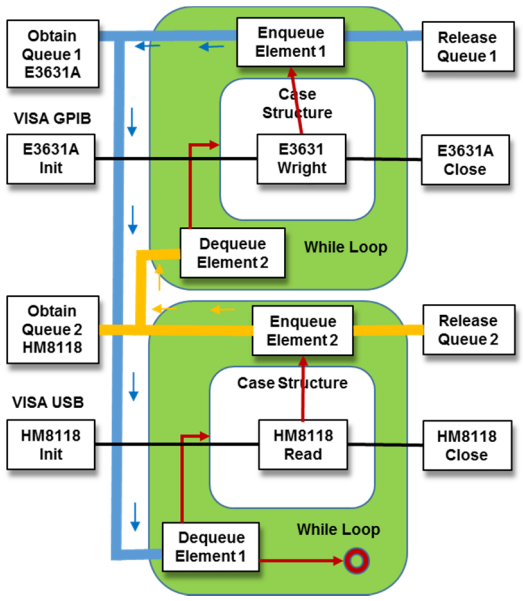

Fig. 2. Pseudocode describing synchronization between power supply E3631A and LCR meter HM8118.

Two measurement instruments synchronize its collaboration by exchanging messages via queues. The Queue 1 is handled by E3631 instrument driver, while the Queue 2 is maintained by driver of HM8118. When the DC Voltage increases with the programmed step, the instrument driver of E3631A enqueue message to driver of HM8118 to establish measurement. The driver of LCR meter dequeue message and just when the measurement of the capacitance (or other impedance parameter) is completed, this driver sends message to E3631A via Queue 2 to increase DC value with next step. If the measurement of capacitance failed, the message isn't send and DC Voltage does not change. The instrument driver of E3631 sends message again with last unchanged DC voltage value and this repeats until acceptable value of capacitance is measured or time out occurs. Thus it is impossible to achieve erroneous measured data for capacitance or to miss some of voltage steps.

The implementation of described method for synchronization in LabVIEW environment is shown in the block diagram of Fig. 3. In the figure two threads with instrument drivers for E3631 Power Supply (VISA resource GPIB0::5::INSTR) and drivers for HM8118 LCR Meter (VISA Resource RS232_USB) can be observed. Near to instrument drivers are placed queues for message exchange between the two instruments. The front panel of suggested virtual system for capacitance measurements is shown in Fig. 4.

IV. Experimental Results

A number of characteristics of various electronic components have been obtained with developed virtual measurement system. The aim of presented results is to illustrate the functionality of the system so any analysis of obtained data is not considered here.

Capacitance vs. DC voltage characteristics of low power photo panel are shown in Fig. 5. Behavior of photo panel up to 200kHz is tested with both instruments Agilent 3136A and HM8118, coupled in the system. For frequency above 200kHz HP4195A as single instrument is used. Above 400kHz the photo panel is already inductive and capacitance is unacceptable.

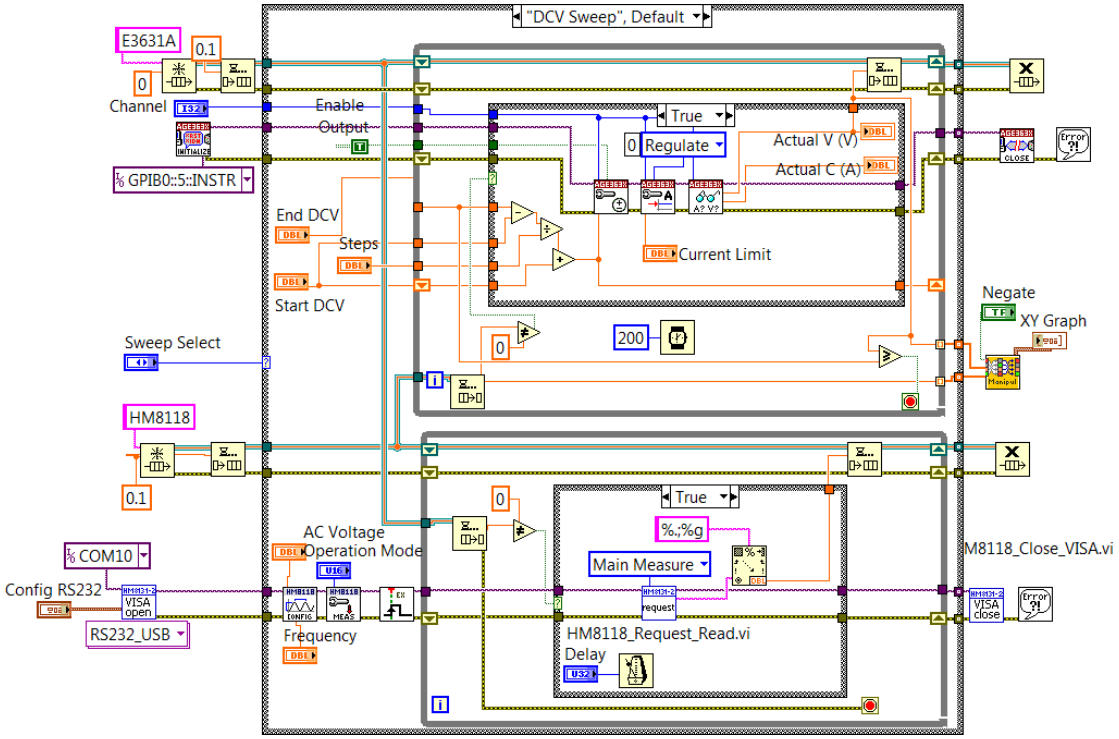

Fig. 3. LabVIEW block diagram for synchronization between power supply E3631A and LCR meter HM8118.

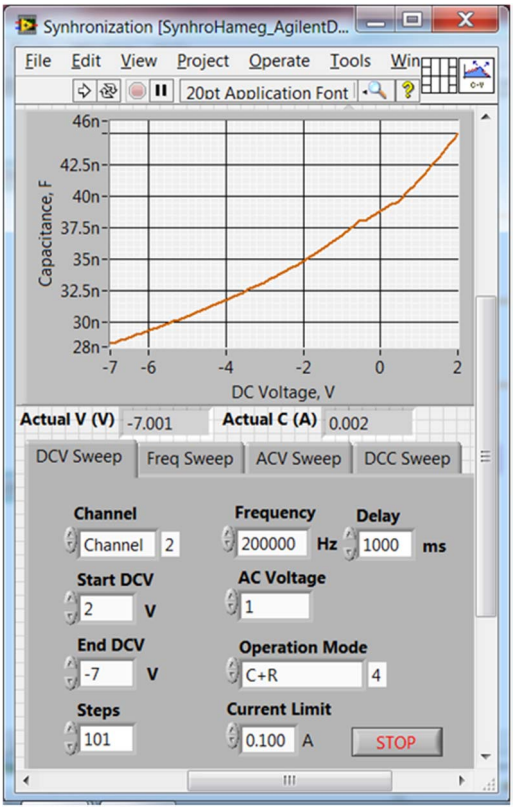

Fig. 4. The Front Panel of virtual system for multi-frequency capacitance – voltage measurement.

In Fig. 6 capacitance versus frequency characteristics of green colour light emitting diode are shown. The measurement is done for frequency above 100kHz and single instrument HP4195A is enough for this purpose.

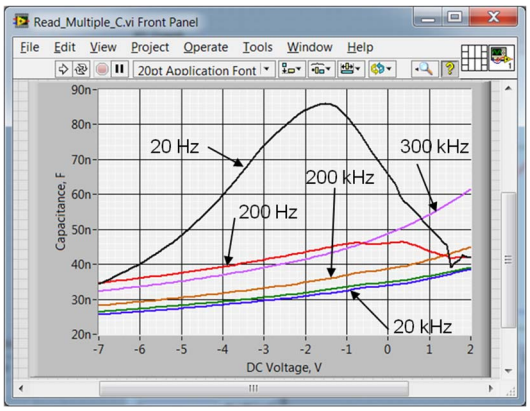

Fig. 5. Multi-frequency Capacitance - Voltage Characteristics of photo panel JW-8026B.

For illustration of capabilities of developed measurement system an AC Sweep from 0.6 Vrms to 1.2 Vrms with 7 MHz constant frequency and applied different DC Voltages are performed for green light emitting diode, as it is shown in Fig. 7. The capacitance of tested device increases twice when DC value is near the threshold voltage of the diode.

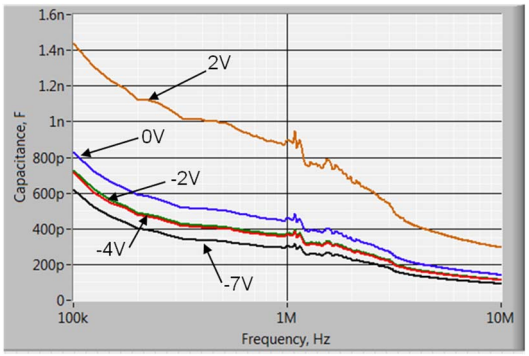

Fig. 6. Capacitance - Frequency Characteristic of green light emitting diode 560PG2D

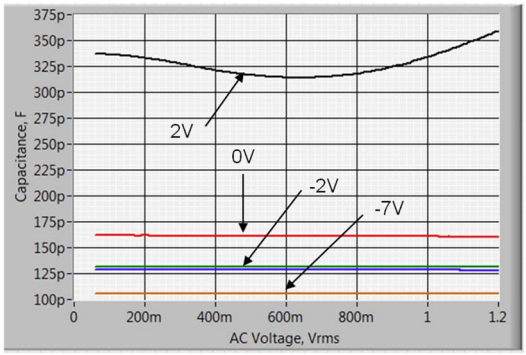

Fig. 7. Capacitance - AC Voltage Characteristics at 7MHz frequency of green light emitting diode 560PG2D

V. Conclusion

In the present work, an effective method is suggested which describes the possibility to construct measurement system with completely new functionality with conventional instrumentation and software

. The developed system allows measuring and researching various characteristic and parameters of electronic devices and structures such as oxide thickness, average and bulk doping, threshold voltage, interface trap density, serial resistance, etc. The presented virtual system is applicable for scientific researches as well as for educational purposes.

ACKNOWLEDGEMENT

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Cross-platform Sensor Networks

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Abstract – **The development of wireless sensor networks offers new challenges for engineers and scientists from different technological areas. The involving of various hardware and software platforms in the implementation and design of sensor node increases the capabilities of sensor networks. Also, cloud services provide effective network management and access to stored data, detected and measured by sensors in the sensor network. This paper presents an approach for developing heterogeneous sensor networks and connecting it with cloud services.**

Keywords – **Arduino, Cloud Platforms, Raspberry Pi, Sensor Networks, ZigBee**

I. Introduction

For many years sensors are connected to processing stations directly via local area networks, but recently a large number of sensors are going to communicate and collecting data wirelessly. Therefore, the wireless sensor nodes must have not only sensors, but also the possibilities for processing, manipulation and storage of data. The capabilities of sensor nodes in the networks can vary widely. Moreover, they can also differ in their communication capabilities. Modern sensor networks have main progress and are develops in two general trends: miniaturization and interconnection (networking). Often the sensor nodes need help to process and display the measured data, because of that they are small devices with limited memory and microcontrollers used for embedded devices. Nevertheless, such sensor nodes are permanently used in sensor networks, which consist of many different sensor nodes with arbitrary density, which collect data. Usually the collected data is sent to destination beyond borders of the local sensor network through one or more gateway. Also the multiplicity of applications of the sensor networks is remarkable. This paper presents the developed cross-platform sensor networks consisting of sensor nodes based on open source platforms such as Arduino and Raspberry Pi, connected via cloud platforms.

II. Cross-platform Sensor Networks' Architecture

The data collected by sensor nodes in a sensor network is typically propagated toward a gateway that links the sensor network with other networks where the data can be collected, analyzed and visualized. Figure 1 shows the architecture of the realized sensor networks working on different network standards. The figure also shows the interconnection between the sensor networks, the cloud services and the possible client devices. The client devices is used for management of the sensor networks or just for monitoring the data measured by the sensors, which previously was processed in the sensor nodes.

The sensor nodes are the central element in the networks. It is through a node that sensing, processing, and communication take place [1].

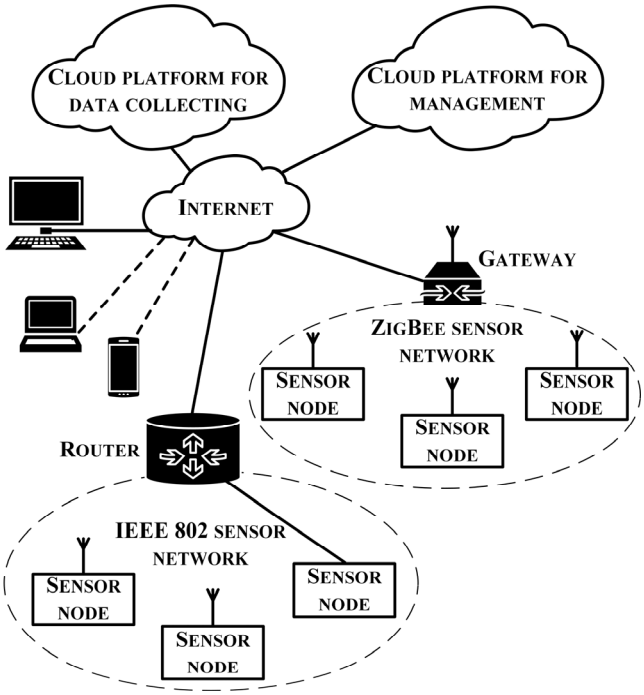

Fig. 1. Architecture of cross-platform sensor networks

It stores and executes the communication protocols and the data-processing algorithms. The physical resources available to the node influence the quality, size, and frequency of the sensed data that can be extracted from the network.

III. Sensors Nodes Architecture

While a Raspberry Pi has advantages like a built-in network connection or a graphical user interface, the lack of any analog inputs puts it at a disadvantage to microcontroller boards, such as the Arduino. Since the standard Arduino boards do not have ZigBee connectivity, the proposed option is the use of extension board, called shield. The shield boards can be placed on the top of the Arduino boards and extend the hardware features of the standard board. It can also be used an external component

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mounted on a breakout board, which are connected to Arduino board [2].

As example in this project are used sensors with digital-output. First one is module DHT22 which consists by a thermistor and a capacitive humidity sensor to measure the temperature and relative humidity (RH). The operating range for temperature is from -40 to 80 ^{O}C and from 0 to 100 % of relative humidity with typical temperature accuracy of ±0.5 ^{O}C and ±2 % for humidity. The sensor generates digital value with 40 bits in length. The first sixteen bits are the value for humidity, the second sixteen bits are for temperature, and the last eight bits are the checksum value to ensure an accurate read. The sensor module has sensing period of two seconds [3]. The sensor module is in factory compensated and calibrated and the calibration-coefficient is saved in type of programme in one-time programmable (OTP) EPROM. When the sensor is detecting, it will read this coefficient from memory, using its own protocol.

Other sensor used as example of implementation of cross-platform sensor network is temperature sensor TMP102 from Texas Instruments.

Actually, any sensor with digital output can be used in sensor nodes with minor change of connection and software. As appropriate sensors can be mentioned MMA7660FC 3-Axis Orientation and Motion Detection Sensor, MPL115A2 Barometric Pressure and Temperature Sensor both from NXP Semiconductors, TSL2561 luminosity sensor from Texas Instruments, L3GD20 three-axis digital output gyroscope from STMicroelectronics, SEN-10972 pH Sensor Kit from Spark Fun and many others. Additionally, in order to use analog sensors, Raspberry Pi can be equipped with external multi-channel analog to digital convertor (such as an MCP3004) but this requires considerable hardware and software effort.

IV. ACCESSING THE NODES

The Raspberry Pi 3 has a 1.2 GHz 64-bit quad-core Advanced RISC Machines Cortex Central Processing Unit and 1 GB RAM. Also the Pi 3 has an identical interfaces to the oldest models Pi 2 and Pi 1 Model B+ and therefore has compatibility with them. Because of this, the third party board add-ons are also compatible. As the Pi 2 model, the Pi 3 board has a set of 40 exposed pins for General Purpose Input and Output (GPIO) interface [5].

The most common operating systems for the Raspberry Pi are Linux-based operating systems and therefore there are a great number of Linux distributions available for the Pi. Raspbian is a free operating system based on Debian optimized for the Raspberry Pi hardware. The Raspbian distribution has many advantages over all of its predecessors. It is faster, it has more recent software, and it is more stable. On fig. 2 is shown the local access to measured data in Raspbian. The measurements of the sensors are made with the use of Python scripts. The running of the scripts is set automatically with the start of the system but also can be made manually from LXTerminal [5].

According to many sources, Ubuntu is the most popular deployed Linux-based desktop OS in the realm of software engineering [5, 6]. The MATE Desktop Environment is the extension of the default desktop environment on Unix and Linux OS GNOME 2. This means that MATE Desktop is very flexible for such applications. The environment uses traditional metaphors and semantics for Unix and other Linux-like operating systems. MATE is under continuous development to give opportunity for new technologies, while a traditional desktop experience is not changed. The default configuration for MATE consumes a lot of RAM (about 175 MB just for booting) of the total amount of RAM for Raspberry Pi 2 and 3 Model B boards, which is with size of 1 GB. Ubuntu MATE is alternative for computers that are not powerful enough to run a composited desktop as Raspberry Pi.

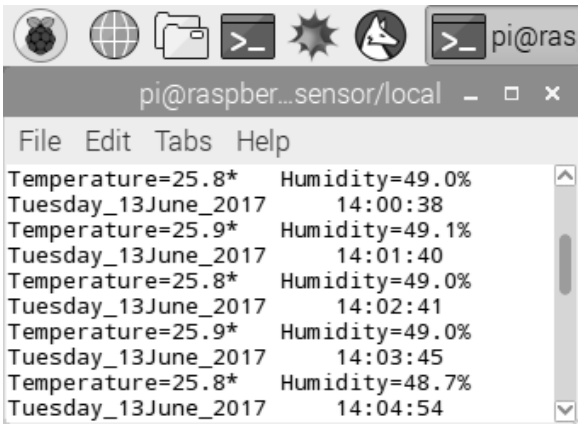


Fig. 2. Local visualization of measured data in Raspbian GNU/Linux

However while the experience is visually similar to the desktop edition of Ubuntu MATE, the underlying architecture is very different. As the Raspberry Pi is based on ARMv8 (ARMv7 for Pi 2) some packages for Ubuntu are not available to install, because they have been written and compiled for the i386 or amd64 architecture. The Pi boards not only needs an operating system but also needs firmware that controls their hardware on a low level. Another peculiarity of the environment is that the kernel is provided by the Raspberry Pi foundation like a firmware and the updates are not distributed via the Software Updater or via Advanced Packaging Tool (APT) command. Fig. 3 shows the local access to the measured data via Python scripts in Ubuntu MATE.

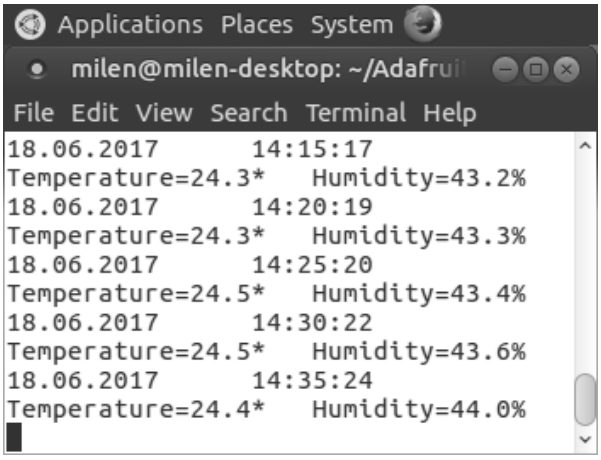


Fig. 3. Local visualization of measured data in Ubuntu MATE 16.04

The network connectivity of Raspberry Pi nodes is either via an Ethernet cable or by use an IEEE 802.11 n Wireless LAN [7]. The Raspberry Pi 2 uses its internal USB hardware for networking and due to this, there is no difference in networking performance between Raspberry Pi 3 and Raspberry Pi 2 with USB-to-WLAN adapter.

Fig. 4 shows the local access to an Arduino-based node in ZigBee sensor network.

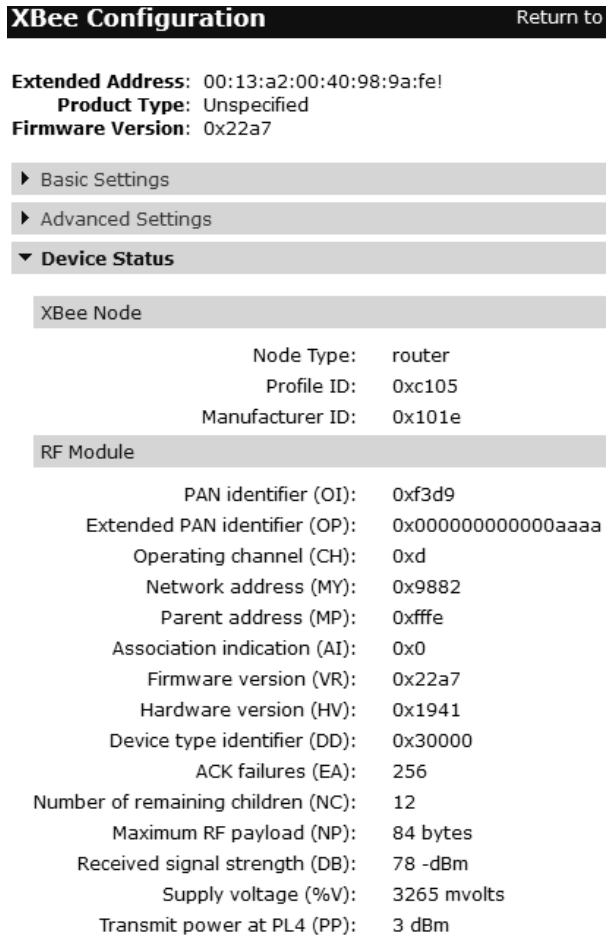


Fig. 4. Local device details of Arduino-based sensor node

Fig. 5 shows the remote access to Arduino-based node from ZigBee sensor network via cloud platform for management as Device Cloud platform by Digi®. The platform provides flexible management of the network and its nodes. [8].

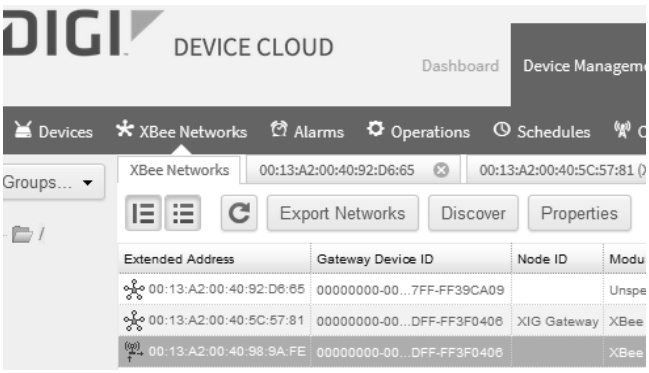
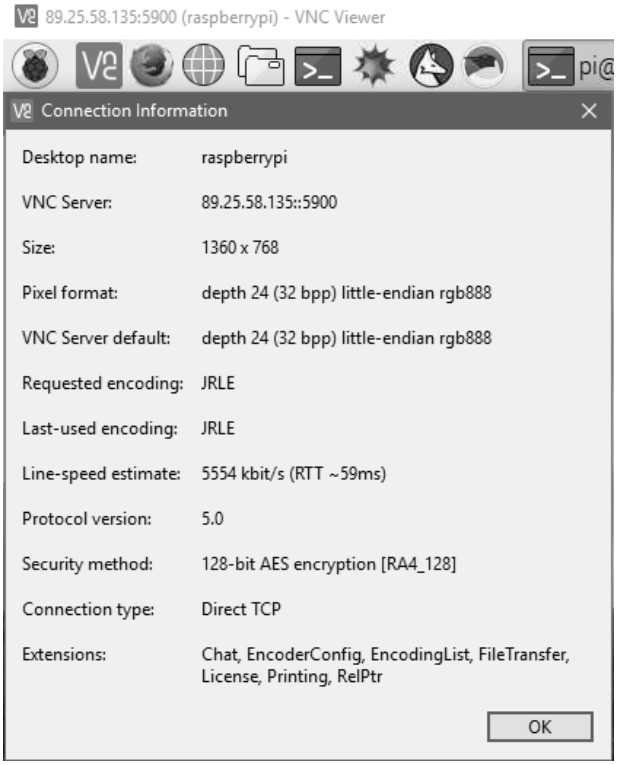
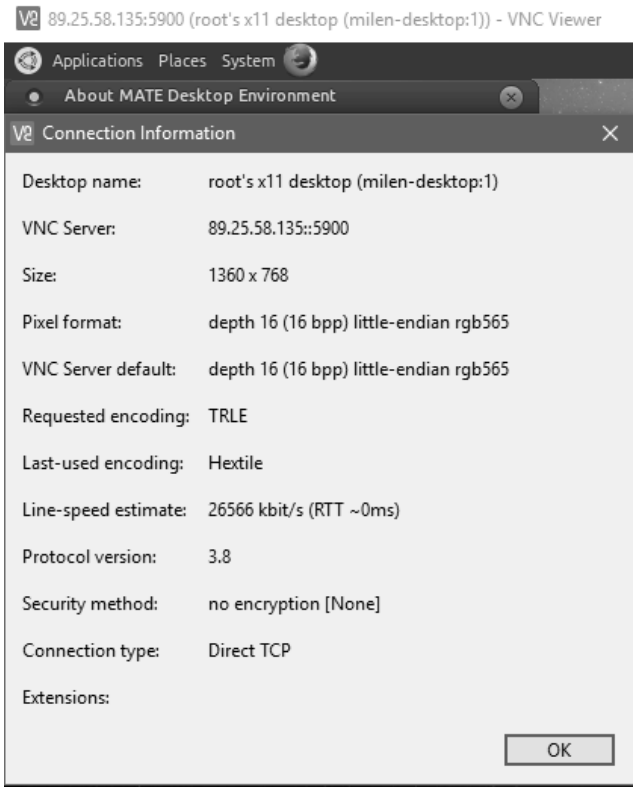


Fig. 5. Remote management of devices in ZigBee network

The remote access to the command line of a Raspberry Pi-based sensor node can be accomplished by using Secure Shell protocol (SSH) and SSH File Transfer Protocol (SFTP). On fig. 6 is shown remote access to sensor nodes running Raspbian GNU/Linux and Ubuntu MATE 16.04.



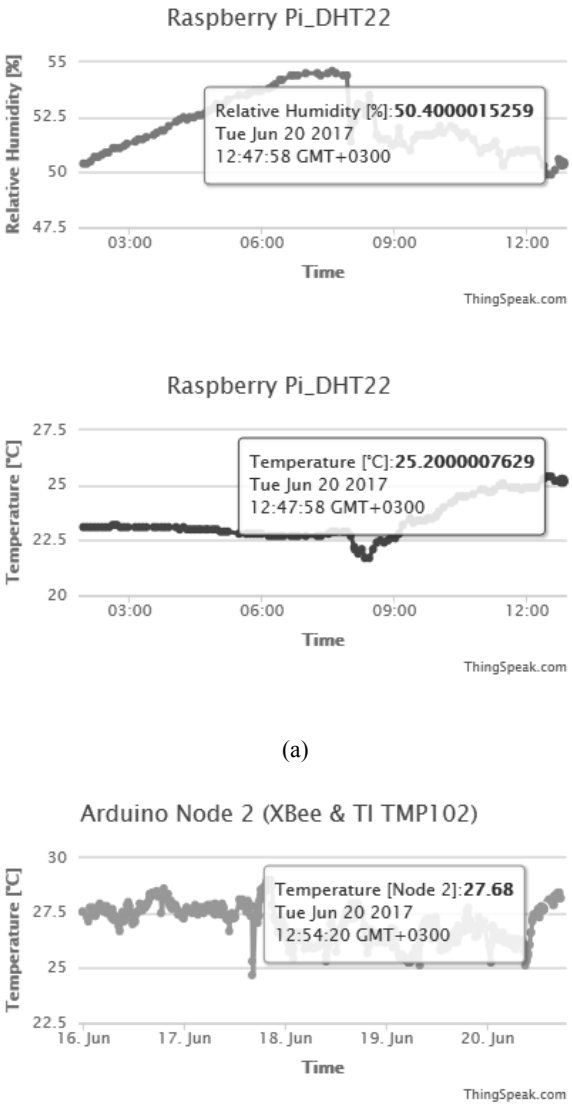
(a)



(b)

Fig. 6. Remote access to sensor nodes running: (a) Raspbian GNU/Linux, (b) Ubuntu MATE 16.04

SSH is a very common way of connecting remote hosts. Perhaps the only drawback is that it is a command-line rather than graphical environment. For remote access to the graphical user interface of Raspbian GNU/Linux and Ubuntu MATE, shown on fig. 6, is used Virtual Network Computing (VNC). VNC uses the Remote Framebuffer Protocol (RBF), which is a protocol for remote access to graphical user interfaces.



(a)

(b)

Fig. 7. Visualization of the measured data stored in the cloud using: (a) Arduino-based node, (b) Raspberry Pi-based node

Because it works at the framebuffer level, it is applicable to all windowing systems and applications. The remote endpoint must use RFB client or viewer, whereas the Raspberry Pi sensor node is running RFB server. Because RFB protocol has very few requirements of the client, clients can run on the wide range of hardware. Furthermore, a different client endpoint can be used to connect to the same sensor node. At the new endpoint, the user will have the same access to the graphical user interface as at the original endpoint. In effect, the interface to the Raspberry Pi-based sensor nodes becomes completely mobile [9]. A Remote Framebuffer server is usually a long-lived process that supports the state of a framebuffer. RFB clients customary connect and communicate with the server for a period of time to use and manipulate the framebuffer, then disconnect A subsequent RFB session will then pick-up where a main session left-off, while the state of the frame buffer intact. The display side of the protocol provides adaptive quality, because it is demand-driven by the client and the update of the framebuffer is only sent to the client from the server in response to a request from the client.

The measured data from each sensor node of both sensor network is sent to the cloud platform for data collecting – ThingSpeak™ [10]. Fig. 7 shows visualization of the stored data in the cloud using Arduino and Raspberry Pi platforms.

The platform enables the nodes to send its data to the cloud and to store it in a channel. After the data is sent to the channel of the cloud platform for data collecting, it can be analyzed, visualized, manipulated or interact with social media, various web services, and other devices.

V. Conclusion

The cross-platform sensor networks presented in this paper, explore the capabilities of interoperability sensor networks. In presented project, the sensor networks are made up of devices based on open source platforms such as Arduino and Raspberry Pi that are used for development of low-cost sensor nodes. The different properties of each platform are described in details. They are compared according to opportunities and advantages for organization of sensor networks with various applications. Moreover, the information from each sensor within the sensor networks is stored in cloud platform and it is accessible for visualization and further manipulation and analysis from different client devices with Internet connectivity.

Acknowledgement

This research is supported by Project № 171ПР0013-07.

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Design of a Portable System for Sensor Data Acquisition and Transmission

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Abstract –**The current paper represents a portable battery powered system which is capable to measure and analyze the data from different type of sensor data like humidity, air pollution gases, dust, smoke, etc. and send it via Bluetooth or GSM/GPRS connection to the remote devices. It contains GPRS modem with integrated Bluetooth module, integrated chip antenna, power management module, rechargeable Li-Ion battery and some analog or digital I/Os to connect to the internal or external sensors for data acquisition. This system may be used as a remote sensor system in smart homes, air monitoring stations, etc.**

Keywords– **data acquisition, Bluetooth, GPRS connection**

I. INTRODUCTION

The Internet of things (IoT) applications require data acquisition systems which are capable to measure, analyze, store and transmit the sensor data. These applications may be recognized such as motion control, security, door control, lighting control, environment monitoring [1], healthcare [2,3], smart infrastructure [4], etc. which utilize some wireless connection (RFID, Wi-Fi, Bluetooth, GPRS) to send the measured data to the remote server or cloud storage.

The requirements to the proposed systems are based on the device functionality such as small size, battery powered with recharge capabilities, data filtering and analysis. Also the system have to combine different types of communication devices such as short-range and long-range ones to ensure the continuous data transmission and long-term operation time during the sensor motion and data acquisition.

These requirements are fulfilled by using the latest communication chips which combine GSM and Bluetooth connectivity, micro SIM card integration and chip antennas.

II. SYSTEM DESCRIPTION

The block diagram of the system design is shown at Figure 1. It consists of GSM/GPRS modem with built-in Bluetooth module with micro SIM card, optional LCD display, alarm block (if the sensor data exceed some limits) and system microcontroller (μP) with general I/O ports which may be configured as analog or digital inputs/outputs depending of the sensor type.

The system connectivity is ensured by M66F as GSM/GPRS modem which supports Bluetooth interface, it is fully compliant with Bluetooth specification 3.0 and supports SPP (Serial Port Profile). It also features GPRS class 12 and is distinguished with an integrated TCP/UDP, FTP and PPP protocols. The current consumption is as low as 1.3 mA in SLEEP mode.

The portable size of the system and the best network coverage are provided by the integrated chip-antenna WE-MCA 7488910245 for the frequency range 2400-2500MHz (Bluetooth module) and external GSM antenna via female SMA connector. The chip antenna peak gain and average gain are equal to 3dBi and 1.0dBi respectively.

The system microcontroller is based on PIC16F family (PIC16F1825) andhas built-in I^2C interface as a part of MSSP module and EUSART w/auto baud interface, which is connected to the GSM/GPRS modem with RTS/CTS hardware flow control. The microcontroller oscillator scheme uses SMD (QFN) crystal at 16.000MHz as a low-profile resonator. The frequency tolerance is equal to approximately ±15ppm@25ºC.

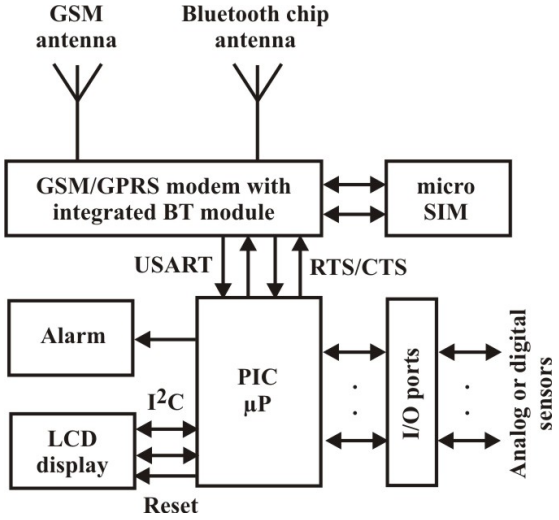

Figure 1. System block diagram

The optional LCD display may be connected to the system via I^2C interface of the microcontroller. This interface requires only 2 wires for data communication and 1 reset (optional) compared with the standard parallel interface LCD displays. As the LCD logic operates at 5V while the power supply voltage is equal to 3V, the external capacitors C2 and C3 are added for the internal voltage booster circuit (Figure 2). The LCD backlight is connected to the external power supply via the current limiting resistor. As the backlight consumption is approximately

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32mA@3,5V this connection example eliminates the current draw from the battery if the external power source is disconnected.

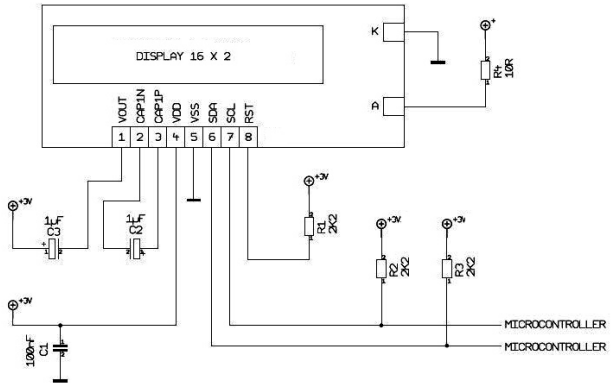

Figure 2. LCD display connection diagram

The power supply (Figure 3) is based on LDO (low-dropout) regulator BA00DD0WHFP with adjusted output voltage which may set in the range from 3.8V to 4.2V to power the GSM/GPRS modem. This chip has a high-precision output voltage of ±1% and may deliver up to 2A with maximum dropout voltage of 0.5V. It also is distinguished with a built-in over-current protection, over-voltage protection and thermal shutdown circuit. The LDO regulator is chosen to allow an USB charging or connection of solar power charging devices. The input maximum voltage is set to 25V with an absolute maximum value of 35V.

Therechargeable Li-Ion battery is used as a backup power supply and is supported by MCP73831T-2ACI/OT ICs as a Li-Ion charge management controller. The charging current is set via an external resistor and its maximum value is equal to 500mA. The power management chip employ a constant-current/constant-voltage charge algorithm and charge termination.

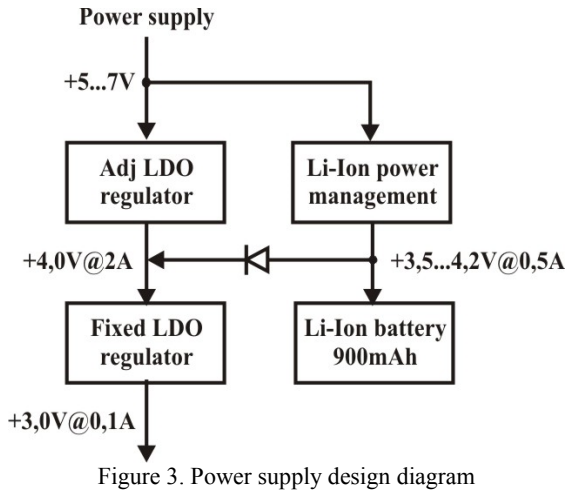

Figure 3. Power supply design diagram

If the main power supply is disconnected the system is powered by the Li-Ion battery via the Shottky diode (for example SS34) which also prevents the battery from the deep discharge. As the main power sources is restored the Li-Ion power management chip controls the battery charging process and the system draws the current directly from the external source. This allows to turn on the system immediately after power restoration regardless of the backup power status. This schematic also allows removing of the backup battery without system interruption.

III. System Test and Operation

The system components allocation on the PCB according to the block diagram from Figure 1 are shown at Figure 4.

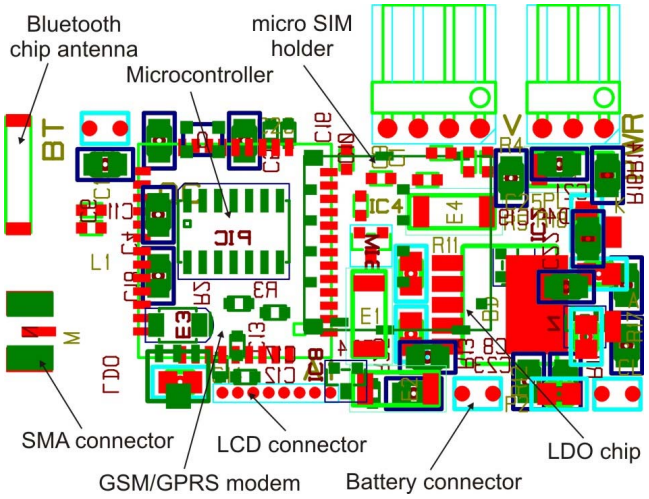

Figure 4. System component allocation

The proposed system is assembled and tested to transmit the data of the water-meter to the remote server with installed MySQL database (Figure 5).

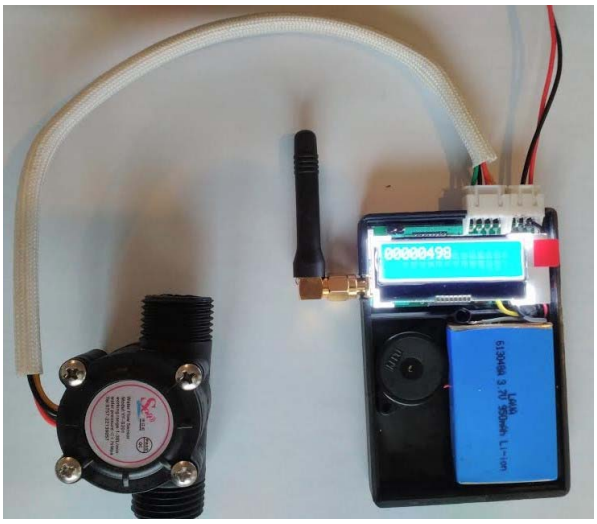

Figure 5. System connections

The water-meter output waveform is a square wave, the output frequency is defined as:

$$F = 7.5 * Q \text{ (L / Min) error: } \pm 2\%$$

The other water-meter specifications are:

- Supply voltage: 3.5-24VDC
- current consumption - ≤10mA@5V
- finished a liter of water flow pulse output – 450

The size of the whole system is compared with the coin to show the portable format of the device and this comparison is represented at Figure 6.

Figure 6. System size vs coin comparison

As the system is powered on by the external power sources from 5 to 7V, the LCD backlight is on and the Li-Ion battery is charged by the integrated Li-Ion power management chip (Figure 7). On the battery mode (when external power source is turned off) the LCD backlight is off but LCD display is still active and shows the measured data. The current state also may is transferred to the remote server and by Bluetooth link when the water-meter is mounted at hard-to-reach place.

As the LCD is an optional component the existing I^2C interface in the microcontroller may be used to connect other sensors to measure temperature, humidity, air pressure, etc. to build a portable air monitoring station.

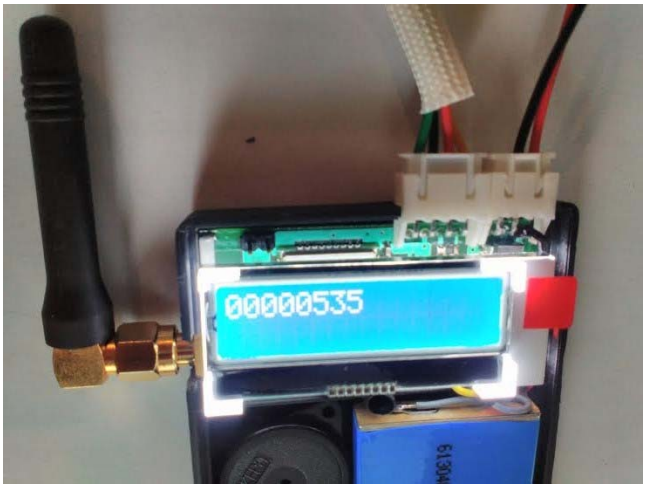

Figure 7. System working state

The measured water flow data, timestamp, network coverage indicator (RSSI) and ICCID number of the SIM card are sent to the remote server and are recorded in the MySQL table shown at Table 1, where pid an sid field denotes "packet id" (auto increment value) and "station id" respectively.

Table 1. MySQL data example

pid	sid	timestamp	rssi	flow	iccid
1227798	2000	2017-02-28 13:21:07	-55	1581	05000070836191
1227836	2000	2017-02-28 13:26:09	-51	1581	05000070836191
1227867	2000	2017-02-28 13:31:11	-51	1581	05000070836191
1227923	2000	2017-02-28 13:36:14	-51	1581	05000070836191
1227961	2000	2017-02-28 13:41:16	-51	1581	05000070836191
1227988	2000	2017-02-28 13:46:19	-55	1582	05000070836191
1228023	2000	2017-02-28 13:51:22	-51	1582	05000070836191

IV. Conclusion

The proposed data acquisition system is built to satisfy the IoT requirements of small size and battery powered device which may read, analyze, store and send the data via Internet to the remote server or to the nearby user via Bluetooth link.

The different microcontroller interfaces allow connections of various kind of sensors – analog or digital (PWM, pulse, I^2C, etc.) to made the system very flexible to the sensors output.

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A model for reverse electrowetting with cost-effective materials

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Abstract – **This paper, presents a model to predict the energy output from reverse electrowetting energy harvesting system with use of cost-effective materials. Reverse electrowetting on dielectric allows energy to be harvested from spontaneous aperiodic mechanical movements, where conventional energy harvesting approaches are not suitable for due to low energy conversion efficiency and frequency .**

Keywords – **reverse electrowetting-on-dielectric, REWOD, energy harvesting, aperiodic mechanical movements**

I. INTRODUCTION

Transformation of environmental to electrical energy is known as energy harvesting. The notion of energy harvesting dates back centuries ago, especially conversion of the energy from mechanical movement and wind. In recent years, a lot of scientific studies are focused on methods to convert mechanical vibrations and vibration-induced jitter to electrical energy [1]–[4]. However, the developed methods i.e. piezoelectric and electromechanical, have small energy conversion efficiency [5]. This limits the use of mechanical energy harvesting solutions mainly to devices with low consumption. In addition, piezoelectric harvesters are not suitable for vibrations with low frequencies (bellow 40 Hz) and are tightly coupled to the resonance frequency, which makes them unsuitable for harvesting energy spontaneous aperiodic movements.

Recently, the scientific community drew its attention to an interesting usage of a century old phenomenon i.e. electrowetting (EW) [6]. The traditional use of EW include micro- and nano-fludics, variable focal length control and electronic displays [7], in contrast the reverse electrowetting-on-dielectric (REWOD) [8] enable design of mechanical energy harvesting system with high conversion efficiency, high power density at low-frequencies of mechanical vibration over a wide range of actuation frequencies. For example in [8] designed and realized energy harvesting devices able to capture mechanical energy with frequency between 0.5 Hz and 350 Hz with energy conversion efficiency up to 75 %. To achieve this, the authors employ a complex set of technological processes to deposit a thin-film hydrophobic layer, with thickness in the range of tens of nanometers, and rare materials.

This paper presents a mathematical model of mechanical energy harvesting system based on reverse electrowetting-on-dielectric constructed with accessible and cost-effective materials. The model will predict the ability of the proposed system to convert mechanical vibrations to electrical energy.

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II. REWOD'S MODEL AND EQUATIONS

The electrowetting phenomenon is defined as "the change in solid-electrolyte contact angle due to an applied potential difference between the solid and the electrolyte" [9]. Consequently, the reverse electrowetting is when external mechanical actuation causes a change in capacitance between electrode and dielectric and the excessive charges flow throughout the load. The concept behind REWOD is shown on Fig. 1, the liquid droplet is placed between electrode and dielectric layer covered with hydrophobic layer. The electrode and dielectric layer are connected to external bias voltage and the load. As the electrode moves the droplet change its area and thus changes the capacitance and if the external bias is held constant excessive charges flow in the load.

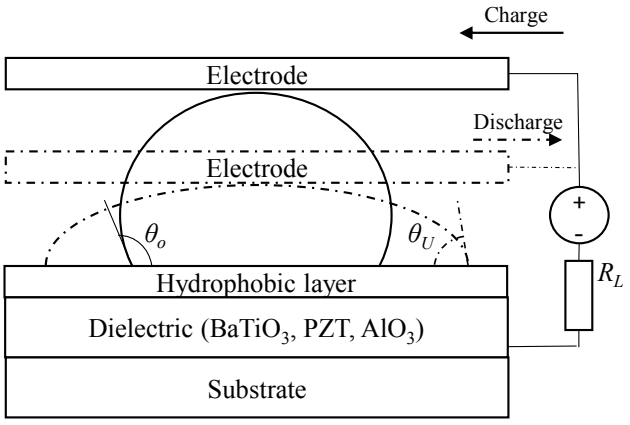

Fig. 1 Electrowetting operation principle

The classical description of contact angle (without external voltage) is defined in Eq. 1

$$\cos\theta_0 = \frac{\gamma_{sa} - \gamma_{sl}}{\gamma_{la}}, \qquad (1)$$

where γ_{sa} is the interface tension between solid and air, γ_{sl} is the interface tension between solid and liquid and γ_{la} is the interface tension between liquid and air. The values of interfaces tensions depend on the used materials for liquid, dielectric and surrounding environment (in the presented case - air) and temperature.

The capillary free energy E_{cap} is given by the Young equation,

$$E_{cap}(\theta) = A_{sa}\gamma_{sa} + A_{sl}\gamma_{sl} + A_{la}\gamma_{la} - V\Delta P, \quad (2)$$

where A_{sa} is the area of solid/air interface, A_{sl} is the area solid/liquid interface, and A_{la} is the area liquid/air interface, V – liquid droplet volume, and ΔP is Laplace pressure. Thus, E_{cap} depends on ΔP, as shown Eq. 1 and 2, given the constant temperature and droplet volume.

Laplace pressure ΔP is the differential pressure between the outside and the inside of a curved surface, i.e the outside and the inside of a liquid droplet, and depends on both the surface tension and the geometry of the droplet. ΔP is given by the Young-Laplace-Gauss equation,

$$\Delta P = \gamma_{la}\left(\frac{1}{r_1} + \frac{1}{r_2}\right), \quad (3)$$

here r_1 and r_2 are the main radii of curvature of the liquid droplet.

When external voltage is applied, the contact angle is described with Young-Lippmann equation,

$$\cos\theta_{YL}(U) = \cos\theta + \frac{\epsilon_0\epsilon_d}{2\gamma_{la}d}U^2, \quad (4)$$

where ϵ_d is the relative permittivity of the dielectric layer, ϵ_0 is relative permittivity of vacuum and d is width of the dielectric layer.

The total energy $E_{el}(\theta, U)$ is a sum of capillary energy $E_{cap}(\theta)$ and electrical/electrostatic energy $E_{el}(\theta, U)$,

$$E_{tot}(\theta, U) = E_{cap}(\theta) + E_{el}(\theta, U), \quad (5)$$

Yet, the electrical/electrostatic energy $E_{el}(\theta, U)$ depends on the total capacitance of the system $C_{tot}(\theta)$ and the external applied voltage U, given by,

$$E_{el}(\theta, U) = -\frac{C_{tot}(\theta)U^2}{2}, \quad (6)$$

where the total capacitance $C_{tot}(\theta)$ is approximately given by,

$$C_{tot} \approx \frac{\epsilon_0\epsilon_d A_{ld}}{d} \quad (7)$$

If the Laplace pressure is changed, as shown on the Eq. 1-6, then the area liquid-dielectric will be changed and consequently the C_{tot} will be changed and if the constant external voltage is assumed then the excessive charges will flow throughout the load. Equations 1-6 show the transformation of the mechanical energy to electrical energy through a REWOD phenomenon.

III. Results and Discussion

A. Model Verification

The Eq. 1-6 are codded in Matlab where ΔP is parametrized. Consequently, both the droplet main radii r_1 and r_2 and the capacitance C_{tot} are calculated in order to predict the energy output the REWOD system.

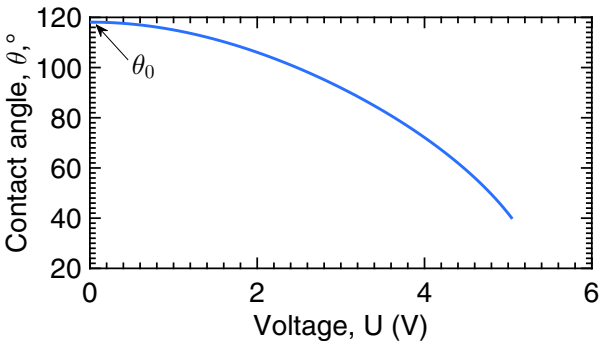

Fig. 2 Contact angle saturation model

The behaviour of the contact angle when external voltage is applied is shown on Fig. 2. The presented model exhibits identical behaviour as theoretical results given in [10]. The parameters of the model are: i) droplet volume – 50 µL, ii) thickness of the dielectric layer – 0.1 µm, iii) permittivity of the dielectric layer – 2.67, iv) permittivity of the liquid – 80, v) dielectric/air surface tension – 12.7 mN/m, vi) liquid/air surface tension – 72.8 mN/m, vi) liquid/dielectric surface tension – 47 mN/m.

Furthermore the verification of the presented model is conducted against the experimental results found in [8]. Both the theoretical model predictions of the presented model and experimental results are shown on Fig. 3. The calculated root-mean-square-error is 10.93 % or 5.04 nJ mm^{-2}, which is satisfactory result for the closeness of the proposed model with experimental data.

The standard deviation of the model i.e. root-mean-squared-error is calculated as follows,

$$RMSE, \% \approx \sqrt{\frac{\sum(E_{calc} - E_{exp})^2}{k}} \cdot \frac{100 \cdot k}{\sum E_{exp}}, \quad (8)$$

where E_{exp} is data from the experiment and $k = 6$ is the number of experiment data.

Experimental setup in [8] is as follows, a single mercury droplet with area of 1 mm2 is placed over the Cytop [11], a thin-film fluoropolymer. The Cytop, is deposited on top of tantalum pentoxide (Ta2O5) with thickness tens of nanometers and permittivity of 50. The Ta2O5 is coated with Cytop a to mitigate surface charge trapping. Mercury has a permittivity of 1.00074 and the capacitance of the plates, where droplet is placed is 16 nF cm-2.

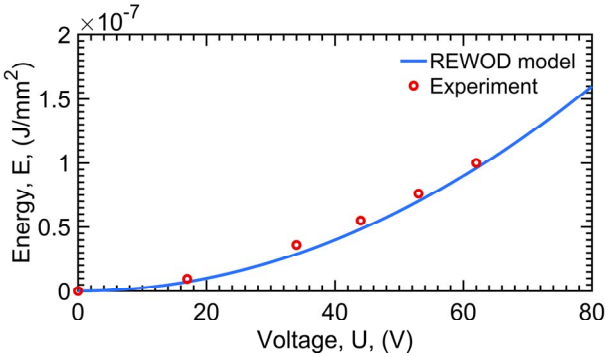

Fig. 3 Electrical energy per cycle per mm2, mercury droplet on cytop dielectric

B. Barium titanate REWOD model

The presented experimental configuration yields a high-power at a small scale, but to achieve this, one needs a rare materials and precisely controlled technological processes. However, to achieve cost-efficiency and scalability one would trade the energy conversion efficiency and power density for use of abundant materials and processes. In order to achieve that, this paper theoretically study use of two distinct REWOD setups. First setup uses a barium titanate ($BaTiO_3$) as a dielectric and second lead zirconate titanate ($Pb[Zr_xTi_{1-x}]O_3$). For both setups first the energy for one cycle is calculated and for stack of 50 droplets..

The stack consist of $BaTiO_3$ covered with thin layer of paraffin [12], droplet of water with NaCl and electrode, the detailed parameters of the stack are shown in Table. 1. As the $BaTiO_3$ dielectric constant is highly dependent on the particle size [13], ranging from 150[1] to 5000[2], the combined dielectric constant of 254 is used throughout the model.

TABLE 1. BARIUM TITANATE REWOD MODEL

	Material	Property	Value
Dielectric	$BaTiO_3$	Thickness	1 µm
		Permittivity	200
Hydrophilic layer	Paraffin	Thickness	0.2 µm
		Permittivity	20
Droplet	Water with NaCl	Volume	5 µL
		Permittivity	78.9

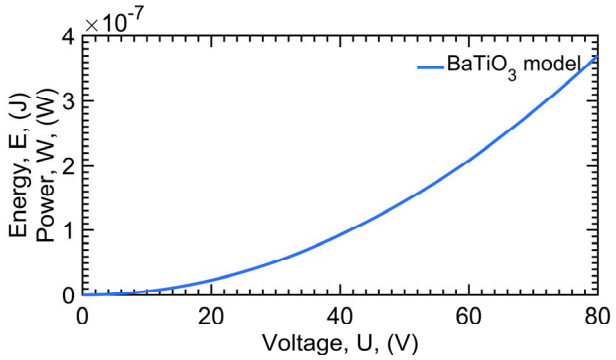

Fig. 4 Energy generated per cycle, power at 1 Hz oscillation

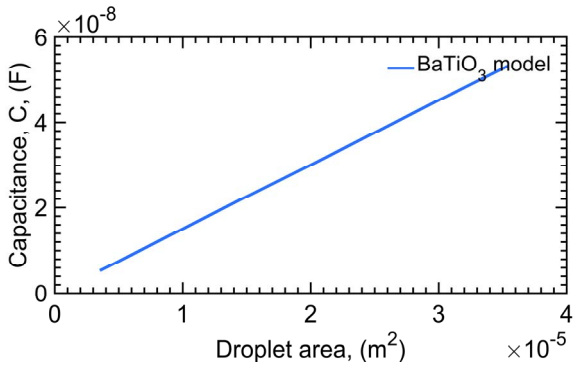

Fig. 5 Capacitance of the REWOD BaTiO3 model

Fig. 4 shows the electrical energy generated from single droplet of one cycle or power generated from mechanical actuation with frequency of 1 Hz. The generated electrical energy is highly dependent on the capacitance Eq. 6, and as a result the capacitance is dependent on the droplet area shown in Fig. 5.

The energy generated from one cycle for a voltage at saturation contact angle from the proposed setup with 50 droplets will be 12.23 µJ.

C. Lead zirconium titanate

Table 2 shows the parameters used for REWOD model with lead zirconium titanate, $Pb[Zr_xTi_{1-x}]O_3$, PZT [14]. The calculations are performed for stack consisting of PZT, droplet of water with NaCl and electrode, the detailed parameters are presented in Table 2. The total dielectric constant, used throughout the calculations, of the stack of PZT and paraffin is 245.

TABLE 2. LEAD ZIRCONIUM TITANATE REWOD MODEL

	Material	Property	Value
Dielectric	PZT	Thickness	1 µm
		Permittivity	290
Hydrophilic layer	Paraffin	Thickness	0.2 µm
		Permittivity	20
Droplet	Water with NaCl	Volume	5 µL
		Permittivity	80

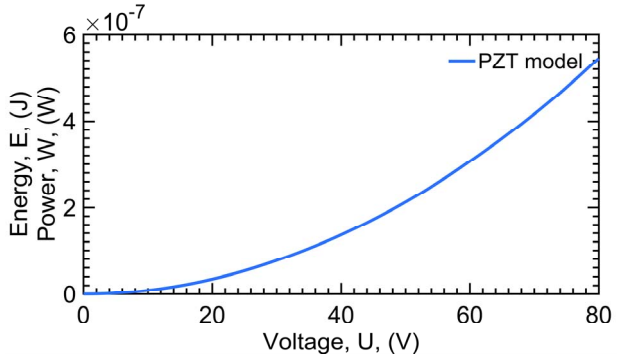

Fig. 6 Energy generated per cycle, power at 1 Hz oscillation

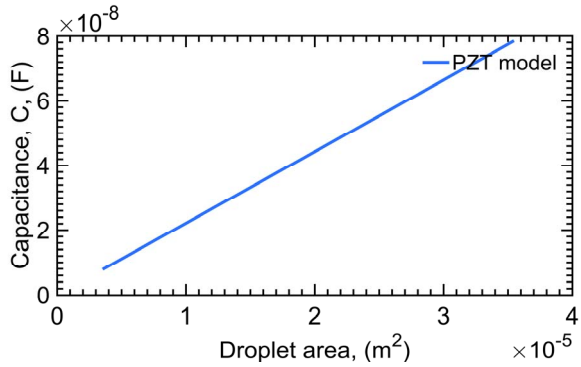

Fig. 7 Capacitance of the REWOD PZT model

[1] When the particle size is <100 nm [15]
[2] When the particle size is 0.8 µm [16]

The electrical energy generated per cycle is shown on Fig. 6 and dependence of the stack on droplet area on Fig. 7. The generated energy for the setup of 50 droplets at external voltage at contact saturation angle is 16.62 μJ.

D. Discussion

The energy generation from REWOD is a straightforward process with intricate balance between material properties, physical dimensions and external circuitry. The electrical energy density is highly dependent on the capacitance between electrode and dielectric, as shown on the Eq. 6. The capacitance itself is proportionally dependent on the droplet area and inversely proportional to the thickness of dielectric layer. Increase of the dielectric thickness will decrease the generated energy due to the decrease in total capacitance Eq. 7.

Another aspect of capacitance is permittivity of the dielectric, the higher the permittivity, the higher capacitance. However, increasing solely the permittivity of dielectric will decrease contact angle saturation and area of the droplet. In order to achieve higher energy density, the higher capacitance is needed, so higher droplet area and thinner dielectric layer with careful consideration of the permittivity of the dielectric.

Frequency behaviour and losses in scaling of the REWOD system with more droplets I parallel is another subject. Both will increase the energy output and make it useful for post-processing and storing. However, the presented model does not explicitly include the frequency behaviour, due to the fact that additional loss mechanisms are at play. The presented model allows only some rough calculations when taking into account frequency and scaling.

IV. Conclusion

The model presented in this paper, describes the behaviour of the energy generation from reverse electrowetting phenomenon. REWOD allows energy to be harvested from spontaneous aperiodic mechanical movements, which conventional energy harvesting approaches i.e. piezoelectric and electromechanical. REWOD is easily scalable, which in turns will increase energy output.

The presented $BaTiO_3$ and PZT setups with 50 droplets prove to harvest 12.23 μJ and 16.62 μJ respectively. When this is scaled with higher frequency and optimized geometrical shapes it would be enough the be powered with human locomotion and spontenous aperiodic mechanical actuations.

V. Acknowledgement

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Some Peculiarities when Interfacing Resonance Tactile Array Sensors

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Abstract – **Tactile resonance sensors are characterized with high sensitivity [1] but their physical principles often place restrictions over the operational modes and the format of the obtained data. The current work is concerning itself with the interfacing particular resonance piezoelectric sensor array structure as the inherent features are explored for improving the sensor workings. An interface schematics and specific scanning method are discussed.**

Keywords – **tactile sensors, interface, standing waves, operational mode**

I. Introduction

Generally piezoelectric resonance structures possess very high sensitivity [1] which is based upon the strong connection between their innate resonance frequency and the applied acoustic load. Changes in the load are ought to bring changes in the frequency on which the system is oscillating (or trying to) and concurrently lead to the change in the output electrical signal amplitude.

The aforementioned changes in the frequency and the amplitude can be used for determining the degree of external influence and the outline of the object that is causing the disturbance as well as the vector of the applied force. In other words the form of tactile image can be acquired with help of the piezoresonance structures.

II. Exposition

A. Resonance Piezoelectric Array

Piezoelectric sensor array means piezoelectric substrate on which multitude of sensor points are made with the help of specialized electrodes, thus the multitude of sensing points makes the sensor array field. In the case of resonance piezoelectric structure every sensing point is in fact a quasi-separate resonator as the separation can be achieved in most cases with the polarization vector of the piezoelectric substrate.

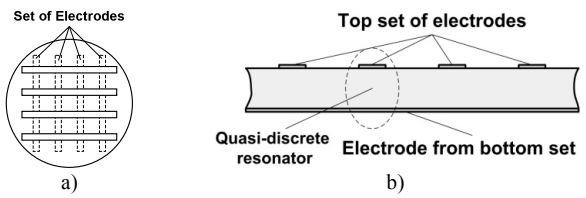

Fig. 1. Electrode configuration forming the piezoelectric array

In the current case the substrate has polarization vector along the Z axis leading to the excitation of thickness waves in the piezoelectric substrate when sinusoidal signal is supplied to the electrodes.

The optimal configuration for forming an array structure considering the wiring complexity is a system of two sets [2] of evenly spaced, parallel straight electrodes which are perpendicular to each other and are formed on the flat sides of the regular disk (Fig. 1,a) or plate [2] from piezoelectric material and which are centered relatively to one another. The sensing points are formed in the location of electrode crisscrossing from both sets (Fig. 1,b) as these points are indeed resonators which can be excited and scanned for data retrieval.

B. Scanning Methods for Resonance Mode

Such type of resonance piezoelectric structure can be scanned by two methods – namely a method that detects the frequency shift and a method that utilizes the amplitude change as both of them are based on the same principle. Assuming that the mass of the piezoelectric medium is constant value, the external load for every sensing point is determined according the piezoelectric effect principles [1] using the following equation [2, 3]:

$$\frac{\Delta f}{f_0} \approx \frac{i}{\pi Z_q} \frac{-\omega^2 u_0 m}{i\omega u_0} = -\frac{2f}{Z_q} m \,, \qquad (1)$$

where:
u_0 – signal amplitude;
m – mass;
f_0 – resonance frequency;
Δf – frequency shift;
Z_q – acoustic impedance of the material.

The method utilizing the frequency shift is extremely precise [1] as it implements measurements of the exact frequency at given sensing point as the difference between the innate resonance frequency and the measured one is indication for the load state. As it is not concerned with the signal amplitude there is no need for complex specialized signal preprocessing circuitry, although the difficulty lies in choosing and implementing a method for frequency recognition. These methods can vary from classical impulse-counting to properly adjusted variations of pitch detection algorithms. The parallel data processing for all of sensing array points would require undue hardware costs and in practice the serial mode of scanning is preferable [1] – the array is scanned one point at time as only one resonator is active in given time period. This also prevents the interference between multiple resonators working simultaneously and decreases the possible measurement error.

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But this excludes the possibility for real time working of the sensor system and significantly reduces the ability to respond in case fast, dynamically changing external loads are present. In those cases more appropriate is the usage of amplitude change method which can be easily configured to use parallel scanning algorithms.

Thus even if the real time mode is not obtained the reaction time of the system will be improved. The amplitude method may require specialized preprocessing circuitry but after that the signal can be supplied directly to analog to digital converter (ADC) in the simplest circuit solution.

C. Resonance Piezoelectric Array

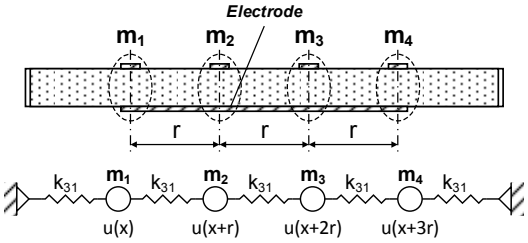


Fig. 2. Representing the array row

Model for amplitude method is shown on Fig. 2 as the one row of the array structure is represented as connected resonators that interfere with each other. If the different resonators are considered as equally weighting objects with similar geometric structure then the following matrix equation will describe the "dislocation" of the resonators:

$$M\frac{d^2u}{dt^2}+Ku=0\,, \tag{2}$$

where:

M – matrix of the masses;

K – matrix of the stiffness.

Then for one of the array rows the following can be written down:

$$\begin{bmatrix} m_1 & 0 & 0 & 0 & \cdots & 0 \\ 0 & m_2 & 0 & 0 & \cdots & 0 \\ 0 & 0 & m_3 & 0 & \cdots & 0 \\ 0 & 0 & 0 & m_4 & \cdots & 0 \\ \vdots & \vdots & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & 0 & 0 & \cdots & m_n \end{bmatrix} \frac{\partial^2}{\partial t} \begin{bmatrix} u_1 \\ u_2 \\ u_3 \\ u_4 \\ \vdots \\ u_n \end{bmatrix} + \begin{bmatrix} 2k_{31} & -k_{31} & 0 & 0 & \cdots & 0 \\ -k_{31} & 2k_{31} & -k_{31} & 0 & \cdots & 0 \\ 0 & -k_{31} & 2k_{31} & -k_{31} & \cdots & 0 \\ 0 & 0 & -k_{31} & 2k_{31} & \cdots & 0 \\ \vdots & \vdots & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & 0 & 0 & \cdots & 2k_{31} \end{bmatrix} \begin{bmatrix} u_1 \\ u_2 \\ u_3 \\ u_4 \\ \vdots \\ u_n \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ \vdots \\ 0 \end{bmatrix}. \tag{3}$$

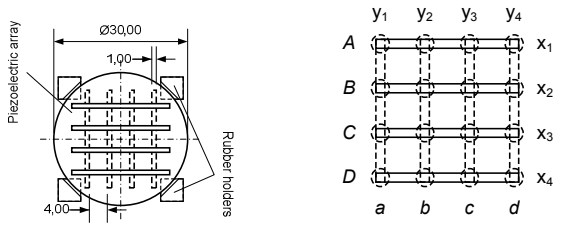
Theoretically the electrical signals from the different array points are described with Eq. 3 and can be predicted with the matrices of differential equations if the appearance of the standing and running waves is discarded. But the reality dictates that these type of waves to be taken consideration of.

In the resonance structure the standing waves are expected to appear, as their configuration patterns should be similar to the Chladni figures.

D. Experiments with Proposed Structure

To investigate the influence of the standing wave experimental research is carried out on sample of 4x4 piezoelectric resonance array formed on the disk shaped substrate as shown on Fig. 3,a. The horizontal set of electrodes is designated with upper case letters (Fig. 3,b) and the vertical electrode set is designated with small case letters (Fig. 3,b) as the two letter designator defines how the excitation signal is applied – the first letter defines where the active phase of the oscillator is applied and the second where the electrical ground is connected. Table 1 shows some of the results from the unloaded resonance structure which confirms the occurrence of the strong standing waves in the sensor array.

The used oscillator supplies the sinusoidal wave with frequency of 220 kHz (which is equivalent to the natural one for the current structure) and 10 V peak-to-peak signal (*pk-pk*) as the measured data is given in peak-to-peak and in root mean square (RMS) values.



a) Array configuration *b) Designations*

Fig. 3. Experimental array structure

TABLE 1. RESULTS FROM CONFIGURATION AA

*Measurements Points for **Aa***	*Signal pk-pk, V*	*RMS, V*
A	10	3,536
B	5,884	2,08
C	4,859	1,718
D	2,665	0,942
a	0	0
b	3,223	1,139
c	3,95	1,396
d	8,626	3,05

The obtained results show that indeed there is a standing wave that affects the signal amplitude which in turn will lead to difficulties in applying the amplitude scanning method. From practical point of view more interesting is the question if the array sensitivity is dependent on the standing waves and is this fact to be of any practical use? Experiments were carried out as in the center of the piezoelectric array was placed dielectric load of 2,764 g and 18 g were additionally inserted for comparing the sensitivity of the different standing waves. Some of the obtained results are shown in Table 2.

TABLE 2. SENSITIVITY FOR SOME OF THE CONFIGURATIONS

Configuration	*Initial Load*		*Load with Added 18g*		*Reaction*	
Bc	Signal pk-pk, V	RMS, V	Signal pk-pk, V	RMS, V	Signal pk-pk, V	RMS, V
A	5,826	2,060	5,803	2,051	–0,023	–0,009
B	10	3,535	10	3,535	0	0
C	3,082	1,090	3,106	1,098	0,024	0,008
D	5,258	1,859	5,191	1,835	–0,067	–0,024
a	3,872	1,369	3,905	1,381	0,033	0,011
b	6,094	2,154	6,070	2,146	–0,024	–0,008
c	0	0	0	0	0	0
d	3,421	1,209	3,447	1,219	0,026	0,010
Configuration	*Initial Load*		*Load with Added 18g*		*Reaction*	
Ca	Signal pk-pk, V	RMS, V	Signal pk-pk, V	RMS, V	Signal pk-pk, V	RMS, V
A	3,188	1,127	3,228	1,141	0,040	0,014
B	4,456	1,575	4,490	1,587	0,034	0,012
C	10	3,535	10	3,535	0	0
D	3,694	1,306	3,717	1,314	0,023	0,008

a	0	0	0	0	0	0
b	4,605	1,628	4,782	1,691	0,177	0,063
c	4,978	1,760	5,175	1,829	0,197	0,069
d	4,829	1,707	4,999	1,767	0,170	0,060
Configuration	*Initial Load*		*Load with Added 18g*		*Reaction*	
Dc	Signal pk-pk, V	RMS, V	Signal pk-pk, V	RMS, V	Signal pk-pk, V	RMS, V
A	3,435	1,214	3,439	1,216	0,004	0,002
B	4,183	1,479	4,181	1,478	–0,002	–0,001
C	4,606	1,628	4,614	1,631	0,008	0,003
D	10	3,535	10	3,535	0	0
a	6,418	2,269	6,408	2,650	–0,010	–0,004
b	4,253	1,504	4,256	1,505	0,003	0,001
c	0	0	0	0	0	0
d	6,149	2,174	6,141	2,171	–0,008	–0,003

From the collected data can be assumed that the pattern of the standing waves changes when shifting between different electrode combinations and there is also different sensitivity depending on the currently excited standing wave as the sensitivity for given array point changes with accordance with the wave configurations. This specific behavior can be utilized for quicker scanning process but there is need for specific interface schematic.

F. Proposed Interface for Resonance Array

For facilitating the sensor array field the signal from electrical oscillator working on the innate system frequency should be supplied to specified electrodes in the array field as well as to insure the common electrical ground of the piezoelectric system. This can be solved with analog switching circuitry and relevant control system.

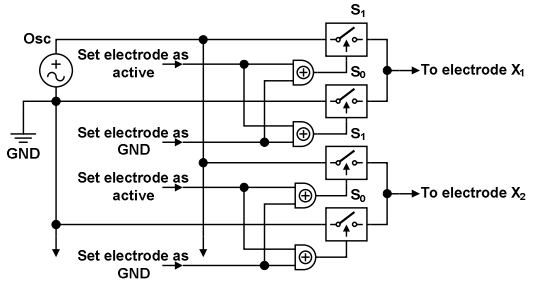
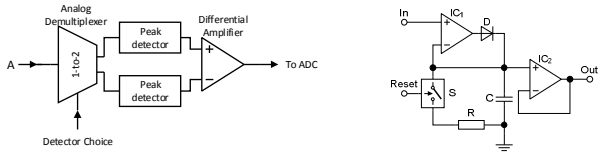


Fig. 4. Switching circuitry, servicing the piezoelectric array

Every electrode from the piezoelectric array is connected to two analog switches (designated as S_0 and S_1 on the Fig. 4) that each of them is either connected to the electrical oscillator or to the electrical ground. This way choosing between the switches and their state multiple electrode configurations can be executed in the piezoelectric array. The XOR logical gates are included to ensure that short circuiting is not going to happen between the oscillator and the ground.



a) Interface for every electrodes *b) Peak detector*

Fig. 5. Output circuitry for piezoelectric array

The distinction between the influences of different loads can be detected using differential amplifiers which will compare the signal values. The signals from piezoelectric array electrodes are fed to the analog 1-to-2 demultiplexer controlling two peak detectors which in turn are connected to the inputs of a differential amplifier (Fig. 5,a). Generally, peak detectors (Fig. 5,b) can be considered as type of memory elements which memorize the peak value of the alternating signal as a charge stored in the capacitor. Thus the peak detector firstly connected to the demultiplexer can store the initial signal value and the secondly connected peak detector can supply the referent value for the differential amplifier. The amplifier output is connected then to ADC so factually the combinations of peak detectors and amplifier (defined as PDA block on Fig. 6) are the outputs from the resonance array that are connected with multichannel ADC.

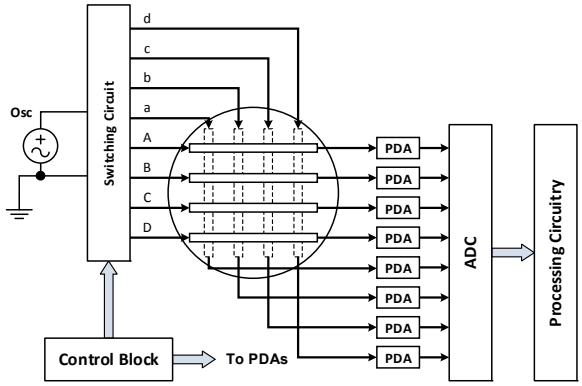


Fig. 6. Simple output interface circuitry

The interface schematic that can serve piezoelectric resonance array is shown on Fig. 6. Because of the differential amplifiers in PDA blocks the presence of additional load in the sensor field is detected when there is nonzero signal in the output.

The detected nonzero values from ADC block are processed according to the mathematical model to obtain the tactile image of the applied external stress.

III. Conclusion

It is evident that the resonance structures have peculiarities that are connected to their mode of operation. The resonance mode is ought to bring standing waves that have patterns similar to those of Chladni figures.

The resonance sensor structures require specific interface circuitry that can ease the problems with the real time mode operations. The amplitude scanning method is proposed as a solution which can utilize parallel algorithms with the proper circuitry that can serve it. The proposed circuit has digital output that can ease the data processing, which will also help with the real time mode problem.

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Hydrogen Bonding Network as a Logic Gate

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Abstract – **A circuit consisting of four- and five-terminal block elements is developed to imitate the behavior of hydrogen bonding networks in the β-lactamase protein. The circuit is implemented in Cadence Spectre to simulate its signal processing capabilities. The analysis shows that circuit outputs have logic levels for the current. The simulations show that the circuit can simultaneously invert and repeat signals, i.e. parts of the protein operate as logic gates.**

Keywords – **logic gates, hydrogen bonding network, β-lactamase, digital operation.**

I. Introduction

The miniaturization of silicon microelectronics elements leads to multiple problems such as short channel and tunnel effects, hot carriers, etc. For this reason, the scientists are focusing to elements and circuits inspired from the nature. They try to fins bioorganic objects that perform logic operations similar to logic gates and semiconductors. For example, D. Bhattacharjee [1] demonstrate two forms of molecular gates in which the DNA works as input signal while the output signal is the fluorescence intensity of different bands; the application of these gates is as DNA sensor. In V. Privman [2] show the realization of AND logic gates based on enzymatic cascade with an additional photochemical processing at the output to allow sigmoid response on both inputs. Other functional forms are created for evaluating the kinetics of such systems to model their response in terms of signal processing. Other authors [3] demonstrate that even small molecules form intramolecular hydrogen bonds might serve classical (Boolean) logic operations. Having in mind that enol-keto isomerization can perform logic operations using its hydrogen bond, we can ask the question if there are other objects which form hydrogen bonding networks that can process digital information. Such objects are the proteins composed of hydrogen bonding networks and potentially each of them may process digital information [4], [5].

In this paper, we extract a small hydrogen bonding network of β-lactamase and verify possibility to operate as digital device.

II. Model and Equations

The hydrogen bonding network (Figure 1) is taken from the β-lactamase protein. The hydrogen bonds between all its residues N132, K73, S70, water molecule w297 with residues N170 and with E166 are investigated in [6]. In [6] the change of the proton transfer parameter (i.e. the current) is shown in each hydrogen bond depending on the electrostatic potential of the heavy atoms that are part of the hydrogen bond. Due to this analysis, we may construct block-elements that possess *I-V* characteristics of the separate heavy atoms that comprise the network of hydrogen bonds. The block-elements and the circuit that they form is thoroughly investigate in [7].

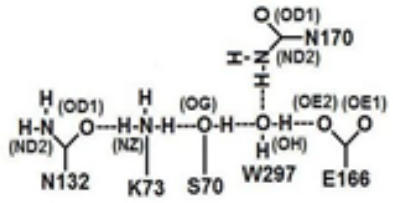

Fig. 1. Hydrogen bonding network consisting N132, N170 Asparagine residues, K73 Lysine residue, S70 Serine residue, w297 water molecule, E166 Glutamic acid residue.

The circuit in Figure 2 is developed based on the hydrogen bonding network. It is implemented in Cadence Spectre where the functional characteristics of each block-element are described.

We start from the input element T1 corresponding to K73NZ. The lysine residue is a strong proton donor and that is why in the circuit it is interpreted as voltage controlled current source – Eq. 1 and Eq. 2.

$$U_{in} = U_1 \quad (1)$$

$$I_1 = 3*10^{-5}U_1^3 - 5*10^{-5}U_1^2 - 7*10^{-5}U_1 + 0.0013 \quad (2)$$

The change of the potential on K73NZ will lead to a change in the potentials S70OG and N132 (designated with T2 and R5) and the conditions for proton transfer respectively.

The equations for the second block-element T2 are:

$$U_2 = 1.0451U_1 - 0.1194 \quad (3)$$

$$I_2 = -0.0236U_2^3 + 0.0379U_2^2 + 0.124U_2 + 1.3046 \quad (4)$$

The equations for R5, the second output of the circuit, are:

$$U_5 = 0.0457U_1 + 1.2273U_1 - 0.8501 \quad (5)$$

$$I_5 = 0*U_5 + 0.0001 \quad (6)$$

The following equation are for the third block-element, analogous to W297:

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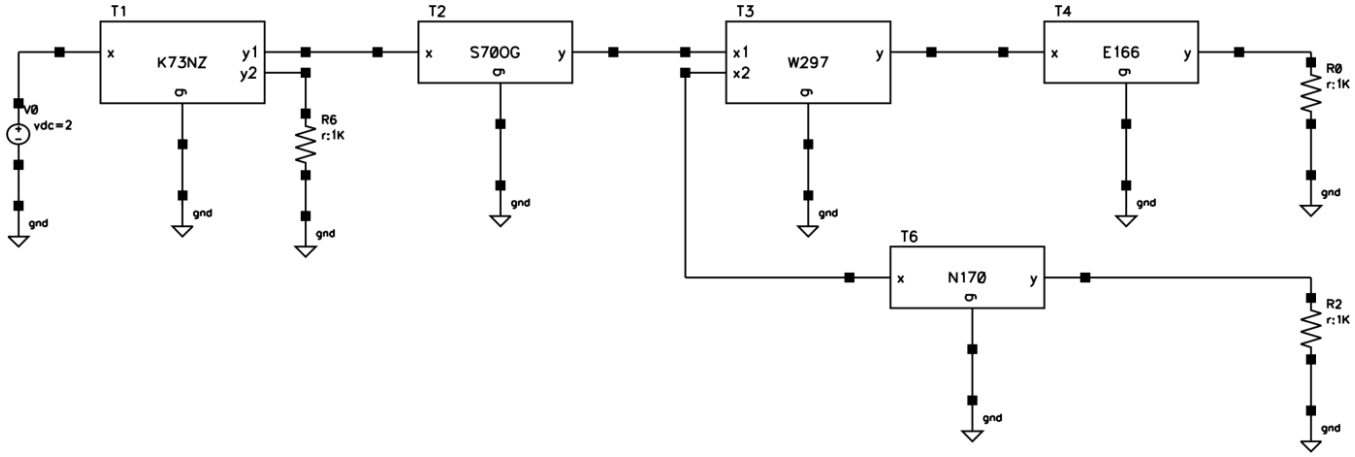

Fig. 2. Equivalent circuit of the hydrogen bonding network consisting of T1 (corresponding to K73NZ), T2 (S70OG), T3 (w297), T4 (E166), T6 (N170).

$$U_3 = 1.0179*U_2 - 0.039 \quad (7)$$

$$I_3 = 0.0015U_3^3 - 0.0015U_3^2 - 0.0171*U_3 + 0.0859 \quad (8)$$

T3 accepts signal from T2 and sends it to other two terminal elements T4 and T6, which have functional characteristics corresponding to E166 and N170.

Description of current and voltage for the fourth block-element T4, which is the first circuit output:

$$U_4 = 0.9703U_3 + 0.0589 \quad (9)$$

$$I_4 = I_3 = I_{out1} \quad (10)$$

For the third circuit of the block-element T6 we have the following equations are:

$$U_6 = 1.0544U_3 - 0.0933 \quad (11)$$

$$I_6 = 0.0058U_6^2 + 0.0367U_6 + 0.7113 \quad (12)$$

The block elements are coded in Verilog-A and simulated in Cadence. Sample code is shown in Figure 3:

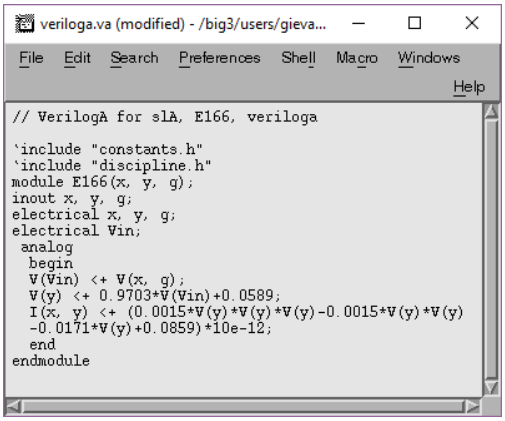

Fig. 3. Input vs. output voltage.

III. Digital Results and Analyses

For performing digital simulations, we proceed from the following assumptions: i) from equations (5) and (6) we can observe that voltage on the second output is proportional to the input voltage; the current of the second output is constant that means no logic levels can be set. ii) in Figure 4 we can see that the output voltages are linearly proportional to the input voltage.

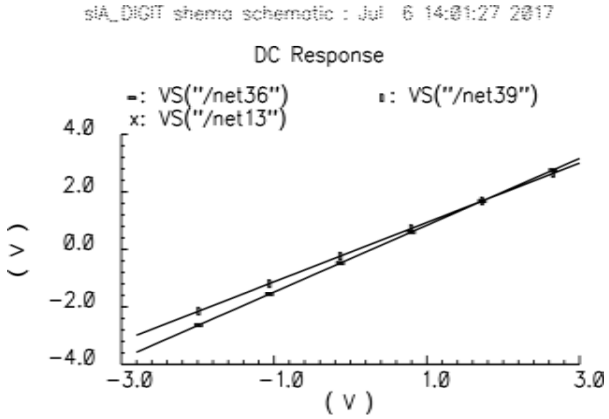

Fig. 4. Input vs. output voltage.

iii) The preliminary analyses show that the output currents are nonlinearly changing with the input current. Hence, logic levels might be set on the outputs.

A. Determination of logic levels

We simulate the transfer characteristic of the circuit in order to determine the boundaries of logic "0" and "1" at the input and outputs (Fig. 5 and Fig. 6).

From the transfer characteristic in Figure 5 we may set logic "0" and "1" at the input and output [8]. We consider the current in output 1 versus the input current. We set the range of –0.1 pA to –0.01 pA for the levels of logic "0". The input levels of the logic "1" are between 0.12 pA to 0.3 pA. For the levels of logic "0" we set the interval

0.58 pA to 0.66 pA and the output levels of logic “1” are in the interval 0.76 pA 1.04 pA.

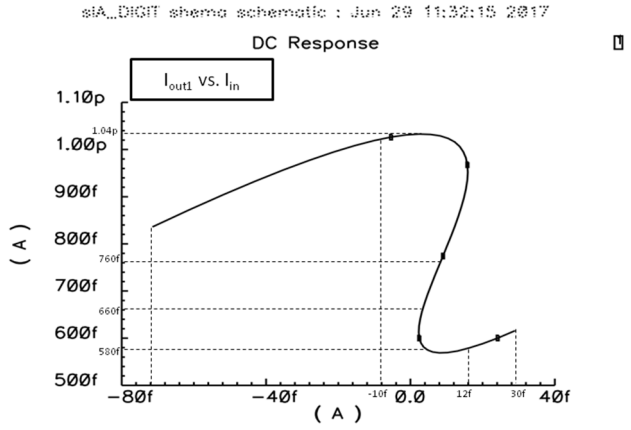

Fig. 5. Transfer characteristic of the first output.

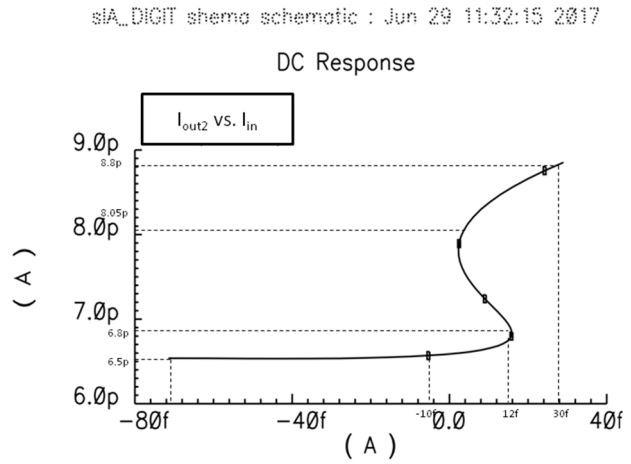

Fig. 6. Transfer characteristic of the third output.

From the transfer characteristic in Figure 6 we may set the levels of logic “0” and “1” at the input and output. We consider the current in output 3 versus the input current [8]. For the levels of input “0” we set the interval of –0.1 pA to –0.01 pA. The levels of input “1” are between 0.12 pA and 0.3 pA. From the transfer characteristic, we observe that the input level in both Figures 5 and 6 are identical. For the levels of output “0” we set the range of 6.5 pA to 6.8 pA and the output “1” is in the interval of 8.05 pA to 8.8 pA.

B. Transient analysis of the logic gate

The analysis is conducted at input voltage with rectangular form between –3 and +3 V (Fig. 7). The characteristics of the input current and the first output current versus time are shown in Figures 8 and 9.

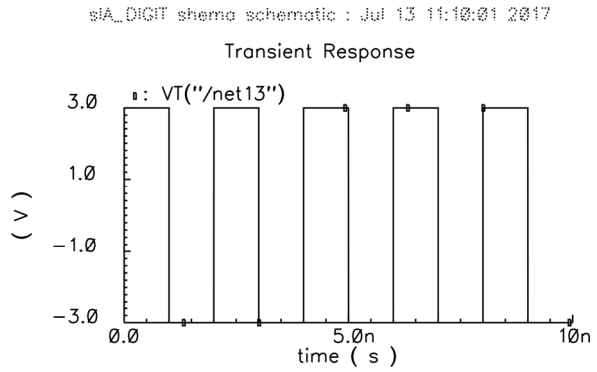

Fig. 7. Rectangular voltage diagram.

Considering the results shown in the above figures we determine that for the input current the logic level of “0” = –0.1 pA and logic level of “1” = 0.22 pA. For the output current the logic “0” = 0.61 pA and the logic “1” = 0.76 pA. These values match the preliminary determined levels of logic “0” and “1” for output 1. It can be seen that the output signal inverts the input signal. Hence, the first output operates as inverter.

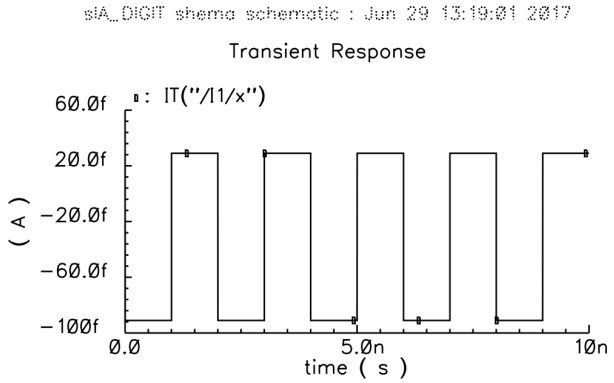

Fig. 8. Rectangular input current diagram.

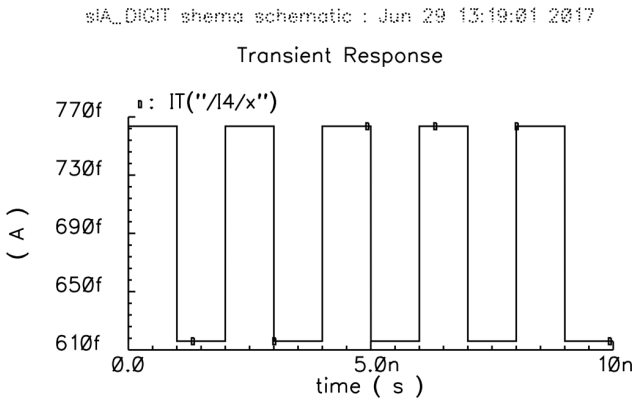

Fig. 9. Rectangular current diagram of the first output.

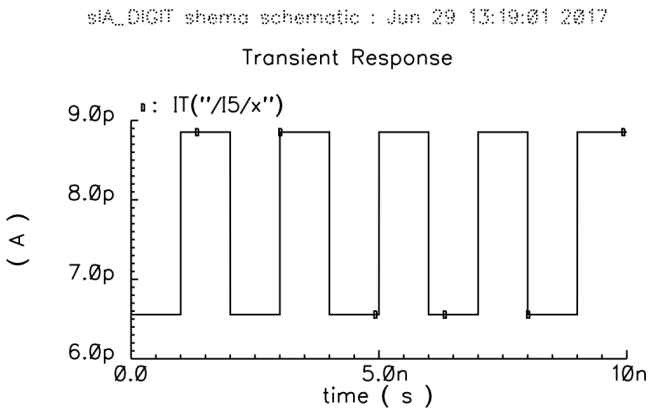

Fig. 10. Rectangular current diagram of the third output.

The results for the current in the third output of the circuit (Fig. 10) and the input current (Fig. 8) we see that we can set logic levels of the input and output. For the input current, the logic "0" = –0.1 pA and logic "1" = 0.22 pA. For the output current the logic "0" = 6.6 pA and logic "1" = 8.8. pA. These values correspond to the preliminary determined logic levels for the transfer characteristic of output 3. It can be seen in Figures 8 and 10 that the input signal repeats the output. The third output operates as a repeater.

IV. Conclusion

The modeled circuit well describes the hydrogen bonding network. The preliminary analysis of the circuit and the equations proved that we can set the logic levels for the current in the first and the third outputs. The simulations show that the circuit can simultaneously invert and repeat signals.

Acknowledgment

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A Microelectronic Circuit in CADENCE Analogous to Michaelis Complex of β-lactamase Protein

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Abstract – **In the present paper a microelectronic circuit in Cadence functionally analogous to Michaelis complex of β-lactamase protein is investigated. The hydrogen bonding networks are described by electrical circuits. Block elements are made for each residue from protein hydrogen bonding networks, which are functionally analogous to residues and describe the proton transport. The block-elements are coded and described in Cadence with polynomials and DC and transient analyses were carried out. The simulation results are compared to electronic circuit and elements.**

Keywords – **protein beta-lactamase, Hydrogen Bonding Networks, CADENCE**

I. Introduction

We investigated the proton transfer through hydrogen bonding networks (HBNs) of the beta-lactamase protein. Results are described in our previous research [1-3]. We investigated the proton transport of each hydrogen bond of the protein using Marcus theory [4]. For each residue from protein HBN block-elements are made, which are functionally analogous to residues and described the proton transport with polynomials. Then we performed static and dynamic analysis in MATLAB. The simulation results are compared to electronic circuit and elements.

The focus is on HBNs in the beta-lactamase protein of Michaelis complex (ES). The behavioral language Verilog-A and Cadence [5] for simulation results are used.

II. Model of Hydrogen Bonding Networks

The HBNs formed in active site of Michaelis complex (ES) of β-lactamase protein are modeled and described in [6]. The polynomials which described a proton transport are given also in [6]. In the present paper block-elements are made using Verilog-A language and Cadence.

In [7] block-elements are described and coded using MATLAB and now a comparison with the simulation results is done.

Figure 1 shows the HBNs in the Michaelis complex (ES).

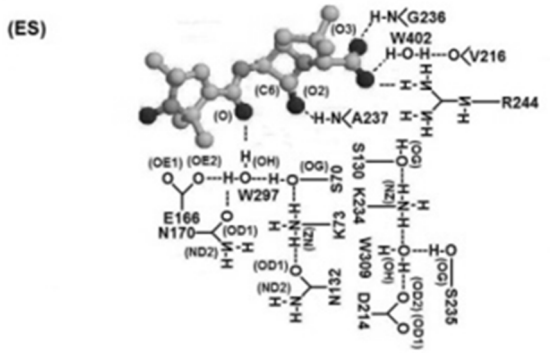

Fig. 1. HBNs in the active site of Michaelis complex [6].

The hydrogen bonding networks on figure 1 are formed from two networks. The first one is referred to nucleophilic and the second one referred to electrophilic. The first network consists of ligand and residues Lysine K73NZ, Serine S70OG, water w297, Glutamine E166, Asparagine N132, Asparagine N170. The second network consists of residues Lysine K234NZ, water w309, Aspartate D214, Serine S130OG and Serine S235OG [6].

The proton transfer in both HBNs occurs at the same time that is the reason why the both networks are not separated. There is proton transport in parallel in both HBNs during the different intermediates of the reaction [6]. The voltages at the first and the second input are equal. The proton transfer depends on interaction between protein and ligand and pH. The input voltages are analogy and depend on pH.

On figure 2 the microelectronic circuit in Cadence functionally analogous to HBNs in beta-lactamase protein in Michaelis complex is shown.

The voltage is generated in parallel to the both inputs. For each residue block-element is coded. For residue Lysine K73NZ block-element T1 is presented. This block-element responds to a generator of the circuit. For residue Serine S70OG block-element T2 is coded with one input and one output. For water molecule W297 block-element T3 is presented. Residue Glutamine E166 is presented block-element T4. Other two residues Asparagines N132 and N170 from first network are similar to block-elements T5 and T6 both with one input and one output.

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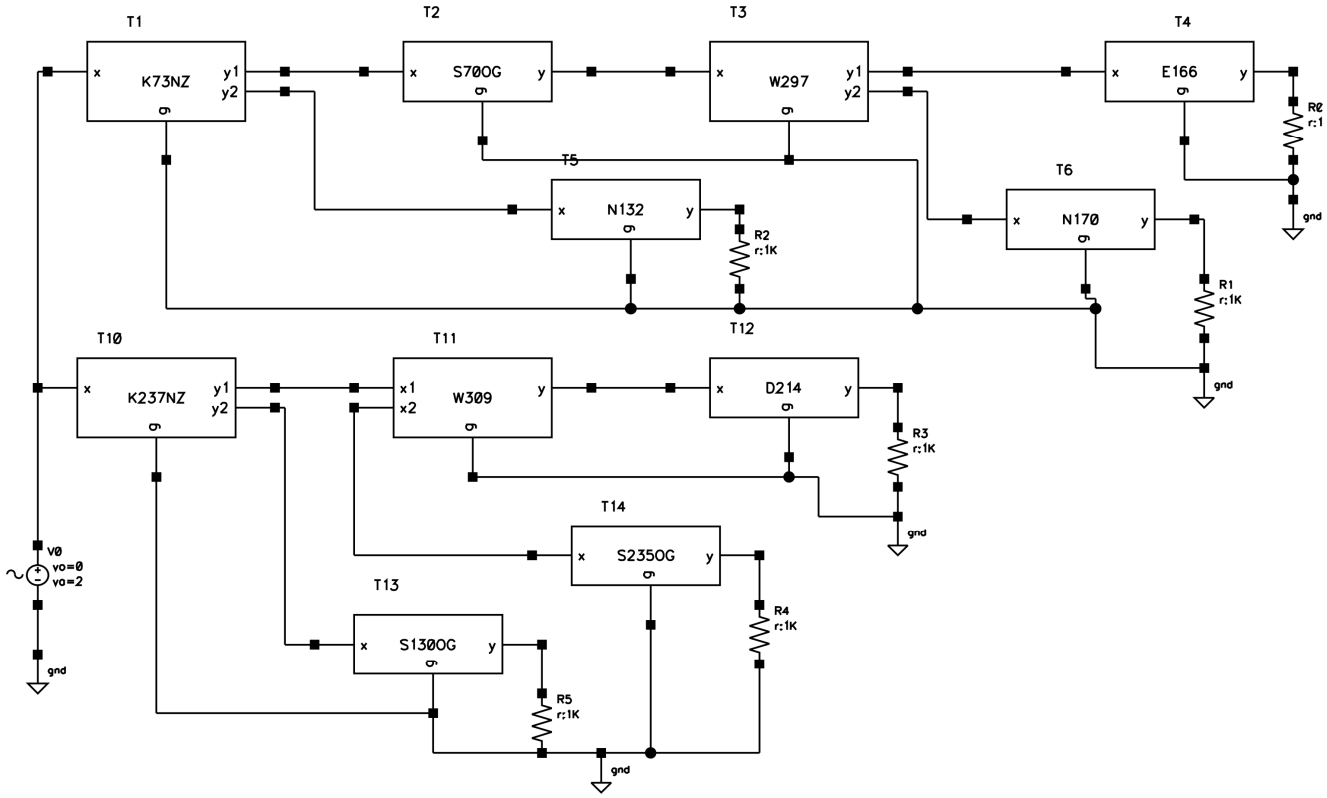

Fig. 2. The microelectronic circuit functionally analogous to HBNs in beta–lactamase protein in Michaelis complex.

For the second network input voltage is identical to the first voltage. Block-element T10 corresponds to residues Lysine K234NZ with one input and two outputs. The block-element T10 is a generator in the circuit. For water w309 block-element T11 is coded with two inputs and one output. Residue Aspartate D214 corresponds to block-element T12 with one input and one output. The block-element T13 is analogues to residue Serine S130OG with one input and one output. The last residue Serine S235OG has the same function as Serine S130OG and is presented with block-element T14.

The equations describing electrical relations of each block-element are given in [6]. The equations are coded using behavioural language Verilog-A in Cadence [5]. The code from Cadence for some of the block-elements is given below:

veriloga.va - /big3/users/gieva/cadence/slB_diplom/T2/veriloga/

File Edit Search Preferences Shell Macro Windows Help

```
// VerilogA for slB_diplom, T2, veriloga

`include "constants.h"
`include "discipline.h"

module T2(x,y,g);
inout x, y, g;

electrical x, y, g;
electrical Vin;

analog

  begin
   V(Vin) <+ V(x,g);
   V(y) <+ 1.0034*V(Vin) + 0.0002;

   I(x,y) <+ 10e-12*(0.0158*V(y)*V(y)*V(y)*V(y) - 0.1264*V(y)*V(y)*V(y) +
         0.184*V(y)*V(y) + 0.1988*V(y) + 1.351);

  end

endmodule
```

veriloga.va - /big3/users/gieva/cadence/slB_diplom/T12/veriloga/

File Edit Search Preferences Shell Macro Windows Help

```
// VerilogA for slB_diplom, T12, veriloga

`include "constants.h"
`include "discipline.h"

module T12(x, y ,g);
inout x, y, g;

electrical x, y, g;
electrical Vin;

 analog
  begin
  V(Vin) <+ V(x,g);
  V(y) <+ V(Vin)*1.0014 + 0.2647;

  I(x, y) <+
  10e-12*(2*10e-6*V(y)*V(y)*V(y)*V(y)*V(y) -3*10e-5*V(y)*V(y)*V(y)*V(y) +
  2*10e-5*V(y)*V(y)*V(y) + 10e-4*V(y)*V(y) - 0.0001*V(y) + 0.00044);

  end

endmodule
```

III. DC Analysis

The DC analysis was carried out in Cadence. The supply voltage on the input is in the range from -2 to 3 [V]. The output voltages of the circuit have the same form like the input voltage and are linear with respect [6]. The results for output currents are very different and are given on the figures below.

Figure 3 shows the current of first output versus first output voltage.

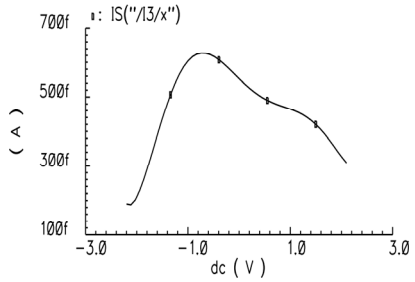

Fig. 3. Current of first output vs. first output voltage.

The *I-V* characteristic from figure 3 is functionally analogues to tunnel diode.

On Figure 4 is shows the current of second output.

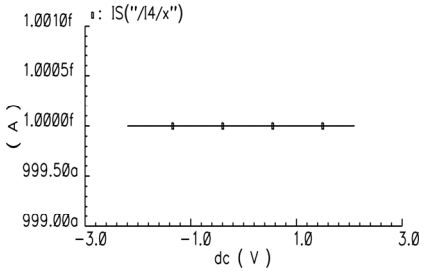

Fig. 4. Current of second output vs. second output voltage.

The output current (figure 4) does not vary with the change of the output voltage. The value of the output current is 1 [fA]. The function of this second output is behaved like current mirror.

On figure 5 the output current versus output voltage is shown.

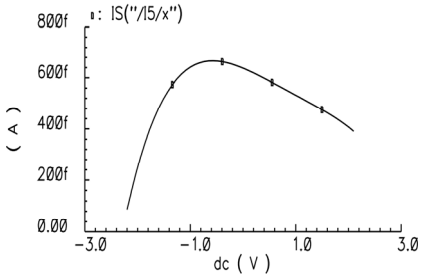

Fig. 5. Current of third output vs. output voltage.

The output characteristic of the third output is not functionally analogues to electronic devices often used in practice.

On figure 6 the output current of twelfth output is shown.

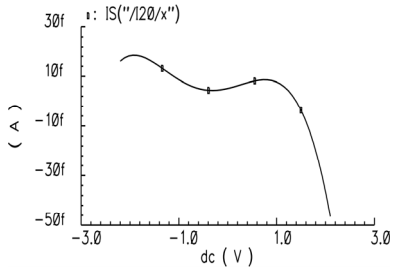

Fig. 6. Current of twelfth output vs. output voltage.

The output characteristics of this output are in different combinations of curves with S-shapes.

On the next figure 7 the output characteristics of thirteenth output is shown. The output current is again (such as on figure 6) combinations of curves with S-shape.

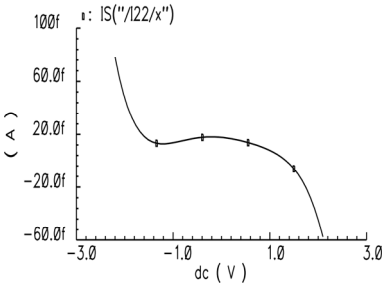

Fig. 7. Current of thirteenth output vs. output voltage.

From figure 8 can be observed that the output current does not vary with the change of the output voltage. The value of the output current is constant 1 [fA]. The function of this output is behaved like current mirror or source like a second output of the circuit.

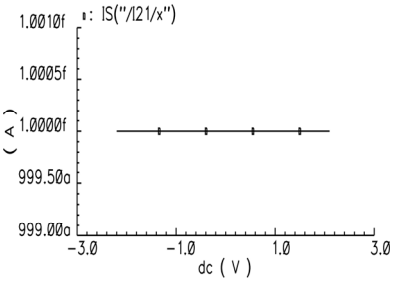

Fig. 8. Current of fourteenth output vs. output voltage.

The simulation results of the DC analysis show that the circuit is functionally analogues as an amplifier or as a current source.

IV. TRANSIENT ANALYSIS

The transient analysis is carried out in Cadence. The frequency of the supply input voltage is 10 [GHz] and the amplitude is from –2.2 to +2.2 [V].

The results from simulation show that the output voltages repeat the input voltage with amplitude in the same order. This dependence can be seen from DC analysis. Therefore, only vary of output currents vs. time will be presented, for convenience.

On figure 9 the current versus time on first output of the circuit is shown.

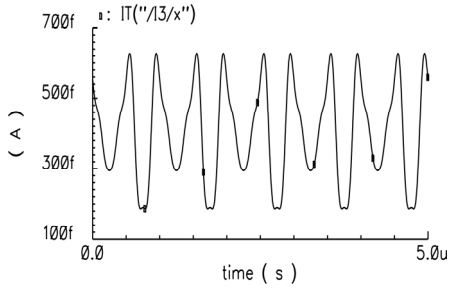

Fig. 9. The current on first output vs. time.

On figure 10 the current vs. time on second output is shown. The output current is behaved like current mirror or current source, because there is no change of the current with the applied voltage. The output current is a constant 1 [fA].

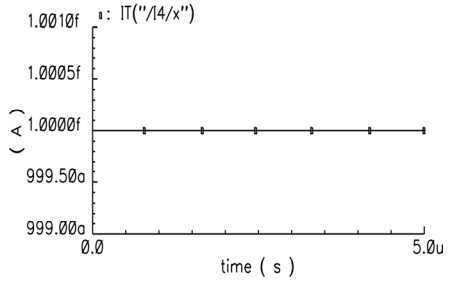

Fig. 10. The current vs. time on second output.

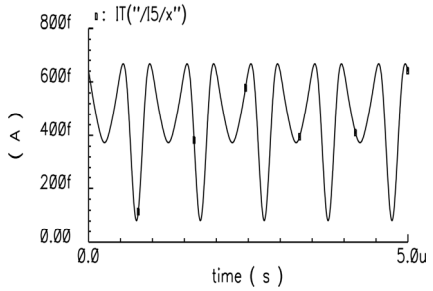

Fig. 11. The current vs. time on third output.

The output current (figure 11) of the third output illustrates modulated signals.

Figure 12 and 13 show the similar results with figure 11 (third output). The signal modulation can be seen which is different from the previous results.

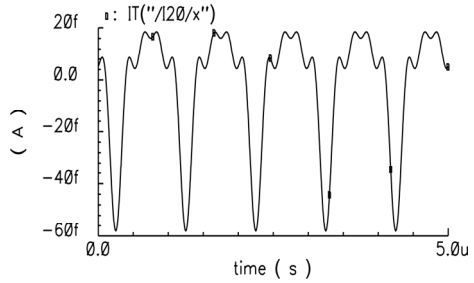

Fig. 12. The current vs. time on twelfth output.

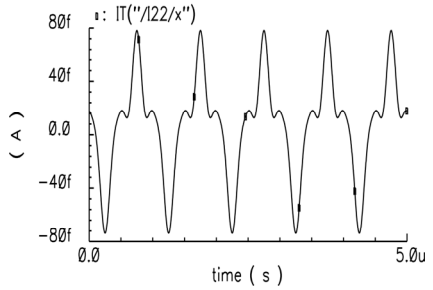

Fig. 13. The current vs. time on thirteenth output.

On figure 14 the current versus time on fourteenth output is shown. The results are similar to these in the second output. The characteristic is similar to current mirror because there is no change of the current with the applied voltage. The output current is a value 1 [fA].

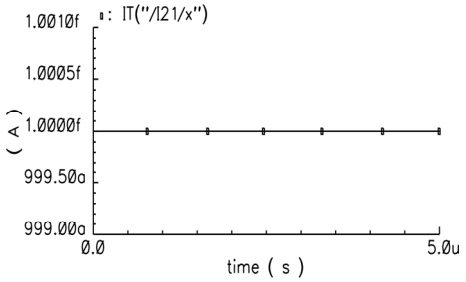

Fig. 14. The current vs. time on fourteenth output.

The transient analysis results show that the investigated microelectronics circuit is functionally analogues with different modulation signal or current source or can be similar to conventional electronic circuit or elements.

V. Conclusion

The results from analysis showed that the microelectronic circuit with block-element well described the behavior of the HBNs. DC analysis showed that the investigated circuit is functionally analogues to an amplifier, current mirror or current source or tunnel diode. The results from transient analysis illustrated that the circuit could operate as signal modulator in different modes.

VI. Acknowledgement

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Fast modeling of SAM layers for electronics

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Abstract – **Self-Assembled Monolayers (SAM) are ordered structures formed by adsorption of an active agent to a solid surface. In general, SAM can be designed to have extreme high functional density. However chemical reactions and perturbations can create variety of structures which are energetically stable. Direct DFT periodic calculations are expensive. We show that extended sampling method combined with dimensionality reduction scheme can be used for identification of preferable adduct conformations obtained under specific thermodynamics conditions at a fraction of the computational cost.**

Keywords – **free energy, modeling, semiconductors, SAM layers**

I. INTRODUCTION

Self-Assembled Monolayers (SAM) are ordered structures, which can be designed to have very high functional density. However, in practice due to perturbations and chemical reactions on a silicon surface, the SAM layers become a mixture of several adducts, each of which is energetically stable. The relation between structure and properties is weak i.e. it is possible to have two or more different adducts each of which exhibit the similar properties. Obviously, precise molecular dynamics calculations can be very valuable. Direct predictions of chemical kinetics with DFT periodic calculations employing hybrid exchange correlation functional(s) even relatively accurate (in comparison to experimental data) are computationally very expensive. Pairwise models are fast and computationally cheap, but are atom centric and do not take into account the chemical bonding. As such, in a case of equilibrium geometry, even simple pairwise force fields with carefully designed parameters may achieve desired accuracy of <1 kcal/mol. For non-equilibrium geometries, however, simple potential models are not applicable because they do not take bonds into account. The problem can be mitigated with adding topological models of possible SAM chain types to existing force field. In this work, we use the extended version of popular OPLS force field extended with topological models of SAM chain types. However, because the dimensionality of collective variables space increase exponentially with the molecule weight of the surface agent, the choice of optimal set of collective variables (CV) is critical. Adsorption free energy surface of SAM is quite rough i.e. it holds sets of relatively shallow basins separated by smooth barriers. In many dimensions, the traditional local methods of FES reconstruction (histogram, mean force) poorly distinguish between basins separate by low barrier, nor are aware of the shape of the basins. Recently in a framework of driven adiabatic molecular dynamics (dAFED) [1][2], we proposed a scheme for accurate reconstruction of free energy surface (FES) based on extension of the Gustafson-Kessel algorithm [3]. Here we describe the mechanism of dimensionality reduction approach, which allows to work in many dimensions. Thus, having a capability to sample globally the conformational space along with precise reconstruction of multidimensional FES can help to identify the predominant adducts and further to control thermodynamics conditions in order to obtain maximal quantity of desirable adduct.

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A. Extended sampling

In this section, we will brief the extended sampling method and specifically driven adiabatic free energy dynamics (dAFED) approach. In the core of the method is adiabatic separation between collective variables and remaining degrees of freedom of the molecular system. The chosen set of collective variables are made “slow variables” by increasing their mass and temperature. The complete method is described elsewhere [1]. Under condition that collective variables have much higher temperature than other variables in a system, the dAFED is capable to provide enhanced sampling along the directions of CVs. Thus, the method is suitable to map rough energy surfaces and therefore compatible to sample free energy surfaces of SAM layers.

B. Entropy driven dimensionality reduction

The description of free energy will require the convolution of several functions in order to describe different regions of a landscape. With the uncertainty of the proper "global" set of collective variables (CV) the brute force approach will require to use as large as possible CV-set. That causes very long calculations due to high dimensionality. In this work, we use mesh and spectral approaches to achieve effective sampling of rough energy surfaces. In proposed approach, we do data and dimensionality reduction along with fast global extended sampling over rough free energy landscapes. The data reduction step uses a mesh based method and generates a data tree each leaf of which contains an "interesting" volume in multidimensional space. It is important to mention, that the method preserves the expectation values of the samples residing in leaves. The second part of the algorithm utilizes a spectral dimensionality reduction approach with the purpose to reveal the low dimensional manifold embedded in each multidimensional volume. As a metric, we use the information content known as well as quadratic Reynil entropy. The output of dimensionality reduction step is a tree structure, which is a direct parser to a domain. As such the

calculations in leaves can be done in parallel utilizing different parallel schemes - from multithreaded to embarrassing parallel, MPI or hybrid models.

Below is given the schematic of the algorithm:

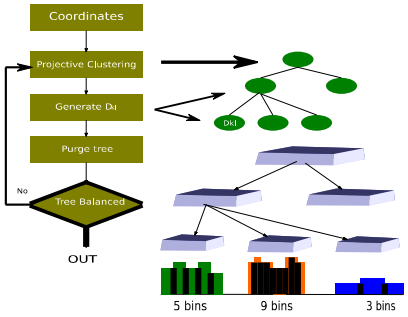

Fig. 1. Algorithm

At each dimension *i, i ∈[1,D]* we calculate the data range R_i and divide the data region in 3 subranges. In each region, we organize the data in a way that the region which holds most samples in in the root of a tree while the one with least samples is right leaf and the remaining is the left leaf. For each region, we calculate the optimal bin width with Scott's formula [4]:

$$w_{ij} = 3.5 * \sigma * n_{ij}^{-\frac{1}{3}}, j = 1,2,3 \qquad (1)$$

where σ is standard deviation for this data range and n_{ij} is number of samples in that range. We continue to generate the leaves in this procedure until we reach some prescribed threshold. At that point each leaf the tree represents some volume in multidimensional space. Then, we calculate information entropy for each leaf by simply:

$$H(x_L) = \sum_{i=1}^{B} p(x_{iL}) \log_2(p(x_{iL})) \qquad (2)$$

where B is the number of bins in this leaf, and x_L is the total population of samples in this leaf and x_{iL} is the populations of samples in bin *i* for this leaf and $p(x_{iL})$ is normalized bin density given by:

$$p(x_{iL}) = \frac{dd_{iL}}{\sum_{k=1}^{B} dd_{iL}} \qquad (3)$$

For uniform distribution q, all bins have the same density and thus the histogram with B bins will have the entropy:

$$H(x_l) = \sum_{k=1}^{B} \widehat{q(x_{kl})} \log\big(p(x_{kl})\big) = \frac{1}{B} \qquad (4)$$

Then for a histogram in each leaf we may calculate multimodal likelihood which describes the probability to observe particular histogram if a distribution actually generates a data set. To do so we use Kullback - Leibler divergence [5]:

$$D_{kl}(p|q) = \sum_i p_i log_2 \left(\frac{p_i}{q_i}\right) \qquad (5)$$

The latter measures proximity of 2 probability distributions p and q. i.e. divergence of particular distribution in a leaf to a uniform distribution. Then we label each leaf of the tree with its D_{kl} coefficient. At that point the graph will be heavy on left side and light on right side. Then we purge the tree in a loop by removing the nodes which have $0 \le D_{kl} < t$ where t is tuned parameter and recalculating the entropy of the leafs at each cycle as was described above. The process continues till no purges are necessary. The dimensionality reduction step is based on Renil's quadric entropy [6], which is a measure of impact on a cluster if a sample is added to all other clusters.

$$H_r(x) = -log_2 \int f_x^2 \, dx \qquad (6)$$

where f_x denotes probability density function. In order to estimate densities, we use Parzen estimator, which estimates density against some kernel function. We use a Gaussian kernel. Thus, for each leaf we get for discrete case:

$$\widehat{f}(x) = \frac{1}{n}\sum_{i=1}^{n} \frac{1}{(\sqrt{2\pi\sigma})^D} e^{\left(-\frac{1}{2}\left(\frac{x_c - x_i}{\sigma}\right)\right)} \qquad (7)$$

here x_c is a center of each cluster and σ is standard deviation of Gaussian at each dimension. The final step uses the convolution of Gaussians which is also Gaussian, but wider than originals. We convolute incrementally respective densities; calculate resulting divergences and QUCKSORT the resulting array. Then we pick the minimal value.

B. Computational methods

The proposed method was implemented in PINY-MD package along with topological extensions for OPLS force field. We use already existing data types defined for proteins in order to define topological models for SAM chains. The simulations were done with distributed parallel implementation (OpenMPI) of the above code when each leaf was calculated in parallel.

II. Conclusion

Proposed method offers a significant speed up of the calculations. The comparison of the simulation times of SiC done with PINY-MD vs. AbInitio calculations showed speed up of 6 to 7 times depend on size of the system. The error in comparison to experimental data was larger than 1 kcal/mol, but most of it was attributed to improper tuning of the parameters for topology models of SAM and choice of Force Field. The further work requires the development and validation of more precise topological models.

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Kinetics of reanodization of porous anodic oxide films on aluminium formed in pore-forming solutions of various acids

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Abstract – **Investigations are carried out towards reanodization of porous anodic oxide films on aluminium formed in aqueous solutions of sulphuric, oxalic and chromic acid. These films are prepared in a way to have one and the same porosity. It is found out that in case of equal porosity the slopes of the kinetic voltage-time curves recorded during reanodization are different. The effect of the anionic species incorporated from electrolyte solution into the porous template could be a probable explanation for the dissimilar rates of barrier layer growth.**

Keywords - **anodic aluminium oxide, reanodization, anion incorporation**

I. INTRODUCTION

Reanodization (pore-filling, forming) of porous anodic alumina (PAA, fig. 1a) is carried out during its anodic polarization in not dissolving the porous film electrolyte solutions such as boric, tartaric, citric acid, etc. [1, 2]. The same electrolyte solutions are used in formation of barrier (dense, non-porous) anodic oxides on aluminium (fig. 1b) as well and are widely implemented in fabrication of aluminium electrolytic capacitors. It has been found [1] that during reanodization increase of the thickness of barrier (non-porous) layer, which is a part of PAA, is attained. In this case, the growth of barrier layer takes place on both metal/oxide and oxide/electrolyte interfaces. As a result, the so called "complex" or "composite" oxide films (fig. 1c) are produced [3-7]. Furthermore, it has been revealed [2] that lowering the PAA porosity results in higher rates of barrier layer growth during reanodization, since the real current density at the pore bottom (J_{pore}) is higher than the preset one (J_{total}),. The porosity α could be presented generally as a ratio of pore section (S_{pore}) to the entire (geometric) electrode surface (S_{total}):

$$\alpha = S_{pore}/S_{total}$$

Reanodization of PAA is an approach of formation of some "dry" systems, e.g. metal/oxide/metal, semiconductor/oxide/metal/oxide, etc. The complex anodic aluminium oxides (AAO) demonstrate improved dielectric properties in comparison to dense (non-porous) ones.

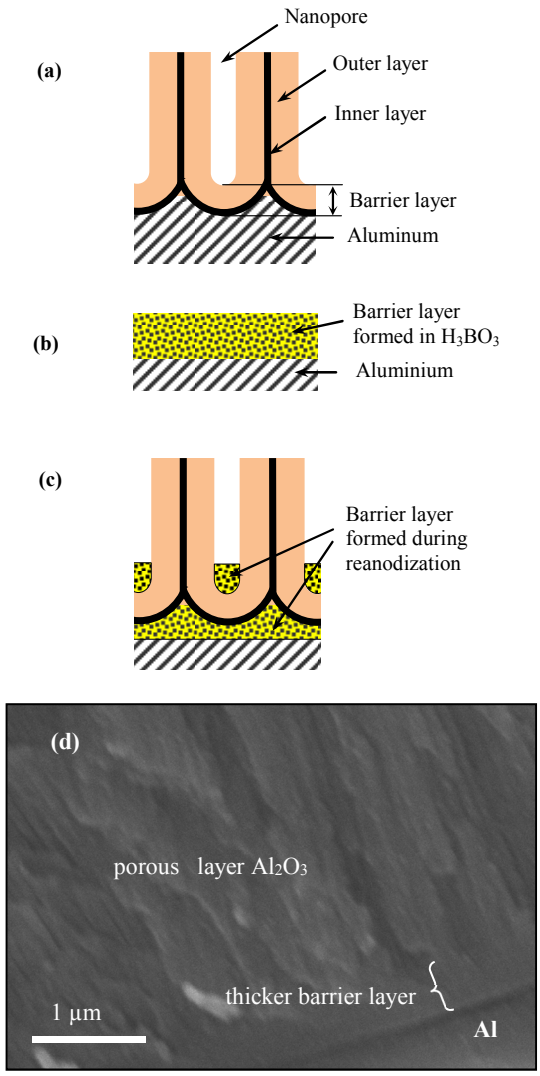

Fig. 1. Schematic representation of the structure of porous (a), barrier (b) and complex (c) anodic aluminium oxide films and (d) for additional illustration, a SEM image is presented illustrating complex AAO prepared by initial porous anodization in 2 % oxalic acid solution and then reanodized in aqueous borate electrolyte

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For example, the insulation resistance of the complex films is proved to be hundredfold higher and dielectric breakdown voltages twice higher than those of the dense films [1, 3]. Comparatively higher values for the specific electric resistance and the effective dielectric constant of the complex films have also been reported [6]. Our preceding results concerning metal/complex film/air present significant increase of the breakdown voltages of porous AAO after reanodization [7].

Most often during investigation of the complex films properties, the porous Al_2O_3 template is produced under one and the same experimental conditions (electrolyte solution of concrete acid, current density or formation voltage, duration and temperature). Therefore, it is of certain interest to estimate the effect of the nature of pore-forming acid on the kinetics of PAA reanodization.

II. EXPERIMENTAL

Growth of porous anodic alumina

Aluminium foil samples (99.9 % Al) having working area of 8 cm^2 were initially electropolished in a phosphoric acid-chromic acid solution at enhanced temperature. According to Keller et al. [8] PAA having equal porosity and thickness were formed in aqueous solutions of three acids – 15 % w. H_2SO_4, 2 % w. $H_2C_2O_4$ and 3 % w. H_2CrO_4. A two-electrode electrolytic cell was assembled for PAA formation, featuring as counter electrodes a lead plate to anodize in H_2SO_4 and $H_2C_2O_4$ as well as a stainless steel plate to anodize in H_2CrO_4. The experimental conditions to accomplish equal porosity covered certain values of voltage and temperature and they are presented in Table 1. The formation voltage was ensured by DC power supply TEC 3. Both the initial current and electrolytic cell voltage drop were regulated by series decade-box variable resistor. PAA of approximately equal thickness (≈ 2.2 μm) were produced by varying the anodization time.

TABLE 1. VALUES OF THE WORKING PARAMETERS DURING THE GROWTH OF PAA ACCORDING TO [8]

Electrolytic solution	15% H_2SO_4	2% $H_2C_2O_4$	3% H_2CrO_4
U (V)	17.2 –17.3	20.7 – 21.0	22.8 – 22.9
I (mA)	115	24	20
t (°C)	10	24	37
Porosity (%)	7		

Reanodization of PAA

Reanodization took place in non-dissolving the film 2.5 % H_3BO_3 (pH 6) aqueous solution, so called aqueous borate electrolyte (ABE). The process was accomplished at 20°C by applying two current densities (1×10^{-3} и 5×10^{-3} A cm^{-2}).

The formation of the complex films was carried out in a two-electrode cell with a platinum mesh serving as a counter electrode, using a home-made high voltage DC galvanostat (600 V, 0.5 A). Kinetic curves, i.e. dependencies of the reanodization voltage on time were registered with a precision multimeter (Mastech MS 8050) and a PC-based data acquisition system.

III. RESULTS AND DISCUSSION

It is known [9-13] that during the formation of PAA various quantities of electrolyte anionic species are incorporated into the outer layer of porous film. This fact gives a reason to assume that electrical, physicochemical as well as mechanical properties of PAAs formed in solutions of various acids would be different.

In fig. 2 and fig. 3 kinetic voltage-time curves of reanodization of PAA formed in aqueous solutions of H_2SO_4, $H_2C_2O_4$ and H_2CrO_4 are presented. The current density is kept constant during both measurements and its values are 1×10^{-3} and 5×10^{-3} A cm^{-2}, respectively. The voltage values are corrected by the voltage drop (U_0) at $t = 0$ due to the initial barrier layer being a part of PAA. Linear increase in the reanodization voltage up to 200V and a clearly visible distinct between the slopes of reanodization and that of barrier (non-porous) anodization are observed in both figures. This difference in the slopes is owing to the higher electric field strength, i.e. higher real current density through pore bottom. Concerning the higher reanodization current density supplied (5×10^{-3} A cm^{-2}, fig.3), the slopes seem more abrupt than when implementing 1×10^{-3} A cm^{-2} both during reanodization and direct barrier anodization of bare aluminium.

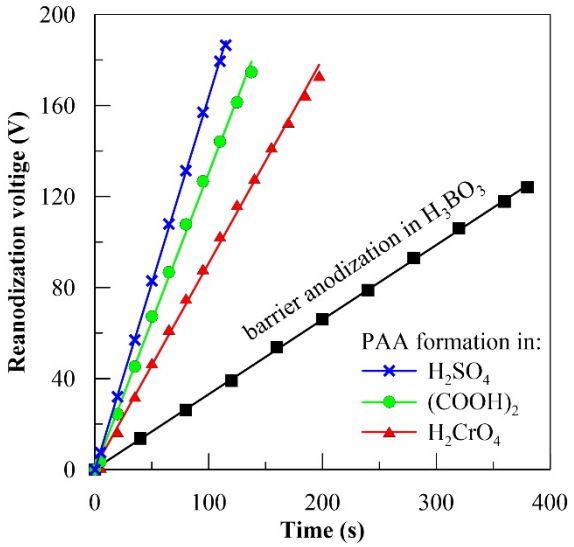

Fig. 2. Kinetic curves of galvanostatic (1×10-3 A cm-2) reanodization of PAA grown in three electrolyte solutions. Aqueous borate electrolyte (ABE) is used for reanodization. For comparison, a kinetic curve of barrier anodization of bare aluminium in ABE at the same current density is presented.

Taking the reanodization curves on both figures into consideration, one could clearly observe a difference in the rates of voltage increase vs. time, depending on the electrolyte for PAA growth. The slope $\partial U/\partial t$ decreases in the order:

$$H_2SO_4 > H_2C_2O_4 > H_2CrO_4,$$

for both current densities (Table. 2). Since PAA possess equal porosity (α = 7%) [8], the effect ascertained is probably due to the anionic species incorporated from electrolyte solution into PAA.

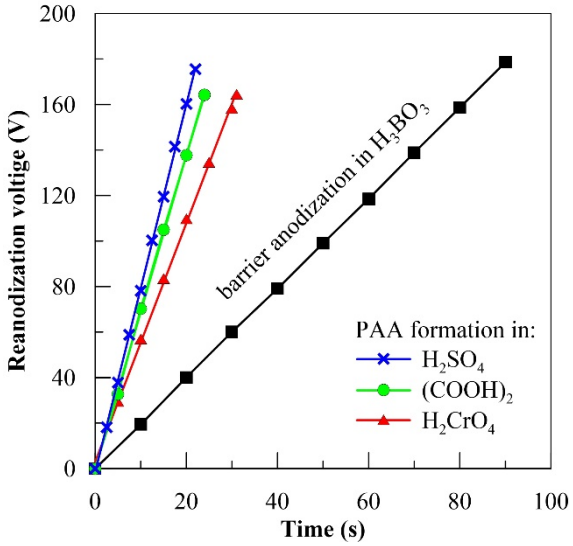

Fig. 3. Kinetic curves of galvanostatic (5×10^{-3} A cm^{-2}) reanodization of PAA grown in three electrolyte solutions. Aqueous borate electrolyte (ABE) is used for reanodization. For comparison, a kinetic curve of barrier anodization of bare aluminium in ABE at the same current density is presented.

TABLE 2. VALUES OF THE SLOPE $\partial U/\partial t$ OF KINETIC CURVES IN GALVANOSTATIC (1×10^{-3} AND 5×10^{-3} A CM^{-2}) REANODIZATION OF PAA GROWN IN THREE ELECTROLYTE SOLUTIONS.

Electrolytic solution	$\partial U/\partial t$	
	1×10^{-3} A cm^{-2}	5×10^{-3} A cm^{-2}
15% H_2SO_4	1.64	8.08
2% $H_2C_2O_4$	1.30	6.89
3% H_2CrO_4	0.90	5.24
borate electrolyte (ABE)	0.33	1.98

It is obvious in Table 2 that fivefold increase of the reanodization current density leads to enhancement of the slopes $\partial U/\partial t$ of kinetic curves equal to 4.93 times for H_2SO_4 and 5.8 times for H_2CrO_4 , in respect to direct barrier anodization revealing the largest (six times) slope enhancement. There is notable increase of slopes difference related to probable effect of incorporated anions in PAA.

The effect of incorporated anionic species into PAA is of significant interest. Therefore, it is worth to subject it to more detailed consideration. Thompson and Wood [9] have shown that various film-dissolving electrolytes incorporate different anionic quantities into PAA. The incorporation proceeds by inward migration from electrolyte solution towards PAA under the electric field applied. As a result, two sub-layers are outlined – outer wherein anion incorporation occurs and inner, which is free of anions, i.e. it represents pure Al_2O_3 (fig. 1a). The amount and dissemination of acidic ions within PAA depends on the anodization potential/current density, electrolyte concentration, temperature and ionic mobility [10]. Because PAA are formed by applying almost equal voltages (U = 17.2 ÷ 22.8V), it would be expected that the anion quantity and distribution within outer layer PAA should depend mainly on the nature and concentration and of the electrolyte and temperature. The concentration of H_2SO_4 in most cases is manifold higher and the mobility of SO_4^{2-} is known as the highest one [11] compared to other acids used. Therefore, a largest amount of SO_4^{2-} distributed within barrier layer of PAA, i.e. the thickest outer sub-layer would be expected as well. According to Thompson and Wood [9] the depth of anionic species permeation decreases in the order:

$$H_2SO_4 > H_2C_2O_4 > H_3PO_4 > H_2CrO_4.$$

The rates of PAA formation decrease in the same order. The results in fig.2 and fig. 3 completely correspond to this concept even in the case of galvanostatic reanodization; the decrease of the slopes follows the above described order. This means that PAA formed in sulfuric acid, where the thinnest inner anion-free layer appears, is expected to reveal ionic conductivity at highest field strength. Concerning both anodic current densities, reanodization of PAA formed in H_2SO_4 occurs most rapidly in relation to other two acids.

By increase of the reanodization current density the rate of barrier layer growth, i.e. the formation of composite anodic oxides rises (fig. 3). The slopes of the kinetic curves draw closer to each other. Nevertheless, the presumable effect of the nature of anionic species incorporated into PAA is retained at higher reanodization current density. Therefore, one could assume that this effect is somewhat more pronounced in the occurrence of lower field strengths.

IV. CONCLUSION

During reanodization of porous anodic aluminium oxides (PAA templates) grown in aqueous solutions of H_2SO_4, $H_2C_2O_4$ and H_2CrO_4 and having equal porosity the following results could be specified:

- Reanodization voltage increases linearly up to 200 V by application of reanodization current densities 10^{-3} и 5×10^{-3} A cm^{-2}.
- The rate of voltage increase depends on the nature of electrolyte for PAA formation. A probable explanation is given concerning the nature, quantity and permeation depth of the anionic species incorporated into PAA.
- The effect of anions incorporated diminishes at higher reanodization current density.

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Experimental study of the melting of a solder paste

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Abstract – The report presents the results of a study of the melting of various solder pastes. The temperature distribution over time with convection heating, conductive and radiant was investigated. Sources of different heat output and different heating speeds were used. The results of cooling the paste are also presented.

Keywords – **soldering, solder paste, surface mounting, temperature profile**

I. Introduction

The literature presents a number of studies on the conditions in conducting the soldering process in surface mounting [1, 2, 3]. Thermal profiles of various components [4] have been studied, depending on the component mass, the type of heating [5] and the printed circuit board used [6]. Primary attention is paid to the temperature profile of the oven [7], the purpose of which is to obtain the recommended temperature profile in time for the solder paste [8].

A. Solder pastes

In practice, different pastes are used both by the type of solder bar, for example lead [9, 10], lead free, base Sn / Cu [11, 12] lead free, base Sn / Bi [13,14]. According to the type of flux, they are neutral or active flux [9, 11], no clean [10, 12], water-soluble [15]. The solder bar in the paste determines the melting temperature and the necessary excess to obtain a complete wetting and the flux is responsible for the cleaning of the soldering elements, their wetting and oxidation protection.

B. Soldering

Welding is done by heating the elements and heating the solder bar to the required temperature. Heat supply is carried out by means of soldering irons [16], convectionally by hot gas [17, 18], radiant [19], the mechanisms themselves being well studied theoretically and experimentally.
Relatively few sources are presenting the results of melting the paste itself.

II. Experiments

Five types of pastes with different solder and flux contents were used to carry out the experiments. The selected pastes have a different melting point and massive use. These are given in Table. 1.

Table 1. Tested solder pastes

Sample	Type	Composition	Company
SP1	BSA04-XSP	Bi57,6Sn42Ag0,4	Cobar
SP2	DP5600	LMPA^{TM}-Q	Interflux
SP3	DP5505	Sn62Pb36Ag2	Interflux
SP4	PF629-P30	SAC	Shenmao
SP5	PF629-P3	Sn99Ab0,3Cu0,7	Shenmao

The paste heating was performed conductively via the 8-157-02 Mulle equipment company USA heating table. Radiant heating uses a non-standard system comprising a 150 watt halogen source and an optical system consisting of a spherical mirror and a condenser. The focusing field of the system is 25x15 mm.

For the experiments, the same amount of paste (0,34 g) was used. The same is placed on the respective heating base and the thermocouple is placed in it. For experiments we used FR4, the base of the bonder, a non-standard holder (crucible) with a small heat mass allowing quick displacement to change the cooling rate.

Measurements were performed with UT109 multimer with RS232 interface and recording over 220 ms.

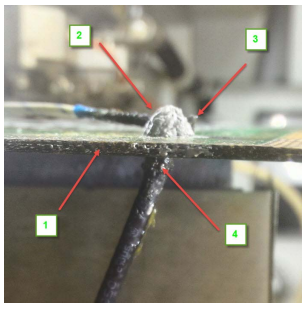

Fig. 1. Melting of paste over FR4. 1-plate, 2-paste, 3-thermocouple, 4- thermocouple.

In part of the experiments, in addition to the thermocouple in the paste, a second control thermocouple is used in the immediate vicinity of the solder bar.

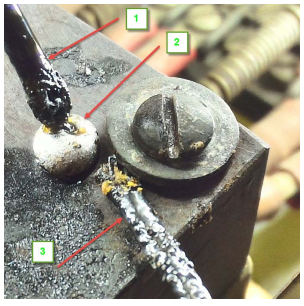

Fig. 2. Melting of the paste on a bonder table. 1 - thermocouple, 2 - ball of melted paste, 3 - thermocouple control.

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For quick cooling a movable paste holder is used.

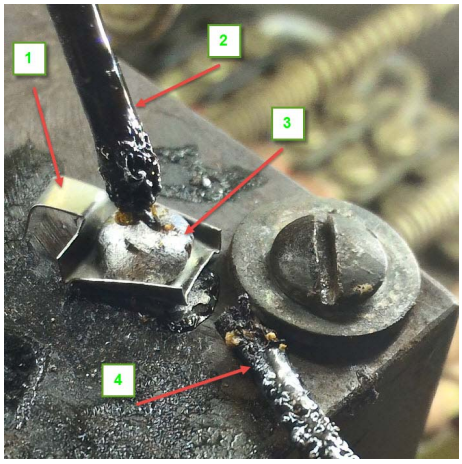

Fig. 3. Melting the paste into a crucible. 1 - crucible, 2 - measuring thermocouple, 3 - ball solder, 4 - thermocouple control.

For checking the influence of the flux, a soldering with an original flux was carried out.

Fig. 4 Stage of solder paste melting with original flux in large crucible.

The same dose of paste was then repeatedly treated with a solution of alcohol and acetone to recover the flux.

Fig. 5. Non-eutectic paste after washing the original flux.

And then another flux is added.

Fig. 6. Paste after adding a new flux .

The study of the thermocouples is done by placing them in the focus of the optic system. To reduce the influence of thermocouple heating on its base, it is protected with aluminum reflective foil.

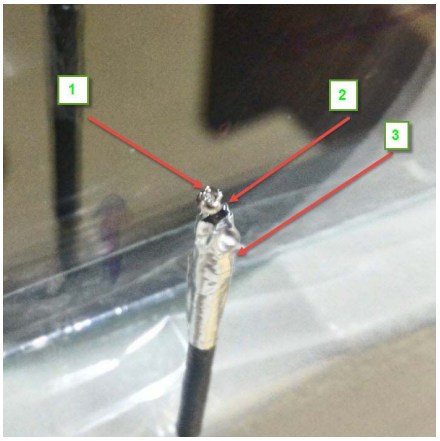

Fig. 7. Thermocouple in optical focus of soldering unit. 1 - solder ball, 2 thermocouple, 3 thermal screen.

III. EXPERIMENTAL RESULTS

The initial cycle involves removing the temperature profile by heating only the thermocouple (wetted with the former from the previous measurements - Fig.3) and the subsequent three welding cycles 1, 2, 3 of two heatings. Each cycle comprises dosing a paste, heating to melting, and cooling, reheating to melt the resulting solder ball with subsequent cooling. The heating was performed optically.

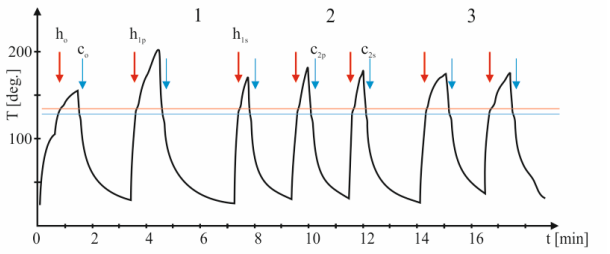

Fig. 8. Thermal profile for optically heated thermocouple with paste addition.

In all cycles, the point of melting of the solder bar is clearly identified at the local change in the slope of the curve (h_x, c_x). Similarly, the curing time is also identified.

To confirm the melting point of a wet thermocouple, two thermocouples are made - wetted and non-wetted.

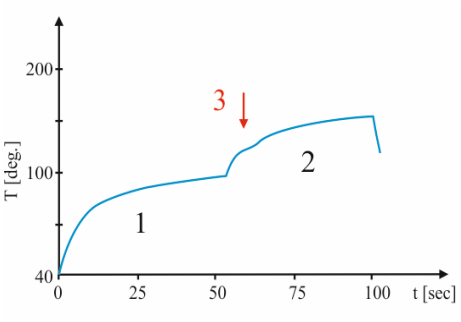

Fig. 9. Profile of the thermocouple with wet surface.

To reliably confirm the influence of the thermocouple wetting, an optical heating at 75 W with extended irradiation is achieved until stationary heating is reached and then the power is doubled.

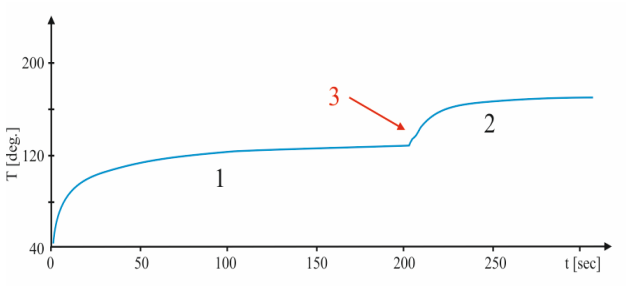

Fig. 10. Profile of the thermocouple with wet surface.

The transition with a changed slope is again observed, confirming the effect of the wetting.

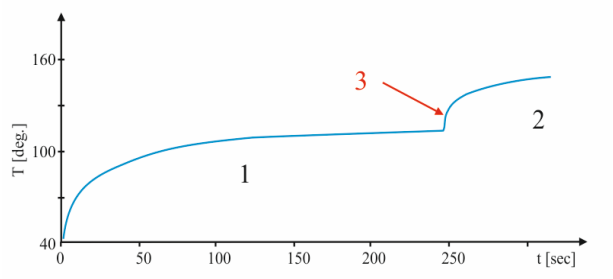

Fig. 11. Profile of the thermocouple not soaked no plateau
In a non-wet thermocouple (figure above) such effect is not observed.

Specific effects are observed when comparing the zones hx (arrow 3) and cx from Fig. 8. In the initial melting of the paste (cycle 1, Fig. 12) the melting zone is smoother and the area with a reduced slope is smaller than the melting of an already obtained ball of solder (loop 2).

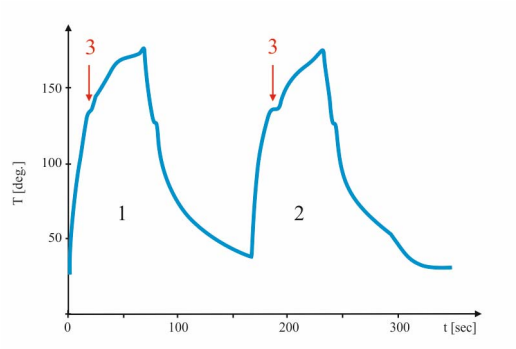

Fig. 12. Profile of the thermocouple for paste-ball cycles.

When cooling the thermocouple, the effects are identical (Figure 12). This is logical, insofar as in both cases we have hardening of the molten solder bar.

Verification of the effect found was carried out by analogous experiments carried out with a conductive welding method on the bonder heating mass. A typical curve is shown in Fig. 13, where the melting zone of the paste is sh, and the solder bole is bh.

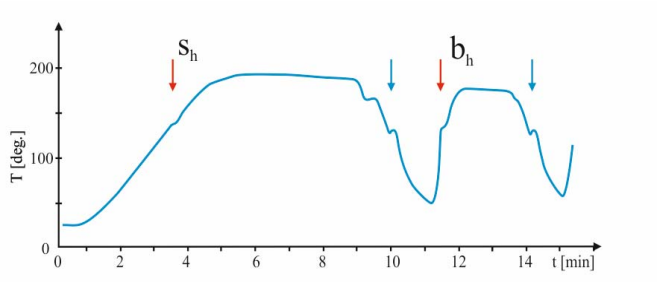

Fig. 13. Conductive melting of non-eutectic paste.

Fig. 14 shows a fragment of the paste and ball melt process using the same solder bar with different flux. The above effects have been confirmed.

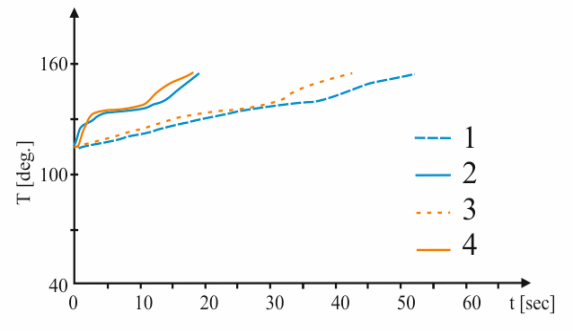

Fig. 14. Heat of paste conductively. 1 - paste with original flux,2 - ball from paste with original flux, 3- paste with changeover flux, 4- ball after shift flux.

The detailed analysis of cooling in a conductive process (Fig.15) confirms the equal course of the temperature curve, regardless of the initial heating and the flux used.

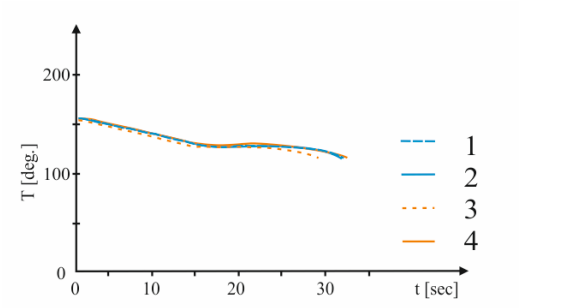

Fig. 15. Cooling not on the heater, but on the air.

IV. ACKNOWLEDGEMENT

The authors would like to acknowledge the contribution of the companie UniPOS Ltd. by material resources and to thank their teams for their support of the experimental work.

V. CONCLUSION

The mechanism of melting of solder paste and solder bar is different. Solder paste requires a longer melting time than a soldering bar and is slowly tempered. The mechanism of melting of a solder paste is not materially influenced by the type of flux. The type of flux influences the way the individual balls melt in the total mass of the non-eutectic solder paste (LMPA paste). The curing of the molten solder is the same mechanism and is not influenced by the flux. This applies to all types of solder paste and solder bars.

The above conclusions are important for using of solder pastes and solder bars for repair technologies and various soldering technologies - Pin in Paste, Hot Bar, Robots soldering, laser soldering, reflow, vacuum soldering, vapor phase soldering, hand soldering and more. They will also be useful in creating new soldering materials and fluxes.

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Extraction of Modified Butterworth – Van Dyke Model of FBAR Based on FEM Analysis

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Abstract – **This paper presents a methodology for extraction of modified Butterworth-Van Dyke model (mBVD) parameters of thin-film bulk acoustic wave resonator (FBAR) using finite elements method (FEM) analysis. Simple FBAR model is developed and its frequency characteristic is obtained through FEM simulations. Then the mBVD model parameters are calculated and further optimized to fit its frequency response to those from FEM analysis with less than 1% relative error.**

Keywords – **FBAR, mBVD, FEM analysis, BAW resonator.**

I. Introduction

In last decades thin-film bulk acoustic wave resonators (FBAR) gained popularity due to its applications in RF filters and oscillators for wireless communications and the diversity of sensors applications [1]. Initially FBAR has been used in duplexers but due to their high quality factors, good temperature stability and low losses they were implemented in other communications devices. FBAR are effectively used in RF range starting from several hundreds of MHz till 2GHz but even applications at 5GHz are reported. Their other advantages are compatibility with standard CMOS process, and capability to process higher powers of the signal.

Typical FBAR architecture, shown in Fig. 1, consists of a sandwich structure with two metal electrodes and piezoelectric in between, placed over a silicon substrate [2], [3]. FBAR utilizes bulk acoustic waves propagating through the bulk structure of the piezoelectric layer. Aluminum nitride (AlN) or zinc oxide (ZnO) are used for piezoelectric layer composition, but lead zirconate titanate (PZT) is also reported as FBAR piezoelectric in some researches, while metal electrodes are made from aluminum, platinum, titanium, etc.

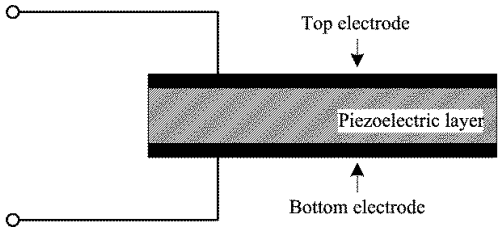

Fig. 1. FBAR cross section view.

Butterworth – Van Dyke (BVD) model is most often used for FBAR description during the design process. It is used for determining the FBAR characteristics in the schematic design and simulations as well. The equivalent BVD circuit of a classical FBAR utilize RLC acoustic arm with one capacitor in parallel. In his research in 1999 [4] Ruby introduced the modified BVD (mBVD) circuit by adding two additional resistors to the conventional BVD model describing more accurately the loss mechanisms in the resonator. The mBVD demonstrates improved accuracy between measured results and extracted model parameters.

The goal of this paper is consideration of the relationships between physical modeling of FBAR, based on finite element method analysis, and its electrical mBVD model. COMSOL Multiphysics software [5] is used for FEM analysis, aiming to characterize the current through the device in the frequency domain. The results, received from COMSOL are used for extraction of mBVD model parameters. Then the values of those parameters are refined by comparison of the frequency characteristics of the mBVD model with those, received from COMSOL.

II. mBVD Circuit of FBAR

The equivalent BVD circuit used for modeling of FBAR electrical parameters is shown in Fig. 2 (a). The standard BVD circuit contains acoustic (or motional) RLC arm and parallel capacitance C_0. The so called "motional tract" of the BVD circuit, consisting of motional capacitance C_m, resistance R_m and inductance L_m, represents the propagation of acoustic wave in the piezoelectric material and defines the acoustic properties of the resonator [2]. Static capacitance C_0 gives the equivalent electrical capacitance formed between top and bottom electrodes within the FBAR structure.

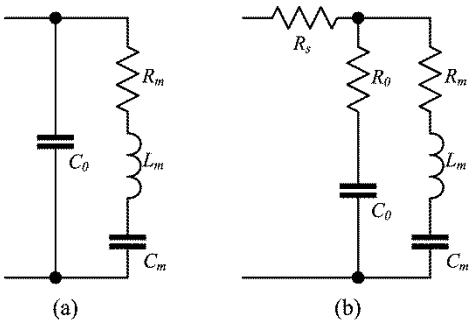

Fig. 2. (a) Equivalent Butterworth-Van Dyke circuit of FBAR; (b) the modified Butterworth-Van Dyke circuit.

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The following formulas give the relationships between BVD elements and FBAR physical parameters [6]:

$$C_m = \frac{8C_0 k_{eff}^2}{N^2\pi^2} \quad (1)$$

$$L_m = \frac{\upsilon}{64.f_s^3.\varepsilon.A.k_{eff}^2} \quad (2)$$

$$R_m = \frac{\eta.\varepsilon}{16.f_s.\rho.A.\upsilon.k_{eff}^2} \quad (3)$$

$$C_0 = \frac{\varepsilon A}{\tau} \quad (4)$$

where k^2_{eff} is the electromechanical coupling coefficient, A and τ are plate electrodes area and thickness respectively, ε is piezoelectric permittivity, η is acoustic viscosity of the wave factor k, υ is wave velocity and N shows acoustic mode number ($N = 1, 3, 5$ ...).

In comparison to the standard BVD, the modified BVD model (Fig. 2 (b)) has two additional loss resistors (R_0 and R_s) giving better fitting between frequency responses of the FBAR and the mBVD model. Both resistors depend on the specific FBAR geometry. In general R_s models the ohmic resistance of the electrodes, while R_0 helps for better description of acoustic losses when the circuit is in parallel resonance. In fact, the acoustic resistor R_m also models acoustic losses, but it affects predominately the series resonance. It has effect also in the frequency area around the parallel resonance, but it cannot define entirely the frequency behavior in this area and for this reason R_0 is introduced. The analysis of the mBVD impedance in Fig. 2(b) gives the following two formulas for FBAR impedance [6]:

$$Z = R_s + \frac{(1+s\tau_p)(s^2+s\omega_s/Q_s+\omega_s^2)}{sC_0(s^2+s\omega_p/Q_p+\omega_p^2)} \quad (5)$$

$$Z = \frac{(1+s\tau_{p0})(s^2+s\omega_{s0}/Q_{s0}+\omega_{s0}^2)}{sC_0(s^2+s\omega_{p0}/Q_{p0}+\omega_p^2)} \quad (6)$$

The resistance R_s is separated in the first formula, while in the second it is included in the general expression. The dependency of resonance frequencies ω_s and ω_p from circuit parameters are given with the expressions [3]:

$$\omega_s = \frac{1}{\sqrt{L_m C_m}}; \quad \omega_p = \sqrt{\frac{C_m+C_0}{L_m C_m C_0}} = \omega_p\sqrt{1+\frac{C_m}{C_o}} \quad (7)$$

The resistance R_s changes the series resonance frequency and in the general expression (6) this frequency is marked by ω_{s0}. Both frequencies ω_s and ω_{s0} differ slightly and there is no exact formula connecting ω_{s0} with mBVD elements.

In mBVD circuit three quality factors could be defined – Q_p (quality factor of the parallel resonance), $Q_s = \omega_s L_m/R_m$ (quality factor of the series circuit $R_mL_mC_m$) and Q_{s0} (quality factor of the series resonance for the whole circuit including resistors R_0 and R_s). They are represented with the following relationships [6]:

$$Q_p = Q_s\frac{\omega_p/\omega_s}{(1+R_0/R_m)}; \quad Q_{s0} = \frac{Q_s}{(1+R_s/R_m)} \quad (8)$$

Generally, Q_s is always bigger than Q_p because ω_s/ω_p ratio varies between 1 and 1.03 while R_0/R_m is from 0.1 to 0.3. Also the effect of R_0 over the Q_{s0} is very small so it is disregarded in the expression (8).

Time constants $\tau_p = R_0C_0$ and τ_{p0} (there is no expression for it) changes the impedance magnitude by less than 2% and phase by up to 3° around the resonance frequencies [6]. The following expression for τ_p can be derived from formulas (7) and (8):

$$\tau_p = \frac{1}{\omega_p^2-\omega_s^2}\left(\frac{\omega_p}{Q_p}-\frac{\omega_s}{Q_s}\right). \quad (9)$$

III. Finite Element Method Analysis of the FBAR

For the purposes of this study an FBAR having a form of parallelepiped is investigated. Its sizes are: 2.9 μm thick AlN piezoelectric layer with length of 50 μm and width of 155μm (Fig. 3(a)). Above and below the piezoelectric layer are the Al electrodes with 0.05 μm thickness.

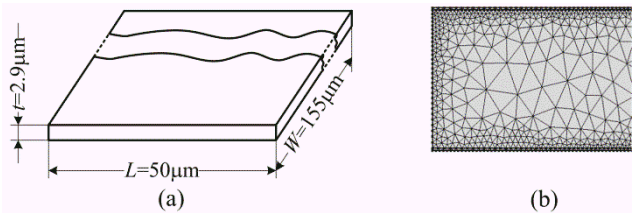

Fig. 3. (a) The sizes of the considered FBAR; (b) The mesh created by COMSOL.

Simulations of FBAR in COMSOL Multiphysics are based on FEM analysis. It is typically used to predict the behavior of complex models with complicated geometries and material properties, where the analytical approach could not lead to any solutions. FEM analysis supposes dividing of the analyzed object into elements with finite sizes forming a mesh and equalizing of the conditions at their boundaries. For the aim of the study presented here automatic division into elements created by COMSOL is used, which could be seen in Fig. 3(b). The mesh is relatively rough in the inner part of the resonator and it is finer in the boundary areas and across the piezoelectric layer-electrode interconnects, where better accuracy is required.

The goal of the FEM analysis, done here, is extraction of the harmonic response of the model when it is excited by an external signal. Current FBAR model is designed to resonate freely in all directions since there is no boundary conditions set for its outer walls. A sinusoidal voltage V_0 with 1 mV amplitude is applied between the electrodes.

The FBAR simulation with COMSOL includes frequency domain analysis of the resonator by varying the frequency of the voltage between the electrodes aiming to obtain the FBAR frequency response and from them – its series and parallel resonance frequencies. Frequency analysis is performed within the range of (1.82 – 1.9) GHz where the two resonance frequencies should appear based on preliminary approximate calculations. The frequency of the input voltage is changed with 10 kHz step – in fact this is the initial accuracy of determining of the resonance frequencies.

The complete characterization of the device supposes performing 3D analysis, which requires large computational resources. As far as the FBAR behavior is homogeneous through its width W, a 2D analysis is applied here, which allows significant reduction of the calculations. Since the third dimension of the model is not defined in the 2D simulations, all results are given as densities per unit width (per 1 m). Here the current through the FBAR is needed in order to receive its impedance. Therefore it is necessary to multiply the current density (given by COMSOL) by the real width (155 μm) of the device. Then the FBAR impedance or admittance can be calculated easily by using the Ohm low.

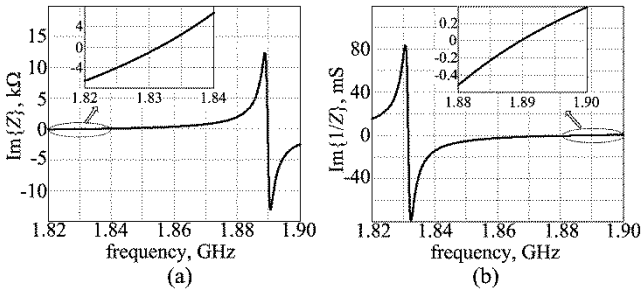

Fig. 4. Imaginary parts of FBAR impedance (a) and admittance (b).

Fig. 4(a) shows the imaginary part of the impedance received using this approach. It is more informative than the real part due to high Q-value, typical for FBAR resonators. The point, where this curve crosses the zero, gives approximately the series resonance frequency. The parallel resonance frequency can be determined from the zero-crossing point of the FBAR admittance shown in Fig. 4(b). From Fig. 4 and from numerical data the resonance frequencies are obtained: f_s = 1.83161GHz and f_p = 1.88976GHz ($f = \omega/(2\pi)$).

However these values are not the exact values of the resonance frequencies in formula (5), from which the elements of the mBVD can be calculated. There is small error due to the masking effect of the real part of the impedance.

IV. Extraction of mBVD Parameters

A. Initial Approximation of mBVD Parameters

The elements of the mBVD model can be calculated from the relationships between them and the impedance parameters ω_s, ω_p, Q_s, Q_p, τ_p, C_0 and R_s given by formulas (7) and (8). Their values will be found in two steps. First, considering the results from COMSOL, approximate values for parameters will be calculated (for resonance frequencies this was done in the previous section). Then, by comparing the frequency responses from COMSOL and the one calculated from mBVD parameters using formula (5) and minimizing the relative error between them, these values will be determined more precisely. All calculations from here on are done in MATLAB.

For frequencies much lower than resonance frequencies $Z \approx R_s + \omega_s^2/(j\omega C_0\omega_p^2)$ and for frequency much above them $Z \approx R_s + 1/(j\omega C_0)$ (the effect of τ_p is neglected). Thus the imaginary part of the admittance approximately tends to ωC_0 when $\omega \to 0$ and $\omega \to \infty$. For calculation of C_0 the FBAR frequency characteristics is simulated with COMSOL in extended frequency range from 0.5 – 4 GHz and from this simulation $\mathrm{Im}\{1/Z\}/\omega$ as function of the frequency (Fig. 5 (a)) is plotted. The approximate value of C_0 is taken as average between the values at 0.5GHz and 4GHz and it is 213.4fF.

The value of R_s can be calculated in a similar way. It follows from (5) that at very low frequencies the real part of the impedance is approximately equal to R_s. Fig. 5 (b) shows the real part of Z in the range 0.5-1GHz and from it $R_s \approx 0.09\Omega$ is determined.

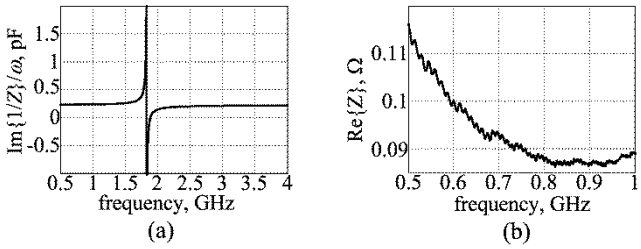

Fig. 5. Determining of C_0 and R_s: (a) The imaginary part of the admittance, divided by ω; (b) The real part of the impedance.

The Q-factors can be received by two methods. The first one is to plot the dependence $|Z(\omega)|$ using logarithmic scale for $|Z|$ (in dBOhms, relating to 1Ω). Then Q_{s0} can be calculated from ω_s and the frequencies ω_1 and ω_2, where $|Z|$ increases by 3dB from its value at ω_s: $Q_{s0} = \omega_s/(\omega_2-\omega_1)$. The quality factor Q_p can be found similarly from ω_p and the frequencies, where $|Z|$ decreases by 3dB from the value at ω_p. The second approach for determining Q_s is to use the slope of the phase characteristic of the impedance. The first approach is used in this paper. The dependence $|Z(\omega)|$ is shown in Fig. 6 and from it Q_{s0} = 1006 and Q_p = 1080 are found. There are no other arguments for determining Q_s except the relationship $Q_s > Q_p$ proved above. For this reason the initial guess for Q_s is chosen arbitrarily as Q_s = 1300 and its value will be improved later.

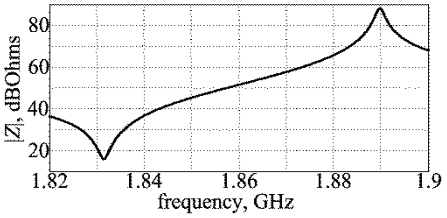

Fig. 6. The dependence $|Z(f)|$ using logarithmic scale for Z.

The received values of the resonance frequencies and Q-factors allow to calculate τ_p = 0.2435ps using formula (9).

B. Optimizing the mBVD Parameters

The best way for matching both frequency responses – the one obtained from COMSOL and the second calculated from mBVD model – is to minimize the relative difference between them. In fact the relative difference is the relative error of approximation of the real frequency response, received from COMSOL, with the mBVD model. The frequency response of the mBVD model can be calculated

by replacing the determined above parameters in formula (5). Then, by varying these parameters a minimization of the relative error will be achieved.

Let us first consider the relative error between the imaginary parts of the frequency responses, calculated as $(\mathrm{Im}\{Z_{mBVD}\}-\mathrm{Im}\{Z_{COMSOL}\})/\mathrm{Im}\{Z_{COMSOL}\}$. It is shown by dashed line in Fig. 7. It can be seen that the relative error is about 1% in the whole frequency range except around resonance frequencies. It can be reduced simply by increasing the capacitance C_0 by 1%, since C_0 divides the imaginary part of Z. Fig. 7 shows the result when C_0 is changed to 215.8fF – the error is very close to 0 for the curves with solid line.

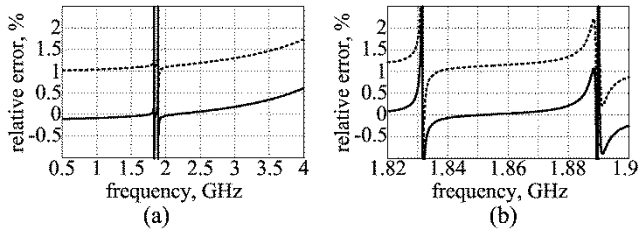

Fig. 7. Relative error of approximation of the imaginary part of the impedance. (a) In the frequency range 0.5-4GHz; (b) in the frequency range around resonance frequencies. The dashed lines are at C_0 = 213.4fF (the initial value), the solid lines are for C_0 = 215.8fF (improved value).

The large error around the resonances in Fig. 7 is due to determining of f_p and f_s with accuracy of 10 kHz. It could be reduced if increase the accuracy. Fig. 8 shows the effect of varying the kilohertz of their values – the error is decreased significantly. The more accurate values are f_s = 1.831602GHz and f_p = 1.889772GHz.

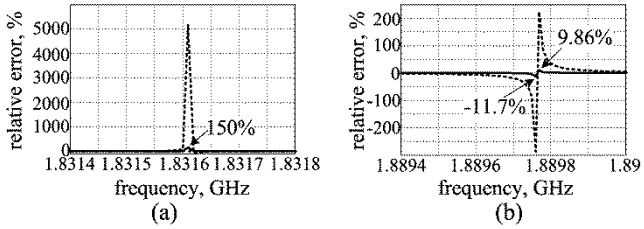

Fig. 8. Relative errors for imaginary parts of the impedance: (a) Around f_s; (b) around f_p. The dashed lines are for initial values f_s = 1.83161GHz and f_p = 1.88976GHz; solid lines are for more accurate f_s = 1.831602GHz and f_p = 1.889772GHz.

The real part of the impedance is influenced to great extent by the Q-factors and the resistance R_s. Thus the values of these parameters can be tuned by using the relative error for the real part of Z as criterion. Fig. 9 shows the effect of varying of R_s and Q_s on the error – the error reduction is significant in the area around resonances, when R_s is changed from 0.09Ω to 0.55Ω and Q_s – from 1300 to 1120. The other quality factor Q_p is also varied but without success and its value remains 1080. Regardless of the improvement, the relative error of the real part of the impedance is still large – several per cents in the area around the resonances and huge (thousands of percents) outside of this area. This means that mBVD model does not approximate the real part of FBAR impedance for frequencies far from resonances.

The elements of the mBVD model are calculated using the improved parameters. The corresponding formulas follow from (7) and (8):

$$C_m = C_0\left[\left(\frac{\omega_p}{\omega_s}\right)^2 - 1\right]; \quad L_m = \frac{1}{\omega_s^2 C_m}; \quad (10)$$

$$R_m = \frac{\omega_s L_m}{Q_s}; \quad R_0 = R_m\left(\frac{Q_s}{Q_p}\frac{\omega_p}{\omega_s} - 1\right). \quad (11)$$

The values, calculated with these formulas, are: C_m = 13.927fF; L_m = 0.54213μH; R_m = 5.5706Ω; and R_0 = 0.39045 Ω.

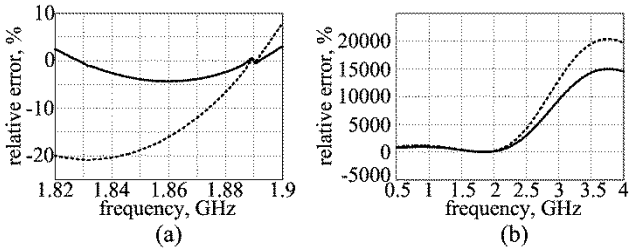

Fig. 9. Relative error in approximation of the real part of the impedance: (a) In the range around the resonances; (b) in wide frequency range. The dashed lines are for initial values R_s = 0.09Ω, Q_s = 1300; the solid lines are for improved values R_s = 0.55Ω, Q_s = 1120.

V. Conclusions

A methodology for deriving the parameters of the mBVD model of a FBAR from the results received by physical simulation based on FEM analysis is proposed. The extracted parameters give very good matching when compared to the FEM results especially for their imaginary parts, when the relative difference is less than 1%. It is also demonstrated that the resonance frequencies can be found with accuracy, better than the step between frequency points in the FEM analysis.

VI. Acknowledgments

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Study of Thermal Conductivity of Nanoporous Anodic Alumina Layer Formed in Sulphuric Acid Using Steady-State Heat Flow Technique

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Abstract – **The paper presents the results of studies of thermal characteristics of nanoporous anodic alumina layer formed in sulphuric acid. One-sided heating of aluminum boards by heating element from carbon filament was used. The temperature of the back side of the board was kept constant by using an aluminum heatsink. Thermograms of aluminum board surface were taken by thermal imaging camera MobIR M4.**

Keywords – **Nanoporous Anodic Alumina, Sulphuric acid, Heat transfer, Thermal conductivity**

I. INTRODUCTION

For modern micro and nanoelectronics, one of the important tasks is the creation of functional nanomaterials with given characteristics [1-3]. For this, an approach based on the fabrication of composite materials by placing nanoparticles in a porous matrix is applied [4]. One of the promising materials for use as such matrices is nanoporous anodic alumina. Geometric parameters of porous anodic alumina (pore diameter, interpore distance, film thickness) can be varied by changing the anodizing modes. An important advantage of such a material is the invariability of the characteristics of the porous structure of the anodic oxide up to a temperature of 1000 °C [5]. Due to the dielectric properties and good thermal conductivity, porous anodic alumina has a high potential for use in board printing technology. In [6, 7] it was shown that the use of printed circuit boards (PCB) with a metal core for high-power LEDs, in which the anodic alumina layer was used as an insulating layer, has allowed to improve the thermal dissipation and lower the temperature of the LED junctions. For the wide application of nanoporous anodic alumina in PCB technology, information is needed on both its thermal characteristics and possible ways to improve them. However, due to the fact that the anodic alumina is obtained in the form of thin coating, it is not easy to carry out the direct measurements of the thermal conductivity using the appropriate technique.

The aim of present paper was to investigate the thermal conductivity of nanoporous anodic alumina films obtained in sulfuric acid for samples of a two-layer structure consisting of a thick aluminum layer and a thin layer of porous anodic alumina. Thermal measurements based on the steady-state method were used for the studies, when the temperature distribution in the sample was independent of time and the samples had a uniform temperature field in bulk. An electric heater in the form of a carbon filament was placed on the surface of a porous anodic alumina.

A. Experimental

The samples of aluminum plates of 0.8 mm thickness were 60 × 24 mm in size. In order to form insulator layer the aluminum substrate was anodized in 2.0 M aqueous solution of sulfuric acid at constant current density of 32 A m^{-2} and temperature of (10.0 ± 0.1) °C. This results in alumina layer of thickness 20 μm. In order to establish the heat properties of porous anodic alumina layer the surface of the board was heated by the carbon fiber. It allows achieving the homogeneous heating over the board surface. The reverse board side was kept constant by the aluminum radiator of large area. In order to produce heating elements carbon fiber with liner dimensions 80 μm (thickness) × 2 mm (width) × 72 mm (length) was used. The ends of the carbon fiber were covered by 30 μm-thickness copper layer for further bending during heater assembly. Carbon fiber was fixed by 80 μm-thickness prepreg on the surface of nanoporous alumina. The heating element with carbon fiber possessed electric resistance 60 Ω [8]. The non-cooling thermal imaging camera (MobIR M4) was used to study the heat field of the samples.

B. Results and Discussion

In order to estimate the thermal characteristics of the specimens the electrical carbon fiber heater was used. As can be seen from Fig. 1, the temperature distribution on the surface of aluminum board in case of 3.3 W of electrical power is homogeneous, i.e. without local overheating. The temperature gradient of the heater relative to the surface of the board is caused by the thermal conductivity of the nanoporous alumina.

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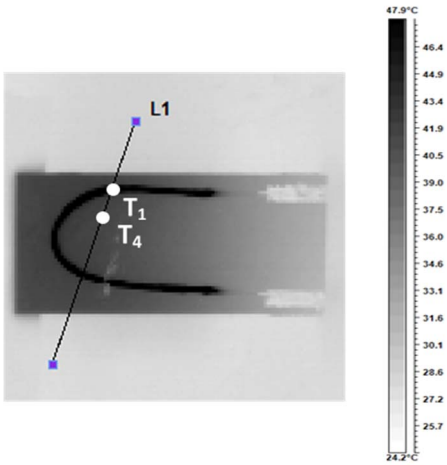

Fig. 1. The circuit board on aluminum with nanoporous alumina layer with carbon fiber heater under electrical power of 3.3 W in the thermal imaging camera measured in 50 s. L_1 is the given line with the control points of T_1 and T_4

For the heating element power of 3.3 W the temperature on the surface of the aluminum board reached 45.1 ºC and 66.1 ºC for carbon fiber in 50 s of heating respectively (Fig. 2).

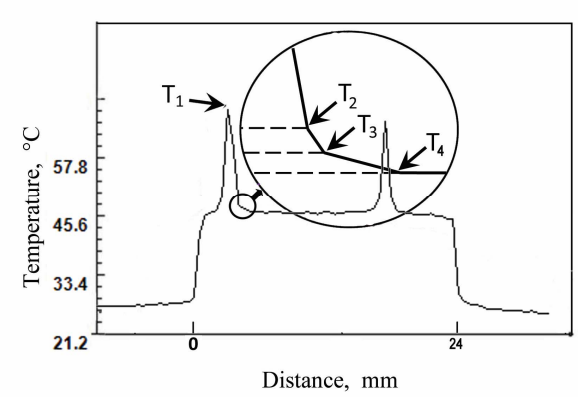

Fig. 2. The temperature distribution profile along the given line (see Fig. 1) for the aluminum board under electrical power of 3.3 W measured in 50 s. The insert shows the points which were chosen to determine the thermal conductivity of the nanoporous alumina: T_1 is the temperature of carbon fiber, T_2 and T_3 are the temperatures of nanoporous alumina layer at the interface with heater and aluminum, respectively, T_4 is an equilibrium temperature of the aluminum layer

For comparison, an experiment was performed with a heating power 2 times greater (6.6 W) than in Fig. 1. As can be seen from Fig. 3, in this case, as well as for an electric power of 3.3 W the thermal field is homogeneously disturbed over the surface of circuit board on aluminum with nanoporous alumina. For the heating element power of 6.6 W the temperature on the surface of the aluminum board reached 101.5 ºC and 57.7 ºC for carbon fiber in 50 s of heating respectively (Fig. 4). Table 1 shows the results of temperature measurements at control points T_1, T_2, T_3 and T_4 on the surface of an aluminum plate with nanoporous anodic alumina if an electric power is 3.3 and 6.6 W, respectively. As can be seen, an increase in the heating power by a factor of 2 leads to a 2-fold increase in the temperature gradient between the carbon filament and the surface of nanoporous anodic aluminum oxide, from 19.4 ºC to 40.6 ºC.

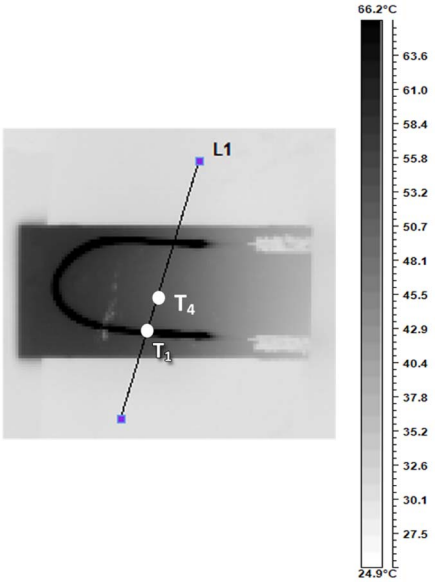

Fig. 3. The circuit board on aluminum with nanoporous alumina layer with carbon fiber heater under electrical power of 6.6 W in the thermal imaging camera measured in 50 s. L_1 is the given line with the control points of T_1 and T_4

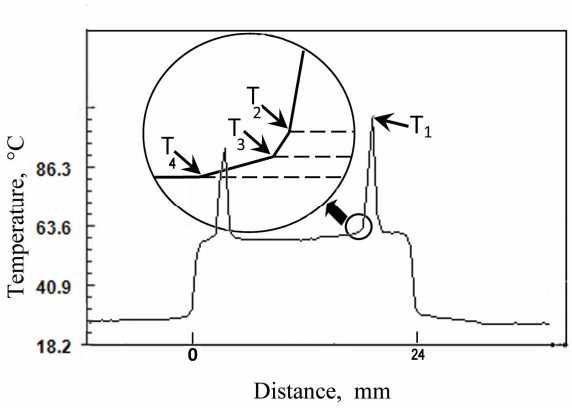

Fig. 4. The temperature distribution profile along the given line (see Fig. 1) for the aluminum board on under electrical power of 6.6 W measured in 50 s. The insert shows the points which were chosen to determine the thermal conductivity of the nanoporous alumina: T_1 is the temperature of carbon fiber, T_2 and T_3 are the temperatures of nanoporous alumina layer at the interface with heater and aluminum, respectively, T_4 is an equilibrium temperature of the aluminum layer

The graphs of temperature change with time for the control points T_1 (temperature of the carbon fiber) and T_4 (the equilibrium temperature of the aluminum layers) for the electric power 3.3 W and 6.6 are shown in Fig. 5. It can be seen that all the temperature curves pass to the saturation area after 30 s of heating. The results of the measurements of the changes in the temperature profile of the aluminum board at the interface with heating element allow

calculating the thermal conductivity of the nanoporous alumina layer.

TABLE 1. THE VALUES OF TEMPERATURE AT THE CONTROL POINTS OF T_1, T_2, T_3 AND T_4 FOR THE CIRCUIT BOARD ON ALUMINUM UNDER ELECTRICAL POWER OF 3.3 (FIG.2) AND 6.6 W (FIG.4)

Electrical power, W	3.3	6.6
Temperature of carbon fiber (T_1), °C	66.1	101.5
Temperature of nanoporous alumina layer at the interface with heater (T_2), °C	46.7	60.9
Temperature of nanoporous alumina layer at the interface with aluminum (T_3), °C	45.4	58.3
Equilibrium temperature of the aluminum layer (T_4), °C	45.1	57.7

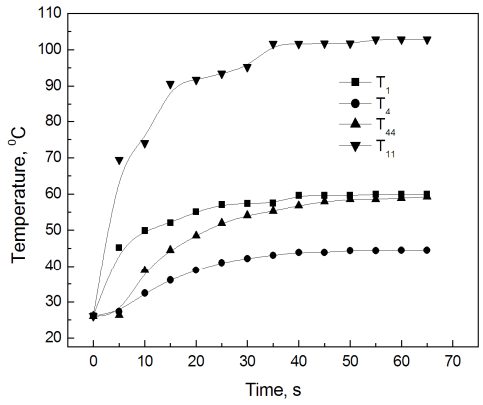

Fig. 5. The change in temperature at the control points T_1 and T_4 (Figs. 2 and 4) on the heating time for the aluminum board with nanoporous alumina layer under electrical power of 3.3 W (T_1, T_4) and 6.6 W (T_{11}, T_{44})

This means that temperature profile has inflection points that correspond to the temperature on the surface of alumina layer at the interface with heater (T_2), the temperature of the alumina layer at the interface with aluminum (T_3) and equilibrium temperature of the aluminum (T_4) (Figs. 2 and 4).

In case when thermal flow passing through the nanoporous alumina layer and aluminum one is the same and cross section is S, the following equation can be written:

$$\lambda_{Al}\frac{(T_3-T_4)}{d_{Al}}S=\lambda_{Al_2O_3}\frac{(T_2-T_3)}{d_{Al_2O_3}}S \qquad (1)$$

from where we can obtain the thermal conductivity of nanoporous alumina:

$$\lambda_{Al_2O_3}=\lambda_{Al}\frac{d_{Al_2O_3}(T_3-T_4)}{d_{Al}(T_2-T_3)} \qquad (2)$$

where $\lambda_{Al_2O_3}$ is the thermal conductivity of nanoporous alumina; λ_{Al} is the thermal conductivity of aluminum layer; $d_{Al_2O_3}$ is the thickness of nanoporous alumina layer; d_{Al} is the thickness of aluminum layer; T_2 and T_3 are the temperatures of nanoporous alumina layer at the interface with heater and aluminum, respectively; T_4 is an equilibrium temperature of the aluminum layer.

In accordance with equation (2) the value of the thermal conductivity of the nanoporous alumina measured in 50 s for 3.3 and 6.6 W (Table 1) was the same and equaled to 1.0 W K^{-1} m^{-1}. The following raw data were used: the thickness of alumina 20 μm; the thickness of aluminum 0.8 mm; thermal conductivity of AA3003 alloy 180 W K^{-1} m^{-1}. This result agrees with literature data for the thermal conductivity of sulphuric acid alumina 0.85–1.0 W K^{-1} m^{-1} [9,10].

II. CONCLUSION

When the aluminum plate with nanoporous aluminum oxide was one-sidedly heated by a filament-like heater and the temperature of the back side of the plate was kept constant, the thermal field after 30 s of heating had a uniform temperature distribution over the surface.

Increasing the heating power of 2 times from 3.3 to 6.6 W results in 2 time increase in the temperature gradient between the carbon filament and the surface of the nanoporous anodic alumina, from 19.4 °C to 40.6 °C.

The thermal conductivity of the nanoporous anodic alumina layer formed in sulphuric acid was determined to be 1.0 W K^{-1} m^{-1}.

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Comparison and Design of DC Chokes Based on Different Magnetic Materials

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Abstract – **Different magnetic materials for cores of DC chokes are considered and compared in this paper. Four components are designed using both manufacturer software and an improved Fast design approach. The compared materials are: ferrites (3F3), powder materials (sendust MS and Hi-Flux™ HF) and amorphous materials (Microlite 245). Recommendations are derived regarding the use of available design software and discussed optimal design procedure aimed at minimizing losses and volume of the component. The competitive results are summarized and final recommendations are formulated regarding the application of compared materials and main core forms (ETD and toroids) in the realization of DC chokes.**

Keywords – **DC chokes, design, software, soft magnetic materials**

I. INTRODUCTION

The electrical components for the realization of power electronic converters are already available off-the-shelf. Usually they are produced in a range of different sizes and/or building materials in order to guarantee desired system's operation according to particular limitations, e.g. allowed power dissipation of the component. In this context magnetic components for power electronics considerably differ from the other electronic components. While having a variety of magnetic components off-the-shelf, it is often that the designer could not find a magnetic component on the market that best fits to the considered design. Furthermore, magnetic components are usually designed on purpose for a given application, especially for high-power applications.

The design of magnetic components is a broadly discussed topic both by academia and industry [1], [2], [3], [4], [5]. An overview on the share of the latter demonstrates that manufacturers of soft-magnetic materials have identified that there is an interest on behalf of their customers to design power magnetic components themselves. Thus, leading producers provide their customers with technical papers describing not only their materials, but also relevant basic laws, definitions and guidelines on how to design magnetic components [6], [7], [8]. Moreover, manufacturers provide software that could even much more facilitate the user in the process of designing a component [9], [10], [11], [12], [13]. This provokes the interest to learn more about the software and to understand how much we can rely on it.

In the paper we focus on the design of the DC chokes — one of the most prevalent components in Switching Mode Power Converters (SMPC). Firstly, the typical materials used for a DC choke realization are considered. Afterwards, an overview of the available design software is made included some software provided by manufacturers. In order to discuss the software, the next step is the design of several DC chokes by the use of previously introduced Fast design approach methodology [3]. Finally, we compare and discuss the results obtained by the use of the software and this methodology.

II. MAGNETIC MATERIALS FOR DC CHOKES

Every soft magnetic material is suitable for building a DC choke provided that there will be an air-gap in the magnetic circuit. The mostly used magnetic materials for the purpose are Mn-Zn ferrites and powders [5], [6], [7], [14]. In case of ferrites, the air gap appears as a discrete gap between halves of a core set; in case of powders there is an intrinsically low permeability in the structure of the composite material, so that an air gap can be avoided. However, a low permeability asks for a very low loss factor, which is not always the case, so it is not just a "distributed air gap".

The type of the air gap predetermines some design specifics. A discrete air gap is a source of a fringing flux much higher than the distributed air gap emits. Acting as an undesirable electromagnetic emission, fringing flux also leads to increased eddy cur-rent losses in the winding in the vicinity of the gap. Powder materials are better performing in terms of EMI considerations and copper losses, but, they are characterized by higher material losses.

Along with ferrites there are also nanocrystalline and amorphous tape-wound cores from the type of the discrete-gaped cores and amorphous tape-wound cores from the group of the distributed-gap cores [15], [16]. The largest variety of core shapes and sizes are offered by the ferrite

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core series. Ferrite core set shapes include different types such as E, ETD, ER, EQ, EFD, EV, ELP, RM, LP, PM, PQ, U, each having different size ranges. Regarding powder cores, the main core shape is the toroid, however some types of powder E core sets are also available. Nanocrystalline cut cores are also available.

III. DESIGN OF DC CHOKES

A. Manufacturers design software

As mentioned earlier, some manufacturers provide their customers with design soft-ware. Available software includes the references [9], [10], [11], [12], [13]. The soft-ware libraries incorporate the respective manufacturer's cores having defined characteristics. In some cases, [11], [12] the user may choose the core shape, material, number of turns, air-gap length, etc. while searching for relevant performance such as predicted power losses, achieved inductance value and so on. Alternatively, a desired set of output parameters may be defined and the program returns the needed conditions for the input to be fulfilled. In other cases, [9], [10], [13] the user is asked to fill out information regarding electrical, mechanical and temperature properties of the inductor and as a result he receive a single solution if available [13] or a number of solutions [10] that accomplish the requirements. It is also possible that the user de-fines the core to be used in the design process. In most of the software valuable in-formation may be extracted [10], [11], [12] appearing in the form of graphs, such as incremental permeability vs DC bias, core power loss vs AC flux density, inductance vs DC bias, etc.

Questions that arise are how much the user may rely on the software and whether the proposed solutions are optimal or not?

While searching for the design methodology used in the different software we found that [11], [12] provide documents that describe the program and some mathematical relationships. Regarding [9] and [10], relevant information may be extracted from the database on the webpages of the producers [2], [8], [17]. There is no relevant information regarding the software [13].

B. Design methodology

The main restrictions concern the allowed power loss of the component. By the use of the design approach 'Saturated, thermally limited fast design approach' [3] DC chokes of ferrite core sets are designed as follows. Firstly, a proper core size is determined. Then, according to calculated AC peak induction value ΔB_p and the core volume, the core losses are found. More precise calculation of core losses P_{Fe} can be made using NSE (Natural Steinmetz Model) model [18], applicable under square voltage waveforms:

$$P_{\mathrm{Fe,\,NSE}}=\left(\frac{\Delta B}{2}\right)^{\beta-\alpha}\frac{k_N}{T}\int_0^T\left|\frac{dB}{dt}\right|^{\alpha}dt \qquad (1)$$

where $k_N=\dfrac{k}{(2\pi)^{\alpha-1}\int_0^{2\pi}|\cos\theta|^{\alpha}d\vartheta}$, α and β are the coefficients in the Steinmetz equation [21],

$$P_{av,v}=k\,f^{\alpha}\,\hat{B}^{\beta} \qquad (2)$$

Using ΔB_p eq.1, the number of turns is determined. Then the copper losses are calculated, including eddy current losses [19]. A global loss factor k_c is introduced, which represents the ratio between the eddy current losses $P_{eddy,cu}$ and the losses in the ohmic resistance R_0 [3]:

$$P_{\mathrm{eddy,\,cu}}=\left(R_0\,I_{ac}^2\right)k_c\left(m_E, f_{op}, d_p, \eta, \lambda\right) \qquad (3)$$

where m_E is an equivalent layer, f_{op} - operating frequency, d_p - wire diameter,η – relative filling between the conductors, λ – relative filling between layers.

At the last step an air gap length is determined.

The guiding rule of the approach is that the overall losses are to be less than predicted allowable power loss capability of the component.

The expected temperature rise of the component may be calculated using the equation given in [3], [5], [8]:

$$\Delta T_{\mathrm{rise}}\,(^{\circ}\mathrm{C})=\left[\frac{P_{\mathrm{loss},\,(\mathrm{mW})}}{SA,\,(\mathrm{cm}^2)}\right]^{0.833} \qquad (4)$$

where ΔT_{rise} is the temperature rise of the component, P_{loss} is its total power loss and SA is the surface area of the core together with the conductor wound.

IV. COMPARISON OF THE OBTAINED DESIGN RESULTS

In order to analyze different magnetic materials and to inspect the design software, we have designed four DC chokes using the methodology described in [3]. Afterwards we tried out the same cores with the manufacturers' software. The input parameters are: step down DC-DC converter, V_{in}=210 V, V_{out}=105 V, $\Delta I_{L,p}$=1 A, I_{out}=3 A, f_{op}=70 kHz, required inductance value: L=375µH. We considered cores having approximately the same volume.

A. Cores under study

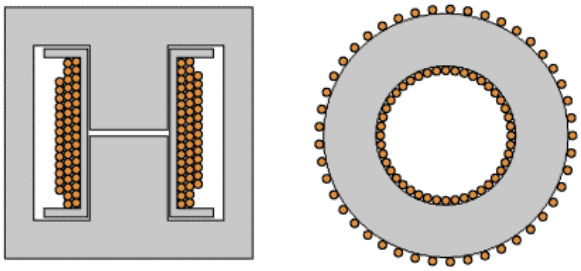
We have used four different core types: an ETD core made of 3F3 ferrite grade [7], MS Sendust and HF Hi-Flux™ powder toroids [14], and distributed air-gap amorphous tape-wound toroidal core Microlite 245 [20]. Some of the properties of the considered materials are given in Table 1. The corresponding software is from references [12], [10], [13], respectively.

TABLE 1. PROPERTIES OF SOFT MAGNETIC MATERIALS COMPARED FOR REALIZATION OF DC CHOKES

	Ferrite 3F3	Sendust MS	Hi-Flux™ HF	Metglas® MICROLITE
Composition	Mn-Zn ceramic	Fe-Si-Al powder	Ni-Fe powder	(B-Fe-Si) ribbon
B_{sat}, [T]	0.35@100°C	0.89	1.48	1.56@25°C

B. Design results

Fig. 1 shows the used types of cores for the designed DC chokes by [3]. The designs using toroids are aimed at a single layer winding along the inner circumference of the core. Eddy current losses in windings of the toroidal inductors are calculated using the approach, described in [3] and [19]. The obtained design specifications are given in Table 2. The "calc" rows present results of designs by the use of [3] whereas the "*soft*" rows present those of the respective software.



a) b)

Fig. 1. DC choke arrangements, a) ETD core design, 3F3; b) toroidal core design.

Concerning the performance of the different cores, the design results lead to following conclusions:

- *ETD design:* The lowest core losses are obtained with the ferrite core. Nevertheless, this is at the cost of high fringing flux and respective eddy current losses in the winding. Its effect is reduced by the use of Litz wire;
- *Design with toroids:* The designs are core-loss dominated. An exception of this is the sendust core MS-133060-2, where to obtain single layer winding a thinner conductor is used leading to higher DC resistivity.

Comparing the results of the fast design approach [3] and the manufacturer software, the design results lead to following conclusions:

1. *ETD design:* The input parameters of the software are 40°C rise in the component self-temperature and 18% copper fill-factor – almost the same values of the parameters obtained by the use of [3]. We chose the same core and let the software determine the turns number. It returns 36 where we calculated 47. Eddy-current losses in the windings seem to be not accounted for in the software.

The obtained value of peak induction using the software is much higher than the saturation point of the core. It seems that the cross-sectional area of the core used by the software is the maximal one. The core losses must be calculated separately in another window. In this case the design is expected not to operate at all due to saturation. It is possible that the fringing is not well taken into account, so that the air gap is not sufficient and the core saturates earlier, so in fact more gap is needed and more turns.

It seems that for calculating the temperature rise of the component mentioned in the software only the winding loss is taken into account.

2. *Powder cores design:* The sets of properties obtained by the two methods, [3] and [10], are very similar. A difference appears in the chosen wire diameter which leads to difference in the copper losses. We aimed at a single layer winding. In the design with the software for core MS-133060-2 "single layer" property is chosen whereas in case of HF-133060-2 "full window" is used instead, otherwise the software de-cides that the core cannot be used in single layer realization. Regarding the obtained value of the copper losses, the software only accounts for the DC resistance at the specified temperature and does not account for skin and proximity effects in the winding. The calculation of temperature rise of the component takes into account both the core and copper losses.

3. *Amorphous tape-wound core design:* In this case the obtained results are also very close to each other. However, a noticeable difference appears. While having obtained the same values of DC and AC flux densities (BDC and BAC), methodology from [3] leads to core losses approximately 8 times more than that obtained by the software [13]. A calculation shows that the losses obtained by the software would be as they are, if Bac is two times less compared to its current value.

V. CONCLUSION

Recommendations for ferrite cores for DC choke design:

Copper losses dominate the design; this concentrated loss reduces the possible heat transfer. The AC peak flux density choice can set the core losses, as the induct-ance can be adjusted using different air gap length.

Recommendations for using powder type toroids for DC cokes design:

Core losses dominate the design. Most of the heat is evacuated trough the copper surface. If a discrete air gap is not used one cannot choose particular peak AC flux density, i.e. particular core losses, as the inductance value is predetermined of the inductance factor. Instead, one should try with the same size but with different initial permeability core or with the same permeability but with different core size.

The *ferrite* ETD core seems a better choice than the other cores, the reason is that the air gap can be adapted and that 34mm square surface is larger than a 34 mm circle diameter, and hence cools better.

The use of manufacturer software may facilitate the work of a designer. In order to take full advantage of the software, one should verify the methodology. The general problem of the design software is that ussualy it does not show how precise are coverd the details of the design. There are main concerns to be included: what type of heat transfer is considered, one thermal resistance for the whole component or separate magnetic and copper; are eddy currents considered in the presence of an air gap, etc.? If several programs are compared, the user will be aware of the presision of designs.

But without knowing what is dominant in the software, the designer could not obtain good results.

Then an analytical approach, like the discussed Fast Desigh Approach [3], is a better choice even taking longer time to apply.

TABLE 2. DESIGN RESULTS FOR DC CHOKES, STEP DOWN DC-DC CONVERTER, V_{IN}=210 V, V_{OUT}=105 V, $\Delta I_{L,P}$=1 A, I_{OUT}=3 A, f_{OP}=70 KHZ, L=375 μH, MAGNETIC MATERIALS: FERRITE 3F3, ETD CORE; SENDUST CORE MS, POWDER CORES HF (TOROIDS), AMORPHOUS MICROLITE 245 CORE MP7254MDGC (TOROID).

Core type		ETD 34	MS-133060-2	HF-133060-2	MP7254MDGC
Dimensions, [mm]		34x34x11	34x19x15		39x25x16
Volume, [mm^3]		7640	7120		7460
P_{core}, [kW/m^3]		20	167.844	358.538	470.872
Allowed total losses, [W]		2.941	2.27	2.27	2.986
$B_{ac,peak}$, [T]	calc	0.064	0.059	0.06	0.108
	soft	*0.094*	*0.0588*	*0.0613*	*0.0945*
B_{dc}, [T]	calc	0.193	0.178	0.187	0.334
	soft	*0.315*	*0.178*	*0.184*	*0.39*
Core losses, [W]	calc	0.153	1.195	2.553	**3.513**
	soft	*out of range*	*1.2*	*2.63*	***0.496***
Number of turns	calc	47	73	71	46
	soft	*37*	*73*	*70*	*49*
Wire diameter, [mm]	calc	Litz 60 x 0.1	0.63	0.71	1.4
	soft	*0.71*	*0.723*	*1.45*	*0.912*
Copper losses, [W]	calc	**1.383**	2.434	1.885	0.367
	soft	***1***	*1.51*	*0.509*	*0.84*
Temperature rise, [°C]	calc	22.783	44.927	52.586	35.618
	soft	*18*	*34.8*	*34.3*	*16*

ACKNOWLEDGMENT

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Fuzzy Logic Based Harmonic Elimination in Single Phase Inverters

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Abstract – **A fuzzy system for the elimination of specific low order harmonics in the output voltage of single phase inverters is proposed. The proposed system does not need look up tables which require much memory as in traditional methods and no need for training which takes much time as in neural networks. Here, modulation index is used as input to fuzzy system and switching signals are generated. Predetermined low order harmonics are successfully eliminated.**

Keywords – **Fuzzy Logic, Harmonic analysis, Harmonic elimination, Inverter, Pulse width modulation.**

I. INTRODUCTION

Many electrical equipment and machine controllers such as ups, smps, drives, traction systems, need pulse width modulated voltage source inverter which is used to convert dc source to ac source with required amplitude and frequency.

Different techniques [1-2] can be used for the generation of gate signals for switching the switching elements in the inverter. The pulse width modulation (pwm) method is the most used modulation technique controlling the magnitude and frequency of the inverter output voltage.

The selected harmonic elimination technique is one of the effective pwm methods for the elimination of selected low order harmonics from the spectrum of the inverter output voltage [3-5].

In selected harmonic elimination technique, the inverter output voltage is represented by a Fourier series and the coefficients of selected harmonics which are going to be eliminated are set to zero. Hence, a set of nonlinear equation obtained need to be solved in terms of unknown switching angles for each value of modulation index. The number of equation depends on the number of harmonics to be eliminated.

Generally this nonlinear equation is solved off line for each value of modulation index and stored in look up tables in microcontroller or microcomputer memory.

The microcomputer takes modulation index as input and generates corresponding switching angle. The number of look up tables is large and need large memory. Therefore intelligent methods are proposed for the selective harmonic elimination. Proposed neural networks for the selective harmonic elimination need offline training but it takes too much time.

Fuzzy logic is used in this study for the generation of the gate signals for switching elements in the single phase inverter.

II. SELECTIVE HARMONIC ELIMINATION

A single phase full bridge inverter structure is given in Fig. 1. In conventional pwm inverters the switching signals for the first leg are obtained by comparing a sinusoidal modulation signal with a triangular carrier wave.

The switching signals for the second leg are obtained by shifting the signals of the first leg by 180°. Thus the signals of the switching elements for S1, S4 and S2, S3 are synchronized.

In general increasing switching frequency decreases the total harmonic distortion in the output voltage but the low order harmonics still have important effect on total harmonic distortion.

An approach based on determination of switching angles or switching times to adjust magnitude of fundamental component and to suppress some low order harmonic components at the output voltage of an inverter is known as the selective harmonic elimination [6-9]. In this method, the magnitude of the fundamental component and the harmonics to be eliminated are determined and the corresponding switching angles are calculated.

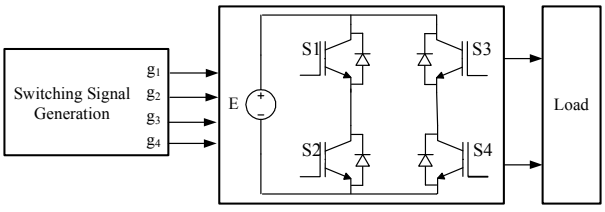

Fig. 1. Single-phase symmetric PWM inverter

The inverter output voltage V_0 obtained by unipolar switching is shown in Fig. 2. Output voltage pulses are generated with the switching angles (α_1, α_2, α_3,..., α_N). The inverter output voltage can be represented by Fourier series as

$$V_0 = a_0 + \sum_{n=1}^{\infty} A_n \cos(n\omega t) + \sum_{n=1}^{\infty} B_n \sin(n\omega t) \qquad (1)$$

where

$$a_0 = \frac{1}{2\pi}\int_0^{2\pi} V_0(t)dt \qquad (2)$$

$$A_n = \frac{4E}{\pi n}\left[-\sum_{i=1}^{N}(-1)^n \sin n\alpha_i\right] \qquad (3)$$

Even harmonics do not exist because of the odd and quarter wave symmetry of the output voltage waveform and Fourier coefficients A_n and a_0 are equal to zero due to symmetry [10].

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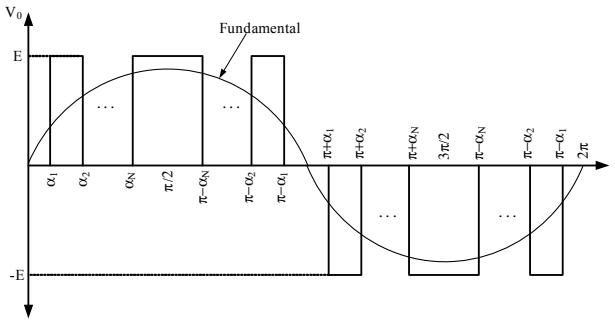

Fig. 2. Inverter output voltage

Only the odd harmonics with sine components exist in the output voltage, thus Eq. (1) can be written as:

$$V_0 = \sum_{n=1}^{\infty} B_n \sin(n\omega t) \quad n = 1, 3, 5, \ldots, \infty) \tag{4}$$

where B_n is given by

$$B_n = \frac{4E}{\pi n} \sum_{i=1}^{N} [-(-1)^n \cos(n\alpha_i)] \tag{5}$$

and

$$0 < \alpha_1 < \alpha_2 < \cdots < \alpha_N < \frac{\pi}{2} \tag{6}$$

E is the dc bus voltage, $\omega=2\pi f_1$, f_1 is the frequency of the fundamental component and N is the number of switching angles per quarter cycle.

Selective harmonic elimination method is used to determine the switching instants $\alpha_1, \alpha_2, \ldots, \alpha_N$ in the inverter output voltage waveform to;

i-) make the values of harmonic components $B_3, B_5, \ldots, B_{N-1}$ to be equal to zero.

ii-) keep the fundamental component value B_1 equal to the desired output voltage.

The equation set can be obtained from Eq. (5) by equating the coefficients of the harmonics to zero.

$$\begin{bmatrix} B_1 \\ B_3 \\ B_5 \\ \vdots \\ B_n \end{bmatrix} = \begin{bmatrix} \cos(\alpha_1) & -\cos(\alpha_2) & \cdots & \pm\cos(\alpha_n) \\ \cos(3\alpha_1) & -\cos(3\alpha_2) & \cdots & \pm\cos(3\alpha_n) \\ \cos(5\alpha_1) & -\cos(5\alpha_2) & \cdots & \pm\cos(5\alpha_n) \\ \vdots & \vdots & & \vdots \\ \cos(n\alpha_1) & -\cos(3\alpha_2) & \cdots & \pm\cos(n\alpha_n) \end{bmatrix} = \begin{bmatrix} 4E/\pi \\ 0 \\ 0 \\ \vdots \\ 0 \end{bmatrix} \tag{7}$$

where n=1, 3, 5… N and N is the number of pulse in every quarter cycle which is the number of switching angles in a quarter cycle. N-1 low order harmonics can be eliminated by choosing appropriate pulse positions.

If the amplitude of the fundamental component B_1 need to be adjusted then

$$B_1 = m\frac{4E}{\pi} \tag{8}$$

where m is the modulation index.

To obtain the switching angles, the set of equations given as matrix form need to be solved.

These equations are nonlinear and can be solved using numerical methods [11-12]. In this study Newton-Raphson method is used to solve the nonlinear equation set. Solution obtained from Newton-Raphson is used to construct the input and output membership functions in the fuzzy controller.

III. Fuzzy Logic Controller

Fuzzy logic systems have been applied in many fields such as intelligent systems, computer vision and control systems.

Fuzzy systems are useful in situations involving complex systems whose behaviors are not well understood, and where an approximate, but fast, solution is warranted [13].

Fuzzification is the first step in fuzzy logic system. In this step, crisp values are converted to fuzzy values using expert's knowledge and experience.

The second step is the development of rule data base which defines the principles of the controller in terms of the relationship between input and output.

The last step is the conversion of the fuzzy outputs to control action.

According to the determination of outputs there are two types of fuzzy inference systems, Mamdani-type and Sugeno-type. Sugeno-type inference gives an output that is either constant or linear mathematical expression.

In this study, because the input and outputs of the fuzzy block are numeric values therefore Sugeno-type fuzzy system is used for the implementation of the input and output data. Fig. 3 shows the input membership function.

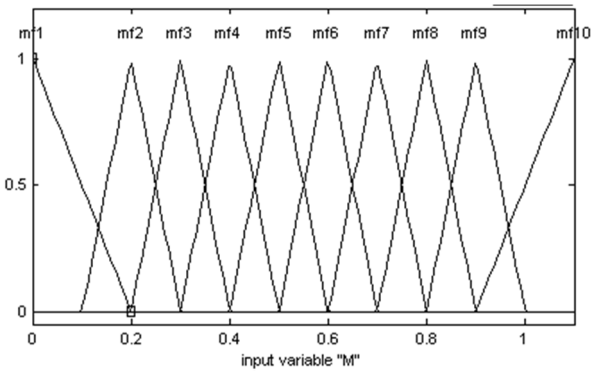

Fig. 3. Input membership function

The outputs of the fuzzy control system which are the switching angles are computed for a given input which is the modulation index as shown in Fig. 4.

Ten membership functions are used for the representation of input data. There are eleven outputs each has 50 constant type membership functions for the representation of output data.

Totally 104 rules are used between the input membership functions and output membership functions.

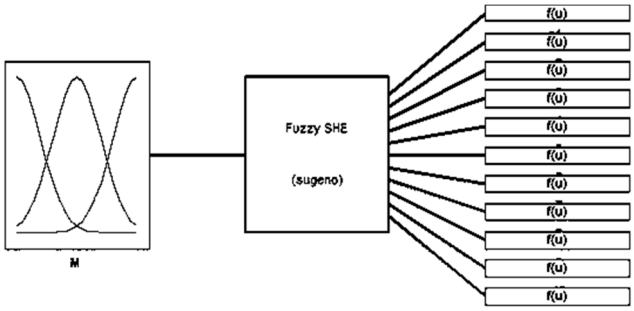

Fig. 4. Fuzzy system

IV. SWITCHING SIGNAL GENERATION

The nonlinear equations are solved by varying modulation index. The corresponding switching angles are obtained for every modulation index. The modulation index and switching angles are used in fuzzy logic controller.

The modulation index is used as the input to fuzzy logic controller and the output of this controller is the corresponding switching angles.

The switching angles obtained from fuzzy logic controller for a given modulation index are used as inputs for generation of switching signals.

Switching angles are compared with a triangular carrier wave and the produced signals are applied to the switching elements of single phase inverter Fig.5. A sample switching signals for N=3 is given in Fig. 6.

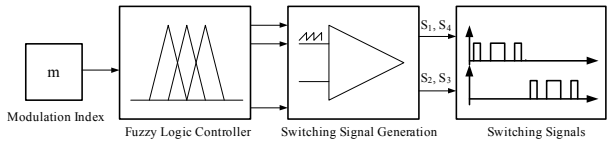

Fig. 5. Switching signals generation

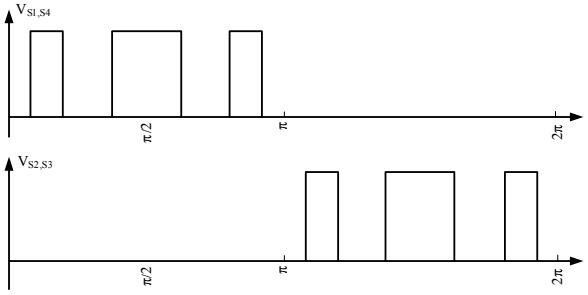

Fig. 6. Sample switching signals for N=3

V. SIMULATION RESULTS

Matlab/Simulink environment is used for the simulation studies. Fig. 7 shows the simulation block diagram. Ten low order harmonics (3, 5, 7, 9, 11, 13, 15, 17, 19, 21) are chosen to be eliminated from the spectrum of the inverter output voltage. Thus the number of switching angles is 11 (N=11). The switching angles and the corresponding switching times for N=11 and m=0.9 are given in Table I.

In order to see the switching angles, one period of the inverter output voltage is given in Fig. 8 in terms of angles in degrees. Fig. 9 shows the inverter output voltage and filtered current waveform when N=11 and m=0.9.

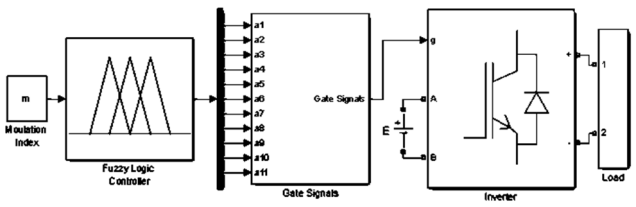

Fig. 7. Simulink block of fuzzy logic based selective harmonic elimination

TABLE 1. SWITCHING ANGLES (DEG) AND SWITCHING INSTANTS (MS) FOR N=11 AND M=0.9

α_1	α_2	α_3	α_4	α_5	α_6	α_7	α_8	α_9	α_{10}	α_{11}
12.62	15.71	25.38	31.44	38.41	47.25	51.91	63.25	66.15	79.78	81.66
t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}	t_{11}
0.70	0.87	1.41	1.74	2.13	2.62	2.88	3.51	3.67	4.43	4.53

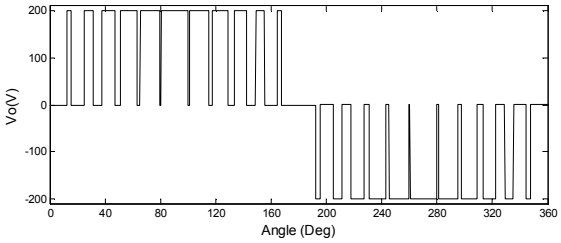

Fig. 8. One period of inverter output voltage

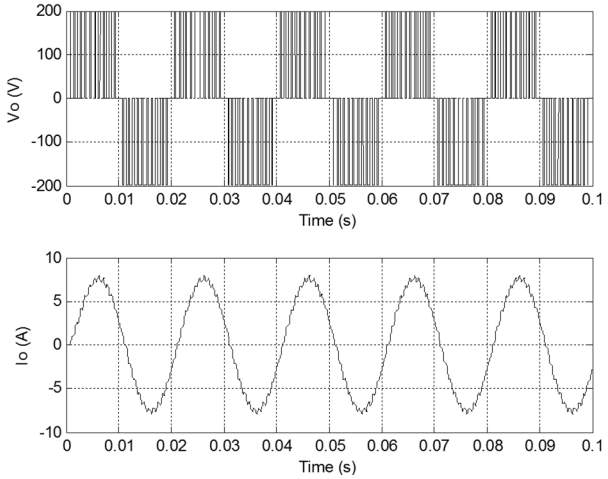

Fig. 9. Inverter output voltage and current

The output voltage spectrum of single phase inverter is given in Fig. 10. The harmonics of order 3, 5, 7, 9, 11, 13, 15, 17, 19, 21 do not exist in the inverter output voltage spectrum.

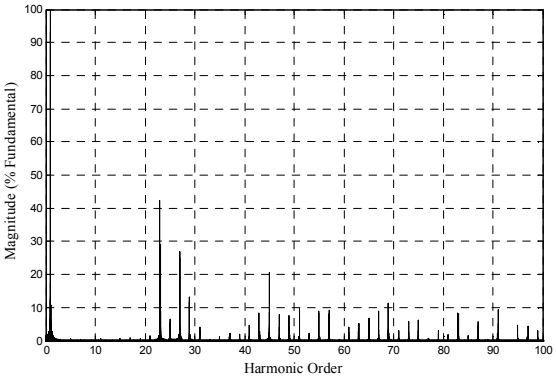

Fig. 10. Inverter output voltage and its spectrum

The modulation index m, is changed from 0.8 to 1 at time t=0.1s and the resulting output voltage waveform is given in Fig. 11.

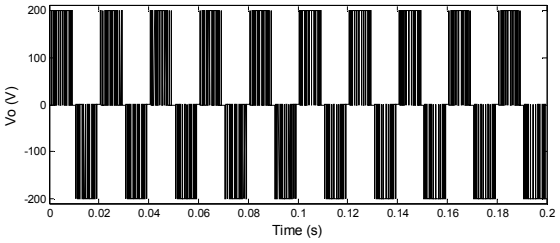

Fig. 11. Zoomed output voltage waveform when m changes from 0.8 to 1 at t=0.1

The output voltage spectrums are given in Fig. 12 and Fig. 13 for both t<0.1 (m=0.8) and t>0.1s (m=1).

The output voltage waveform is zoomed in Fig. 14 to see the transition from m=0.8 to m=1.

It is also seen that 10 predetermined low order harmonics do not exist in the inverter output voltage spectrums as expected.

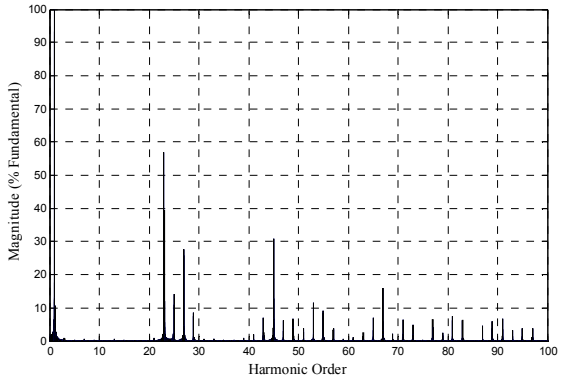

Fig. 12. Inverter output voltage and its spectrum for m=0.8 (t<0.1)

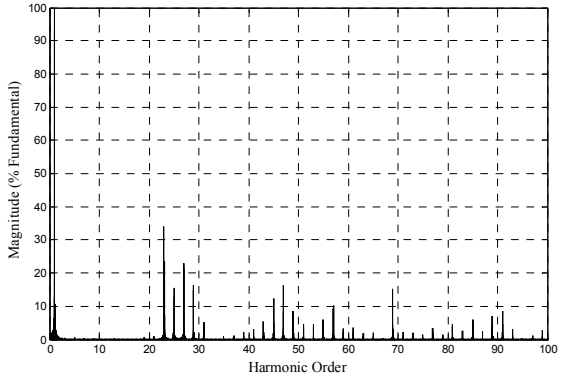

Fig. 13. Inverter output voltage and its spectrum for m=1 (t>0.1)

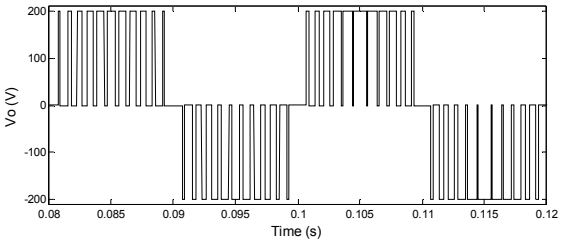

Fig. 14. Zoomed inverter output voltage

VI. CONCLUSION

A fuzzy logic system for the computation of switching instants and implementing switching signals for selective harmonic elimination (SHE) in single phase inverters is presented in this study. Sugeno-type fuzzy system is used to obtain the desired switching instants for any given modulation index as input.

The selective harmonic elimination in single phase PWM inverter using fuzzy logic is implemented in Matlab/Simuink programming environment. Simulations were carried out for different modulation index values and some are presented here. The simulations verified the elimination of the predetermined low order harmonics from the output voltage spectrum.

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IoT-Based Wireless Induction Motor Monitoring

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Abstract – **In this study, a factory induction motor (IM) was monitored with wireless TCP/IP protocol in order to detect and predict deviations from normal operating parameters before the occurrence of motor failure. In this way, the production process is not impeded and the required maintenance or replacement can be performed with the least possible disruption. In this study, the motor cycle, the current drawn by the motor and the motor voltage were read by the Hall-effect current sensor and the required power consumption was calculated. With this aim, the designed architecture read the accepted parameters of the motor and reported them to the central management software. The central management software operating in real time was then able to assemble these parameters and form predictive maintenance models.**

Keywords – **wireless Wi-Fi sensor monitoring, induction motor, motor parameters**

I. INTRODUCTION

In today's manufacturing industries, mechanical and electromechanical systems are driven by electric motors on the premises. The drivers of these motors are mostly on motor control and the predictive maintenance schedules of the motors are not calculated. Attempts are being made to maximize efficiency by using enterprise resource planning (ERP), especially in 7/24 production enterprises. However, unexpected failures not predicted by the ERP system can cause disruptions in the production process. In this study, the temperature, current, voltage, cycle, speed, frequency, torque and flux data of single and three phase induction motors (S / 3P-IMs) were read using TCP/IP protocol via Wi-Fi. By using the existing Internet network, these parameters were read and transferred to the central software without the need for additional wiring. The central software collected the parameters of all the motors and determined the necessary maintenance schedules. This system has been applied and used in a textile factory. Frequency-controlled motors have special 50/60 Hz filters in their structure which make it impossible to measure energy using the unified integrations developed for normal energy measurement. For this reason, the energy measurements were calculated by the processor.

A number of relevant studies carried out on the subject are briefly summarized here:

[1] Motor failure was detected by using different models to analyze the stator current. These included FFT, Hilbert-transform, continuous wavelet transform (CWT), discrete wavelet transform (DWT), the Wigner-Ville distribution (WVD) and instantaneous frequency (IF).
[2] A hybrid model was developed combining fuzzy min-max (FMM), neural networks and classification and regression tree (CART) models. The motor stator current was also applied with the model.
[3] Motor currents, acoustic vibrations and mechanical vibrations were analyzed wirelessly using the Hilbert-Huang transform.
[4] A different wavelet transform was used to remove errors caused by load variability in measurements made with motor current signature analysis (MCSA).
[5] Pattern recognition studies were carried out on motor currents and voltages and as a result, motor faults were classified using the hidden Markov model.
[6] An industrial wireless sensor network that transmits motor currents and vibrations wirelessly was applied and its behavior at different loads examined.
[7] In order to detect motor faults, an evaluation was carried out under unloaded and fully loaded conditions, and real-time motor currents and voltages were examined.
[8] Electrical devices were monitored via the wireless ZigBee network. Motor parameters included current, voltage and torque.
[9] Motor health was explored both mechanically and electrically. The study demonstrated that readings obtained by monitoring motor parameters could reveal information about the motor.

In the present study, the hardware was designed with the NXP LPC1769 cortex-m3 100 MHz ARM architecture. This processor included a hardware encoder reader and a 6-channel 12-bit ADC. The Wi-Fi communicated with the central software via UDP protocol with 802.11.bg. The central software was developed with C ++ to read motor parameters, apply mathematical models of prediction and present statistics. Details of the designed IoT induction motor monitoring hardware (IoT-IMM-H) and central monitoring system (CMS) software are described below.

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II. MATERIALS AND METHODS

2.1. Proposed IoT-IMM-H structure

The overall structure of the system hardware is shown in Figure 1. Figure 2 shows the connections of the IoT-IMM-H. Figure 3 shows the physical form of the IoT-IMM-H equipment that was developed. The system has two components, hardware and software, which are described in the following sections.

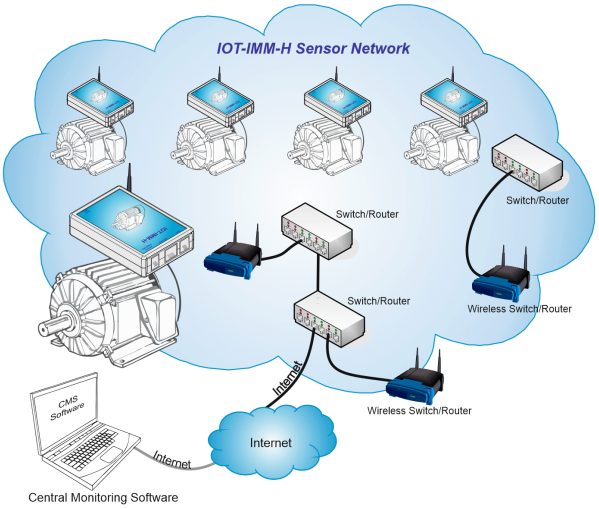

Fig. 1. IoT-based monitoring structure

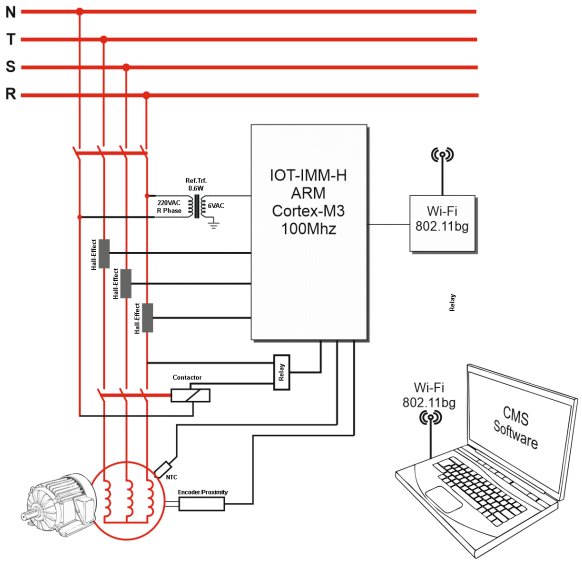

Fig. 2. Connections diagram of IoT-IMM-H

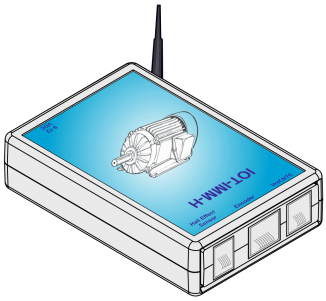

Fig. 3. IoT-IMM-H module

2.2. The Hardware

In this study, experiments were carried out on the three phase IM at ~ 0.3 kW/1400 rpm and 2.5 kW/1200 rpm. The designed hardware used an ARM NXP LPC1769 Cortex-M3 processor, a 802.11.bg Wi-Fi module, an ACS711 (-25 – +25A) Hall-effect current sensor, a high-speed Hall-effect proximity sensor for cycle measurement, NTC and a 220 VAC/6 VAC/0.6 W reference transformer. The entire system was fed externally with a 9-12 VDC power supply. The LPC1769 contained a 6-channel 12-bit ADC in its make-up. The ACS711 modules used for each phase were 2.5 V centered and produced output voltage of between 0-5 V, according to the current drawn. The ACS711 connection is shown in Figure 4. The ACS711 has a bandwidth of 100 kHz with negligible phase shift. The outputs of the ACS711 modules were connected to the analog input of the IoT-IMM-H. Moreover, the IOT-IMM-H was linked via encoder and NTC connections. The ACS711 Hall-effect current sensor, with -/+ 1% nonlinearity, met the desired accuracy. Figure 4 shows a schematic diagram of the ACS711 connection and the module.

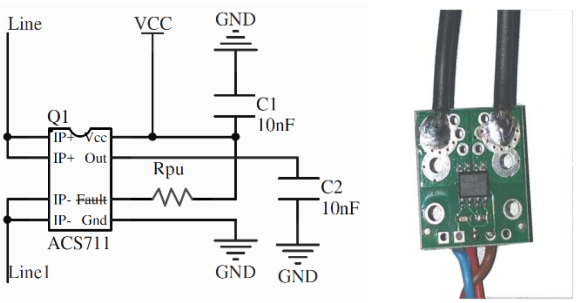

Fig. 4. ACS711 current connection diagram and module

Figure 5 shows the PCB design of the IoT-IMM-H, while the implemented design is shown in Figure 6. Table 1 gives the IoT-IMM-H connection details.

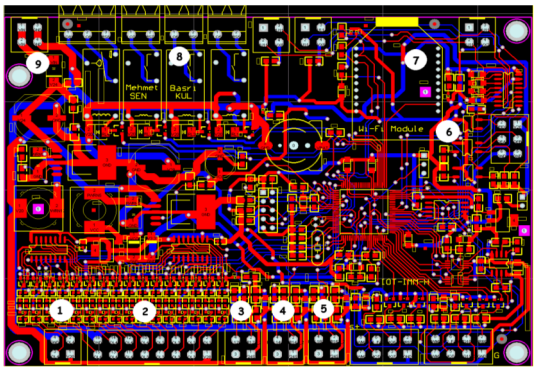

Fig. 5. IoT-IMM-H PCB artwork

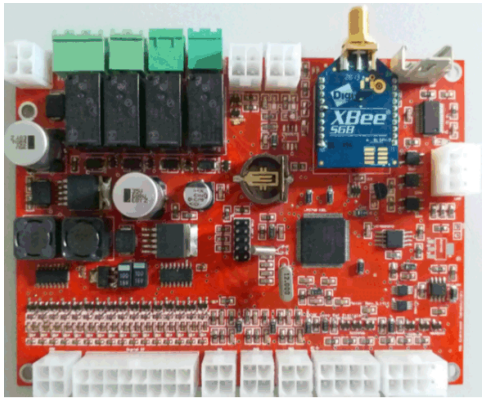

Fig. 6. Implemented IoT-IMM-H without enclosure

TABLE 1. IoT-IMM-H connection details

1	Vref, NTC input	6	Encoder input, Phase A,B,Z
2	Proximity Inputs, 0-30VDC	7	Zigbee 802.11bg Wi-Fi module
3	Phase R, ACS711 Hall-effect sensor input	8	Relay outputs
4	Phase S, ACS711 Hall-effect sensor input	9	16-27VDC power input
5	Phase T, ACS711 Hall-effect sensor input		

The ACS711 modules were prefabricated and due to the long cable connection, a low pass filter was added on the IoT-IMM-H for each phase, as shown in Figure 7.

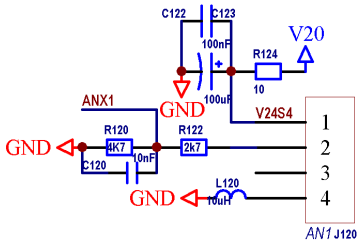

Fig. 7. Low pass filter on IoT-IMM-H for ACS711 modules

Figure 8 shows the encoder input on the IoT-IMM-H. The encoder inputs were isolated with an optocoupler. Because of the long cable length, EMI effects occurred at quadrature encoder outputs and both isolation and a low pass filter were required. Figure 9 shows the schematic part of the Wi-Fi module on the IoT-IMM-H. As the diagram of the whole circuit is quite extensive, only the necessary parts are shown.

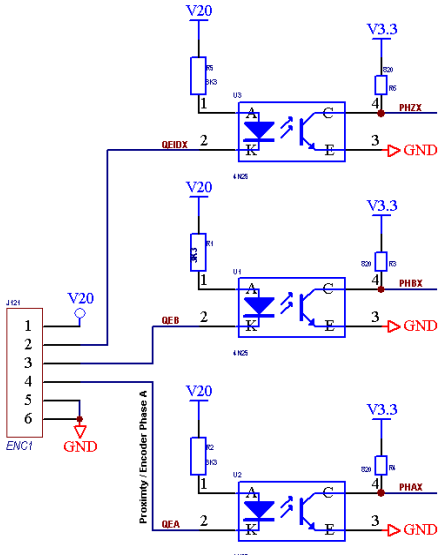

Fig. 8. IoT-IMM-H encoder/Proximity input

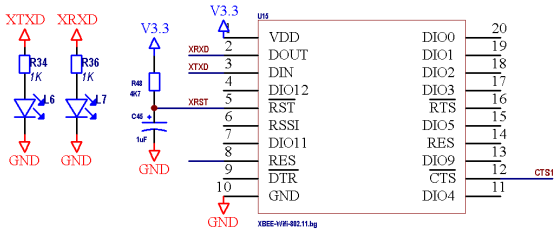

Fig. 9. IoT-IMM-H Wi-Fi-802.11.bg section

2.3. Embedded Software

The embedded software was developed with GNU-ARM C. In recent years, encoders, ADC and RTC have been read using the CMSIS-CM3 library developed as OpenSource for Cortex-M3 processors and supported by the processor manufacturers. In addition, the energy measurements of each phase were made using the "FFT-Based Algorithm for Metering Applications" library developed by Freescale Semiconductor Inc. The reference voltage input on the IoT-IMM-H was taken on a transformer, using a single reference for the R, S, and T phases. The difference of 120 ° between the R, S, and T phases was equalized by the software. A single voltage reference was used to reduce cost. However, the currents belonging to each phase were taken separately. The sensitivity required for predictive maintenance was not needed since the difference between the phases was minimal.

In AC energy measurement, true power (P), measured power (W), apparent power (S), measured voltage (VA) and reactive power (Q) are calculated. Complex and real components are shown trigonometrically in Equations 1

and 2, and a depiction of energy calculation is given in Figure 10a. The "FFT-Based Algorithm for Metering Applications" is explained in detail in the AN4255 application note and will not be described further in this study. The embedded software performed Vrms and Irms energy calculations separately for each phase. The embedded software performed 3750 samplings for this process, at an average of 25 samplings per alternation (Fig. 10b). The root mean square (RMS) was used to determine the effective value of the AC signals. As a result, with its high processing power, the LPC1769 was easily able to perform the energy calculations for the three phases.

(1) (2)

$$I_{RMS} = \sqrt{\sum_{k=0}^{\frac{N}{2}-1} (I_{RE}^2(k) + I_{IM}^2(k))}$$

$$U_{RMS} = \sqrt{\sum_{k=1}^{\frac{N}{2}-1} (U_{RE}^2(k) + U_{IM}^2(k))}$$

where *IRE(k), URE(k)* are real parts and *IIM(k),UIM(k)* imaginary parts of *k.*

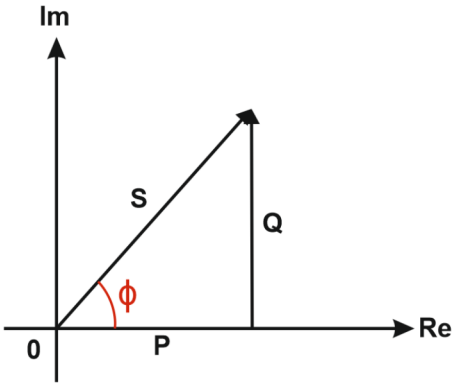

Fig. 10a. Energy calculation triangle: apparent power (S), true power (P), reactive power (Q) and CosFi

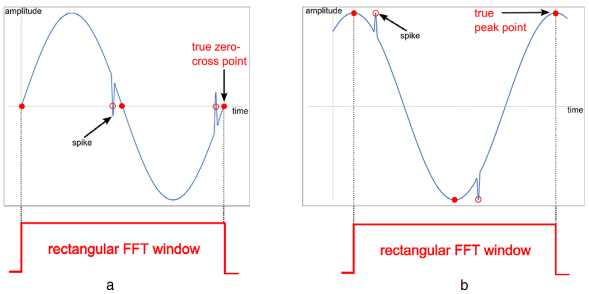

Figure-10b ADC sampling window

2.4. CMS Software

The CMS software reads by scanning the IoT-IMM-H modules and the other sensory data calculated by the IoT-IMM-H with UDP protocol. The UDP protocol is ideal for such sensor readings because handshaking is not necessary. If there are new packet losses, or if some of the IoT-IMMH modules are closed, the TCP/IP stack software does not waste extra processing power. The CMS software reads the data about the motor for about three seconds and then sends a UDP broadcast packet to all IoT-IMM-H modules. They receive this packet and send a data packet in response. Because the CMS software is written as "event driving", there is no packet loss, even if all IoT-IMM-H modules have the same data. The data packets from the IoT-IMM-H modules are immediately added to the pool of data packets. According to the data in the pool, a CMS thread updates the database with other predictive maintenance and energy data. A screenshot of the process can be seen in Figure 11.

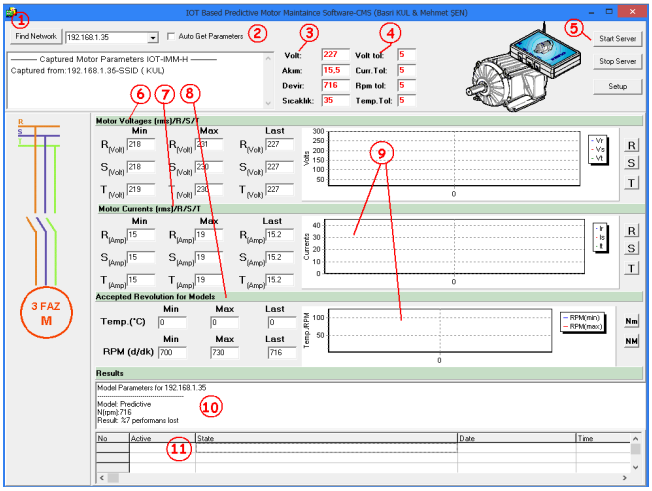

Fig. 11. CMS screenshot

TABLE 2. Description of CMS software

1	Find on Network Connectivity check	**7**	Min,Max, Last measured current for prediction at settled rev.
2	Update each captured data	**8**	Revolution setting for model
3	Last captured data	**9**	V,I,Rpm graphics
4	Fault tolerances	**10**	Model results
5	UDP server thread functions	**11**	Updated values and status
6	Min,Max, Last measured voltage for prediction at established rev.		

Motor current signature analysis (MCSA) was used in the study. Unlike other studies, a preloading method was chosen. In mass-production enterprises, the operation of the machines is repetitive. As a solution to the variable load problem, the method allowed the introduction of motor parameters during the processing of the relevant product. Data outside the user-specified tolerance limit was eliminated if it was not repeated. Power values according to motor parameters were updated via FIFO with 1024 samples. Then, after calculating the standard deviation over the 1024 samples in the table, data apart from the average deviation values were eliminated. The average of the remaining data was taken and compared with the learned values (%). The incoming data was repeated at 3-second intervals for all machines in all IoT-IMM-H units. As a result, the magnitude of deviation was regarded as the wear value of the motor.

In addition, software algorithm will be published in another study.

III. EXPERIMENTAL STUDY

The system is being tested in a factory in Bursa, the textile center of Turkey. There are 18 looms in the factory working in the range of 2.7 kW - 4.5 kW. The maintenance schedule of the motors has been determined and the energy consumed per product calculated. The data indicate that better linear results are obtained when the stator winding temperature of the motor is included in the model.

IV. CONCLUSION

The system developed in this study has yielded successful results for production environments where there is little variation in the load on the motors. This learning method can be used for motor power ratings, especially for 7/24 machines. This study has provided statistics not only for creating mathematical models but also for enabling the CMS operator to establish a motor maintenance schedule.

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Selection Guidelines for BMSs Used in Ultralight Electric Vehicles

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Abstract – **This paper highlights the importance of a BMS when operating with lithium-ion cells, especially within narrow SOA. A classification of BMSs is proposed based on four criteria. Based on the classification guidelines for optimal selection of a BMS for given application are also proposed. Using the guidelines an example BMS is selected and studied experimentally. The studied system operates within the SOA, reveals high accuracy during the balancing process, obtains achieves short response time and it is easy to setup and use. The algorithm applied for experimental validation is presented and discussed.**

Keywords– **BMS, battery pack monitoring, Li-ion battery charging and balancing, $LiFePO_4$ batteries.**

I. Introduction

The battery as a portable energy source has a fundamental role in the modern electronics. Medical equipment, notebooks, cellphones and many others are mainly powered by lithium batteries. However, nowadays the EV industry needs more batteries than the other industries combined [1], [2], [3], [4]. Furthermore, the battery packs get bigger and bigger which tightens their Safe Operation Area (SOA). This leads to constant advances in the battery technology and charging monitoring and protection of the battery packs.

This progress is especially true for lithium batteries. Those batteries have superior efficiency, energy and power density and cycle life compared to other series production batteries but they need additional electronics. For example, a traditional car battery would have six lead-acid cells and in the ideal case they would be charged to 2.25 V resulting to a total voltage of 13.5 V.

In a real battery not all the cells would be equal and can vary from 2.20 V to 2.50 V [5] without any additional electronics to regulate this voltage. However, this is not the case when a traditional lithium battery is charged. If such a battery with only two cells (4.2 V nominal voltage) without any additional electronics to regulate the cell voltage is being charged from 8.4 V supply one of the cells can be charged to 3.1 V and the other one to 5.3 V. In practice the charging process can result in any two voltages the sum of which gives 8.4 V (an extreme case would be 2.8 V and 5.6 V). As a result, the lithium batteries cannot be used without additional electronic circuits to monitor and protect the battery pack.

A Battery Management System (BMS) is the electronic circuit which ensures that the battery pack operates in its SOA. It can monitor, protect, estimate the states, maximize the performance and communicate with user or other device.

This paper focuses at the experimental study of BMS for six $LiFePO_4$ cells with 40 Ah capacity.

II. Comparative Study of BMS

A BMS can be categorized based on several factors. Those are technology (analogue or digital), topology (centralized, modular, master-slave or distributed), functionality (regulators, meters, monitors, balancers or protectors) and features [6], [7]. This paper suggests guidelines of choosing a proper BMS for wide range of applications via Figure 1 and presents a particular example.

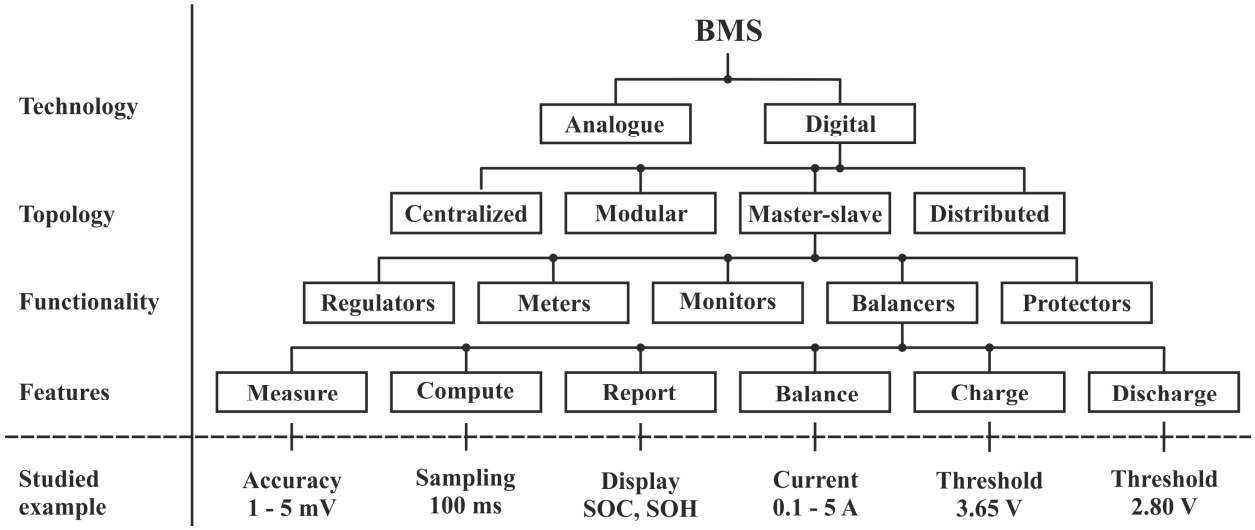

Fig. 1. BMS classification

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Comparing both technologies, BMS can be built upon (analogue and digital) a set of advantages and disadvantages can be noted. An analogue system has the benefits of simplicity and reliability respectively since it does not need a microprocessor for calculations. However, the absence of a microcontroller limits the information that can be received from the BMS. Such system uses a threshold detection for the high and low voltages of each cell (the voltage that the cell should not exceed and the voltage that the cell should not be discharged below). Typically, there is no information about which cell has reach a limit but if necessary a LED indication is possible. A digital system provides detailed information for the condition of the cells. As a summary an analogue BMS is much cheaper and suitable for small established productions. A digital BMS is more expensive, suitable for large battery packs and systems in development [8], [9], [10], [11] and voltage balancing over series connected supercapacitor cells [12].

Comparing the most common topologies, a BMS can be built as a centralized system which is cheapest to build on its own and has good reliability but has several disadvantages. It needs long wires to connect to all the cells. The modular topology solves this problem with a separate module for a group of cells. Big disadvantage of the modular approach is that all modules are equivalent but only one is fully utilized, the rest are used only for measurements (normally only the first module operates with the rest of the charging system). This problem is solved with the master-slave combination where the modular part consists of equivalent (simple) slave devices and a master device is used for computation. A completely different approach is the distributed topology where for each cell there is a separate cell board. This solution has advantages in measurement accuracy, safety and reliability but is more expensive to produce.

III. Guidelines for Selection of BMS

As a summary, choosing the correct topology is crucial for the performance, reliability, reparability, safety and total cost of the BMS. A centralized solution is a proper choice in battery packs with fewer cells and established production, the modular one is proper for prototyping, the most versatile solution has the master-slave topology and for precision measurements and better safety the distributed topology is superior.

A BMS needs a set of features to be sufficient on its own. A BMS that can only regulate (regulator) the total current and the voltage of a system is not sufficient for lithium cells as the example in the introduction shows. An improvement of this system is the meter. It measures each cell's voltage and indicates when a threshold is reached but cannot switch the charger ON and OFF. This problem is solved in the monitor circuits. Such a circuit cannot increase the performance of the whole system significantly (if any) since they are not able to balance the battery pack. So, a monitor circuit as a stand-alone is not sufficient as a BMS. Where a balancer circuit completes all the essential task of a BMS. It drastically increases the efficiency of the charge-discharge cycle of the battery pack. The last variation in this category is the protector circuit. Essentially the protector is a balancer circuit that incorporates a semiconductor switch in the same package. As a summary, regulators, meters and monitors are not sufficient to act as a stand-alone BMS while a balancer and protector circuits are. The protector circuits are suitable for small battery packs and the balancer circuit are suggested as superior for professional applications according to Fig. 1.

Based on this analysis a selection guideline later is synthesized. When working with lithium cells the following steps can be used to extend the SOA, the efficiency, reliability and response time:

- With or without BMS – if more than one cell is used a BMS is mandatory
- Analogue or Digital – for low price, small packs and established productions an analogue and for large pack and in development a digital BMS should be used
- Choosing the correct topology:
  - Centralized – fewer cells and established production
  - Modular – prototyping
  - Master-slave - most versatile
  - Distributed – precision measurements
- Sufficient as a stand-alone BMS:
  - Regulators - not sufficient
  - Meters - not sufficient
  - Monitors - not sufficient
  - Protector - sufficient for small battery packs
  - Balancer - superior
- Typical parameters:
  - Accuracy – 1 ÷ 5 mV
  - Sampling – 0.1 ÷ 1 s
  - Balancing current – 0.1 ÷ 5 A
  - Low voltage threshold – 2.8 ÷ 3.2 V
  - High voltage threshold – 3.65 ÷ 4.20 V

IV. Realized and Studied BMS

The system studied in this paper has a 12 bit ADC, 12 multiplexer inputs, 12 digital outputs and a communication interface. An operational amplifier at every analog input is used in order to measure the voltage of each cell. The measurement accuracy of each channel is ±5 mV. A transistor switches at each digital output is used in order to control the control the ballast resistors discharging the cells to the threshold voltage.

A classical approach of testing with passive balancing is used. Furthermore, a hysteresis cycles are used while balancing in order to receive as efficient charging as possible. The experimental setup, studied in this paper consist of six $LiFePO_4$ cells with 40 Ah capacity each.

Input parameters of the system:

- Charging current – 2.5 A
- Balancing current – 400 mA
- Balancing voltage – 3.630 V
- Cell high voltage threshold – 3.650 V
- Charge enable threshold (balancing) – 3.630 V

The following algorithm is used while balancing – when one of the cells reaches the high voltage threshold (3.650 V) during the charging state the process stops and all the cells with voltage greater than the balancing voltage (3.630 V) are discharged to the charge enable threshold (3.630 V) through the ballast resistors. When all the cells have been

discharged to 3.630 V the charging process continues. The process of charging and discharging is known as hysteresis charging. It is important to note here that only the cells with voltage higher than 3.630 V are being discharged. This operation is being repeated until all the cells reach the balancing voltage.

A block scheme of the example studied in this paper is presented in Figure 2.

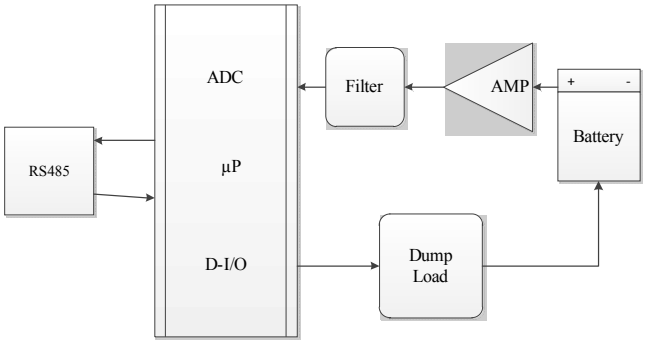

Fig. 2. Block scheme of the studied BMS example

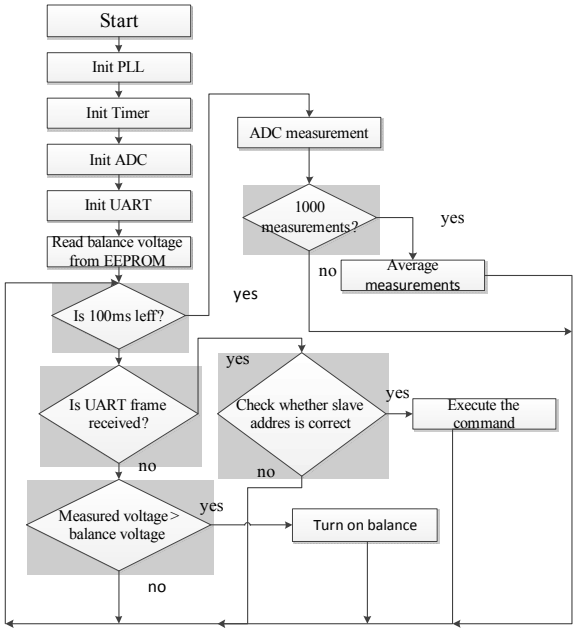

Fig. 3. Realized algorithm of operation of the studied BMS

The BMS presented with the block scheme (Figure 2) and studied in this paper operates based on the algorithm depicted in the block scheme Figure 3.

V. Experimental Results

Figures 4 and 5 present the charging process where an active level (1) means that a charging current is flowing and low level (0) where there is no charging. During the active period the cells are being charged and some of them reach the upper threshold (3.650 V). The interval between two active levels represents cells reached this threshold and being discharged through the ballast resistors. It should be noted that in the beginning of the balancing process the periods for charging and balancing are relatively short. However, when the cells are getting more and more equalized those intervals become longer and longer.

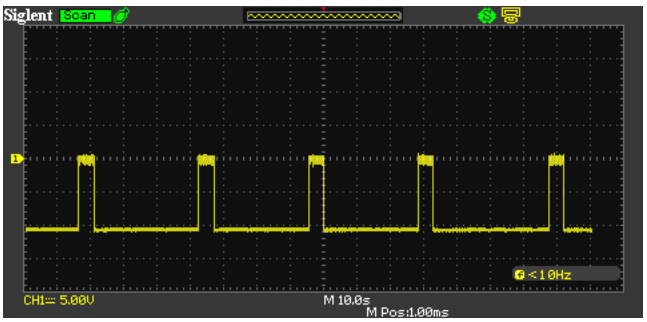

Fig. 4. Experimental results, strongly unbalanced cells, series 4 shown on fig.5, charging current 5 A

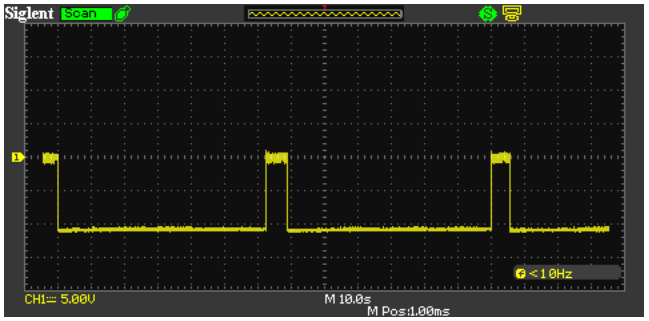

Fig. 5. Experimental results, last balancing cycle, series 1 shown on fig.5, charging current 5 A

Figure 6 shows the voltages of the six studied cells via samples during charging and balancing. There is a noticeable difference between the cell voltages and the cell capacities respectively in the beginning of the charging process. In the other sampling points it can be seen that the differences in the voltages reduces and in the last sample it is ±10 mV. This is acceptable unbalance for the nominal operation of the stack and the cells are assumed as balanced.

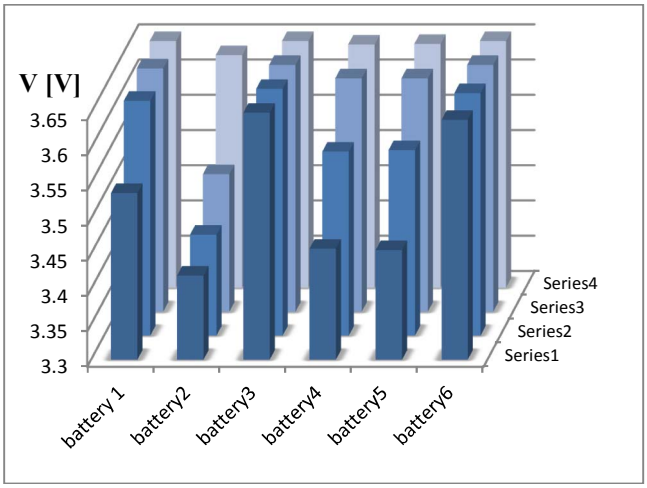

Fig. 6. Comparison of the voltage across six studied cells during the charging process

The temperature of cells is being measured during the charging process via digital temperature sensors.

Experiments with twice as large battery pack are also conducted. The results from the experimental study are summarized in Table 1 and visually presented in Figure 7. Important parameters from the experiment are the balancing time of 60 minutes and the cut of voltage of 3.65 V corresponding to the high voltage threshold of the system, determined in section four.

TABLE 1. EXPERIMENTAL RESULTS PRESENTING THE BATTERY PACK BALANCING PROCESS

time	Cell 1	Cell 2	Cell 3	Cell 4	Cell 5	Cell 6	Cell 7	Cell 8	Cell 9	Cell 10	Cell 11	Cell 12
min	V	V	V	V	V	V	V	V	V	V	V	V
0	3.536	3.419	3.650	3.457	3.455	3.640	3.550	3.500	3.602	3.579	3.469	3.592
20	3.633	3.543	3.650	3.561	3.563	3.644	3.641	3.620	3.640	3.647	3.590	3.648
40	3.645	3.595	3.650	3.631	3.631	3.650	3.650	3.650	3.650	3.650	3.648	3.650
60	3.650	3.630	3.650	3.645	3.646	3.650	3.650	3.650	3.650	3.650	3.650	3.650

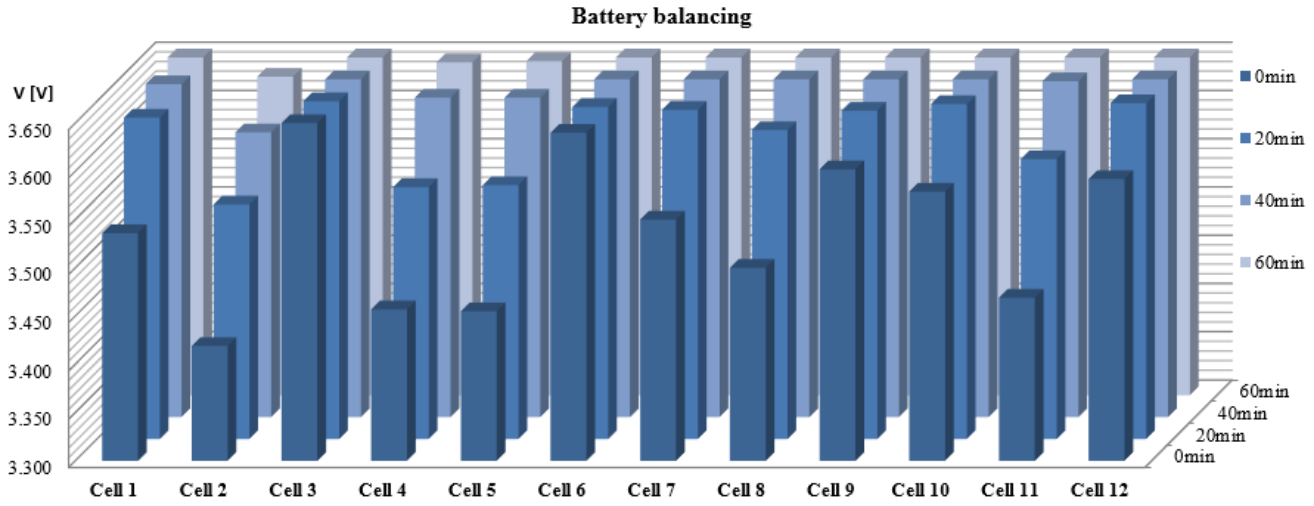

Fig. 7. Comparison of the twelve studied cells during the balancing process

VI. CONCLUSION

The importance of a BMS when operating with lithium-ion cells, especially within narrow SOA is highlighted in this paper.

A classification of BMSs is proposed based on four criteria (technology, topology, functionality and features).

Based on the classification guidelines for optimal selection of a BMS for given application are also proposed. Furthermore an example of common applications and typical parameters are also given. Using the proposed guidelines an example BMS is selected and studied experimentally.

The studied system operates within the SOA, reveals high accuracy during the balancing process, and achieves short response time. The proposed BMS is easy to setup and use. The algorithm applied for experimental validation is presented and discussed.

ACKNOWLEDGEMENTS

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Investigation and Analysis of the Modified Phase-Shifted Pulse Modulation Resonant DC/DC Converter

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Abstract – ***In this paper an investigation and analysis of the modified phase-shifted pulse modulation (PSPM) DC/DC resonant converter topology, is presented. The possibilities for achieving soft switching conditions with high-efficiency operation in a wide range of power regulation activities will be investigated.***

In the paper, the first harmonic analysis method can be employed to develop expressions for the output circuit variables of the of the modified PSPM DC/DC resonant converter. The results of the analysis are confirmed with computer simulations.

Keywords – ***phase-shifted pulse modulation (PSPM) DC/DC resonant converter topology***

I. INTRODUCTION

Resonant power converters have gained increased attention in the industry due to their varied advantages over conventional pulse-width (PWM) converters. Resonant converters have been widely used because of their ZVS, ZCS capabilities [1,2,3]. Based on them, DC-DC converters [3,4,6], power factor correction circuits, electronic welding, etc. are being developed. The investigations are focused on searching for circuit topologies and algorithms to control DC/DC converters with the following requirements: high efficiency for a wide load range and low idle losses; decrease of the switching losses of the switching devises (conditions for soft commutation); output voltage control and maintaining soft commutation conditions when there are load changes.

In the paper [1] a cost effective high-efficiency high frequency soft switching PSM (phase shift modulation) controlled full bridge inverter for induction heating applications is proposed.

Based on the control method shown in [1], in the present paper, an investigation and analysis of the modified phase-shifted pulse modulation (PSPM) DC/DC resonant converter topology is proposed. The possibilities for achieving soft switching conditions with high-efficiency operation in a wide range of power regulation activities will be investigated.

In this paper, the first harmonic analysis method can be employed to develop expressions for the output circuit variables of the modified PSPM DC/DC series resonant converter. The results of the analysis are confirmed with computer simulations with *Cadence PSpice* simulator.

II. OPERATIONAL PRINCIPLE

Figure 1 shows a proposed full-bridge modified PSPM series resonant DC/DC converter and Fig.2 shows the converter operation waveforms.

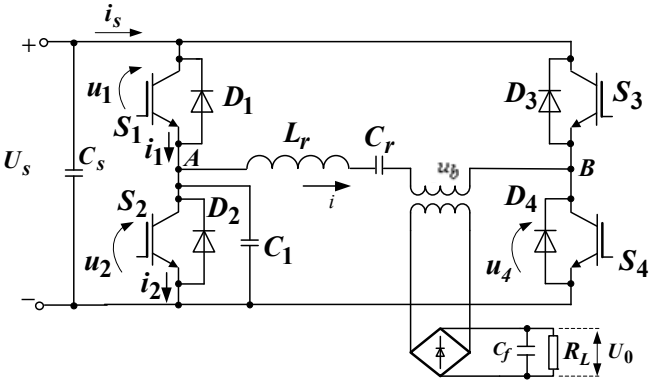

Fig.1 Full-bridge modified PSM series resonant DC/DC converter

The full-bridge converter consists of two legs (transistors S1, S2 and S3, S4 and their antiparallel diodes) and a lossless snubber capacitor C1 [1]. This topology can maintain soft switching operation in a wide range of power regulation activities, without others lossless snubber circuits. The gate pulses of the diagonal switches are fed with phase difference φ. In addition, the transistors S1, S2 and S3, S4 are both off for a short time interval, known as a dead time t_d. The transistors S1 (S2) are operated in current lagging mode and realize ZVZCS turn-on, while the transistors S3 (S4) can operate in the current leading mode and turn-off with ZVZCS. The lossless snubber capacitor C1 provides ZVS turn-off in S1 and S2. The PSPM converter can achieve soft switching operation when $\omega_0 = \omega_s$ by using the control algorithm, shown in Fig.2.

The following common symbols are used:

$\omega_0 = \frac{1}{\sqrt{L_r C_r}}$ - angular resonant frequency; ω_s - switching frequency, $Z_0 = \sqrt{L/C}$ - characteristic impedance of the resonant circuit.

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The analysis is made under the following assumptions: the matching transformer is ideal; transformer turn ratio is one, the converter elements are ideal.

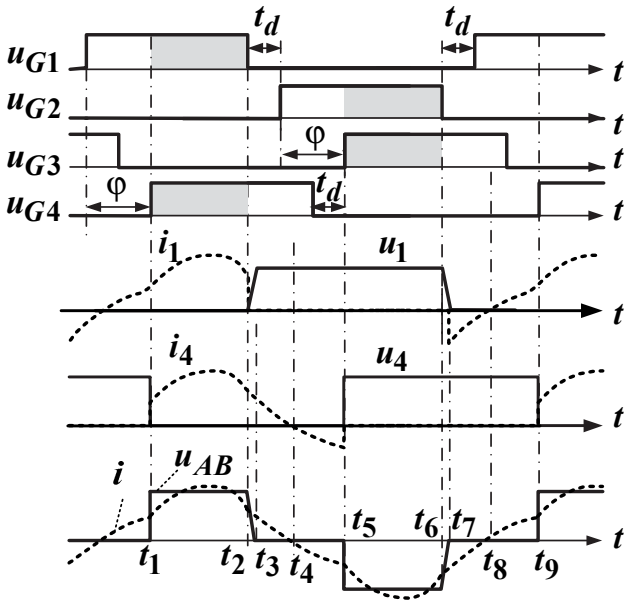

Fig.2 Waveforms of PSPM resonant converter.

The operational principle includes eight intervals, as follows:

- Interval $t_1 \div t_2$ - the transistors S1 and S4 are turned on and the power supply voltage Us is fed to the load.
- Interval $t_2 \div t_3$ - the transistor S1 is turned off, while the transistor S4 is still on. The capacitor C1 starts to discharge. Voltage u_2 across the capacitor C1 gradually changes from Us to zero. At the same time, voltage u_1 gradually increases from zero to Us, i.e. the transistor S1 is turned off at zero voltage conditions.
- Interval $t_3 \div t_4$ - the voltage of the transistor S2 is zero, while the current starts to flow through the diode D2.
- Interval $t_4 \div t_5$ - in this mode, S2 is turned on at zero voltage (ZVZCS) and S4 is turned off at ZVZCS. The resonant current i flows in the following loop: S2 - D4 -Cr -Lr.
- Interval $t_5 \div t_6$ - the transistor S3 is turned on and the power supply voltage Us is fed to the load through transistors S2 and S3. The output power of the inverter is controlled by the duration of this interval.
- Interval $t_6 \div t_7$ - the transistor S2 is turned off and capacitor C1 starts charging from zero to U_S, which allows the transistor S2 to turn-off at zero voltage.
- Interval $t_7 \div t_8$ - when the capacitor C1 is fully charged, the diode D1 is turned on. The current i flows in the following loop: D1 - S3 - Cr -Lr.
- Interval $t_8 \div t_9$ - in this interval the resonant current i flows in the opposite direction, as a result the transistor S1 is turned on at ZVZCS and the transistor S3 is turned off at ZVZCS.

To prevent the capacitor C1 discharge current from affecting the inverter operation, the capacitor must be charged to the supply voltage before starting up [1]. The value of C1 is recommended to be evaluated as follows:

$$C1 = \frac{U_S}{t_{com}} I_{off} \ , \tag{1}$$

where t_{com} is the voltage soft commutation time and I_{off} is the instantaneous current value at turn-off.

In this converter, the phase difference φ provides the soft switching operation and the capability of power regulation.

According to the first harmonic analysis method, it is assumed that in the considered circuit (Fig.1) only the first harmonics of the current i, voltages u_{AB}, u_b, u_{Lr}, u_{Cr} and u_o are operated.

The series-resonant converter uses a capacitive output filter. The equivalent ac circuit of Fig. 3 will be used [5].

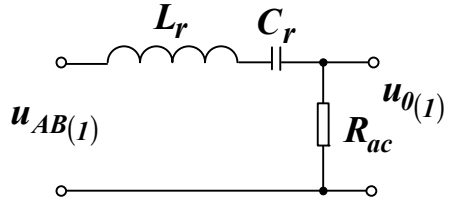

Fig. 3 AC equivalent circuit for the converter

For this case the equivalent ac resistance is given by

$$R_{ac} = \frac{8}{\pi^2} R_L \tag{2}$$

Note that $u_{AB(1)}$, is the fundamental component of the voltage applied to the resonant circuit by the inverter. This voltage is, for the full bridge converter, of magnitude Us**.** Therefore, the RMS value of AC fundamental voltage $u_{AB(1)}$ in the inverter is given by

$$U_{AB(1)} = \frac{2\sqrt{2}}{\pi} U_s \cos\left(\frac{\theta_\varphi + \theta_d}{2}\right) \tag{3}$$

The RMS value of AC fundamental voltage $u_{0(1)}$ can be expressed as:

$$U_{0(1)} = \frac{2\sqrt{2}}{\pi} U_0 \tag{4}$$

The phase difference φ and the dead time t_d are calculated in radians as follows: $\theta_d = 2\pi f_0 t_d$ and $\theta_\varphi = \frac{\pi\varphi}{180}$.

The proposed converter operates at resonant frequency and the output power P_0 is given by:

$$P_0 = \frac{U^2_{AB(1)}}{R_{ac}} = \frac{8}{\pi^2 R_{ac}} U^2{}_s \cos^2\left(\frac{\theta_\varphi + \theta_d}{2}\right) \tag{5}$$

The three-dimensional representation of the normalized power P'_0 is plotted on Fig. 4.

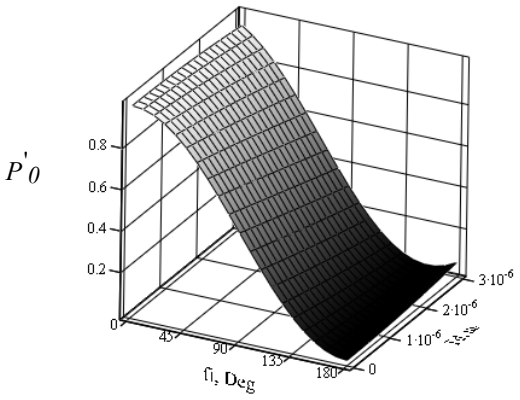

Fig. 4. Three-dimensional representation of the normalized power P'_0 as a function of φ [deg] and t_d [μs]

A wide soft switching region within the power regulation range can be achieved if the phase difference φ meets the following conditions [1]:

$$\theta_d \le \theta_\varphi \le \pi - \theta_d \tag{6}$$

It can be seen that the soft switching operation of the converter is limited by the dead time t_d.

The amplitude of the fundamental wave of the resonant current i can be calculated

$$I_{(1)m} = \frac{4}{\pi R_{ac}} U_s \cos\left(\frac{\theta_\varphi + \theta_d}{2}\right) \tag{7}$$

The normalized amplitude of the fundamental wave $I'(1)_m$ is plotted on Fig. 5.

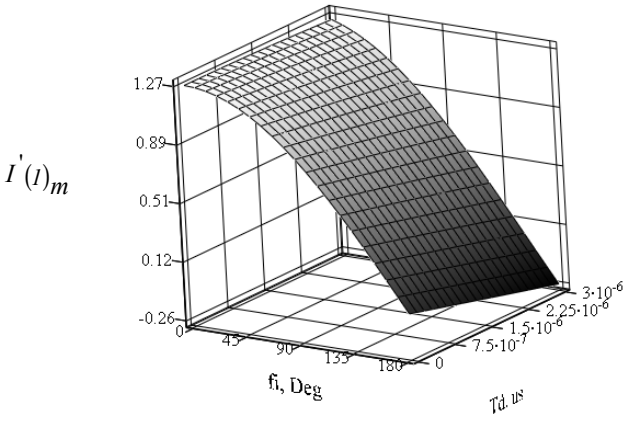

Fig. 5. Three-dimensional representation of the normalized current $I'(1)_m$ as a function of φ [deg] and t_d [μs]

Hence, the maximum amplitude of the voltage across the resonant capacitor C is given by

$$U_{Crm} = \frac{I(1)_m}{\omega_0 C} \tag{8}$$

Fundamental wave of the turn-off current $Ioff_{(1)}$ is obtained from the equation

$$Ioff_{(1)} = \frac{4}{\pi R_{ac}} U_s \cos\left(\frac{\theta_\varphi + \theta_d}{2}\right) \sin(\theta_\varphi - \theta_d) \tag{9}$$

The normalized fundamental wave of the turn-off current $I'off_{(1)}$ is plotted on Fig. 6.

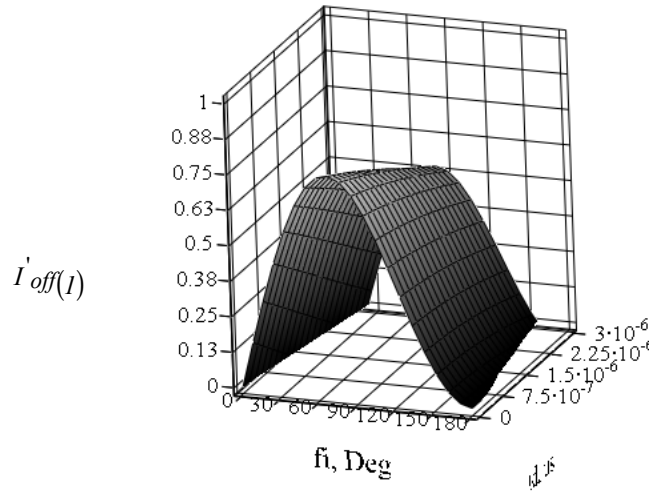

Fig. 6. Three-dimensional representation of the normalized current $I'off(1)$ as a function of φ [deg] and t_d [μs]

As shown in Fig. 6, the value of the turn-off current $I'off(1)$ becomes largest when the pulse phase difference $\varphi = 45^\circ - 90^\circ$ and the maximum value is obtained around $\varphi \approx 77^\circ$.

To achieve the converter high-efficiency operation, the turn-off operation of S1 and S2 and the turn-on operation of S3 and S4 need to be improved to achieve soft switching.

The switching loss included: turn-off loss per device, turn-on loss per device, diode reverse-recovery loss and semiconductor output capacitances loss.

The losses of the output capacitances and diode reverse-recovery are not significant therefore they can be neglect [7]. Then the switching losses for one commutating period can be expressed as:

$$E_{S1,S2} = E_{on} + E_{S1,S2turn-on} + E_{S1,S2turn-off} \tag{10}$$

and

$$E_{S3,S4} = E_{on} + E_{S3,S4turn-off} + E_{S3,S4turn-on} \tag{11}$$

The energy losses $E_{S1,S2turn-on}$ and $E_{S3,S4turn-off}$ are neglected due to the soft switching.

III. SIMULATION RESULTS

The computer simulation results of the DC/DC converter are given by the following conditions: power supply U_S=100V; resonant link elements L= 40μH and C= 450nF; capacitor C1=0.047μF; dead time $t_d = 1\mu s$ and phase difference $\varphi \approx 67^\circ$. The MOSFET IRF250 power devices are chosen.

Fig. 7 shows waveforms of the voltages u_{AB} and u_b, and Fig. 8 shows waveforms of the resonant current i and the drain current of the transistor S1. The simulation results are compared with theoretical results in Table 1.

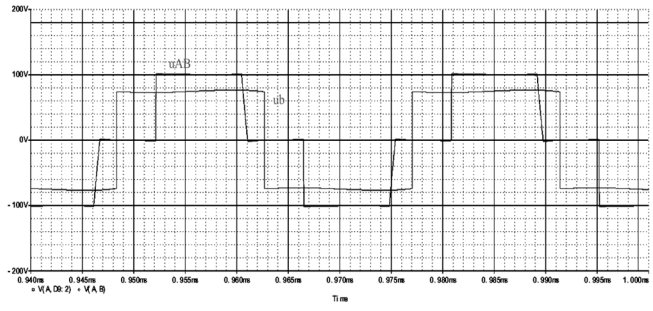

Fig. 7 Waveforms of the voltages u_{AB} and u_b,

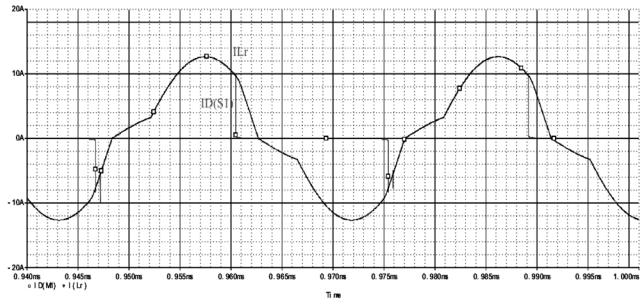

Fig. 8 Waveforms of the current i and the drain current of the transistor S1

TABLE I COMPARISON BETWEEN THEORETICAL AND SIMULATION RESULTS

	I_m	I_{off}	U_{Crm}
Evaluation (FHA)	12.1A	9.7A	114,4V
From PSpice	12.6A	9.8A	114V
Error δ, %	4%	1%	0.5%

A good coincidence between theoretical and simulation results can be seen.

Figure 9 shows the voltage and current waveforms of S1 when phase difference $\varphi \approx 67^\circ$. It can be seen the turn-off losses per device. Figure 9 demonstrates that S1 completed the ZVZCS turn-on. Furthermore, the turn-off operation was improved to ZVS condition due to the voltage soft commutation effect of C1.

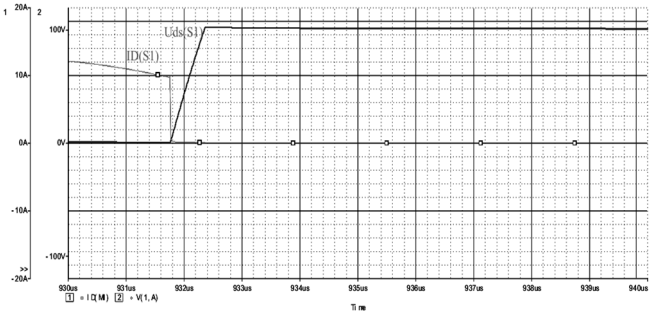

Fig. 9 Voltage and current of S1

II. CONCLUSION

In the paper an investigation and analysis of the modified phase-shifted pulse modulation (PSPM) full bridge DC/DC resonant converter topology is proposed. The control algorithm is based on the control method known in the literature.

The possibilities for achieving soft switching conditions with high-efficiency operation in a wide range of power regulation activities will be investigated.

In this paper, the first harmonic analysis method can be employed to develop expressions for the output circuit variables of the modified PSPM DC/DC series resonant converter. The results of the analysis are confirmed with computer simulations with *Cadence PSpice* simulator. As a future work the main steady-state equations can be presented, which allow fast engineering design, as well as the converter load characteristics will be built.

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Comparative Loss Analysis of Boost and Synchronous Boost DC-DC Converters

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Abstract – **The following paperwork presents a comparative analysis of synchronous and non-synchronous boost converters. Analytical determination of the losses is derived and compared with the results of the simulations. The compared converters are realized and investigated experimentally. Thermographic images are used to analyze the dissipated losses in the two converters and each of their components. A methodology for magnetic components loss calculations is proposed targeting loss optimization.**

Keywords – **DC-DC converters, losses, synchronous boost, magnetic components**

I. Introduction

Loss reduction and efficiency improvement of the power electronic converters is one of the most important problems for the power electronic experts. One of the methods for improvement of the electronic converters energy parameters is the reduction of the semiconductor devices switching losses by using the so called soft switching of current and/or voltage (ZVS or ZCS). They are usually realized via auxiliary resonant tanks connected either in series or in parallel to the semiconductor switch [1, 2, 3]. Another common approach in the DC converters is to use only controllable devices within the power circuit – the so called synchronous DC-DC converters [4, 5, 6]. In the following paperwork, evaluation of the losses in Boost DC-DC converter realized on the base of the classic and the synchronous topologies is made. In order adequate assessment to be carried out, the same passive elements, switching frequency, load and power supply are used.

II. Analytical Determination of the Losses

The circuit of the synchronous boost DC-DC converter is presented in fig. 1. It consists of two transistors T1 and T2, a filter capacitor C and a filter inductor L. In the classic topology, the transistor T2 is substituted by a diode VD.

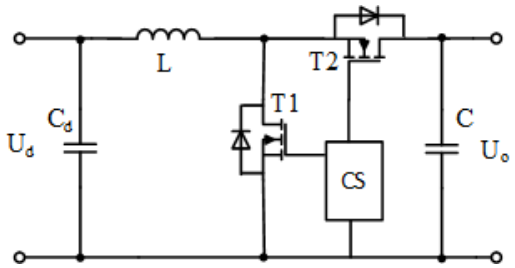

Fig. 1. Synchronous boost DC-DC converter circuit.

The circuit losses for the classic topology are as follows [7, 8, 9, 10]:

- transistor losses P_{T1} (due to conduction and switching), determined by the expression:

$$P_{T1} = P_{R_{DS}} + P_{SW} = \left[\frac{DR_{DS}}{(1-D)^2 R} + \frac{1}{2} f C_0 R\right] P_0 \qquad (1)$$

where D is the duty cycle; R_{DS} – drain-source on resistance; f – switching frequency; C_O – transistor output capacitance; R – load resistance; P_O – output power.

- diode losses P_{VD} (due to the forward voltage drop and the dynamic forward resistance):

$$P_{VD} = P_{V_F} + P_{R_F} = \left[\frac{V_F}{V_0} + \frac{R_F}{(1-D)R}\right] P_0 \qquad (2)$$

where V_F is the forward voltage drop; R_F is the diode dynamic forward resistance; V_O – output voltage.

- filter inductor losses:

$$P_{R_L} = \frac{R_L P_0}{(1-D)^2 R} \qquad (3)$$

where R_L is the filter inductor active resistance.

- filter capacitor losses:

$$P_{R_C} = \frac{DR_C P_0}{(1-D)R} \qquad (4)$$

where R_C is the filter capacitor active resistance.

When a synchronous DC-DC converter is used, the circuit losses are determined analogically with respect to the second transistor operation:

$$P_{T2} = P_{R_{DS}} + P_{SW} = \left[\frac{DR_{DS}}{(1-D)^2 R} + \frac{1}{2} f C_0 R\right] P_0 \qquad (5)$$

III. Modelling Results

Fig.2 and fig. 3 present three-dimensional dependences of the overall circuit losses P_{SUM} for the two examined topologies as function of the duty cycle D and the output power P_0.

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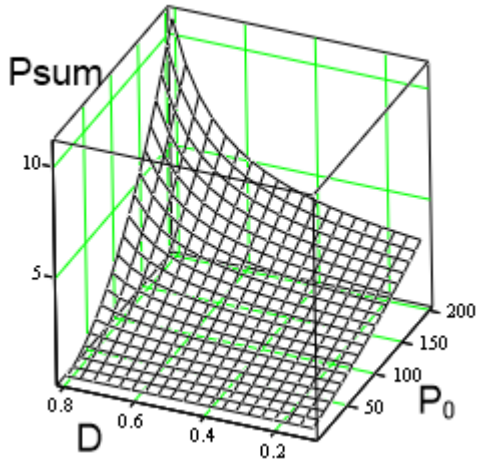

Fig. 2. Overall circuit losses (classic topology) as function of the duty cycle and the output power.

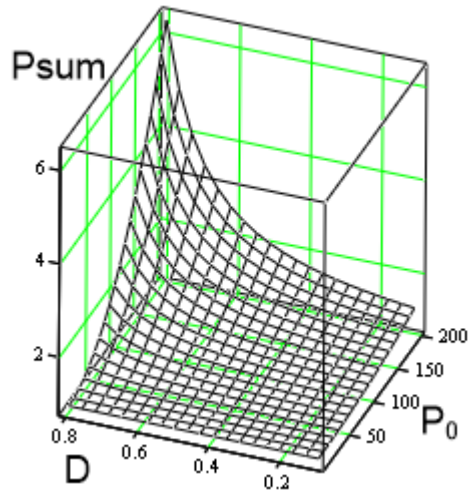

Fig. 3. Overall circuit losses (synchronous topology) as function of the duty cycle and the output power.

IV. Simulation Results

Simulation examinations of a synchronous and a non-synchronous boost converters are carried out. Fig. 4 presents the transistor T1 voltage rising edge, and fig. 5 presents both the transistors T1 and T2 voltages. Inferences for the switching losses can be made on this base.

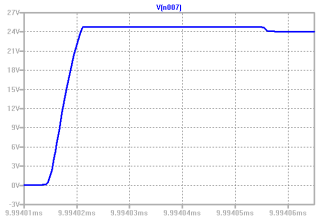

Fig. 4. Transistor T1 voltage rising edge for a synchronous converter.

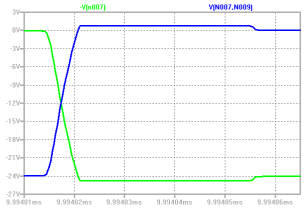

Fig. 5. Transistors T1 and T2 voltages for a synchronous converter.

Fig. 6 presents results from simulation examinations of the transistor T2 losses for a synchronous circuit and the corresponding diode VD losses for a non-synchronous converter with variation of the two circuits switching frequency.

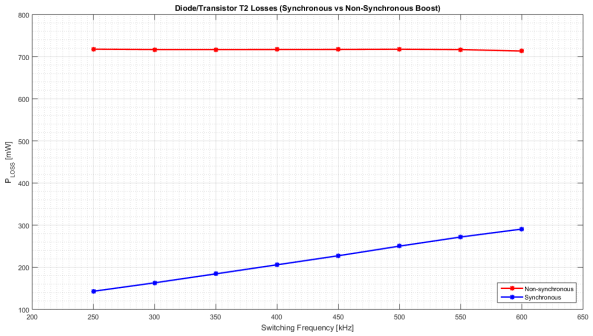

Fig. 6. Losses in the transistor T2 and the diode VD.

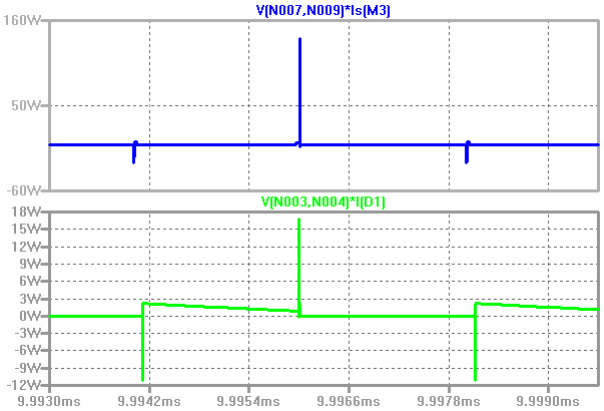

Fig. 7. Transistor T2 loss power for a synchronous circuit and diode loss power for a non-synchronous circuit.

V. Loss Reduction Design for Inductors

Further, the converter total losses could be optimized by a proper design of the inductors. Possible approaches for loss reduction of eddy current losses in gapped inductors:

1. Using Litz wire or paralleled wires;
2. Keeping some distance between the winding and the air gap.

An important fact to be considered in that the field close to the air gap causes an ‘induction heating’ of the windings by the transverse field to the air gap has to be avoided.

- Design methodology for loss reduction

To optimize the design the approach 'Saturated, thermally limited fast design approach' [11] is used. The approach starts with defining a proper core size. Loss calculation contains two important steps: according to calculated AC peak induction value ΔB_p finding the core losses, and calculating eddy current losses in windings. The classical equation of Dowell for the ferrite core losses in the case is not accurate as the voltage waveforms are square. More precise calculation of core losses P_{Fe} is possible by NSE (Natural Steinmetz Model) model [12], valid for square voltage waveforms:

$$P_{Fe,NSE} = \left(\frac{\Delta B}{2}\right)^{\beta-\alpha} \frac{k_N}{T} \int_0^T \left|\frac{dB}{dt}\right|^{\alpha} dt \qquad (6)$$

According to the used approach, eddy current losses in the windings in high-frequency cases ($d < 2.7\delta$, d is the wire diameter and δ is the current penetration depth) are presented by a global loss factor k_C, which represents the ratio between the eddy current losses $P_{EDDY,CU}$ and the losses in the ohmic resistance R_0 [11]:

$$P_{EDDY,CU} = \left(R_0 I_{AC}^2\right) k_C\left(m_E, f_{op}, d_P, \eta, \lambda\right) \quad (7)$$

where m_E is an equivalent layer, f_{op} - operating frequency, d_P - wire diameter, η – relative filling between the conductors, λ – relative filling between the layers.

A simplified eddy current loss factor k_C is defined as:

$$k_C = \left(\frac{pNd_P}{w}\right)^2 k_F k_{in}\left(f_{eq}\right) \quad (8)$$

where k_F is the 'field factor'; the coefficient k_{in} is found according to the Fig.1; p is the number of wires in parallel, if there are such (or the number of strands in a Litz wire).

The field factor k_F represents the influence of the air gap fringing field. It is highly dependent on the distance of the winding to the air gap. The corresponding high eddy current losses are located close to the air gap and can cause local overheating.

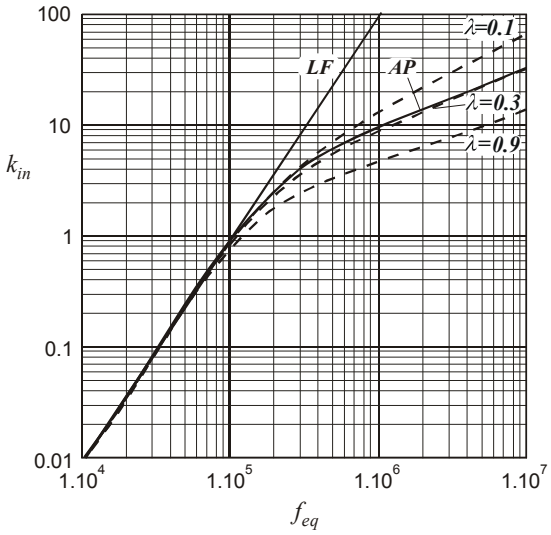

Fig.8 Inductor case, kin as a function of feq for η = 0.9, d = 0.5mm, ρ = 23×10-9, high mE values; Straight full line: low frequency solution LF; Full curve AP - recommended approximation; Dashed curves: solutions for λ = 0.1, 0.3, 0.9.

The geometric parameters used to describe k_{in} are:

- copper fill factor in the direction of the layer η can be defined as $\eta = n \cdot d/w$, where d is the wire diameter, n is the number of turns in a layer, w is the winding width;
- copper fill factor in the direction perpendicular to the layer λ can be defined as $\lambda = m_E \cdot d/h$, where h is the window height.

To use the provided graph (Fig.8) for any frequency fop and wire diameter, the equivalent frequency is to be found by:

$$f_{eq} = f_{op}\left(\frac{d}{0.5}\right)^2 \quad (9)$$

where $d[mm]$ is the wire diameter of the considered design.

At the last step an air gap length is determined.

Following the approach, an optimized design is realized. The inductor parameters are shown in Table I. Total power loss of the inductor based on pot core P14x8, core material N87 is 0.753W under the experimental conditions. For comparison, the power loss of the commercially offered inductor Coilcraft XAL7030-103MEB is 1.035W, found by manufacturer facilities.

TABLE I. DESIGN PARAMETERS, CORE P 14 X 8, MATERIAL N87

Wire diameter, [mm]	Number of turns	Bp, [T]	Air gap [mm]	Pcu,[W]		Pfe, [W]	Ptot, [W]
				ohm	eddy		
0.45	7	0.101	0.147	0.306	0.084	0.363	0.753

VI. EXPERIMENTAL RESULTS

Experimental examinations of two converters (a synchronous and a non-synchronous) are carried out with respect to the following parameters: input voltage 12V, output voltage 24V, load current 1.5A and operating frequency 400 kHz. Fig. 9, fig. 10 and fig. 11 present waveforms of the diode voltage for the non-synchronous circuit and the transistors T2 and T1 voltages for the synchronous converter.

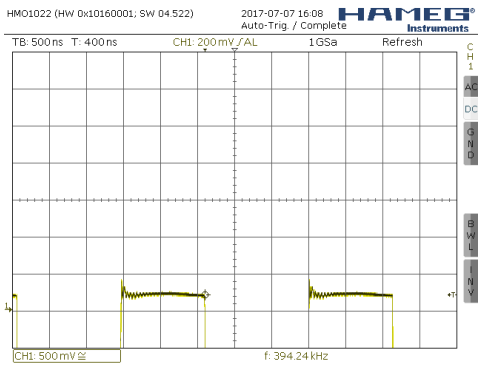

Fig. 9. Diode voltage for the non-synchronous circuit.

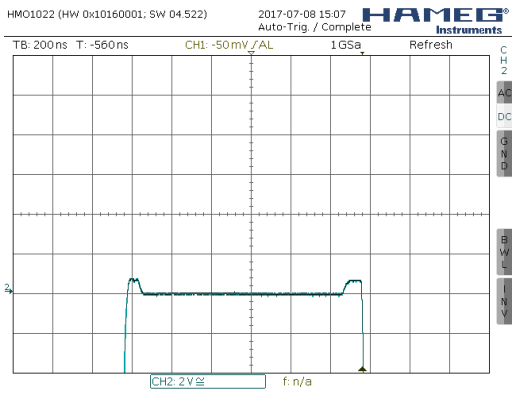

Fig. 10. Transistor T2 voltage for the synchronous converter.

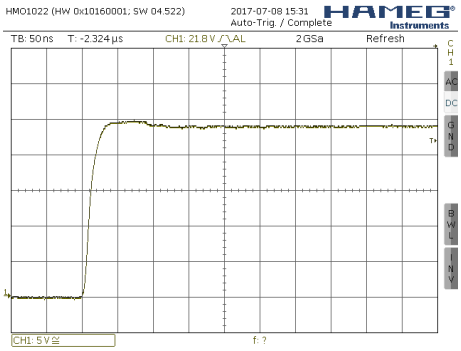

Fig. 11. Transistor T1 voltage rising edge for the synchronous circuit.

Fig. 12 presents a thermographic image of a module with two converters - a synchronous and a non-synchronous circuit. The two converters are identically loaded. Markers showing the separate elements temperatures are placed as follows:

For the non-synchronous circuit:

- Marker 1 – inductor temperature (92.2°C)
- Marker 2 – diode temperature (73.0°C)
- Marker 3 – transistor temperature (75.2°C)

For the synchronous circuit:

- Marker 4 – Inductor temperature (84.3°C)
- Marker 5 – transistor T2 temperature (74.1°C)
- Marker 6 – transistor T1 temperature (68.3°C)

Fig. 12. Thermography image of the experimentally examined converters.

From the displayed temperatures, it can be seen that the synchronous circuit inductor losses are reduced due to the slightly smaller input current and the ferrite core composite material. The diode and the equivalent transistor T2 temperatures are commensurable, which is caused by the smaller heatsink area of the synchronous converter.

VII. Conclusion

The paperwork presents a comparative analysis of non-synchronous and synchronous boost DC-DC converters. Loss comparison between the two converters is made.

As a result from the analysis, expressions are obtained and dependencies are built for the losses in the two circuit topologies. The obtained characteristics allow quick evaluation of the losses in order the proper topology to be chosen depending on the particular requirements. The analytical dependencies are verified by examinations with experimental stand.

From the examinations carried out, it can be seen that the magnetic component losses are commensurable to those in the semiconductor switches. This is confirmed by the thermographic investigation of the converters. The classical simulation examinations can provide only the inductors active resistance losses. For design and evaluation of high efficiency DC-DC converters, models of the magnetic components are necessary to be developed in order to provide their losses during simulation of the circuit operation. This is possible with the use of the model based design advantages, as well as, the development of magnetic component reduced models allowing fast calculation process and comparatively good accuracy.

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A Control Technique for a Bidirectional Series Resonant DC-DC Converter

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Abstract – **The following paperwork considers a bidirectional series resonant DC-DC converter operating above the resonant frequency with the usual phase-shift control. Its features are discussed. Some of the converter disadvantages are proposed to be compensated by means of a control technique. For this purpose, simultaneous phase-shift and frequency control is applied. The advantages of the proposed solution are verified by computer simulations.**

Keywords – **Bidirectional Converter, Series Resonant DC-DC Converter, Control Technique, Efficiency**

I. INTRODUCTION

Although they are well-known and widely used [1, 2], the bidirectional resonant DC-DC converters continue to be thoroughly examined [4]. This is due to their multiple advantages. During operation above the resonant frequency similarly to the other resonant converters, it is possible the power devices to switch at zero voltage (ZVS). In this way, the switching losses are significantly reduced and high efficiency is obtained.

Regardless of the topology for realization of the bidirectional converter, the direction and the quantity of the transferred energy are varied mainly by means of applying phase-shift control technique [1, 2]. This solution has some drawbacks the options for overcoming of which are continuously being looked for [4, 5].

The results from the theoretical analysis presented in [6] show an important advantage of the bidirectional series resonant DC-DC converter with classical phase-shift control. It has a behavior of an ideal current source. The non-linear control characteristic and the large resonant tank current value at no-load mode (when no energy is transferred in any direction) can be pointed as drawbacks. Of course, this is not a problem for operation at fixed load close to the nominal one.

In order to linearize the control characteristic of a bidirectional series resonant DC-DC converter operating above the resonant frequency, the classical phase-shift control in [7] is proposed to be combined with a proper variation of the operating frequency. The theoretical analysis shows that a nonlinear increase of the frequency is necessary. Nevertheless, a linear approximation leads to very good results. Moreover, the resonant tank current value at no-load mode is significantly reduced, which is a premise the converter efficiency to be increased.

In the following paperwork, the presented in [7] research is extended. According to the filled requirements, a system for control of bidirectional series resonant DC-DC converter operating above the resonant frequency is synthesized. The features of this implementation are verified via computer simulations.

II. THE CONTROL TECHNIQUE

A. Converter Operation at Constant Frequency

The converter circuit is well-known (fig. 1). It consists of two identical bridge inverter stages, a series resonant tank (L, C) and a coupling transformer Tr with a transformation ratio k. Fig .1 also presents the snubber capacitors $C_1 \div C_8$ by which a zero-voltage switching is obtained. Each of the transistors in the inverter stages is controlled by means of a ZVS driver such as the one presented in [3].

The inverter stage (transistors $S_1 \div S_4$) to which a voltage U_d is applied is chosen to be the "input" one, and the other (transistors $S_5 \div S_8$) to which a voltage U_0 is applied to be the "output" one.

According to the energy transfer direction, two operating modes are possible. During the first one called ***DIRECT MODE***, the energy is transferred from the "input" to the "output", i.e. from the source with voltage U_d to the one

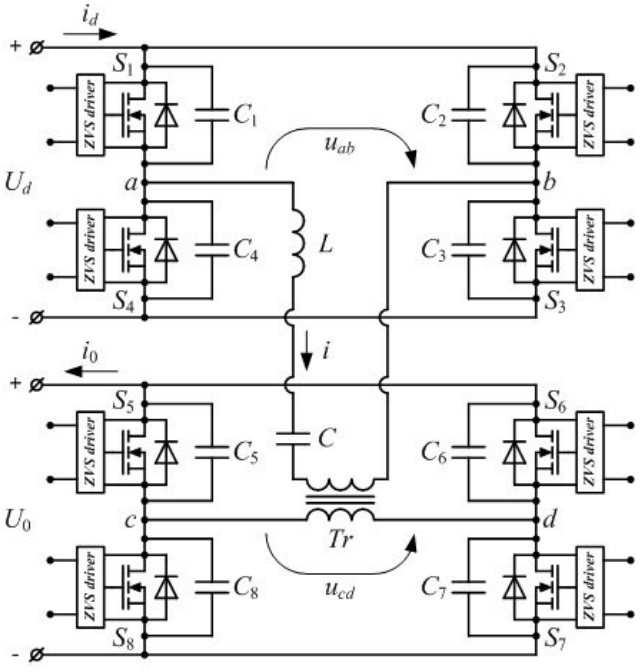

Fig. 1. The Bidirectional Converter Circuit

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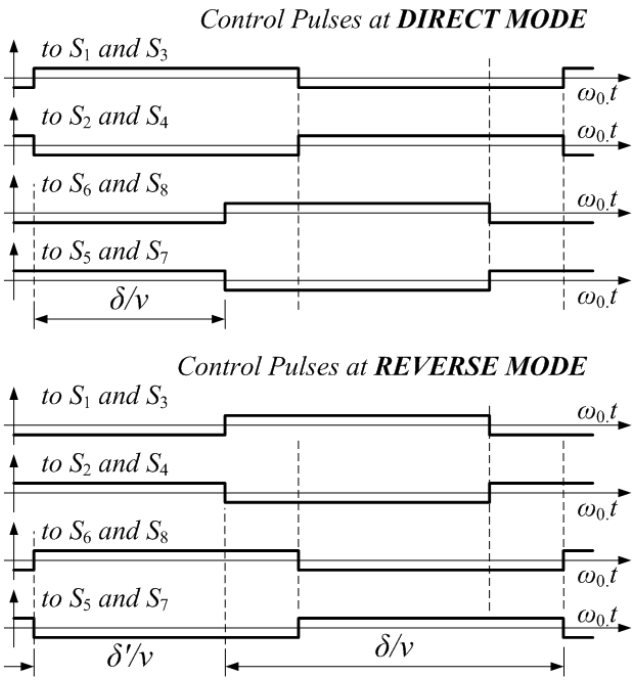

Fig. 2. Waveforms of the control pulses

with voltage U_0. The second one is called ***REVERSE MODE***. During this mode the energy is transferred oppositely (from U_0 to U_d).

Fig. 2 presents waveforms of the control pulses submitted to the ZVS drivers in the inverter stages. According to the classical control technique, the converter operates at a constant frequency $\omega_S = 2\pi f_S$ which is above the resonant frequency ω_0. The control pulses submitted to the "output" stage switches ($S_5 \div S_8$) are phase-shifted from the ones submitted to the "input" stage switches ($S_1 \div S_4$) at an angle δ with respect to the operating frequency ω_S. In this way, the output power control is obtained by phase-shifting – the variation of the angle δ. For $\delta < \pi$, ***DIRECT MODE*** is obtained, and for $\delta > \pi$ – ***REVERSE MODE*** is obtained.

Angle δ is related to the operating frequency ω_S.

The presented in [6] theoretical analysis is carried out considering the following assumptions: all the circuit elements are ideal, the commutations are instantaneous, and the ripple of the voltages U_d and U_0 is negligible. Then, the resonant frequency, the characteristic impedance and the frequency detuning are determined as follows:

$$\omega_0 = 1/\sqrt{LC}\ ;\ \rho_0 = \sqrt{L/C};\ \ \nu = \omega_S / \omega_0 \qquad (1)$$

In order to obtain generalized results, all the quantities are normalized as follows: the voltages with respect to U_d; the currents – with respect to U_d/ρ_0.

At these conditions, expressions are obtained and load and control characteristics are built in [6]. From them, it can be seen that the converter behaves as an ideal current source. Moreover, independently from the energy transfer direction, the output voltage may significantly exceed the input. However, at values of the control parameter in the range $-\pi/2 \le \delta \le +\pi/2$, the converter ZVS operating area is significantly restricted. Another important result is the nonlinear shape of the control characteristic.

B. Linearization of the Control Characteristic

In [7], an idea for linearization of the control characteristic at variation of the control parameter in the range $\pi/2 \le \delta \le 3\pi/2$ where the converter operates at ZVS with no limitation is shown. It is illustrated in fig. 3. In this case, U'_0 and I'_0 annotate the normalized output voltage and the average output current values. The figure presents a „conventional" control characteristic (with dotted line). It is obtained at $U'_0 = 1$, $k = 1$, $\nu = \text{const} = 1{,}15$ and variation of the control angle in the range $\pi/2 \le \delta \le 3\pi/2$. A new desired linear characteristic (with thick line) determined by the two endmost output current values at $\delta = \pi/2$ and $\delta = 3\pi/2$ is also presented.

In ***DIRECT MODE***, a point A_1 from the first characteristic at which the output current has a value of I'_{01} corresponds to a value of the angle $\delta = \delta_A$. Again for angle $\delta = \delta_A$, a point A_2 is obtained upon the desired characteristic. Now, the output current has a smaller value $I'_{02} < I'_{01}$. It is known that when a series resonant converter operates above the resonant frequency, its output current value can be reduced by increasing the operating frequency ω_S, in this case – the frequency detuning ν. Only at $\delta = \pi/2$,

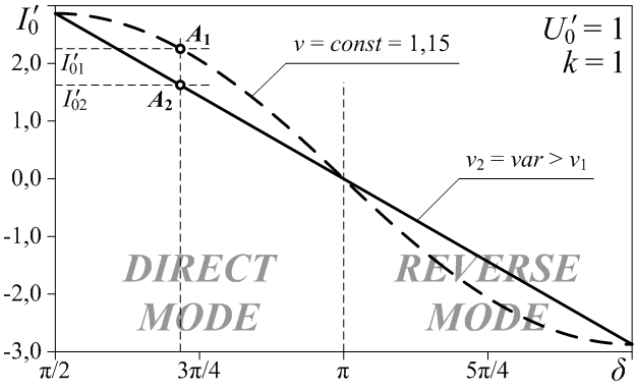

Fig. 3. Linearization of the Control Characteristic

the frequency is the same for both the old and the new characteristics.

For control angle variation in the range $\pi/2 \le \delta \le \pi$, the necessary variation of the detuning ν is determined in [7] by means of an iteration procedure. It turns out that in order to obtain the desired linear control characteristic, the detuning should be varied almost linearly together with the increase of angle δ from a minimum value ν_{min} at $\delta = \pi/2$ to a maximum value ν_{max} at $\delta = \pi$. Thus, for a control example when $\nu_{min} = 1.15$, it turns out that $\nu_{max} = 1.27178$.

Similar procedure can be used in ***REVERSE MODE*** too. Therefore, in order to realize the desired linear converter control characteristic, a normalized control variable σ [7] is implemented with range from 0 to 1. By this variable two parameters vary simultaneously – the angle δ and the frequency detuning ν:

$$\delta = (1 + 2\sigma)\pi / 2 \qquad (2)$$

$$\nu = \begin{cases} \nu_{\min} + \sigma(\nu_{\max} - \nu_{\min}), & \sigma \le 0{,}5 \\ \nu_{\min} + (1-\sigma)(\nu_{\max} - \nu_{\min}), & \sigma > 0{,}5 \end{cases} \qquad (3)$$

With respect to (1), expression (3) actually sets the converter operation frequency which varies from a minimum value ω_{S_min} at $v = v_{min}$ to a maximum value ω_{S_max} at $v = v_{max}$.

From fig. 3 and equation (3), it can be seen that the operating frequency maximum value is obtained at $\sigma = 0{,}5$. Therefore, the inductor current value at no-load mode will be smaller than the one set with the „classical" phase-shift control technique.

III. Circuit of the Control System

A. Control System Principle of Operation

The synthesis of the control system is hampered by the logic condition in (3). Therefore, the control is chosen to be realized separately for each operating mode. As it can be observed in fig. 2, in ***DIRECT MODE***, the "input" inverter control pulses precede those for the "output" one at an angle $\delta \leq \pi$. In ***REVERSE MODE***, the opposite is conditionally observed. The "output" inverter control pulses precede those for the "input" one at an angle $\delta' \leq \pi$.

The control system of the bidirectional resonant DC-DC converter is realized on the principle of the Analog Behavioral Modeling implemented in the PSPICE A/D simulation software [8]. In many cases, this approach allows mathematical description of circuit parts to be used instead of real components for their modeling.

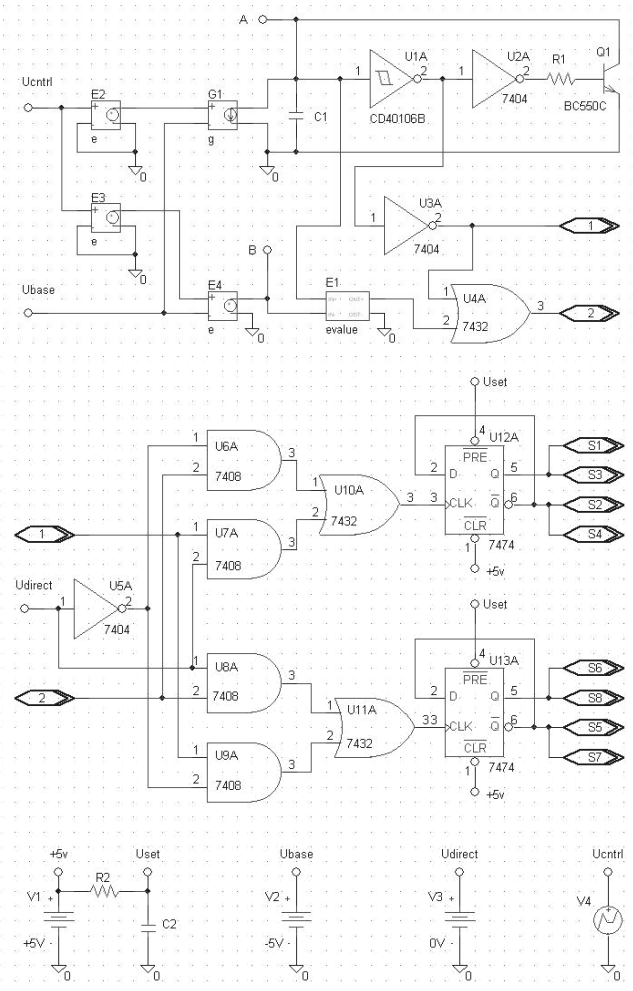

Fig. 4. Circuit of the Control System

In order to verify the proper control system operation, in the environment of OrCAD PSpice, a bidirectional series resonant DC-DC converter with power of 200W is designed according to the following data: $U_d = 100$V; $U_0 = 100$V; k = 1; $f_{S_min} = 0{,}5\omega_{S_min}/\pi = 50$kHz; $v_{min} = 1{,}15$; $v_{max} = 1{,}27178$. The resonant tank elements are determined as: L = 524,608μH; C = 25,542nF ($\rho_0 = 143{,}314\Omega$). IRF640 MOSFETs and snubber capacitors $C_1 \div C_8 = 4{,}7$nF are chosen for the inverter stages. ZVS drivers as the presented in [3] are realized.

Fig. 4 presents circuit of the control system. It consists of three main parts: a voltage controlled oscillator of two sequences of pulses (VCOSP); a logic circuit for the mode choice (LCMC); a distributor of the control pulses (DCP) to the ZVS drivers of the both inverter stages.

VCOSP is realized on the base of the linearly variable voltage generator which includes the voltage controlled current source (G1), the capacitor (C1), the Schmitt trigger (U1A), the inverting buffer (U2A) and the transistor (Q1). The frequency variation of the linearly variable voltage in point A is realized by variation of the Ucntrl voltage in the range from 0V to 5V. By the voltage Ubase = -5V, the minimum frequency is provided to be $2\omega_{S\_min}$. At Ucntrl = 5V, the frequency is set to $2\omega_{S\_max}$. The first pulse sequence is completely formed by the inverting buffer U3A.

The linearly variable voltage is compared in E1 to a constant voltage proportional to Ucntrl. After that, the logic element U4A forms the second pulse sequence which is phase-shifted from the first. In this case, by Ubase a minimum phase-shift π is set. At Ucntrl = 5V, the phase-shift is set at 2π.

It can easily be seen that the frequency and the phase-shift are proportional to the control parameter Ucntrl.

The formed by means of VCOSP two pulse sequences are submitted to LCMC. It is intended to determine which control pulses to be "leading" – the ones for the "input" or for the "output" inverter. LCMC has one logic input to which the signal Udirect is applied. It consists of only logic elements (U6A÷U11A). When the Udirect level is low, the bidirectional DC-DC converter operates in ***REVERSE MODE***. Otherwise, ***DIRECT MODE*** is present.

DCP consists of two D flip-flops (U12A, U13A) which distribute the control pulses to the ZVS drivers of the two inverters. The D flip-flops reduce the VCOSP signals frequency twice. In this way, the phase-shift is also reduced twice varying in the range from π/2 (Ucntrl = 0V) to π (Ucntrl = 5V).

Considering the above, the operating mode change is best to be done at Ucntrl = 5V, when the phase-shift angle is $\delta = \pi$.

The proposed circuit of the control system suffices expressions (2) and (3), but an additional logic signal should be used for this purpose.

B. Simulation Results

In order to verify the behavior of the bidirectional series resonant DC-DC converter control system, simulation examinations are carried out with the developed models in the environment of OrCAD PSpice. Fig. 5 presents waveforms for illustration of the control system behavior at

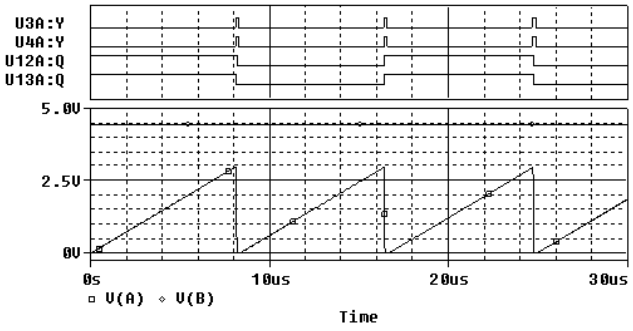

Fig. 5. The Control System Behavior at Start Mode
Ucntrl = 7,5V

start-up. This appears to be easy at a higher value of Ucntrl > 5V which does not affect the phase-shift angle ($\delta = \pi$) but additionally increases the operating frequency ($\omega_S > \omega_{S\_max}$). The converter starts up similarly to the well-known conventional series resonant DC-DC converter with uncontrolled rectifier and capacitive output filter. Actually, this is almost the same mode as the one defined at $\sigma = 0{,}5$.

Fig. 6 and fig. 7 demonstrate the control system behavior at maximum converter output current in ***DIRECT MODE*** and ***REVERSE MODE*** respectively. In this case, only

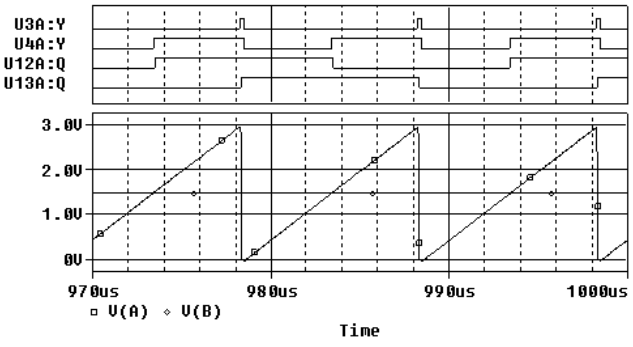

Fig. 6. The Control System Behavior at ***DIRECT MODE***
Ucntrl = 5V ($\sigma = 0$)

visible is the difference in the output pulses of the D-flip-flops (U12A и U13A) which show the direction of phase-shift.

By the simulation examinations, the behavior of the bidirectional converter using the proposed control technique is evaluated. Fig. 8 presents a control characteristic (with thick line) obtained as a result of the theoretical analysis. The simulation results obtained at different values of the control parameter are marked with

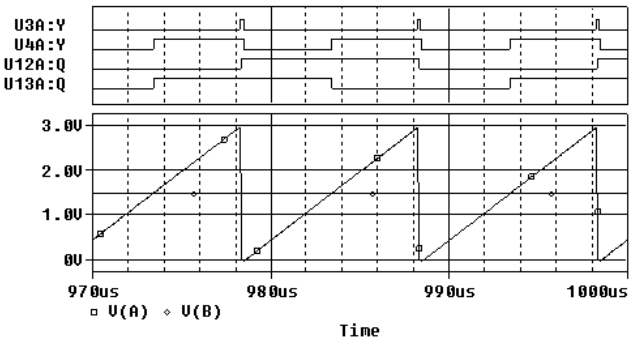

Fig. 7. The Control System Behavior at ***REVERSE MODE***
Ucntrl = 5V ($\sigma = 1$)

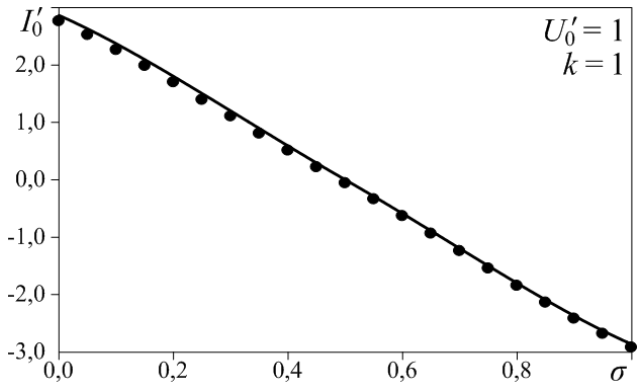

Fig. 8. Comparison between theoretical and simulation results

dots. Fig. 8 shows a good matching between the theoretical and the simulation results.

IV. Conclusion

A technique for control of bidirectional series resonant DC-DC converter operating above the resonant frequency is presented. The classical phase-shift control technique is proposed to be combined with a proportional variation of the operating frequency. This solution allows linearization of the control characteristics.

By means of computer simulations this new control technique has been examined. The research has shown a very good matching between the theoretical and the simulation results.

The obtained results can be used to design a system for control of bidirectional series resonant DC-DC converters.

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Analysis and Design of Quasi-Resonant ZVS Inverter for Induction Heating in a Magnetic Circuit

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Abstract –**This paper presents a ZVS quasi-resonant inverter for induction heating in a magnetic circuit. A mathematical modeling of induction coil - heated metal piece system has been done to establish the equivalent electrical parameters of the load. Analysis and design of a quasi-resonant inverter have been presented along with experimental examinations at different loads.**

Keywords – **quasi-resonant inverter, zero voltage switching, induction heating, induction coil**

I. INTRODUCTION

Induction heating in a magnetic circuit has been increasingly used, especially in heating small pieces or foils in low power portable units up to 1kW. Due to the relatively low power of those units and the high efficiency and reliability requirements of the power supply, it is extremely convenient to use single switch quasi-resonant /QR/ inverters operating at ZVS. They have been widely applied in modern induction cooktops (induction hobs) where they supply flat induction coil with magnetic core [3]. Their use for induction heating in a magnetic circuit has to do with load coordination, hence designing them to maintain the favorable operating modes when changing the load.
The aim of the present paper is to present an adequate model of an induction coil - heated metal piece system in magnetic circuit induction heating, the purpose being the optimal design of a single switch QR ZVS inverter.

A. "Induction coil – heated metal piece" system in magnetic circuit heating.

The induction coil – heated metal piece system is shown in fig.1. Unlike the conventional induction coil-heated metal piece system, for example in heating cylindrical pieces, schematically shown in fig. 2, where the work-piece is placed in the magnetic field of a low resistance inductor with few windings, in magnetic circuit heating the load is placed in the air gap of a magnetic core, the magnetic flux being created by a number of turns. This excludes the bobbin effect and the proximity effect and to some extend the fringing. Thus by considering only the electromagnetic induction and the skin effect in induction heating the system is simplified. Such configuration of the "induction coil-heated metal piece" system has not been considered in classical literary sources [1], [5], [6]. Similar to that system is the induction heating in induction coil-transformer, presented in [5], however there is low resistance inductor at high power and low frequencies.

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Fig. 1. Induction coil for heating in a magnetic circuit.

1- magnetic core, 2-induction coil, 3- heated metal foil.

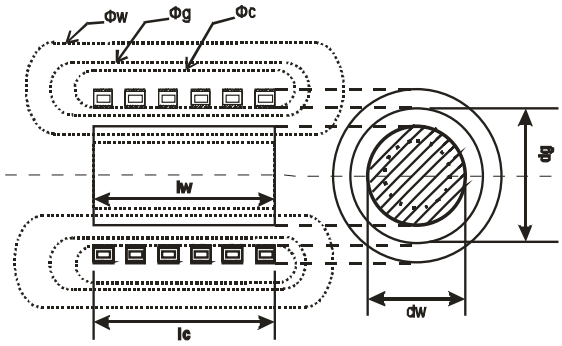


Fig. 2. Magnetic fields of "induction coil – heated metal piece" system in cylindrical piece induction heating.

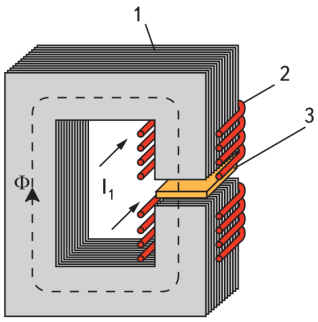


Fig. 3. Magnetic fields of the "induction coil – heated metal piece" system in magnetic circuit induction heating.

1- magnetic core, 2-induction coil, 3- heated metal foil.

To analyze the "induction coil – heated metal piece" system in a magnetic circuit heating the method of the magnetic flux equivalent circuit is used [2], [6].

The magnetic flux of the induction coil has three components: ϕ_w – magnetic flux that closes across the piece; ϕ_g – magnetic flux across the air gap; ϕ_c – magnetic flux across the surface of the induction coil: $\phi_0 = \phi_w + \phi_g + \phi_c$

$$\phi_0 = \mu_0 H_s \left[\left(A_g + \mu_r q A_w + k_r \frac{\delta_c \pi d_g}{2} \right) - j \left(\mu_r p A_w + k_r \frac{\delta_c \pi d_g}{2} \right) \right] \quad (1)$$

where $A_W \ (m^2)$ - the piece cross-section, k_r is a correlation coefficient and depends on the magnetic flux between the induction coil turns, δ_c - skin depth of the induction coil, A_g - the cross-section of the air gap area , l_C – induction coil length, D_c – induction coil diameter.

With short induction coils, i.e. $l_w/d_w<5$ in fig.2, k_r can be found from $k_r = \frac{2,3}{2,3 + d_w/l_w}$.

The values of the coefficients p and q are determined according to the solutions of the differential equations for the electromagnetic field and are as follows:

$$p = \frac{\sqrt{2}\Delta}{R} \cdot \frac{ber\sqrt{(2)}R/\Delta . ber'\sqrt{(2)}R/\Delta + bei\sqrt{(2)}R/\Delta . bei'\sqrt{(2)}R/\Delta}{ber^2\sqrt{(2)}R/\Delta + bei^2\sqrt{(2)}R/\Delta} \quad (2)$$

$$q = \frac{\sqrt{2}\Delta}{R} \frac{ber\sqrt{(2)}R/\Delta . bei'\sqrt{(2)}R/\Delta + bei\sqrt{(2)}R/\Delta . ber'\sqrt{(2)}R/\Delta}{ber^2\sqrt{(2)}R/\Delta + bei^2\sqrt{(2)}R/\Delta} \quad (3)$$

Bessel functions are as follows:

$$berx = 1 - \frac{(x/2)^4}{2!^2} + \frac{(x/2)^8}{2!^4} - \frac{(x/2)^{16}}{2!^8} + \ldots$$

$$beix = \left(\frac{x}{2}\right)^2 - \frac{(x/2)^6}{3!^2} + \frac{(x/2)^{10}}{5!^2} - \frac{(x/2)^{14}}{7!^2} + \ldots \quad (4)$$

The magnetic field strength across the surface becomes:

$$H_s = \frac{I_c N_c}{l_c}, \quad (5)$$

where Nc – number of induction coil turns, Ic – current across the induction coil, lc – induction coil length, $l_c = \pi.(D_1 - D_2)$.

Taking into account the change of the work piece parameters the model of the "induction coil – heated metal piece" system is reduced to 5 passive elements shown in Fig. 4. [2].

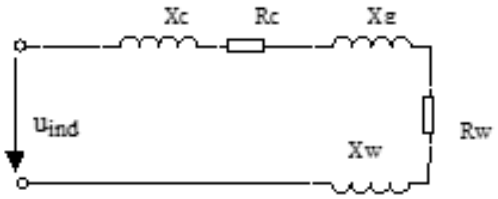


Fig. 4. Equivalent circuit of the load in induction heating in a magnetic circuit

In Fig. 4 the resistance R_W is the equivalent resistance of the work piece and it is proportional to parameter p;

$$R_w = \frac{2\pi f \mu_0 N_c^2}{l_c} \mu_r p A_w \quad (6)$$

R_C is the equivalent resistance of the inductor coil;

$$R_c = \frac{2\pi f \mu_0 N_c^2}{l_c} k_r \frac{\Delta_c \pi D c}{2} \quad (7)$$

X_W is the equivalent inductive reactance of the work piece and it is proportional to parameter q;

$$X_w = j \frac{2\pi f \mu_0 N_c^2}{l_c} \mu_r q A_w \quad (8)$$

X_g is the inductive reactance of the air gap;

$$X_g = j \frac{2\pi f \mu_0 N_c^2}{l_c} A_g \quad (9)$$

X_C is the internal inductive reactance of the inductor.,

$$X_c = j \frac{2\pi f \mu_0 N_c^2}{l_c} k_r \frac{\Delta_c \pi D c}{2} \quad (10)$$

where f is the operating frequency, and $\mu_0=4.\pi.10^{-7}$- magnetic constant.

The power that is released in the work piece is as follows:

$$P_w = \pi . \frac{(D1 - D2)^2}{4} . H_s^2 \mu_0 \mu_r . f . p \quad (11)$$

It can be seen that the equivalent parameters of the inductor - piece system depend both on the geometrical dimensions, and on the magnetic permeability μ_0 and the internal resistance ρ of the piece being heated, which are largely dependent on temperature [3]. To calculate their values at different heating temperatures these dependences should be presented by the analytical expressions:

$$\mu_r = 1 + \frac{\alpha . H_s^{\beta} - 1}{(1 + (\frac{T}{T_k - T})^{\chi})^{\delta}} \quad (12)$$

where $\alpha=3.10^5$, H_S – magnetic field strength, β= -0,85, χ=1,9, δ=0,16. For temperatures above Curie temperature – $T_к$, the magnetic permeability of carbon steels becomes μ=1. The work piece internal resistance depends on the metal temperature coefficient α_T and is obtained from the relationship:

$$\rho(T) = \rho_0 . [1 + \alpha_T . (T - T_0)] \quad (13)$$

where for steel α_T=0.005 1/°C

Internal resistance ρ, relative permeability μ_r, penetration depth δ and the surface resistance ρ_s of the most commonly used cookware materials in the household are shown in table 1

TABLE 1 MATERIAL PARAMETERS

Metal parameters					
Material	**ρ, (10^{-6} Ω.mm)**	**μ_r**	**δ, mm**	**ρ_s, (10^{-3} Ω/mm²)**	**Against copper**
Carbon steel	0,13-1,25	200	1,5	2,25	56,25
Aluminum	0,027	1	0,48	0,051	1,28
Copper	0,018	1	0,39	0,04	1

Calculations for the equivalent parameters of the "induction coil – heated metal piece" system in heating in a magnetic circuit have been made based on formulae (1)-(13), the load is the foil from the respective metal in table 1. Calculations for multi-winding litz wire induction coil of external diameter D1=82 mm, internal diameter D2=45mm and 20 windings have been made. A coated magnetic ferrite toroidal core produced by Kaschke company has been used. The type is R80/40/15 L and the material is K4000 . The results from the calculations are systemized in table 2.

However, there is a striking difference between ferromagnetic and nonmagnetic materials. The operating frequency is selected to be in the range of 35-40 kHz. If the same power is to be obtained by heating with a conventional inductor it is necessary to increase the frequency up to about 2,5-3 MHz, which is technically too complex and economically unjustified. It is the heating of thin layers or small pieces at frequencies in the middle range of induction heating that is the main advantage of induction heating in a magnetic circuit.

TABLE 2. RESULTS OF CALCULATIONS.

Basic parameters of "induction coil-hated metal piece" system					
Material	**Rw, Ω**	**Rc, Ω**	**Xw, Ω**	**Xc, Ω**	**Xg, Ω**
Carbon steel	0,835	62,9u	1,2	19,8m	10m
Aluminum	0,004	62,9u	0,006	19,8m	10m
Copper	0,004	62,9u	0,006	19,8m	10m

Material	**Re, Ω**	**Le, Hr**	**Uc,V**	**Ic, A**	**Pw,W**
Carbon steel	0,835	7,75u	1205	-	300
Aluminum	4,24m	0,1u	1102	-	140
Copper	4,24m	0,1u	1150	-	230

B. Quasi resonant ZVS inverter for induction heating in a magnetic circuit:

In the quasi resonant circuit there is one transistor that takes up little space on the circuit board and is easier to cool. In addition, it is possible to use a simpler control scheme. The main disadvantage of the circuit is the presence of a higher voltage than the supply voltage in the resonant circuit, which requires the use of more expensive higher voltage transistors.

The power circuit consists of an input uncontrolled rectifier with capacitive filter /Graetz circuit/ and a quasi-resonant inverter shown in fig.5. The key part in the inverter consists of an IGBT (Insulated Gate Bipolar Transistor) and a diode connected in counter-parallel. The transistor is ON when the diode is in a conductive state thus providing resonant switching of the transistor at zero current and zero voltage - ZCS и ZVS. Resonant oscillating circuit consists of a resonant inductance (Li) and a resonant capacitance (C_2).

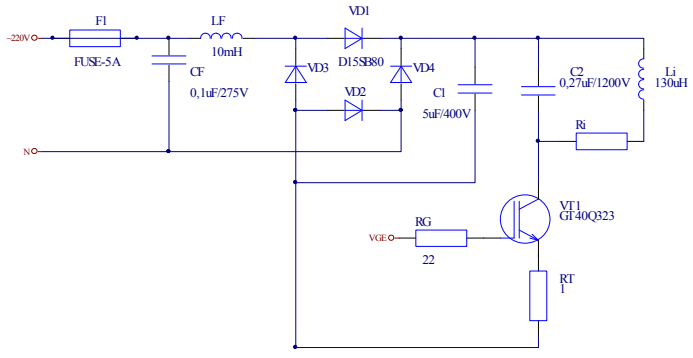
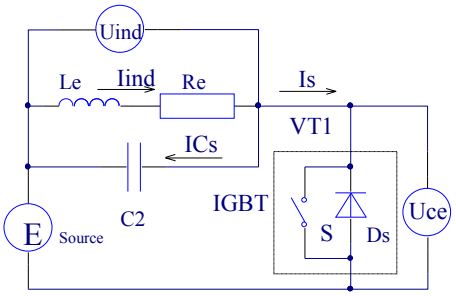


Fig. 5 Power circuit of a single switch QR inverter for induction heating in a magnetic circuit.

The operation of the circuit is as follows: when Ds connected to the S switch is in a conductive state the control system sends an impulse that triggers the transistor on at zero voltage Uce [5]. "Induction coil – heated metal piece" system is represented by the elements connected in series Re= R_C+ R_W and the reactive Le= L_W+ L_c+ L_g. In this inverter circuit the transistor must withstand the high voltage Uce voltage oscillation due to oscillation of the oscillating circuit.



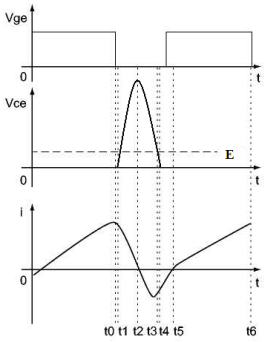
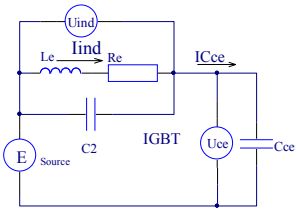
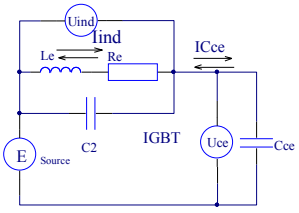


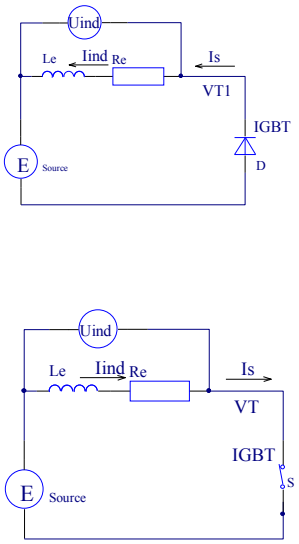
Fig.6 Equivalent circuit and working time-diagrams of QR ZVS inverter

Fig. 6 shows the time diagrams of operation of all elements of the inverter circuit. Initially S1 is blocked by the control circuit when the current flowing through Le reaches its maximum value and starts to decrease. At this point the voltage of the collector of the transistor is Vce (0)=0V. There are four operating modes shown in fig. 4.





Mode I Mode II



Mode III Mode IV

Fig.7 Operating modes of a quasi-resonant ZVS inverter

MODE I:t0-t1

As mentioned earlier the switch is switched off once the current in the resonant circuit reaches the maximum, i.e. at the point t0. This switch-off process results in switching losses, the magnitude of which depends on the switch off time of the transistor. Uce voltage rises sharply by exponent which is determined by the value of the capacitance (C2) until DC voltage of the mains power supply (E) at the moment t1 is reached.

Despite of the fact that the transistor switches off at t0, the current continues to increase to t1 when the Uce voltage becomes equal to E, i.e. the DC voltage was greater than the resonant voltage of the circuit. At this point the energy that is stored in the inductor starts to transfer to the capacitor.

MODE II:t1-t4

Since E is less than Uce after t1, the current decreases to zero at t2, when the resonant voltage reaches its maximum. This is the point where the transfer of the energy stored in the inductor to the capacitor of the circuit ends. The maximum value of the resonant voltage of the circuit is directly related to the switch-on time of the switch (IV: t5-t6).

After t2 the capacitor starts to discharge supplying the inductor with energy which determines the current-voltage inversion as the current reaches a minimum value at t3, i.e. Uce=E. After t3 the resonant current increases as Uce<E and the capacitor discharge ends at t4.

MODE III: t4-t5

After t4 the energy from the capacitor and stored in the inductor is recuperated to the DC supply since the diode D1 is on. The resonant current flows through the diode D1 until the switch S1 is switched on.

MODE IV: t5-t6

The control circuit sends a signal to switch the transistor on. The transistor switches on as the current flows through its reverse parallel diode D1. After the transistor is switched on the current starts to change its direction and the inductor starts to store energy, which enables the transistor to switch on at zero voltage. The voltage across the transistor is the voltage drop of the switched on diode D1 at the point of switching on, i.e. we have zero voltage switching ZVS. At t6 the switch is switched off as the process is repeated with the start of mode I. Since the maximum value of the resonant voltage depends on the frequency of operation and the fill factor of the switch, the output energy is very easy to control, i.e. to regulate the output power. It should be noted that the voltage wave form changes with the mains supply voltage variations as well as with the load impedance changes.

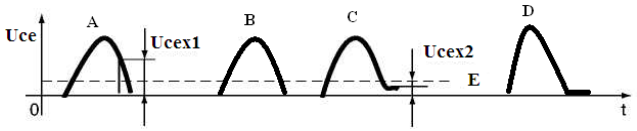


Fig.8 Transistor voltage wave forms

DC voltage (E) is pulsating and alternates from zero to maximum of the mains voltage because filtering capacitor with relatively low capacitance is used to achieve a satisfactory quality factor of the mains power supply. The waveform of the resonant voltage is divided into three types shown in fig. 8.

In this fig. A, B, C and D are time diagrams of the voltage at earlier (рано отпушване) switching on of the transistor, normal load, low load or idle mode and at delayed (късно отпушване) switching on of the transistor. If the form of C is obtained at proper inverter operation it means that the values of the induction coil inductance or the values of the capacitance of the compensating circuit capacitor are not correctly selected. When the voltage is in the form of A or D at normal operation the switching-off time of the transistor must be set, respectively the frequency of the control pulses.

When the switch is switched on enough energy must be stored in the inductor. Otherwise the voltage wave form will appear as if the load is insufficient. In this situation the resonant voltage will not reach zero value (Ucex2), thus the mode of free oscillation will be eliminated III (t4-t5) and the switch will not be switched on at zero voltage.

The energy stored/accumulated in the capacitor will be lost. The switch will take it over when it is switched on:

$$W = \frac{1}{2}.C_2.U^2_{cex2}.f_s \qquad (12)$$

C. Inverter operation analysis:

To simplify the analysis of the electromagnetic processes we will assume that the inverter has only two equivalent circuits - when the transistor is turned either on or off. The proposed methodology for analysis in [1] can be used as a combination of a fitting method and harmonic analysis. For the first-half period of switched on position t5-t6 we have:

$$i_s = \frac{E}{R_e}.\left(1 - e^{-\tau.t}\right) + I_{Le2}.e^{-\tau.t}, \qquad (13)$$

where $\tau = \frac{R_e}{L_e}$ is time constant of the oscillating circuit. The voltage of the transistor is determined by the voltage drop Uce_{sat} which is dependent on the current and is taken from the catalogue data. The next half-period starts with the transistor switching off t0-t4. The current through the load is determined by the accumulated energy in the previous half-period:

$$i_{Le} = \frac{\omega_0}{\omega}.\left(e^{-\alpha.t}\right).\left[\begin{array}{l}\left(E - U_{Cce}\right).\sqrt{\left(\frac{C_{ce}}{Le}\right)}.\sin\left(\omega.t\right) + \\ I_{Le}.\cos\left(\omega.t + \vartheta\right)\end{array}\right] \quad (14)$$

The voltage across the transistor will be:

$$U_{Ce}(t) = E + \frac{\omega_0}{\omega}.\left(e^{-\alpha.t}\right).\left[\begin{array}{l}\left(U_{Cce} - E\right).\cos\left(\omega.t - \vartheta\right) + \\ I_{Le1}.\sqrt{\frac{L_e}{C_{ce}}}.\sin\left(\omega.t\right)\end{array}\right] \quad (15)$$

where $\alpha = \frac{R_e}{2.L_e}$, $\omega_0 = \sqrt{L_e.C_e}$ and $\vartheta = arctg\left(\frac{\alpha}{\omega}\right)$

The power in the load will be determined by:

$$P_0(t) = f.E\int_{t5}^{t6} i_{Le}dt, \quad (16)$$

The results obtained from calculating of the electrical parameters of a quasi-resonant ZVS inverter for heating in a magnetic circuit of metal foils of different materials are summarized in table 3.

TABLE 3. ELECTRICAL PARAMETERS FROM CALCULATION.

Load	I_{DC}, A	I_{Le} , A	U_{Ce}, V	f, kHz	P_{DC}, W
-	0,16	0,4	873,7	35	66
Cu foil	0,16	0,5	1202,4	35	72,6
	0,67	0,5	1306,2	35	231
Al foil	0,3	0,4	1219,7	35	99
	0,34	0,5	1366,7	35	132
Fe foil	0,94	0,4	1202,4	35	330

D. Experimental results:

Presented below are the oscillograms of the operation of the equipment for induction heating in a magnetic circuit for different loads.

1. Transistor gate controlling impulse (ch1), transistor's collector voltage (ch2) and current through the power circuit (ch3) when heating foil, respectively of copper (0,02 and 0,2 mm thickness) (fig.9 a, b), aluminum (0,1 and 2,1 mm thickness) (fig.9 c, d) and steel (0,9 mm thickness) (fig.9 e). The oscillogram shows that the transistor switches on when the voltage after the circuit drops to zero, i.e. soft switching is realized correctly. The form of the resulting oscillogram is not different from the theoretical one.

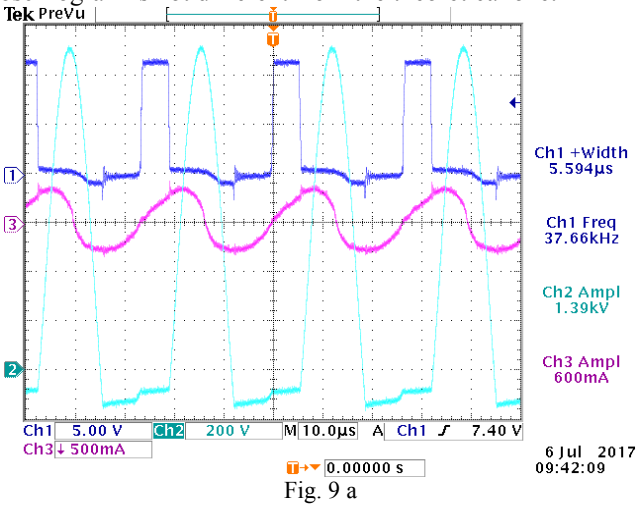


Fig. 9 a

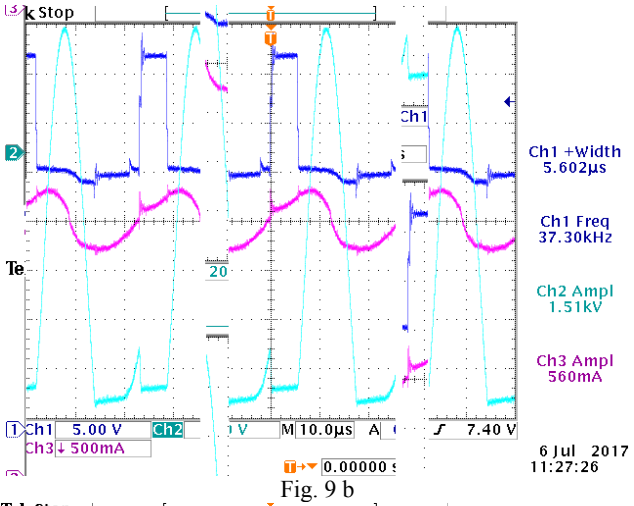


Fig. 9 b

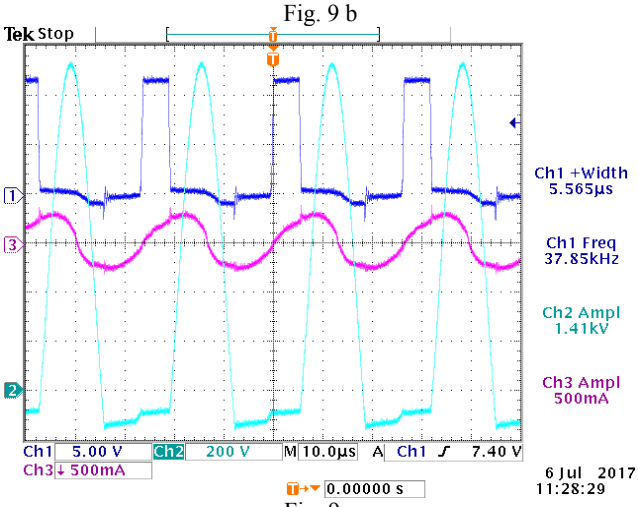


Fig. 9 c

It can be seen that the voltage of the transistor resulting from the calculations and the experimental studies differs within 50-60V, i.e. 6,7%. As far as the current through the transistor is concerned a significant error is observed, which may be due to an error resulting from the measurement with a HAMEG AC/DC Current Clamps HZ56-2 connected to the drain of the BUP314 transistor.

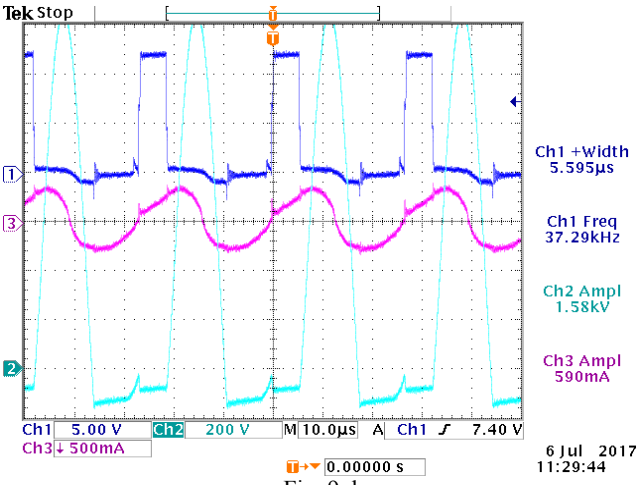


Fig. 9 d

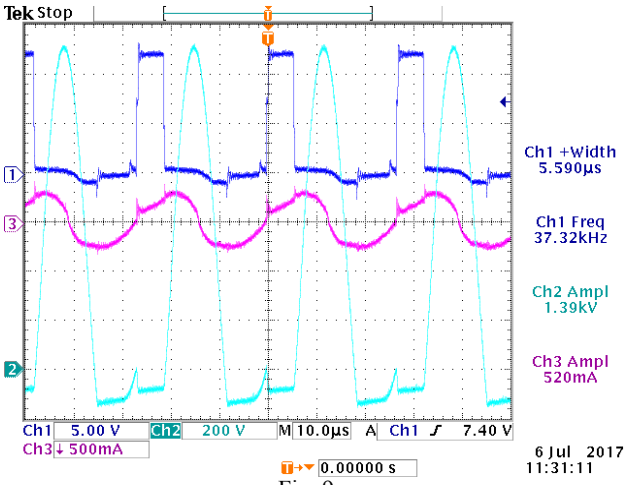


Fig. 9 e

2. Voltage and current in the resonant circuit.

The oscillogram shows the waveform of the voltage and current in the resonant circuit when heating foil, respectively of copper (0,02 and 0,2 mm thickness) (fig.10 a, b), aluminum (0,1 and 2,1 mm thickness) (fig.10 c, d) and steel (0,9 mm thickness) (fig.10 e).

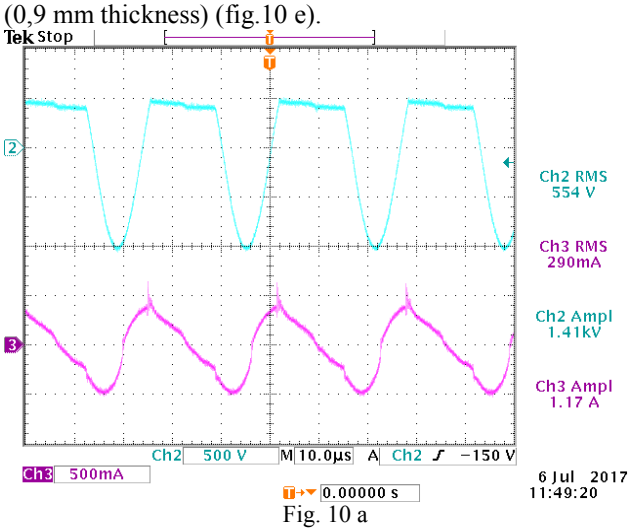


Fig. 10 a

When the transistor is off the voltage changes direction and the current flows through the reverse diode of the transistor. The peak value of the voltage is 1410 V but the first harmonic effective value is around 1000 V, which is close to the calculated value of 965 V.

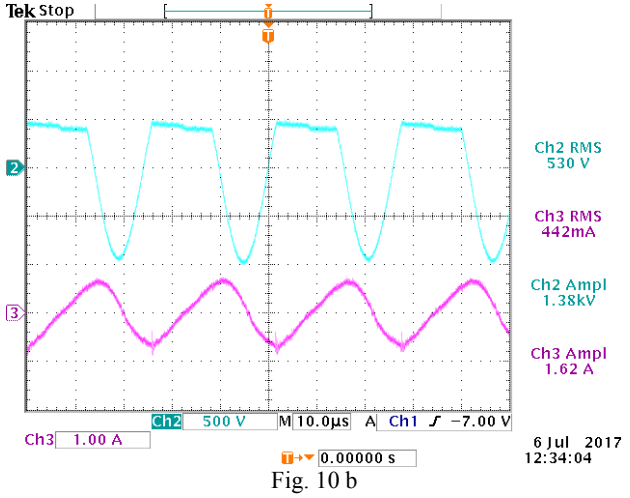


Fig. 10 b

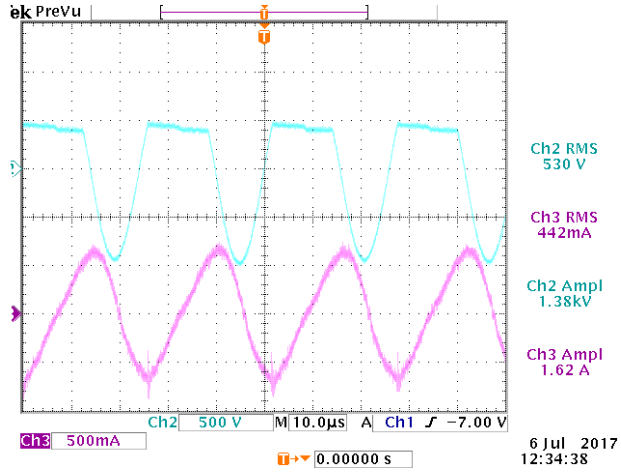


Fig. 10 c

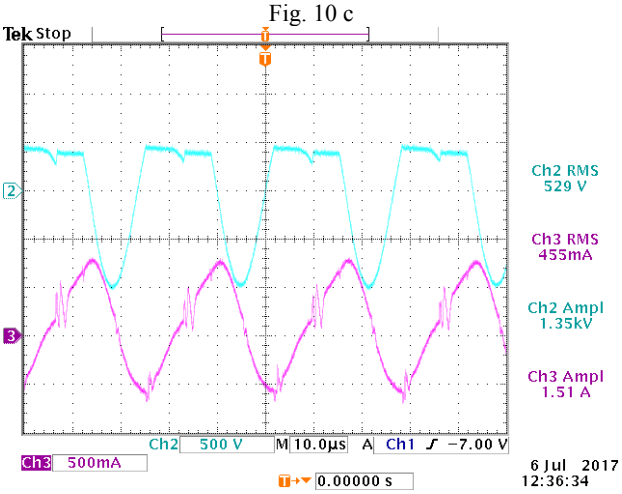


Fig. 10 d

TABLE 4. EXPERIMENTAL ELECTRICAL PARAMETERS.

Load	I~, A	I_{DC}, A	It , A	Ut, V	f, kHz	P_{DC}, W
-	0,53	0,16	0,48	1010	37,70	52,8
Cu foil	0,61	0,17	0,6	1390	37,66	56,1
	3,5	0,67	0,56	1510	37,3	221,1
Al foil	0,96	0,3	0,5	1410	37,85	99
	1,7	0,34	0,59	1580	37,29	112,2
Fe foil	2,7	0,94	0,52	1390	37,32	310,2

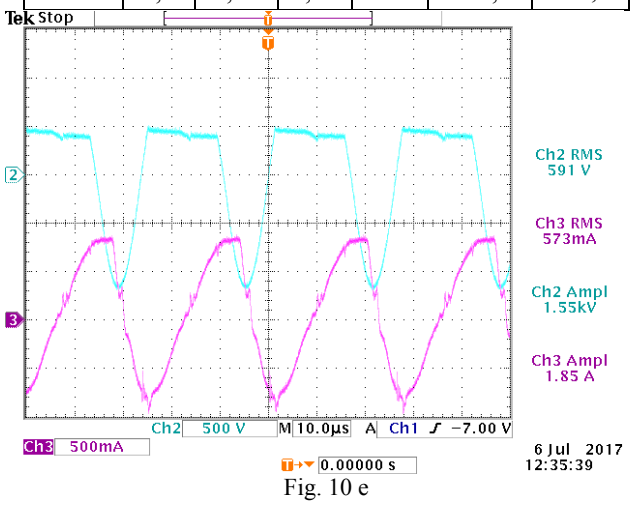


Fig. 10 e

The results from the measurements made in the experimental study of the system for heating in a magnetic circuit are summarized in table 4.

D. Conclusion:

The following conclusions can be drawn based on this experimental study:

- The methods for analysis of the "induction coil-heated metal piece" system for induction heating in a magnetic circuit proposed in this paper provide a good basis for further development. This is evident from the experiments done and the recorded time diagrams which show similarity to the theoretically described QR inverter circuits. The modeling and experimental verification done in this work have proven the correctness of the chosen model and they have also proved to be very useful in understanding the electromagnetic processes.

- Along with the advantages of the quasi inverter conductor used, such as high switching losses and simplicity , it can be further optimized by using SIC transistors, for instance.

- The proposed systems for induction heating in a magnetic circuit can be widely used in soldering printed circuit boards, or different types of foils, in heating metal sheets in car repair shops or heating non-ferromagnetic utensils in induction cooking.

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Modeling of Electronic Energy Converter for Induction Heating Using LabVIEW

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Abstract – **The aim of this paper to present the modeling of electronic energy converter in the popular development system LabVIEW. Using the various extensions and hardware capabilities it allows an intuitive, easy and comfortable way to examine, study and prototype these kind of devices. For example is reviewed an induction heating energy converter – parallel current source thyristor inverter. In the formalization and analysis of the power circuit are used interconnected parameters with which are described the behavior and operating regimes. The model is verified using the specialized simulation software LTSpice® and data taken from real electrothermic plants for induction heating.**

Keywords – **Modeling, Induction Heating, LabVIEW, Electromagnetic Processes, Design**

I. Introduction

Induction heating is one of the classical technologies in the industrial production – for example the plants for melting of ferrous and nonferrous metals. The advantages of the technology are well known as in [1, 2], such as operation with high energy-efficient indicators, the reach of high quality production because of ability to operate in inert gases or vacuum environments, good dynamics of the heating process and last but not least clean processes, which do not affect worker safety and environment threat. The development of the semiconductor switches made this technology readily available also for domestic appliances such induction hot-plates and boilers.

The aim of this paper is the creation of a current-source parallel thyristor inverter model in the visual programming development system LabVIEW.

II. Converter Description

The examined power circuit is shown on Fig. 1. It is composed of four thyristors (*VS1* ÷ *VS4*) which form an inverter bridge. The input is connected with a direct current (DC) supply block U_d in series with input inductor L_d – together forming a current source. To the output of the bridge is connected a parallel resonant circuit. It is composed from a compensating capacitor *C* and active-inductive load (*L*–*R*), representing the system inductor – heated body. For the analysis and examination will be used the following close to reality assumptions:

- Active energy is consumed only from the resistance *R* in the load circuit.
- The thyristors are replaced with ideal switches. There is no energy loss in the other circuit elements.
- The supplying DC voltage source has zero internal resistance.
- The commutation of the current from thyristor to thyristor is instantaneous. The inductance in the commutation circuit is neglected.

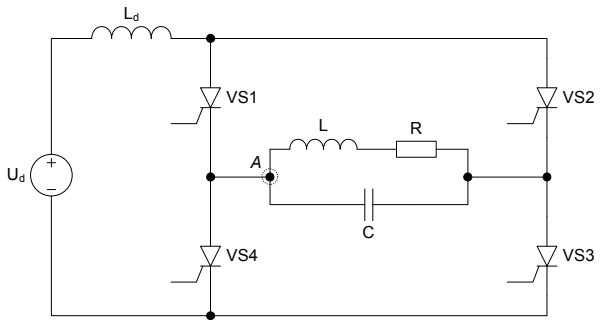

Fig. 1. Parallel current source inverter. One of the widely used power circuits for induction melting of metals.

III. Mathematical Model of the Inverter

For the creation of the model are used in conjunction the methods of the instantaneous values, switching functions and the state variables [3, 4]. From the circuit operation is known that in transient and steady state operation there are two discrete commutation intervals. The first is when thyristors *VS1* and *VS3* are conducting, assuming that these are the uneven half periods of the circuit operation. The second interval is when the other pair of thyristors are conducting (*VS2* and *VS4*) which are the even half periods.

A. Analysis of the electromagnetical processes in the circuit

Using the circuit from figure 1 and the laws of electricity a system of ordinary differential equations (ODEs) is composed, which describe the relationship between the currents and voltages of the reactive elements. The accepted positive signs for the state variables correspond to the uneven half periods.

When one of the diagonal of the inverter bridge is conducting (for example *VS1* and *VS3*), the balance of the currents using first Kirchhoff law for net *A* is described by the equation:

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$$i_C = C\frac{du_C}{dt} = i_d - i_L \quad (1)$$

The voltage balance according the second Kirchhoff law for the closed circuit $U_d - L_d - VS1 - u - VS3 - U_d$ is given by the equation:

$$U_d = L_d\frac{di_d}{dt} + u_C \quad (2)$$

For the closed circuit $C - R - L$ the relation is:

$$u_C = Ri_L + L\frac{di_L}{dt} \quad (3)$$

These equations are combined together in a system of linear ODEs:

$$\begin{cases} \dfrac{du_C}{dt} = \dfrac{1}{C}\left(i_d - i_L\right) \\ \dfrac{di_d}{dt} = \dfrac{1}{L_d}\left(u_C + U_d\right) \\ \dfrac{di_L}{dt} = \dfrac{1}{L}\left(u_C - Ri_L\right) \end{cases} \quad (4)$$

When the other diagonal of the inverter bridge is conducting (*VS2* and *VS4*), the equation's members are the same, only the signs of the input current i_d in equation (1) and the voltage over the capacitor u_C in (2) change.

B. Generalization of the system of equations

The changes of signs in the equations are affected by the operational principle because when the circuit is working the inverted current is changing its direction in the output diagonal of the bridge, where the load circuit is connected. According to the method of the momentary values the state variables must be pieced together at the moments of commutation of the semiconductor power switching elements. This designates that the calculated values of the state variables produced in the end of the half period from the circuit operation are involved as the initial conditions for the next half period. In order to do a generalized description of the workings of the circuit in the individual half periods a switching function should be defined, having the following form [3]:

$$F(\omega t) = (-1)^{J+1} \quad (5)$$

where J is the number of the half period – during the uneven half periods, when the first diagonal is conducting, the value is +1 and during the even, when the other is conducting, the value is –1. Then the system of equations (4) can be written in the following generalized way:

$$\begin{cases} \dfrac{du_C}{dt} = \dfrac{1}{C}\left(F(\omega t)\cdot i_d - i_L\right) \\ \dfrac{di_d}{dt} = \dfrac{1}{L_d}\left(-F(\omega t)\cdot u_C + U_d\right) \\ \dfrac{di_L}{dt} = \dfrac{1}{L}\left(u - Ri_L\right) \end{cases} \quad (6)$$

For the model verification will be used the following circuit parameters of a plant device for induction heating type "PT160", production of factory "Industrial electronics" – Gabrovo. It is composed of currents source inverter with output power of 160 kilowatts and nominal operational frequency f_{sw} = 2400 Hz, designed using the method of the first harmonic approximation (FHA), given in literature source [4]. The values of the elements in hot regime (after passing the Curie temperature) are [1, 2]:

- Capacitor capacitance C = 204,8 μF
- Load inductor L = 23.2 μH
- Load resistance R = 35.2 mΩ

The power supply of the inverter is from a three-phase controlled rectifier with a maximum output voltage U_d = 500V. Using specified by design inverter current pulsation coefficient K_I = 5% the input inductance has a value of L_d = 1.39 mH.

IV. BUILDING A MODEL IN LABVIEW

The development software platform LabVIEW is quite popular among the engineering society. The main advantage is the presence of a graphical programming environment, which allows engineers without deep knowledge of programming to work with it. Other distinctive features includes options for real world hardware interaction – simplified measurement and outputting of electrical signals, including the ability for automated measurements, data acquisition, analysis and processing [5 ÷ 11]. In this regard the time for development and evaluation of prototypes is considerably reduced. In the field of power electronics the risks which should be consider in the development cycle of a new device are diverse. Considering safety these are devices which operate with high power, dangerous for the human health voltages and high currents, so any omission in the protection and regulation systems can cause vast damage. In regard to the construction elements and components which the devices are built from – usually they are specific and custom designed for each given plant. This involves very high financial prime cost of the end product and every unreasonable decision or unpredicted fault can lead to significant economical losses. These types of devices do not tolerate evaluation and experience gathering using the "trial and error" method. Thus with such a development environment can be reviewed and simulated safely different configuration variants, including specific parameter optimizations. Using the built-in functionalities of the software platform the development time is significantly reduced and the whole process from development to prototyping of power electronic devices is greatly simplified. Other aspect of the considered platform for visual programming, quite popular in the academic community, is its widespread usage for education and conduction of remote measurements in various fields of the industry [12 ÷ 18].

In the development system LabVIEW the design consist of two stages – creation of a block diagram which in practice is the visual programming and description of the operating algorithm of the studied device; and the creation of a front panel which could be use to set up parameters and data, and

to observe the results with different elements of the visualization palette.

A. Creating block diagram from mathematical model

To create the block diagram of the examined device the "functions palette" is used. During the long history of the software (since 1986) the engineers from National Instruments have developed large number of functional blocks that could be used to solve specific problem in various different ways. In this paper will be used one relatively easy and fast way to construct a mathematical model, using the „Control Design and Simulation" palette [5, 19].

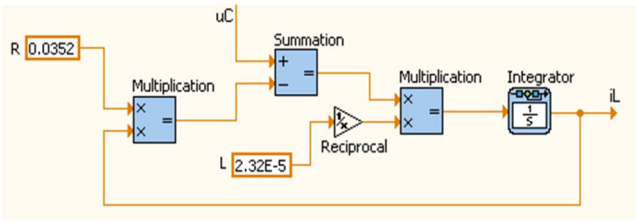

Fig. 2. Block diagram of the equation for the load inductor current (3). The equation is written in integral form, as it can be denoted by the mathematical block labels.

The creation of each block diagram from this palette begins with the „Control & Simulation loop" loop-frame, in which the other blocks are positioned. The main options of the simulation frame are the Simulation time – initial and end; Integration method – options to choose from Runge-Kutta, Adams-Moulton, Rosenbrock etc.; Options to set up the Time Step and the Absolute and Relative tolerances.

The other blocks from the "Simulation palette" such as mathematical, logical and functional are allowed to be placed only in this "ground" frame, because they share the same Simulation time and Time step. To describe the mathematical model of the device, the differential equations must be represented with these blocks. This could be achieved in several ways, but in this paper we will represent them in integral form. On figure 2 is shown for example the block diagram of equation (3), which is the equation for the inductor current iL. It is composed from two summations and one for subtraction, division and integration.

By analogy the system of linear ODEs (6) is constructed. The whole model is built by tracing the logical links between the individual blocks. On figure 3 is shown the block diagram of the model of the parallel current source inverter. The switching function is represented using block „Pulse Signal", which is set up with Amplitude 2, DC offset –1 – the goal is to produce values [+1, –1]. The oscillation period is set up externally from the front panel as the reciprocal value of the frequency. For the synthesis of the waveform a „Simulation Time Waveform" block is used, which functionality is to collect and sort the values of the simulation time with those of the state variables. Its usage is necessary from the specifics of the computational process – the time step can be split, it can be variable in order to increase the accuracy etc. At the end the output is a sorted two-dimensional array, suitable for waveform indicator on the front panel.

The front panel is shown on figure 4a. Knobs for setting the values of the operational frequency and DC supply source voltage are provided, with which the operational regime of the inverter is modified. Measurement indicators are available for reading the values of the state variables. Also there are additional digital indicators, which can be used to trace the momentary circuit commutated turn-off time of the thyristors and the maximum value of the voltage over the switching semiconductor devices.

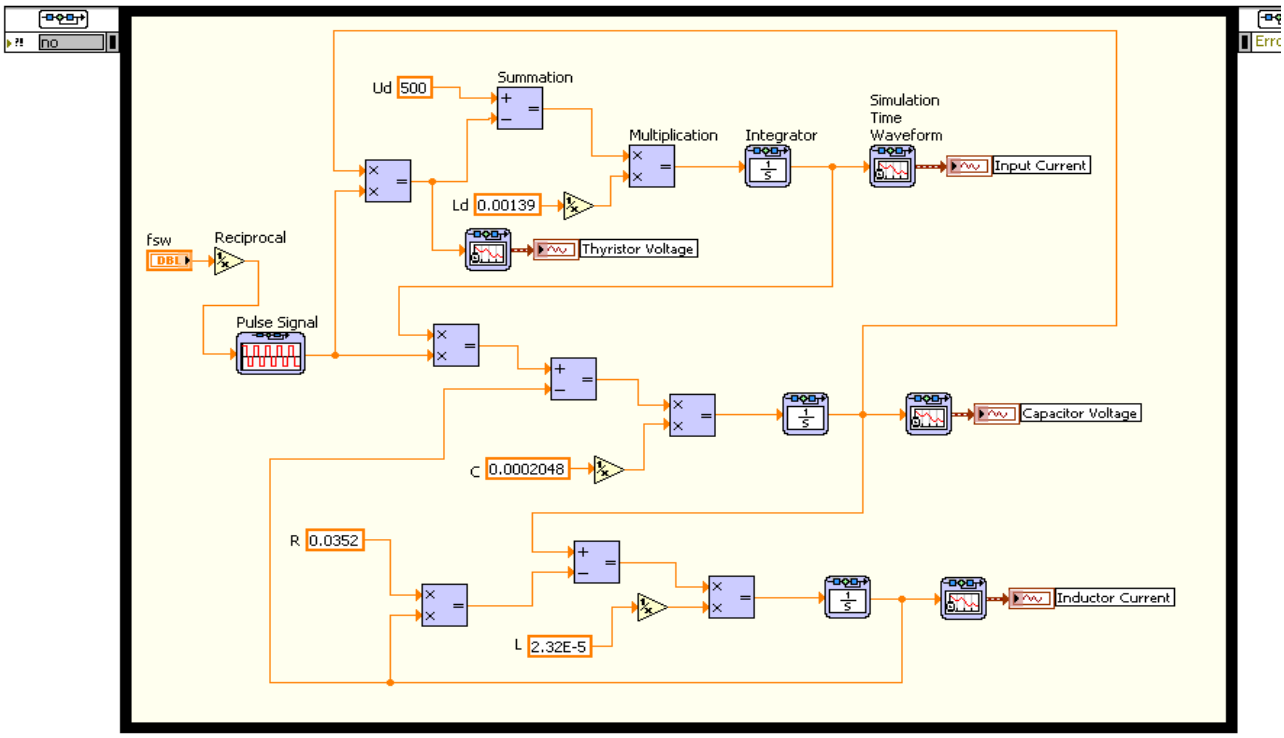

Fig. 3. Block diagram of the system of differential equations (6). On it are show all blocks, inputs and outputs forming the mathematical model of the inverter.

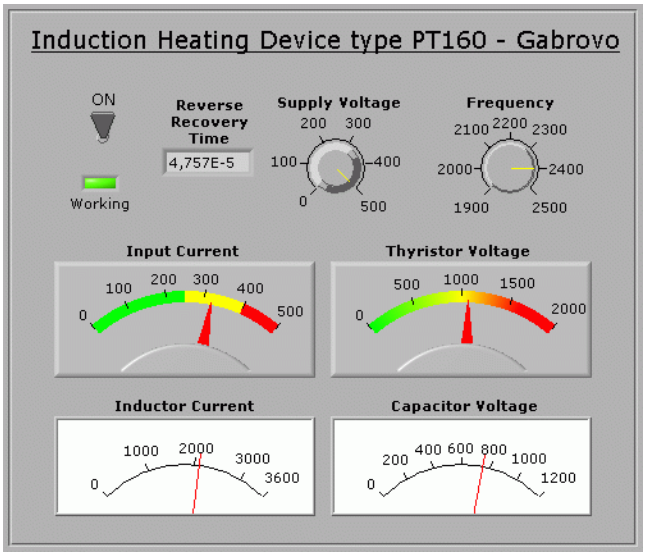

Fig. 4a. Front panel of the induction heating device. Provided is the ability to set up the values of the power supply voltage and the operating frequency; with the provided indicators can be monitored in real time the main parameters during operation.

They are chosen, because are critical for the operation of the current source inverter.

On figure 4b are shown the waveforms of the state variables and the voltage over the semiconductor switches from the bridge. The simulation time is chosen, so that the electronic converter can achieve operation in steady-state.

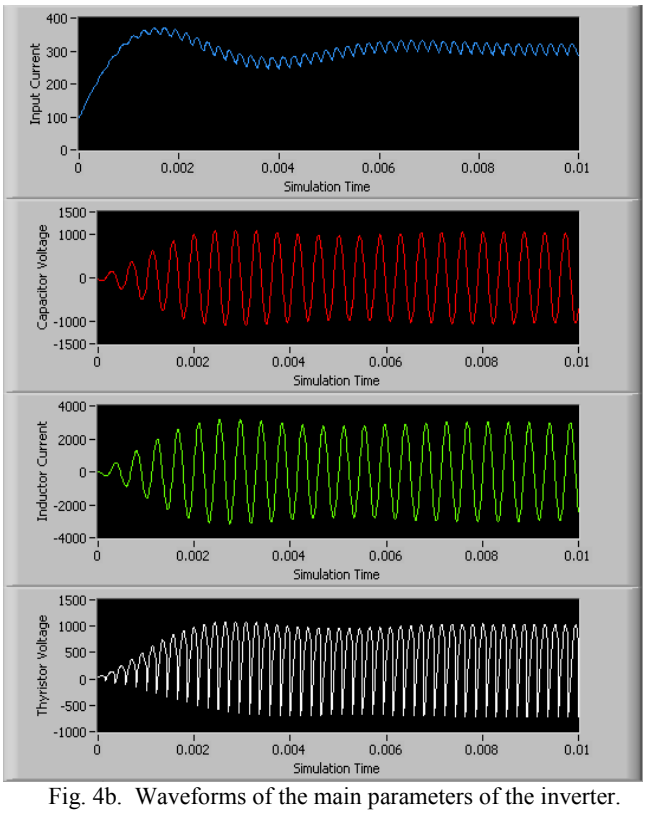

Fig. 4b. Waveforms of the main parameters of the inverter.

The used method accurately presents the processes in the power circuit, by giving also the necessary information and allows tuning and changing the working regime of the inverter.

V. Simulation Results and Comparsion

To verify the model results a comparison is made with a simulation executed with the specialized computer aided design (CAD) software for electrical circuit examination LTSpice® IV.

TABLE I
COMPARSION OF THE SIMULATION RESULTS

Parameter	LabVIEW	LTSpice® IV
Input Current	321.6 A	329.5 A
Inverter Voltage	745.6 V	756.45 V
Inductor current	2.09 kA	2.11 kA
Thyristor voltage	1058.6 V	1060,7 V
Commutated turn-off time	47.6 µs	48.5 µs

The analysis of the data shown in Table I shows that there is a very good match with the results conducted with different examination methods of the power circuit. Also they match with the measured results, conducted during the exploitation of the plant in a real technological melting process [2].

VI. Conclusions

The work proposes the usage of the visual programming development system LabVIEW for the modeling needs of power electronic converters. A successful verification of the model is conducted.

A consideration for future model expansion is to be developed by adding the change of load parameters during real technological process. In this case will be used regulator for maintaining the circuit commutated turn-off time of the thyristors using the appropriate feedback.

Using the developed hardware for data acquisition and signal generation from the National Instruments Company, the test set-up can be expanded even further, which will allow the testing of the auxiliary circuits attached to the technological device. For example these are the regulators, generators, feedbacks, protection etc. – the requirements for accuracy and reliability of such components are very high and this possibility not only cuts the development time, but cuts the costs associated with the verification of such components of the system [20 ÷ 22, 23, 24, 26].

From another point of view the usage of LabVIEW allows during the training of employees, specialists and developers to advance their skills and knowledge in an accessible and flexible way, which does not involve high qualification in software and mathematics as in the usage of similar software platforms [23]. In LabVIEW there aren't accompanying risks both for the employee safety and also for the executive board, which have invested significant resources for the creation and development of given production factory.

ACKNOWLEDGMENT

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Modeling and Investigating the Steady State Mode of Power Inverters for Electro Technology Applications

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Abstract – **This article formulates the new unified interpretation of the analysis of electromagnetic processes in the autonomous (usually resonant) inverters with power circuits having a serial RLC configuration either with or without free wheeling diodes. On this basis, generalized models of resonant inverters with and without reverse diodes are proposed. On this basis the novel compendious relationships between the most important internal inverter parameters are given. With these models, various inverter operating modes were investigated to search for optimal parameters with a defined target function. The whole processed information helps for good understanding and for organizing intelligent design, measurement and control of the inverters for technological applications (induction heating).**

Keywords – **Modeling, Electromagnetic Processes, RLC inverters, Steady State, Unified Interpretation**

I. INTRODUCTION

Inverters are powerful electronic devices with great application in the industry and household. The voltage fed RLC inverter (Fig. 1), its dual counterpart the current fed RLC inverter and the serial RLC inverter without free – wheeling diodes (Fig. 2) cover very wide range of practical autonomous inverter circuits generally applied in electronic technology [4, 6, 11, 12]. In this case important and complex mutually connected problems are the accurate design of the power circuit, appropriate adjustment between the inverter and the load and adequate control providing stable, reliable and efficient operation of the converter when wide variations of the load are expected [3, [6, 12].

The mathematical relationships between the parameters of the mentioned inverters are rather complicated [1, 2, 3, 7, 14]. It has been proved that all the quantities in these second order topologies depend on two variables - the ratio between the controlling angular frequency and the generalized angular frequency (frequency coefficient) $n_{\omega 1} = n_{\omega} = \omega / \Omega$ on one hand, and the ratio between the damping coefficient and the generalized angular frequency $n_{\delta 1} = n_{\delta} = \delta / \Omega$ of the power circuit, on the other. At the same time engineering practice in the area of the power electronics would like to have fast and accurate means for simultaneous solution of the already stated problems. On the other hand, a similar representation of the inverter's AC circuit facilitates formalization and supports power electronics training.

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Then for oscillatory mode $R_i < 2\sqrt{L_i / C_i}$ of the inverter circuit (Fig 1, Fig. 2) coefficient is $c = 1$, for over damped mode ($R_i > 2\sqrt{L_i / C_i}$) $c = -1$ and for critical mode ($R_i = 2\sqrt{L_i / C_i}$) $c = 0$.

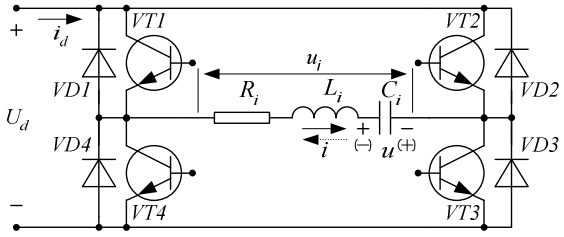

Fig. 1. Voltage fed RLC inverter

The parameters that determine the development of the electromagnetic processes in the steady state in the power inverter circuits are

$$n_{\delta 1} = n_{\delta} = \frac{\delta}{\Omega} = \frac{B_1 \cos\phi_1}{\sqrt{c(4B_1 \sin\phi_1 - B_1^2 \cos^2\phi_1)}} \; (osc.; over\ damped); 1\ (critical) \qquad (1)$$

For resonant inverters (oscillatory mode) the coefficient of hesitation is

$$k_1 = 1/[1 - \exp(-\pi\delta / \omega_0)] = 1/[1 - \exp(-\pi n_{\delta})] \qquad (2)$$

The frequency coefficient is

$$n_{\omega 1} = n_{\omega} = \frac{\omega}{\Omega} = \frac{2}{\sqrt{c(4B_1 \sin\phi_1 - B_1^2 \cos^2\phi_1)}} \; (osc.; over\ damped); \qquad (3)$$

$$\frac{2}{B_1 \cos\phi_1} \; (critical)$$

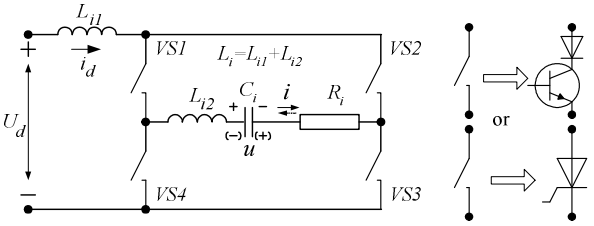

Fig. 2. A serial RLC inverter without free – wheeling diodes

II. THE INVERTER ANALYSIS IN THE STEADY STATE MODE

In contrast to the approaches used in the [4, 6, 7, 8, 9, 12, 13, 14] provided herein is a unified approach to the analysis, which alleviates the description of the behavior of

the power circuit. A constant c_i reflecting the type of the inverter is introduced, having values $c_i = +1$ for the RLC inverter with free wheeling diodes (Fig. 1) or $c_i = -1$ for the RLC inverter without free wheeling diodes (Fig. 2).

The following designations are applied: $f_S(x) = \sin x$, $f_C(x) = \cos x$, $\delta = R_i/(2L_i)$, $\Omega = \omega_0 = \sqrt{1/(L_i Ci) - \delta^2}$ for oscillatory mode; $f_S(x) = \sinh x$, $f_C(x) = \cosh x$, $\delta = R_i/(2L_i)$, $\Omega = \sqrt{\delta^2 - 1/(L_i C_i)}$ for over damped mode; $f_S(x) = x$, $f_C(x) = 1$, $\delta = R_i/(2L_i)$, $\Omega = \delta$ for critical mode.

Then the inverter current and the voltage across the capacitor C_i can be written in the following manner

$$i = \frac{U_d + U_0}{\Omega L} e^{-\delta t} f_S(\Omega t) - c_i I_0 e^{-\delta t}\left[f_C(\Omega t) - \frac{\delta}{\Omega} f_S(\Omega t)\right] \quad (4)$$

$$u = U_d - (U_d + U_0) e^{-\delta t}\left[f_C(\Omega t) + \frac{\delta}{\Omega} f_S(\Omega t)\right] - c_i \frac{I_0}{\Omega C} e^{-\delta t} f_S(\Omega t) \quad (5)$$

The angle $\theta_2 = \theta_0 = \pi\Omega/\omega = \pi/n_\omega$ corresponding to the half period is determined from the controlling angular frequency $\omega = 2\pi f$ and the generalized frequency Ω.

The parameters of the inverter circuit (Fig. 1, Fig. 2) can be determined taking into account the initial conditions for the steady state

$$\begin{aligned} i(0) &= -c_i . i(\theta_0) \\ u(0) &= -u(\theta_2) \end{aligned} \quad (6)$$

And $$i(\theta_1) = 0 \quad (7)$$

Then the determination of the parameters follows. The parameter $a = I_0 \Omega L/(U_d + U_0)$ is

$$a = \frac{f_S(\theta_2)}{e^{n_\delta . \theta_2} + c_i . f_C(\theta_2) - c_i . n_\delta . f_S(\theta_2)} \quad (8)$$

For the inverter in Fig. 1 only the angle θ_1 is determined from

$$\frac{f_S(\theta_1)/f_C(\theta_1)}{1 - n_\delta . f_S(\theta_1)/f_C(\theta_1)} = a \quad (9)$$

The generalized coefficient of hesitation is

$$K = \frac{1}{1 + e^{-n_\delta . \theta_2}\left[(c_i . ca + n_\delta + c_i . a\, n_\delta^2) f_S(\theta_2) + f_C(\theta_2)\right]} \quad (10)$$

It should be underlined that when calculating a and K for discontinuous inverter current mode for Fig. 2 $\theta_0 = \theta_2$ must be put to be equal to π in the already given expressions (8) and (10). This coefficient is analogous to the quality factor of the consecutive resonant circuit and its value gives direct information about the maximum voltage of the resonant capacitor.

The initial capacitor voltage is

$$U'_0 = \frac{U_0}{U_d} = 2.K - 1 \quad (11)$$

The maximal voltage across the capacitor C_i U_m for Fig. 2 is also given by (11). For Fig. 1 it is given by

$$U'_m = \frac{U_m}{U_d} = 2\left(\frac{K}{K_1} - K\right) - 1 \quad (12)$$

The expression for the coefficient K_1 is the same as (10) but the variable θ_2 is exchanged with θ_1 ($\theta_2 \to \theta_1$).

The normalized inverter current and capacitor voltage are respectively

$$i'(\theta) = \frac{i(\theta)\Omega L}{U_d} = 2Ke^{-n_\delta \theta}\left[(1 + c_i . a . n_\delta) f_S(\theta) - c_i . a . f_C(\theta)\right] \quad (13)$$

$$\begin{aligned} u'(\theta) &= \frac{u(\theta)}{U_d} = 1 - 2Ke^{-n_\delta \theta} \\ &\left[(c_i . c . a + n_\delta + c_i . a . n_\delta^2) f_S(\theta) + f_C(\theta)\right] \end{aligned} \quad (14)$$

The average value of the input current (all values are normalized) is

$$I'_d = \frac{I_d \Omega L}{U_d} = \frac{1}{\theta_0}\int_0^{\theta_0} i'(\theta) d\theta = \frac{1}{\theta_0} . \frac{2(2K-1)}{n_\delta^2 + c} \quad (15)$$

The RMS value of the inverter current is

$$I' = I\Omega L/U_d = \sqrt{I'_d/(2.n_\delta)} \quad (16)$$

The output characteristic (Fig. 1 and Fig. 2) is

$$OCH = I'/I'_d \quad (17)$$

The input characteristic is

$$ICH = 1/(n_\omega . I'_d) \quad (18)$$

The characteristic of the coefficient of nonlinear distortion (klir – factor) of the inverter current is

$$kf[\%] = 100 . \sqrt{I'^2 - I'^2_{(1)}}/I'_{(1)}, \quad (19)$$

where $I'_{(m)}$ $(m = 1,3,5,7,...)$ is the m- th harmonic component of the inverter current. (The mathematical expressions for calculation of the harmonic components in the different circuits and modes of operation are disparate, and they are rather complicated. They have been found and published in earlier authors' publications.)

From that point on the analysis of the power inverter may be continued without problems in a normalized or in a non normalized form.

III. MODELING SERIAL RESONANT INVERTER WITHOUT FREE WHEELING DIODES

It is known that resonant inverters are capable of operating with discontinuous continuous and continuous continuous mode [3, 4, 5, 6, 7]. Mathematical models based on switching functions have been developed for these cases, thus generating a uniform differential equation system. The power losses in the inverter are neglected. the model is based on the following assumptions: The commutation of the power semiconductor devices is instantaneous. A parallel equivalent circuit represents the induction heater. The quality factor of the load circuit is

sufficiently high that the voltage across the load has a close to the sine wave shape.

Figure 3 presents a generalized model of a parallel resonant inverter without free-wheeling diodes, realized in the Matlab/Simulink environment.

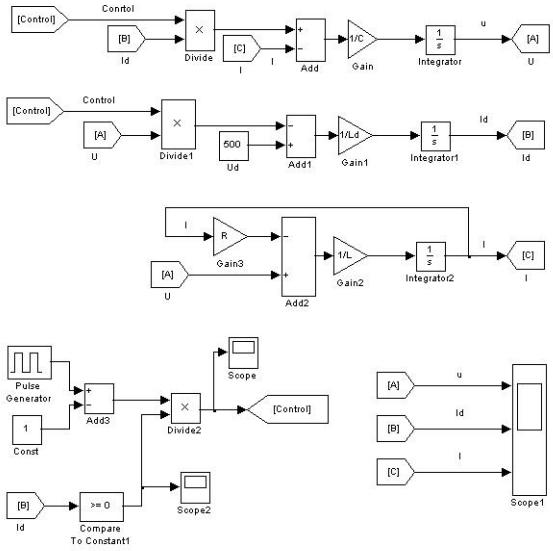

Fig. 3. Model of resonant inverter without free – wheeling diodes

Figure 4 shows the results of the model's experiments when operating in a continuous continuous mode (current fed invertor mode) with the following data: input DC voltage $U_d=500\ V$; input inductance $L_d=2.5872\ mH$; load parameters: $R=0.049\ \Omega$, $L=32.3313\ \mu H$, load capacitors $C=145.0415\ \mu F$, switching frequency $f=2400\ Hz$.

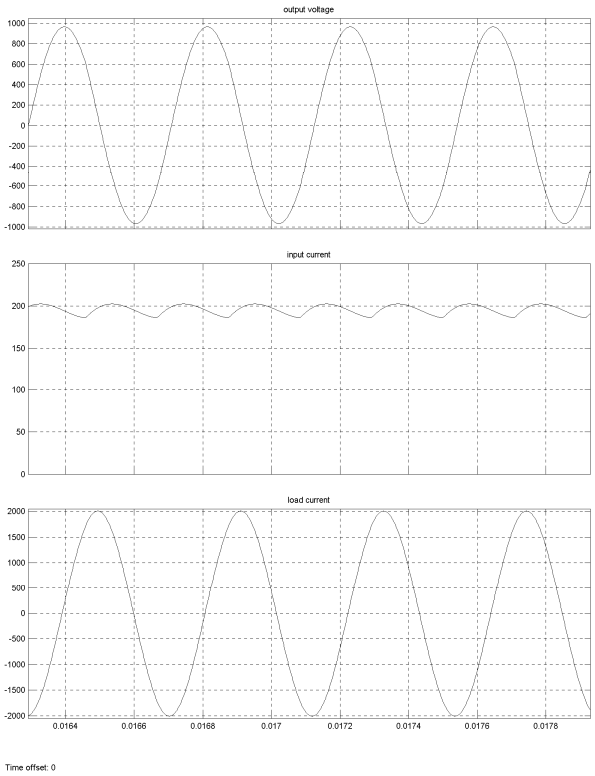

Fig. 4. Results for operating in continuous continuous mode

The power chain variables are built in the figure. All the necessary voltage and currents for the design of the inverter can be determined.

Figure 5 shows the results of the model's experiments when operating in a discontinuous continuous mode (resonant invertor mode) with the following data: input DC voltage $U_d=500\ V$; input inductance $L_d=67.5398\ \mu H$; load parameters $R=0.1266\Omega$, $L=33.1919\ \mu H$, load capacitors $C=56.0497\ \mu F$, switching frequency $f=4000\ Hz$.

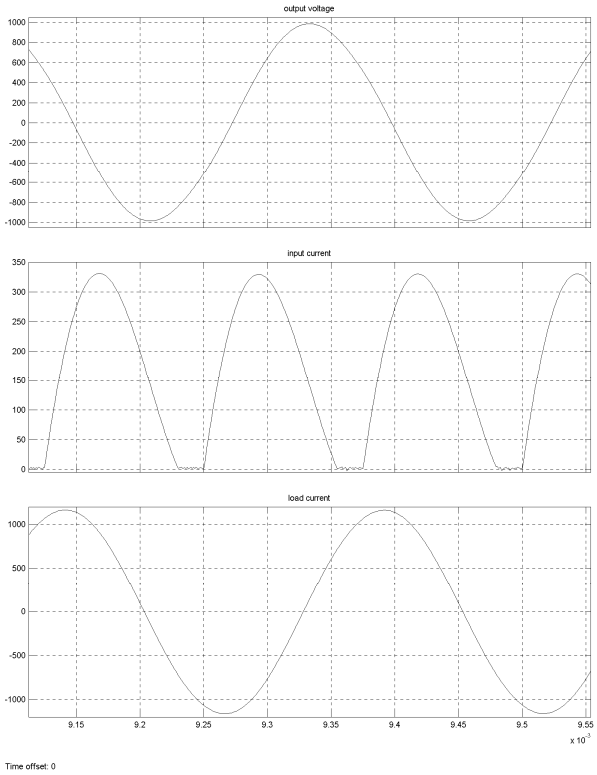

Fig. 5. Results for operating in discontinuous continuous mode

This mode is suitable for operation with thyristors, because it guarantees a larger circuit time for recovery.

IV. Modeling Serial Resonant Inverter with Free Wheeling Diodes

Figure 6 presents a generalized model of a parallel resonant inverter with free-wheeling diodes, realized in the Matlab/Simulink environment. The proposed model allows experiments to be performed in a frequency control mode below and above the resonant.

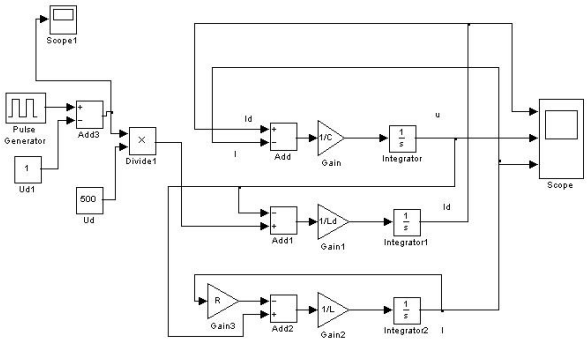

Fig. 6 Model of resonant inverter with free – wheeling diodes

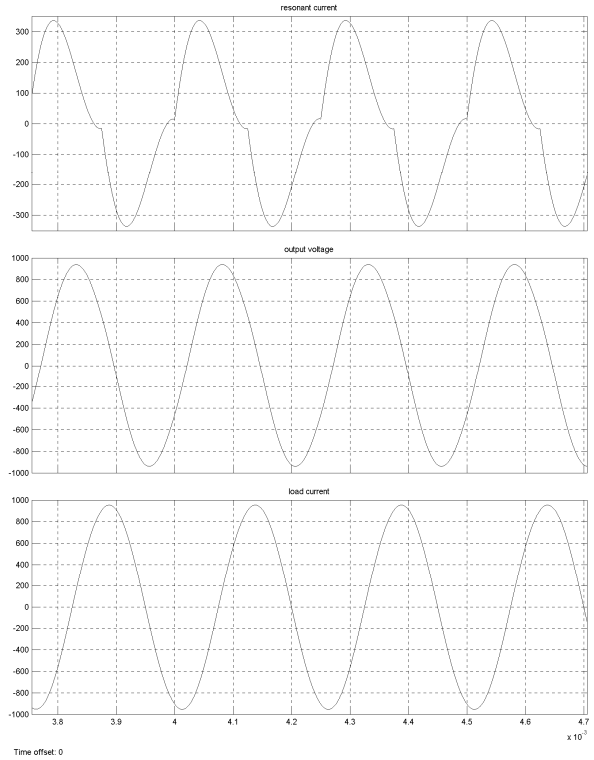

Fig. 7. Results for operation with switching frequency below the resonance

Figure 7 shows the results of the model's experiments when for inverters operation with switching frequency below the resonance, with the following data: input DC voltage $U_d=500\ V$; resonant inductance $L_d=65.072\ \mu H$; load parameters $R=0.196\ \Omega$, $L=38.197\ \mu H$, load capacitors $C=49.709\mu F$, switching frequency $f=4000\ Hz$.

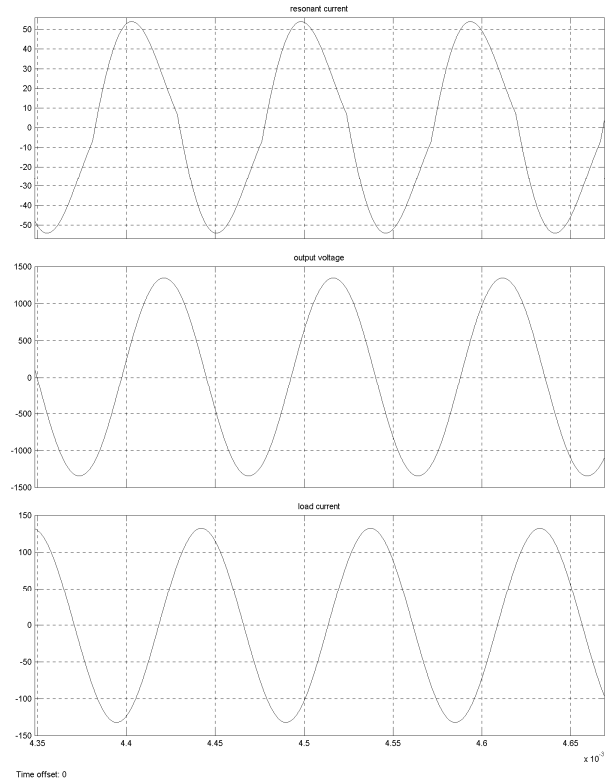

Fig. 8. Results for work with switching frequency above resonant

Figure 8 shows the results of the model's experiments when for inverters operation with switching frequency above the resonance, with the following data: input DC voltage $U_d=500\ V$; resonant inductance $L_d= 338.8438\ \mu H$; load parameters $R= 1.96\Omega$, $L=152.82\ \mu H$, load capacitors $C= 1.9782243\mu F$, switching frequency $f=10000\ Hz$.

The figures are represented sequentially as follows: the resonant current, the output voltage and the current through the load. These are the state variables for the studied power scheme.

In both modes of operation of resonant inverters with free – wheeling diodes, a switching frequency almost equal to the resonant is selected. In this way, small times of conduction of the reverse diodes are obtained, which produces good energy parameters of the converters.

The presented models of resonance inverters with electro technology applications are verified using computer simulations and real technological devices.

The use of a visual programming environment greatly facilitates the development and deployment of models because it does not require advanced engineering and applied mathematics knowledge.

V. Conclusions

Serial RLC inverters without or with free wheeling diodes for industrial application are investigated. A novel unified interpretation of the electromagnetic processes is applied based on the previously calculated inverter network parameters in a normalized form.

The requirements for the control system are defined, which is useful for research on the type of offline simulation, hardware in the loop and rapid prototyping. In the development of power electronic devices, off-line simulations are applied, as for the implementation of practical escapements a powerful power supply network, water cooling, expensive high volume and weight building blocks is needed [15, 16].

The main contribution of the work is an approach to analysis of a series RLC DC / AC converters for electro technology application. This allows the creation of methods for engineering design that are simple, such as mathematical, but with sufficient precision for engineering practice. This is very important because it supports the training of power electronics specialists and facilitates the understanding of the complex processes in the inverters.

The use of formalization of electromagnetic processes in the inverter by switching functions allows the realization of the models in other environments as for visual programming as well as with mathematical software. This is very useful because it does not oblige the user to own certain software that is often a paid license.

Acknowledgment

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Analysis and Improvements of a Buck Converter Based LED Driver

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Abstract – **This paper studies a buck converter based LED driver with a current control method. A wide input voltage range is considered as well as the power factor of the circuit. To improve the efficiency soft switching conditions are provided. Simulations and experimental investigation is carried out to obtain the converter performance relations. An advanced inductor design is applied in order to reduce the eddy current losses in windings due to air gap fringing field. Combined Litz wire - full wire approach is considered to reduce the effect of air gap fringing field. Experimental results and measurements confirm the simulation results and performance of the investigated converter.**

Keywords – **Light-Emitting Diode Driver, Inductor Design, Air Gap Fringing field**

I. Introduction

Nowadays there are two groups of converters used for driving LEDs - converters with and without a transformer. The total efficiency and mass/volume parameters are better for AC/DC/DC drivers without a transformer [1]. Conventional voltage mode control and the peak-current mode control are analyzed in order to compare its output current ripple responses [1]. A practical comparison of circuit topologies suitable for passive LED drivers is presented in [2] with energy efficiency of 92–94 % at 50 W consumption. Dimmable light-emitting diode (LED) driver with adaptive feedback control is introduced in [3] suitable for low-power lighting applications. A special converter with limited duty cycle for driving LEDs is presented in [4]. The converter is applicable for street, home, and automotive lightning applications. Two topologies for LEDs street lighting are investigated in [5] and high power factor is reported. The converters are supplied with an alternative source (battery) during the peak load time. A two-stage LED driver achieving high efficiency over a wide load range [6] is based on a buck converter as the first stage and a multichannel constant current CLL resonant converter as the second stage. A novel bias supply scheme for LED controller is considered in [7] based on buck converter.

The purpose of the current paper is to investigate the performance main indicators of an industrial unregulated AC/DC/DC converter without transformer in nominal operational mode and the deviations (improvements) based on it in order to verify the quality indicators and search for solutions to improve them.

The tasks to be solved are:

1. Choosing a mass production LED illuminant with built in buck converter.
2. Creating a laboratory setup and investigation of the selected sample.
3. PSPICE simulation of equivalent circuit of the selected driver circuit.
4. Analysis of the results and investigation of improved circuits.

II. Investigated Converter Topology

The selected illuminant and appropriate buck converter is TOWN ST-18W with parameters as given in Table 1.

Table 1. Parameters of TOWN ST-18W

Ud	AL	P	BA	Fx	CT N White	ΔP
[V]	*[h]*	*[W]*	*[°]*	*[Lum]*	*[K]*	*%*
48 - 50	50000	18	180	3750	3500 - 5500	5

The investigated LED illuminant consists of 18 high-power diodes that are connected in series. The LED bulb type is bubble ball bulb. The equivalent schematic of the illuminant is acquired from [8]. It consists of a diode Dn, voltage source En (48 V) and resistor Rn (3 ÷ 4 Ω). This equivalent schematic explains the obtained current and voltage values of the examined LED illuminant that acts like a non-linear element.

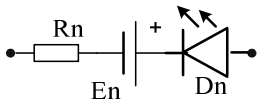

Fig. 1. Equivalent scheme of a LED

Based on the schematic of the selected power converter for LED and the equivalent schematic of the illuminant a PSPICE model is built (Fig. 2).

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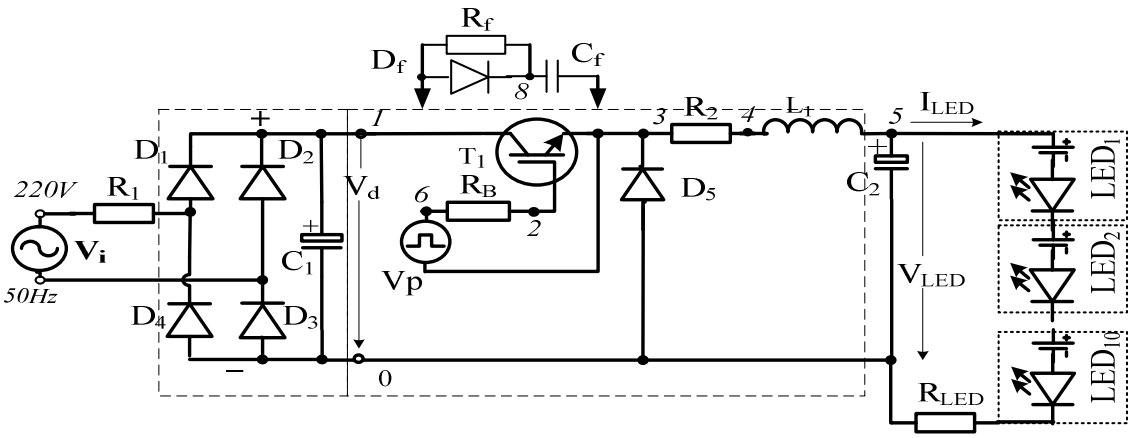

Fig. 2. Investigated converters for driving LEDs (PSPICE model)

The investigated simulation model consists of 3 parts with different functions:

- I part – grid rectifier with smoothing capacitor;
- II part – DC/DC buck converter;
- III part – equivalent schematic of LED illuminant.

The duty ratio δ range of variation is defined by:

$$\delta = \frac{V_{LED}}{V_d} = \frac{48}{310} = 0{,}16 \qquad (1)$$

The elements from the simulation model have the following values: Transistor Z_1 - IXGH40N60A, R_1 = 0,1 Ω, C_1 = 1 μF, R_2 = 0.2 Ω, L_1 = 435 μH, C_2 = 10μF, V_{LED} = 48 ÷ 50 V, f_{op} = 50 kHz.

The results from the simulation of the investigated power converter for LED illuminant are given in Fig. 3: transistor T_1 voltage and current U_{EC} = 310V, I_c = 1.2A, load current and average current value I_{LEDavg} = 280 mA.

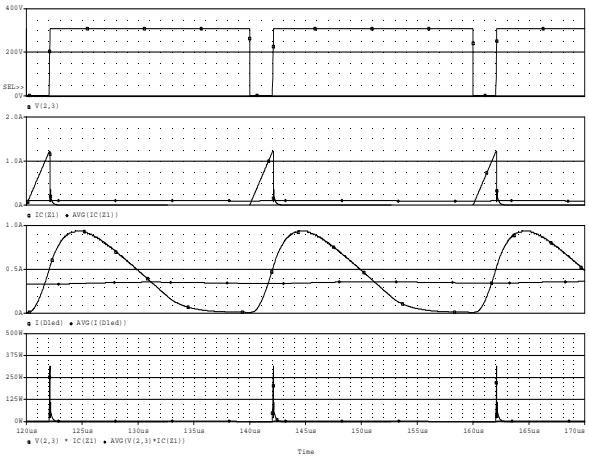

Fig. 3. Operating diagrams of the buck converter (simulations), voltage across the switch, diode current, average load current, switching losses of the transistor

The simulation results for the studied LED parameters at voltage range 0 ÷ 240 V are given in Fig. 4 and Fig. 5. The presented results lead to the following 4 conclusions:

1. The LED voltage and current variations are observed for the input voltage range 50÷120V because the buck converter output is stable in the range 120 ÷ 240 V.
2. The regulation of the light flux is outside the stabilization range of the DC/DC converter and is in a narrow range;
3. The investigated converter has increased switching losses when turning off the transistor (Fig.6);
4. The Power factor cosφ of the converter depends on the selection of proper values of the reactive elements of the AC/DC/DC converter.

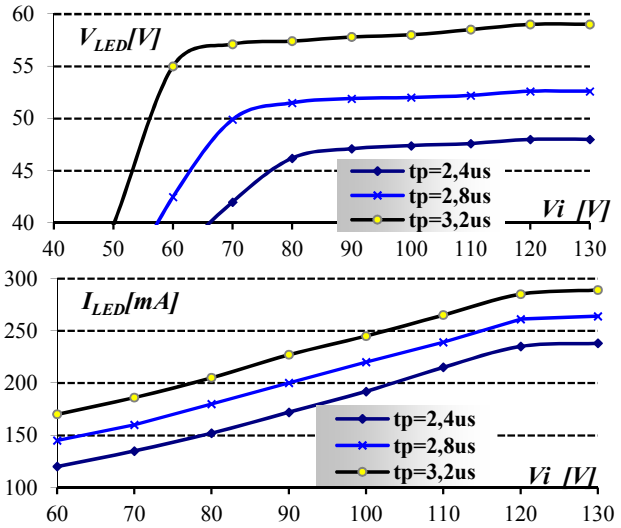

Fig. 4. Voltage V_{LED} and current I_{LED} of the LED as a function of the input voltage RMS value, V_i

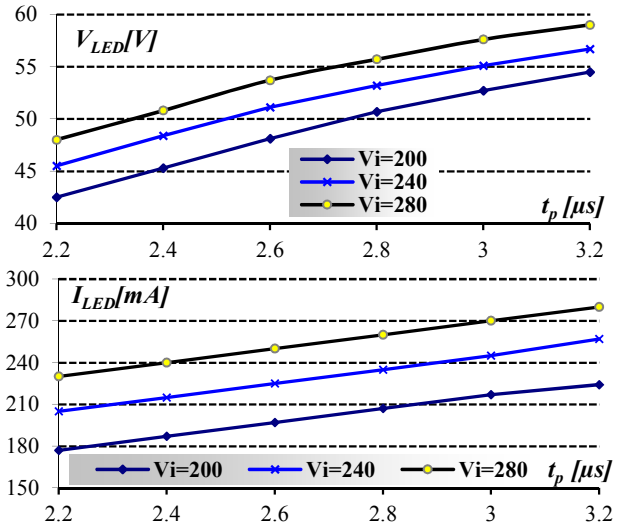

Fig. 5. Voltage V_{LED} and current I_{LED} of the LED as a function of the ON interval of the transistor (t_p)

III. Soft Switching Mode

Soft switching in DC-DC converters is recommended for obtaining lower losses [9]. The reduction of the switching losses of the investigated driver circuit can be realized using R_f, C_f, D_f group, connected in parallel to the commutating transistor. The switching losses in both cases are given in Fig.6 and Fig. 7. The auxiliary group elements have the following values: $R_f = 30\ \Omega$, $C_f = 0.030\ \mu F$ and D_f is a fast Schottky diode. A significant reduction of transistor losses is obtained as the average value is below 0.5 W.

Further, a laboratory setup is realized for measurement of the technical indicators of LED illuminant in nominal operational mode and variation of supply voltage. It is shown in Fig. 8. The acquired experimental results are summarized in Table 2.

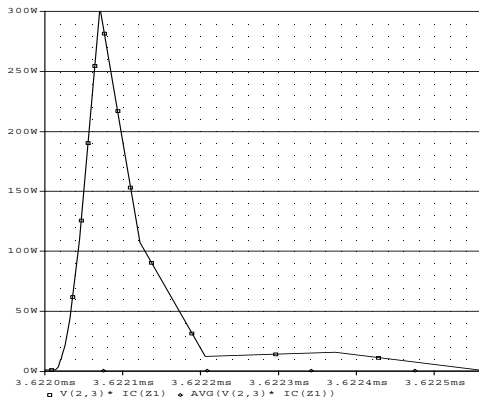

Fig. 6. Transistor switching losses without an auxiliary circuit

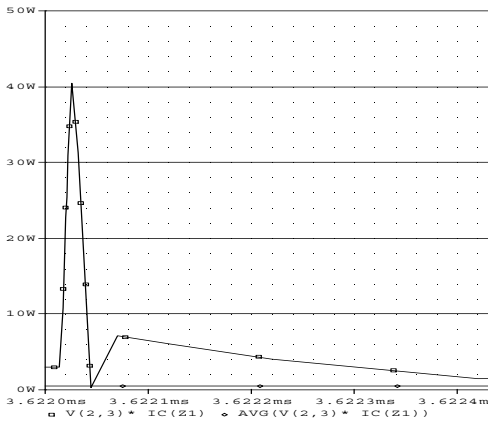

Fig. 7. Transistor switching losses with an auxiliary circuit - obtained soft switching

The experimental results of the illuminatnt control circuit are given in Fig. 9 and Fig. 10 presenting the current I_{LED} of the simulated circuit and the power factor (cosφ) of the total circuit. The experimental results confirm the carried out simulations.

IV. Combined Litz Wire - Full Wire Inductor Design Application

A proper design of inductors includes the specifics, depending on the type of inductor DC inductors, HF (high frequency) inductors and combined DC-HF inductors.

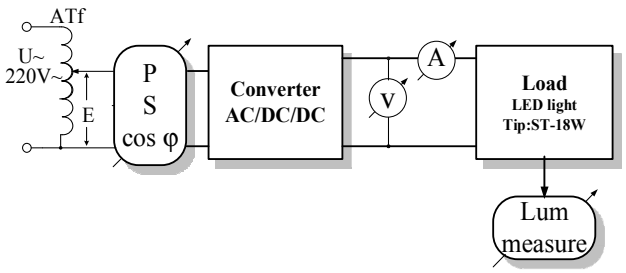

Fig. 8. Block diagram of the realized experimental set up for measuring the converter main parameters

TABLE 2. EXPERIMENTAL RESULTS , LOW SUPPLY VOLTAGE, 60 ÷ 140 V

Ui	*[V]*	60	70	80	90	100	110	120	130	140
Ud	*[V]*	*57*	*57.7*	*57.9*	*58*	*58.2*	*58.4*	*58.7*	*58.7*	*58.7*
Id	*[mA]*	170	210	210	220	230	240	260	260	260
Light	*[Lux]*	1140	1250	1250	1600	2000	2500	3000	3600	3600
cosφ		0.21	0.7	0.8	0.84	0.88	0.94	0.98	0.98	0.98
P	*[W]*	9.7	12.1	12.2	12.8	13.4	14.0	153	15.3	15.3

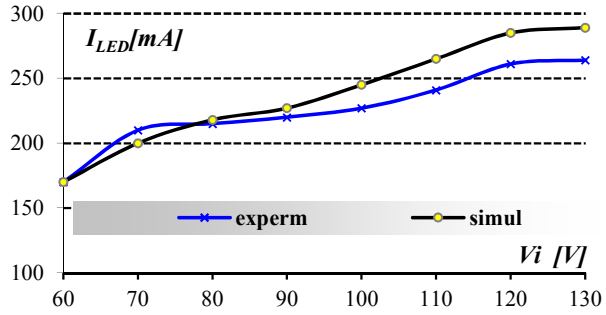

Fig. 9. Current I_{LED}, measurements and simulations

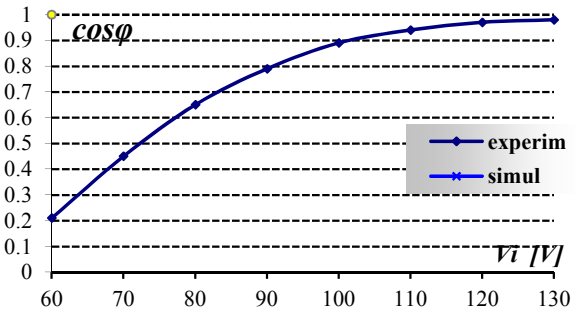

Fig. 10. Measured and simulations obtained power factor (cosφ) of the total LED driver circuit

In the considered converter we have a combined DC—HF inductor, where the losses of the HF component are comparable to the DC or LF (low frequency) losses. A special combined design: full wire – Litz wire solution is discussed, Fig.11 [10] to be applied in the converter. The construction includes a cylindrical spacer, Litz wire area and full wire area. Thus, in the vicinity of the air gap, where the fringing field is strong there is no windings (spacer). Then in the next area where this fringing filed is decreased, only Litz wire is placed. The second innovation is screening the HF MMF (magneto-motive force) of the air gap using Litz wire, the remaining part of the winding area is filled with full wire.

Thus, both benefits of Litz wire and full wire could be used in one design.

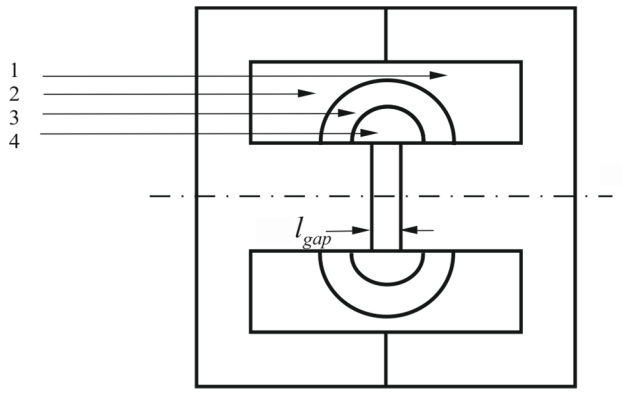

Fig. 11. Cross section of the considered combined inductor design: full wire – Litz wire, 1) full wire winding 1, 2)) full wire winding 2, 3) Litz wire winding, 4) spacer

Moreover, a special arrangement is achieved in which the HF losses only in the Litz wire have to be considered (calculated), based on the first design proposed in [10, 11]. The HF losses in the full wire part can be neglected. The Litz wire area is located near the air gap, Fig.11. Assuming that only the Litz wire carries HF current, then almost no fringing field is present for a radius higher than r_2. The H-field depends on the enclosed MMF and it is inverse proportional to the distance to the air gap:

$$H = \frac{N_L\, i}{2\pi r}\frac{r_2^2 - r^2}{r_2^2 - r_1^2} \tag{2}$$

where N_L is the number of Litz wire turns;
r_1, r_2 is the inner/outer radius of the Litz wire area
Then, based on LF eddy current loss approximation [12, 13]:

$$P_{LF}(f) = \frac{l_c\, \pi (\omega \mu_0 H)^2 d^4}{64\rho}\, p \tag{3}$$

the following expression is derived for the power losses $P_{cu,eddy,Litz}$ in p strands of Litz wire:

$$P_{cu,eddy,Litz} = \frac{\pi l_w d_s^4\, p}{64\rho_c}\left(\frac{\mu_0 N_L\, \omega I}{2\pi r_1}\right)^2 \frac{1}{3}\, k_L\left(\frac{r_2}{r_1}\right) \tag{4}$$

where p is the number of strands;
d_s is the diameter of the strand;
l_w is the length of the Litz wire [11].

Using the presented combined DC-HF inductor design allows to obtain a design with reduced eddy current losses in windings in the studied LED driver circuit up to 30%. It was found that the reduction obtained depends on the ratio $I_{L,AC}/I_{L,DC}$. The design was made on EE13/7/4 core, N87 grade, with 81 turns, d=0.25mm.

V. Conclusion

This paper studies a buck converter used for LED driver with a current control method. A wide input voltage range is considered as well as the power factor of the circuit. Further improvement of PF (power factor) can be obtained by reducing the input filter capacitor value.

To improve the efficiency soft switching conditions are provided. An auxiliary circuit including components R_f, C_f, D_f is used to obtain soft switching conditions for the power switch, thus reducing the switching losses more than 2 times.

An advanced inductor design is applied in order to reduce the eddy current losses in windings due to air gap fringing field. Combined Litz wire - full wire approach is considered to reduce the effect of air gap fringing field. It was found that the reduction obtained depends on the ratio $I_{L,AC}/I_{L,DC}$ and could reach 30%.

Experimental measurements confirm the simulation results and performance of the investigated converter concerning the efficiency, power factor (cosφ) and flux of the studied LED driver circuit.

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Design of a MOSFET Bypass Switch for Individual Pixel Control in a Matrix LED Headlamp Application

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Abstract – **A low-cost, high performance solution for single LED control in a matrix LED configuration is presented in this paper. The integrated solutions on the chip market are evaluated and an improved discrete, robust LED bypass circuit is designed und simulated. A complex prototype PCB with the proposed LED bypass circuit has been designed and thoroughly investigated. The performance of the proposed LED bypass solution has been evaluated in terms of speed, resolution and power losses.**

Keywords – **LED Driver, LED Matrix, LED Bypass, Level Shifter, Single LED Diagnostics**

I. Introduction

The LEDs play a key role in the modern automotive headlamp technology, due to their high efficiency, robust mechanical construction, high life expectancy and design advantages. Applying individual LED control in multi-LED-arrays [1], [2] enables brand new lighting functions like dynamic bending light without moving parts, glare-free high- and low beam, information projection on the road (Fig. 1):

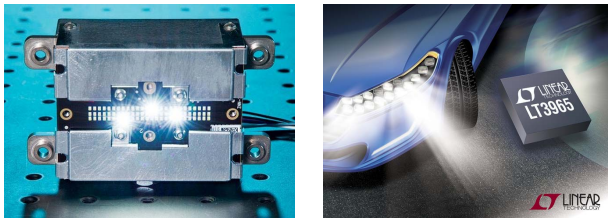

Fig.1. Example for LED matrix light module (left) and headlamp (right)

While highly integrated LED-matrix controllers [3], [4] have been designed in the past, they rely on costly and high-ohmic solutions, not capable of meeting the demands of the market.

This paper presents a discrete, cost-efficient und low-ohmic solution for a single LED bypass control.

II. Bypass LED Control Basics

The common single LED control technique comprises a FET in parallel with each LED. Since the LEDs are usually connected in series, the saturated FET diverts the current, turning the LED off on request (Fig.2):

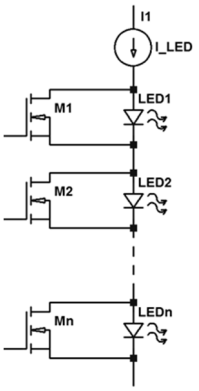

Fig.2. Individual LED control with bypass switches

N-channel FETs are mostly used as bypass switches *M1…Mn* due to their better R_{DS}-to-cost ratio. Since these FETs "float" relative to the ground, a voltage source with amplitude higher than the source potential of the uppermost FET *M1* plus its gate-source threshold voltage is required. In power LED application, two types of voltage step-up generators are widespread: standard boost converters with magnetic energy storage and non-inductive charge pumps (Fig. 3):

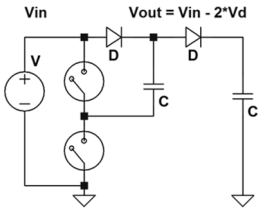

Fig.3. Example for voltage "doubler", a simple charge pump

In the commercial chip solutions, an integrated charge pump is widely used to deliver the elevated gate supply voltage. The disadvantages of a charge pumps are mainly of EMC nature – the high slew rate of the capacitor charging and discharging currents introduces rich harmonics content which often violates the automotive EMC regulations.

In the proposed solution the readily available output voltage of the step-up converter is used as a gate voltage source (Fig. 4), due to the fact that most LED drivers require enough headroom (a difference between output and input voltage) in order to work properly. This headroom usually easily satisfies condition (Equ. 1) at no added cost.

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III. Proposed LED Bypass Circuit

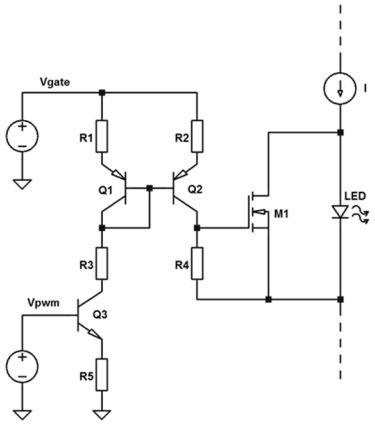

Fig. 4. Proposed LED bypass control circuit

Obviously, the minimum supply voltage of the proposed LED bypass driver must satisfy the condition:

$$V_{GATE} \geq V_{LED\ STRING-1,MAX} + V_{CEQ2,SAT} + V_{THRESHOLD,M1} \quad (1)$$

in order to guarantee the robust commutation of the transistor *M1*.

The voltage source V_{PWM} (e.g. a microcontroller PWM output) controls the transistor *Q3*. Due to the resistor *R5* the transistor *Q3* works as a constant current sink with nominal current expressed by:

$$I_{R5} = \frac{V_{PWM} - V_{BEQ3}}{R_5} \quad (2)$$

This current also flows through *R3, Q1* and *R1*. The transistors *Q1* and *Q2* (ideally a dual matched transistor) form a current mirror. Thus, the collector current of *Q2* is approximately equal to the collector current of *Q1*. It flows through the resistors *R2* and *R4*, introducing a voltage drop across *R4*. With properly selected ratio of *R4* to *R5,* the gate-source voltage of the bypass transistor *M1* can be chosen so that it guarantees the saturation of *M1:*

$$V_{GATE,M1} \geq V_{SOURCE,M1} + V_{THRESHOLD,M1} \quad (3)$$

The gate of the bypass transistor *M1* is biased by the voltage across *R4*, therefore its value should be selected in accordance with the condition:

$$R4 \geq \frac{R_5 V_{THRESHOLD,M1}}{V_{PWM} - V_{BEQ3}} \quad (4)$$

IV. Component Choice

For the purposes of the circuit analysis we will assume a gate supply voltage of 45V and maximum LED string voltage of 30V. The bypass switch of choice, FDS3812, is a dual 80V-FET with low R_{DSon} and gate charge. The gate capacitance of the bypass FET, which must be charged by the level-shifter is

$$C_{GS\_T7} \approx \frac{Q_{T_{M1}}}{V_{GS_{M1}}} = \frac{13nC}{8V} = 1.63nF \quad (5)$$

The current, needed to charge this capacitor within 3…4µs in order to achieve an 8-bit dimming PWM resolution, is approximately

$$I_{GS\_M1} \geq C_{GS_{M1}} \frac{\Delta V_{GS_{TH_{M1}}}}{\Delta t} = 1.63nF \frac{4V}{3.3\mu s} \approx 2mA \quad (6)$$

Thus, the resistors *R4, R5* (assuming that they have equal value) can be determined as

$$R4 \leq \frac{5.0V - 0.6V}{2mA} \approx 2.2k\Omega \quad (7)$$

The resistor *R3* absorbs part of the power losses, which would otherwise emerge in the level shifter transistor *Q3*. The resistors *R1, R2* have rather low values and introduce a local positive feedback to improve the current symmetry in the current mirror *Q1/Q2*. The level shift transistor *Q3* must withstand the voltage V_{GATE}. The circuit parameters and component values and are summarized in Table 1:

TABLE 1. LED Bypass Circuit Values

Parameter, Component	Value, Part Number
U_{GATE}	30V...45V
I_{LED}	1A
R_1, R_2	100Ω
R_3	8.2kΩ
R_4	2.2kΩ
R_5	2.2kΩ
Q_3	BC546B
Q_1,Q_2	BC556B
M_1	FDS3812
PWM resolution	8-bit
PWM frequency	300Hz

V. Simulation

A SPICE simulation with the chosen components can now be performed with a detailed schematic (Fig. 5):

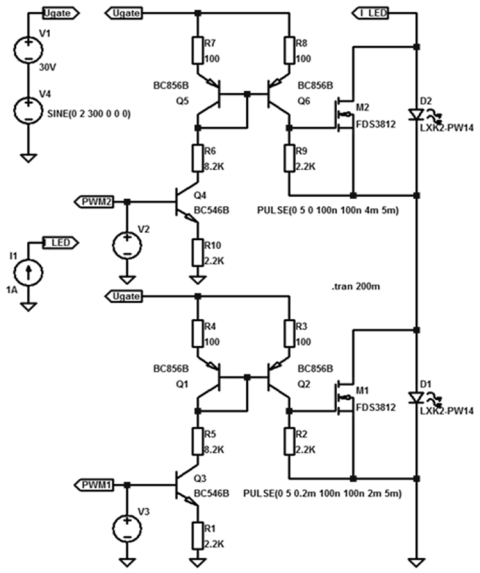

Fig. 5. Spice simulation schematic for the proposed LED bypass

The simulation results show the LED string voltage (1st trace), two phase-shifted control PWM signals (2nd and 4th trace) and the tightly controlled LED currents through LEDs *D1* (5th trace) and *D2* (3rd trace) on Fig. 6:

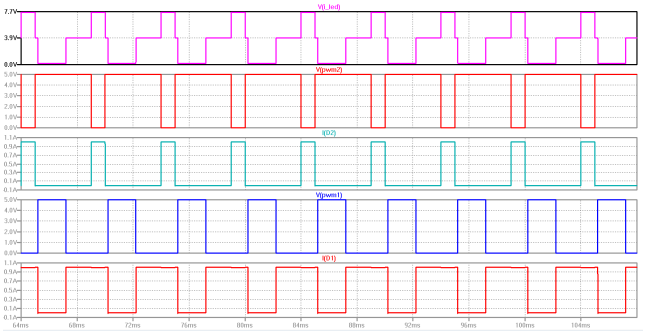

Fig. 6. Simulation results for the proposed circuit. The individual LED currents are well controlled by the dimming PWM signal

VI. Experimental Evaluation

A. Prototype

The proposed LED bypass circuit has been assembled on a single PCB with 40 bypass FETs and two microcontrollers for PWM signal generation (Fig. 7):

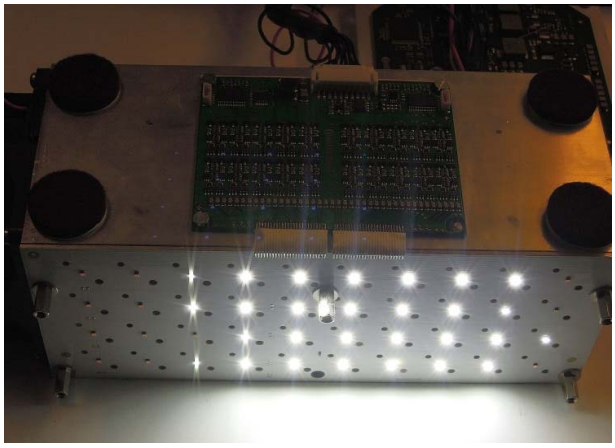

Fig. 7. Practical implementation of the proposed circuit for individual LED dimming control

The LEDs are organized in a matrix configuration and can be individually controlled by 10-bit, 300Hz PWM. As can be seen on the picture, some of the LEDs have different dimming levels applied.

B. LED Current Spikes

A practical problem arises due to the output capacitance of the constant current driver (e.g. capacitor *C22* on Figure 9). A certain amount of capacitance is usually needed to smooth out the inductor ripple current and reduce the electro-magnetic emissions, since the constant current source is mostly a DC/DC-converter, for example the one presented in [5]. This capacitance will be charged to the maximum LED string voltage and the energy, stored in it will induce a large LED current spike upon reducing the length of the LED string by a bypass switch (Fig. 8):

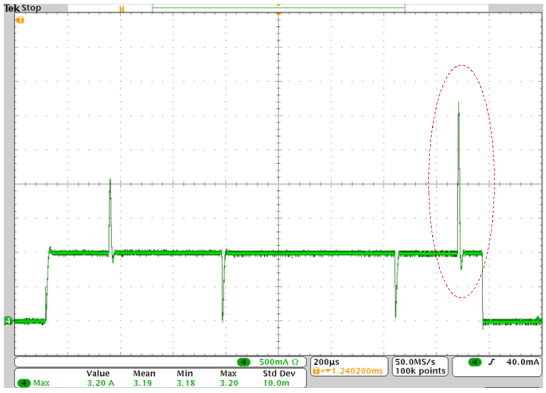

Fig. 8. LED current spikes due to current source output capacitance

C. Adding Miller Capacitors

The peak LED current amplitude might well exceed the maximum values specified in the LED datasheet due to the bypass spikes. Therefore, Miller capacitors *C50, C51* are added between gate and drain of the bypass FETs to increase the switching time and reduce the amplitude of the current spike [6] (Fig. 9):

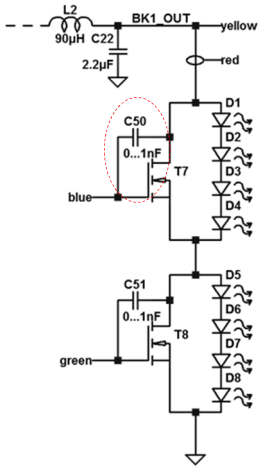

Fig. 9. Evaluation circuit including Miller capacitors

The capacitance C_{GD} provides a positive feedback path between output and input of the bypass FET. Increasing C_{GD} by an external capacitor effectively decreases the drain voltage slew rate, forcing the bypass FET to remain longer in the active region (Fig. 10):

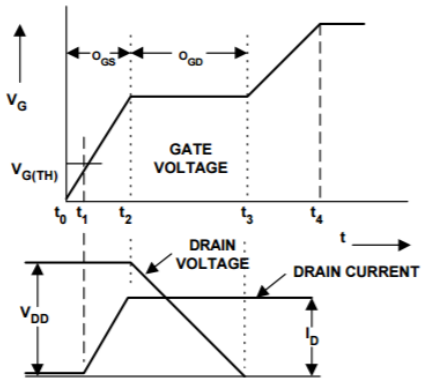

Fig. 10. Effect of increasing the value of C_{GD}

Experimental tuning of the Miller capacitors until the LED current overshoot is reduced below the design margin of 10% yields longer switching times (Fig. 11):

Fig. 11. Evaluation circuit including Miller capacitors

D. Power Losses in the Bypass FET

Adding Miller capacitors helps decreasing the current peaks in the LEDs during the dimming, but also increases the bypass FET switching losses. Consider, for instance, a situation, where four from the eight LEDs in the sting are bypassed. This forces the voltage across the output capacitor C22 to decrease from 28V to 13V. The measured switching time is 40µsec (Fig. 12):

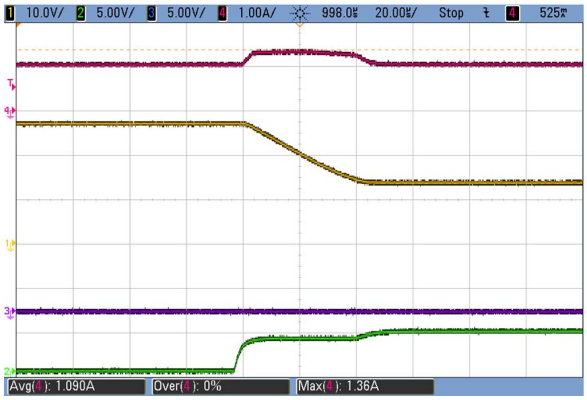

Fig. 12. LED current (1st trace) and voltage (2nd trace) during bypass commutation of four LEDs

A quick estimation of the switching losses in the bypass FET, according to the equation in [7], results in:

$$P_{SW} = 2f_{SW}\int_{o}^{40\mu s} u(t)i(t)dt \qquad (8)$$

and, after substituting the measured values:

$$P_{SW} = 2 * 300Hz * 40\mu s\frac{1.33A(28-13)V}{2} = 0.239W \qquad (9)$$

The conduction losses of the bypass FET can also become significant. Consider, for example, a PWM duty cycle of 90%, the typical R_{DSon} of the hot FET FDS3812 be 140mΩ and 1.5A LED current. Thus, the total FET losses become:

$$P_{LOSS} = P_{SW} + P_{COND} = = 0.239W + 0.95 * 2.25A * 140m\Omega = 0.538W \qquad (10)$$

This power loss figure clearly indicates the limitations of the integrated LED bypass solutions: for instance, in a ten-LED configuration the momentary total power losses of the switches might well exceed 4-5W and cannot be handled by conventional IC package.

VII. Conclusion

Driving an N-channel-FET with floating source potential is a demanding task, which calls for a high common-mode voltage level shifter. This work introduces a cost-efficient discrete solution, capable of 10+ bits of PWM dimming resolution. Attention has to be paid to the LED peak current ratings, which may degrade the performance of the circuit due to the need for additional Miller capacitors. Still, the presented solution enables a scalable matrix light concept with improved thermal performance.

The proposed N-FET driver circuit is not restricted to LED applications only. It can serve well in light bulb drivers, motor controllers, half-bridge drivers and many other applications, where driving a low-gate charge, floating high-side N-FET is required.

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Design of a Digitally Controlled Boost Converter for Automotive Headlamp Applications

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Abstract – **A voltage-mode boost converter for automotive (primarily LED headlamp) applications with DSP digital control is presented in this paper. A lean digital control design procedure is proposed. The transfer function of the boost converter's power plant is derived and a three-pole three-zero (3p3z) compensator is designed in MATLAB. The 3p3z-compensator is translated into the z-domain and implemented on a microcontroller with DSP core. A prototype boost converter is designed, built and thoroughly investigated. The performance of the tuned boost controller is evaluated in terms of stability, steady-state precision, transient response and efficiency.**

Keywords – **Automotive, Boost Converter, Digital Control, 3p3z-Controller, MATLAB, Control Loop Stability, Bode Plot**

I. Introduction

The presented boost converter targets the link voltage generation in an automotive LED headlamp control unit. The concept of cascaded boost and buck converters combines the advantages of both topologies – low ripple at input and output of the unit, reduced EMC emissions, excellent load- and line regulation. The block diagram of the LED headlamp control unit is presented on Fig. 1.

The LED current regulation takes place in the buck converter stage, for instance similar to the one described in [1], while the input voltage of the buck converter supply voltage is held at a constant level by the proposed boost converter. The output voltage of the boost converter in this configuration must be higher than the sum of the maximum LED string voltage and the headroom required for the normal operation of the buck converter. The output power of the boost converter must be greater than the total output power of all LED strings plus the power losses in the buck converter stages. The presented boost converter has been designed for 45W output power and 45V output voltage. A digital control algorithm, implemented on a DSP microcontroller (Microchip dsPIC33-series) allows for flexibility and adaptive digital control functionality.

II. Goals and Tasks

The goal of this work is to select a cost-efficient boost control concept, suitable for the high-volume automotive market and establish a lean digital control design procedure which ensures solid performance in terms of stability, control speed and precision. A prototype of the digital boost converter will be designed and thoroughly investigated with the aid of the proposed methodology.

III. Model of the Proposed Boost Converter

The power plant of the proposed boost converter can be modelled with the power components *L, C,* their parasitics r_L, r_C, the active components *Q, D* and the equivalent load resistance *R* (Fig. 2). The basic operation principles of the boost converter have been thoroughly investigated and referenced in various sources, e.g. in [4] and are out of the scope of this work. After comprehensive research, a voltage-mode (VM) boost control scheme has been chosen in favor of the current-mode control since the later requires more sophisticated control algorithm with continuous switch current evaluation and an artificial slope compensation ramp for suppressing the sub-harmonic oscillations which might occur at duty cycles greater than 50% [2], [3]. The voltage-mode control does not require slope compensation, but the power plant behaves as a second-order system due to the presence of two reactive components with a well-pronounced resonance peak in its

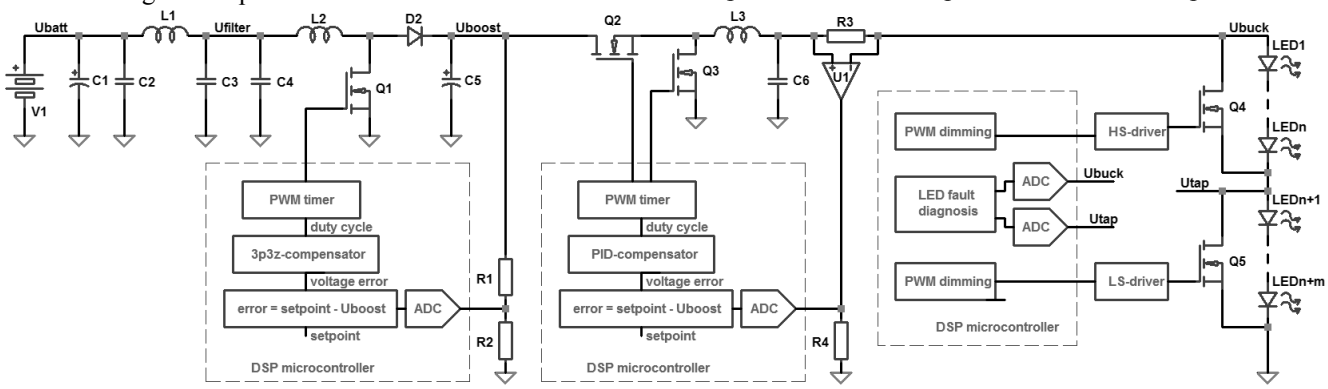

Fig. 1. Block Diagram of a digitally controlled headlamp ECU

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open-loop transfer function. Care must be taken that the crossover frequency of the voltage-mode controller is set much higher than the native resonance frequency of the power plant.

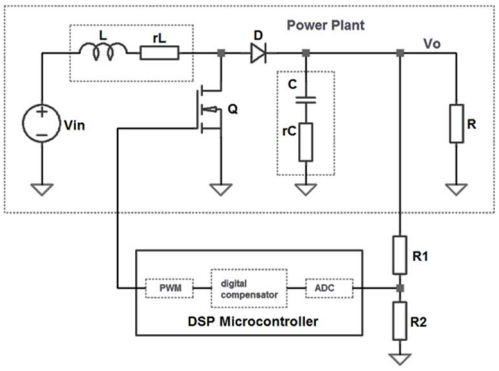

Fig. 2. Proposed boost converter with digital control

A. Component Choice

In accordance with the LED headlamp system demands, the requirements for the boost converter are summarized in Table 1.

TABLE 1. BOOST CONVERTER PARAMETERS

Boost Converter Parameters	Value
output power, max.	45W
output current, max.	1A
supply voltage , min.	9V
supply voltage, max.	20V
efficiency, min.	85%
switching frequency	215kHz...255kHz
controller x-over frequency	3.8kHz

The design procedure for the boost power plant has been carried out in accordance with [5] and following components have been selected: power inductor 22µH IHLP5050 by Vishay, power FET BUK9Y25-100 by NXP, power diode SS8PH100 by Vishay, gate driver IR4427S by Infineon and a 39µF polymer output capacitor HHXA800ARA390 by United Chemi-Con.

IV. BOOST CONTROLLER DESIGN

The transfer function of the boost converter power plant can be extracted from [4]:

$$G_{dv}(s) \approx \approx \frac{V_{in}}{(1-D)^2}\frac{-s^2\frac{1}{\omega_1\omega_2}+s\left(\frac{1}{\omega_1}-\frac{1}{\omega_2}\right)+1}{s^2\frac{1}{\omega_O{}^2}+s\frac{1}{Q\omega_O}+1} \quad (1)$$

where

$$\omega_1=\frac{1}{R_C C},\ \omega_2\approx\frac{(1-D)^2R-R_L}{L} \quad (2)$$

$$\omega_O\approx\frac{1}{\sqrt{LC}}\sqrt{\frac{(1-D)^2R+R_L}{R}},\qquad Q\approx\frac{\omega_O}{\frac{R_L}{L}+\frac{1}{C(R+R_C)}} \quad (3)$$

The derived transfer function of the power plant can be simulated in MATLAB, using the parameters of the boost components in Table 2.

TABLE 2. MATLAB SIMULATION PARAMETERS

Simulation Parameter	Value
Vin	10V
Vout	45V
D	0.78
Iout	1A
R	45Ω
L	22µH
RL	33mΩ
C	39µF
RC	0.55Ω
FS	250kHz
TS	4µs
Gain(FB)	0.053

The Bode plot of the open-loop system indicates the resonant peak, typical for a second-order system, at 1.21kHz (Fig. 3).

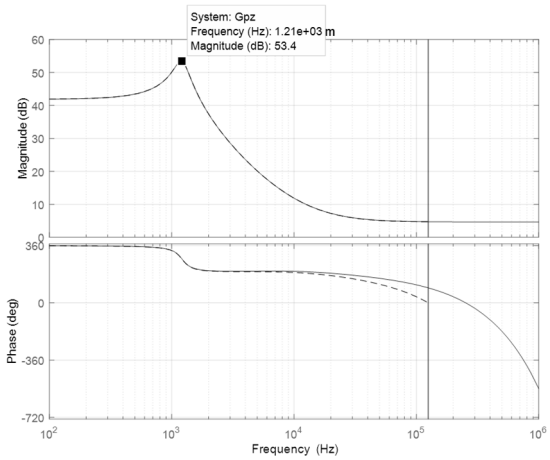

Fig. 3. Bode plot of the boost converter power plant (MATLAB simulation)

A. 3p3z-Controller: analog design

The VM power plant requires a compensator with two zeros for resonant peak compensation, a third zero at origin for proper DC gain definition, one pole for the output ESR zero compensation and a second pole for high-frequency attenuation. According to multiple references [6], [7], a 3p3z - compensator (also known as "compensator type III") is the proper choice for a voltage mode controlled boost converter. Its transfer function is

$$H(s)=\frac{\omega_{P0}}{s}\frac{(\frac{s}{\omega_{Z1}}+1)(\frac{s}{\omega_{Z2}}+1)}{(\frac{s}{\omega_{P1}}+1)(\frac{s}{\omega_{P2}}+1)} \quad (4)$$

For a fast and lean design of a 3p3z-compensator the authors of this work propose following design procedure:

1. Place two zeros around the resonant peak at 1.21kHz, to compensate for the double pole.
2. Place one pole at the Nyquist frequency at 120kHz to provide high-frequency attenuation.
3. Place one pole at the ESR frequency at 11kHz to improve the phase margin.
4. Place the pole of origin at low frequency, around 60Hz in order to adjust the crossover frequency to approx. 4kHz.

The choice of the crossover frequency f_C is governed by the stability considerations. f_C must be much higher than the power plant resonant frequency f_{LC} .On the other side, f_C shall be much lower than the right half-plane zero frequency f_{RHP}. Following condition can be considered as a good estimation:

$$3f_{LC} \leq f_C \leq 0.3f_{RHP} \tag{5}$$

Using the component values from Table 2, the frequencies f_{LC}, f_{RHP} can be calculated:

$$f_{LC} = \frac{V_{IN}}{V_{OUT}} \frac{1}{2\pi\sqrt{LC}} = 1.208kHz \tag{6}$$

$$f_{RHP} = R\frac{(1-D)^2}{2\pi L} = 15.764kHz \tag{7}$$

Thus, a crossover frequency of approx. 3.7kHz fulfills the requirement (Equ. 5) and shall be targeted. For proper pole/zero placement and closed loop response optimization the Sistool/MATLAB module has been used (Fig. 4).

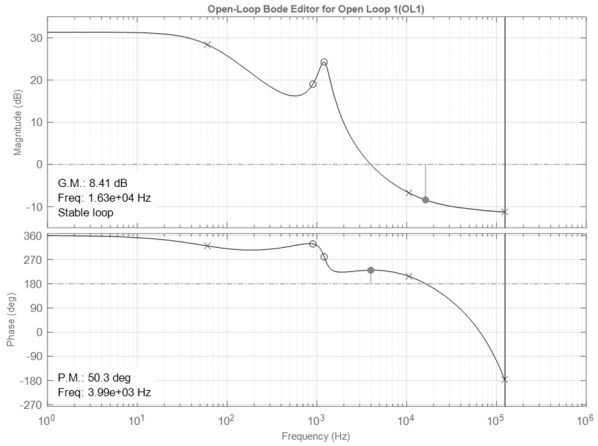

Fig. 4. Bode plot of the compensated boost converter with closed loop digital control (MATLAB simulation)

The calculated closed loop response indicates a phase margin of around 50°, crossover frequency of 4kHz and gain margin >5dB, thus promising a stable regulation and fast load step response. The positions of the calculated poles and zeros are summarized in Table 3.

TABLE 3. POLE & ZERO LOCATIONS

3p3z-Parameters	Value
f_{P0}	60.4Hz
f_{P1}	10.6kHz
f_{P2}	124kHz
f_{Z0}	0.903kHz
f_{Z1}	1.21kHz
$Gain$	0.151

B. 3p3z-Controller: digital design

In order to translate the compensator design form the continuous s-domain into the digital z-domain, the Tustin transform [8] hast to be applied:

$$H(z) = \frac{d(n)}{e(n)} = \\ = \frac{B_0 + B_1 z^{-1} + B_2 z^{-2} + B_3 z^{-3}}{1 + A_1 z^{-1} + A_2 z^{-2} + A_3 z^{-3}} \tag{8}$$

Thus, the differential linear equation can be derived:

$$\begin{aligned} d[n] = B_0 e[n] + B_1 e[n-1] \\ + e[n-2] + B_3 e[n-3] \\ - A_1 d[n-1] - A_2 d[n-2] \\ - A_3 d[n-3] \end{aligned} \tag{9}$$

This recursive equation can be easily implemented on a microcontroller by storing the last three successive errors and duties in arrays and multiplying them with the A, B coefficients (Fig.5).

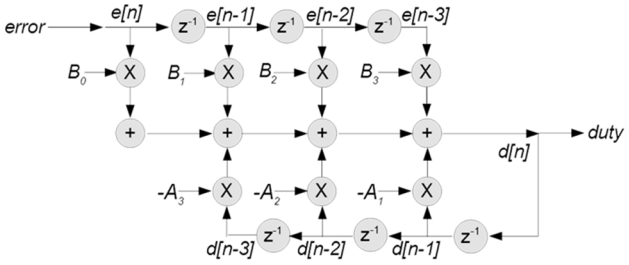

Fig. 5. Flowchart of a digitally implemented 3p3z-controller

The derivation of the compensator coefficients A_X, B_X can be accomplished with the aid of the DCDT-Tool by Microchip [9].

V. EXPERIMENTAL EVALUATION

A. Static Operation

The experimental boost converter prototype delivers continuous 45W output power, 45V output voltage with 0.8% offset error. The execution time of the 3p3z-algorithm is 2µsec - short enough to guarantee a PWM update in every switching cycle and thus - minimum phase margin deterioration (Fig. 6).

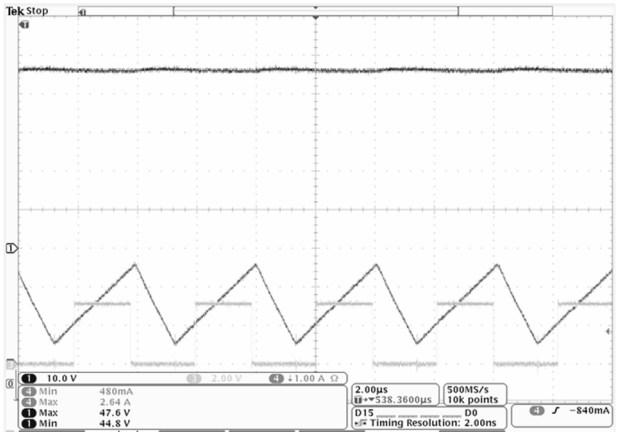

Fig. 6. Static operation of the compensated boost converter. Output voltage (1st trace), inductor current (2nd trace), 3p3z-controller execution time (3rd trace)

B. Load Step Response

The step response is investigated by stepping the output power rapidly between 20W and 40W (Fig. 7). Due to the limited output capacitance, an under-shoot (~1V) can be observed. The step response is well behaved and damped – a fact that indicates a sufficient phase margin.

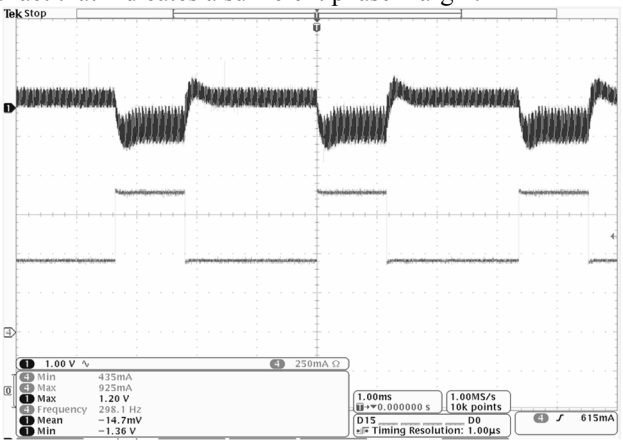

Fig. 7. Dynamic operation of the boost converter. Output voltage step response, 1Vac (1st trace), load current (2nd trace)

C. Closed Loop Stability

The stability has been investigated with the Bode 100 vector network analyzer [10] in a classic analysis approach based on a sine sweep signal injection in the feedback loop. The measured closed loop response (Fig. 8) reveals a good phase margin of 53° and a crossover frequency of 3.8kHz. The gain crosses the 0dB-axis with shallow -20dB/dec-slope, the gain margin is >10dB.

D. Efficiency

The efficiency of the prototype boost converter has been measured with resistive load, adjusted for 10W and 40W output power at 10V and 20V supply voltage. The efficiency ranges from 85.4% to 92.1%, depending on operation point. A synchronous boost topology as the one described in [11] can further improve the efficiency on the expense of an increased cost and complexity.

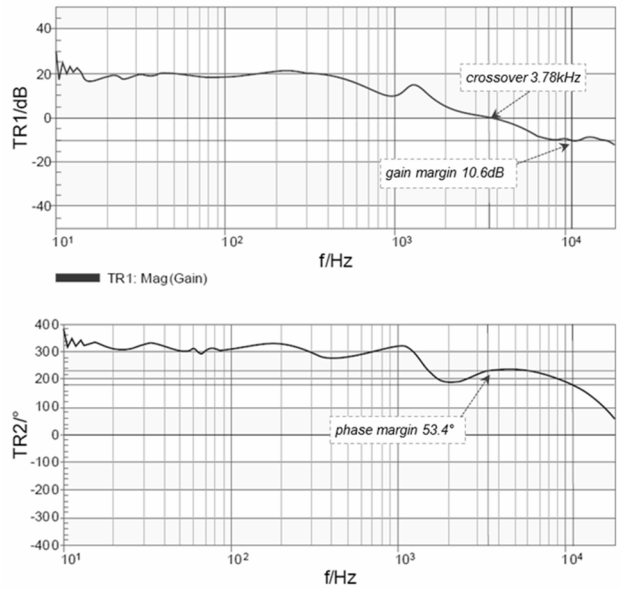

Fig. 8. Bode plot of the compensated boost converter with closed loop digital control (measured with network analyzer)

VI. CONCLUSION

The proposed digital boost converter performs up to expectations. The static offset is merely 0.8%, the stable regulation loop with 53° phase margin and fast settling time of ~250µs easily meet the goals of this work and prove the plausibility of the contributed design procedure. The proposed digital design allows for fast and flexible control coefficient adaptation for shaped loop response during start-up, dynamic load, static operation, shut-down conditions or to compensate for component ageing.

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Methods and Power Converters for Charging/Formation of VRLA Batteries

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Abstract – **This paper looks at the different requirements when designing power converters in applications involving charging/ formation of lead- acid batteries. For this reason, it first reviews the known methods and proposes a new classification, based on the number of independently set parameters for the process.**

Based on the classification it is noted, that a power converter that has the ability to charge or discharge a battery, along with accompanying software to enable the user to implement a custom charging algorithm is able to implement most of the types of mentioned charging/formation techniques. The design of such a converter, capable of delivering up to 600W is presented, after a short review of the possible power topologies that can be used to implement it.

Keywords – **Reflex charger, Pulse Charging, VRLA Battery Charger, Power electronics, Power converters, Charging, Formation**

I. INTRODUCTION

Electricity is the most convenient and versatile carrier of energy. However, its ability to be stored locally and used on demand is very limited. For his reason the appropriate construction and use of mobile power sources, more specifically, batteries can provide an important link between the primary source of energy and its actual use. Their formation and exploitation heavily depends on the appropriate construction of flexible power converters. As a case in point pulsed charging, with variable duty ratio, has been shown to improve the quality and charging time during the formation (the first charge) of lead-acid batteries [1]. In addition, the same approach has been shown to be a superior algorithm for their recharging, leading to increasing both charge time and reducing capacity loss [2].

The use of such algorithms to better exploit the energy source is only possible by using a specialized power converter. For this reason, the paper covers the main requirements and possible solutions, during the design and construction of such a power converter.

Although, similar in some aspects the first charge (or formation) and the recharge of a battery have some specific requirements that are mentioned, were appropriate.

The paper organization is as follows: In section II, a new classification of the charging methods is proposed. It is based on the number of independently set parameters during the process. This sets the stage for the basic requirements for an intelligent battery charger, which should be able to be software reconfigurable to implement the most general set of algorithms. In section III the applicable power topologies are reviewed, that can be used to design such a converter. Section IV presents the constructed 500W intelligent charger, capable of implementing reflex, pulse or constant current charging. In Section V some concluding remarks are mentioned.

II. CHARGING/FORMATION TECHNIQUES

There is a lot of different algorithms that can be used to charge batteries: constant voltage, constant current, two or more steps constant voltage or current charging, pulse charging and reflex charging [3]–[6]. This standard classification discusses only the desired feedback signal to control the process. Using this feedback the power converter can be modeled as a variable current or voltage source that feeds the battery. The simplest algorithms just implement one of the two possible variants, while the more advanced ones have more phases during the charge process.

However, the charging algorithm can be viewed from a different perspective that involves the amount of parameters independently adjusted to obtain the desired charging algorithm. If based on these criteria the available techniques are shown in Figure 1. The amount of parameters that can be set excludes any parameters that are used to signal the end of the process, because they are needed in any implemented algorithm.

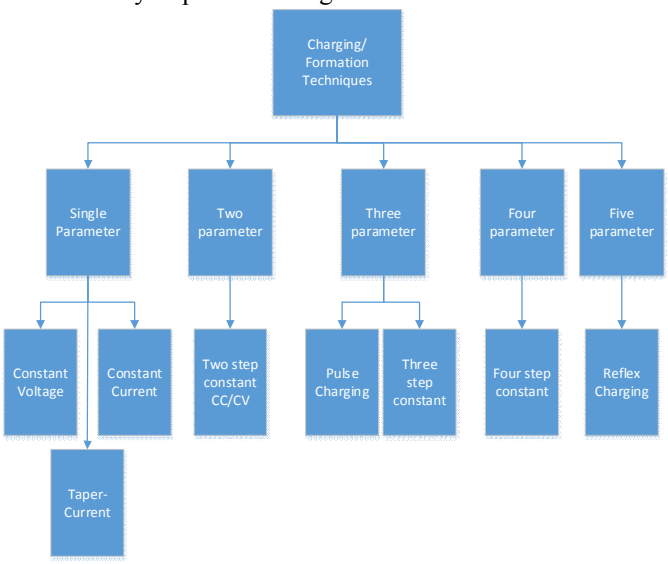

Figure 1 – Charging/Formation techniques classification according to the number of independently set parameters

Possible parameters for determining the end of the charging process are based on fixed time for the whole process, erivative of the battery voltage and current or the Ah input [4], [5].

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II.1. Single parameter charging Techniques

These are the simplest charging methods, where the algorithm can set only the charging current or voltage. It should be noted however, that in practice these methods are difficult to implement using only a single independent parameter. For example when using constant voltage charging, there must be a current limit, and in the constant current case, some upper limit on the battery voltage must be set. Nevertheless, they are classified as single parameter methods. Here we can also mention the taper-current charging, where the parameter is the load resistor [5]. Figure 2 shows some typical waveforms. These methods can be used in both formation and recharging of batteries with small modifications.

There are some very significant disadvantages when using these methods for charging [3],[5] or formation of batteries [6]. By controlling a single parameter, the process cannot be optimized for charge/formation time and battery temperature. The need to independently set more parameters is obvious.

II.2. Two parameter charging Techniques

The constant current initial charging and then constant voltage phase is the typical two parameter algorithm for recharging. Here the voltage and current of the two phases can be independently set. A typical waveform is shown in Figure 3. For the formation of VRLA batteries a two-step constant current charging profile can be classified as a two parameter technique [6].

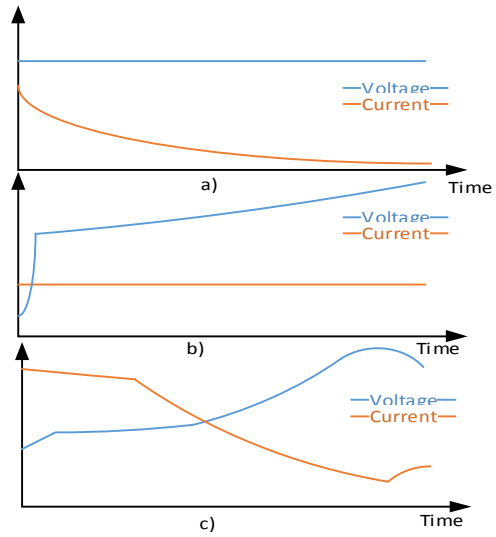

Figure 2 Single independent parameter methods
a) Constant Voltage, b) Constant Current, c) tapper-current

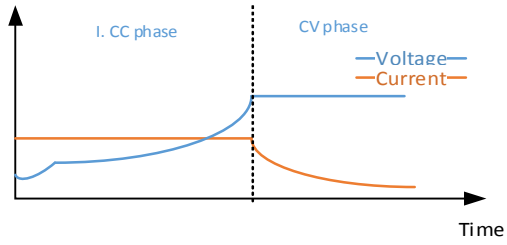

Figure 3 Two parameter recharging of VRLA batteries

II.3. Three parameter Charging Techniques

There are two main variants of this family. The first one relies on constant charge with different phases, while the second involves periods where the current is zero, or pulsed charging

For the first family constant current/ constant over voltage/ constant voltage (IUoU) recharging is shown in Figure 4.

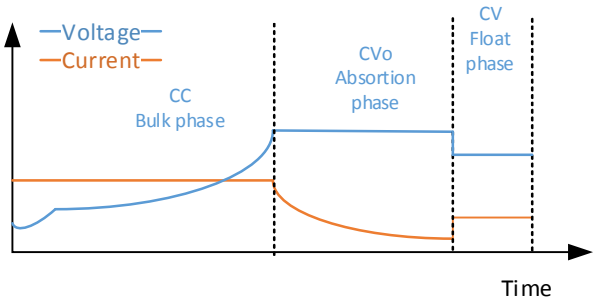

Figure 4 Three Parameter Constant current/Constant over Voltage/Constant Voltage Recharging technique.

There are some variants of this technique, including the IUI algorithm [5].

The second approach to fixing three independent parameters is the pulse charging method, where we can independently set the period, duty cycle and max current of the process. This is applicable to both the formation and charging of batteries. The reflex charging principle is a generalization of this principle, adding also a discharging phase.

II.4. Four Parameter Charging Techniques

Some manufacturers of AGM VRLA argue that a fourth step with even lower float voltage will increase the battery life [7], while some integrated circuits offer the possibility of a fourth equalization stage with even higher voltage before then the absorption [8]. It used for batteries that are not sealed, because of the gassing, but it is suggested that this eliminates the sulfates on the electrodes. Also, the multi- step voltage limited constant current charge can also be included in this category [5], [9].

II.5. Five Parameter Charging Techniques

This category includes the most complex charging/ formation technique, called reflex charging. It can independently set the charge (I1) and discharge (I2) current, charge, discharge and pause time (T1, T2 and T3 respectively). It is possible to implement the Constant current, and pulse charging as particular cases. A generalized waveform is shown in Figure 5. It is argued that this approach when used for charging or formation of batteries can lead to optimization of the charging time, battery temperature, and in the case of formation efficiency of the process [1],[2], [10],[11].

In practice, there can also be an additional pause after the charge and before the discharge, which can be considered as an additional parameter, but this will not be classified independently. The practical realization of a power converter achieving this algorithm will be covered next.

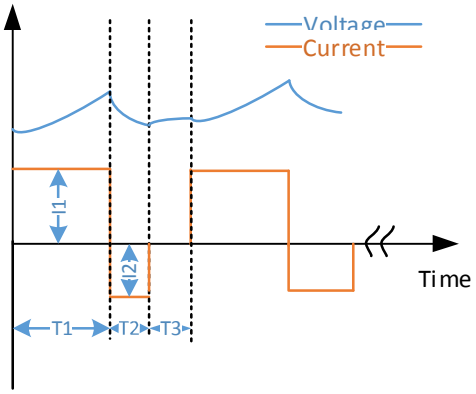

Figure 5 Five Parameter Reflex Charging

III. POWER CONVERTERS FOR REFLEX CHARGING

The power topologies that can be used to implement reflex charging, powered from single phase ac grid are divided into two groups, with some typical realization given for both of them. The three phase variants are similar.

The first group consists of variants that are capable of recovering the energy, generated during discharge cycle into the ac grid. The two principle block diagrams of such a power converter are shown in Figure 6. The simpler block diagram consists of a single bidirectional ac/dc converter that can work in both I and II quadrant. This can be realized with a dual bridge SCR rectifier is shown in Figure 7. It is a reliable technology still in use, especially for lager power levels of the charger.

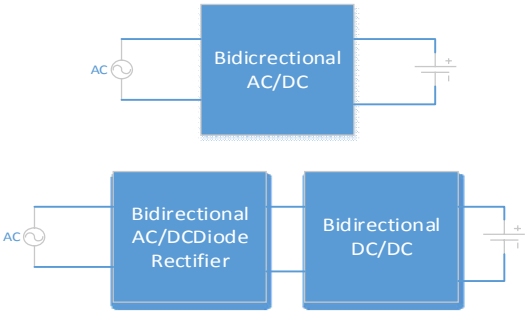

Figure 6 – Regenerative reflex chargers

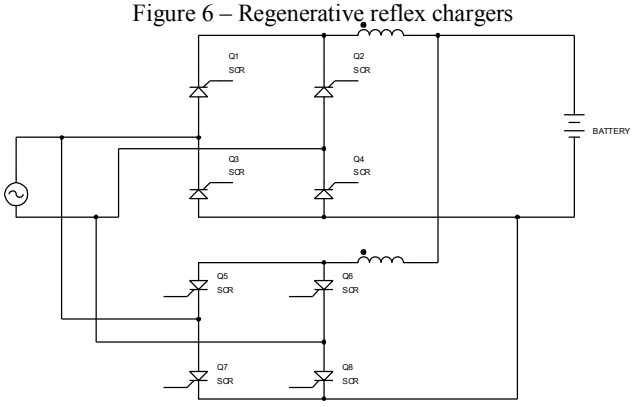

Figure 7 Single bidirectional ac/dc converter for reflex charging

The variant consisting of separate bidirectional ac/dc converter and dc/dc converters has many different realizations for each of blocks. Some of them for the dc/dc converter are given in [12], [13], [14], and a review of the single phase bidirectional ac/dc converters can be found in [15]. Figure 8 shows a typical schematic.

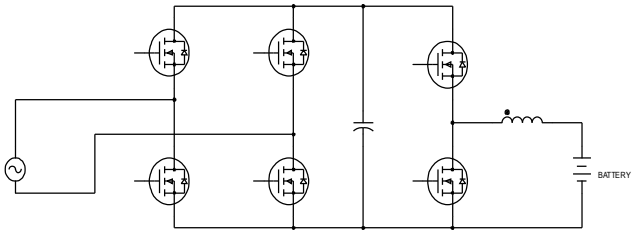

Figure 8 – Two stage standard regenerative reflex charger

The second group is consisting of reflex chargers that are dissipating energy in the discharge cycle in a resistive load, as shown in Figure 9 . Despite its energy inefficiency, it is a plausible variant, when the converter nominal power is not large (<1kW). In these cases, the added complexity for recovering the energy is not necessary. The designed converter in the next section is based on this diagram.

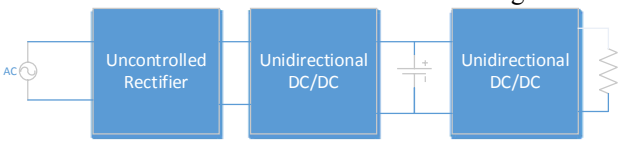

Figure 9 – Dissipative reflex charger

IV. DESIGNED REFLEX CHARGER

The designed reflex charger is with the following parameters:

- Output voltage U=12- 60V – for the individual formation of up to 4 VRLA batteries
- Reconfigurable Charge current of Ic 0-10A,
- Reconfigurable Discharge current Idisch 0-5A
- Charge time: 0s to 96hours
- Discharge time:0s to 30s
- Pause time after charge or discharge: 0s to 30s,
- Fixed time or derivative end of the charge process

The additional software on the PC also shows the current and voltage for each connected battery, while calculating in real time the delivered capacity [Ah] and energy [Wh] for each battery.

The main window of the program is shown in Figure 10, while the dialog for setting the parameters of a particular charging process is shown in Figure 11.

The user can independently set the required parameters for the available programs:

- Charge only process with fixed time duration
- Pulse charging with fixed duration of the charge and pause times.
- Fixed time discharge process
- Reflex charging with fixed duration of the charge, pause after charge and discharge and discharge time

An additional option, as an alternative to fixed duration of the charge time value during reflex or pulse program is to measure the derivative of the battery stack voltage and while it is below a value set in the program configuration to keep the charging.

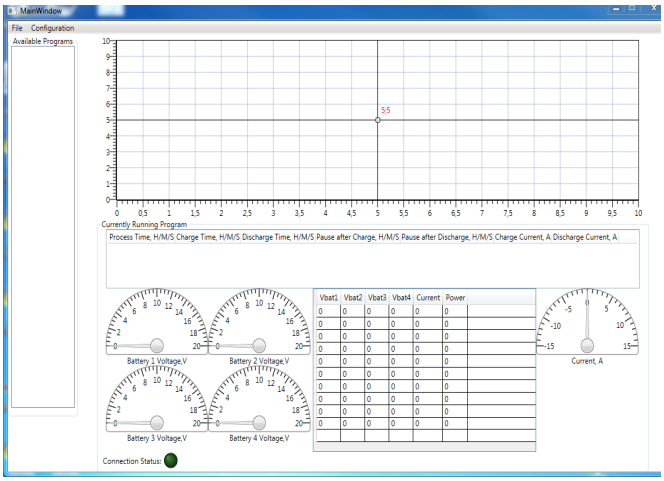

Figure 10 Main Program Window

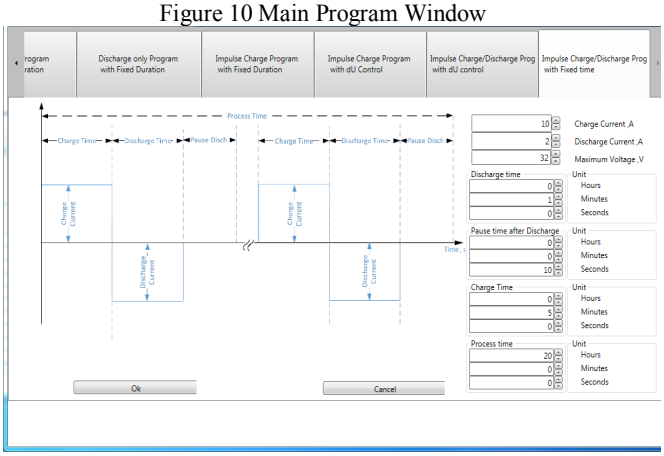

Figure 11 Program parameters for a reflex charge program

Block diagram of the whole charger is shown in, and the final designed prototype in Figure 13.

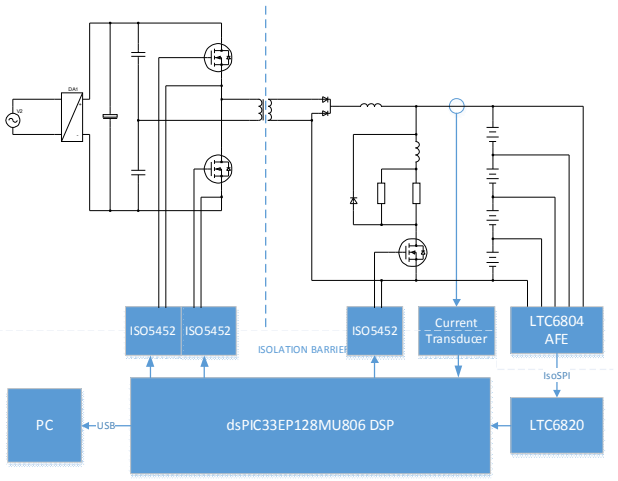

Figure 12 Designed Reflex Charger

V. CONCLUSION

The paper reviewed the main algorithms used in the charging/formation of VRLA batteries. A new classification was proposed, based on the amount of independently set parameters during the charging process. As the reflex method has five independent parameters that can be set it is the most advanced method. A power converter that can realize reflex charging, can be adopted for some of the other methods. The various power topologies that can be used to design such a charger were briefly mentioned, and a realization was proposed, along with the software customizations possible for its operation.

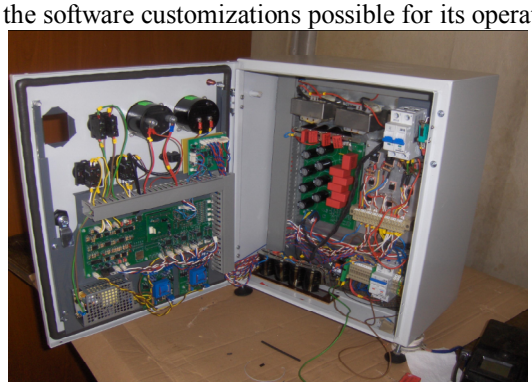

Figure 13 – The designed power converter for reflex charging

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Influence of asymmetry in multiphase resonant converters for energy storage systems

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Abstract – **The following paperwork presents an investigation of multiphase converter for charging energy storage elements (ESE). The converter is studied with asymmetry in one of the units. Basic relations for the impact of the values of the elements in one of the units have been made. The shown relation can be used for reporting the loading change of the different units when there is an asymmetry in one of them.**

Keywords – **DC-DC converters, energy storage, multiphase converter, asymmetry.**

I. Introduction

For charging of energy storage elements different converters can be used [1, 2, 3, 4]. The converters which can work with load changing in wide ranges are the resonant inverters with voltage limitation over the commutating capacitor (RIVLCC) [2, 3, 5]. Different circuits of RIVLCC have been tested. When there is an asymmetry in one of the units the loading of the others changes too.

II. Modeling of a Three-Phase Converter for Charging of Energy Storage Elements

The block diagram of the converter for charging ESE is presented in fig. 1. It consists of three stage (DC-AC converters), three transformers [6, 7] and rectifier. The circuit of the converter and the rectifier are shown on fig. 2 and fig. 3.

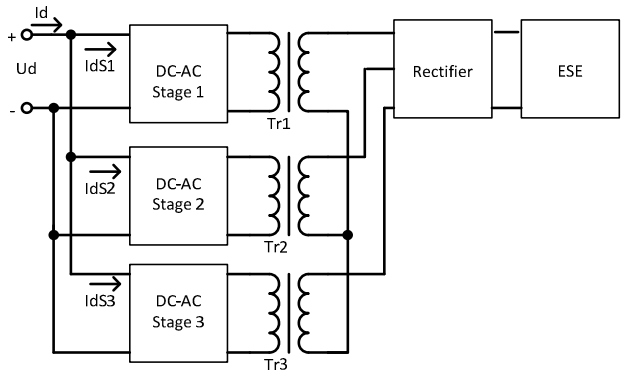

Fig. 1. Three-phase converter for charging ESE.

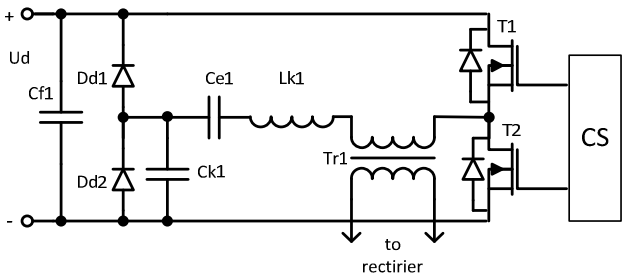

Fig. 2. Resonant converter circuit.

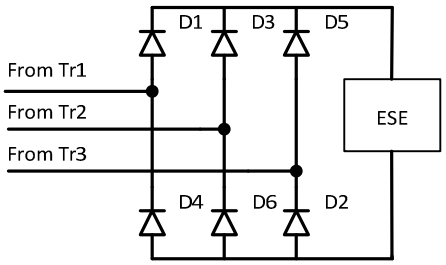

Fig. 3. Rectifier circuit.

The principle of operation of this converter is explained in [2]. The ESE is supercapacitor or rechargeable battery.

III. Modeling and Simulation Results

For studying the converter in figure 1 a model in LTspice has been developed. The values of L_k and C_e in the first unit are changed in the range ±20%. The current and the voltage in the separate units of the converter are taken into account.

Figure 4 and 5 shows the results from the simulation of the converter.

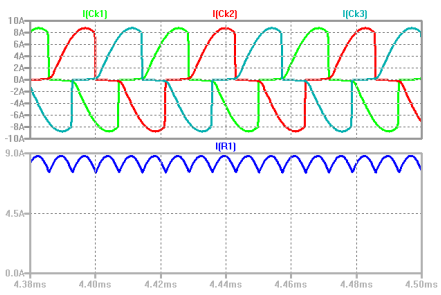

Fig. 4. Current through capacitors Ck1, Ck2 Ck3 and through ESE at identical parameter of components.

Figure 4 shows the currents through the capacitors Ck1, Ck2, Ck3 (capacitors from the three different units, which

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are used for limitation of the voltage). I(R1) is the current through the shunt resistor which is series connected with the energy storage element (current through ESE).

Figure 5 shows the currents through the rectifier diodes D1, D3 and D5 and the current through the ESE for equal elements in all three units.

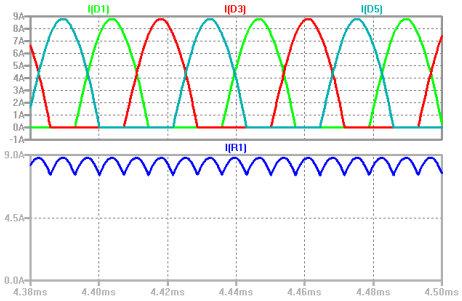

Fig. 5. Currents trough the rectifiers diodes and ESE, at identical parameter of components.

Figure 6 shows the currents through the capacitors C_{k1}, C_{k2}, C_{k3} and the current through the ESE for value of L_{k1} 20% higher than the values of L_{k2} and L_{k3}).

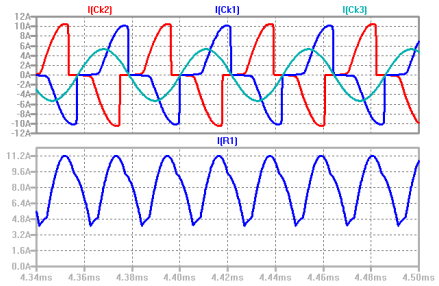

Fig. 6. Current through capacitors C_{k1}, C_{k2} C_{k3} and through ESE at different value of the L_k.

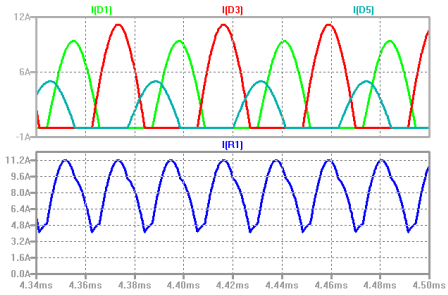

Fig. 7. Currents trough the rectifiers diodes and ESE, different value of the L_k.

Figure 7 shows the currents through the rectifier diodes D_1, D_3 and D_5 and the current through the ESE for L_{k1} 20% higher value then L_{k2} and L_{k3}.

During the simulation studies the values of the L_k and C_e are changed and the following parameters are measured:

- average value of the input current Id;
- average value of the input currents through the separate units: IdS1, IdS2 and IdS3;
- average value of the current through the ESE: I_ESE;
- ripple ratio of the current through the ESE: Kr;
- maximum value of the current through the same transistor for all three units T1, T3 and T5: IT1m – IT5m;
- maximum value of the current through the reverse diodes (reverse diodes of transistors T1, T3 and T5);
- maximum value of the current through the limitation diodes from all three units Dd1, Dd3 and Dd5 – IDd1, IDd3 and IDd5;
- average value of the current through the rectifier diodes D1, D3, D5 – ID1av, ID3av, ID5av;

Figure 8 to figure 13 shows the relation of the currents through the components when the value of C_e changes in the range ±20%. The results are presented in relative units. The values with index "r" are the values of the currents divided to the value of the same current, obtained for equal values of the components in all three units.

IV. Results

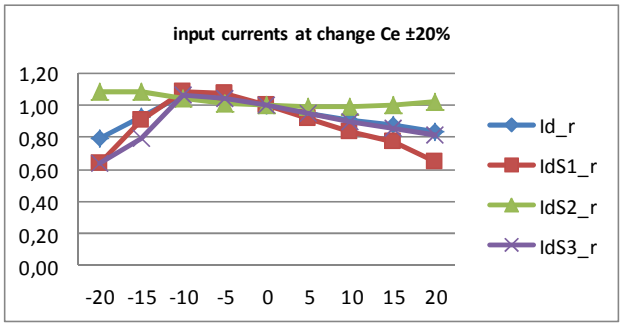

Fig. 8. Currents at change of C_e.

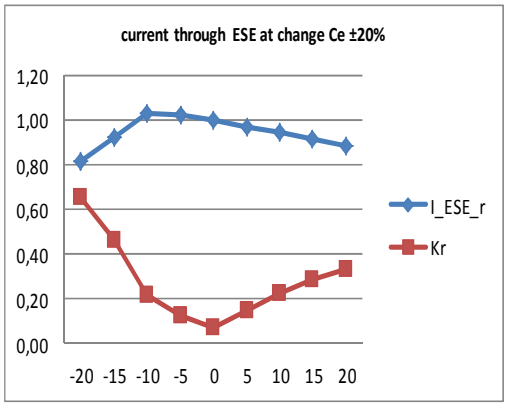

Fig. 9. Currents at change of C_e.

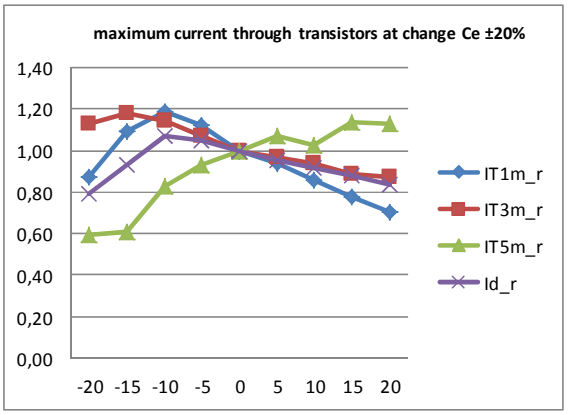

Fig. 10. Currents at change of C_e.

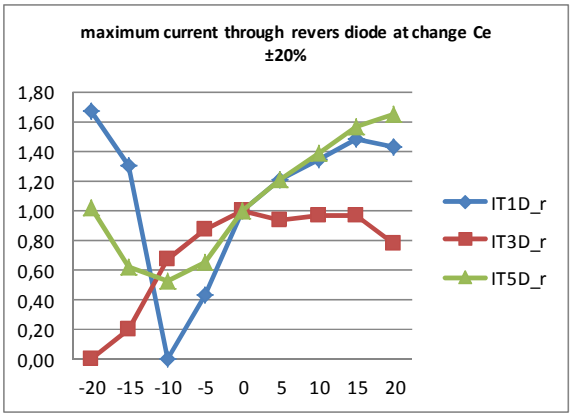

Fig. 11. Currents at change of C_e.

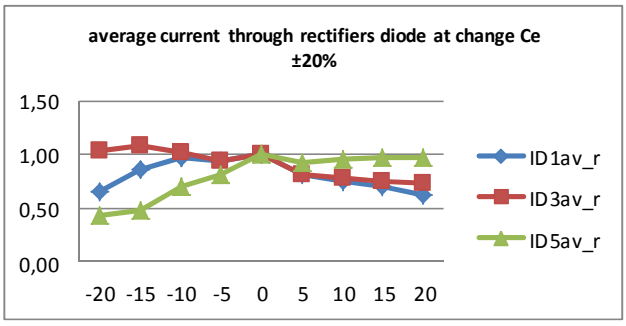

Fig. 12. Currents at change of C_e.

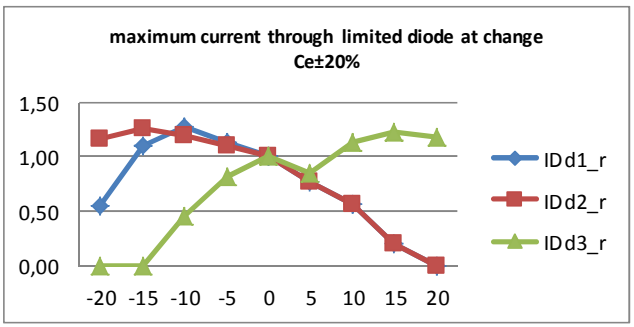

Fig. 13. Currents at change of C_e.

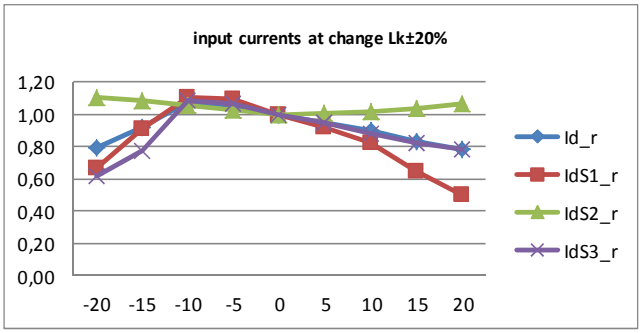

Fig. 14. Currents at change of L_k.

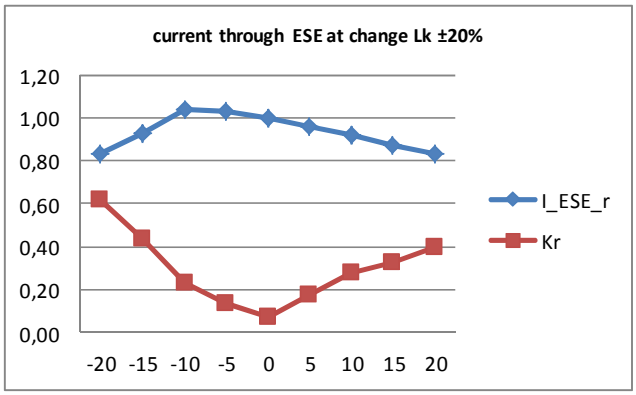

Fig. 15. Currents at change of L_k.

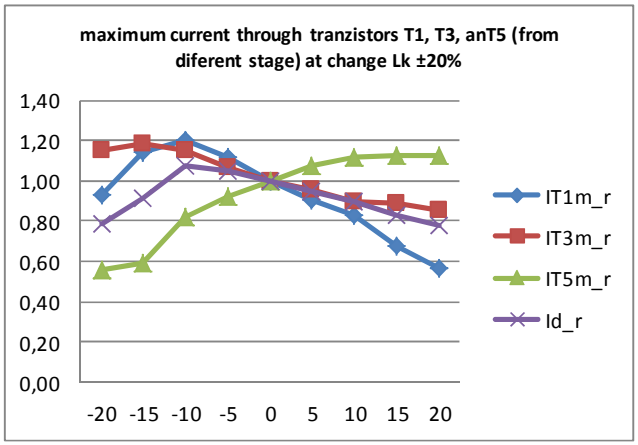

Fig. 16. Transistor T1 voltage rising edge for a synchronous converter.

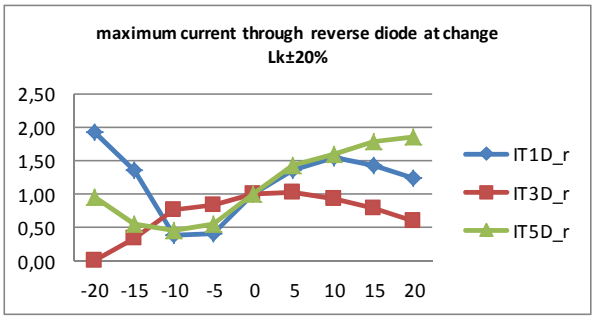

Fig. 17. Currents at change of L_k.

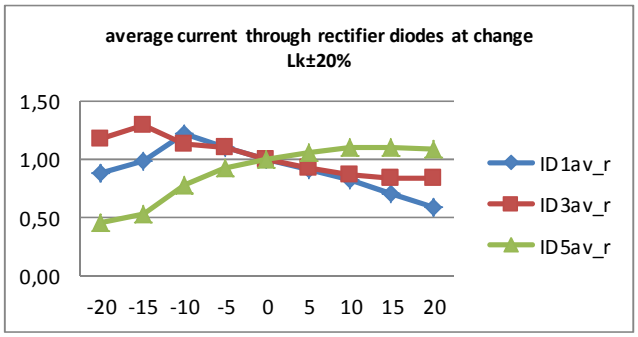

Fig. 18. Currents at change of L_k.

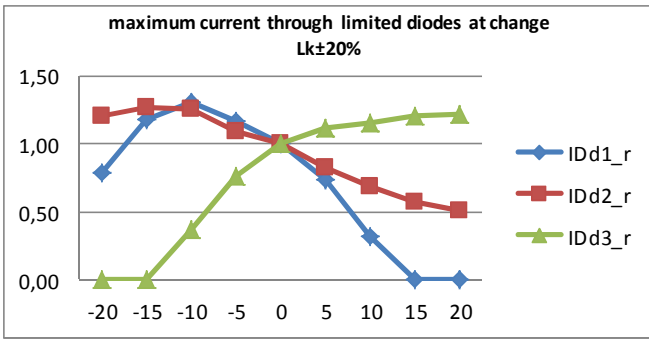

Fig. 19. Currents at change of L_k.

V. CONCLUSION

The carried out study of the impact of asymmetry in units of a multiphase converter for charging energy storage elements gives opportunity to evaluate the properties of this kind of converters.

The created relations in relative units can be used for the designing of the studied converters. From these characteristics the overloading of the components can be determine. Also the change in the provided energy in the load can be determined.

From the shown relations for the ripples of the current through the ESE in figures 9 and 15 it can be seen that the ripples highly depend on asymmetry. Therefore for ESE which needs less ripples of the current through them filter elements must be used.

Likewise it can be seen that overload of the components in the separate units is around 20%. That can be seen from the created characteristics in relative units. Exception makes the current through the reverse diodes of the transistors. This is so because the working regime of the inverters changes because some of the units of the starts working in under or above the resonant frequency. The difference between the working and the resonance frequency can be too high.

From the graphics on figures 13 and 19 (maximum value of the current through the limitation diodes) it can be seen that as a result of the asymmetry the limitation diodes from one of the units dose not conduct. This means that this unit works in regime without limitation of the voltage over the commutating capacitor. This working regime is different from the nominal. This can be also seen from the waveforms from figure 6 (current through the capacitor of the third unit - C_{k3} – I(Ck3)).

The simulation results are confirmed with experiments.

ACKNOWLEDGEMENTS

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Design of Induction Motor Drive with Parallel Quasi-Resonant Converter

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Abstract – **A parallel quasi resonant DC link converter for induction motor drive application is analyzed and designed. The proposed soft-switching inverter is formed from the traditional pulse-width modulated (PWM) inverter by simply augmenting with auxiliary resonant circuits, and the soft switching is achieved through applying PWM switching control signals with suitable delays for the switches. The designed soft-switching inverter is used for powering an induction motor drive which is connected to drive the constant nominal load. The converter is designed to achieve the maximum voltage gradient and simultaneously to have low peak current and voltage stresses on the devices and thereby to reduce the losses.**

Keywords– **Induction Motor Drive, Parallel Quasi Resonant DC Link Converter**

I. INTRODUCTION

Variable speed drives using induction machines require power electronic circuits that are capable of producing sinusoidal voltages of varying frequency and magnitude [1]. The control of adjustable speed drives is done by the power converters. In hard-switched power converters switching losses limit the applicable switching frequency. Switching with large du/dt reduces the switching losses. Bigger voltage gradients combined with long feeders lead to high frequency parasitic effects, like over voltages at motor terminals, high common mode ground current, bearing currents, etc. In addition, electromagnetic interference increases and efficiency decreases. To overcome these problems, the application of soft switching techniques is essential [1-6].

The resonant DC-link inverter is the most commonly used one for induction motor drives, owing to its simplicity, but it possesses the disadvantage of having a high resonant link voltage, which is equal to or greater than twice the supply voltage [2].

Quasi-resonant (QR) inverters offer several advantages compared with resonant DC-link inverters with regard to resonant link design and control, device rating requirements and use of pulse width modulation (PWM) [3]. The QR inverter schemes generate zero-voltage instants in the DC link at controllable instants that can be synchronised with any PWM transition command, thus ensuring a zero-voltage switching condition of inverter devices. As a result, these inverters can be operated at high switching frequencies with high efficiency [3].

A number of discontinuously resonant link circuits employing a parallel resonant link arrangement in conjunction with additional switches have been reported in the literature [1-8]. These have in common that the resonant link is only active when the bus voltage has to be reduced to zero in order to commutate the inverter switches. Two distinct advantages can be identified. The voltage across the dc link is resonated from supply voltage level down to zero, hence, the voltage stress for the inverter devices never exceeds the supply voltage. A resonant cycle can be initiated at any time which enables inverter switching at any desired instant.

These inverters can be designed not only for the soft switching but also for the voltage gradient reduction. In addition to switching loss reduction, the resonant circuit undertakes the filter's task of reducing voltage overshoot at motor terminals. It is important to minimize the peak value of the resonant current in order to reduce the stress on circuit devices.

The object of this work is to analysis and design a parallel quasi resonant DC link converter for a three-phase induction motor drive soft-switching inverter. The passive component values must be selected to meet specific design criteria, to reduce the level of the common mode voltage and to minimize the peak value of the resonant current.

A. Mathematical model

The circuit diagram of the QR inverter is illustrated in Fig. 1 [4, 5]. This topology is similar to the classic converter, plus an auxiliary circuit consists of switch S_{a2}, antiparallel diode D_{a2} and the coupled inductors L_{r1} and L_{r2}, the dc-link switch is S_{a1}, antiparallel diode D_{a1} and the dc-link resonant capacitor is C_r. The induction machine is fed by a three phase bridge IGBT inverter ($S_1 \div S_6$) connected to a rectifier.

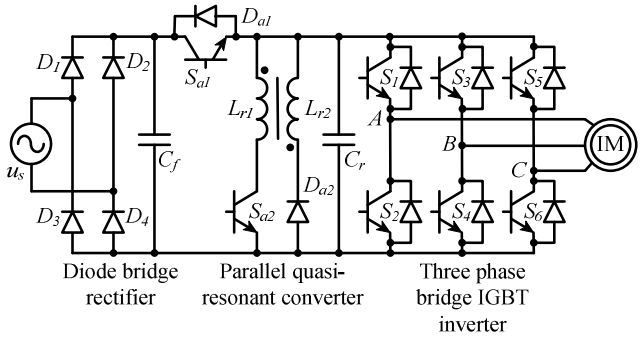

Fig. 1. Parallel quasi-resonant converter with coupled inductors

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In Fig. 2, the main operational waveforms of the resonant circuit are shown. A three-phase sine-triangle PWM command generator was implemented to control the six inverter switches. The operating mode of the DC quasi-resonant converter depends on the input DC voltage U_s and the load current in the DC link i_o. Formation of current i_o is determined by the signal of the PWM generator and the load mode (induction machine).

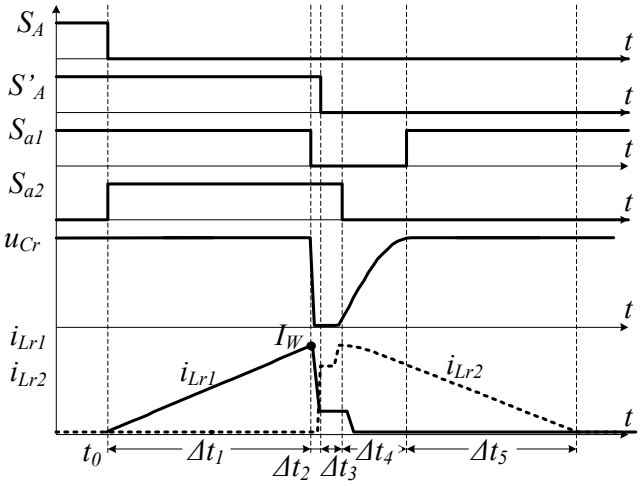

Fig. 2. Operational waveforms of the resonant circuit

The rms value of the basic harmonics of the inverter output line voltage at the space-vector PWM is:

$$U_{ab} = \frac{1}{\sqrt{2}} m U_s, \qquad (1)$$

where m is the modulation index.

The modulated currents of the three phases are defined by the expressions:

$$\begin{aligned} i^*_{мA} &= S_A i^*_A = S_A I^*_m \sin(\omega_s t - \varphi); \\ i^*_{мB} &= S_B i^*_B = S_B I^*_m \sin(\omega_s t - \varphi - 2\pi/3); \\ i^*_{мC} &= S_C i^*_C = S_C I^*_m \sin(\omega_s t - \varphi - 4\pi/3), \end{aligned} \qquad (2)$$

where: I_m^* - Amplitude value of the phase current in per units: $I_m^* = I_m/I_{mb}$, $I_{mb}=I_{mn}$; I_{mn} – nominal value; $\varphi=\psi_u-\psi_i$ - phase difference.

The current in the DC link is determined by the expression [4]:

$$i_o = S_A i_A + S_B i_B + S_C i_C, \qquad (3)$$

where S_A, S_B and S_C are the state of the S_1, S_3, and S_5 keys defined by the PWM generator, and i_A, i_B and i_C are instantaneous currents in the three phases of the motor.

Inverter control is implemented based on the link operation requirements, whenever a switching signal is generate, the auxiliary circuit must first be turned on to initiate a resonant transient. The inverter switches, when the link voltage reaches zero.

The operation of the DC quasi-resonance converter can be divided into six intervals (Fig. 2): steady state (up to t_0); energy storage interval (Δt_1); resonant link voltage ramp down interval (Δt_2); zero voltage interval (Δt_3); resonant link voltage ramp up interval (Δt_4); resonant energy recovery interval (Δt_5).

It can be seen from the figure that when switching to one of the main inverter switches (eg S_A) is necessary, it is performed with a certain delay $T_W=\Delta t_1+\Delta t_2$ after the voltage in the DC link drops to zero via the signal S'_A. First, the resonant coil is switched on and its current starts to increase to I_W. This value must be large enough so that the stored energy in the coil ensures resonant charging of the resonant capacitor. Equation of electromagnetic and electrostatic energy at full transformation results in:

$$W_{ем} = \frac{1}{2} L_{r1} I_{Lr}^2 = \frac{1}{2} C_r U_{Cr}^2. \qquad (4)$$

Here, the I_W current limit value corresponding to the required energy stored in the coil can be determined:

$$I_W = U_{Cr} Z_r, \qquad (5)$$

where $Z_r=\sqrt{(L_{r1}/C_r)}$ - characteristic resonance circuit impedance.

After replacing the expressions for U_{Cr} and Z_r, [4, 5] is obtained:

$$I_W = \sqrt{\left(\frac{U_s}{Z_r} + I_{o1} + I_{o2}\right)^2 - \left(\frac{U_s}{Z_r}\right)^2} - I_{o1}, \qquad (6)$$

Where I_{o1} and I_{o2} are the rms values of the current in the DC before and after switching the main switches.

The loading time of the resonant coil Δt_1, the discharge time of the capacitor Δt_2 and the total time of the transient process of the T_W resonance elements are obtained [4, 5]:

$$\begin{aligned} \Delta t_1 &= \frac{L_{r1} I_W}{U_s}; \\ \Delta t_2 &= \frac{1}{\omega_r} a\tan\left(\frac{U_s}{Z_r(I_W + I_{o1})}\right); \\ T_W &= \Delta t_1 + \Delta t_2. \end{aligned} \qquad (7)$$

A good design of the resonant elements is important in order to reduce the peak voltage stress and the peak current stress on the devices [6]. The specifications to design the quasi resonant dc link inverter circuit parameters are as follows [6, 7]:

- The inverter input voltage must be pulled down to zero for zero voltage switching (ZVS) and again boosted to the DC link source voltage;
- The trip currents should be as small as possible in order to reduce the circuit power loss;
- It is important to minimize the peak values of the resonant voltage and the resonant current in order to reduce the stress on circuit devices;
- The rising and falling slope of the inverter output voltage must be low for long cable drives;

- The resonant transition interval must be designed to be much shorter than inverter's switching frequency cycle time.

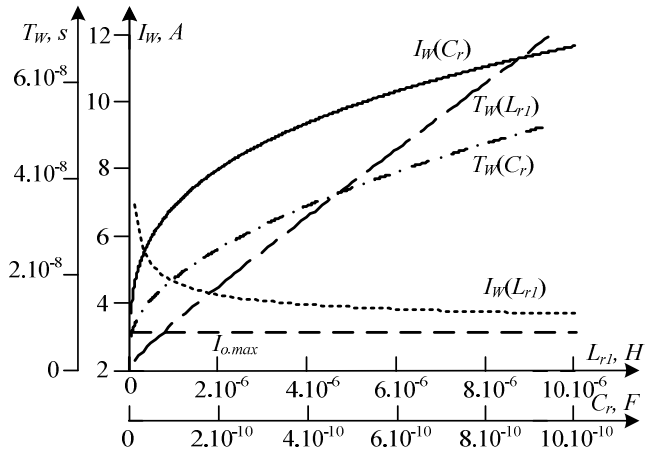

Fig. 3. Dependences T_W=f(L_{r1},C_r) and T_W=f(L_{r1},C_r)

In order to meet the input requirements, the transition time of the T_W resonant elements and the current supplying energy in the I_W coil need to have minimum values. Fig. 3 shows the shapes of T_W and I_W depending on the variation of L_{r1} and C_r. The minimum value of T_W is obtained at the minimum values of L_{r1} and C_r and the minimum value of I_W is obtained with a minimum value of C_r and a maximum value of L_{r1}.

The set for the optimal determination of the parameters of the resonance elements can be formulated in the following form: to find the values of L_{r1} and C_r for which the time T_W has a minimum value and the current I_W does not exceed the maximum set load current $I_{o.max}$. The equation of T_W is the target function, and the equation of I_W is a limiting condition. Therefore, a local minimum must be found on the function. The target function is given by an expression (7) and the constraint condition is obtained from an expression (6) in the form: I_W-$k_z I_{o.max}$=0, where k_z=1,1 is the stock ratio. As a second limiting condition, it is required that the voltage U_{Sa2}=(1+1/n)U_s have a value no less than the KU_s, where K=1,1 is a clamp factor. As a third limiting condition, it is required that the resonant capacitor have a value no less than the real one that can be used, not less than $C_{r.mim}$. For $C_{r.min}$ the value of 1nF is taken. Lagrange function takes the following form:

$$\begin{aligned} &L(L_{r1},C_r,n,\lambda_1,\lambda_2,\lambda_3)=T_W(L_{r1},C_r)+\\ &+\lambda_1\left(I_W(L_{r1},C_r,n)-k_z I_{o.max}\right)+\\ &+\lambda_2\left(U_{Sa2}(n)-KU_s\right)+\lambda_3(C_r-C_{r.min}), \end{aligned} \tag{8}$$

where λ_1, λ_2 and λ_3 are coefficients and n is coupled inductors turns ratio.

Kuhn-Tucker's terms are taught with the expressions:

$$\left|\begin{aligned} &\frac{\partial L(L_{r1},C_r,n,\lambda_1,\lambda_2,\lambda_3)}{\partial L_r}=0;\\ &\frac{\partial L(L_{r1},C_r,n,\lambda_1,\lambda_2,\lambda_3)}{\partial C_r}=0;\\ &\frac{\partial L(L_{r1},C_r,n,\lambda_1,\lambda_2,\lambda_3)}{\partial n}=0;\\ &\frac{\partial L(L_{r1},C_r,n,\lambda_1,\lambda_2,\lambda_3)}{\partial \lambda_1}=0;\\ &\frac{\partial L(L_{r1},C_r,n,\lambda_1,\lambda_2,\lambda_3)}{\partial \lambda_2}=0;\\ &\frac{\partial L(L_{r1},C_r,n,\lambda_1,\lambda_2,\lambda_3)}{\partial \lambda_3}=0. \end{aligned}\right. \tag{9}$$

The resulting system is of six equations with six unknowns - L_{r1}, C_r, n, λ_1, λ_2 and λ_3. The optimal values of the resonant elements depend only on the voltage and currents in the DC link - U_s, I_{o1} and I_{o2}.

B. Received results

Simulation is done on a three phase induction motor fed by a PWM inverter developed in PSpice [9]. The basic circuit of the proposed scheme consists of a three phase induction motor type 4AO-80B-4D having ratings as 0,75 kW, 380 V, 50 Hz which is connected to drive the constant nominal load.

The power supply to the circuit is three phase with U_{mr}=380V. The input voltage of the DC link takes U_s= $\sqrt{2}U_{mr}$=537V. The nominal mode of the induction machine is obtained with power supply U_L=380V and f_m=50Hz and nominal load. For space-vector modulation, the nominal supply voltage is obtained at a modulation index m=1 defined by an expression (1). The signal charts S_A and the modulated voltage signals u_{mA}^* and the currents i_{mA}^* and i_o^* for phase A at cosφ = cosφ$_n$, for space-vector modulation (SVPWM) are shown respectively in Fig. 4. - Fig. 6.

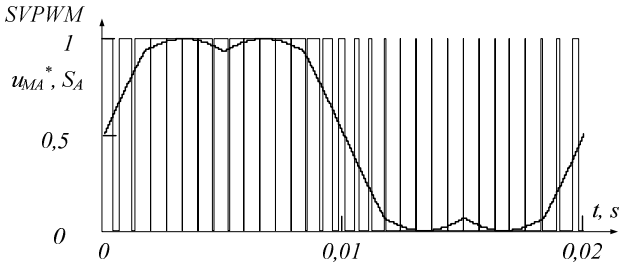

Fig. 4. Dependences u_{MA}^*, S_A=f(t)

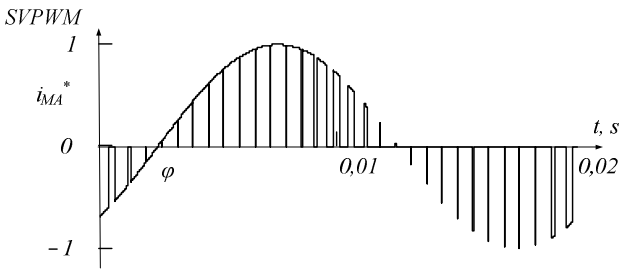

Fig. 5. Dependence i_{MA}^*=f(t)

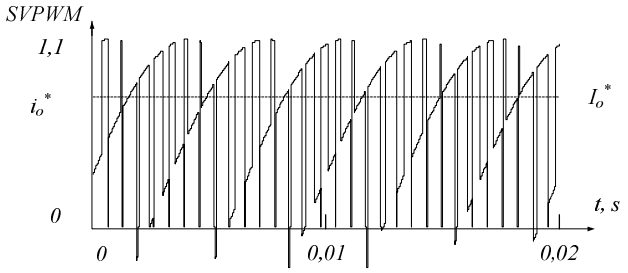

Fig. 6. Dependence $i_o^*=f(t)$

The analysis of the operation of the converter at first interval $T_{i1}=T_{pwm}$ is made on the basis of the graphs shown in Fig. 7 for space-vector PWM.

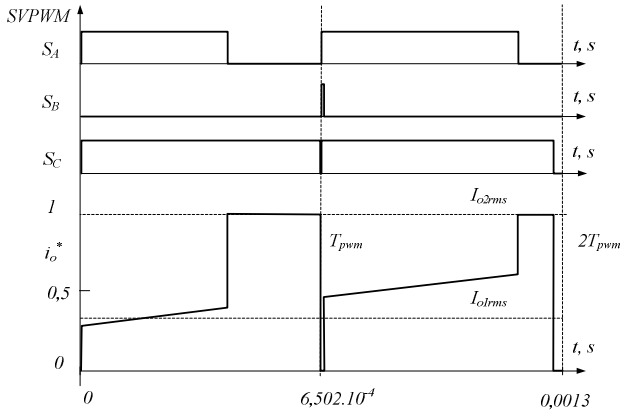

Fig. 7. Operation of the converter at first interval

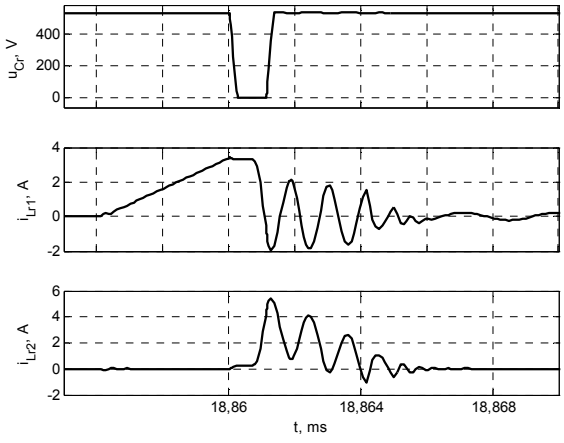

Fig. 8. Dependences u_{Cr}, i_{Lr1}, $i_{Lr2}=f(t)$

The design the quasi-resonant converter involves determining the parameters of L_{r1} and C_r. Based on the input data: U_s=537V; I_{o1}=1.073A; I_{o2}=3,172A, optimal values are calculated by the equation system (9). The results are summarized in Table 1. In the same table are given the minimum values of the time $T_{W.min}$ and the current $I_{W.min}$, obtained by expression (7) and expression (6), respectively.

Fig. 8 presents a part of the results obtained for one cycle of the scheme. Table 2 summarizes the results obtained from the computation methodology with those obtained from the simulation model.

TABLE 1. OPTIMAL VALUES FOR THE RESONANT ELEMENTS

L_{r1o}	µH	603,089
L_{r2o}	µH	498,421
C_{ro}	nF	1
n_o	-	0,909
λ_1	-	$1,216.10^{-5}$
λ_2	-	$6,546.10^{-8}$
λ_3	-	$-3,952.10^{3}$
$T_{w.min}$	µs	4,165
$I_{w.min}$	A	3,522

TABLE 2. SIMULATION RESULTS

	Methodology	PSpice model
Δt_1, µs	3,952	4,000
Δt_2, µs	0,213	0,24
Δt_3, µs	0,5	0,5
Δt_4, µs	1,109	0,210
Δt_5, µs	2,940	4,65
I_W, A	3,522	3,20

Table 2 shows that the results obtained by the computational methodology are close to the results obtained from the simulation model.

II. CONCLUSION

A parallel quasi resonant DC link converter for induction motor drive application is analyzed and designed. Link waveforms and operation modes are analyzed to reveal various soft switching characteristics. The converter is designed to achieve the maximum voltage gradient and simultaneously to have low peak current and voltage stresses on the devices and thereby to reduce the losses.

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Induction Machine Parameters Identification Method Suitable for Self-commissioning

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Abstract – **Induction machines are nowadays used also in electric drives with high demands on dynamic properties. However their control strategies usually need a mathematical model of the machine with a set of parameters. Obtaining of these parameters can be done by laboratory procedures but in-field procedures are more favorable due to potential savings in time and financial costs. This paper proposes an off-line parameter identification method that is suitable for self-commissioning of an electric drive in cases when machine and converter comes from different producers. The method is carried out entirely by means of a standard power inverter only by impressed stator voltages.**

Keywords – **Induction motor drive; parameter identification; self-commissioning**

I. INTRODUCTION

Induction machine became nowadays the most common type of converter of electrical to mechanical energy in industry, traction and variety of other higher power drives. It is robust with simple construction, easy to use and has low maintenance cost with comparatively long operational life. However their control has been problematic for a long time so they were used only in drives with low or no requirements on control of their speed or torque. Only the development of power semiconductor converters and microcontrollers capable of complex control tasks enabled to use the induction machines also in drives with higher requirements on dynamic properties. These can be the drives in manufacturing lines or in transportation. In all these fields, better positioning and better dynamic properties can bring significant advantages to the application. The most accurate common control strategies of the induction machines, such as Field Oriented Control (FOC) or the Direct Torque Control (DTC), are however complex and can be characterized by using of a mathematical model of the induction machine.

Mathematical model of the machine needs to be supplied by particular parameters to work accurate. It can be represented by an equivalent circuit. For the field oriented control, so called Inverse Γ equivalent circuit (Fig. 1) is widely used.

Its popularity stems from the fact that the current divides into two branches that represent flux and torque component of the induction machine stator current (Fig. 2).

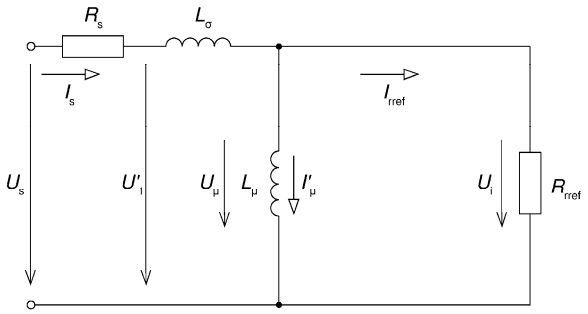

Fig. 1 "Inverse Γ" equivalent circuit of an induction machine.

If the parameters of the model are not known properly, the controller cannot estimate the real conditions of the system which can lead to decrease of the dynamic performance of the drive and to the worsening of the efficiency. [4]

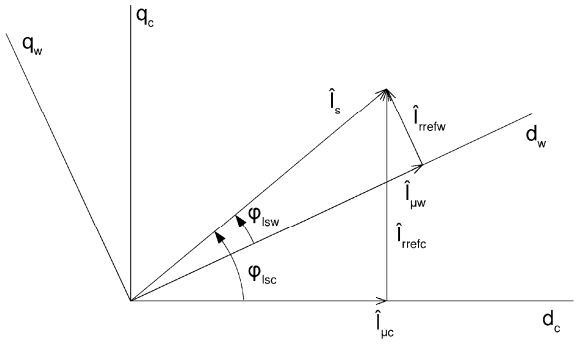

Fig. 2 Difference between rotor flux components for two different temperatures.

Parameters of the equivalent circuit shown on Fig. 1 are stator resistance R_s, leakage inductance L_σ, magnetizing inductance L_μ and a rotor resistance R_{rref} (referred to stator). Out of these parameters, only stator resistance R_s is directly measurable.

Fig. 2 shows an example of deployment of an incorrect value of the rotor resistance R_{rref}. The controller expects the value of the resistance for a given temperature ϑ_c so it makes the decomposition to the components $\hat{I}_{\mu c}$ and $\hat{I}_{rrefc}$. However the real value of the rotor resistance is higher and the right values of the components should be $\hat{I}_{\mu w}$ and $\hat{I}_{rrefw}$. This can happen very often as the rotor resistance is dependent on temperature. If we imagine a machine working outside of a building (e.g. traction, electric vehicles etc.) in certain climate conditions, the temperature range can be very wide. Other parameters of a machine can

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vary as well. It should be noted, that even parameters of the same type of the machine can vary up to 10-15 % from the manufacturing process [1], [2].

As mentioned before, the majority of required parameters is not directly measurable, so only experimental methods are viable. These are often divided into two main groups: conventional methods, and on-site methods [4], [5], [6]. Under the term Conventional methods (sometimes referred also as standard tests) we understand DC measurement of the stator resistance, no-load test and locked-rotor test [3]. These are mainly laboratory procedures which have some disadvantages for field usage such as the need of a special-purpose jig for blocking the machine's rotor.

As a response, on-site methods were developed. These can be further divided into off-line and on-line methods [4], [5], [6]. Off-line methods that should obtain parameters of the machine before its start are distinguished into methods suitable for commissioning and self-commissioning. On-line methods should further ensure respecting changes of parameters during the operation of the drive.

It is nowadays common that machine and inverter comes from different producers. This formed a demand for obtaining the machine parameters in field by means of the inverter. Self-commissioning methods should be able to gather the required parameters at standstill. This permits a situation that the load is already connected to the drive but it is not desired to move with it before good operation of the drive can be assured. The commissioning methods allow the drive to rotate. Self-commissioning methods are more preferable, because they can be performed within every still stand of the drive. For applications with breaks in operation it can be also used for respecting the parameters change. This paper concerns an offline method of parameter identification that is suitable for self-commissioning.

II. DESCRIPTION OF THE METHOD

Self-commissioning methods should provide the control system of the drive with suitable information about the induction machine only by means of the power inverter itself. This brings certain problems e.g. the impossibility of measuring voltage at the motor terminals or usually small resolution of current measurement. Basic idea of the proposed method was presented in [7], but modifications had to be done to deploy it on a standard voltage source inverter.

In general most of the approaches try to carry out the similar measurements as in case of conventional methods but only by means of the inverter. Fig. 3 shows common parts of a variable speed electric drive with an induction machine that can be used for self-commissioning: a rectifier that is supplied from the grid, a DC link (represented by capacitor), a frequency converter (inverter) and a controller.

The only sensors that are used are current sensors on the phase conductors the machine terminals and voltage sensor in the DC link. The speed sensor is not taken into account as no rotation of the drive is permitted in case self-commissioning.

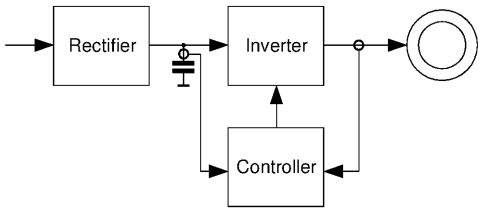

Fig. 3 Common structure of a variable speed electric drive with an induction machine. Speed sensor is not shown as it cannot be used by self-commissioning.

This method can be divided into two parts. In the first part, short circuit time constant T_k and leakage inductance L_σ are obtained. In the second part stator resistance R_s and stator time constant T_s are obtained from which the rest of the parameters are calculated.

A. First part of the measurement

First part of the procedure is done by connecting two opposite voltage pulses of nominal amplitude to the motor terminals (Fig. 4).

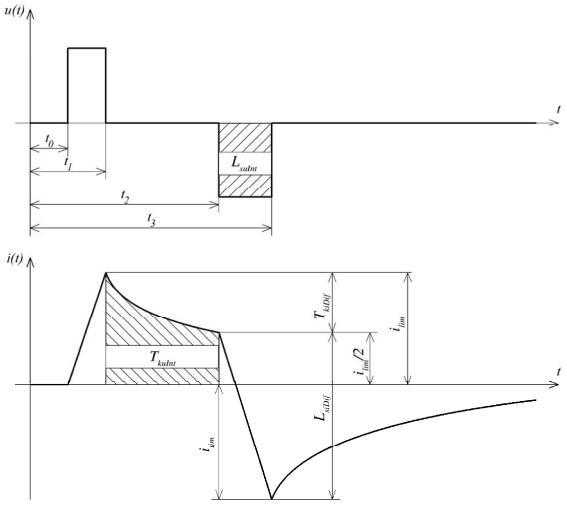

Fig. 4 First part of the method.

First voltage pulse is a positive one and it can be connected to any combination of two of the motor terminals (a-b, a-c or b-c). The induction machine behaves like a first-order delay element. By the instant t_0, the stator current starts to rise and it is monitored by the current sensors of the inverter. Voltage is calculated from the DC link voltage and the duty cycle. The voltage drop on the switching devices can be taken into consideration however small it is compared to the nominal voltage value.

Duration of the first voltage pulse is given by rising stator current. After it reaches the value i_{lim} which should be equal to the peak rated stator current the motor terminals are short circuited by the inverter. Stator current starts to decrease. Measured waveform of this decrease is numerically integrated to get T_{kiInt} value. Change of the current value is monitored as well.

When the current reaches half of the of the i_{lim} value, negative voltage pulse is applied and exact value of T_{kiDif} is stored. Value $i_{lim}/2$ was chosen because the current

transient cannot be measured until the zero because of the nonlinearity of the switching devices in the inverter.

The integral of the voltage L_{suInt} and the change in the current L_{siDif} are measured during the interval of the negative voltage. Duration of this voltage pulse is given by the current. When it reaches negative value of i_{lim} the machine is short circuited again and it is only checked whether the current reached zero.

Short circuit time constant T_{kx} and leakage inductance $L_{\sigma x}$ are obtained by this measurement as follows:

$$T_{kx} = \frac{T_{kiInt}}{T_{kiDif}} \tag{1}$$

$$L_{\sigma x} = \frac{L_{suInt}}{L_{siDif}} \tag{2}$$

These equations are not scaled so it needs to be further recalculated:

$$T_k = \frac{T_{kx}}{f_v},\ L_\sigma = \frac{L_{\sigma x} \cdot s_u}{f_v \cdot s_i} \tag{3}$$

where f_v is the sampling frequency (Hz), s_u is the voltage scale (V/ bit) and s_i is the current scale (A/ bit).

B. Second part of the measurement

Second part of the measurement starts with a ramp of both voltage and current (Fig. 5). Specific measuring level of voltage is given by a steady state current that must fit into a tolerance belt of $i_{meas} \pm \delta$. The converter must work as a current controller in this phase. If the current is out of the bounds, the duty cycle must be adjusted.

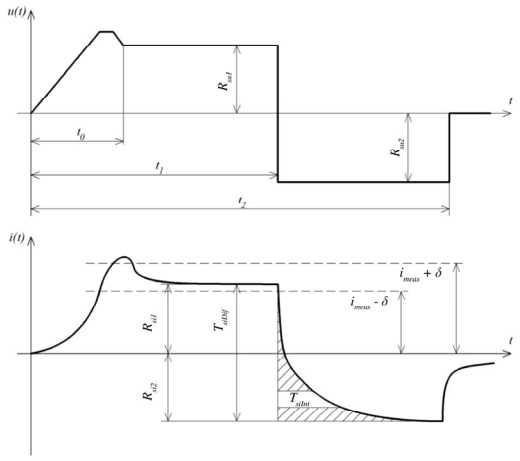

Fig. 5 Second part of the method.

After the current reaches the target steady state, voltage R_{su1} and current R_{si1} are measured. Both values can be measured multiple times and filtered. The value of i_{meas} was tested to be 30% of the peak value of the stator current of the motor. Duty cycle of the inverter is not changed for several seconds. Then the voltage of the same amplitude but opposite level (with the same duty cycle) is applied to the motor terminals which lead to a current transient.

From this instant the current waveform is integrated to get value of T_{siInt}. This is the major difference from the procedure presented in [8]. Voltage is applied until the current reaches value R_{si2} which is opposite to R_{si1}. Exact value of current change T_{siDif} is stored and values of the steady state current R_{si2} and voltage R_{su2} are measured. The resulting stator resistance R_{sx} and stator time constant T_{sx} are then evaluated by relations:

$$R_{sx} = \frac{\left(\frac{R_{su1}}{R_{si1}} + \frac{R_{su2}}{R_{si2}}\right)}{2} \tag{4}$$

$$T_{sx} = \frac{T_{siInt}}{T_{siDif}} \tag{5}$$

And again has to be rescaled:

$$R_s = R_{sx} \cdot \frac{s_u}{s_i},\ T_{sr} = \frac{T_{srx}}{f_v} \tag{6}$$

For calculating the rest of equivalent circuit parameters following relations are utilized:

$$R_{rref} = \frac{L_\sigma}{T_k} - R_s \tag{7}$$

$$L_\mu = \frac{T_{sr} \cdot R_s \cdot R_r}{R_s + R_r} \cdot \tag{8}$$

III. RESULTS

Proposed method has been simulated in Matlab – Simulink environment and then examined on a real drive with an induction motor. The drive consisted of rectifier, power inverter, three phase induction motor and a controller as on Fig. 3. The controller was based on EK-TM4C123GXL development board with Texas Instruments Cortex-M4F processor. Measurement procedure has been implemented within the controller program. Power inverter is equipped with IGBTs rated 1200V/100A. Parameters of the tested induction machine are presented in TABLE I.

TABLE I. INDUCTION MOTOR NOMINAL VALUES

Type	1AY112L-L	Star (Y) connected
P_n	3,5 kW	Nominal power
U_n	380 V	Nominal voltage
I_n	11 A	Nominal current
cos φ	0,6	Nominal power factor
n_n	960 · 1/ min	Nominal speed

The DC link voltage U_{DC} was 440 V, the value of the i_{lim} current used in first part of the measurement was set to 10 A. Value of the i_{meas} was set to 6 A and the measurement time of the steady state current and voltage was 5 s. Sampling period of the ADC was 250 ksps. Parameter values obtained by the method described in this paper as well as comparison with the data obtained by conventional tests are presented in TABLE II.

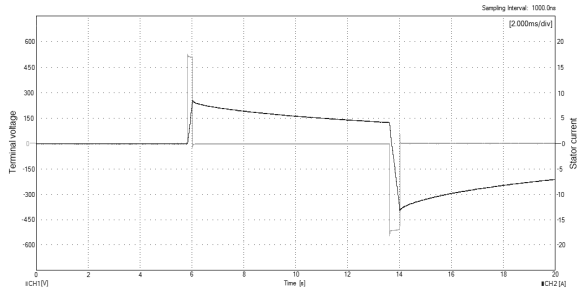

Fig. 6 Waveforms of machine terminal voltage and stator current during the first part of the test.

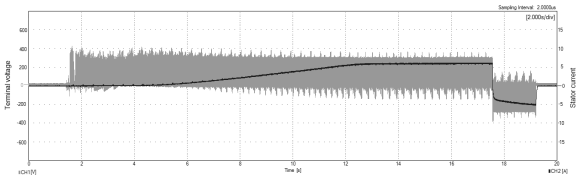

Fig. 7 Waveforms of machine terminal voltage and stator current during the second part of the test.

Fig. 6 and Fig. 7 present waveforms taken by the oscilloscope (as mentioned before, the controller itself obtains only the voltage of the DC link and the voltage on the motor terminals has to be calculated from the duty cycle of the switching devices). Especially in Fig. 7 we can see that the current transients are very fast and thus problematic to measure with the standard inverter current sensors and AD converters. This is probably the biggest source of error of the whole measurement.

TABLE II. COMPARISON BETWEEN PARAMETERS OBTAINED BY CONVENTIONAL MEASUREMENT AND PROPOSED OFFLINE IDENTIFICATION METHOD

Parameter	Unit	Standard test	Proposed method	Difference [%]
R_s	Ω	1,1066	1,6200	46,4
R_{rref}	Ω	0,9790	0,7500	-23,4
L_σ	H	0,0165	0,0156	-5,2
L_μ	H	0,0978	0,1246	27,4

IV. CONCLUSION

This paper deals with an offline self-commissioning parameter identification method. This procedure can obtain parameters needed for a mathematical model of an induction machine only by means of supplying power converter. Mathematical model is a cornerstone of popular precise induction machine control methods such as FOC and DTC and accuracy of the parameters can influence the performance of the whole drive and its operation.

Induction machine parameters can be obtained by laboratory measurements called standard tests which include DC test, no-load test and locked rotor test. However, these measurements require special sinusoidal power sources and special-purpose jigs which is a complication in an in-field application. Parameter identification methods that require no special equipment or specially trained workforce can thus make time and financial savings during the drive installation as well as more benefits with increased accuracy and efficiency and overall dynamic properties of the drive.

Presented offline identification method can fulfill the demands of self-commissioning of the drive as it uses only the converter and does not need to rotate with the machine. This permits the load to be connected to the drive and the method can be executed before every start of the operation or within breaks. As an example of a dynamic drive that can utilize such a method is a passenger train that can commit the parameter identification of its traction motors when calling at a station.

Presented measurements on the 3,5 kW induction machine compared the data obtained by the presented off-line method with the values gained by conventional measurements. The method gives results sufficient for the start of the drive but not satisfying when compared to conventional tests results. The achieved accuracy is lower than the natural variation of parameters between machines of the same type so drives with high demand on dynamic properties deployment of some further on-line method or improvement of the accuracy would be needed.

When a drive is being commissioned the machine and a converter often come from different producers. In these cases the converter is connected to an "unknown" machine. In such cases the presented method is sufficient and useful.

ACKNOWLEDGMENT

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Analysis of high-speed rotary wireless power transmitters

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Abstract - **This article provides a review and study of the possible types of rotating wireless transmitter (*RWT*) constructions. The object of the study is the high-speed transmitters with a rotation speed of the order of 10 000 revolutions per minute and more. They are mainly used in number of innovative technologies for machining details of sophisticated shape and hardness. The paper examines the influence of centrifugal forces, speed, acceleration, mass and dimensions on the *RWT*. In order to clarify the advantages of the types of constructions, computer simulations were made using the software product *Ansoft Maxwell,* showing the distribution of the magnetic field and its intensity at the individual points of the *RWT*. This article revises four main types of the *RWT* constructions, along with the design methodology, mechanical and electromagnetic analysis.**

Keywords – **high-speed rotary, wireless power transfer, innovative technology, magnetic coupling factor.**

I. Introduction

Wireless energy transmission is an innovative technology which launches a new stage in the development of automated systems. It also involves the optimization of a lot of technological processes, as it offers great flexibility, removal of power cables, lack of moving electrical contacts and associated problems (sparks, wear, etc.). It also allows application in explosive environments, such as high humidity and high speeds. It is used for the wireless supply of consumers, which perform linear and rotary motion.

The article presents an innovative concept used in mechanical machining of details. The concept itself allows, in addition to the rotational movement of the tool also an additional ultrasonic vibration in the direction of drilling. It is used in the processing of materials with high hardness and brittleness such as ceramics, glass, silicon, hardened steels and others. This technology requires a *RWT* to supply of the ultrasonic transducer, determined by the high speed of rotation. There are a number of mechanical and electrical problems related to the rotary module. Mechanical problems are determined by the design, shape, dimensions and mass of the *RWT*. The electrical problems depend on the geometric configuration of the magnetic circuit, obtained between the transmitter and the receiver parts, which determines a good magnetic coupling factor and a high efficiency.

II. Types of Rotary Wireless Transmitters

There are two basic designs of rotary wireless energy transmitters - axial (*A*) and radial (*R*) shown on Fig. 1a and Fig. 1b. They are divided into several sub types, differing in the location of the coils and the shape of the body to which they are attached. A variation of the two constructs is the coaxial transmitter - Fig. 1c and Fig. 1d. It combines the advantages of both configurations.

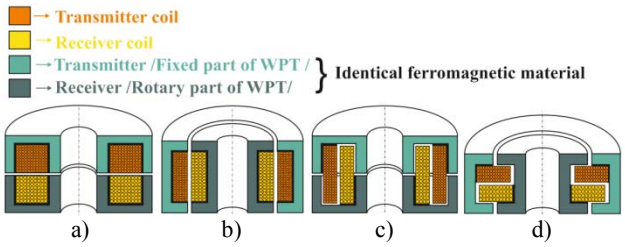

Fig. 1. Types of rotary wireless transmitters: a) radial, b) axial, c) coaxial R, d) coaxial A

In the design of the conductors for the individual types of *RWT*, a major problem is the inconsistency between the standard ferrite cores, offered by the companies and the dimensions of the transmitter designed by the constructors. This requires the usage of composite magnetic cores, which complicates the design and construction of the mechanical system. A solution the problem is the use of new magnetoelectric materials, which have a number of advantages comparing to the traditional ferrites [6]. Table 1 presents a comparison between the most commonly used materials for making *WT* magnetic cores. The conclusion that could be made is the magnetoelectric materials have a significant advantage, because they are subject to mechanical machining and practically each and one required shape of a magnetic core could be obtained.

Table 1. Types of Materials

Material	Permeability	El. Resistivity Ohm.cm	El.Strength Vrms/mm (300kHz)	Availability in sizes and shapes	Curie temp. 0C	Thermal conduct. W/cm2
Fer. 559	18-20	High >15000	Medium ≤100	Any when machined	>300	0.04
Fer. 119	7	Very High	>300 Vrms/mm	Any when machined	>300	0.02
Fluxtrol 50	50	Low	<100 Vrms/mm	Any when machined	>300	0.05

III. Mechanical Analysis of Rotary Transmitters

For the analysis of the mechanical forces impacting on the receiving part of the *RWT*, the solid body rotation theory about the constant axis (two-dimensional rotation) is applied [1].

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In a symmetrical construction, the rotation axis passes through the center of gravity of the magnetic core, as there are cases in which it is offset from the center. To clarify the impact force mechanism, is proposed the following theoretical overview of the rotational body kinematics [1].

The basic quantities describing the rotational movement are presented in Fig. 2a and the corresponding expressions are:

$$\Delta\varphi = \Delta S/r \quad (1)$$

$$\omega = \frac{\Delta\varphi}{dt} = \frac{\Delta S}{r.\Delta t} = \frac{v}{r} \quad (2)$$

$$v = \omega.R \quad (3)$$

$$\alpha = d\omega/dt \ [rad/s^2], \quad \text{where} \quad (4)$$

$\Delta\varphi$ - angle of rotation;

ΔS_i - path taken from a certain point i in the course of rotation;

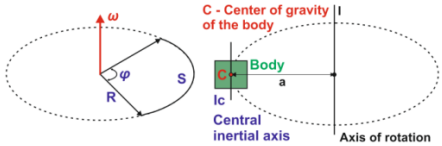
R_i - distance of a certain point i to the axis of rotation;

$v[m/s]$ – linear velocity;

$\omega[rad/s]$ – angular velocity;

$\alpha[rad/s^2]$ - angular acceleration.

$\Delta\varphi$ - angle of rotation;



a) b)

Fig. 2. Description of rotary motion; a) basic dimensions, b) rotation around a random axis

The main dynamic parameter characterizing the rotational movement is the moment of the force according the axis of rotation, i.e. torque - M $[N.m]$. It is a vector product of the force $\vec{F}$ applied at a certain point and the distance $\vec{R}$ to the axis of rotation:

$$\vec{M} = \vec{r}.\vec{F} \quad (5)$$

$$M = r.F.sin(\vec{r}.\vec{F}) \quad (6)$$

The remaining mechanical forces impacting on the rotary transmitter system are determined by the kinetic and potential energies, and the three principles of Newton's mechanics. The kinetic energy Ti is equal to:

$$T_i = \frac{1}{2}.m_i.v_i^2 = \frac{1}{2}.m_i.R_i^2.\omega_i^2 = \frac{1}{2}.m_i.R_i^2.\omega^2, \text{where} \quad (7)$$

mi – mass of the certain material point i.

The quantity $I_i = m_i.R_i^2$ $[kg.m^2]$ has been introduced, called inertial moment of a point relative to a certain axis. Then for the kinetic energy Ti is the following result:

$$T_i = \frac{1}{2}.I_i.\omega^2 \quad (8)$$

The kinetic energy of the whole rotation transmitter is:

$$T = \sum_{i=1}^{n} T_i = \frac{1}{2}(\sum_{i=1}^{n} I_i)\omega^2 = \frac{1}{2}I\omega^2 \quad (9)$$

The quantity $\sum_{i=1}^{n} I_i$ is the inertial moment of the rotary transmitter related to a certain axis of rotation.

For more sophisticated applications of RWT, a linear motion is added to the rotary process. In these cases, its full kinetic energy is the sum of the energies of the two types of movements, i.e. obtained:

$$T = T_{LIN} + T_{ROT} \quad (10)$$

$$T_{LIN} = \frac{1}{2}.m.v^2, \quad T_{ROT} = \frac{1}{2}.I.\omega^2 \quad (11)$$

The equation (11) indicate that the linear velocity v, corresponds to the angular velocity ω and the mass m is equivalent to the moment of inertia I.

The moment of inertia depends not only on the mass, but also on its distribution. The shape and dimensions of RWT are extremely important. In rotation about an axis passing through the center of the receiver's magnetic core, only its moment of inertia Ic impacts and it's determined by the center of inertia of the body C. For calculating the moment of inertia related to a random axis – Fig. 2b is used the expression:

$$I = I_C + m.a^2 \text{ , where} \quad (12)$$

a – distance between the two axes.

An example scheme is shown in Fig. 2b.

The conclusion from the Eq (12) is that for the optimal design of a rotation transmitter, the axis of rotation has to pass through the center of the receiving part. Then the dynamic forces impacting on it are minimal, which reduces the imbalancing factors and the loading on the suspension and bearing system. Equation (8, 12) are the mathematical formulas for the mechanical load, which impacts the RWT according to the rotation speed and RWT'mass. It is directly related to the choice of the magnet core making materials, the geometric configuration and its dimensions.

IV. Electromagnetic Analysis of Rotary Transmitters

A. Rotary transmitter with radial (R) configuration.

Cross section of a radial RWT is shown in Fig. 3 [2]. The radial configuration is applicable in cases with constructive limitation of the permissible dimension in direction x according to Fig. 3. This requires an extension of the transmitter in direction y, i.e. perpendicular to the axis of rotation, which at the same time improves the magnetic coupling factor. It is typical for this kind of transmitters to allow fluctuation and slight displacement of the coordinate system y. The displacement on x coordinate, causes some increment of the air gap δ, hence some worsening in the efficiency.

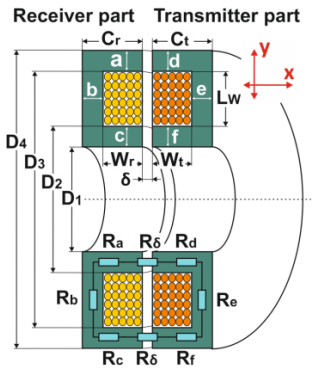


Fig. 3. Radial rotary transmitter

Symbols for the main design dimensions as follows:

Lw, Wr, Wt –geometric dimensions of the coils, length and width, as the index denotes transmitter (t) and receiver (r);

$D_{(n)}$ – diameter of the *RWT*. The diameter D_1 is determined by the thickness of the axis of rotation. Often this is a spindle axis or an axis of a certain type electric motor. The optimization of the diameters D_2 and D_3 allows improving of the magnetic coupling factor between the transmitting and receiving coils.

R – magnetic resistance of the individual parts, which set up the transmitter chassis. They are a closed circuit with lengths *l(n)*, as the intensity *H* of the field through them is constant. The sum of the individual lengths gives the average length of the magnet core.

$$l = \sum l_{(n)} = l_a + l_b + l_c + l_d + l_e + l_f + 2.l_\delta \quad (13)$$

The value of *R* in the individual parts is defined by:

$$R_{(n)} = \frac{l_{(n)}}{\mu_M S_{(n)}}, \text{ where} \quad (14)$$

$l_{(n)}$ – length of a respective part;

$S_{(n)}$ – section of a respective part;

μ_M – magnetic permeability of the particular material.

The magnetic resistivity of the magnet core R_M is the sum of the resistance of the individual parts - $R_M = \sum R_{(n)}$.

The influence of the air gap δ is determined by its magnetic resistance $R\delta$ according to the expression:

$$R_\delta = \frac{l_\delta}{\mu_0 S}, \text{ where} \quad (15)$$

$l\delta$ – length of the air gap;

μ_0 – magnetic permeability of the air.

The full magnetic impedance for the entire circuit of the *RWT* is determined by the principle diagram in Fig. 4 [3].

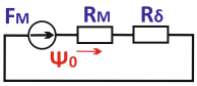


Fig. 4. Diagram of the electromagnetic circuit

The equivalent magnetic impedance of the closed magnetic circuit is defined by the sum of the magnetic resistances of the sequentially joined parts.

$$R = R_M + R_\delta \quad (16)$$

The current flowing through the transmiter coil creates a magnet flux Ψ. The main part Ψ_0 passes through the magnet core, and the other part generates a dissipation flux $\Psi\sigma$, i.e.

$$\Psi = \Psi_0 + \Psi_\sigma . \quad (17)$$

The absolute magnetic permeability of the material of the ferrite core exceeds in many times the magnetic permeability of the the air ($\mu >> \mu_0$), therefore $\Psi_0 >> \Psi\sigma$ and $\Psi \approx \Psi_0$.

The value of the magnetic voltage *Fm* is obtained by the following expressions:

$$F_m = w_t . i_t \quad (18)$$

$$F_m = \Psi_0 . R, \text{ where} \quad (19)$$

w_t – winding of the transmitter coils;

i_t – magnetic current through the transmitter coil.

This magnetic circuit could be represented by the following expressions:

$$F_m = \Psi_0 . R = \Psi_0 . (R_M + R_\delta) = \Psi_0 . \left(\frac{l_{(n)}}{\mu_M S_{(n)}} + \frac{l_\delta}{\mu_0 S}\right) \quad (20)$$

The inductance of a magnetic circuit is related to magnetic resistances *R* and the number of winding turns *N*:

$$L_1 = \frac{N_1}{R}, \qquad L_2 = \frac{N_2}{R}, \qquad M_{12} = \frac{N_1 N_2}{R}. \quad (21)$$

The number of turns of the primary and secondary coils are determined according to the expressions:

$$N_1 = \frac{U_E . \Delta t}{A_{min} . \Delta B}, \qquad N_2 = \frac{U_{out}}{U_E} . N_1, \text{ where} \quad (22)$$

Amin – minimum cross-section of the magnetic core;

B – magnetic induction;

Δt – RWT'transformer operating time. It is set by the operation mode of the converter – one-way or two-way mode [4];

U_E – power supply voltage; *Uout* – output voltage.

For designing the coils, except the coil inductance *L*, another important parameter, which must be observed is the parasitic capacity *Cp* - called coil capacity [5]. It occurs between adjacent turns and between the rows of the coil. This capacity induces additional losses in the coils, therefore it should be minimal. To reduce *Cp*, segmentation of the coil is used. From a construction point of view, decreasing the width of the coil *Wr*, *Wt* respectively its rows decreases *Cp*. Increasing *Lr*, *Lt* allows achieving the desired inductance at fewer rows of the coil. In addition, this parameter improves the magnetic coupling factor.

The voltage of the two coils of the RWT'transformer can be expressed by applying the Kirchof's second law, through their self inductance of the coils and their mutual.

$$V_1 = L_1 \frac{di_1}{dt} + M_{12} \frac{di_2}{dt}, \quad V_2 = M_{12} \frac{di_1}{dt} + L_2 \frac{di_1}{dt} \quad (23)$$

The mutual inductance is related to the magnetic coupling factor *k* and self coil inductances:

$$k = \frac{M}{\sqrt{L_1 L_2}} \quad (24)$$

B. Rotary transmitter with axial (A) configuration.

Cross-section of an *A* transmitter is shown in Fig. 5[2]. Its electromagnetic analysis and its design is identical to the ones of the radial. It is applicable in cases whit constructive limitations of the permissible dimensions in direction *y* according to Fig. 5. This requires an extension of the transmitter in parallel to the axis – coordinate *x*. It is typical for this type of transmitters to allow instability, fluctuation and slight displacement in the *x* - direction, making this kind of rotary transmitter suitable for hit- drilling purposes.

A disadvantage of the axial *RWT* is the construction difficulty, which appears in producing the transmitter coil.

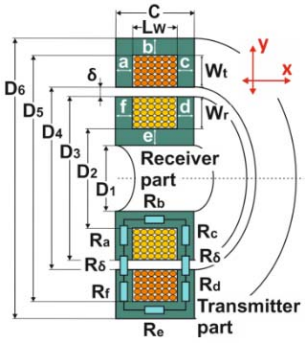


Fig. 5. Axial rotary transmitter

C. Rotary transmitters with coaxial configuration.

The design of the coaxial transmitter might be with both, radial (*CR*) or axial (*CA*) configuration. Cross-section of the two types are respectively represented in Fig. 6a and Fig. 6b [2].

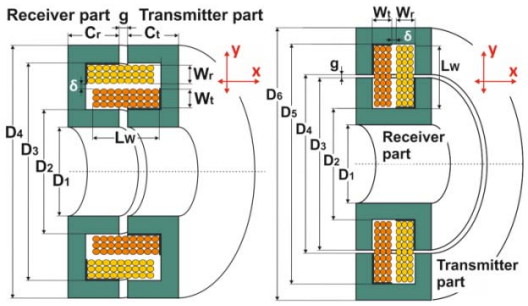


Fig. 6. Coaxial rotary transmitters; a) coaxial radial, b) coaxial axial

A main advantage of this type of transmitter is the high magnetic coupling factor between the coils and greater efficiency, determined by minimal dissipation losses of the magnetic field. The level of magnetic induction is less, which reduces the losses of saturation in the magnetic core.

The disadvantage is the sophisticated construction and the existing difficulties in producing the coils. In this construction, instability and displacement in both directions (x and y) is unacceptable and is limited by δ and g respectively. This requires a balanced rotating mechanism.

V. Magnetic Induction and Distribution of the Magnetic Field in The Types of RWT

The date of the reviewed types of *RWT* reported by simulating the magnetic processes at identical input parameters and material basis of the structures.

The results of a simulation of radial and axial *RWT* are respectively represented in Fig. 7a and Fig. 7b. To create the simulation we've used the *Ansoft Maxwell* software. The analysis of the results of the *A* and *R* transmitter simulation, shows that the intensity of the magnetic field among the coils of the *A* is greater, which create conditions for saturation of the magnetic core and worsen the efficiency. Another disadvantage of the *A* transmitter is the existing conditions for heating of the receiver part, determined by the high level of magnetic induction in the areas around the axis of rotation.

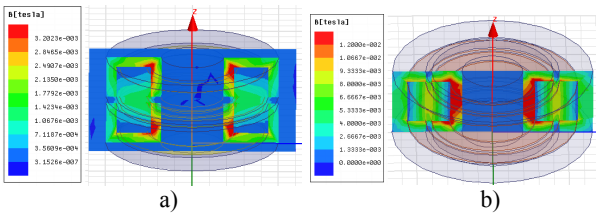


Fig. 7. Density of the magnetic field; a) radial, b) axial

A comparison of the *R* and *A* configurations shows that *R* one has higher efficiency and more uniformly distribution of the magnetic induction between the transmitter and the receiver part, which determines a better thermal performance.

The result of the analysis of the *CR* and the *CA* transmitter simulations are respectively represented in Fig. 8a and Fig. 8b. A comparison between them shows that the *CR* is better than the *CA*.

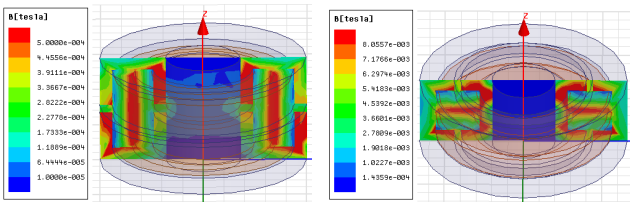


Fig. 8. Density of the magnetic field; a) coaxial radial, b) coaxial axial

Table 2 represents the value of magnetic induction of the reviewed types of *RWT*.

TABLE 2. MAGNETIC INDUCTION

Type *RWT*	*R*	*A*	*CR*	*CA*
B[mT]	1,4	8	0,5	0,7

In summary, the coaxially made transmitters are more efficient than axial and radial. This is determined by greater overlapping area between the transmitter and receiver coils. Additionally the radial configuration has better electricals parameters, than the axial one.

VI. Conclusion

This article is a review of high-speed *RWT*. It revises the four main types of the *RWT* and the constructive requirements, defined by the high speed of rotation. It analyzes the major imbalance factors, which affect both – the suspension and the bearing system. Furthermore it introduces the methodology for electrical design and gives a detailed description of the respectively simulated electromagnetic processes. There are diagrams included in order to show the electromagnetic induction and the magnetic field distribution. The article also presents the advantages and the disadvantages of the four main types of the *RWT*.

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Micro and Nanogrid Active Power Management under Stand Alone and Grid Connected Operation

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Abstract – **This paper presents test evaluation and experimental results from the implementation of the approach for smart active power management in micro and nanogrids given in [1-4] under island and grid- connected mode.**

A new power electronic smart load controller for improving the power system stability and active power management is proposed and realized. The controller interaction is tested in a "power hardware in the loop" test performed at the Power System Stability Laboratory of TU- Sofia.

The analysis of the results proves the functionality of the proposed concept and hardware realization. The approach offers cost effective solution to the main issues related to normal and stable micro and nanogrid operation.

Keywords—***Smart load controler; active power management; nanogrids; microgrids; island mode; flexible loads; non-flexible loads; demand side responce***

I. INTRODUCTION

The global trend of growing distributed generation in the electrical power systems opens new opportunities for smarter power management. The implementation of distributed renewable generation and storage sources allows more flexible concepts such as micro and nanogrids operating in grid connected, autonomous or partially connected mode. The power system stability, balancing and control arises to be a challenging issue in this regard. This article presents hardware test realization and proof of functionality of a simple and effective dual leading signal concept for smart power management of micro and nanogrids which was originally proposed in [1].

II. METHODOLOGY

The concept under test considers the active power control as a shared and mutual responsibility of all of the microgrid players (loads, distributed generators and storage units) [1-4]. A control of the dispatchable low priority loads is applied in order to support the maintenance of the active power balance [2-17]. For this purpose the loads are divided in flexible, non-flexible, and partially flexible. Thus [1]:

$$\sum_{i=1}^{n} P_{G,i} = \sum_{i=1}^{f} P_{flexible\ L,i} + \sum_{i=1}^{g} P_{partially\ \ flexible\ L,i} + \ldots$$
$$\ldots + \sum_{i=1}^{h} P_{non-flexible\ L,i} \pm \sum_{i=1}^{m} P_{S,i} + \Sigma \Delta P_{loss}, \quad (1)$$

where $P_{G,i}$ is the active power generated from the i^{th} generator, $i = 1,\ldots,n$; $P_{flexible\ L,i}$ is the active power consumed from the i^{th} flexible load, $i = 1,\ldots,f$; $P_{partially\ \ flexible\ L,i}$ - active power consumed from the i^{th} partially flexible load, $i = 1,\ldots,g$; $P_{non-flexible\ L,i}$ - active power consumed from the i^{th} non-flexible load, $i = 1,\ldots,h$; $P_{S,i}$ - active power consumed or emitted from the i^{th} storage device, $i = 1,\ldots,m$.

The flexible load power management is supported is supported by a smart load controller [11, 12] using modified positive voltage droop.

III. TEST SYSTEM

The test system represents a microgrid consisting of the following physical models (Fig. 1):

- Pelton turbine (T);
- three phase generator (G);
- power lines (W1) and (W2);
- non-flexible loads (Rnf); `
- flexible load connected to the microgrid via smart load controller Sitalkes 4600 (SLC);
- three phase circuit breaker (Q);
- power transformer (T1);
- low voltage distribution Power system (S).

The study considers the system physical model performance under constant turbine water flow rate and constant voltage applied to the excitation winding of the synchronous generator.

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Fig. 1. Physical model

IV. PHYSICAL MODEL

To estimate the functionality of the control concept and the smart load controller hardware realization a physical model of a test microgrid system is configured in the Electrical Power System Stability Laboratory of Technical University of Sofia. A general layout of the realized laboratory power hardware test model of the microgrid is presented on Fig. 2. Some of the major nominal parameters of the microgrid model elements for this test are: Transformer: UT1=1 p.u., Generator: UG=1,05 p.u., PG=0,8p.u., IGf =0,7p.u.; Power lines: RW1= RW2= 1 Ω; Load: Pflexible=1p.u.W; Pnon-flexible=0,07p.u.

V. TEST CASE

To estimate the control concept and hardware realization performance the following test cases are studied.

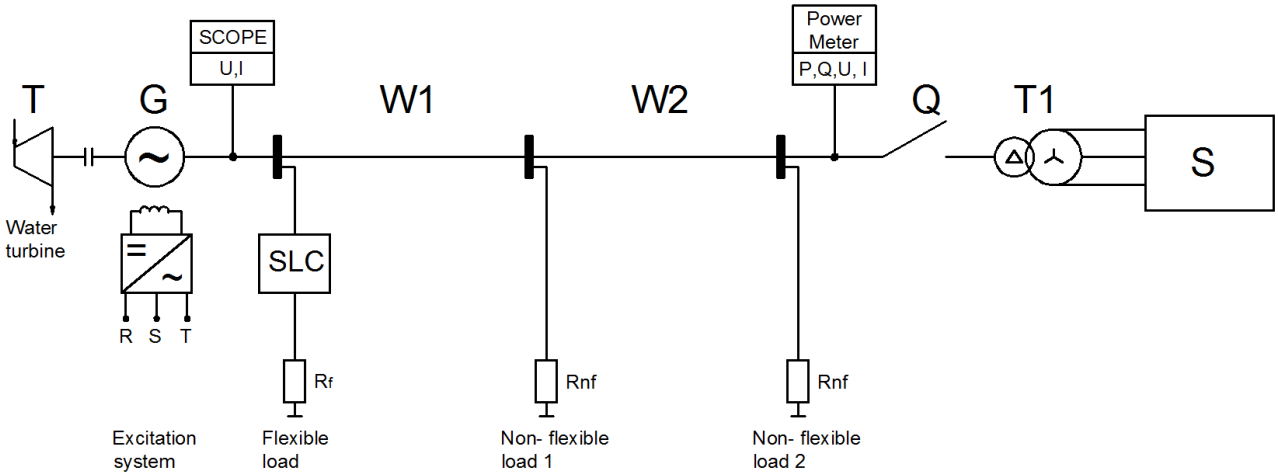

Fig. 2. General layout of the power hardware model of the test system

The microgrid is connected to the power system (S) via circuit breaker (Q). The non-flexible load is supplied by the hydro generator and the surplus active power is fed into the power system (S). A contingency of island mode occurrence

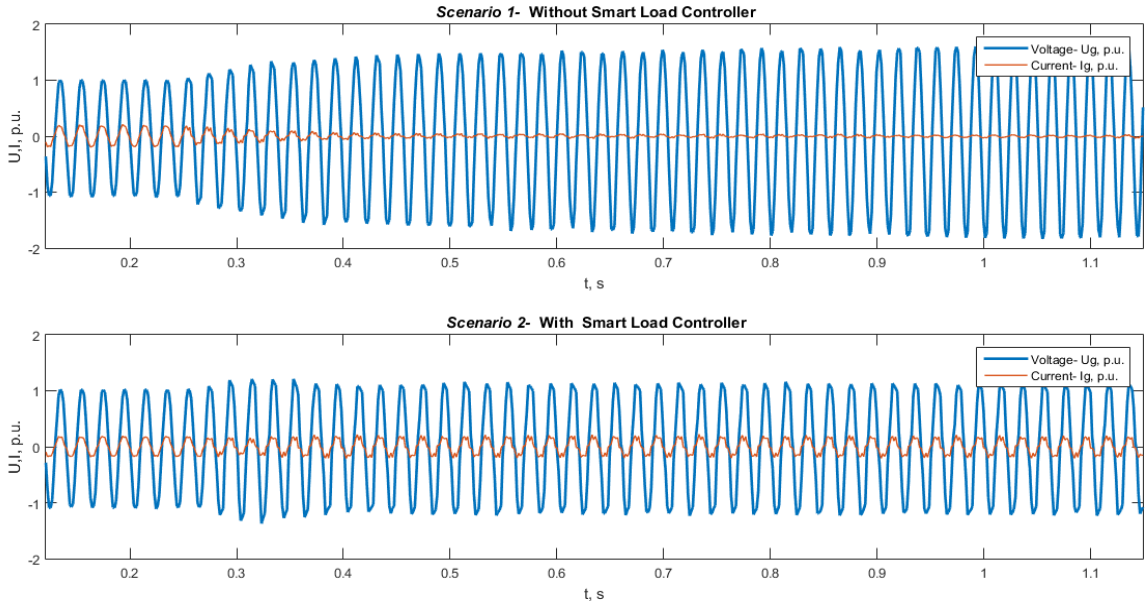

Fig. 3. Recorded voltage and current values with and without smart load controller

is considered. Suddenly the circuit breaker Q trips and in this manner the microgrid remains in autonomous (island) mode. Two test scenarios are considered and realized:

Scenario 1- none smart load controller is present;

Scenario 2- a smart load controller Sitalkes 4600 with the control principle described above is implemented.

VI. RESULTS

Before the contingency occurrence the circuit breaker is switched on. A normal operational state between the generator G and the system S is observed. Under this grid connected mode the microgrid voltage and frequency are dictated by the main power system (S) and thus remain close to their nominal values of 1 per unit (p.u.). The generator's rotor angular velocity and revolutions per minute remain nearly equal to 1 p.u.

A. Scenario 1

The upper section of Fig. 3 presents the voltage and the current before and after the contingency occurrence without smart load controller interaction. By turning the circuit breaker Q off, the power balance (1) is no longer present. The mechanical power supplied by the turbine remains nearly constant but the surplus power cannot be fed into the power system (S) anymore. Thus the generated power remains higher than the load power. As a result the voltage, frequency and the rotor speed of the generator start to increase. In approximately 0,9 s after the contingency the voltage reaches 1,65 p.u. which could be considered as unacceptably high value. Table 2 presents the main steady state microgrid parameters before and after the island mode occurrence. The line to line voltages U_{12},U_{23},U_{31} are given in Volts (V) and per unit (p.u.)

TABLE 1

Grid connected mode				
U_{12}, V	U_{23}, V	U_{13}, V	f, Hz	n, rpm
119,94	119,41	119,25	50,02	1500
U_{12}, p.u.	U_{23}, p.u.	U_{13}, p.u.	f, p.u.	n, p.u.
0,9995	0,9951	0,9938	1,0004	1,000
Island mode				
U_{12}, V	U_{23}, V	U_{13}, V	f, Hz	n, rpm
200,2	200,2	200,3	61,2	1840
U_{12}, p.u.	U_{23}, p.u.	U_{13}, p.u.	f, p.u.	n, p.u.
1,6683	1,6683	1,6692	1,2240	1,2267

It could be clearly noted that the high voltage and frequency settled in this island mode could harm and even be dangerous for both producers and consumers.

B. Scenario 2

The lower section of Fig.3 presents the voltage and current before and after the contingency occurrence with the smart load controller interaction. In this case with turning off the circuit breaker the voltage slightly increases (Fig. 3 and Fig. 4) after which the controller reacts and adapts the flexible load power in order to maintain the voltage and the frequency within admissible range.

Table 3 presents the steady state parameters before and after the island mode occurrence.

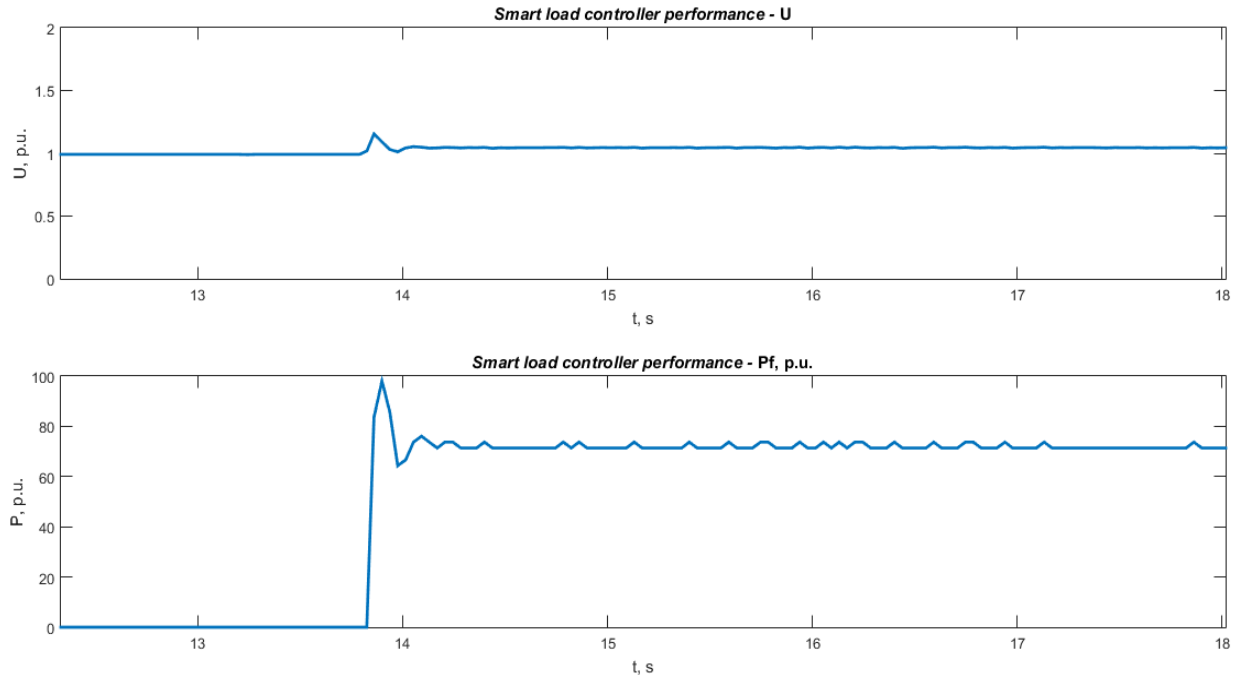

Fig. 4. Recorded smart load controller voltage and flexible load power

TABLE2

Grid connected mode				
U12, V	U23, V	U13, V	f, Hz	n, rpm
120,3	119,7	119,6	50,06	1501
U12, p.u.	U23, p.u.	U13, p.u.	f, p.u.	n, p.u.
1,0025	0,9975	0,9967	1,0012	1,0007

Island mode				
U_{12}, V	U_{23}, V	U_{13}, V	f, Hz	n, rpm
131,6	131,72	131,7	50,07	1502
U_{12}, p.u.	U_{23}, p.u.	U_{13}, p.u.	f, p.u.	n, p.u.
1,0967	1,0977	1,0975	1,0014	1,0013

Due to the smart load controller interaction the microgrid voltage and frequency remain with acceptable values after the island mode occurrence.

VII. CONCLUSION

The approach for smart active power management in micro and nanogrids under island and grid- connected mode given in [1] is tested and evaluated. The mircrogrid hardware set up enable small scale experimental evaluation which provides valuable results. The analysis of the results proves the functionality of the proposed concept and electronic smart load controller. The approach and hardware realization offer a cost effective solution to the main issues related to normal and stable micro and nanogrid operation under grid connected and island mode.

It also provides powerful active power balancing support features to the bulk power system. The laboratory tests have successfully confirmed that the solution performs dynamically adaptive and responsibly oriented according to the grid and also according to the other grid users both locally and externally. Additionally the solution provides more efficient use of the energy and ensures and safe operation of the existing micro and nanogrids.

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Energy Performance Modeling of a Stand-Alone PV System Using Real Meteorological Data

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Abstract – **The paper evaluates energy performance of stand-alone PV systems. The main parameters of the system are obtained by proper models based on real meteorological data. Recommendations are derived for stand-alone PV-systems with boost charge controller based on the performance evaluation. MATLAB Simulink models are developed and long period operation is simulated for PV-systems with common MPPT algorithms and without MPPT. The annual increase of the energy output of the system was found to be 19%, if a MPPT algorithm is implemented. The derived guidelines and results can be further used for the decision-making process of PV-standalone system development.**

Keywords – **Boost Charge Controller, Energy Performance, System Modeling, MPPT, Stand-Alone Photovoltaic System**

I. Introduction

Since the end of 2016 the solar energy is recognized as cheapest energy in more than 30 countries [1], [2]. Taking into account also the Paris agreement and the trend of installing small residential renewable electrical generation, it can be expected that in the following years the share of the energy market taken by small photovoltaic power systems will increase drastically. This however, introduces new problems to the European grid system such as effective use of these distributed power generations, load and generation planning for the grid balance, etc. [3]. The focus of the current researches and modeling software is on grid connected renewable generation which leaves a gap for studies on the effective use of small residential and especially stand-alone systems, not only for the specific conditions, but for a whole year. Therefore, the main purpose of this paper will be modeling and simulating a small 104Wp stand-alone photovoltaic system with a boost charge controller and constant load. The outcome of the study will be used in the future for recommendations and further research on opportunities for optimization the annual energy and cost performance of small stand-alone photovoltaic systems.

II. Systems Topology

For this particular report three different stand-alone photovoltaic systems are developed. All of them consist of a PV array, Boost Charge Controller, Lead-Acid battery and a directly coupled DC load, Fig.1.

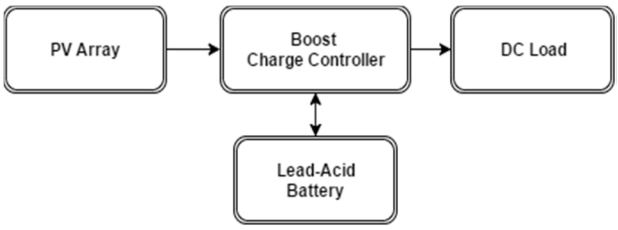

Fig.1. Block diagram of a Stand-Alone PV - System

Two of the systems use MPPT algorithms for Duty cycle (D) control and the third one is left without such a control. The implemented MPPT algorithms are Perturb and Observe, Incremental Conductance.

III. Methodology

The following model is developed in order the energy performance of a PV-system during a whole year to be simulated. This is done by simulating different days (24h) during a whole year and later analyzing the results.

A. Input Data

The simulation uses real methodological data from the meteorological station of Technical University of Varna for Feb-2012 – Feb 2013. The input data for a whole day are discretized on steps of 10 min and consist of information about Irradiation, Ambient Temperature and Wind for 43°13.3858'N, 27°56.3065'E (Varna, Bulgaria) [4]. The irradiation during a summer day is presented in Fig 2.

B. PV-array model

The PV-array is modeled by the predefined Simulink block made by Mathworks. The input data required are irradiation and internal cell temperature. The equivalent single diode circuit of a PV-module can be seen in Fig. 3 [5].

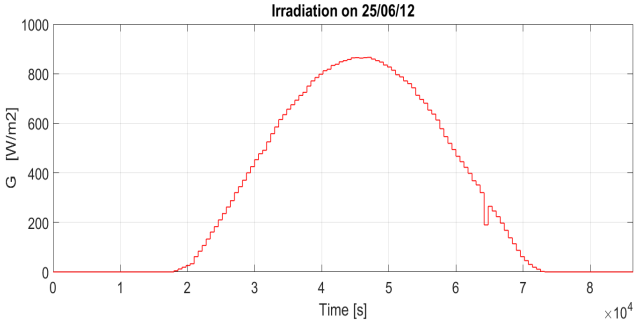

Fig. 2. Measured irradiation on 25/06/12

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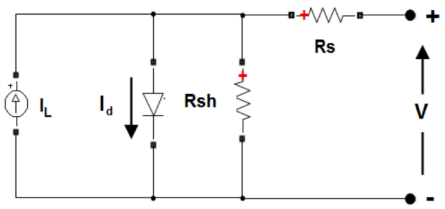

Fig. 3. PV- module equivalent circuit [5]

For the estimation of the internal cell temperature an improved 'NOCT-2p' model is selected and implemented, see Eq. 1. The model outperforms the accuracy of the standard NOCT model by taking into account not only the irradiance (G) in W/m2 and the ambient temperature (Tamb) in °C, but also the wind speed (W) in m/s and two empirical parameters b, c, dependent by the type of the solar cells. See Table 1 for PV-characteristics [6], [7].

$$T_m = T_{amb} + b\left[\frac{G}{800}(NOCT - 20°C)\right] + c(W-1) \quad (1)$$

TABLE 1. BIPV052-S86 CHARACTERISTICS [7]

Technology	poly-Si
P mpp	52W
Voc	8.7 V
Isc	8.07 A
MPP	6.79V 7.65A
Cross area	0.53 m^2
Array- config.	2 panels in parallel

C. Charge controller

The main function of a charge controller is to keep the battery charged and to prevent it overcharge by the PV-array or over-discharge by the systems loads [8]. The boost charge controller achieves that through PWM control of the voltage and current in the system. An ideal boost charge controller converts the voltage and current by controlling the Duty cycle (D), see Eq.2:

$$\frac{V_{out}}{V_{in}} = \frac{1}{1-D}, \quad \frac{I_{out}}{I_{in}} = 1 - D \quad (2)$$

In the cases of soft switching boost converters [9], [10], [11] various relations are possible depending on the control strategy. For the purposes of this report, a boost controller is modeled with an IGBT switching device working on a 5 kHz frequency. The relatively small frequency is selected for computational power point of view. The control is achieved through a PWM generator with an input D – either generated by the MPPT algorithm or predefined constant value for the model without MPPT. The complete architecture of the boost controller is shown in Fig.4. Further improvements and modeling of the inductor in the circuit in order to increase the efficiency could be done based on approches mentioned in [12], [13].

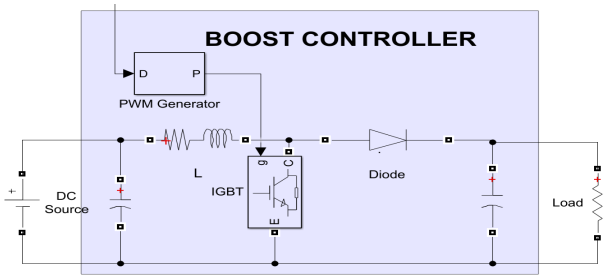

Fig. 4. Simulink model of boost charge controller

D. MPPT algorithms

In order to keep the PV-array power output close to the maximum possible value for the specific moment, a maximum power point tracking (MPPT) algorithm for D control is often installed. Many different MPPT techniques are developed, but Perturb & Disturb and Incremental Conductance algorithms can be designated as the most common choice for small stand-alone PV-systems [14].
Both of the algorithms use feedback information for the voltage and current output of the PV-array (Vpv, Ipv). The methodology of control of the D however, is different.

E. DC load

A good representation of applications of the stand-alone system can be an outdoor lighting, back up alarm systems, remotely located sensor stations, etc. Many of these loads have requirement for two days of autonomy use. Therefore, a good estimation of the load can be a 5Ω resistor connected in parallel to the battery turned on for the whole simulation.

F. Battery

Due to the mismatch between the power generation and the load profiles, every sustainable power system needs an energy storage device. The most common choice for energy storage of a stand-alone PV-system is the Lead-Acid battery due to its availability, low price, scalability and well-studied performance.

For the estimations of the battery characteristics of the PV-system, the two days of autonomy requirement is taken into account. This sizing technique results to the following parameters: V=12V, Capacity 120Ah, SoC is 60%.

G. Overview of the system

All the components explained in the chapter are interconnected in a model and the results of this MATLAB-Simulink PV-system can be seen in Fig.5, Fig.6.

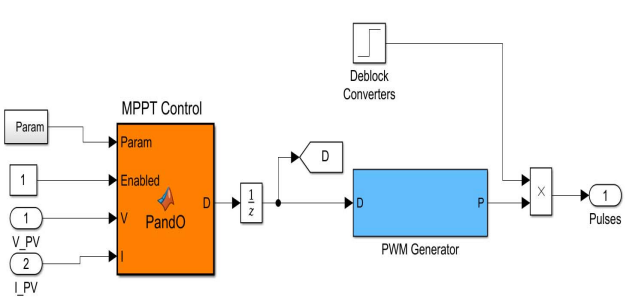

Fig. 5. MPPT charge controller with PWM generator

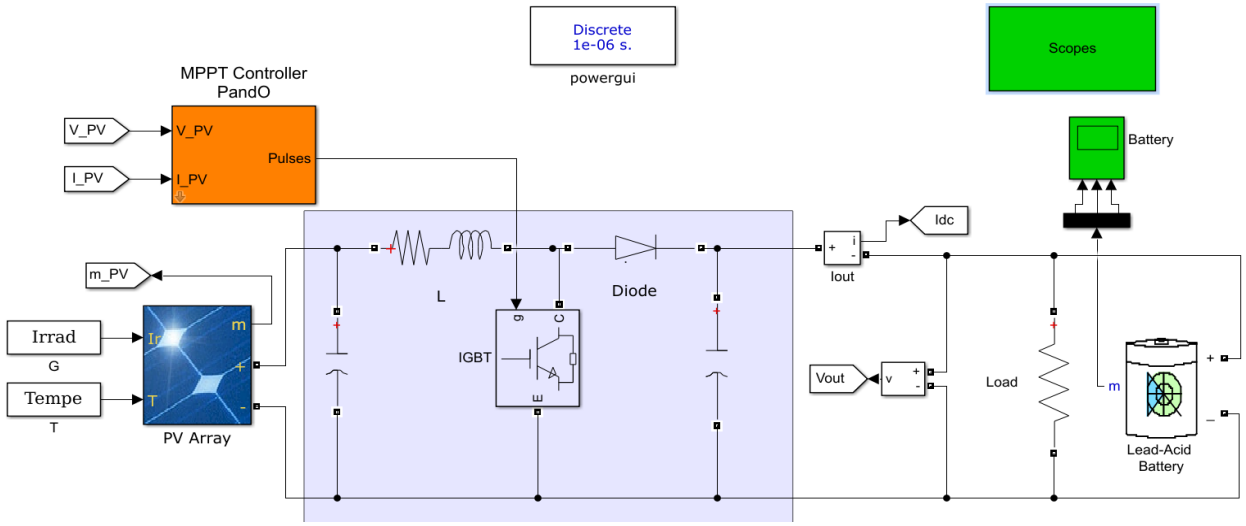

Fig. 6. Matlab Simulink model of the stand-alone PV-system

IV. Results and Discussion

In order to understand the energy performance of the proposed stand-alone PV-system, the models are simulated for 24 full days, distributed between 02.2012-01.2013. For the simulations, various parameters are monitored including the PV-array output (Vpv, Ipv, Ppv), Boost controller output (Vdc, Idc, Ppv) and the Lead-acid battery State (Vbat, Ibat, SoC).

First, it is studied the effect of the MPPT algorithms on the power output of the system, see Fig.7. The results clearly point out that the power output of the systems with an MPPT algorithm manages to keep the power output close to the maximum possible value, which increases the overall energy performance. The small difference between the irradiance and the P&O system can be explained with the high internal cell temperature between 11:00 and 14:30. The Non-MPPT system however, is capable to deliver close to the maximum power only in the low irradiation conditions and only with slight change of the irradiation values. The simulation shows that once the rate of change of the irradiation increases for high irradiance, the non-MPPT system starts to lag and does not manage to keep increasing the power output.

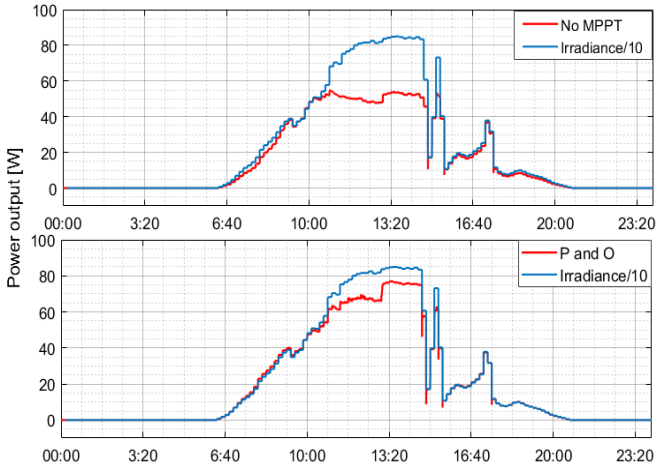

Fig. 7. Power output of the system on 11.03.12

The second set of parameters, which are collected for analysis, are the average daily conversion efficiencies of the system. The distribution and the values of these efficiencies are presented in Fig.8. As it can be seen, there is almost complete overlap of efficiencies between the two MPPT systems. The PV-system without an MPPT however, has lower efficiency for all simulated days. The relative increase with an MPPT is between 6% and 40%, dependent on the weather conditions during the day. Highest difference between the two approaches is found to be in the days with rapidly change in the irradiation or in other words days with changing cloudiness with sunny weather (25/May, 25/ Oct). For the days with clear sky or constant low radiation conditions, the non-MPPT system tends to keep close to the MPPT system. On 10th October the irradiation is relatively low and constant during the day. This approximately constant irradiation and the predefined D settings allow the non-MPPT system to decrease the difference to only 6% of the overall energy output, which is the best performance found by the simulations.

During the year, the relative efficiency of all the systems is highest for the winter months and lowest for the summer months. This can be explained with the lower ambient temperature and lower irradiance. However it is important to note, that the solar energy during the winter months is only 15.2% of the overall annual solar energy potential.

The average annual efficiency between the energy output of the system and the solar energy is also calculated and compared for all the systems. It is found annual efficiency

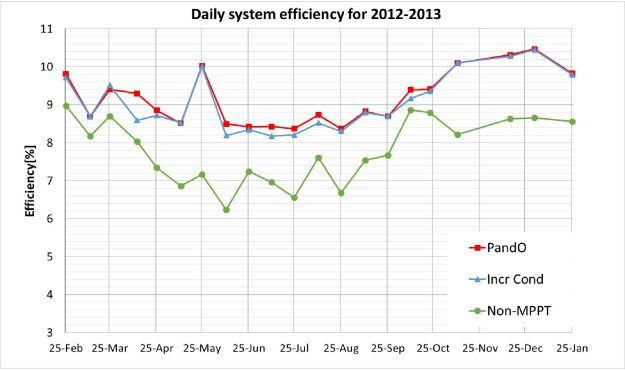

Fig. 8. Daily energy efficiency through the whole period

of 8.95%, 8.81% and 7.55% respectively for the model with Perturb and Disturb MPPT, with Incremental conductance MPPT and without an MPPT. From this, it can be concluded that the two MPPT systems have similar energy performance, which is increase of 19% of the final energy delivered to the loads and the battery. Consequently, the maximum energy output of the system for a whole year is increased from 121kWh to 143.7kWh with integrating a MPPT algorithm.

The presented results about the energy performance of the systems with and without MPPT controller can be further used for an informed choice related to the type and the sizing of the boost controller for a stand-alone PV-system in North-East Bulgaria. In order to do that a linear payback period analysis is performed for the cost difference between MPPT and non-MPPT controllers. The outcome of this analysis is presented in Fig.9. The analysis demonstrates that currently the investments for more expensive MPPT controller are paid back after at least 8 years, assuming the same annual energy output difference and constant electricity price - 0.40€/kWh. Therefore, this report recommends integration of a MPPT boost charge controller if the cost difference between the MPPT and non-MPPT controller is lower than 55€ due to the longer payback period than the predefined desired 7 years. Such small difference is not common, but it is expected to become possible in the near future, which is the scope of this research.

Currently the equipment of TU Varna could provide similar meteorological measurements for North Bulgaria. Therefore, it is also recommended to apply the same model and analysis method for the other possible locations for all types of PV-systems.

V. Conclusion

The paper evaluates energy performance of stand-alone PV systems. The main parameters of the system are obtained by modeling based on real meteorological data. Guidelines are derived for stand-alone PV-systems with boost charge controller based on the performance evaluation.

MATLAB Simulink models were developed to investigate a stand-alone PV-system using boost charge controller and two poly-Si PV-panels with and without MPPTs.

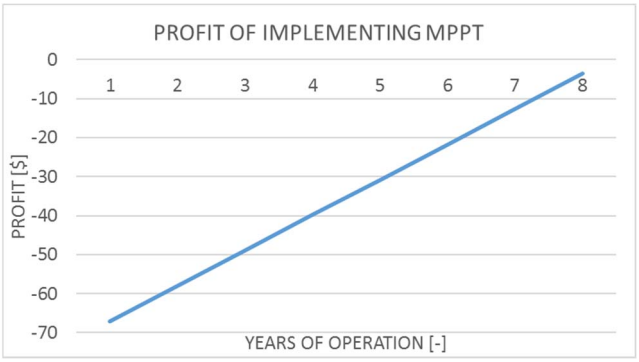

Fig. 9. Profit through the years by implementing MPPT

The models are simulated for a sufficient period and obtained results show an average annual efficiency of 8.95% and 8.81% for the systems with MPPT control and 7.55% for the system without MPPT.

Finally, a simple linear economic analysis is performed which recommends using a MPPT charge controller. The authors of the report recommend automation of this decision making process using the same modeling approach process for different locations in Bulgaria and for other types of charge controllers.

VI. Acknowledgment

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A Test System for the Front-End Electronics of the PADME charged particle detector system

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Abstract – **The PADME charged particle detector system aims to detect positrons and electrons with efficiency better than 99 % and time resolution below 1 ns. The system hosts about 200 readout electronics channels whose operation has to be verified and commissioned. A custom based test system allowing performing qualitative check of the detector and the front-end electronics has been developed. The initial tests and the performance of the front-end electronics are described and discussed. Time resolution better than 400 ps was achieved.**

Keywords – **scintillation detectors, front-end electronics, LED driver.**

I. INTRODUCTION

The PADME experiment at LNF-INFN [1] is devoted to the search for new neutral particles A' produced in the positron-on-target annihilation process. The process of interest is $e^+e^- \rightarrow \gamma A'$ and only the parameters of the recoil photon in the final state are measured. PADME will exploit the positron beam from the DAΦNE Linac with energy of 550 MeV [2]. This provides access to A' mass range up to 23.7 MeV. A GEANT4 schematics of the proposed experimental setup is shown in fig. 1.

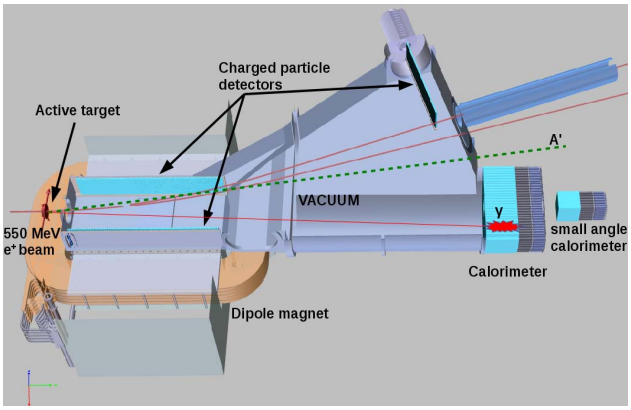

Fig. 1. A schematics of the PADME setup

The positrons interact in a 100 um thick polycrystalline diamond target which will also provide measurement of the beam profile. The recoil photon energy and position will be measured by an electromagnetic calorimeter (ECAL), located 300 cm downstream of the target. A dipole magnet with 0.6 T magnetic field will deflect the non interacted beam outside the acceptance of the ECAL. The positrons that undergo high energy loss through bremsstrahlung emission in the target will experience stronger deflection and will be detected by a charged particle detector placed inside the gap of the magnet. The whole experimental setup will be placed in vacuum to minimize background from beam-gas interactions.

II. THE PADME CHARGED PARTICLE VETO SYSTEM

A. General description

The events with bremsstrahlung photons represent one of the dominant components in the background, relevant to the search for new particles in the $e^+e^- \rightarrow \gamma A'$ process. The suppression of these type of events relies on the efficient detection of the emitting positron and a dedicated system serving this task is foreseen at PADME [3]. The charged particle veto system is composed by detectors made from polystyrene plastic scintillator bars. Each bar has dimensions 10 x 10 x 184 mm^2. The scintillation light is collected by a 1.2 mm diameter BCF-92 wave-length shifting fibre, placed inside a 1.3 x 1.3 mm^2 groove along the scintillator bar. A minimally ionizing particle deposits around 1.8 MeV of energy in the scintillator bar resulting in about O(100) photo-electrons emitted in a photodetector with O(20 %) quantum efficiency.

Three sets of charged particle detectors will be used at PADME – two, each made of 96 scintillator bars, will be placed within the magnetic field of the dipole magnet and will detect positrons and electrons with momentum less than 450 MeV. An additional array of scintillator bars will be located further downstream and close to the non-interacted beam in order to provide detection of positrons with momentum up to 500 MeV.

B. Block diagram and specifications of the SiPM front end electronics

The captured light by the WLS fiber is read out by a Hamamatsu 3 x 3 mm^2 silicone photomultipliers (S12752 SiPM). The SiPMs are placed onto a custom developed optoelectronic modules, realized on a PCB. Each PCB module hosts four identical readout channels. A single channel includes the SiPM itself, a transimpedance amplifier, a buffer, a dedicated high voltage regulation module, as well as a circuit to monitor the voltage supply and the current through the photodetector (fig. 2).

The relevant parameters for a single channel of the front end electronics are given below.

- Fixed Gain =4
- Type of output differential =100Ω

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- Bandwidth =70MHz
- Excellent stability with less C_{in} <500pF
- Repetition rate of more >1MHz
- Pulse resolution better than <10ns
- Dynamics of the output signal =1V
- Total noise with C_{in} 2 pF equivalent =2nV/√Hz
- Input protection =300mJ
- Single power supply =8V

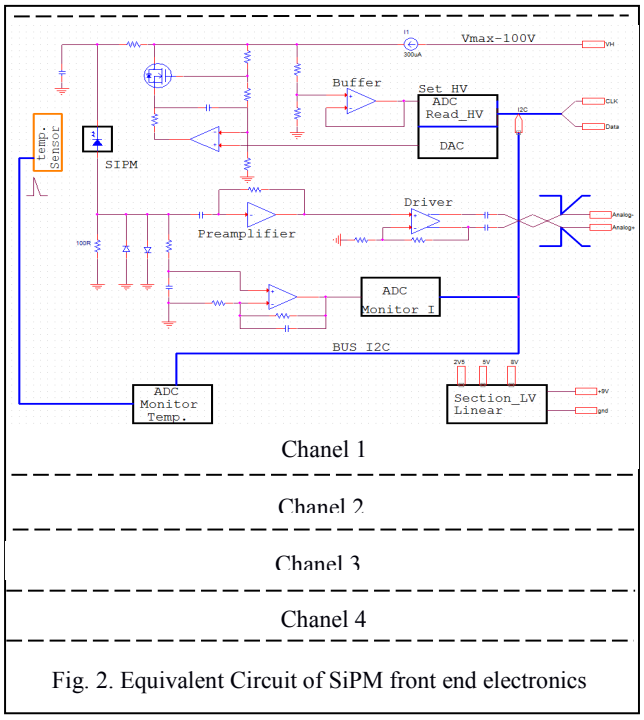

Fig. 2. Equivalent Circuit of SiPM front end electronics

- Dissipated power for channel =35mW

The small power dissipation is important for the operation of the FEE electronics in vacuum. A special care was taken to allow efficient heat transfer through the scintillator support structure to the walls of the vacuum chamber. A preliminary prototype of the possible detector assembly is shown in fig. 3. The scintillator bars are rotated at 0.1 rad to avoid inefficiency for positrons traversing perpendicularly the detector plane.

III. DETECTOR AND FRONT-END ELECTRONICS COMMISSIONING

A. FEE tests justification

The complete charged particle detection system will contain at least O(300) individual readout channels. PADME collaboration also considers the possibility to equip both sides of the plastic scintillator bars with photodetectors which will double the amount of the necessary electronics channels. The operation of all these channels has to be tuned and kept at nominal.

Two types of tests are required for the certification of the proper and efficient operation of the RO electronics – commissioning and continuous. The initial commissioning of the RO electronics will be executed in Sofia and has the goal to select and install only the defect free channels. However, due to the stringent requirements on the time resolution of the charged particle veto detector, namely below 1 ns, the operation of the RO electronics should also be monitored in-situ throughout the data taking of the experiment. The accelerator repetition rate, 50 Hz, allows

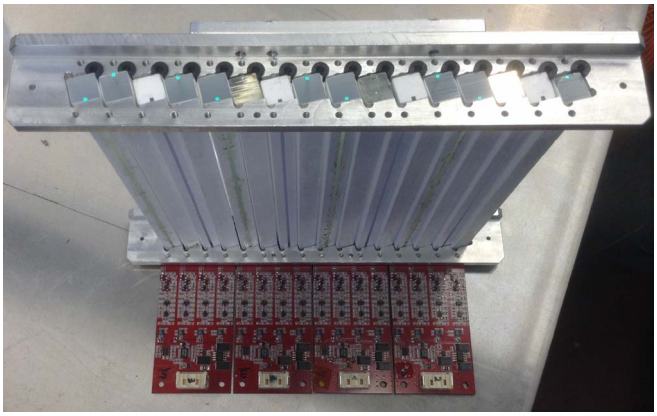

Fig 3. A prototype assembly of the charged particle veto scintillator bars together with a prototype of the front-end electronics readout coupled to the plastics scintillators

performing out-of-spill measurements of the stability of the gain and the light output of the scintillators.

B. Elements of the system to be monitored

The complete detection system consists of a plastic scintillator, a wave-length shifting fibre and a photodetector. The solvents in the plastic base absorb UV light and re-emit it in the blue part of the visible spectrum, with maximal emission at around 420 nm. The blue light is further absorbed in the WLS fibre which emits light in the green part of the spectrum, with maximal emission at 492 nm. Depending on the available light source, different aspects of the detection system could be tested:

- Operation of the photodetectors: Due to the employment of WLS fibres the operation and the functional performance of the FEE-cards hosting four photodetectors should be tested with green light. This can be achieved by using a 505 nm LED.
- WLS fibres structural integrity: The WLS fibres are one of the most sensitive components of the system. Minor defects along the fibre serve as absorption centres and decrease the total light output per unit of deposited energy inside the scintillator. The WLS fibre light transmission can be checked with blue light, directed towards the non-equipped end of the scintillator bar.
- Plastic scintillator light emission: The overall performance of the system can be checked with UV light. This scheme consequently validates each of the components of the detection system.

C. Test system requirements

The ideal test system for the study of the operation of the front-end electronics cards should be able to test all the critical elements. It should incorporate three light emitters at different wave-length – green, blue and ultraviolet. It should allow individual regulation for each of the three light beams. In addition to the continuous light emission, the test system should also have the possibility to emit short light pulses with minimal duration of 10 ns. It is also desirable that the pulse duration can be varied in the O(10 ns) range. The system should also provide external reference signal, allowing synchronizing any additional electronics with the generation of the light pulse. Such a

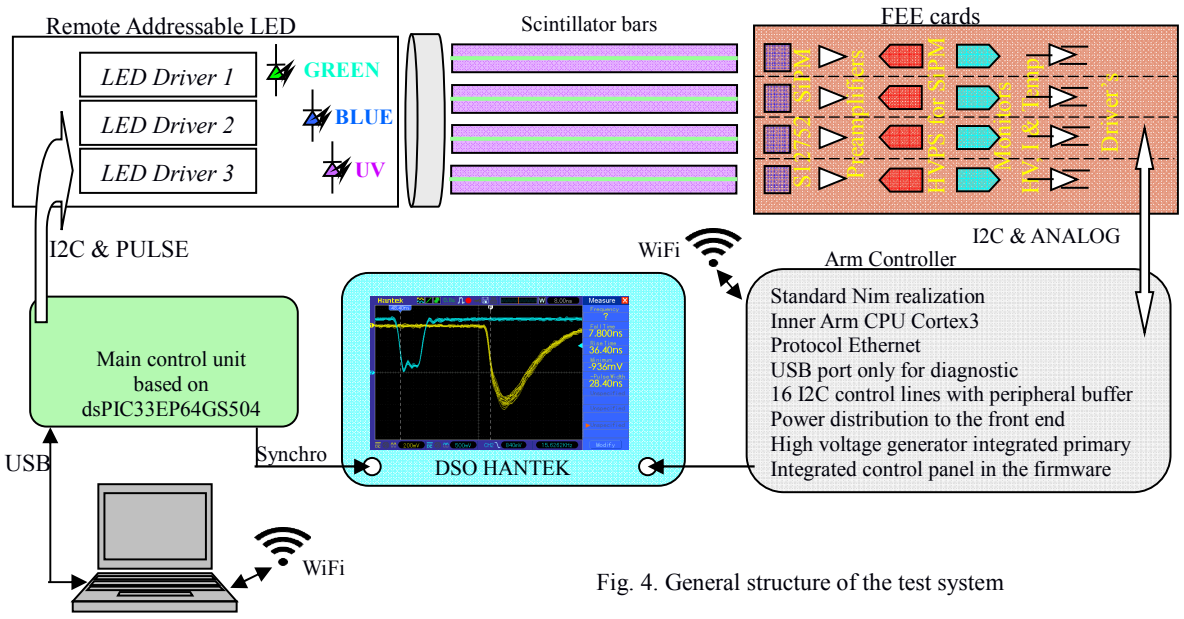

Fig. 4. General structure of the test system

system could be achieved, with few modifications, by using the development described in [4].

The output pulses of the front-end electronics are translated from differential to single ended inside the SiPM card controller and are further used to determine the properties of physical interest – the arrival time of the pulse, its amplitude and the collected charge. During the initial test of the FEE cards, the shape, the amplitude, and the signal delay could be controlled by a digital oscilloscope with sampling rate of 1 GS/s and bandwidth of at least 200 MHz.

IV. TEST SYSTEM PERFORMANCE AND RESULTS

A dedicated system allowing to check the functional operation and to determine the parameters of the individual channels of the detector system has been developed. By construction, it satisfies all the requirements mentioned above.

A. Design of the setup

The general block schematics of the test system is shown in fig. 4. The objects to be tested are the 4-channel light pulse detection modules, the wave-length shifting fibers, and the scintillation detector as a whole. The light is emitted from the LED driver and is directly registered from the SiPM, locate in the FEE card. Initially, the LED driver was coupled directly to the SiPM front-end electronics and the performance was checked with two regimes of operation — continuous and pulsed light emission.

B. Continuous light mode

The continuous light regime of the LED driver was used to check the linearity of combined emission-detection response of the system. The LED driver allows to vary the current through each of the three LED separately up to 32 mA in steps of 1 mA.

The SiPMs were powered through the controller to their nominal voltage provided by the producer (around 67 V), which assures a gain of $5.5*10^5$. The SiPM current was measured in two different ways — using the built-in controller circuit and with a digital voltmeter by reading the voltage across the 100 ohm resistors connecting the SiPM to the ground. The two values were found to be equal in the whole range of the LED light intensity scan, thus verifying the implemented on-board current measurement. The obtained values are shown in fig. 5, separately for the

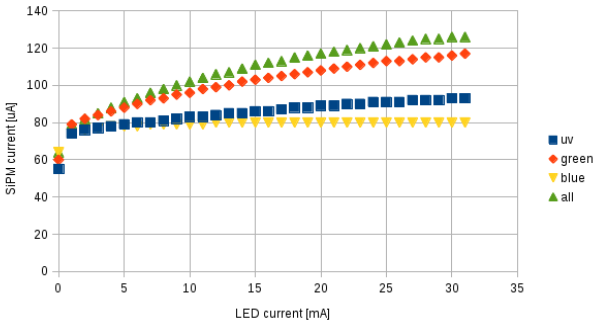

Fig. 5 Dependence of the SiPM current as a function of the LED current

green, blue and ultraviolet LED, and when they are switched on simultaneously.

The response of the system was found to be linear for SiPM currents up to 100 μA. This corresponds to a voltage drop of about 10 mV over the 100 ohm resistor. Since the gain variation of the SiPM for 10 mV is negligible, the non-linearity which is observed at high light intensity was attributed to the increased probability for two photons hitting the same SiPM pixel before it recovers from the break-down.

Fig.6 An oscillogramme of the pulses from the SiPM FEE.

C. *Pulsed mode*

The nominal operation of the light detection electronics will be related to the measurement of the properties of signal from a scintillation pulses from the charged particles traversing the detector. The employed LED driver has the

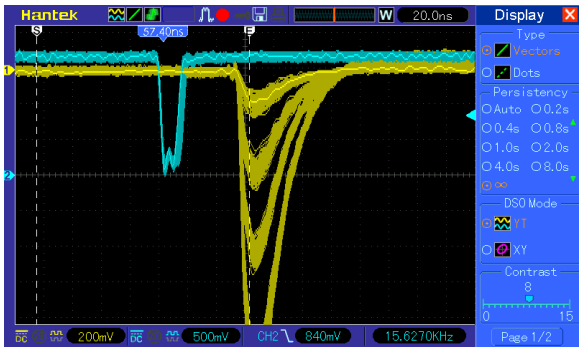

Fig. 7 Oscilogrammes of the output pulses of the SiPM FEE for LED pulses duration from 13 ns to 16 ns. The reference signal is also shown

possibility to emit pulses with variable and controllable duration in the interval 8 ns – 65 us, period – up to 65 us, and phase with respect to a reference signal. For the present test the duration of the pulses was fixed to 15 ns. The properties of a output from the FEE electronics to a pulses with 12 mA current through the LED are shown in fig. 6. The pulse has an 8 ns rise time and duration of 36 ns. Fig. 7 shows the increase of the pulse amplitude when changing the LED pulse duration from 13 ns to 16 ns. This reflects the total emitted light and the corresponding collected charge of the SiPM.

The signals from the four SiPM front-end electronics channels were fed into a CAEN V1751 digitizer, sampling at 1 GS/s with 10 bit resolution [5]. The total charge was reconstructed by integrating the measured amplitudes after pedestal subtraction over an interval of 280 ns. A medium duration run was taken to check the stability of the operation of the whole system – the LED driver, the SiPM and the front-end electronics. The average reconstructed charge for each of the four channels of a single FEE card is shown in fig. 8. The error bars indicate the RMS of the charge distribution in each of the 5 s time intervals.

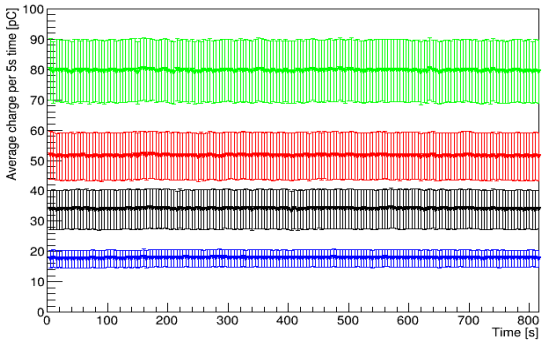

Fig. 8 Average charge stability over an interval of 800 s

The digitizer data allows also to perform the reconstruction of the time of the signal pulses. It was derived separately for each SiPM as the time of the zero-crossing using the time of the signal when it reaches 20 mV and 40 mV. The distribution of the time difference between the reconstructed times for two channels for each LED pulse is shown in fig. 9.

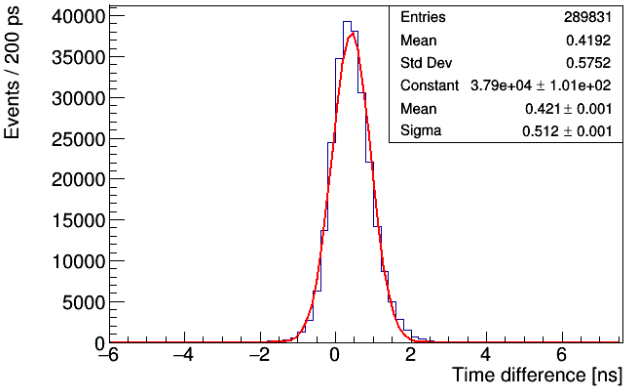

Fig 9. Time difference between two SiPM channels

The difference was approximated by a Gaussian with a sigma of 512 ps. By assuming that the two channels have equal time resolution this translates into a time resolution per single channel of 360 ps. The obtained value is consistent with the PADME requirements.

V. CONCLUSION

The performance of the charged particle veto system of the PADME experiment is crucial for the suppression of the background in the search for new light particles from the positrons suffering hard bremsstrahlung in the target. The presented development focuses on the commissioning and the nominal operation of such a complex multichannel detection system. An effective mechanism for the testing of a large number of detection elements allowing to obtain confidence in their operation and functional operation is described. The results obtained in this work allow to make the conclusion that during the construction of such complex systems it is appropriate to incorporate a testing equipment which can ease the problem discovery procedure and can provide information in advance before the actual execution of the experiment.

VI. ACKNOWLEDGEMENT

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Experimental setup for investigation of optically inhomogeneous objects by the spectral-correlation method

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Abstract – **The description of the experimental setup for investigation of optically inhomogeneous surfaces and objects by spectral correlation method is given. The principle of operation of the device, the essence of the spectral-correlation method and the method of processing the received data are discussed. The results of studies of electrical insulating paper during its thermal aging are present as an example of the use of the experimental setup. The possibility of using spectral correlation method to determine the parameters of the inhomogeneities of the materials for electrical and electronic engineering is shown.**

Keywords– **Spectral correlation, semiconductor laser, diagnostics, image processing, speckles**

I. INTRODUCTION

Interferometric methods are widely used in engineering to determine the deformation of metal and other types of surfaces, detecting the phase inhomogeneity in various environments and for other applications [1]. In the case of diffuse scattering of radiation by the investigating object the use of conventional interferometric methods becomes difficult or impossible. In this case, it is advisable to use speckle interferometric methods [2]. A detailed description of speckle interference methods are given in the review [3].

There are speckle-interferometric measurement methods with the use of so-called reference beam and no reference beam. Each of these methods has certain advantages and disadvantages. Classical speckle interferometric methods have very high sensitivity to a spatial change in the position or shape of objects. If such sensitivity is excessive, it is possible to use other interferometric methods, such as [4, 5].

The use of multiple radiation sources with different wavelengths or radiation source with variable wavelength substantially extends the capabilities of classic interferometric methods. In particular, the dependence of the intensity distribution of the scattered coherent light [6-8] of the wavelength of the radiation allows using this property for the diagnosis of optical inhomogeneities. This property is the basis of spectral-correlation method to study the phase-heterogeneous surfaces and objects.

Coherent radiation is scattered on optical inhomogeneities, forms in a surveillance plane spotted pattern called speckle [2-3]. When changing the radiation wavelength is taking place the directed movement of spots and their transformation. The essence of the spectral-correlation method consists in recording the intensity distributions scattered by the studied object at different wavelengths and the detection of statistical regularities of the changes of such distributions using correlation analysis. The cross-correlation function (CCF) of the images of the speckles at different wavelengths is calculated and it's the parameters are used for determination of the characteristic sizes of the scattering object. So, in work [9] showed the possibility of remote determination of the height of surface roughness, thickness of transparent film and plates with a diffusely scattering surfaces.

The research of the CCF of intensity distributions of radiation scattered by the samples of transformer insulating paper was carried out as an example of the use of the described experimental setup. It is known that the parameters of the transformer paper substantially define reliability and durability of operation of power transformers [10-12]. As will be shown below, the technique allows by non-destructive way to assess the degree of impregnation of the paper insulation by dielectric fluid, and also to assess the extent of ageing of paper-impregnated insulation. That can be used to monitor parameters of the paper during thermal aging in a laboratory environment with the aim of creating new types of cellulose for paper-impregnated insulation [13-14] of power transformers.

In this experimental setup uses visible light with the wavelength λ of approximately 650 nm. However, the spectral-correlation method can be applied in the microwave range of wavelengths, where providing of changing of the radiation wavelength is significantly easier.

II. EXPERIMENTAL SETUP

Block scheme of the experimental setup is shown in the Fig. 1. The semiconductor laser 1 ($\lambda \approx 650$ нм, 5 mW) with collimating lens served as an optical radiation source. The beam diameter was approximately 2 mm; the coherence length of the laser radiation was approximately 1 mm. The laser diode was mounted on the Peltier element 2. The laser power supply is carried out from the power source 3 having a high stability and small ripple.

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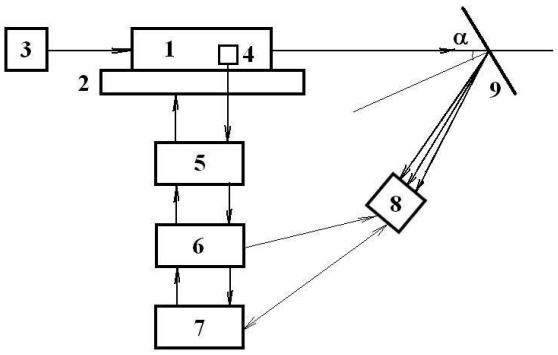

Fig. 1. Block scheme of the experimental setup: 1 – semiconductor laser, 2 – the Peltier element, 3 - power supply, 4 – temperature sensor, 5 – control unit, 6 – synchronization unit, 7 – personal computer, 8 – CCD TV camera, 9 – the sample.

The laser diode was equipped with the temperature sensor 4, the signal from which was entered into the Peltier element control unit 5. Unit 5 was connected with a personal computer 7 via the device of conjugation and synchronization 6. The CCD television camera 8 recorded the video images corresponding to the spatial distribution of the radiation scattered by the examined sample 9. Mode of automatically adjustment the brightness and contrast of the television camera was turned off. The angle of incidence of the beam on the sample relative to the normal does not exceed 10^0. The laser diode and the Peltier element were placed in the flask with double glass wall with vacuum thermal insulation and transparent flat optical window.

The wavelength tuning of the radiation was produced by changing the temperature of the laser diode by changing the current through the Peltier element. Measuring the spatial intensity distributions fulfilled after the establishment of stationary thermal regime of the laser diode. Measurements didn't make at temperatures at which occurred unstable operation of the laser diode. The rate of temperature change was approximately 0.5^0 C per minute. However, no significant reduction in the accuracy of the rate of change of the temperature can be increased to $2^0..5^0$ C per minute. The dependence of the wavelength on the temperature of the emitting diode was measured with the spectrometer "AvaSpec-2048" (Fig. 2).

Experimentally obtained data were approximated by a straight line, the expression for which is given below:

$$\lambda = 649.89 + 0.339 \cdot T \qquad (1)$$

where T is the temperature of the heterojunction laser diode in degrees Celsius. Then the change of wavelength was calculated on the basis of temperature difference.

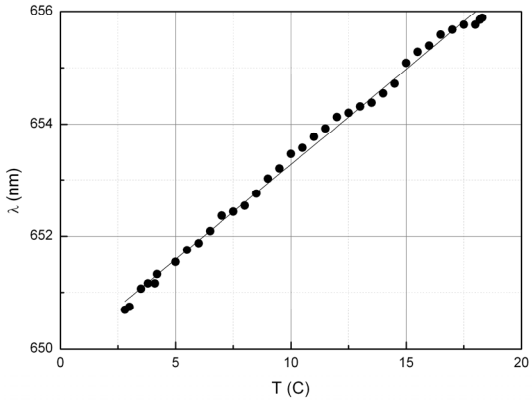

Fig. 2. The dependence of the wavelength on the temperature of the heterojunction laser diode

III. DATA PROCESSING

Cross-correlation functions were calculated regarding the intensity distribution at the initial temperature, i.e. relative to the initial wavelength. With reference to the images that are set in the pixels, the integral expression for the CCF [9] go to:

$$CCF(\Delta i, \Delta j, \lambda_1, \lambda_2) = \sum_{i=ix0-lx}^{ix0+lx} \sum_{j=jy0-ly}^{jy0+ly} V_1 V_2 \qquad (2)$$

where:

$$V_1(i, j, \lambda_1) = I(i, j, \lambda_1) - A(\lambda_1),$$
$$V_2(i, j, \lambda_2) = I(i + \Delta i, j + \Delta j, \lambda_2) - A(\lambda_2),$$

Δi, Δj – are the offset by the axes $0x$, $0y$, $I(i,j,\lambda)$ – is the value of the radiation intensity in the coordinates of the pixel i, j at the wavelength λ, A – is the average intensity value in the area of integration, i.e. for the points for which the summed intensity values was calculated, $ix0$, $jy0$ – coordinates of the center of the square of integration, lx, ly – half-width area of the integration over the corresponding coordinate.

The effect of directional movement of the speckles separated from the so-called boiling of the speckles, by searching for the maximum of the function CCF on the x and y coordinates – CCF_{max}. The dependence of the function CCF_{max} on the difference between the wavelengths $\Delta\lambda$ in which the image obtained characterize the phase heterogeneity of the investigated object. Change this feature under the influence of any factors allows to give some objective assessment of this impact. The results of measuring the dependency CCFmax on $\Delta\lambda$ for electrical insulating paper during the process of artificial thermal aging are presented below as a special case.

III. EXPERIMENT

Electrical insulation paper type K140 for use in power transformers and cables was investigated by spectral correlation method in the process of thermal aging that was carried out according to the methods [12-13].

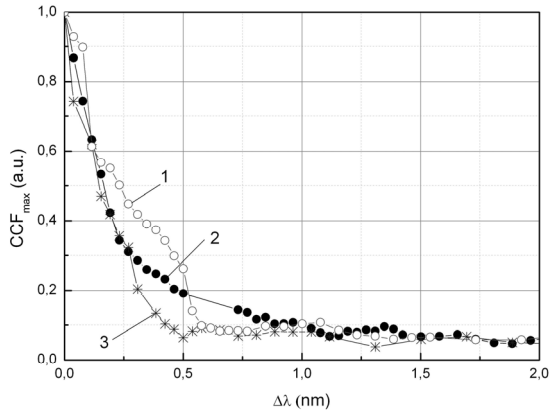

Fig. 3. The CCF_{max} at the thermal aging process of insulation paper K140: 1 – new (befor thermal aging), 2 – after 170 h, 3 – after 530 h.

The calculated dependences CCF_{max} on Δλ are shown in the Fig. 3. It should also be noted that measurable functions are well reproduced under repeated measurements. The data obtained indicate that the degree of aging of this type of insulating paper in the considered range of the duration of the thermal exposure (up to 530 hours inclusive) can be estimated by comparing two values of the function CCF_{max}, calculating the values for Δλ at 0 and, for example, at 0.385 nm. The example of the dependence of expected time of aging on CCF_{max}(0.385) is given in Fig. 4. We assume that this dependence can vary for other materials of natural origin; however, the possibility of estimating of the time of aging using parameters the cross-correlation function can be maintained.

It was found that various types of insulating paper are differ in dependence CCFmax on Δλ, despite the fact that differences in the structure of cellulose fibers is difficult to identify in images obtained by optical or scanning electron microscope. An ability to estimate the magnitude of volumetric heterogeneities in plastic films and electrical insulation of cross-linked polyethylene (XLPE) is demonstrated also.

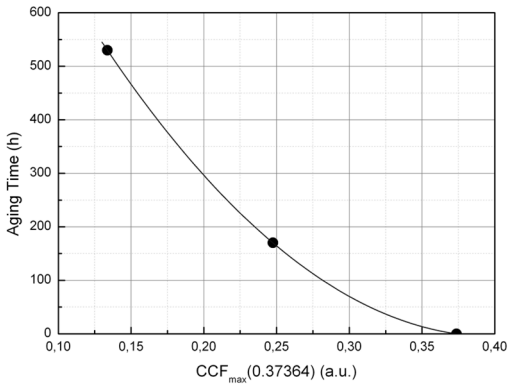

Fig. 4. Dependence of expected time of aging on CCF_{max}(0.385).

IV. Conclusion

Thus, spectral correlation method that is implemented using the described experimental setup allows to estimate the parameters of optical inhomogeneities of different objects and materials that can be used in scientific and educational purposes.

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Synchronization of the distributed readout frontend electronics of the Baby MIND detector

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Abstract – **Baby MIND is a new downstream muon range detector for the WGASCI experiment. This article discusses the distributed readout system and its timing requirements. The paper presents the design of the synchronization subsystem and the results of its test.**

Keywords – **WAGASCI, Baby MIND, neutrino, distributed readout, synchronization**

I. Introduction

A. Detector overview

Baby MIND is a 70 ton modular magnetized iron detector developed and tested at CERN. It will be used as a downstream muon range detector in the WAGASCI experiment on the T2K neutrino beam line in Japan [1].

Fig. 1. Baby MIND detector at T9 beam-line at CERN.

It is composed of multiple magnet and scintillator modules [2]. The modular design allows for easy reconfiguration of the geometry of the detector and flexibility for transport and installation.

B. Readout electronics overview

Figure 1 shows the detector under test at CERN beam-line, with the readout electronics installed in 8 mini-crates on top of the detector. Each mini-crate can accommodate up to 7 Front-End Boards (FEB) (fig. 2). Each FEB can read-out up to 96 detector channels. The data is transferred to the Data Acquisition System (DAQ) via USB 3 interface. The FEBs can work either in standalone mode, in which every FEB is connected to the readout computer via a USB3 connection, or in time division multiplexing (TDM) mode in which all FEBs of a mini-crate are chained and the data is passed to a single USB3 master FEB which sends it to the DAQ. This allows sharing the available data bandwidth and reducing the amount of required cables. There also is a possibility, while in TDM mode, to assign the full USB bandwidth to any selected FEB in the chain.

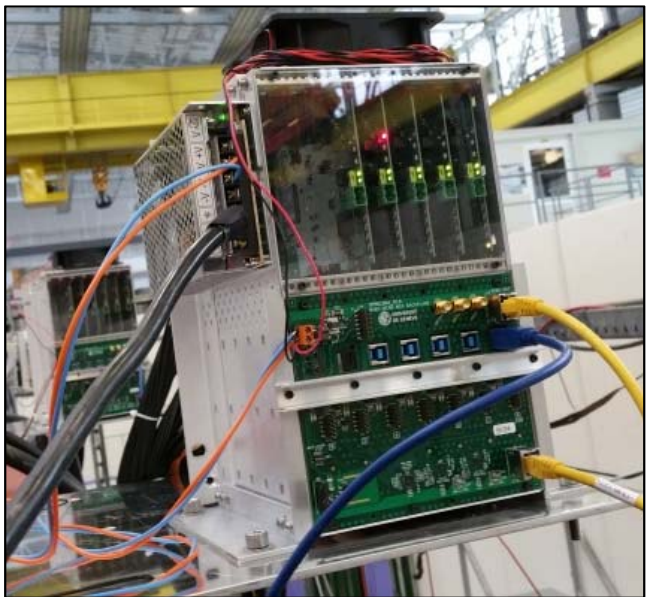

Fig. 2. Frontend electronics mini-crate.

C. Synchronization requirements

In order to achieve a good timing resolution the FEBs run on a 2.5 ns internal clock, synchronized to a common 100 MHz clock. That puts some very tight requirements to the clock and synchronization distribution subsystem. Delays of the global clock delivered to the separate FEBs have to be kept within few hundred picoseconds accounting for all possible delay sources like the difference in the link lengths, chip-to-chip delay difference and signal jitter.

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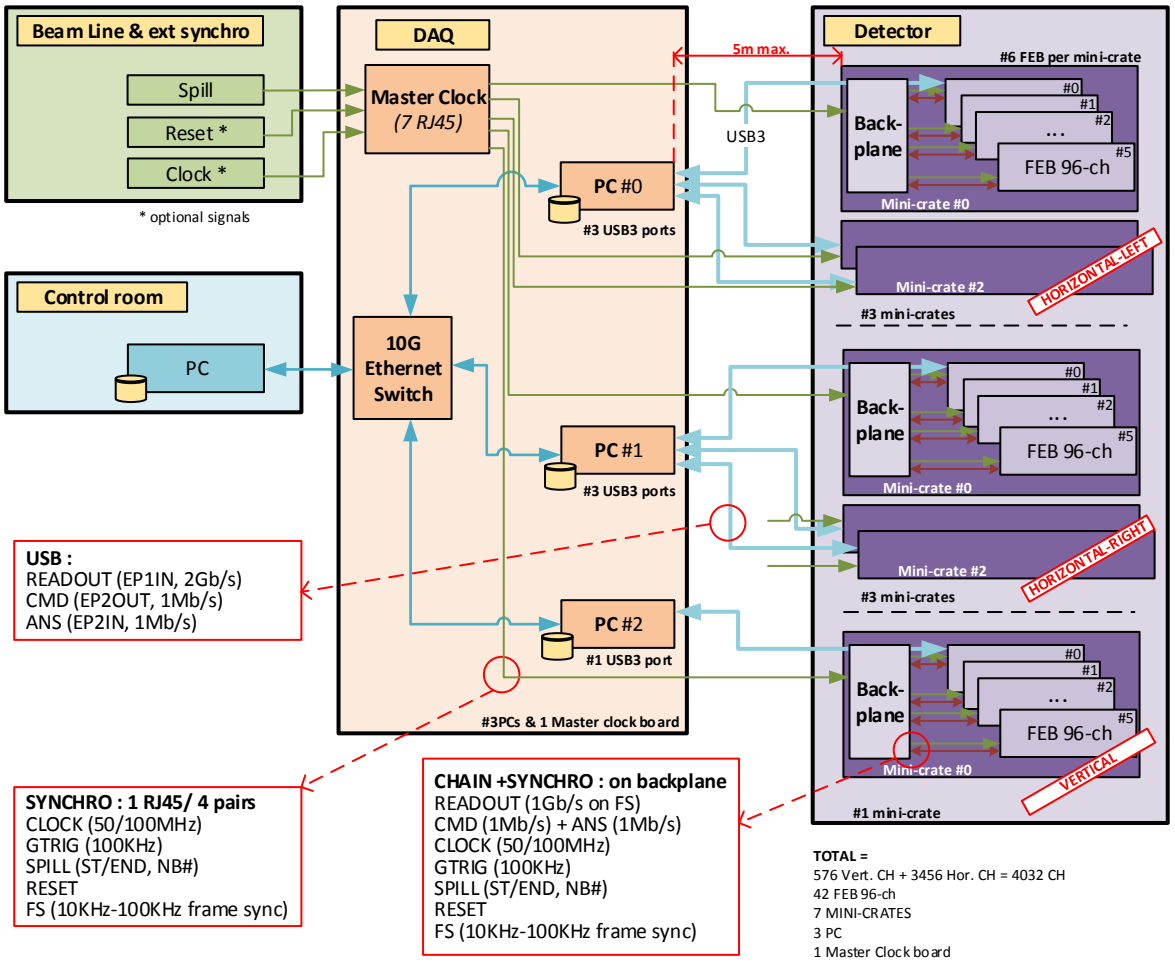

Fig. 3. Baby MIND readout block diagram.

D. Synchronization subsystem overview

The block diagram of the Baby MIND readout system is shown on fig. 3. The synchronization subsystem (shown in green lines) takes input signals from the beam-line and combines them in a digital synchronization signal (SYNC). It also produces the global detector clock (CLK) and eventually synchronizes it to an external experiment clock. Both signals are then distributed to the readout FEBs.

The distribution path has a two-level fan-out structure. The first level contains the master clock board (MCB) which distributes the signals to the FEB mini-crates over 5m long CAT6 shielded Ethernet cables. The second level consists of the mini-crate backplane which distributes the CLK and SYNC to the FEB slots. It also provides a couple of gigabit links from one slot to the next which pass the data in the TDM mode readout chain.

II. Synchronization Subsystem Implementation

At the time of writing only the backplane has been developed and tested. The master clock board is still under development. In order to test and qualify the detector a FEB emulates the signals of a single output of the MCB. A separate fan-out board was developed to distribute the signals to the mini-crates.

A. Mini-crate backplane block diagram

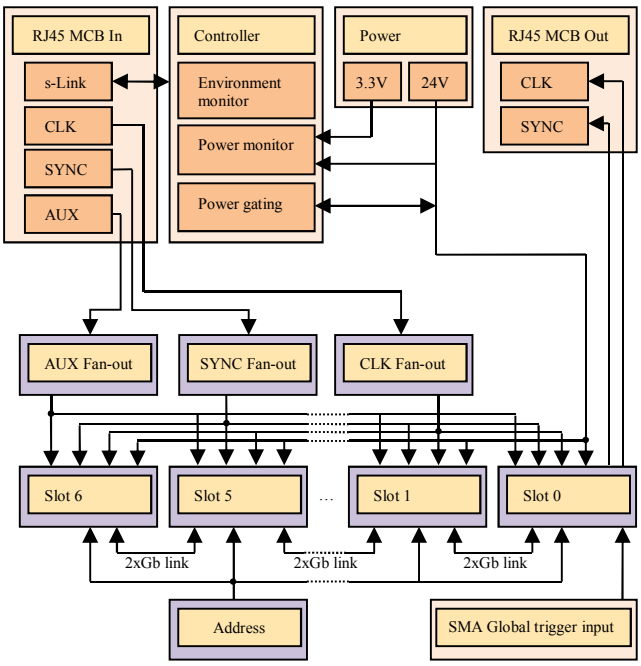

Fig. 4. Baby MIND mini-crate backplane block diagram.

The mini-crate backplane receives differential CLK and SYNC signals from the MCB (fig. 4). A second spare data

line AUX running from the MCB through the fan-out to the FEBs has been added to facilitate flexibility and future upgrades. The 3 differential signals are distributed to all 7 FEB slots. The last remaining pair of the CAT6 cable is dedicated to a serial link for the back-plane controller, used to monitor slow-control parameters on the back-plane and control individual slot power gating.

Between every two adjacent slots there is a pair of serial links running at 1 Gb/s (with a possible future upgrade to 2 or 3 Gb/s), which allow to use the mini-crate FEBs in TDM mode.

Slot 0 is connected to SMA connectors on the back-plane, which allow the FEB in that slot to read external trigger and reset signals. The slot is also connected to a separate RJ45 connector that allows the FEB to output MCB emulation CLK and SYNC signals.

B. Test setup and test fan-out PCBs.

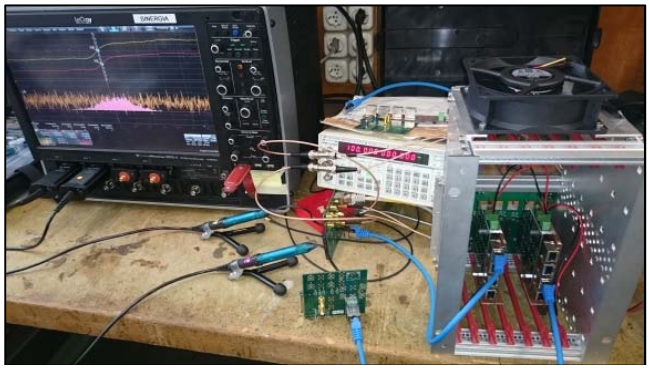

Fig. 5. Baby MIND qualification fan-out board being tested.

Due to the unavailability of the master clock board for the qualification tests at CERN a stop-gap solution was developed. It uses an additional mini-crate with a FEB running in MCB emulation mode in slot 0. The dedicated MCB emulation output is fed back into the MCB input of the backplane. Two 4-output fan-out PCBs are connected to the back-plane and deliver the synchronization signals to the read-out mini-crates installed on Baby MIND.

While this solution works well, it has a few disadvantages to the real MCB. Due to the chips used it has worse pulse rise and fall times, jitter and output clock skew. It has no means to compensate a difference in the delays of the synchronization channels in contrast to the MCB. It is also harder to interface to the beamline signals.

III. Test Results

This paper presents the timing parameters achieved by the test setup used to qualify the Baby MIND detector. The final setup to be used in Japan is expected to outperform it.

The measurements have been taken using an SRS CG635 precision clock generator (1ps random jitter, 80ps rise/fall time) and a 20 GHz LeCroy WaveMaster 820Zi oscilloscope.

A. Backplane parameters and oscillograms

Figure 6 shows the difference in delays of a 100MHz signal passing through the back-plane. Rise and fall times around 60ps were observed.

The scope was found to show a difference of 42ps between the probes on channel 1 and two when connected to the same signal source (solder-in tip). This value was used to correct the measured clock delays. The values presented are obtained after statistical processing of 1000 samples. An example of the delay distribution can be seen on the lower plot on fig. 6.

Fig. 6. Backplane clock 100MHz signal skew.

Table 1 lists the minimum and maximum values of the clock delay variation between slot 0 and the other slots. It lists the median of the distribution which is taken as the delay value and also the difference between the minimum and maximum delay values.

TABLE 1. SLOT-TO-SLOT CLOCK DELAY

Slot delay	min (ps)	max (ps)	median (ps)	max – min (ps)	delay (ps)
CLK_0-to-1	-3.4	3.8	-0.374	7.2	-0.374
CLK_0-to-2	4.5	10.4	7.45	5.9	7.45
CLK_0-to-3	10.2	16	12.96	5.8	12.96
CLK_0-to-4	6.4	12.4	9.494	6	9.494
CLK_0-to-5	2.1	7.9	4.647	5.8	4.647
CLK_0-to-6	-5.2	1.8	-1.979	7	-1.979

Fig. 7. Input CLK to SYNC delay after in-scope compensation.

To measure the delay between the CLK and SYNC signals we split the signal from the signal generator. Due to the difference in the used cable length an input delay of approximately 2 ns was observed. It was compensated in the scope and figure 7 shows the remaining measured input delay difference of 20 ps. This value was used to correct the measurements presented in table 2.

Figure 8 and table 2 show the CLK-to-SYNC delay for the slots of the back-plane. The average value of the delay is around 740ps. It is mostly due to the different driver chips (and delays) used for the fan-out of the CLK and SYNC/AUX, a choice driven by input level compatibility requirements. The SYNC/AUX signals are driven on the rising edge of the clock and sampled on the falling edge. To read the SYNC data properly the delay should not exceed Tclk/2 or 5 ns. The measured SYNC setup delay value is well within that margin.

Fig. 8. CLK to SYNC delay on the backplane.

TABLE 2. CLK-TO-SYNC DELAY FOR EVERY SLOT

Slot delay	min (ps)	max (ps)	median (ps)	max – min (ps)	delay (ps)
CLK-to-SYNC_Input	-1	41	20.66	42	20.66
CLK_0-to-SYNC_0	709.2	738.7	725.5	29.5	746.2
CLK_0-to-SYNC_1	715.2	737.2	725.3	22	745.9
CLK_0-to-SYNC_2	700	722.5	710.6	22.5	731.2
CLK_0-to-SYNC_3	709.4	733.4	720.2	24	740.9
CLK_0-to-SYNC_4	708.4	732.9	720.3	24.5	740.9
CLK_0-to-SYNC_5	699.2	724.2	711.2	25	731.9
CLK_0-to-SYNC_6	717.9	744.4	730.3	26.5	750.9

B. Test fan-out setup parameters

TABLE 3. TEST FAN-OUT OUTPUT-TO-OUTPUT CLOCK DELAY

Output delay	min (ps)	max (ps)	median (ps)	max - min (ps)	delay (ps)
CLK 0-to-0	-59.1	-17.1	-36.85	42	0
CLK 0-to-1	-98	-52	-77.13	46	-40.28
CLK 0-to-2	-70	-19	-44.71	51	-7.86
CLK 0-to-3	-89	-30	-58.63	59	-21.78
CLK 0-to-4	-83	-23	-48.66	60	-11.81
CLK 0-to-5	-105	-47	-70.58	58	-33.73
CLK 0-to-6	-70	-19	-42.91	51	-6.06
CLK 0-to-7	-87	-27	-58.3	60	-21.45

The MCB fan-out emulation setup delays were measured in a way very similar to the back-plane delay measurement (see fig. 5). As previously mentioned the setup consists of a backplane and a pair of 4-outut active fan-out boards. Table 3 lists the aggregate setup clock delays that were measured on the outputs. A maximum delay difference of 41ps has been observed among the outputs. Similar delays have been measured for the SYNC.

C. Beam-line synchronization chain delay parameters

The beamline delay parameters are a superposition of MCB fan-out, cabling and back-plane delay parameters. Special measures have been taken to ensure equal cable lengths. The total FEB-to-FEB clock delay difference can be calculated as the sum of the maximum delay differences of the fan-out and the back-plane and equals:

$$_{\Delta}Td_{clk} = (7.2ps + 40.3ps) \approx 50ps \quad (1)$$

Similarly for the SYNC delay difference:

$$_{\Delta}Td_{sync} = (29.5ps + 40.3ps) \approx 70ps \quad (2)$$

IV. CONCLUSION

The test setup used to qualify the Baby MIND detector fulfills the synchronization timing requirements.

The resulting FEB-to-FEB clock delay difference is around 50ps.

The resulting FEB-to-FEB SYNC delay difference is around 70ps.

On the negative side the test setup isn't well suited to interface to beam-line signals. Also it is unable to compensate for cable delay difference, for example in the case when a cable has to be replaced and the length of the new cable doesn't match exactly the old one. These issues will be addressed with the design and development of the master clock board.

This study doesn't take into account FEB onboard delay differences - signal traces and FPGA internal signal distribution. When the MCB development is complete the whole synchronization subsystem should be re-evaluated.

The synchronization beam-line test setup fulfilled its role to allow test and qualification of the Baby Mind detector at CERN in a correct and timely manner.

ACKNOWLEDGEMENTS

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Electronic Circuits for the High Voltage Supply and Additional Sensors for the Polyphemus ^{222}Rn in Soil-Gas Scintillation Detector

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Abstract – A microcontroller system for managing the high voltage supply of a plastic scintillation detector for continuous *in situ* monitoring of the ^{222}Rn concentration in soil gas is developed and tested. Additional sensors are provided to the system to follow up some ambient parameters (atmospheric pressure, temperature, relative humidity and 3D acceleration)

Keywords – **^{222}Rn in soil-gas measurements, environmental parameters measurements**

I. INTRODUCTION

We are developing a detector for continuous ^{222}Rn in soil-gas measurements which is based on scintillation spectrometry of ^{222}Rn absorbed in scintillating polymers. The detector (hereafter referred to as the Polyphemus detector) consists of an optical chamber optically coupled to a hermetic volume which contains a photomultiplier tube (PMT, Hamamatsu R7600U-200), high voltage power supply (HVPS) (Hamamatsu C4900-51), multi-channel analyzer (labZY nanoMCA-SP) and an outside board with chip-controlled sensors for pressure, temperature, humidity and an accelerometer. The Polyphemus detector is compact, portable and is designed for ^{222}Rn in soil-gas measurements in boreholes. The proper operation of Polyphemus requires stable and computer-controlled high voltage supply for the PMT and continuous measurement of the environmental conditions in the soil such as: pressure (P), temperature (T), relative humidity (RH) and vibrations (ACC). A schematic description of the Polyphemus detector is given in Fig. 1.

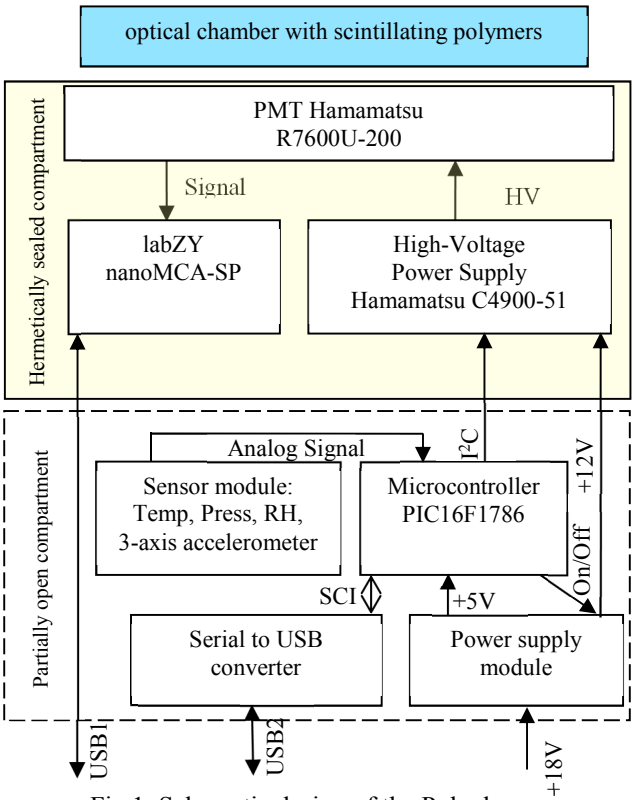

Fig.1. Schematic design of the Polyphemus scintillation detector.

The objective of this work is to present the design of the

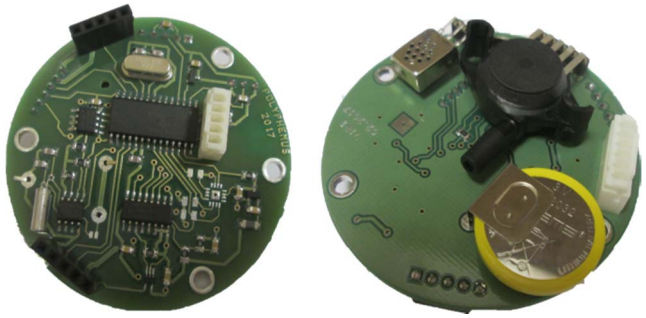

Fig. 2. P, T, RH, ACC sensors boards.

HVPS control board as well as the board responsible for the sensors for measurement of P, T, RH, ACC and their communication with a PC (fig.2). The HVPS stability over time is studied for a period of two weeks and the results are presented.

II. METHODS AND MATERIALS

High-voltage power supply control board.

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Hamamatsu C4900-51 is an on-board HVPS with compact design (46 mm x 12 mm x 29 mm) which is suitable for portable devices. Its output voltage ranges from +200V to +1250V and is proportional to a control input voltage ranging from 0V to +5V. The possibility to control the output high-voltage is utilized with MCP47FxB21Ax digital-to-analog converter which is controlled by I^2C from the MCU (PIC16F1786). The HVPS has an Enable/Disable

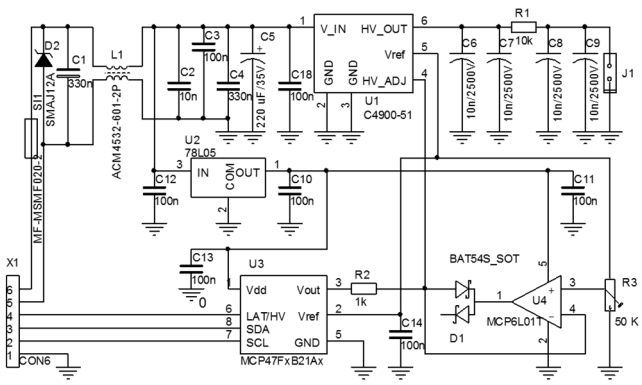

Fig. 3. Left: HVPS control board.

pin which is also controlled by the MCU and is used as a supplementary security measure to ensure that high-voltage is supplied to the PMT only when the optical chamber is closed (see Fig. 3). A possibility for gradual high-voltage incrementation up to the desired value is implemented. All commands for the HVPS come from a PC through a USB interface and are interpreted by the MCU.

P, T, RH and ACC control board.

The Radon-222 in soil-gas concentrations depend on some ambient parameters such as humidity, pressure and temperature. To monitor those parameters the Polyphemus detector is equipped with relative humidity module 808H5V5 (+/- 4% accuracy in the range of 30-80%RH), absolute atmospheric pressure module SPD015AAsil (+/- 1.8% accuracy in the range of 0 – 1024hPa) and temperature to voltage converter TC1047A (linear response from -40ºC to +120ºC). The data from the sensors is stored on an external F-RAM module FM24VN10 along with a timestamp from a real time clock unit DS1307. The stored data is periodically flushed to the PC and stored in a database. Due to the possible correlation of the radon in soil-gas concentration with earthquakes, the board is equipped with a 3D accelerometer ADXL330 with analog output. Analog outputs for all sensors are chosen. The design of the control board for the P, T, RH, ACC and power supply is given in Fig. 4.

All the data to and from the MCU passes through a serial to USB converter module FT232RL. The module communicates with the MCU via UART interface and the RX/TX lines are insulated with optocouplers as to minimize the influence of the external noise to the underground system.

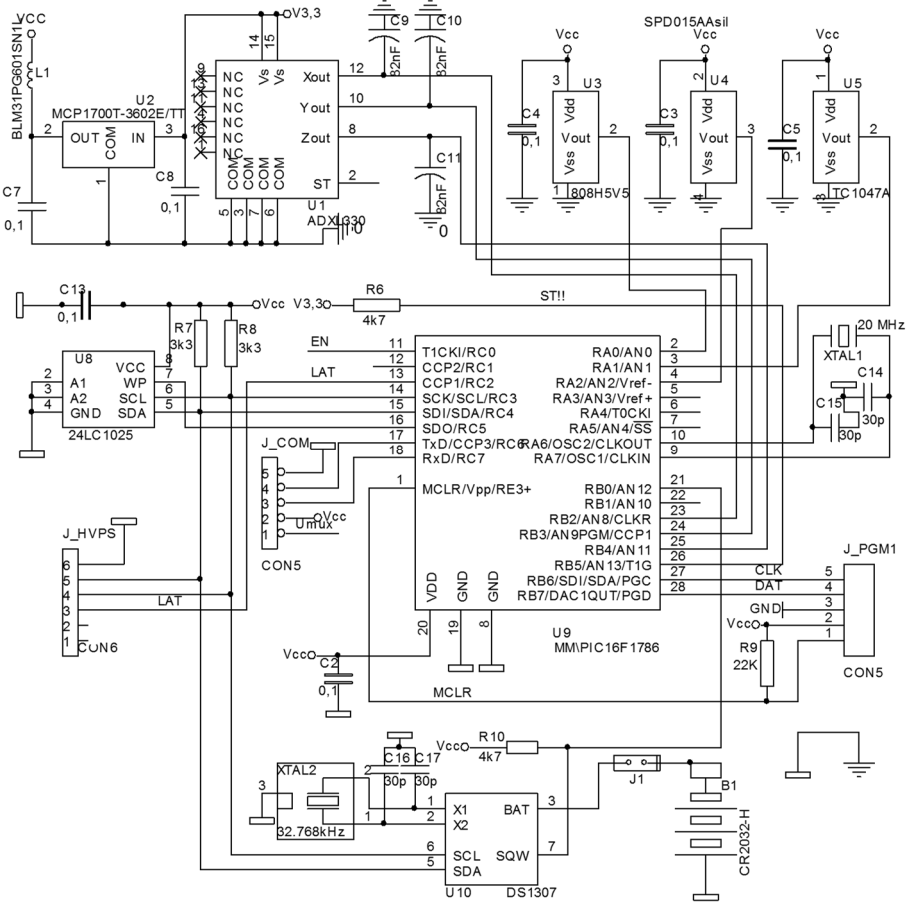

Fig. 4. Design of the P, T, RH, ACC and power supply

Sensors, MCU and HVPS are all powered by a power-supply module with a switching voltage regulator AX3007

at +12V and a linear voltage regulator MIC29302WU at +5V. Input and output filters are implemented (Fig. 5). The input voltage to the module is between +15V and +18V and passes through multiple filters and surge protection circuits.

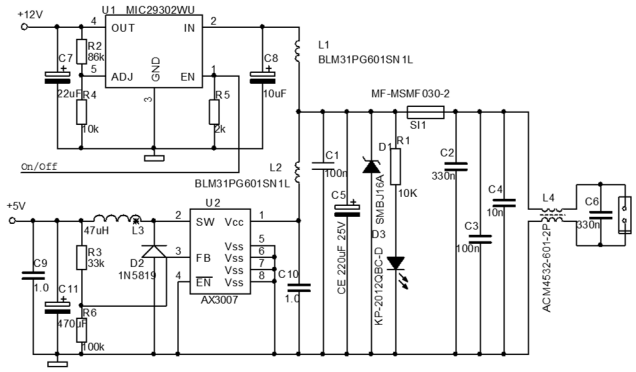

Fig. 5. Input filter and surge protection circuit. Voltage regulators for HPVS and MCU boards.

III. Results.

The HVPS control board and the sensor control board are both implemented in a Polyphemus test prototype detector. Together with the PMT and the MCA they all fit in the internal volume of the Polyphemus detector which is confined by a stainless steel tube with 60 mm internal diameter and 600 mm length. After the completion of the prototype the linearity of the high voltage power supply and the stability over time are tested in dedicated experiments.

To test the linearity of the high voltage power supply system, which includes the HVPS board controlling the Hamamatsu C4900-51 high voltage power supply, 12 values of the input voltage were set from a computer to the HVPS board and the corresponding high voltages are measured on the output of the system without load. As can be seen from Fig. 6, there is an excellent linearity of the high voltage supply system.

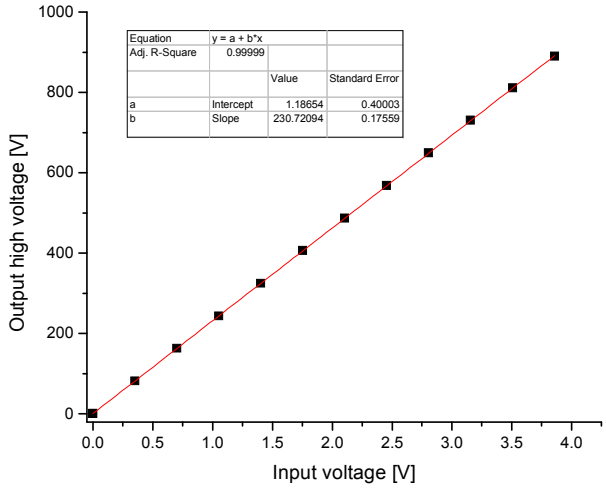

Fig. 6. Linearity test if the high voltage supply system.

The stability over time of the prototype is tested with a ^{239}Pu source mounted on 0.25 mm thick EJ-212 plastic scintillator on top of the PMT. The labZY MCA has linear 16bit ADC with 16 k channels spectrum size.

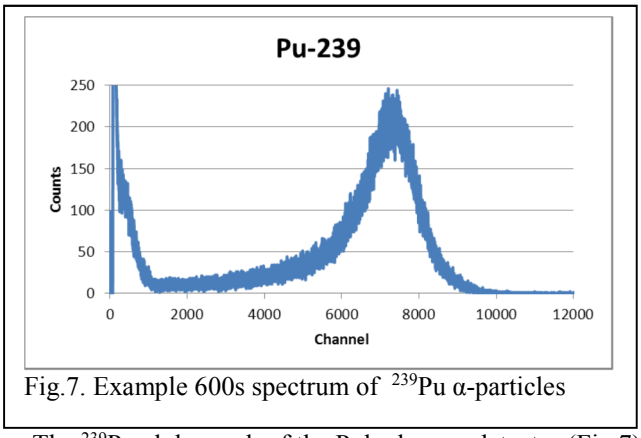

Fig.7. Example 600s spectrum of ^{239}Pu α-particles

The ^{239}Pu alpha-peak of the Polyphemus detector (Fig.7) is found to be well described by an exponentially modified Gaussian distribution [1] with three left and one right exponent [2]. The centroid of the peak is found with a least-squares fit from the model distribution and the stability over time is tested by evaluation of the position of the ^{239}Pu alpha peak in successive 600s measurements

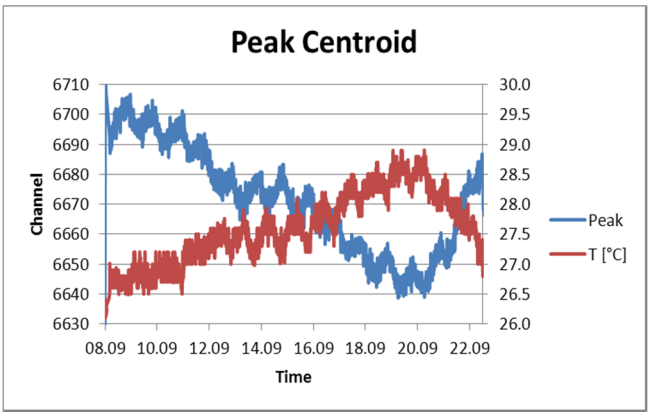

Fig. 8. Drift of the Polyphemus spectrometer with time and ambient temperature

acquired for a period of 14 days. The peak centroid is subjected to some variations mainly due to temperature change (note that the estimated standard deviation of the peak position for each individual 600s spectrum is σ=2 channels). Diurnal peak position variations are well pronounced in an anticorrelation with the temperature (see Fig 8).

Overall, the stability of the spectrometric tract of the Polyphemus detector (less than 1 per cent peak-to-peak for 14 days) is adequate for the purpose of scintillation measurements of ^{222}Rn absorbed in plastic scintillators.

IV. Conclusion.

In this work we develop and test a control board for Hamamatsu C4900-51 high-voltage power supply as well as circuit boards for measurement of ambient parameters such as relative humidity, absolute pressure, temperature and vibrations. Data from the sensors is successfully send to and stored on a computer. Various surge protection and filtering circuits for ensuring proper detector operation are implemented. A linearity test of the high voltage power supply system is performed which showed excellent system linearity. A test of the drift of the spectrometer is

performed and it is found that the response is stable enough to support radon in soil-gas measurements.

V. ACKNOWLEDGEMENT.

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LED equipment for light influence on photosynthesis investigations

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Abstract – **The purpose of this work is design an energy-efficient LED lamp suitable for investigations in greenhouse production. The spectral characteristics of the lamp are consistent with the results of the latest research in this area. Possibilities for independent stepless control of the radiation's intensity in the different spectral areas are realized. The distribution of the irradiance in the processing field under different lamp operating modes is investigated. The appropriate thermal management ensures small thermal load on the LEDs with a passive cooling system. The realized lamp gives the opportunity to study the influence of the light flux's features on the development of different plants species and the determination of the optimal characteristics at low energy costs.**

Keywords – **Horticulture lighting, LEDs for horticulture applications**

I. Introduction

One of the fastest growing areas in LED lighting during the past few years is associated with applications in greenhouse production [1 ÷ 15]. There are many reasons for this - the cost of artificial lighting forms a substantial part of the cost of production in greenhouses and the possibility to realize various modes of lighting and control automation. Use of LEDs in lighting devices offers many advantages - significant reduction in energy costs; options for selecting appropriate power and spectral composition of the radiation depending on the type of plants been grown; possibilities for managing the characteristics of the radiant flux depending on the developmental stage, etc. At the same time, the life of LED lighting equipment with appropriate thermal management is much longer than those used earlier, its performance is more reliable and it is easier to service.

It should be stressed that the choice of appropriate lighting for a particular plant is not a simple task and there is no single solution.

Finding optimal characteristics of the lighting equipment - energy efficiency, power and appropriate spectral distribution of radiant flux requires extensive research and implementation of precision control of the used equipment.

II. Problem Statement

Typical absorption spectra of the pigments that determine the efficiency of the photosynthesis process are shown in Fig.1 [5]. It should be noted, however, that these spectra are approximate. In reality the situation is much more complicated.

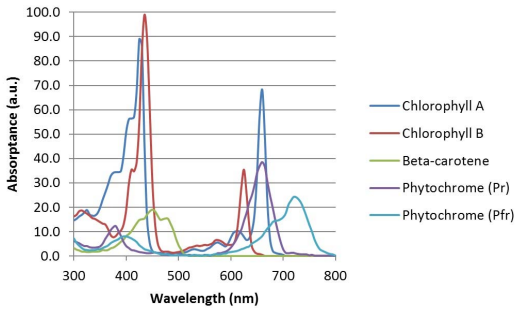

Fig. 1. Photopigment spectral absorptances.

McCree (1972a) measured the spectral absorptance - Fig. 2 for the leaves of 22 species of crop plants [5] and established photon-weighted relative quantum yield – Fig.3 that is representative of most crop plants.

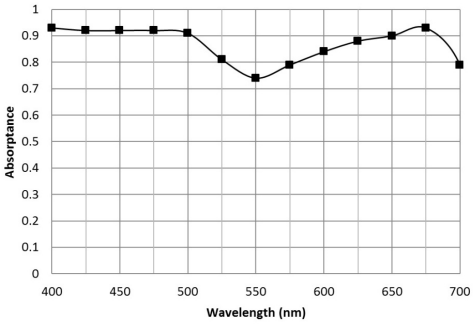

Fig. 2. Average crop plant spectral absorptance.

To evaluate the effectiveness of the luminous flux on the photosynthesis process the most commonly used quantities are so called **Photosynthetically Active Radiation** (PAR) – metrics for the total electromagnetic radiation over the spectral range of 400 nm to 700 nm that photosynthetic organisms are able to use in the process of photosynthesis. One unit for PAR measurement is **photosynthetic photon flux density** (PPFD) – the number of PAR photons that fall on a given surface for given time, measured in units of moles per square meter per second (mol/m^{2}s).

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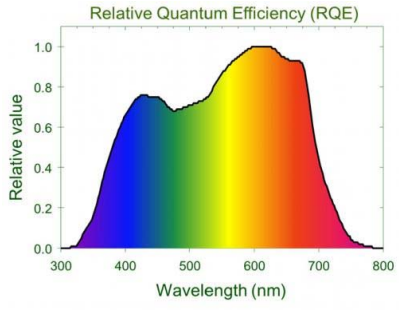

Fig. 3. Relative quantum efficiency curve of photosynthesis. (Adapted by Erik Runkle from McCree, 1972. Agric. Meteorology 9:191-216.)[5].

In accordance with the Stark-Einstein law, every photon in the interval 400 nm ÷ 700 nm that is absorbed will excite one electron, regardless of the photon's energy.

Therefore PPFD is the preferred parameter for assessing the properties of light flux for the photosynthesis process when using sources with different spectral power distributions [1, 3, 5].

Application of LEDs in greenhouse production.

For artificial lighting in plant growing so far the most widely used source were high-pressure sodium lamps. Nowadays, LED technology evolves rapidly and replaces the HPS – "the current gold standard" in greenhouse lighting [6]. Their objective is to develop lighting equipment which is as good as HPS, but also has about two times lower power consumption [6].

With growing interest in greenhouse production that relies heavily on electrical lighting, light-emitting diodes offer many advantages. This is particularly true for multilayer plant cultivation where close distances of plants in vertical shelves make HPS lighting impractical [5].

The relative quantum efficiency of photosynthesis of the crop plant has two peaks at 440 nm and about 620 nm [1 - 9], Fig. 3. It is known that photosynthesis in the presence of two or more simultaneous wavelengths radiation may be more effective than the sum of that due to the individual wavelengths. In particular, the addition of white or red light (with wavelength less than 680 nm) to deep red light (greater than 680 nm) can favorably increase the rate of photosynthesis [5].

In the process of photosynthesis the radiation in the green part of the spectrum plays an important role too - Fig. 2. Photosynthesis in leaf depth is found to be more strongly influenced by green light than by red or blue beam radiation. In addition, insects used in greenhouses such as pollinators and biological control agents see better in the green and ultraviolet areas of the spectrum.

Effective intensive 450 nm indium-gallium-nitride (InGaN) deep blue LEDs and 660 nm aluminum-indium-gallium phosphide (AlInGaP) deep red LEDs are developed and widespread. These products are quite efficacious, converting about 45% of their electrical input power into visible light. Green LEDs are rarely used because of their much lower radiant efficacies [5].

In the last years specialized lighting fixtures for greenhouse production have appeared on the basis of efficient white LED modules. The combination of white LED modules with red and deep red LEDs allows the creation of efficient lighting sources with appropriate spectral characteristics for plant growing. In Fig. 4 spectral characteristics of such a source compared to the curve of the McCree and the characteristics of a HPS lamp [6] are presented. The power consumption of the LED lamp is two times less than that of HPS lamp.

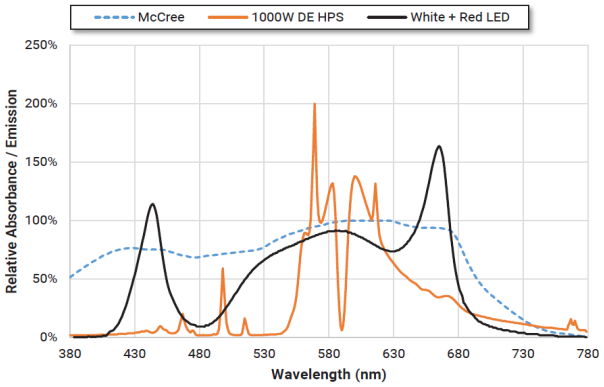

Fig. 4. McCree curve and spectral characteristics of HPS and LED lamps [6].

III. EXPERIMENTAL

There are many contradictory data about the required spectral and power characteristics for different plants (including completely opposite results); that is why we believe that lighting equipment needs the following options:

- The power of the emitted radiation in different spectral regions - blue, red and yellow-green must be controlled independently from 0 to 100%;
- It should be possible to realize a variable (interrupted) light flux with different spectral characteristics and different light pulse loading coefficients;
- The possible variations of luminous flux PPFD should be easily varied from 0 to about 450 μmol/m^{2}s (saturation limit for most plants).

LED luminaire

In order to create an experimental lighting luminaire for research purposes in plant growing a modular structure is used. Each LED module consists of 6 pcs. blue XLamp XQ-E LEDs – CREE corp., 5 pcs. red XLamp XQ-E LEDs – CREE corp., 7 pcs. deep red HPL LEDs and one CXA2520 4000K CREE LED module, mounted on a 255/105/28 mm heat sink.

The LEDs XLamp XQ-E LEDs – CREE corp. are mounted on a MCPCB 30/30 mm. These types of LEDs are recommended for greenhouse applications [6] and are characterized by a very good heat transfer from the p-n junction to the heat sink.

Three or six such LED modules are used to create a luminaire for greenhouse applications. Depending on the needs, the location of the modules can be varied and a luminaire with dimensions of 105/1600 mm, 350/550 mm, etc. can be obtained.

The individual LED groups (blue, white and red) are powered independently of constant DC sources; the

magnitude of the current through the LEDs can be controlled fluently from 0 to 800 mA. Drivers MEAN WELL LCM-60 are used. One such driver is sufficient to control the current through LEDs of the same color in three LED modules connected in series.

The light-flux characteristics of the experimental LED modules are obtained using a Stellar Net spectrometer and a 1 m diameter integrating sphere.

A photo of one LED module in the integrating sphere is shown in Fig. 5.

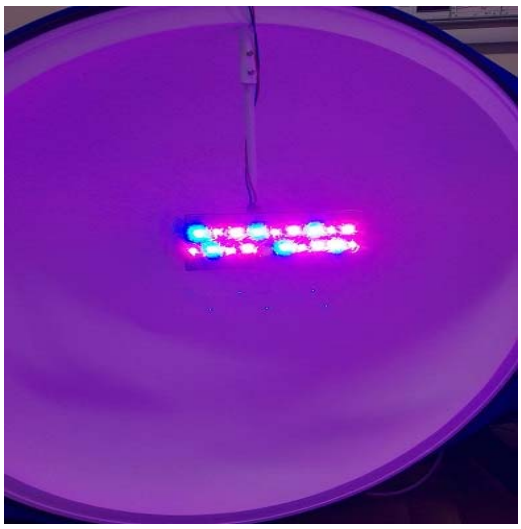

Fig. 5. Experimental LED module in the integrating sphere.

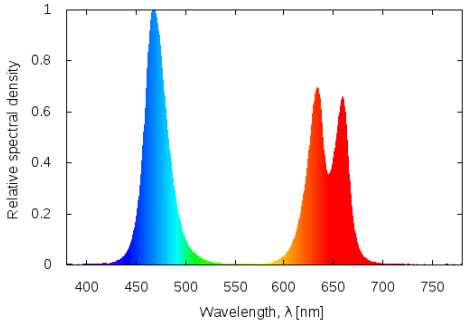

Fig. 6. Experimentally obtained spectra of blue LEDs (I_F=400 mA), red and deep red LEDs (I_F=350 mA).

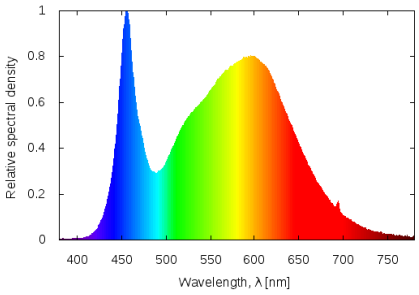

Fig. 7. Experimentally obtained spectrum of CXA 2520 module (I_F=500 mA).

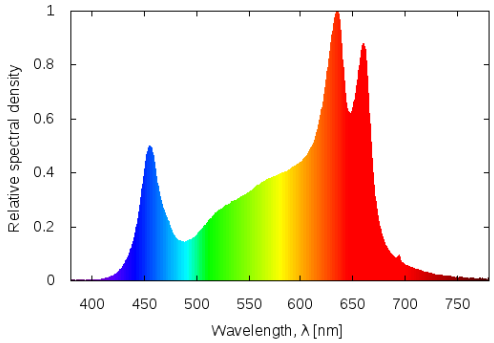

Fig. 8. Experimentally obtained spectra of: CXA 2520 module (I_F=500 mA) and red LEDs (I_F=350 mA).

Four boxes with different lighting were designed to study the influence of radiation with a different spectral composition on the development of different plant species – Fig. 9.

Fig. 9. Plants illuminated by light with different spectral power distribution.

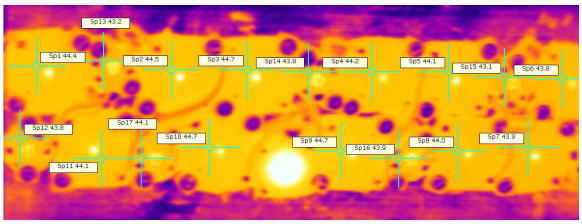

Fig. 10. Temperature distribution measurements by IR camera.

Performance characteristics

The electrical power P_{LED} consumed by one LED chip at nominal regime of operation is calculated:

$$P_{LED} = I_F * U_F; \quad (1)$$

$P_{WHITE\ (CXA)} = I_F * U_F = 0.5*34.5 = 17.25$ W;
$P_{BLUE} = I_F * U_F = 0.35*3.1 = 1.09$ W for blue LED;
$P_{DEEPRED} = I_F * U_F = 0.35*2.1 = 0.74$W for deep red LED;
$P_{RED} = I_F * U_F = 0.35*2.2 = 0.77$ W for red LED.

Because the LEDs are mounted on large MCPCBs, the area of the radiator is completely covered. When all LEDs are switched on the maximum power is:

$$P_{tot} = P_{WHITE} + 6*P_{BLU} + 5*P_{RED} + 7*P_{DRED} = 32.8 \text{ W}$$

at nominal regime of operation.

Photosynthetic photon flux density (PPFD) in units of moles per square meter per second is measured and photosynthetic photon flux per watt – PPF/W (µmol/s)/W; (µmol/J) for different type of LEDs are evaluated.
For blue LEDs - PPF/W ≈ 1.3 (µmol/s)/W; For red LEDs - PPF/W ≈ 1.4 (µmol/s)/W; For white CXA - PPF/W ≈ 1.2 (µmol/s)/W.

Thermal Management

LEDs thermal loads investigations at different currents and different ambient temperatures are performed in a thermal chamber. The temperatures are measured by both thermocouples and infrared camera Therma Cam E300 - FLIR Systems.

The temperatures of the solder points (cases) of the various LEDs are measured (Fig. 10), and based on the thermal resistors scheme (Fig. 11) and equation (2) the temperatures of the p-n junctions are calculated.

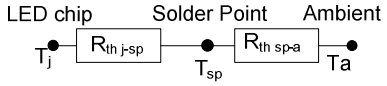

Fig. 11. Scheme of the thermal resistances between p-n junction and the ambient environment: T_j – temperature of p-n junction; T_{sp} - temperature of solder point (case); T_a - ambient temperature; $R_{th\ j\text{-}sp}$ and $R_{th\ sp\text{-}a}$ - thermal resistance between p-n junction and solder point (case) and between solder point and ambient.

$$T_j = T_{sp} + R_{th\ j\text{-}sp} * P_{LED} \qquad (2)$$

Thermal resistances between p-n junction and solder point (cases) $R_{th\ j\text{-}sp}$ are obtained using data sheets:
for XLamp XQE – blue, $R_{th\ j\text{-}sp}$ = 6 K/W; for red XQE LEDs $R_{th\ j\text{-}sp}$ = 5 K/W; for deep red LEDs $R_{th\ j\text{-}sp}$ = 5 K/W.

In Fig. 12, results relating to the heat load of the different types of LEDs at nominal regime of operation are shown.

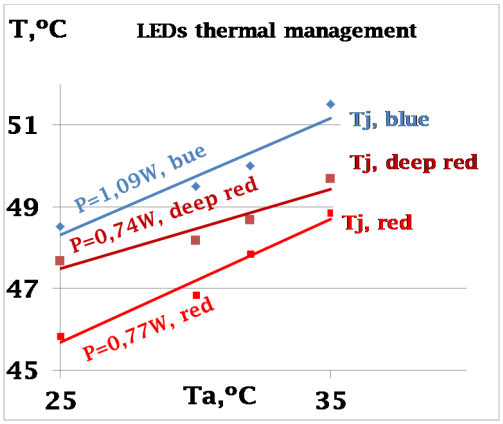

Fig. 12. Blue, red and deep red LEDs' p-n junction temperature (**Tj**) in dependance of the ambient temperature (**Ta**).

It can be seen from the presented results that the heat load of the LEDs is low. As it was mentioned above, the used LEDs boards are of large size and cover the whole area of the heat sink as the number of used LEDs is relatively small. It results in a little heat load, which is essential for the operation of the red and deep red LEDs. It is known that when increasing the temperature of the p-n junction of LEDs of this type their light efficiency decreases considerably [6], therefore it is important that they operate at relatively low thermal loads.

IV. Conclusion

LED module for application in plant breeding is developed and tested. The nominal power of the module is about 35 watts, and maximum is about 50 watts. Combining 3, 6 or more such LED modules allows the creation of luminaires with different capacities and sizes depending on the illuminated areas, the type of plants, etc. The independent, stepless control of the light streams of different spectral composition - red, blue and white allows the created module to be used in investigation of the influence of spectral composition and the power of light flux on the development of different plant species and the search for optimum characteristics. Passive cooling of the LEDs is used. Operation with low thermal load is assured. This ensures a long life and reliable operation of the developed equipment.

Acknowledgment

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Method and equipment for controlling LED lamp for therapeutic purposes

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Abstract – **In the present study a method for managing therapeutic purposes LED lamp is shown. The main goal is to facilitate the potential user (e.g. medical practitioner) in configuring appropriate parameters such as correlated color temperature (CCT) and luminous flux in a relevant room (as facility for senior citizens). The controlled LED lamp consists of 2 independent channels - the first includes 2 white LED CXA2520 modules and the second 16 blue XPE from Xlamp series all form CREE Copr. The constant current drivers for both channels are Meanwell LCM-60. To provide remote management of the whole unit ATmega328P (Arduino) microcontroller are used. The luminous flux of the lamp can be tuned up to 5000 lm and CCT can be set in the range from 3500 K to over 20000 K.**

Keywords – **LED driver, CCT, therapeutic lamp,**

I. Introduction

With the advent of LED, lighting lamps with a special purpose become more and more popular. This is due to the wide variety of light characteristics throughout the visible spectrum, making it easy and convenient to mix different light modules in a common luminaire. An exemplary use are the lamps for medical purposes, such as in facilities for elderly people. It is well known that as the human eye ages several irreversible changes took place - size narrows and lenses become denser and yellow [1]. Several studies note that the elderly people mood could be positively affected by the proper tune of light sources characteristics such as luminous flux and correlated color temperature (CCT) [2, 3]. Light with proper CCT can also help syncing the internal circadian clock to the natural 24 hour light cycle [4] of old people as their synchronization worsens with increasing age [5].

In prior studies [6] of our research group a lamp has been developed to assist elderly people through appropriate light characteristics - luminous flux that can be tuned to up to 5000 lm and CCT that can be set in wide range interval from 3500 K to more than 20000 K. The current work is focused on providing an easy method to control the luminaire characteristics.

II. Problem Statement

The investigated luminaire (Fig. 1) contains two independent channels. The first contains two CXA2520 [7] CREE Co. LED modules mounted in series. Their nominal current is 550 mA with forward voltage at about 36 V. The second channel consists of 16 blue LEDs - Xlamp XPEBlue [8] Cree Co. connected in series. Their nominal current is 350 mA with forward voltage at about 3.3 V. From now on the index “w” for all variables related to the white CXA group and “b” for the blue LEDs will be used.

The spectral characteristics of the LEDs are shown in Fig. 2 and Fig. 3.

Fig. 1. Photo of the luminary.

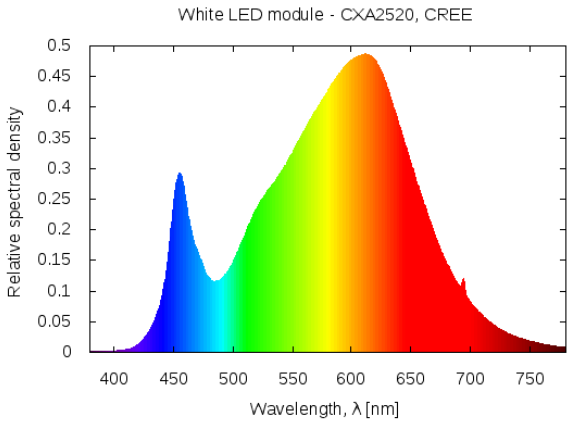

Fig. 2. Spectral power distribution of the white LED module CXA2520. Forward current I_{Fw}= 550 mA.

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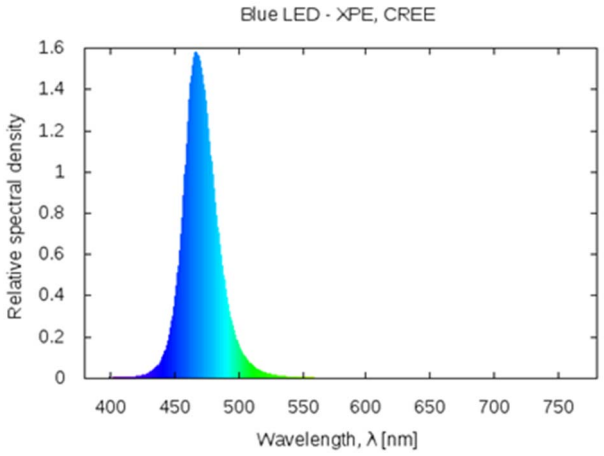

Fig. 3. Spectral power distribution of the blue LEDs XPE series. Forward current I_{Fb} = 500 mA.

The color characteristics of each modular group are shown in CIE1931 diagram, Fig. 4. Zone A shows the location of the chromaticity coordinates of the lamp when only the blue LEDs are on, and Zone B - when only the white LEDs are on. Theoretically, the light obtained by mixing the two modular groups will have chromaticity coordinates located in the area surrounded by red lines.

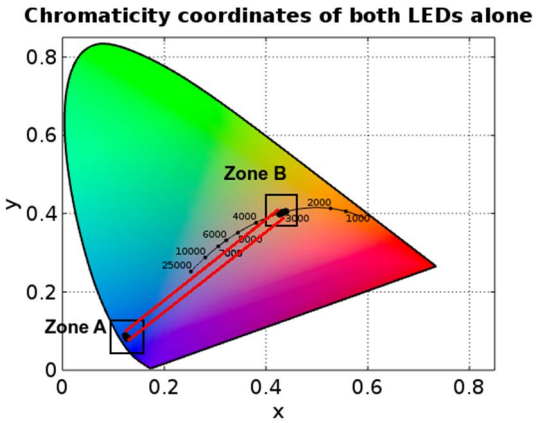

Fig. 4. Chromaticity coordinates of light obtained from the two LED groups separately. In zone A - only the blue LEDs are on, in zone B only the white are on. All possible colors mixes are located in the area between red lines.

When using the lamp the therapist must have an easy and convenient way to set the desired characteristics - light flux (Φ) and correlated color temperature (CCT). This requires the determination of a functional dependence in one or another form that converts the specified Φ and CCT into currents I_{Fw} and I_{Fb} for each of the LED groups. This dependence must then be programmed into a suitable microcontroller. Because of the non-linear nature of dependencies, the solution is not trivial and requires a more in-depth analysis.

III. Investigations

The LED management is accomplished by regulating the current through it. For easy control of the constant current driver it is necessary to have an appropriate interface for communication with external controllers. LCM-60 MEAN WELL Enterprises Co. drivers are proper solution and have been used in the present work. They support extra communication line with extended 0/1-10 V protocol implemented in such a way that allows one to send PWM signal by making simple shorts on a communication line in order to control the current. In this way the driver output current becomes simple linear function of the PWM duty cycle.

To study all possible lamp operating modes each module group is powered alone at different currents - those through the white CXA are I_{Fw}= 50, 100,...,950 mA and for the blue I_{Fb}= 50, 100,...,750 mA. The corresponding experimentally obtained spectral characteristics were measured with Stellar Net spectrometer and 1m-diameter integrating sphere. The problem of the needed current I_{Fw} and I_{Fb} for given Φ and CCT can be solved in different ways.

A. Theoretical solution

Theoretical solution to the problem was done using the following scheme:

- The tristimulus values X, Y, Z (normalized such as Y equals the luminous flux) for both channels for a given current through the respective LEDs are computed; then the chromaticity coordinates x, y (see Fig. 4) are calculated, then correlated color temperature is obtained; all calculations are made using freely available Matlab/Octave module – pspectro [9] that follows the CIE definitions.
- A quadratic fit for the tristimulus values is made as a function of the current through the corresponding LED groups, so that:

$$V(I_F) = a_V I_F^2 + b_V I_F + c_V, \qquad (1)$$

where V denotes any of X_w, Y_w, Z_w , X_b, Y_b, Z_b. From a given parameter CCT and Φ one can compute the closest (in *Yuv* CIE 1960 terms) chromaticity coordinates *x,y* corresponding to line AB from fig. 4, then the tristimulus values X_{mixed}, Y_{mixed} and Z_{mixed} are calculated.

- The nonlinear system (Eq. 2.):

$$\begin{aligned} X_{mixed} &= X_w\,(I_{Fw}) + X_b\,(I_{Fb}) \\ Y_{mixed} &= Y_w\,(I_{Fw}) + Y_b\,(I_{Fb}) \end{aligned} \qquad (2)$$

is solved for the unknowns I_{Fw} and I_{Fb} considering Eq. 1 and assuming X_{mixed} and Y_{mixed} to be known. Note that here the equation for Z is not needed because we obtained the system from the normalized 2D version of CIE 1931 *xyY*. More in-depth explanation of the color mixing arithmetic can be found in [6].

All the 6 quadratic fits from Eq. 1 have coefficient of determination (R-Squared) above 0.9998. Both the theoretical symbolic solution as well as it simplified one (with all possible numerical substitutions for given X_{mixed} and Y_{mixed}) computed with the Matlab solver lead to extremely complex computation formula for I_{Fw} and I_{Fb} with more than 100 operations in it. In order to use cheap microcontrollers and simple program a more straightforward approach need to be developed.

B. Lookup table solution

Instead of solving analytically the inverse problem - CCT and Φ as function of I_{Fw} and I_{Fb} - a pure numerical solution could be applied. For each of the six tristimulus values $X_w(I_{Fw})$, $Y_w(I_{Fw})$, $Z_w(I_{Fw})$, $X_b(I_{Fb})$, $Y_b(I_{Fb})$ and $Z_b(I_{Fb})$ the corresponding quadratic fit (Eq 1) is used in order to calculate the light characteristics (x, y, CCT and Φ). The chosen discretization step for the current is 10mA so that the white LEDs is "theoretically driven" at I_{Fw}= 10,20,30,…,950 mA (95 as a number) and the blue LEDs at I_{Fb}= 10,20,30,…,750 mA.(75 as a number). Then the theoretical light mix for each discrete combination of I_{Fw} and I_{Fb}, (95*75=7125 as total number) is computed using Eq. 2 but this time X and Y are explicitly known (calculated from Eq. 1). Then using [9] the corresponding mixed CCT (Fig. 5), Φ (Fig. 6) and *x, y* (Fig. 7) are obtained.

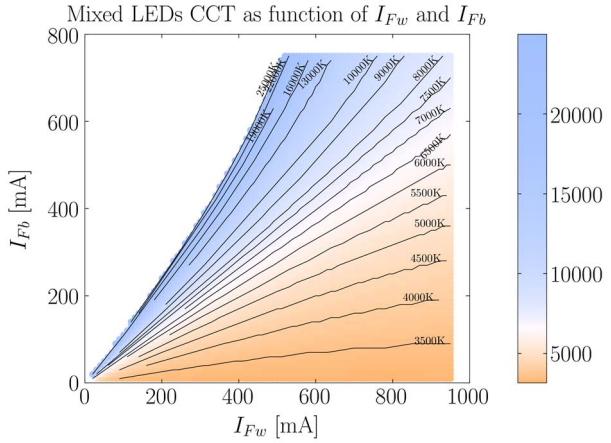

Fig. 5. CCT as a function of the current through the white CXA2520 LEDs (I_{Fw}) and through the blue LEDs (I_{Fb}). Only the combinations giving CCT < 25000 K are shown. The color in the graph corresponds roughly to the light tint of the mixed light and the label on the isolines shows the approximate values.

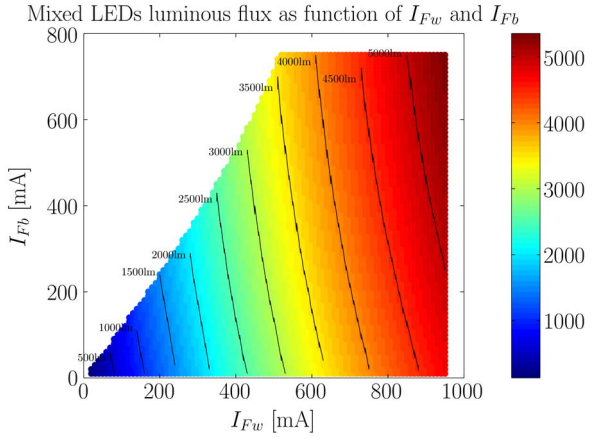

Fig. 6. Luminous flux as function of the current through the white CXA2520 LEDs (I_{Fw}) and through the blue LEDs (I_{Fb}). The color and isolines show the approximate values in lumen.

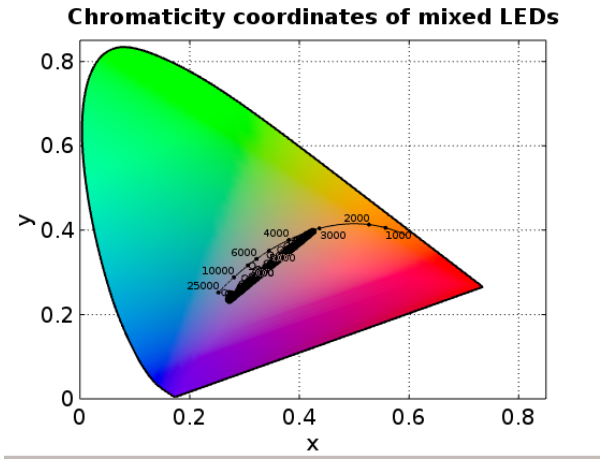

Fig. 7. Chromaticity coordinates *x,y* of the mixed LED light.

Graphical representation of the functional dependency of the CCT can be seen in Fig. 8.

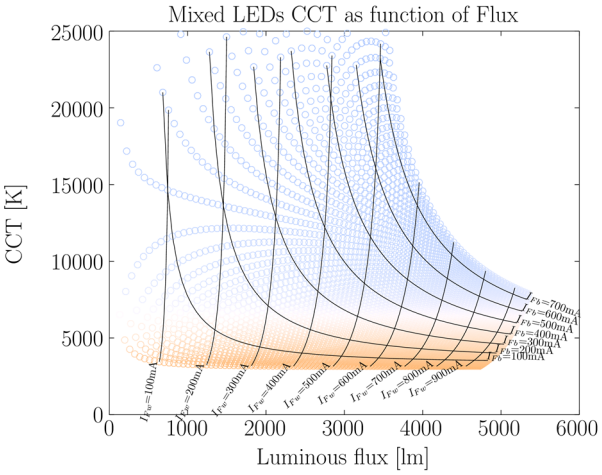

Fig. 8. CCT as function of light flux, 100 mA isolines illustrate the nonlinearity of the current dependency for both the white and the blue channel.

To prepare the resulting lookup table (4 columns with values for I_{Fw} I_{Fb} CCT Φ) for use in microcontroller we follow the scheme:

- first sort the rows by CCT and Φ;
- then calculate extra binning array B_Φ – we split the interval (200 lm, 5400 lm) in 50 equal intervals/bins and find and add to the B_Φ array the first row index which has Φ with value great than the left side of the bin;
- similar binning but in two groups $B1_{CCT}$ and $B2_{CCT}$ is done for the CCT - the interval (3500 K, 8000 K) is split in 50 bins and (8000 K, 25000 K) in 20 bins; in this way a better resolution is achieved in the lower part of the CCT, where there are many theoretical mixed values;
- all matrices values are rounded to closest integer.

The use of extra binning array is not mandatory but if there is enough memory available in the controller it can drastically reduce the computation needed to find the closest I_{Fw} and I_{Fb} values for given CCT and Φ. Binary search also increases the speed.

IV. Experimental results

Using the described algorithm a lookup table and extra binning arrays are calculated and programmed in Arduino UNO clone based on the ATmega328P chip. Two PWM-available pins are used to control separately the two LCM-60 drivers powering the blue and the white LED lamp channel. When an operator enters through PC (UART) the desired CCT and luminous flux the microcontroller calculates the needed currents (I_{Fw} and I_{Fb}) using the lookup table. The duty cycles of the PWM signals is calculated from the ratio of the I_{Fw} and I_{Fb} and the maximum possible current value for the corresponding LCM-60 driver channel. Popular optocouplers (4N36) to separate the circuits are used.

The controller program source code could be found at [10]. Schematic electrical block diagram is shown in Fig. 9 and photo of the final lamp with the driver is presented at Fig. 10.

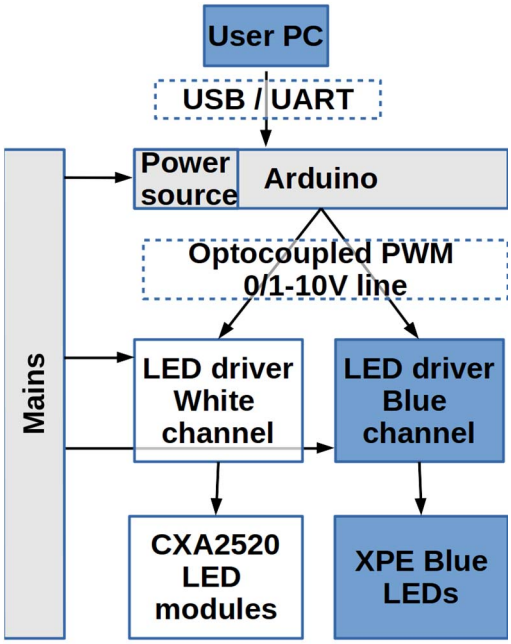

Fig. 9. Schematic electrical block diagram of the controller and the LED modules wiring.

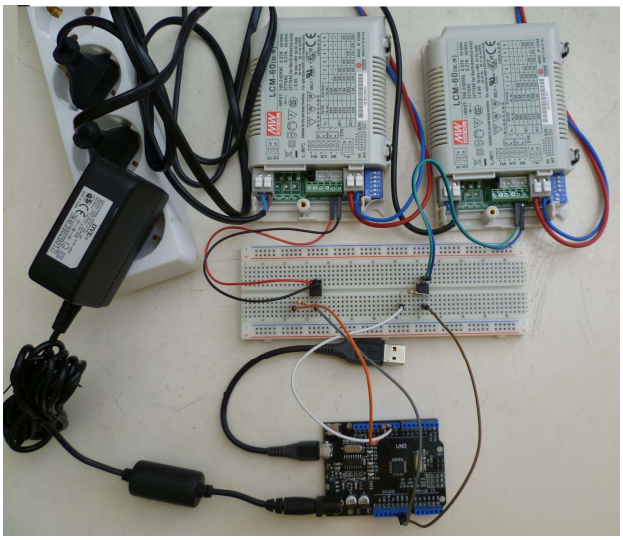

Fig. 10. Photo of the lamp controller.

The thermal stability of the lamp that ensures constant spectral characteristics is fully described in [6].

V. Conclusions

A method and equipment for controlling a LED lamp for therapeutic applications is developed. It allows easy adjustment of the luminaire's parameters - CCT and total luminous flux. A lamp controller using cheap and popular electronic components (ATmega328P, optocouplers) is built. In this way the user can easily and remotely adjust the desirable characteristics of the light in dependence of the therapeutic purposes. Thus, the configured device can be used to further regulate the hormonal balance in the patients' body and hence improve their health, especially in elderly people facilities.

ACKNOWLEDGEMENT

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Iterative Estimation and Simulation Analysis of the Amplifying Sections in Optical Communication Network

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Abstract – **Optical WDM networks use high-speed optical trunk lines as backbone network. The maximum number of amplifying sections in the optical line is causally related to power budget, dispersive expansion of code pulses and nonlinear distortions. All parameters are closely correlated. Total signal losses are estimated and through series of iterations a solution is found which for a given number of amplifying sections for the current iteration will yield minimum relative percentage error. A simulation model is developed to validate the proposed approach.**

Keywords – **wavelength division multiplexing, amplifying section, optical amplifier, nonlinear distortions, optical power level, OSNR.**

I. INTRODUCTION

The power potential of the optical line is used to determine the optimal number of amplifying sections in certain optical trunk line. It is equal to the difference between the maximum possible signal level and the signal losses in the transmission line and termination devices.

Wavelength division multiplexing systems are widely used when building optical trunk lines [1,4]. Structural diagram of an optical system for transmission with wavelength multiplexing is shown in Fig. 1.

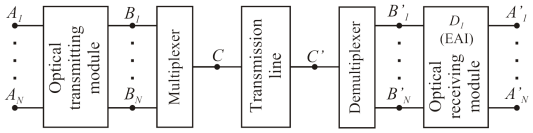

Fig. 1. Structural diagram of an optical communication system with wavelength-division multiplexing

A transmission line can be rendered as consecutively connected amplifying sections [1-4] each of which can be

On Fig. 2 p_S is the signal level in the transmission line, A_{NL} – total power of nonlinear transient distortions and A_{ISD} – the losses due to intersymbol distortions.

In Figs. 3 and 4 are shown substitution models of optical transmission and receiver modules [2,3].

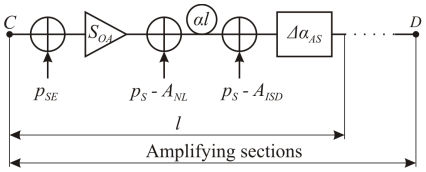

Fig. 2. Structural diagram of amplifying sections

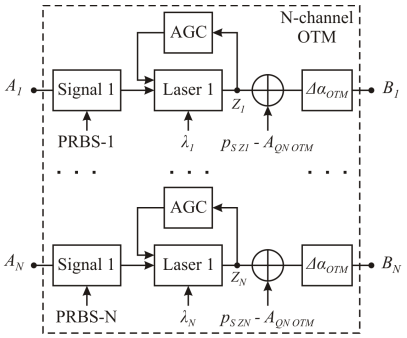

Fig. 3. Structural diagram of optical transmitter module

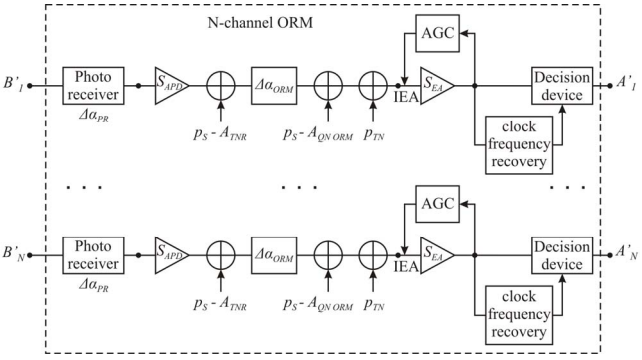

Fig. 4. Structural diagram of optical receiver module

The basic parameters characterizing the optical transmitter module (OTM) are as follows:

- absolute signal level $p_{S\,ZI}$ at the laser output in point Z_I;
- additional amplitude losses due to inaccuracy of automatic gain control (AGC), degradation of laser in

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time and its thermal instability, the type of linear code and energy losses during its input in the fiber: $\Delta\alpha_{OTM}$;
- signal protectability from laser quantum noise: $A_{QN\,OTM}$.

The basic parameters characterizing optical receiver module (ORM) are:
- attenuation of photo-receiver: α_{PR};
- amplification of photo-diode S_{APD};
- signal protection from photo-receiver quantum noise: $A_{QN\,ORM}$;
- noise figure of electrical amplifier (EA): NF;
- additional signal amplitude losses due to inaccuracy of AGC, instability of the decision device threshold level due to phase distortions of the clock frequency divider, and due to the energy losses at the optical receiver module input plus other factors: $\Delta\alpha_{ORM}$;
- signal protectability from intersymbol distortions generated by the limited frequency band of the signal of the electronic amplifier: $A_{ISD}(0)$.

II. ITERATIVE ESTIMATION OF THE NUMBER OF AMPLIFYING SECTIONS

A. An iterative approach for determining the number of amplifying sections

Optimum number of amplifying sections in the optical trunk lines of HFC network can be determined by means of iterative approach [2,3]. By applying iterative cycle it is possible to search for such a solution which, given the number of amplifying sections m_j for the current iteration, will yield relative error that satisfies the inequality

$$\delta_{Cj} = \left|\Delta A_E(m_j) / A_{N_E}(m_j)\right| \le 0{,}1 \qquad (1)$$

where $\Delta A_E(m_j)$ is the difference between the maximum possible and the total real signal losses given for the input of the electrical amplifier (EAI) (see Eq. (2) in [3]); $A_{N_E}(m_j)$ – is the minimum permissible signal level (see Eq. 18 in [3]). Consequently, this is a strict criterion, which demands that the minimum permissible signal level at the EAI should be 10 times higher than the level of the relative signal percentage losses. A complete analysis of Eq. (1) has already been made in [2,3].

Calculations for signal losses are to be performed for the electronic amplifier input (Fig. 1), therefore the index "E" is introduced. The solution of the problem is reduced to determining the number of amplifying sections m according to permissible signal losses due to transient and intersymbol distortions [2]. This solution is used as boundary condition at the second more complex iterative solution for determining the number of amplifying sections according to total losses [3].

By substituting the terms in Eq. (1), there should be checked whether j-th step of iteration from the calculations for m_j gratifies the inequality. Provided $\Delta A_E(m_j) \le 0$ then in the next $(j+1)$-th iteration m should be decreased (i.e. $m_{j+1} < m_j$) and all calculations repeated in order to determine δ_{Cj+1}. If $\Delta A_E(m_j) > 0$, but Eq. (1) is not gratified then in the next $(j+1)$-th iteration m should be increased (т.е. $m_{j+1} > m_j$).

Sequential iterations are applied unless the condition of Eq. (1) is fulfilled. Consequently the final result for the number of amplifiers (amplifying sections) will gratify limitations imposed by the total signal losses in assuring respective quality factors of the transmitted signals.

B. An example of analytical determination of the number of amplifying sections

Table 1 shows input parameters of an exemplary optical communication line with spectral multiplexing (WDM).

TABLE 1. OPERATING PARAMETERS OF OPTICAL WDM COMMUNICATION LINE

Parameter	Value
1) Optical system:	
– Wavelength, λ	1550 nm
– Number of channels, N_{CH}	8
– Acceptable BER	1.10^{-13}
2) Optical transmitter module:	
– Optical power, $p_{S\,Zi}$	3 dBm
– $\Delta\alpha_{OTM}$	3,2 dB
– $A_{QN\,OTM}$	50 dB
3) Optical receiver module:	
– α_{PR}	24 dB
– S_{APD}	15 dB
– $A_{QN\,ORM}$	56,6 dB
– NF_{EA}	3 dB
– $\Delta\alpha_{ORM}$	9 dB
– $A_{ISD}(0)$	23 dB
4) Amplifying sections – optical fiber:	
– Fiber attenuation, α	0,242 dB/km
5) Amplifying sections – EDFA amplifier:	
– NF_{EDFA}	4 dB
– Output power, $p_{S\,OA}$	25,4 dBm
– Input power, p_S	-3.65 dBm
– Gain, S_{OA}	20 dB
– A_{NL}	26,7 dB
6_ WDM multiplexer and demultiplexer:	
– Insertion loss, α_{mux} / α_{demux}	0,45 dB

With the input parameters thus set, the maximum length of the optical fiber in one amplifying section will be:

$$l_{AS} = \frac{\Delta\alpha + S_{OA}}{\alpha} = \frac{0{,}3 + 20}{0{,}242} = 83{,}9km \qquad (2)$$

The results of applying the iterative approach to determining the number of amplifying sections in an optical WDM network are presented in Table 2

TABLE 2. RESULTS FROM ITERATIVE DETERMINATION OF THE NUMBER OF AMPLIFYING SECTIONS

Iteration number, j	1	2	3
Number of amplifying sections, m	9	18	13
$\Delta A_{NE}(m_j)$	21,89 dB	22 dB	21,95 dB
$\Delta A_E(m_j)$	-8,48 dB	10,06 dB	1,65 dB
Relative error, δ_{Cj}	0,387	0,457	0,075

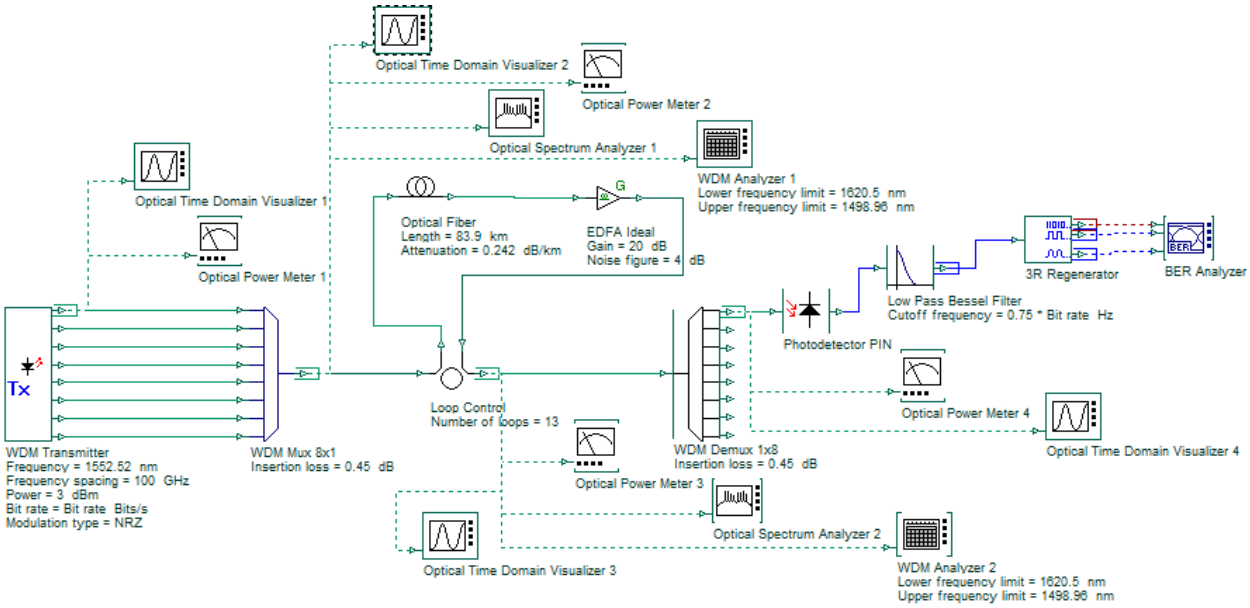


Fig. 5. Simulation model of optical 8-channel WDM network

It can be seen from Table 2 that the third iteration produces a relative error δ_{C3} = 0,075 < 0,1, i.e., the inequality is respected. This means that at a maximum length of 83,9 km the maximum number of amplification sections will be 13, which determines a maximum total length of the optical WDM network equal to 1090,7 km.

III. Simulation analysis

The next step is to develop a simulation model to validate the proposed iterative approach.

In Fig. 5 is shown simulation model of optical communication line with spectral multiplexing, created with OptiSystem software.

The simulation model consists of 8-channel optical transmitters, merged into a common WDM Transmitter, the first of which transmits at a wavelength of 1552,52 nm and the optical power level is variable in simulation. The following is an 8-channel WDM Multiplexer (WDM Mux) with insertion loss α_{mux} = 0,45 dB. The amplifying sections are represented by the optical fiber and block EDFA Amplifier. Their number is set in the Loop Control block.

The 8-channel WDM Demultiplexer (WDM Demux) is with an insertion loss of α_{demux} = 0,45 dB. Only one optical receiver is introduced, consisting of a PIN-photodetector and a Low-Pass filter. All block parameters are in line with those presented in Table 1.

The parameters and characteristics of the signals are measured and visualized by a set of visualizers located at different control points (Fig. 5): optical power meters, optical time domain visualizers, optical spectrum analyzers, WDM analyzers and end-to-end BER analyzer.

The following figures are presented below:

- Fig. 6 – the Q-factor of the optical system versus optical transmitted power (P_{TX});
- Fig. 7 – end-to-end BER versus optical transmitted power (P_{TX});
- Fig. 8 – optical received power (P_{RX}) versus optical transmitted power (P_{TX});
- Fig. 9 – optical Signal-to-Noise ratio (OSNR) versus optical transmitted power (P_{TX}).

The presented results are comparative and, respectively, for the three iterations – for 9, 18 and 13 amplifying sections (i.e. NAS – number of amplifying sections).

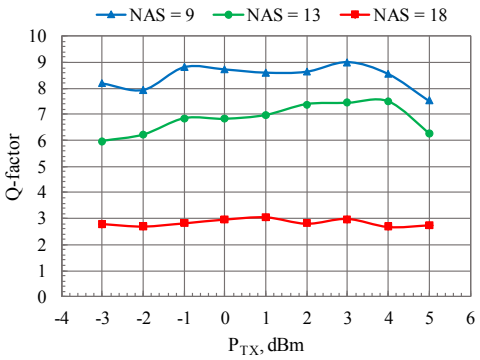


Fig. 6. $Q = f(P_{TX})$

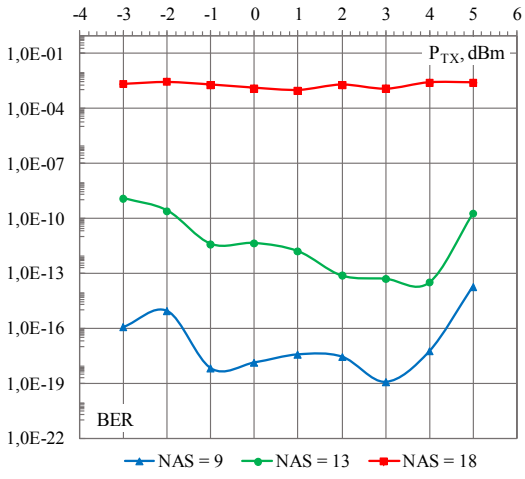


Fig. 7. $BER = f(P_{TX})$

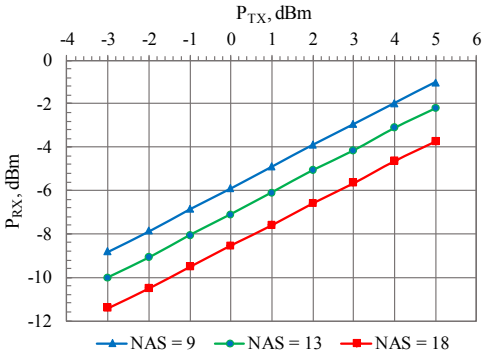


Fig. 8. $P_{RX} = f(P_{TX})$

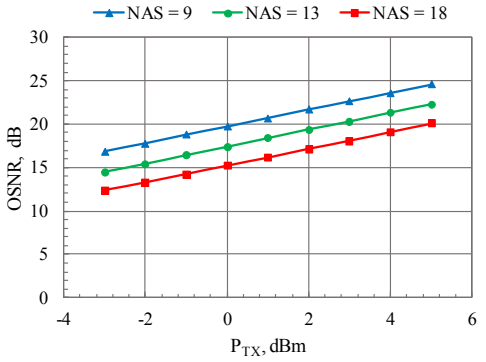


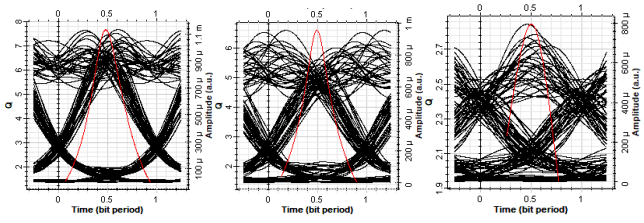
Fig. 9. $OSNR = f(P_{TX})$

As can be seen from the presented results, an optimal value of Q-factor (Fig. 6) and BER respectively (Fig. 7) is obtained for optical transmitted power P_{TX} = 3 dBm. On Fig. 10 is shown an eye diagram for the optimal case of 13 amplifying sections and input optical power P_{TX} = 3 dBm.

With a large number of amplifying sections, attenuation and dispersion in the fiber are high and the BER is worse than the accepted value 1.10^{-13}. The horizontal opening of the eye diagram shrinks due to the jitter and the vertical one – due to the greater attenuation and fiber dispersion and the insertion of noises.

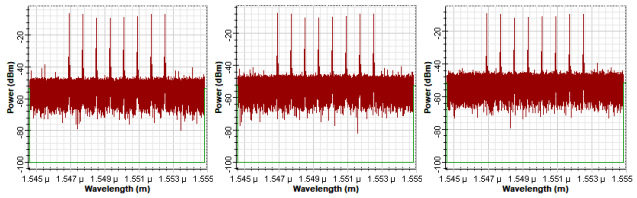
With fewer amplifying sections, the BER and Q-factor of the system are much better (Fig. 10a), but the length of the line is much smaller, which is economically ineffective.

In addition, losses and attenuation are less, but the received optical power may be very high, which produces non-linear distortions in the receiver and four-wave mixing of the signals (Fig. 11a).



a) N_{AS} = 9 b) N_{AS} = 13 (optimum) c) N_{AS} = 18

Fig. 10. Eye-diagram and Q-factor of the system



a) N_{AS} = 9 b) N_{AS} = 13 (optimum) c) N_{AS} = 18

Fig. 11. Optical spectrum diagram:

CONCLUSION

The results of the analytical application of the iterative approach and the developed simulation model are identical and predict with sufficient precision the behavior of the optical WDM network.

The iterative approach allows optimal determination of the number of amplifying sections based entirely on principal criteria. Therefore, the proposed approach is applicable and easy to use i.e. it is based on the physical characteristics of the used optical equipment.

As a future work on the developed model, it is possible to study the effect of different inserted noises and interference from non-linear effects on different input parameters and configurations of the optical communication equipment.

V. ACKNOWLEDGEMENTS

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A nanosecond-resolution method of TDC implementation, based on time-to-time converters

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Abstract – **Time-to-time converters (TTCs), also called time expanders, represent a useful approach to measurement of small-time intervals. In short, their aim is to take a small-time interval, expand it in the order of thousand to tens of thousand times and measure the resulting interval.**

The usual way they are being used is as a single standalone unit, doing all the work in a consecutive order for different time variant sources. In this paper we propose a different approach, consisting of multiple TTCs working in parallel, being synchronized to the first incoming event.

Keywords – **Time-to-time converters, programmable logic, calibration**

I. Introduction

The traditional approach of implementing a TTC can be objectively reduced to charging and discharging a capacitor. This introduces three main areas of operation for the converter, regarding the charging states:

- Low charge area – when the capacitor has been discharged and is just starting to gain charge – in this area voltage level advancement characteristically exhibits exponential and not entirely defined properties
- Linearly charging area – as the name suggests, in this area voltage level gradually rises, following a linear progression.
- High charge area – in this area, the voltage begins to slow its progression, at an exponential rate

Usually TTC working properties, such as accuracy, precision, dead time and so on are defined precisely for the linear charging area, as the other two are avoided. This introduces a working window for measuring time intervals smaller than hypothetical X seconds and larger than Y seconds. In order to mitigate this problem we use a method employing signal aligning to a reference clock and formation of an individual time interval for each signal, which changes in a much narrower range (2-4 periods of the reference frequency) [1]. This method has the advantage that it avoids measuring short intervals. It is illustrated on Fig. 1.

The pulses form the detectors are marked S0 - S3 and the pulses synchronized to the reference frequency are τ_{E0} - τ_{E3}, which are then fed to time-to-time converters (TTC).

The delays of the detector signals are measured as the difference of the lengths of the clock aligned pulses of the reference detector and the corresponding base plane detector. Their values are calculated after an analog-to-digital conversion.

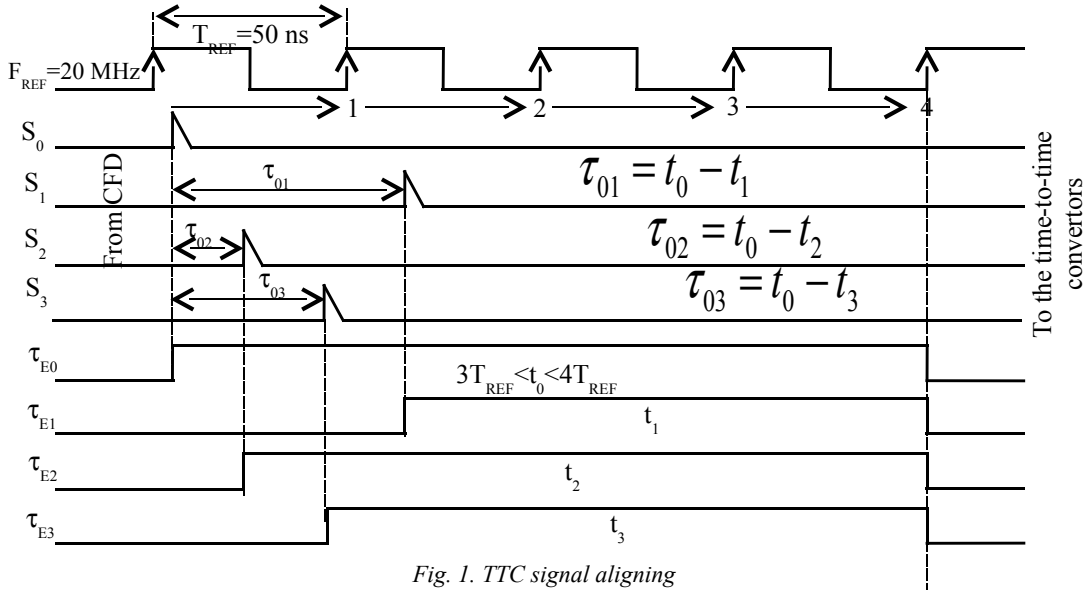

Fig. 1. TTC signal aligning

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II. Block Diagram

Figure 2 shows the block diagram of the signal processing circuit, which implements the method for measuring very short time delays. The constant fraction detectors (CFDn) normalize the amplitude of the input pulses, thus eliminating its influence on the process of input pulse moment determination [2].. The circuit has three modes of operation – "measurement", "test" and "auto-calibration".

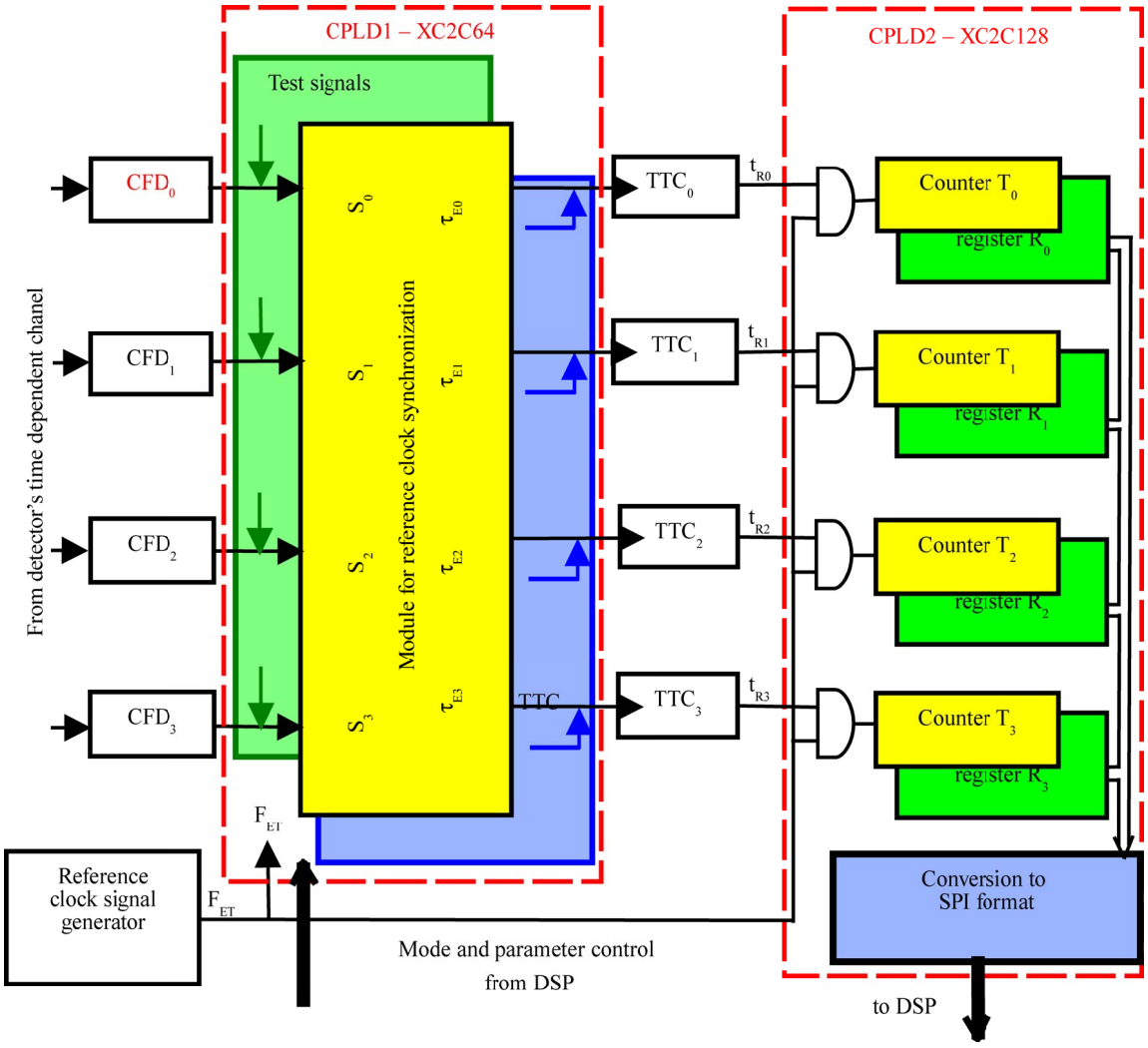

Fig. 2. Signal processing unit

In "measurement" mode the signal alignment circuit synchronizes the trailing edge of all CFD pulses to a single reference frequency (FREF) edge. Its output pulses are with variable length in the range of 100 to 200 ns, defined by the delay of individual input pulses. They are fed to the time-to-time converters which extend their length about 1000 times, in the range of 100 to 200 Ãs. Their length is then measured by counting the FREF pulses (with 50 ns period) that fit into the time interval. Thus the schematic is able to achieve 50 ps time domain resolution. The real aligned pulse length is calculated using the individual TTC conversion coefficients and the number of FREF pulse counts for the corresponding channel. The time delays of the input signals are calculated by subtracting the lengths of the base plane detector signals from the reference one (τ_{E0}).

This method is applicable for registration of low rate events, a few hundreds per second at the most, which is usually the case when registering Extended Air Showers (EAS).

In "auto-calibration" mode reference pulses with a known length are fed to the TTCs. Measuring the output pulse length allows the calculation of the individual TTC conversion coefficients. Determining their values is the key to measurement accuracy. The calibration signals circuit can generate 8 different reference signal lengths in the whole range of the expected input signal lengths, which allows for precise TTC calibration.

In "test" mode the CFD outputs are cut from the signal alignment circuit and it's fed with test pulses. That allows testing the circuitry without real input signals. Considering the low rate and the random nature of the EAS this mode allows for convenient and deterministic testing, tuning and repairs.

III. C. Input Signals Alignment to the Reference Frequency

The input signals alignment circuit is one of the main functional blocks in the system. Its schematic is shown on Figure 3. The formation process of an output pulse starts at the leading edge of the reference detector signal and ends at the 3rd consecutive leading edge of the reference clock. The output signals of the base plane detectors are triggered by their input leading edge only if it occurs within that time frame. After that a 50 ns reset pulse clears the flip-flops and forms the trailing edges of the output signals.

This circuitry is comprised of digital elements, which provides an opportunity for use of programmable logic. The benefits of this are better speed performance, better stability, better conformity for the TTCs and possibility for easier reconfiguration if required.

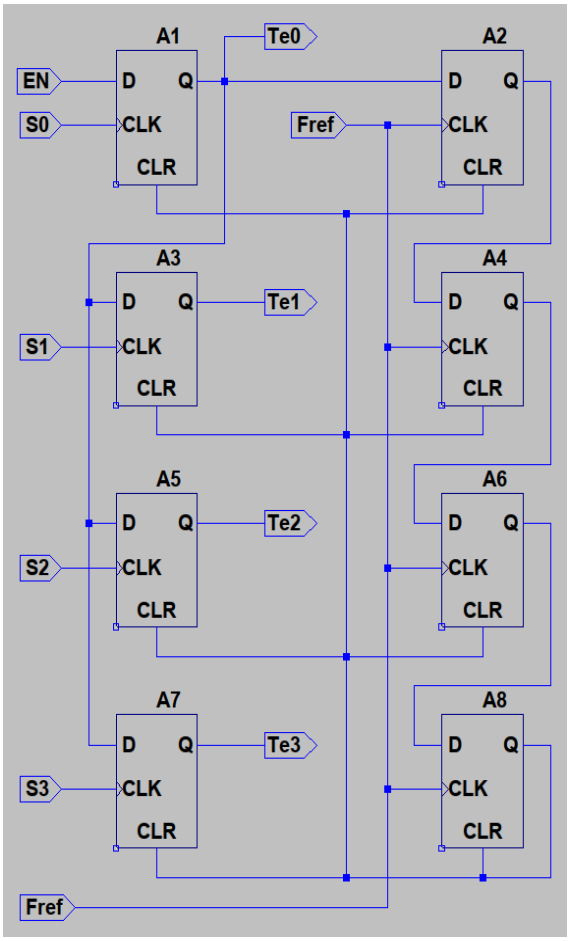

Fig. 3. Reference clock synchronization circuit

IV. Experimentation Results

Figure 4 represents an oscillogram showing the alignment of the reference detector (S0) signal to the reference clock. The oscilloscope was put in data logging mode. It can be seen that the leading edge varies with the moment of detector pulse input and the trailing edge is always aligned to the 3rd leading edge of the reference clock. For this test a 16 MHz clock was used to enable better visualization of leading edge jitter, caused by phase difference with the 40 MHz clock used for the test signals and TTC calibration pulses.

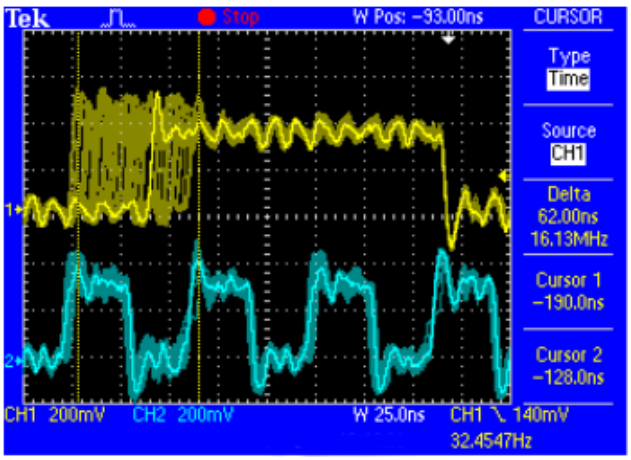

Fig. 4. Oscillogram of experimental results

V. Conclusion

A system has been developed, for establishing the delay of the signals coming from a group of high time-resolution detectors. The performed tests confirm that the proposed method, as well as the tested circuit, can be successfully applied for the signal processing.

Acknowledgments

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Input noise filtering and initialization of constant fraction discriminators

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Abstract – **Constant Fraction Discriminators (CFDs) are often used as the first step for signal modification for time measurement. Their purpose is to produce definitive time dependent property of a signal (usually a steep rising slope for a digital pulse) from a series of signals with wide array of amplitudes. In this paper we define two problems for the CFDs and provide a single solution for both.**

Keywords – **Constant Fraction Discriminators, time measurement**

I. Introduction

Precise determination of event occurrence moment is of utmost importance in time measurements. The resulting output signal must undergo amplitude normalization in order to be postprocessed in a logic circuitry. Accurate detection of an initial moment is dependent on amplitude fluctuations and shape variations of an input signal [1], [2]. To minimize the influence of these factors several schemotechnical approaches are applicable – fixed threshold circuit, zero crossing detector (with double signal differentiation) or a constant fraction discriminator (CFD) [4].

In CFD circuits the initial moment detection is independent of the input amplitude and is minimally influenced by the rise/fall time of the input signal. These circuits apply a strictly defined proportion of the input amplitude as a threshold level – an optimal level is generated for each input pulse in correspondence to its amplitude.

To put this principle into practice the input pulse is passed through two parallel channels – direct and delaying (fig. 1). In the direct channel an attenuator with a coefficient *k* reduces the amplitude of the pulse to a level corresponding to the ratio between the threshold and the initial amplitude. In the delaying channel the amplitude of the signal remains unchanged but a time delay is introduced. The value of this delay is calculated to ensure the delayed signal reaches the threshold level at the same time the direct signal is at its peak. A valid output is generated by the comparator K when the amplitude difference between the signals from the two channels changes its sign [5].

Constant fraction discriminators can operate in a wide dynamic range of input amplitudes (up to 1:1000) providing high precision of transient detection (±30 ps) [3]. These top-level features make the CFD broadly used and a preferred choice with signals of strongly varying amplitudes.

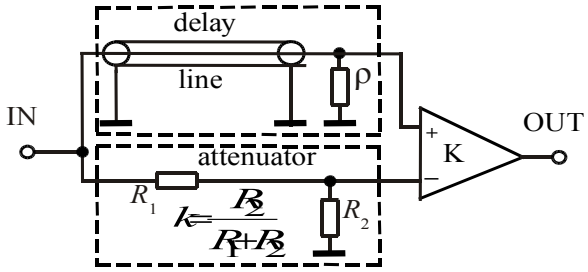

Fig. 1 Structure of a constant fraction discriminator

II. Basic CFD circuit construction

Fig. 2 shows the basic construction of a CFD for positive-only input signals.

The fast AD8561 comparator is powered by a positive supply voltage. Its propagation delay is 7 ns. and the CFD circuit is designed for pulses of approximately 10 ns. rise/fall time.

The delay line, constructed of passive (LC) elements, introduces 9.2 ns delay. Its characteristic resistance is 160 Ω.

The input attenuator (R1 and R2) is calculated to terminate a 75 Ω input signal cable.

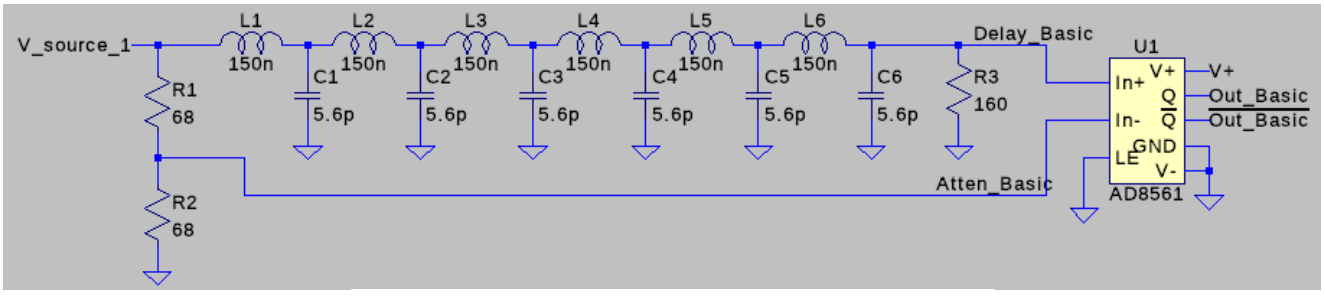

Fig. 2 Basic CFD schematic

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III. Problem identification

A. input signal noise

There exists a real possibility that low level voltage noise from the detector sources can trigger a false positive on the CFD. Aside from the obvious false detection, this also would disable the CFD for the duration of the comparator intrinsic propagation delay.

Fig. 3 shows the results of preliminary calculations (a simulation of the circuit). It is obvious that noise levels as low as 11 mV can trigger the above mentioned false positive – V(out_basic) goes HIGH (its TRUE state).

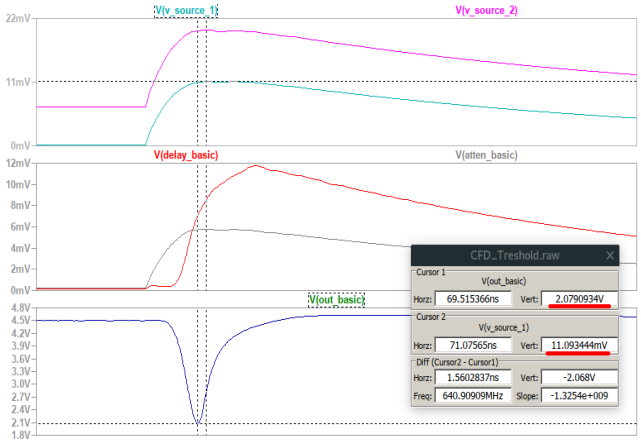

Fig. 3. Input noise triggering illustration

B. Comparator resetting

Since the attenuator reduces the source voltage level, and the delay line introduces almost no distortion (in terms of shape and level), the comparator theoretically would be stuck in its TRUE output state indefinitely. It would be set to FALSE only a short fraction of time (equal to the delay of the passive LC delay line) before going back to TRUE again. This is illustrated in fig. 3 (the setting of FALSE state) and fig. 4.

This is highly unwanted behavior, as it extends the dead time for the CFD.

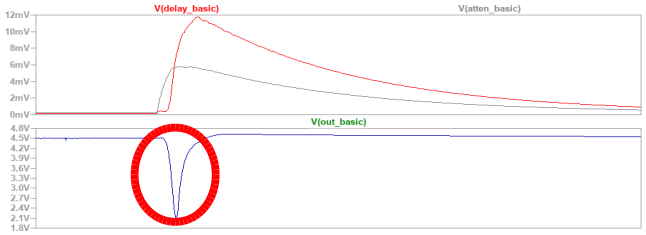

Fig. 4. Comparator non-reset state

IV. Proposed solution

Our proposed solution solves both problems by offsetting the attenuator voltage threshold. By doing this, for the problems:

A. input signal noise

Increased voltage threshold creates a barrier for low voltage level noises

B. Comparator resetting

Increased voltage level to the FALSE triggering state input for the comparator ensures faster state resetting.

The schematic is shown in fig. 5, as the enclosed in red is a simple voltage buffer, to ensure minimum cross-talk between the CFD source and threshold level source.

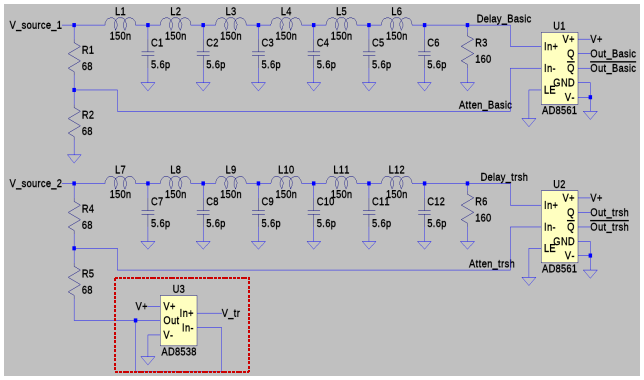

Fig. 5. Proposed solution schematic

Fig. 6 shows results of preliminary comparative calculations (a simulation of both circuits). As can be seen, the proposed solution has all the promises of working correctly.

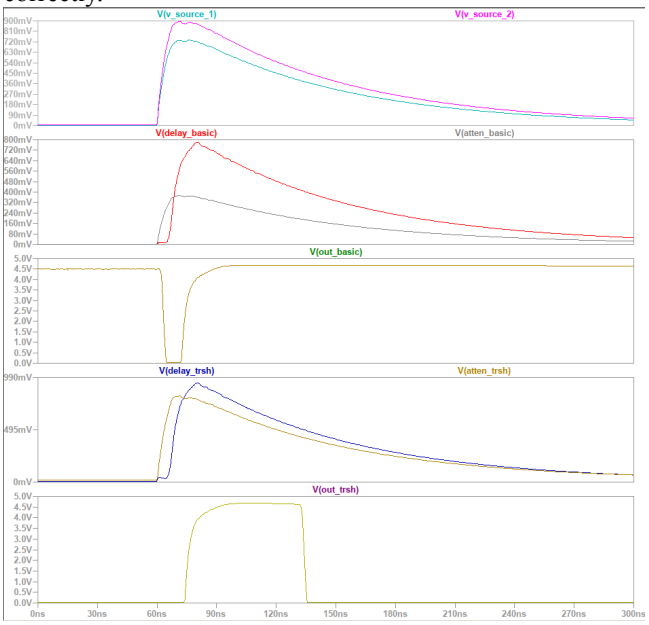

Fig. 6. Simulation comparative results

VI. Conclusion

Simulation results show a promising solution. As the experiments are currently ongoing, we will update the current paper, when the data is available.

Acknowledgments

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Corrosion Evaluation with Stepped Induction Thermography

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Abstract – **The aim of the paper is to studying the possibilities of stepped induction thermography for corrosion evaluation. It is proposed non-destructive and contactless corrosion evaluation method. It is presented accuracy decreasing factors and used solutions in proposed method. Test specimens made from different magnesium alloys is prepared. The results are presented in graphical form and discussed.**

Keywords – **stepped induction thermography, non-destructive evaluation, corrosion evaluation, active thermography**

I. Introduction

The corrosion is one of the serious problems for reliability of electronic systems. For this purpose, it is needed to study a new methods for corrosion evaluation, because classical method for corrosion evaluation are in many cases destructive, contact and it is needed preparation of tested surface, resulting in an increase in the cost of production. In addition, the use of destructive methods does not allow testing of the whole production, but only of the part. The use of non-destructive methods leads to an increase in the quality of the manufactured products due to the possibility of testing all or larger part of production as well as increasing their reliability due to the possibility of carrying out more reliability tests. The use of non-destructive methods, not requiring special treatment before testing, can significantly lower the cost of the final product and reduce the quality testing time as well as reduce the reliability test time.

In the electronics manufacturing are used a lot of metals and alloys which may corrode and corrosion evaluation is an important factor for high reliability. One of the materials which may corrode used in electronic systems are magnesium alloys due to their advantages. Magnesium alloys are an excellent for engineering applications when weight is an important in design of elements. Magnesium alloys have been widely used in recent years in the manufacturing of different parts for automotive, aerospace and portable computers industry. Magnesium is readily available and strong material and has good heat dissipation and good damping but it is extremely corrosive in wet environments.

A corrosion monitoring of components made from magnesium alloy can prevent relatively frequent cause for catastrophic failure.

The classical corrosion evaluation technique (including X-ray, microscopic, SEM-EDX) is most effective, but destructive and not always possible approach. In order to determinate an object state, and take decision about its fit for the needed purpose, very often non-invasive and non-destructive testing (NDT) is used. NDT includes wide group of techniques: acoustic, optical, radiography, electromagnetic, infrared. Corrosion of metals is usually evaluated using ultrasonic and eddy current methods of non-destructive testing. Disadvantages of these methods are the availability of special requirements to controlled surfaces, as well as presence of contact and low test performance. Infrared thermography (IRT) has already used successfully for non-destructive testing (NDT) of materials [1, 2] with rather slow thermal kinetics (composites, conductive or insulating materials, plastics, etc.).

In this work, we use active thermography approach for corrosion evaluation – stepped induction thermography. Contrary to the passive approach, an external thermal excitation is required for active thermography, it this case – eddy current excitation.

In stepped induction thermography, the examined specimen warmed up with induced long duration eddy current and the increase in specimen surface temperature is captured by IR camera during the active heating. The rate of surface temperature changing gives information about corroded surface, because the anomalies in the surface heating correspond to in-homogeneities in the material.

The presence of defects with high thermal resistance in a conductive material (such as corrosion products) can be easily detected using stepped thermography assessing the time of deviation in increase surface temperature over the defect, from its early time response.

Thermographic methods in some cases can be combined with the classic ones. Based on the results of the thermographic methods, it is possible to estimate which samples are to be tested with a more precise method. This allows cost savings and testing time to be reduced, as only individual specimens from the group of tested samples are tested by a more accurate method.

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II. Stepped Induction Thermography Principle

Stepped Induction thermography is based on three physical processes: heat diffusion, infrared radiation and eddy current induction.

Typical elements of the experimental setup for stepped thermography are a heat source and an infrared camera. Stepped thermography monitors the surface temperature rise of the tested object with respect to time during the application of a continuous step heating pulse. This technique is attractive for field application due to using simple equipment and test procedure. Stepped thermography use low power heating unlike conventional pulsed thermography. The variation of the surface temperature profile as a function of time depends on the heat diffusion inside the tested object, which is affected by the existence of corrosion.

The surface temperature will rise linearly with respect to the square root of time for infinitely thick homogeneous structure. This linear temperature rise for finite thickness structure will be affected by reflections of the thermal wave from the rear surface of the object. As a result, a non-linear rise in surface temperature begins at time, depending on the thickness. The presence of corrosion in the structure of the test object will cause a similar variation in the temperature with times and magnitudes specific to the location of corrosion and its severity.

Analysis of stepped thermography uses well known 1-D relationship for linearly temperature variation with the square root of time for a semi-infinitive plate (equation (1)).

$$T = \frac{2Q}{k}\sqrt{\frac{\alpha \cdot t}{\pi}} \tag{1}$$

where T [K] is the surface temperature, Q [W] is the uniform heat flux, k [W/m.K] is the thermal conductivity of the material, and α [m^2/s] is the thermal diffusivity and t [s] is the time.

The temperature response for small characteristic times is the same as that of a semi-infinite thickness. In this case, when increasing the time, the reaction deviates from the semi-infinite behavior of the plate due to reflections from the rear wall. Analytical solutions become more difficult for inhomogeneous plates (plates containing corrosion products). For analyzing 1-D heat conduction in layered materials can be used "quadripole method" [3]. Finite element method can be used in 3-D effects modeling in stepped thermography. It is shown that all errors for defect depth and thermal resistance of defects predicted from the early time behavior of the surface temperatures over the defects are less than 20 % when 1-D models are used [3].

It is shown for large defects in stepped thermography the early time behavior of the rising temperature over the defect depends on the defect depth and is independent of the lateral defect size [4].

After applying an electromagnetic field, the temperature of the material increases. Heat Q generated by dielectric loss (for dielectric materials) or the Joule heat (for conductive materials) will be conducted from inside to the surrounding material. The heat conduction equation is a time-dependent heat diffusion equation, where the first member of the sum defines the thermal diffusion until the second member of the sum defines the microwave heating. In this case $T = T(x, y, z, t)$ is the temperature distribution of the surface given by equation (2).

$$\frac{\partial T}{\partial t} = \frac{k}{\rho \cdot C_p}\left(\frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial y^2} + \frac{\partial^2 T}{\partial z^2}\right) + \\ + \frac{1}{\rho \cdot C_p} Q(x,y,z,t) \tag{2}$$

where $Q(x, y, z, t)$ is the heat generation function with induction heating, ρ is the density of specimen [kg/m^3] and C_p is the specific heat capacity of the specimen [J/(kg.K)].

For conductive materials, like metals and alloys, the induction heating is eddy current heating. Heat generated by induced eddy current heating can be expressed by the equation 3 [5].

$$Q \cong I_i^2 \sqrt{t \cdot \frac{\mu \cdot f}{\sigma}} \tag{3}$$

where, I_i [A] is the current through the inductor, σ [S/m] is the electrical conductivity, f [Hz] is the frequency of the induced current and μ [H/m] is the permeability.

During the practical thermography monitoring a measure for errors minimization should be taken, due to presence of dissipation and heat transfer problems.

During induction thermography measurements a part of power in the inductor is lost and the efficiency of induction heating should be evaluated using [5] and expressed by the equations (4) and (5).

$$\eta = \frac{P_p}{P_p + P_i} \cong \frac{1}{1 + \frac{2h}{r_i}\sqrt{\frac{\sigma_p}{\sigma_i \cdot \mu_i}}} \tag{4}$$

$$P_i = I(t)^2 \frac{l}{2\pi a s_I \sigma_I} \tag{5}$$

where η is the efficiency, P_p [W] is the power dissipated in specimen, P_i [W] is the power dissipated in inductor, h [m] is the distance from the inductor to the surface, r_i [m] is the radius of the inductor, σ_p [S/m] is the electrical conductivity of the tested specimen, σ_i [S/m] is the electrical conductivity of the inductor and μ_i [H/m] is the permeability of the inductor. Equation (4) indicates that the permeability of the inductor material should be as close to 1 as possible and that the electrical conductivity of the inductor should be as high as possible. Therefore, most inductors are made out of copper.

Characterization of corrosion products (determination of parameters such as depth, size and heat resistance using stepped induction thermography is a complex inverse heat transfer problem. Algorithms for defect characterization can be based on numerical modeling, analytical methods,

statistical analysis or black-box methods (neural network, fuzzy logic) and others.

III. Corrosion Evaluation Method

The possibility for corrosion evaluation with using stepped induction thermography is based on the difference between metals or alloys and corrosion products in magnetic characteristics. The dissipated power in metal or alloy is significantly greater than dissipated power in corrosion products [6]. If one metal specimen is measured before and after treatment in corrosive environment, the heating rate will be different. The weight of metal or alloy part of specimen before treatment in corrosive environment is more than after this treatment and the heating rate of specimen before treatment is lower.

The proposed corrosion evaluation method contains these steps:

- adjustment of the heating power with respect to tested specimen characteristics;
- placement of the tested specimen;
- turning on the induction heating system and staring capturing of IR thermogram sequence;
- turning off the induction heating system and stopping capturing of IR thermogram sequence after it is reached set time.

The used for corrosion evaluation parameter is difference between surface temperature of non-corroded specimen and specimen with corrosion (with same material and dimensions or one specimen before and after treatment in corrosive environment).

The accuracy of the proposed method depends on many factors:

- environment parameters;
- environment parameters variations during measurement;
- reflections of IR electromagnetic waves from surface of the tested specimen;
- emissivity differences between tested specimens materials and the high emissivity difference between surface of non-corroded and corroded specimen;
- dependence between output heating power of induction heating system and specifications of tested specimen;
- convective heat transfer between induction heating system and tested sample.

The usage of IR camera makes possibility for simultaneously capturing of more than one specimen, if there is no significant heat transfer between specimens.

This method can decrease significantly time for reliability testing due to its non-destructivity.

IV. Stepped Induction Thermography Experimental Setup

The induction heating system is realized with using a push-pull inverter [7]. The block diagram of the inverter is shown on fig. 1. The inverter contains power part (inductor - for induction heating of the test specimen, output capacitor, power switching elements and input filter) and control part (control block and feedback transformer).

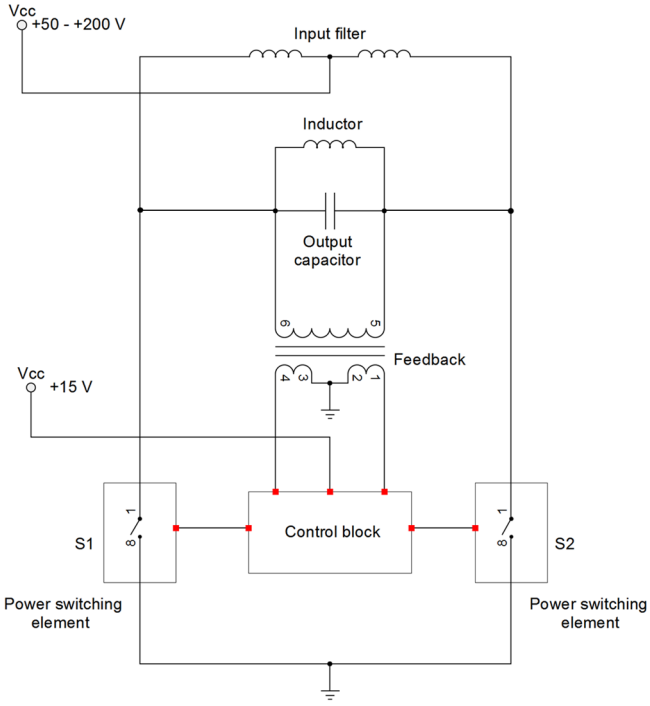

Fig. 1. Block diagram of used inverter

The used IR camera is FLIR SC640 with resolution of 640 × 480 and frame rate of 30 frames per second.

For studying the possibilities of the proposed method, tested samples from different magnesium alloys with known characteristics (AZ91, AM50 and AE42) are prepared. The specimens are with cylindrical shape with a diameter of 13 mm and height of 6 mm. As corrosion environment is used 3.5 % NaCl solution. The samples are immersed for 24 hours in corrosion solution. The samples before and after preparation in corrosion environment are studied. The distance between IR camera and the surface of tested specimen is approximately 40 cm.

For decreasing the effect of described in above factors are used these solutions:

- calibrating the IR camera with environment parameters before measurement;
- it is used special box for decreasing the effect of environment parameters variations during measurement and reflections from the surface of tested specimen;
- it is made emissivity correction for surface temperature of tested specimens with using of black thermal resistant tape;
- used inverter has low dependence between output heating power and specifications of tested sample due to used feedback. Also it is used stabilized current mode power supply for power part of the inverter also for decreasing this dependence;
- it is used water cooling of the inductor, output capacitor and power switching elements.

For processing of IR thermograms is used software ThermaCAM Researcher.

V. Experimental Results and Discussion

IR thermogram of corroded specimen is shown on fig. 2. It can be seen, that the surface areas with corrosion of specimen has higher emissivity than areas without corrosion (red areas is the areas with corrosion products and yellow areas is areas without corrosion products). The red color represents higher temperature than yellow color. The real temperature difference between areas with corrosion and areas without corrosion is significantly lower than measured with the IR camera, because the measured temperature depends strongly from the emissivity. For this reason, it is used maximum surface temperature for corrosion evaluation and emissivity correction.

The emissivity depends not only from surface material but also from thickness (different corrosion products thickness – different emissivity). This dependence can be used for quantitative corrosion evaluation [6].

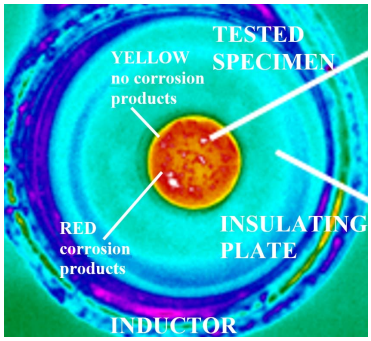

Fig. 2. IR thermogram of corroded specimen

Results from measurement of the tested samples using proposed method are shown on fig. 3.

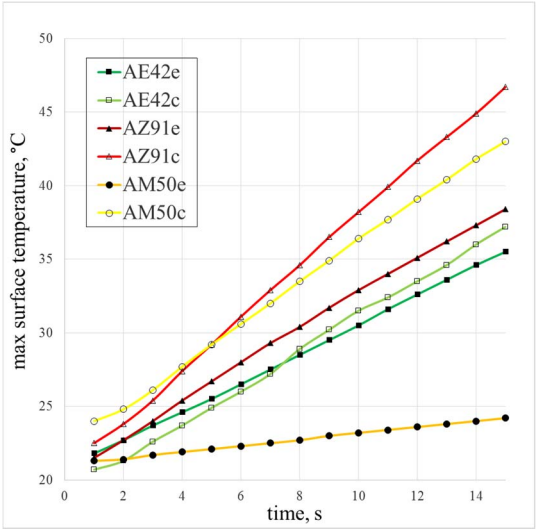

Fig. 3. Results from measurement (index e – specimen without corrosion products, index c – specimen with corrosion products)

It is shown, that surface temperature of specimen with corrosion products at time moment 14 s (time for heating) is higher than surface temperature of specimen without corrosion products due to lower heating rate of specimen without corrosion (higher percentage weight metal or alloy – lower heating rate at constant heating power).

Also the difference between surface temperature of specimen with corrosion products and without corrosion products made from same alloy is different, because the different alloys has different amount corrosion products on the surface (AM50 has more corrosion products on its surface than AE42 [6]).

It is shown also, that the surface temperature of specimens without corrosion products made from different alloys is different. Specimens made from different alloys have different magnetic and electrical properties and therefore the dissipated power in specimens is different (it can be seen the dependence of generated heat from permeability and electrical conductivity from equation (3)).

After measurement, it is used weight loss method with using of analytical balance for determination of corrosion products weight. The corrosion products weights are approximately 0.1 – 0.8 % from the weight of specimens [6]. From fig. 3 can be seen that this low difference in metal or alloy part weight of specimen leads to a noticeable difference in heating time. Therefore this method can determine presence of corrosion products with high sensitivity for more applications.

VI. Conclusion

It is proposed method for non-destructive and contactless corrosion evaluation and it is presented accuracy decreasing factors of this method and solutions for decreasing the effect of these factors.

It is performed a stepped induction thermography measurement and it is studied the possibility for using this method for corrosion evaluation.

The proposed method can decrease significantly time for reliability testing due to its non-destructivity and fastness, because it is not needed to stopping the reliability testing system for a long time for measurements.

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Dynamical Reliability Estimation and Critical State Early Detection by Application of FIDES Guide 2009

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Abstract – **This article presents an approach to dynamical assessing the reliability of electronic systems. Such an assessment can be done on the basis of information collected for a given set of factors describing various aspects of the life of the system, and affecting its reliability. The reliability is assessed by applying the methodology proposed in FIDES guide 2009 by evaluating the failure rates of electronic system items and their current deviations from the values previously accepted as normal.**

Keywords – **reliability prediction, failure rate, FIDES**

I. Introduction

Nowadays the electronic systems are characterized by high level of reliability, resulting from technology development. The operational reliability estimation based on statistical data for failure occurrence is a difficult task because such failures are extremely rare or missing. Different approaches are performed to solve this problem. There are works there on identification of "healthy" and "bad" areas in the system states domain, and definition of boundary states ascertainment of these could be a signal for approaching a critical state so the maintenance team to undertake appropriate actions. M. Pecht put accent on these problems in [1], formulating the term Prognostics and Health Management (PHM) suggested especially for information and electronics-rich systems. The contemporary approaches in this area most frequently apply methods and techniques usually put in to practice in regard to the artificial intellect and machine learning. Very often is applied the "novelty detection" approach, also known as one-class classification method, as an approach to selection of anomalies [6]. Such approach is presented in [2], by usage of Bayesian Support Vector Machine. Fuzzy sets approach is a method also used for electronic system reliability estimation in cases when there is insufficiency of initial information there [3,4]. The Negative selection is another possible way to identify an upcoming problem in system operation [5].

This article presents an approach to dynamical reliability state assessment of a technical system comprising electronic components and units. This requires periodical or continuous collection of data regarding certain set of parameters, reflecting different aspects of the system operation. These parameters are for example temperature, humidity, vibrations etc. Additionally is collected information regarding different system operational modes, their duration and consecution, required for depiction of so called "life profile" (LP) of the system. The reliability state assessment is performed applying the methodology and reliability data presented in FIDES guide 2009 [7], by failure rate estimation of system components and the current deviation in their values from such, set in advance as normal ones. FIDES guide 2009 is a well-known reliability prediction tool, which methodology is studied and compared to others of this kind in [8].

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II. Basic formulations of FIDES guide 2009

FIDES guide 2009 [7] presents an approach to failure rates λ estimations prediction in regard to electronic items in the form.

$$\lambda = (\Sigma_{Physical\_contributions})\mathrm{X}(\Pi_{Process\_contributions}) \qquad (1)$$

where $(\Sigma_{Physical\_contributions})$ represents the impact of physical and technological factors to reliability; and $(\Pi_{Process\_contributions})$ represents the impact of the development, production and operation process on reliability.

As the latter does not change itself during the operational life of devices, only the former is this which might be ascertained changes in, and to play the role of indicator for upcoming undesirable changes in the device monitored. The part $(\Sigma_{Physical\_contributions})$ is represented by $\lambda_{\mathrm{Physical}}$, which is an assessment of the physical contributions to the items failure rate estimation value λ. The factors, which belong to the physical contributions set, are grouped into two main groups: direct impact physical stress factors, also called acceleration factors, and induced impact stress factors. Examples for the first group factors are: thermal stresses, electrical stresses, humidity stresses. The second group factors are these which could change themselves according to the usage environment. For the value of $\lambda_{\mathrm{Physical}}$ is given the equation

$$\lambda_{\mathrm{Physical}} = [\Sigma_{Physical\_contributions}(\lambda_0.\Pi_{Acceleration})].\Pi_{Induced} \qquad (2)$$

where λ_0 is the basic failure rate of the item; $\Pi_{Acceleration}$ represents the contribution of normal stresses; $\Pi_{Induced}$ represents the contribution of induced factors, inherent to an usage environment. For example, the general model of $\lambda_{\mathrm{Physical}}$ associated with resistors is

$$\lambda_{Physical} = \lambda_{0_{Resistance}} \cdot \sum_i^{Phases} \left[\left(\frac{t_{annual}}{8760} \right)_i \cdot \begin{pmatrix} \Pi_{Thermo-electrical} + \\ \Pi_{TCy} + \Pi_{Mechanical} + \Pi_{RH} \end{pmatrix}_i \cdot (\Pi_{Induced})_i \right] \quad (3)$$

and for each of contribution factors Π within, the equations are as follow

$$\Pi_{\substack{Thermo \\ -electrical}} = \gamma_{TH-EL} \cdot exp\left[11604.0{,}15. \left(\frac{\frac{1}{293} - }{T_{\substack{board \\ -ambient}} + 273 + A. \frac{P_{applied}}{P_{rated}}} \right) \right], \quad (4)$$

$$\Pi_{TCy} = \gamma_{TCy} \cdot \left(\frac{12. N_{annual-cy}}{t_{annual}} \right) \cdot \left(\frac{min(\theta_{cy}, 2)}{2} \right)^{\frac{1}{3}} \cdot \left(\frac{\Delta T_{cycling}}{20} \right)^{1,9} \cdot exp\left[1414. \left(\frac{1}{313} - \frac{1}{T_{max-cycling} + 273} \right) \right], \quad (5)$$

$$\Pi_{Mechanical} = \gamma_{Mech} \cdot \left(\frac{G_{RMS}}{0,5} \right)^{1,5}, \quad (6)$$

$$\Pi_{RH} = \gamma_{RH} \cdot \left(\frac{RH_{ambient}}{70} \right)^{4,4} \cdot exp\left[11604.0{,}9. \left(\frac{1}{293} - \frac{1}{T_{board-ambient} + 273} \right) \right] \quad (7)$$

$$\Pi_{induced} = \left(\Pi_{placement} \cdot \Pi_{application} \cdot \Pi_{ruggedising} \right)^{0,511.\ln(C_{sensibility})}, \quad (8)$$

where: t_{annual} is the time associated with each phase over a year (in hours); γ_{TH-EL}, γ_{TCy}, γ_{Mech} and γ_{RH} are initial values of the respective contribution factors; $RH_{ambient}$ is the relative humidity associated with a phase, [%]; $T_{board-ambient}$ is the average board temperature during a phase, [°C]; $\Delta T_{cycling}$ is the amplitude of the temperature variation, associated with a cycling phase [°C]; $T_{max-cycling}$ is the maximum board temperature during a cycling phase [°C]; $N_{annual-cy}$ is the number of cycles associated with each cycling phase over a year [cycles]; θ_{cy} is the cycle duration [hours]; G_{RMS} is the vibration amplitude associated with each random vibration phase [G_{rms}]; A is the maximal working temperature, [°C]; $P_{applied}$ is the power dissipated by a component during a phase [W]; P_{rated} is the maximum admissible power dissipated by a component specified by the supplier [W]; $\Pi_{placement}$ represents the influence of the item placement in the equipment or the system; $\Pi_{application}$ represents the influence of the usage environment for application of the product containing the item; $\Pi_{ruggedising}$ represents the influence of the policy for taking account of overstresses in the product development; $C_{sensibility}$ represents the coefficient of sensitivity to overstresses inherent to the item technology considered.

Regarding electronic units FIDES 2009 suggests a methodology for assessing the failure rates. The formulae have similar structure to those shown above. For instance, the AC/DC converter's $\lambda_{Physical}$ is estimated as follows:

$$\lambda_{Physical} = \sum_i^{Phases} \left[\left(\frac{t_{annual}}{8760} \right)_i \cdot \begin{pmatrix} \lambda_{0TH-TCY} \cdot (\gamma_{TH} \cdot \Pi_{TH} + \gamma_{TCy} \cdot \Pi_{TCy}) \\ + \lambda_{0M-RH} \cdot (\gamma_M \cdot \Pi_M + \gamma_{RH} \cdot \Pi_{RH}) \end{pmatrix}_i \cdot (\Pi_{Induced})_i \right]. \quad (9)$$

It can be seen that the difference, comparing with (3) is appearance of two basic failure rates $\lambda_{0TH-TCY}$ and λ_{0M-RH}, which values depend on the features of the units:

$$\lambda_{0TH-TCY} = \sqrt{1150 + 86. \sqrt{P}. \ln(P)}, \quad (10)$$

$$\lambda_{0M-RH} = \frac{1}{6{,}48.10^{-3} + 0{,}296. \frac{\ln(Vol)}{Vol}}. \quad (11)$$

where P is the output power of the unit in Watts, and Vol is the volume of the unit, in cm^3.

The data regarding current status of the factors, listed above, can be used as a basis for reaching a conclusion for existence of disturbing change tendencies of current values of the reliability indices monitored. Many of them can be used for the purpose of planning and conduction of maintenance of complex electronic systems, as presented in [9,10]. From one hand, as indicators of a pre-failure state can be used the estimated failure rate values exceeded the admissible ones, set in advance, or accelerated crawling failure rate increase, which is a presage of a parametrical failure, and ascertainment of rapid failure rate increase, comparing to the previous value, which is a presage of a sudden failure, from the other. Such type of data in combination with information on operational modes and the "life profile" (LP) can form a set of indicators which identify the current status of an item under study within a space of states, divided in advance to area of "normal operation", "transitional zone" and "pre-failure state". Going out of the "normal operation" area must be considered as a signal for execution of certain maintenance activities different in their scope and particularity.

Analyzing the factors presented above it is ascertained that some of them are predetermined by the item production process and cannot change themselves. Therefore they cannot be used for a dynamic reliability analysis. Such factors are $\Pi_{placement}$, $\Pi_{ruggedising}$ and $C_{sensibility}$.

TABLE 1. INDICES OF THE CONTRIBUTION FACTORS RELATED TO DIFFERENT TYPES OF ELECTRONIC COMPONENTS

IC, Discrete semiconductors*, LED, Optocouplers	**Resistors*, Fuses****	**Capacitors – ceramic, aluminium, tantalum**	**Inductors and Transformers**	**Piezo-electric components**	**Electromechanical relays, Switches**	**PCB**	**Connectors**
t_{annual}	t_{annual}	t_{annual}	t_{annual}	t_{annual}	t_{annual}	t_{annual}	t_{annual}
N_{ann-cy}	N_{ann-cy}	N_{ann-cy}	N_{ann-cy}	N_{ann-cy}	N_{ann-cy}	N_{ann-cy}	N_{ann-cy}
$\Delta T_{cycling}$	$\Delta T_{cycling}$	$\Delta T_{cycling}$	$\Delta T_{cycling}$	$\Delta T_{cycling}$	$\Delta T_{cycling}$	$\Delta T_{cycling}$	$\Delta T_{cycling}$
$T_{max-cycling}$	$T_{max-cycling}$	$T_{max-cycling}$	$T_{max-cycling}$	$T_{max-cycling}$	$T_{max-cycling}$	$T_{max-cycling}$	$T_{max-cycling}$
θ_{cy}	θ_{cy}	θ_{cy}	θ_{cy}	θ_{cy}	θ_{cy}	θ_{cy}	θ_{cy}
G_{rms}	G_{rms}	G_{rms}	G_{rms}	G_{rms}	G_{rms}	G_{rms}	G_{rms}
$RH_{ambient}$	$RH_{ambient}$	$V_{applied}$	$T_{board-ambient}$	$RH_{ambient}$	$RH_{ambient}$	$RH_{ambient}$	$RH_{ambient}$
$T_{board-ambient}$	$T_{board-ambient}$	$T_{board-ambient}$	ΔT	$T_{board-ambient}$	$T_{ambient}$	$T_{board-ambient}$	$T_{board-ambient}$
P_{diss}	$P_{applied}$*			I_{output}	$V_{contact}$		ΔT
$V_{applied}$*	$I_{applied}$**				$I_{contact}$		$I_{contact}$
T_j					V_{coil}*		

TABLE 2. INDICES OF THE CONTRIBUTION FACTORS RELATED TO THEIR INHERENT FEATURES

Time/number of cycles	**Termal and thermal cycles**	**Environmental**	**Electrical**
t_{annual}	$\Delta T_{cycling}$	G_{rms}	$P_{dissipated}$
$N_{annual\text{-}cy}$	$T_{max\text{-}cycling}$	$RH_{ambient}$	$V_{applied}$
θ_{cy}	$T_{board\text{-}ambient}$	Saline pollution	$I_{applied}$
Number of operations per hour	T_j	Application pollution	Load type
	ΔT	Environmental pollution	

III. SELECTION OF INDICES FOR MONITORING

Considering the overview of FIDES guide 2009 [7], is performed a grouping of indices in regard to respective contribution factors and related to different types of electronic components. It is presented in Table 1. Some indices are not shown there because of their impact on few types of components.

In their inherent features the contribution factors and the respective indices can be determined as thermal, electrical, thermal cycling, mechanical, humidity, chemical etc. The grouping in regard to these features is shown on Table 2.

There are some indices in the tables, which are not explained previously in the article, and they are listed below: T_j is the junction temperature of Integrated Circuits and discrete semiconductors; ΔT is the insert temperature increase for connectors, inductors and transformers; $V_{applied}$ and $I_{applied}$ are respectively the operating voltages and currents; "Load type" represents whether the load is of resistive, inductive or capacitive type, or an incandescent lamp; "Number of operations per hour" is the number of maneuvers per hour of relays and switches; "Saline pollution level" represents the assessment of the level of saline in the ambient area by two levels, low and high; "Application pollution level" and "Environmental pollution level" represent the assessment of the pollution level depending respectively on the placement of the item in the system or on the environmental conditions, by three levels, low, moderate and high.

The indices listed above are selected as they might demonstrate deviations in their current values from the values applied for initial reliability indices estimation of certain electronic item. The "Number of operations per hour" of a relay, for example, might increase or decrease, which leads to the relay's failure rate estimation change.

Except of monitoring of the changes in the entire item failure rate, it is also necessary to be assessed the importance of each particular index or a group of indices in order to appraise the additional information for the current status of the item, provided by them. The ascertainment of an increased value of T_j of an IC can be an indicator of a probable incoming failure, despite of lack of changes in value of the item failure rate. From the other hand it is also possible the indices of a group to change themselves moderately but this to result in a tangible increase of the failure rate estimation of the item. Thus the dynamical failure rate estimation represents itself as an integral indicator for an upcoming failure.

IV. CASE STUDIES

Two electronic devices are tested, applying the approach described above: an electronic unit AC/DC converter and an electronic component, such as power film resistor. The impact of the different LP parameters on the devices failure rates is put under study. The assessment of $\lambda_{Physical}$ is performed according to the methodology of FIDES guide 2009, in FIT (failures per 10^9 hours). Two life profiles are applied – standard LP and industrial LP [7], which parameters are shown in Table 3. It is accepted that the values of $\Pi_{Induced}$ remain constant. Values of $\gamma_{TH\text{-}EL}(\gamma_{TH})$, γ_{TCy}, γ_{Mech} and γ_{RH} are shown in Table 4. The referent value $\lambda_{0Resistor}$ is 0,4 FIT.

TABLE 4. VALUES OF $\gamma_{TH\text{-}EL}(\gamma_{TH})$, γ_{TCy}, γ_{Mech} and γ_{RH}

	$\gamma_{TH}/\gamma_{TH\text{-}EL}$	γ_{TCy}	γ_{Mech}	γ_{RH}
AC/DC converter	0,359	0,523	0,09	0,028
Power film resistor	0,04	0,89	0,01	0,06

A. AC/DC converter

The calculations of $\lambda_{Physical}$ are performed using equations (9-11). It is chosen that $P=500W$ and $Vol=1000cm^3$. The results obtained are two significantly different values of $\lambda_{Physical}$:

$\lambda_{Physical}^{AC/DC}(standard\ LP) = 331{,}71\ FIT$,

$\lambda_{Physical}^{AC/DC}(industrial\ LP) = 2902{,}94\ FIT$.

These different values of $\lambda_{Physical}$ also determine a significant difference in the reliability function P(t) of the module complying with exponential distribution law, which is clearly seen in Figure 1.

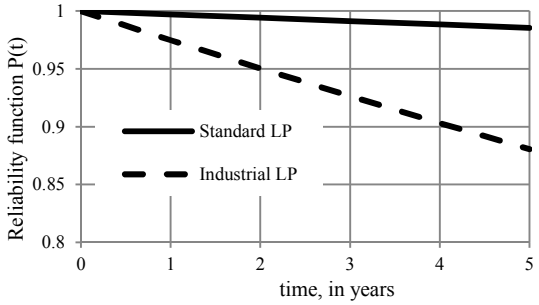

Fig.1. Reliability function curves for standard and industrial life profiles.

TABLE 3. PARAMETERS OF THE STANDARD LIFE PROFILE AND THE INDUSTRIAL LIFE PROFILE

Phase	t_{annual}	on/off	$T_{ambient}$	RH	ΔT	$N_{ann\text{-}cy}$	θ_{cy}	$T_{max\text{-}cycling}$	G_{rms}	Saline pollution	Environmental pollution	Application pollution	Protection level	$\Pi_{Induced}$
Standard LP														
Dormant	5110	off	20	70	5	365	14	23	0	low	low	low	non herm	1
Operation	3650	on	40	22	20	365	10	40	7	low	low	low	non herm	1.9
Industrial LP														
Operation 1	2450	on	30	30	15	350	7	30	0.1	low	high	moderate	non herm	5.1
Operation 2	3500	on	55	30	25	1400	2.5	55	0.1	low	high	moderate	non herm	4.6
Dormant	2810	off	15	80	10	365	7.7	20	0	low	high	moderate	non herm	2.6

TABLE 5. CHANGES OF $\lambda_{Physical}$ OF THE CONVERTER DEPENDING ON THE CHANGES OF THE LIFE PROFILE PARAMETERS

AC/DC converter	**$T_{ambient}$ in operation phase, °C**				
	40	45	50	55	60
$\lambda_{Physical}$	331,71	398,88	480,42	578,80	696,82
	ΔT in operation phase, °C				
	20	25	30	35	40
$\lambda_{Physical}$	331,71	441,36	580,26	752,32	961,65
	$N_{ann\text{-}cy}$/ θ_{cy} in operation phase, hours				
	365/10	730/5	1095/3.3	1460/2.5	2190/1.6
$\lambda_{Physical}$	331,71	388,58	445,45	502,31	591,59
	G_{rms} in operation phase				
	0.5	3	5	6	7
$\lambda_{Physical}$	331,71	446,18	587,65	670,79	761,17

The impact of the individual factors, influencing on reliability, is examined independently in relation to the initial, accepted as normal conditions of the standard life profile. The results are shown in Table 5.

B. Power film resistor

The calculations of $\lambda_{Physical}$ are performed by usage of formulae (3-8). For this pupose there are chosen temperature and electrical stress parameters values as follow: P_{rated}=2W; A=130°C; $P_{applied}$=1W.

The results obtained for $\lambda_{Physical}$ in both profiles are listed below:

$\lambda_{Physical}^{Resistor}(standard\ LP) = 0{,}998\ FIT$,

$\lambda_{Physical}^{Resistor}(industrial\ LP) = 6{,}656\ FIT$.

Table 6 presents the results obtained for the impact of the separately and independently changed parameters on the resistor's $\lambda_{Physical}$.

TABLE 6. CHANGES OF $\lambda_{Physical}$ OF THE RESISTOR DEPENDING ON THE CHANGES OF THE LIFE PROFILE PARAMETERS

Power film resistor	$T_{ambient}$ / ΔT / $T_{max\text{-}cy}$ in operation phase, °C				
	40/20/40	45/25/50	50/25/55	50/30/60	55/35/65
$\lambda_{Physical}$	0,998	1.645	1.756	2.564	3.595
	$N_{ann\text{-}cy}$/ θ_{cy} in operation phase, hours				
	365/10	730/5	1095/3.3	1460/2.5	2190/1.6
$\lambda_{Physical}$	0.998	1.843	2.689	3.534	4.862
	G_{rms} in operation phase				
	0.5	3	5	6	7
$\lambda_{Physical}$	0.998	1.106	1.24	1.319	1.404

The results show that the reliability indices, as in this case the monitored $\lambda_{Physical}$ of an electronic unit or of a single component, change their values significantly when the operational parameters are changing. If there are estimated the initial failure rates λ_{i0} for each component or unit and also for the entire system λ_{SYS0}, the information collected about a set of parameters, such as those considered in the cases above, could be used also for estimation of their changes, as in the absolute value $\Delta\lambda_i$ as well as in dynamic of the change $V_{\lambda i}$. Then the system status can be assessed considering criteria set in advance, regarding the admissible limits of the deviations $\Delta\lambda_i$ and the velocities of changes $V_{\lambda i}$ of all critical components and also for the entire system, separately or by an integral index ε summarizing all relative values of the failure rate deviations, multiplied by a weight coefficients ω_i also set in advance:

$$\varepsilon = \frac{\Delta\lambda_1}{\lambda_{10}}.\omega_1 + \frac{\Delta\lambda_2}{\lambda_{20}}.\omega_2 + \cdots + \frac{\Delta\lambda_n}{\lambda_{n0}}.\omega_n + \frac{\Delta\lambda_{SYS}}{\lambda_{SYS0}}.\omega_{SYS} \qquad (12)$$

Based on the data obtained it must be taken a decision for undertaking proper activities in line with technical maintenance plans regarding the system monitored.

V. CONCLUSIONS AND FINAL REMARKS

As it is presented above, the approach to dynamical assessment of the electronic systems reliability status suggested by this article has the aim to give an opportunity for to avoid of system failures during the system operation by early detection of the failures probability increase, particularly in regard to highly reliable and critical complex electronic systems, trough introduction of specific set of indices.

The deviation values of the critical components failure rates, as well as these of the entire system, can play the role of primary indicators of system reliability status. The integral index introduced, expands the approach applicability to early pre-failure states detection, by ascertainment of undesired tendencies in the current system condition, which could lead to a system reliability decrease, but cannot be detected through the usage of the primary indicators only.

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Infrared Survey in Electrical Preventive Maintenance

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Abstract – **The article discusses the basic elements of procedure applicable to programs for maintenance of electrical equipment with infrared inspection. Based on accumulated experience of experimental thermographic measurement of electrical equipment in different companies was proposed approach to creating a typical procedure, taking into account the specificities of the studied electrical equipment and targets set.**

Keywords – **Infrared Thermography, Electrical Preventive Maintenance**

I. INTRODUCTION

Increasingly widespread introduction into operation of advanced technologies for assessment of electrical installations, leads to ensure safety, reliability and economy of enterprises. Infrared thermography (IRT) successfully has the function of a powerful diagnostic tool for predictable maintenance of facilities of various engineering fields [1]. By detection of thermal anomalies often invisible to the human eye, infrared thermography allows take corrective impacts before the work of relevant electrical or mechanical equipment and production lines get out the nominal operating parameters. An increasing number of industry standards for safety and preventive programs include the use of infrared inspection at least once every three years [2] A justification for the additional cost of infrared measurements are great possibilities of thermal control. Infrared thermography has established itself as a key element of the thorough electrical preventive maintenance (EPM) programs due to the destructive nature and the possibility to control the operational status of the electrical equipment and components without interrupting their work.

Practical use of infrared technique requires qualified engineers to perform the inspection and the use of different procedures for processing and analysis of images. It is often discussed a typical infrared scanning procedure, without a common understanding what is included in it.

This article presents the vision of the key elements of the inspection procedure of electrical equipment, which is applied to the inspection of several companies in Bulgaria.

II. THERMAL ANOMALIES MEASUREMENTS BY INFRARED THERMOGRAPHY

Overheating of electrical components and equipment can lead to potential unplanned outages or violation of efficiency due to heat generation and unnecessary losses [3].

Typical problems regarding heat in electrical equipment are bad contact connections, short circuit, and overload, defects in the body of the equipment or its components.

Two ways to analyze the thermal characteristics in electrical equipment are used - quantitative and qualitative evaluation [4], [5]. The quantitative measurements usually are difficult to obtain. It needs determination the real and accurate temperature value, the true emissivity value and atmospheric attenuation. The qualitative measurement, considers the relative temperature value of a particular hotspot with respect to other equipment in a similar environment. The second way is widely used to evaluate electrical systems by employing Delta T (temperature difference) criteria [6]. The levels of severity of the suspected electrical systems were classified into four categories, according to the International Electrical Testing Association (NETA) standards [6]. The temperature criteria indicating the change in temperature ranges and the recommended action should be taken according to the level of priority are shown in Table. 1. This classification can be used for qualitative and for quantitative measurements. Quantitative measurements use the ambient temperature as the reference. The reference temperature has to be measured and a greater understanding of the variables influencing radiometric measurements.

It is important to be emphasized that the measurement errors resulting from inadequate spatial resolution of the used infrared camera depends on the magnitude of the error and the criticality of the target. For example a high resolution IR camera gives twice the delta-T (ΔT) temperature rise compared to a low resolution IR camera and 25% more than the medium resolution camera. These differences will only increase as the emissivity is lowered. Image processing techniques can be used to extract the thermal profiles within the electrical components for an automatic analysis the condition of electrical systems.

The common steps used in evaluating the thermal anomaly of electrical systems based on top-down approach includes: finding region of interest (ROI), identify the repeated structure, segmentation on process, relevant information, decision making for a result.

Three approaches can be used to determine the thermal severity of electrical systems:

- maximum temperature identification of each ROI for direct interpretation;

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- histogram distance evaluation for finding the similarity between two objects;
- gradient analysis of the segmented region.

TABLE 1. CLASSIFICATION OF THERMAL PROFILE OF ELECTRICAL SYSTEMS

ΔT over ambient temperature, (ºC)	ΔT similar equipment, (ºC)	Action required	Level of priority
> 40	> 15	Repair immediately - major discrepancy	**1**
21 – 40	–	Monitor until corrective measures can be accomplished	**2**
11 - 20	4 – 15	Repair as time permits - indicates probable deficiency	**3**
1 - 10	1 - 3	Warrants investigation - possible deficiency	**4**

Both bottoms-up and top-down approaches can be successfully implemented using various techniques for fault identification. The thermographic images of electrical equipment show a very high variation in appearance such as object distance from camera (scale change) and angle (view point change). It is important to use the most robust to this kind of changes approach for describing the IR image.

III. BASIC ELEMENTS OF THE INFRARED SURVEY PROCEDURE

Conceptual block diagram of an infrared system used in Electrical Preventive Maintenance is presented on Fig. 1. IR survey requires various factors to be considered during monitoring and a complex analysis of collected data. An automatically thermal monitoring and analysis system for the current state of electrical components is good to use machine learning approach. Advanced decision for the analysis block is the combination of image-processing and artifcial intelligence techniques.

The images of the surveyed electrical equipment are captured and then send to the monitoring system for calibration by using the input variables from additional sensors and further analysis. The electrical equipments recognition from the complex background is very difficult task. In conventional inspection of electrical equipment requires a large amount of certified and experienced personnel as well as cost and time. In order to assess whether potential troubles would happen and find position of suspected equipments infrared image processing must be applied.

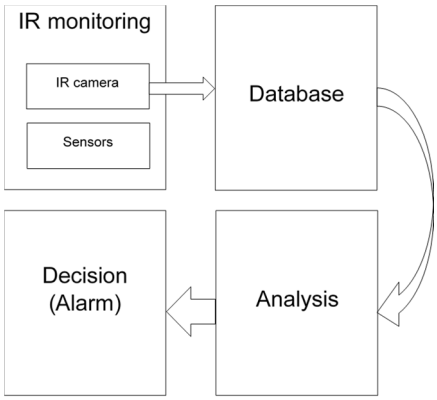

Fig.1. Block diagram of an IR thermal monitoring system

The captured infrared images should be filtered and enhanced. Next have to be fulfilled several steps: image preprocessing, feature extraction, type recognition, state analysis and classification. Infrared image processing can be divided in two categories - preprocessing and real processing. The preprocessing aim is to improve image quality and real processing is to find the ROI. The most frequently used approach for ROI determination is the segmentation. Located image features then used as inputs of neural network (ANN) that has been trained. In this step the relation to various operating parameters must be accomplished. A neural network can be applied for fault models. The general structure of the analyzing process as is shown in the Fig. 2.

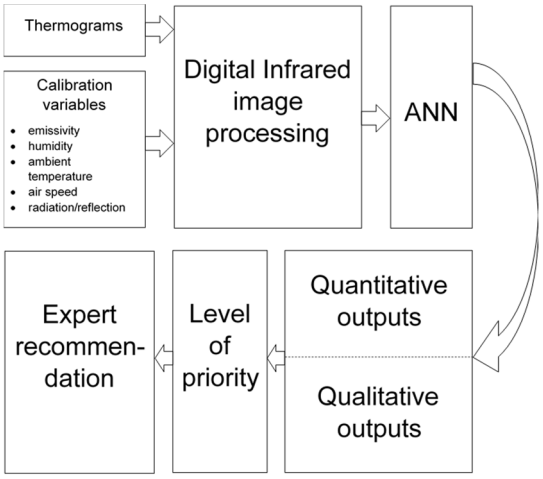

Fig.2. Base structure of data analyzing process

The accurate determination of the current temperature of the monitored electrical equipment depends on two categories factors: external (environmental factors) and internal (emissivity of the components and thermal gradient). Prior to analysis, all data for these factors have to be collected by set of sensors. The output of the automated IR systems will be given according to qualitative and quantitative analysis. The level of priority of the suspected electrical equipments can be classified according to Table 1 and respective actions will be recommended.

IV. EXPERIMENTAL RESULTS

More significant typical applications of IR preventive diagnostics in electrical equipment for instrumentation control and automation (IC&A) in thermal power plant "Bobov Dol" EAD that have substantially reduces costs and emergency stays are:

- Detection of "bad" contacts in various connection points;
- Localization of hidden defects in cable channels;
- Inspection of fuses and circuit breakers;
- Monitoring of low and medium voltage devices;
- Opening of unilateral load or misbalance in the distribution of energy;
- Verification of transformers and small components;
- Detection of increased electrical loads.

Some of the results on significant IC&A systems, which are responsible for trouble-free and safe operation of equipment in the plant, are presented. These are terminals, circuit breakers, contactors, relays, circuit boards, fuses, cable channels, transformers, electrical loads (motors), inverters, systems of protection and others.

A. Thermograms of terminal blocks and check the electrical connections

Fig. 3 and Fig. 4 present optical and infrared images from the diagnosis of terminal blocks.

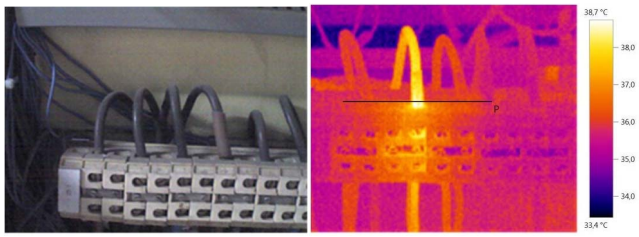

Fig.3. Presence of loosened bolting leading to a rise in temperature of one of the conductors

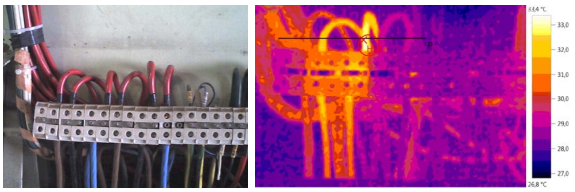

Fig.4. Temperature increase of several conductors due to unilateral load or misbalance in the distribution of energy

B. Thermograms of circuit breakers, contactors and relays

Fig. 5 shows pictures of the circuit breaker in the power supply of automation panel in IC&A system. Fig. 6 shows images of contactors and relays in automation panel in IC&A system.

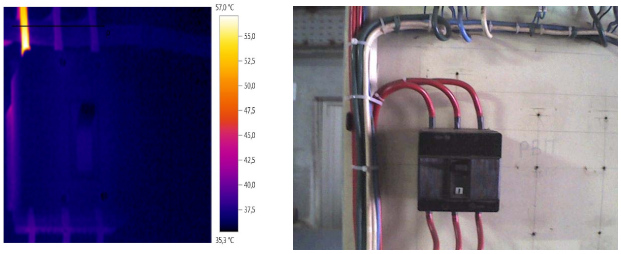

Fig.5. Presence of oxidation of terminal

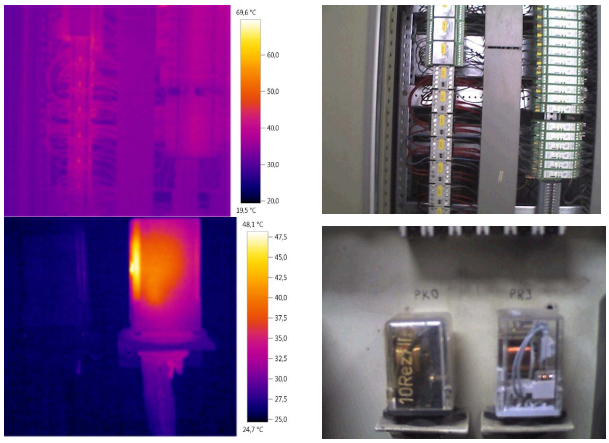

Fig.6. Results from preventive diagnosis of contactors and relays

C. Thermograms of fuses

Fig. 7 shows pictures of fuses in panel for lighting.

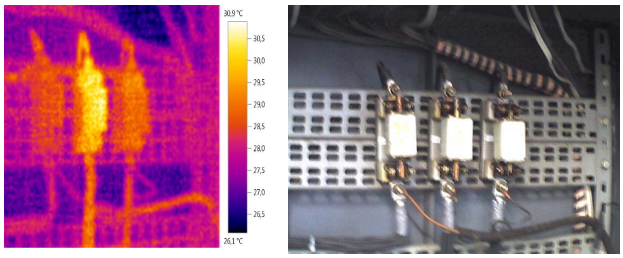

Fig.7. There is an increase in temperature of one of the fuses due to unilateral load or misbalance in the distribution

D. Thermograms of transformers and rectifiers

Fig. 8 shows pictures from diagnosis of transformers and rectifiers in the signaling panel. (above) and transformer and rectifier elements in the automation cabinet (below).

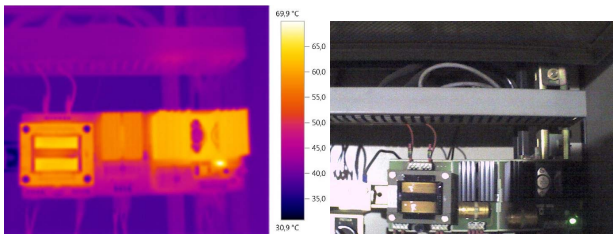

Fig.8. Presence of loosened bolting leading to a rise in temperature of one of the conductors

Fig. 9 shows pictures from diagnosis transformer and rectifier elements in the automation cabinet.

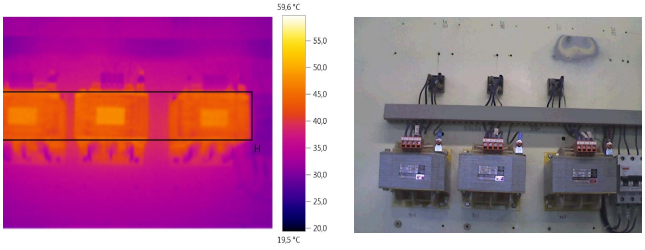

Fig.9. Presence of loosened bolting leading to a rise in temperature of one of the conductors

E. Thermograms of PCB and low voltage electronics

Fig. 10 shows pictures of power bus bars of voltage inverter (above) and input circuit boards for low signal levels with built-in multiplexer, part of the management system of energy block (below).

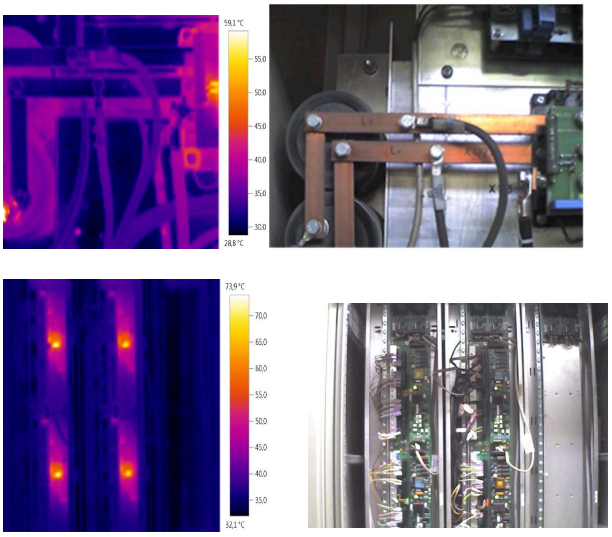

Fig.10. Presence of loosened bolting leading to a rise in temperature of one of the conductors

IV. CONCLUSION

Enhancing and preserving system reliability and reducing maintenance costs are top priorities for electric utilities today. The infrared inspections of electrical systems are beneficial to reduce the number of costly and catastrophic equipment failures and unscheduled plant shutdowns leading to the improvement of system efficiency and power quality. Using cost-effective electrical preventive maintenance infrared survey, strongly depend on the specific features of the inspection of electrical equipment and targets. These factors are important when choosing a procedure of investigation and relevant economically justified program. An automatic infrared thermal diagnosis system in Electrical Preventive Maintenance can provide more accurate and faster analysis. Important part in a predictive and preventive maintenance program is the presence of a classification procedure.

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