Analog Engineer's

Circuit Cookbook: Op Amps

TEXAS INSTRUMENTS

Analog Engineer's Circuit Cookbook: Op Amps

Edited by:

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Analog Engineer's
Circuit Cookbook: Op Amps
(First Edition)

Message from the editors:

The *Analog Engineer's Circuit Cookbook*: *Op Amps* provides operational amplifier (op amp) sub-circuit ideas that can be quickly adapted to meet your specific system needs. Each circuit is presented as a "definition-by-example." They include step-by-step instructions, like a recipe, with formulas enabling you to adapt the circuit to meet your design goals. Additionally, all circuits are verified with SPICE simulations.

We've provided at least one recommended op amp for each circuit, but you can swap it with another device if you've found one that's a better fit for your design. You can search our large portfolio of op amps at ti.com/opamps.

Our circuits require a basic understanding of op amp concepts. If you're new to op amp design, we highly recommend completing our TI Precision Labs (TIPL) training series. TIPL includes courses on introductory topics, such as device architecture, as well as advanced, application-specific problem-solving, using both theory and practical knowledge. Check out our curriculum for op amps, ADCs and more at: ti.com/precisionlabs.

We hope you find this collection of op amp circuits helpful in developing your designs. Our goal is to regularly update the cookbook with valuable op-amp-circuit building blocks. You can check to see if your version is the latest at ti.com/circuitcookbooks. If you have input on any of the existing circuits or would like to request additional op amp cookbook circuits for the next edition please contact us at: opampcookbook@list.ti.com.

Additional resources to explore

TI Precision Labs
ti.com/precisionlabs
- On-demand courses and tutorials ranging from introductory to advanced concepts that focus on application-specific problem solving
- Hands-on labs and evaluation modules (EVM) available

  - TIPL Op Amps experimentation platform, ti.com/TIPL-amp-evm
  - TIPL SAR ADC experimentation platform, ti.com/TIPL-adc-evm

Analog Engineer's Pocket Reference
ti.com/analogrefguide
- PCB, analog and mixed-signal design formulae; includes conversions, tables and equations
- e-book, iTunes app and hardcopy available

***The Signal* e-book**
ti.com/signalbook
- Op amp e-book with short, bite-sized lessons on design topics such as offset voltage, input bias current, stability, noise and more

TI Designs
ti.com/tidesigns
- Ready-to-use reference designs with theory, calculations, simulations schematics, PCB files and bench test results

TINA-TI™ simulation software
ti.com/tool/tina-ti
- Complete SPICE simulator for DC, AC, transient and noise analysis
- Includes schematic entry and post-processor for waveform math

Analog Engineer's Calculator
ti.com/analogcalc
- ADC and amplifier design tools, noise and stability analysis, PCB and sensor tools

Analog Wire Blog
ti.com/analogwire
- Technical blogs written by analog experts that include tips, tricks and design techniques

TI E2E™ Community
ti.com/e2e
- Support forums for all TI products

Op Amp Parametric Quick Search
ti.com/opamp-search
- Search for precision, high-speed, general-purpose, ultra-low-power, audio and power op amps

Op Amp Parametric Cross-Reference
ti.com/opampcrossreference
- Find similar TI op amps using competitive part numbers

DIY Amplifier Circuit Evaluation Module (DIYAMP-EVM)
ti.com/DIYAMP-EVM
- Single-channel circuit evaluation module providing SC70, SOT23 and SOIC package options in 12 popular amplifier configurations

Dual-Channel DIY Amplifier Circuit Evaluation Module (DUAL-DIYAMP-EVM)
ti.com/dual-diyamp-evm
- Dual-channel circuit evaluation module in an SOIC-8 package with 10 popular amplifier configurations

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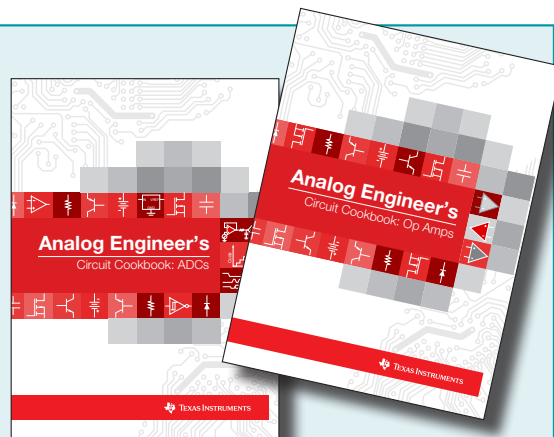
Buffer (Follower) Circuit

Design Goals

Input		Output		Freq.	Supply	
V_{iMin}	V_{iMax}	V_{oMin}	V_{oMax}	f	V_{cc}	V_{ee}
−10V	10V	−10V	10V	100kHz	15V	−15V

Design Description

This design is used to buffer signals by presenting a high input impedance and a low output impedance. This circuit is commonly used to drive low-impedance loads, analog-to-digital converters (ADC) and buffer reference voltages. The output voltage of this circuit is equal to the input voltage.

Design Notes

1. Use op amp linear output operating range, which is usually specified under the A_{OL} test conditions.
2. The small-signal bandwidth is determined by the unity-gain bandwidth of the amplifier.
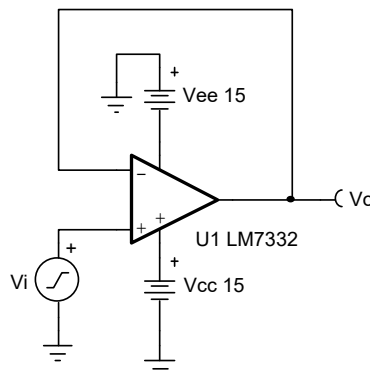3. Check the maximum output voltage swing versus frequency graph in the datasheet to minimize slew-induced distortion.
4. The common mode voltage is equal to the input signal.
5. Do not place capacitive loads directly on the output that are greater than the values recommended in the datasheet.
6. High output current amplifiers may be required if driving low impedance loads.
7. For more information on op amp linear operating region, stability, slew-induced distortion, capacitive load drive, driving ADCs, and bandwidth please see the *Design References* section.

Design Steps

The tranfer function for this circuit is given below.

$$V_o = V_i$$

1. Verify that the amplifier can acheive the desired output swing using the supply voltages provided. Use the output swing stated in the A_{OL} test conditions. The output swing range of the amplifier must be greater than the output swing required for the design.

   $$-14V \le V_o \le 14V$$

   - The output swing of the LM7332 using ±15-V supplies is greater than the required output swing of the design. Therefore, this requirement is met.
   - Review the Output Voltage versus Output Current curves in the product datasheet to verify the desired output voltage can be acheived for the desired output current.

2. Verify the input common mode voltage of the amplifier will not be violated using the supply voltage provided. The input common mode voltage range of the amplifier must be greater than the input signal voltage range.

   $$-15.1\ V \le V_{icm} \le 15.1\ V$$

   - The input common-mode range of the LM7332 using ±15-V supplies is greater than the required input common-mode range of the design. Therefore, this requirement is met.

3. Calculate the minimum slew rate required to minimize slew-induced distortion.

   $$SR > 2 \times \pi \times V_p \times f = 2 \times \pi \times 10V \times 100kHz = 6.28V/\mu s$$

   - The slew rate of the LM7332 is 15.2V/µs. Therefore, this requirement is met.

4. Verify the device will have sufficient bandwidth for the desired output signal frequency.

   $$f_{signal} < f_{unity}$$
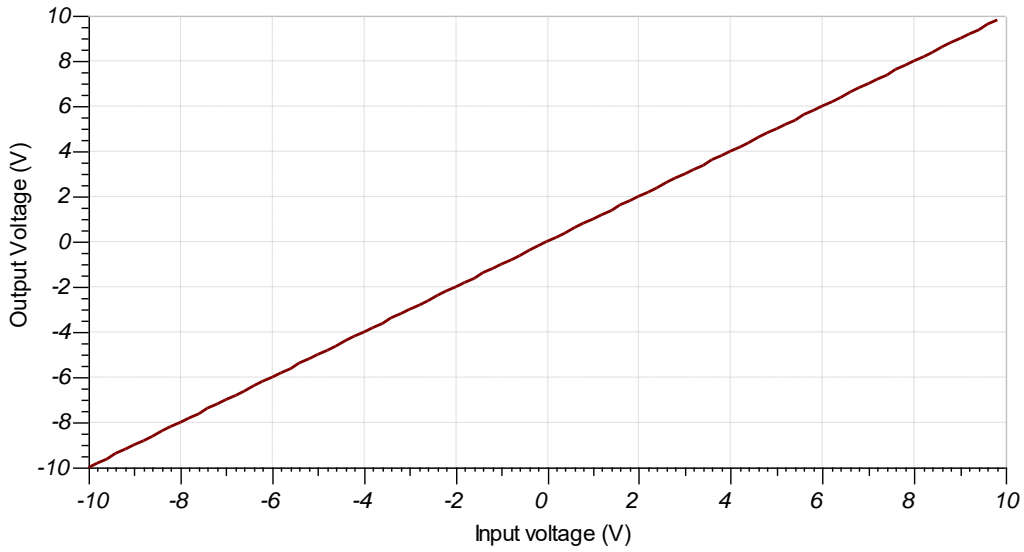 $$100kHz < 7.5MHz$$

   - The desired output signal frequency is less than the unity-gain bandwidth of the LM7332. Therefore, this requirement is met.

Design Simulations

DC Simulation Results

AC Simulation Results
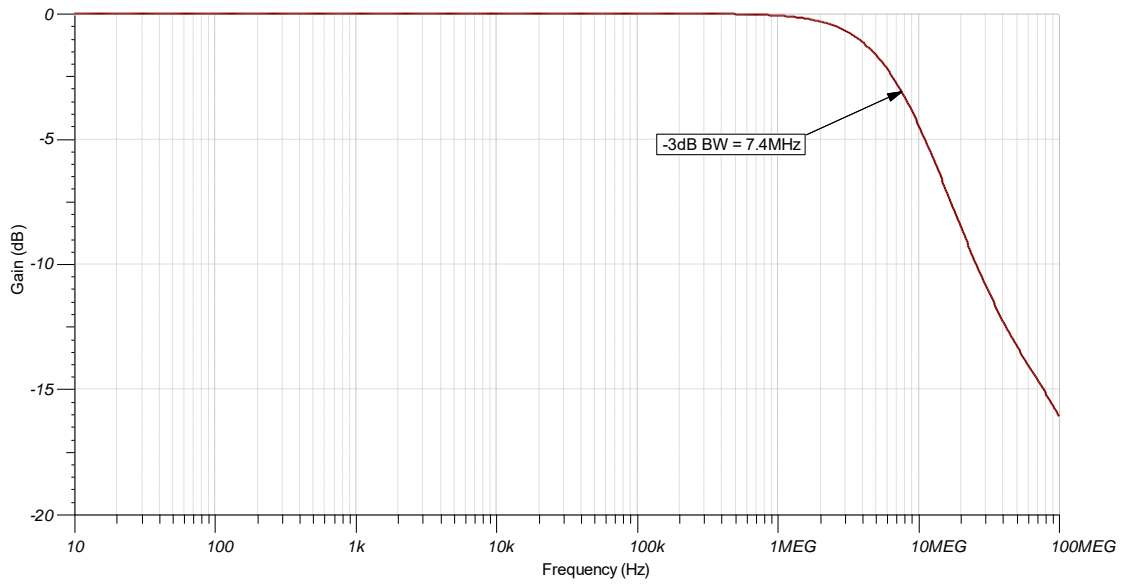
Design References

See TIPD128, www.ti.com/tool/tipd128

For more information on many op amp topics including common-mode range, output swing, bandwidth, slew rate, and how to drive an ADC please see TI Precision Labs.

Design Featured Op Amp

LM7332	
V_{ss}	2.5V to 32V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	1.6mV
I_q	2mA
I_b	1µA
UGBW	7.5MHz (±5-V supply)
SR	15.2V/µs
#Channels	2
www.ti.com/product/LM7332	

Design Alternate Op Amp

OPA192	
V_{ss}	4.5V to 36V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	5µV
I_q	1mA
I_b	5pA
UGBW	10MHz
SR	20V/µs
#Channels	1, 2, 4
www.ti.com/product/opa192	

Inverting Amplifier Circuit

Design Goals

Input		Output		Freq.	Supply	
V_{iMin}	V_{iMax}	V_{oMin}	V_{oMax}	f	V_{cc}	V_{ee}
–7V	7V	–14V	14V	3kHz	15V	–15V

Design Description

This design inverts the input signal, V_i, and applies a signal gain of –2V/V. The input signal typically comes from a low-impedance source because the input impedance of this circuit is determined by the input resistor, R_1. The common-mode voltage of an inverting amplifier is equal to the voltage connected to the non-inverting node, which is ground in this design.
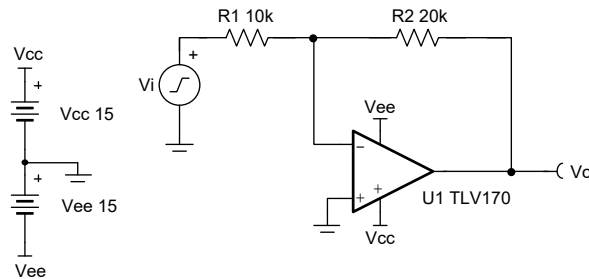
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Design Notes

1. Use the op amp in a linear operating region. Linear output swing is usually specified under the A_{OL} test conditions. The common-mode voltage in this circuit does not vary with input voltage.

2. The input impedance is determined by the input resistor. Make sure this value is large when compared to the source's output impedance.

3. Using high value resistors can degrade the phase margin of the circuit and introduce additional noise in the circuit.

4. Avoid placing capacitive loads directly on the output of the amplifier to minimize stability issues.

5. Small-signal bandwidth is determined by the noise gain (or non-inverting gain) and op amp gain-bandwidth product (GBP). Additional filtering can be accomplished by adding a capacitor in parallel to R_2. Adding a capacitor in parallel with R_2 will also improve stability of the circuit if high value resistors are used.

6. Large signal performance may be limited by slew rate. Therefore, check the maximum output swing versus frequency plot in the data sheet to minimize slew-induced distortion.

7. For more information on op amp linear operating region, stability, slew-induced distortion, capacitive load drive, driving ADCs, and bandwidth please see the Design References section.

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Design Steps

The transfer function of this circuit is given below.

$$V_O = V_i \times \left(-\frac{R_2}{R_1} \right)$$

1. Determine the starting value of R_1. The relative size of R_1 to the signal source's impedance affects the gain error. Assuming the signal source's impedance is low (for example, 100Ω), set $R_1 = 10k\Omega$ for 1% gain error.

    $R_1 = 10k\Omega$

2. Calculate the gain required for the circuit. Since this is an inverting amplifier use V_{iMin} and V_{oMax} for the calculation.

    $$G = \frac{V_{oMax}}{V_{iMin}} = \frac{14V}{-7V} = -2\frac{V}{V}$$

3. Calculate R_2 for a desired signal gain of $-2V/V$.

    $$G = -\frac{R_2}{R_1} \rightarrow R_2 = -G \times R_1 = -\left(-2\frac{V}{V} \right) \times 10k\Omega = 20k\Omega$$

4. Calculate the small signal circuit bandwidth to ensure it meets the 3kHz requirement. Be sure to use the noise gain, or non-inverting gain, of the circuit.

    $$GBP_{TLV170} = 1.2MHz$$
    $$NG = \left(1 + \frac{R_2}{R_1} \right) = 3\frac{V}{V}$$
    $$BW = \frac{GBP}{NG} = \frac{1.2MHz}{3V/V} = 400kHz$$

5. Calculate the minimum slew rate required to minimize slew-induced distortion.

    $$V_p = \frac{SR}{2 \times \pi \times f} \rightarrow SR > 2 \times \pi \times f \times V_p$$
    $$SR > 2 \times \pi \times 3kHz \times 14V = 263.89\frac{kV}{s} = 0.26\frac{V}{\mu s}$$

    - $SR_{TLV170} = 0.4V/\mu s$, therefore it meets this requirement.

6. To avoid stability issues ensure that the zero created by the gain setting resistors and input capacitance of the device is greater than the bandwidth of the circuit.

    $$\frac{1}{2 \times \pi \times (C_{cm} + C_{diff}) \times (R_2 \| R_1)} > \frac{GBP}{NG}$$
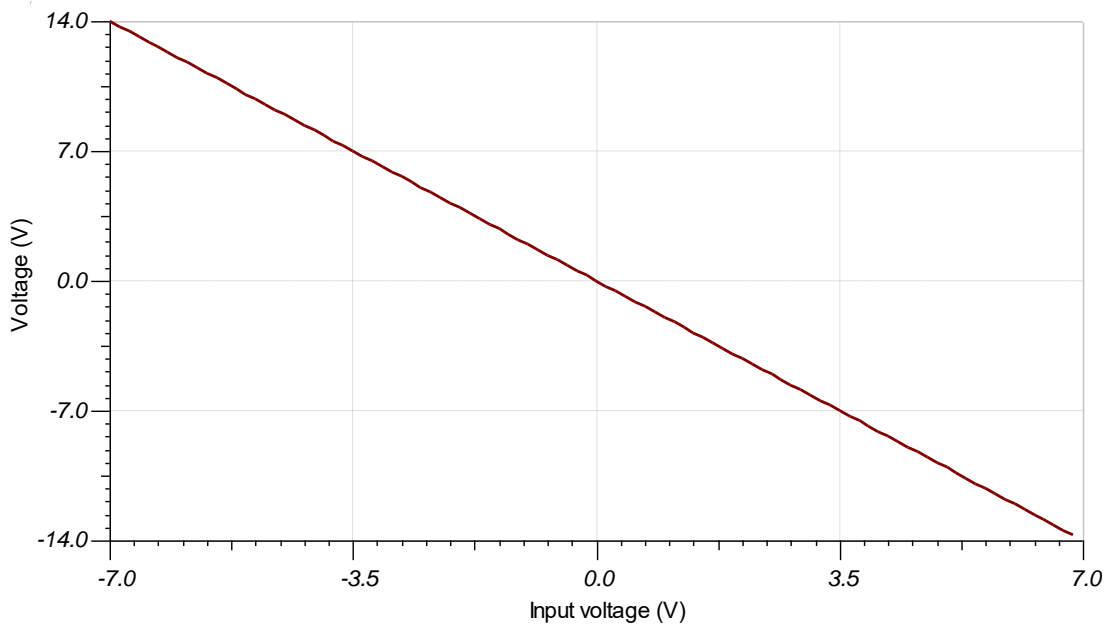 $$\frac{1}{2 \times \pi \times (3pF + 3pF) \times \frac{20k\Omega \times 10k\Omega}{20k\Omega + 10k\Omega}} > \frac{1.2MHz}{3V/V}$$
    $$43.77MHz > 400kHz$$

    - C_{cm} and C_{diff} are the common-mode and differential input capacitances of the TLV170, respectively.
    - Since the zero frequency is greater than the bandwidth of the circuit, this requirement is met.

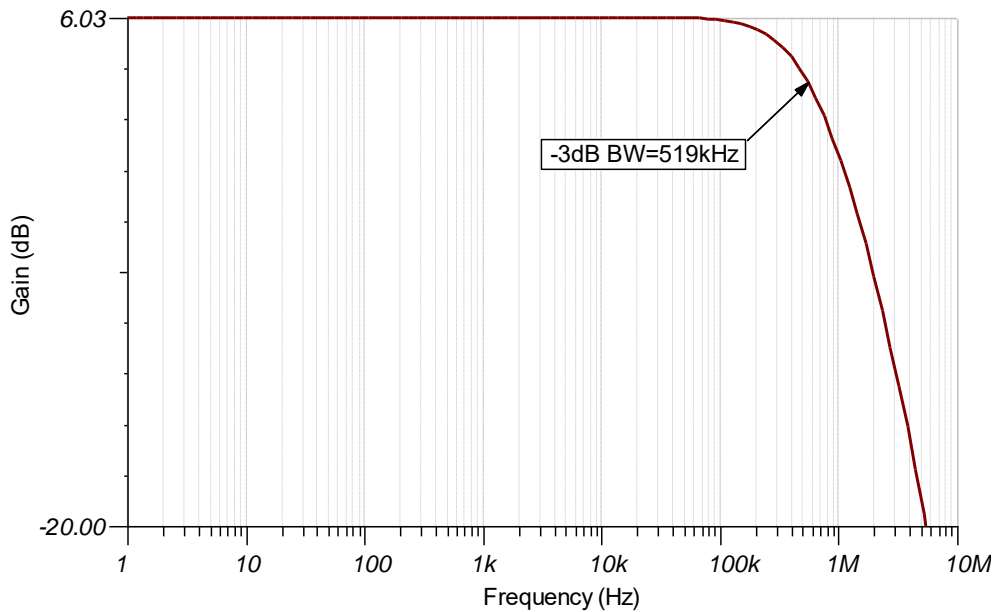*Inverting Amplifier Circuit*

Design Simulations

**DC Simulation Results**

AC Simulation Results

The bandwidth of the circuit depends on the noise gain, which is 3V/V. The bandwidth is determined by looking at the –3dB point, which is located at 3dB given a signal gain of 6dB. The simulation sufficiently correlates with the calculated value of 400kHz.

Transient Simulation Results

The output is double the magnitude of the input, and inverted.
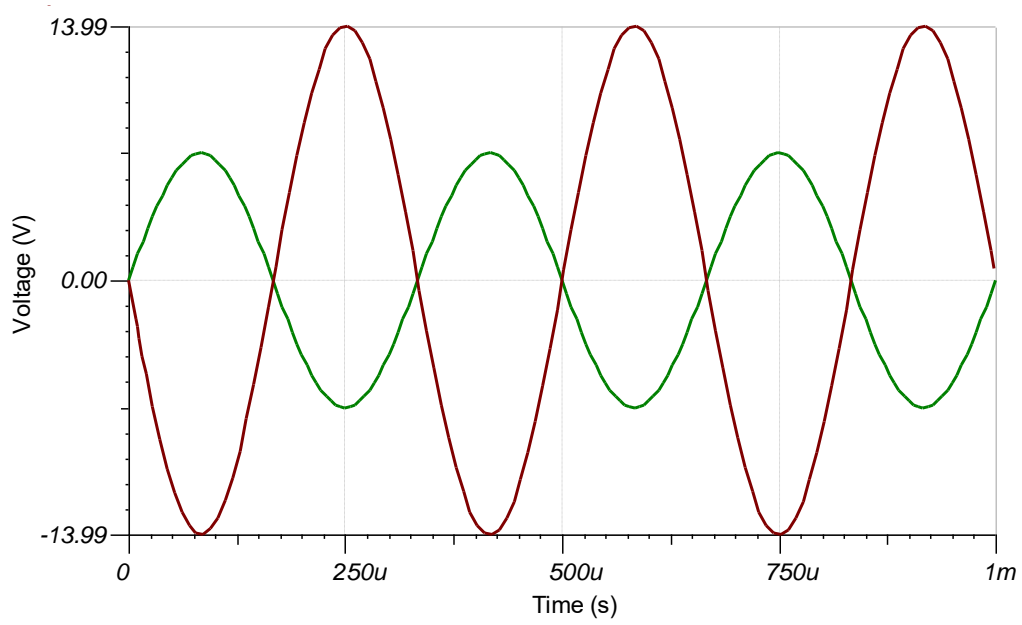
Design References

For more information on many op amp topics including common-mode range, output swing, bandwidth, and how to drive an ADC please visit TI Precision Labs.

Design Featured Op Amp

TLV170	
V_{ss}	±18V (36V)
V_{inCM}	(Vee-0.1V) to (Vcc-2V)
V_{out}	Rail-to-rail
V_{os}	0.5mV
I_q	125µA
I_b	10pA
UGBW	1.2MHz
SR	0.4V/µs
#Channels	1, 2, 4
www.ti.com/product/tlv170	

Design Alternate Op Amp

LMV358	
V_{ss}	2.7 to 5.5V
V_{inCM}	(V_{ee}–0.2V) to (V_{cc}–0.8V)
V_{out}	Rail-to-rail
V_{os}	1.7mV
I_q	210µA
I_b	15nA
UGBW	1MHz
SR	1V/µs
#Channels	1 (LMV321), 2 (LMV358), 4 (LMV324)
www.ti.com/product/lmv358	

Non-Inverting Amplifier Circuit

Design Goals

Input		Output		Supply	
ViMin	ViMax	VoMin	VoMax	Vcc	Vee
−1V	1V	−10V	10	15V	−15V

Design Description

This design amplifies the input signal, V_i, with a signal gain of 10V/V. The input signal may come from a high-impedance source (for example, MΩ) because the input impedance of this circuit is determined by the extremely high input impedance of the op amp (for example, GΩ). The common-mode voltage of a non-inverting amplifier is equal to the input signal.
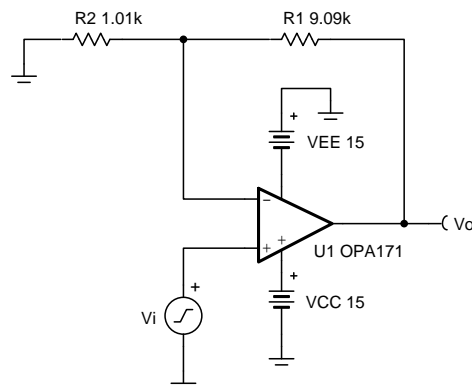
Design Notes

1. Use the op amp linear output operating range, which is usually specified under the A_{OL} test conditions. The common-mode voltage is equal to the input signal.

2. The input impedance of this circuit is equal to the input impedance of the amplifier.

3. Using high-value resistors can degrade the phase margin of the circuit and introduce additional noise in the circuit.

4. Avoid placing capacitive loads directly on the output of the amplifier to minimize stability issues.

5. The small-signal bandwidth of a non-inverting amplifier depends on the gain of the circuit and the gain bandwidth product (GBP) of the amplifier. Additional filtering can be accomplished by adding a capacitor in parallel to R_1. Adding a capacitor in parallel with R_1 will also improve stability of the circuit if high-value resistors are used.

6. Large signal performance may be limited by slew rate. Therefore, check the maximum output swing versus frequency plot in the data sheet to minimize slew-induced distortion.

7. For more information on op amp linear operating region, stability, slew-induced distortion, capacitive load drive, driving ADCs, and bandwidth please see the *Design References* section.

Design Steps

The transfer function for this circuit is given below.

$$V_o = V_i \times \left(1 + \frac{R_1}{R_2}\right)$$

1. Calculate the gain.

$$G = \frac{V_{o\_max} - V_{o\_min}}{V_{i\_max} - V_{i\_min}}$$

$$G = \frac{10V - (-10V)}{1\,V - (-1\,V)} = 10V\,/\,V$$

2. Calculate values for R_1 and R_2.

$$G = 1 + \frac{R_1}{R_2}$$

Choose $R_1 = 9.09k\Omega$

$$R_2 = \frac{R_1}{G-1} = \frac{9.09k\Omega}{(10V/V)-1} = 1.01k\Omega$$

3. Calculate the minimum slew rate required to minimize slew-induced distortion.

$$SR > 2 \times \pi \times V_p \times f = 2 \times \pi \times 10V \times 20kHz = 1.257V\,/\,\mu s$$

   • The slew rate of the OPA171 is 1.5V/µs, therefore it meets this requirement.

4. To maintain sufficient phase margin, ensure that the zero created by the gain setting resistors and input capacitance of the device is greater than the bandwidth of the circuit.

$$\frac{1}{2 \times \pi \times (C_{cm} + C_{diff}) \times (R_1 \| R_2)} > \frac{GBP}{G}$$
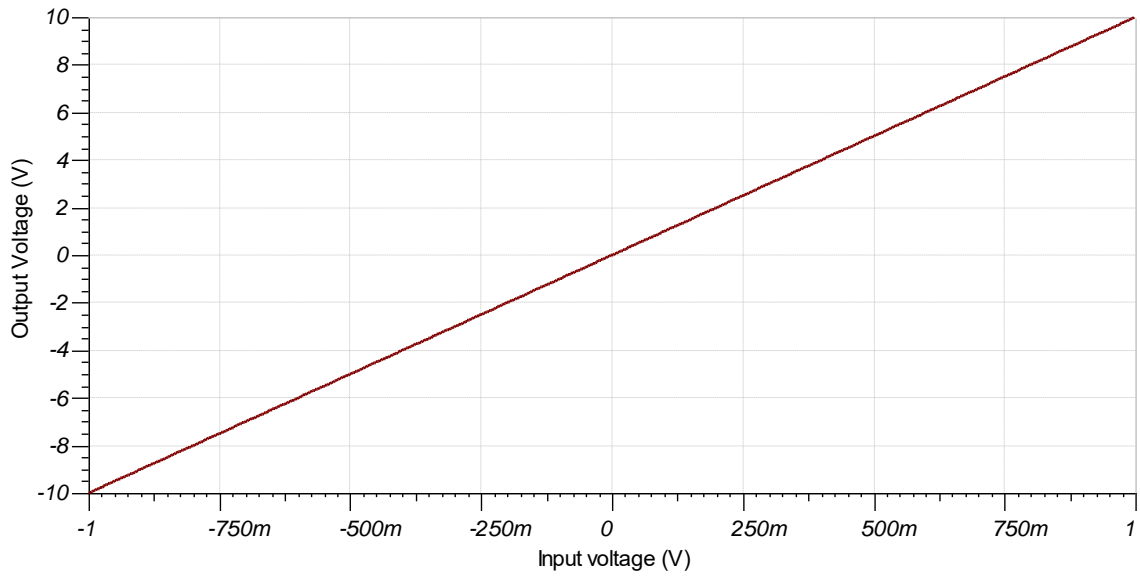
$$\frac{1}{2 \times \pi \times (3pF + 3pF) \times \frac{1.01k\Omega \times 9.09k\Omega}{1.01k\Omega + 9.09k\Omega}} > \frac{3MHz}{10V/V}$$
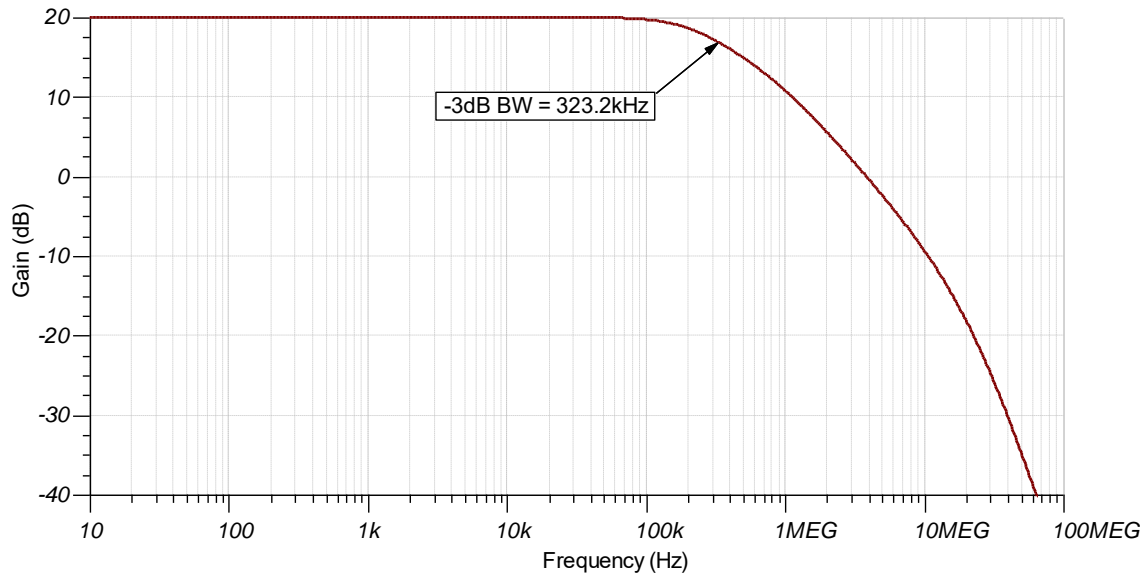
$$29.18MHz > 300kHz$$

   • C_{cm} and C_{diff} are the common-mode and differential input capacitances of the OPA171, respectively.
   • Since the zero frequency is greater than the bandwidth of the circuit, this requirement is met.

Design Simulations

DC Simulation Results

AC Simulation Results

-3dB BW = 323.2kHz

Design References

For more information on many op amp topics including common-mode range, output swing, and bandwidth please visit TI Precision Labs.

Design Featured Op Amp

OPA171	
V_{ss}	2.7V to 36V
V_{inCM}	$(V_{ee}-0.1V)$ to $(V_{cc}-2V)$
V_{out}	Rail-to-rail
V_{os}	250µV
I_q	475µA
I_b	8pA
UGBW	3MHz
SR	1.5V/µs
#Channels	1, 2, 4
www.ti.com/product/opa171	

Design Alternate Op Amp

OPA191	
V_{ss}	4.5V to 36V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	5µV
I_q	140µA
I_b	5pA
UGBW	2.5MHz
SR	7.5V/µs
#Channels	1, 2, 4
www.ti.com/product/OPA191	

Inverting Summer Circuit

Design Goals

Input 1		Input 2		Output		Freq.	Supply	
V_{i1Min}	V_{i1Max}	V_{i2Min}	V_{i2Max}	V_{oMin}	V_{oMax}	f	V_{cc}	V_{ee}
−5V	5V	−250mV	250mV	−4.9V	4.9V	10kHz	5V	−5V

Design Description

This design sums (adds) and inverts two input signals, V_{i1} and V_{i2}. The input signals typically come from low-impedance sources because the input impedance of this circuit is determined by the input resistors, R_1 and R_2. The common-mode voltage of an inverting amplifier is equal to the voltage connected to the non-inverting node, which is ground in this design.
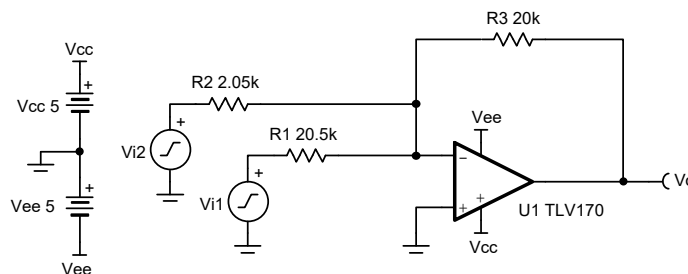
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Design Notes

1. Use the op amp in a linear operating region. Linear output swing is usually specified under the A_{OL} test conditions. The common-mode voltage in this circuit does not vary with input voltage.
2. The input impedance is determined by the input resistors. Make sure these values are large when compared to the output impedance of the source.
3. Using high-value resistors can degrade the phase margin of the circuit and introduce additional noise in the circuit.
4. Avoid placing capacitive loads directly on the output of the amplifier to minimize stability issues.
5. Small-signal bandwidth is determined by the noise gain (or non-inverting gain) and op amp gain-bandwidth product (GBP). Additional filtering can be accomplished by adding a capacitor in parallel to R_3. Adding a capacitor in parallel with R_3 will also improve stability of the circuit if high-value resistors are used.
6. Large signal performance may be limited by slew rate. Therefore, check the maximum output swing versus frequency plot in the data sheet to minimize slew-induced distortion.
7. For more information on op amp linear operating region, stability, slew-induced distortion, capacitive load drive, driving ADCs, and bandwidth please see the *Design References* section.

Design Steps

The transfer function for this circuit is given below.

$$V_o = V_{i\,1} \times \left(-\frac{R_3}{R_1}\right) + V_{i\,2} \times \left(-\frac{R_3}{R_2}\right)$$

1. Select a reasonable resistance value for R_3.
   $R_3 = 20k\Omega$

2. Calculate gain required for V_{i1}. For this design, half of the output swing is devoted to each input.

$$|G_{Vi1}| = \left|\frac{\frac{V_{oMax} - V_{oMin}}{2}}{V_{i\,1\,Max} - V_{i\,1\,Min}}\right| = \left|\frac{\frac{4.9V - (-4.9V)}{2}}{2.5V - (-2.5V)}\right| = 0.98\frac{V}{V} = -0.175dB$$

3. Calculate the value of R_1.

$$|G_{Vi1}| = \frac{R_3}{R_1} \rightarrow R_1 = \frac{R_3}{|G_{Vi1}|} = \frac{20k\Omega}{0.98V/V} = 20.4k\Omega \approx 20.5k\Omega \text{ (Standard Value)}$$

4. Calculate gain required for V_{i2}. For this design, half of the output swing is devoted to each input.

$$|G_{Vi2}| = \left|\frac{\frac{V_{oMax} - V_{oMin}}{2}}{V_{i\,2\,Max} - V_{i\,2\,Min}}\right| = \left|\frac{\frac{4.9V - (-4.9V)}{2}}{250mV - (-250mV)}\right| = 9.8\frac{V}{V} = 19.82dB$$

5. Calculate the value of R_2.

$$|G_{Vi2}| = \frac{R_3}{R_2} \rightarrow R_2 = \frac{R_3}{|G_{Vi2}|} = \frac{20k\Omega}{9.8V/V} = 2.04k\Omega \approx 2.05k\Omega \text{ (Standard Value)}$$

6. Calculate the small signal circuit bandwidth to ensure it meets the 10-kHz requirement. Be sure to use the noise gain (NG), or non-inverting gain, of the circuit. When calculating the noise gain note that R_1 and R_2 are in parallel.

$$GBP_{OPA170} = 1.2MHz$$

$$NG = \left(1 + \frac{R_3}{R_1 \| R_2}\right) = \left(1 + \frac{20k\Omega}{1.86k\Omega}\right) = 11.75\frac{V}{V} = 21.4dB$$

$$BW = \frac{GBP}{NG} = \frac{1.2MHz}{11.75V/V} = 102kHz$$

   • This requirement is met because the closed-loop bandwidth is 102kHz and the design goal is 10kHz.

7. Calculate the minmum slew rate to minimize slew-induced distortion.

$$V_p = \frac{SR}{2 \times \pi \times f} \rightarrow SR > 2 \times \pi \times f \times V_p$$

$$SR > 2 \times \pi \times 10kHz \times 4.9V = 307.87\frac{kV}{s} = 0.31\frac{V}{\mu s}$$

   • $SR_{OPA170}=0.4V/\mu s$, therefore it meets this requirement.

8. To avoid stability issues ensure that the zero created by the gain setting resistors and input capacitance of the device is greater than the bandwidth of the circuit.

$$\frac{1}{2 \times \pi \times (C_{cm} + C_{diff}) \times (R_1 \| R_2 \| R_3)} > \frac{GBP}{NG}$$

$$\frac{1}{2 \times \pi \times (3pF + 3pF) \times 1.7k\Omega} > \frac{1.2MHz}{11.75V/V}$$

$$15.6MHz > 102kHz$$

   • C_{cm} and C_{diff} are the common-mode and differential input capacitances.
   • Since the zero frequency is greater than the bandwidth of the circuit, this requirement is met.
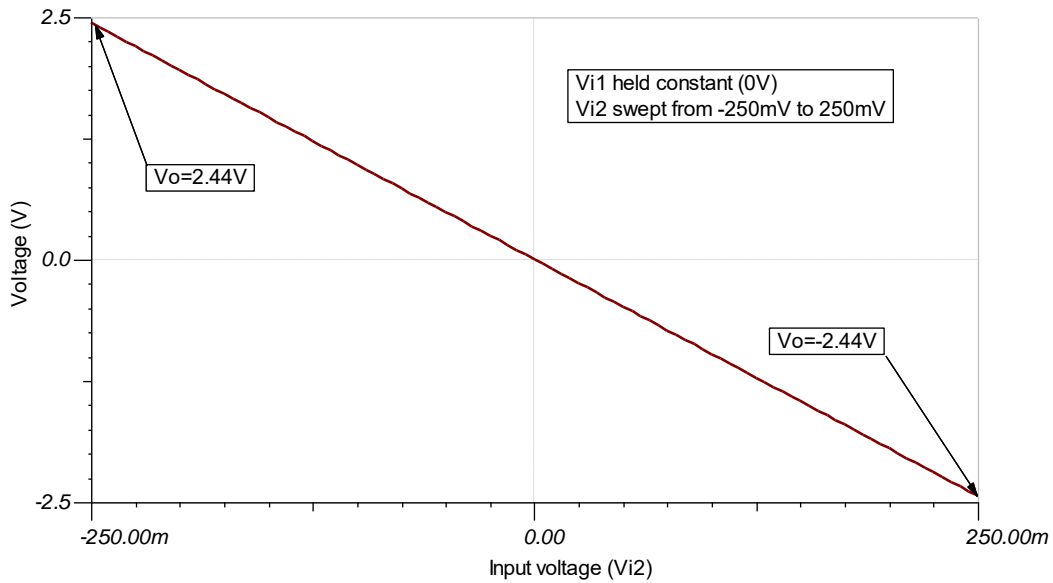
Design Simulations

DC Simulation Results

This simulation sweeps V_{i1} from –2.5V to 2.5V while V_{i2} is held constant at 0V. The output is inverted and ranges from –2.44V to 2.44V.
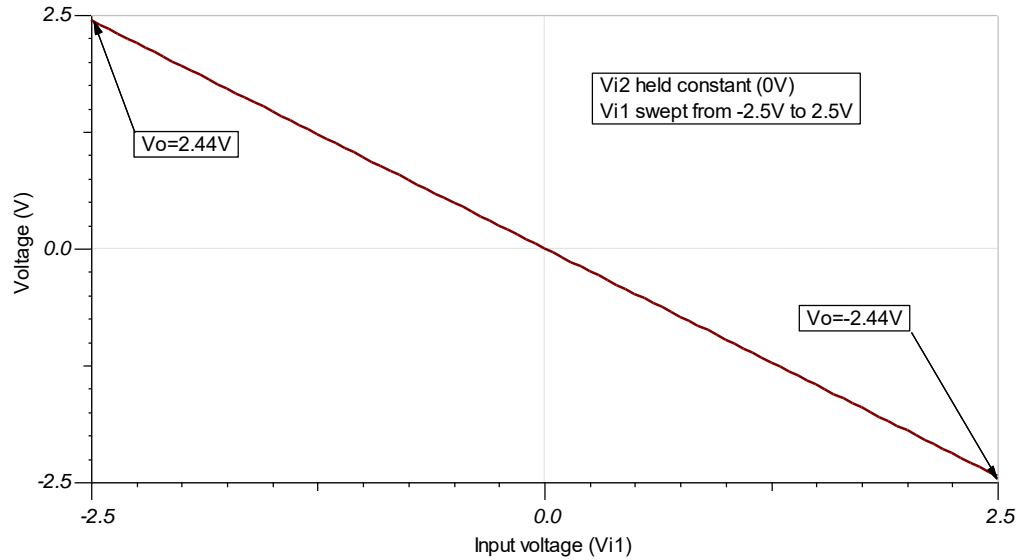
This simulation sweeps V_{i2} from –250mV to 250mV while V_{i1} is held constant at 0V. The output is inverted and ranges from –2.44V to 2.44V.

AC Simulation Results

This simulation shows the bandwidth of the circuit. Note that the bandwidth is the same for either input. This is because the bandwidth depends on the noise gain of the circuit, not the signal gain of each input. These results correlate well with the calculations.
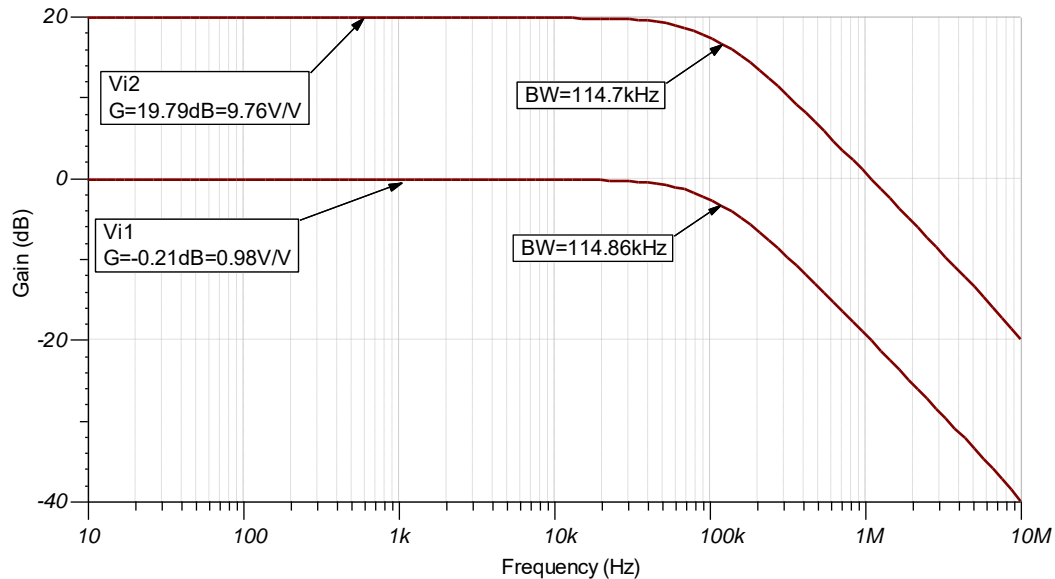
Transient Simulation Results

This simulation shows the inversion and summing of the two input signals. V_{i1} is a 1-kHz, 5-V_{pp} sine wave and V_{i2} is a 10-kHz, 500-mV_{pp} sine wave. Since both inputs are properly amplified or attenuated, the output is within specification.
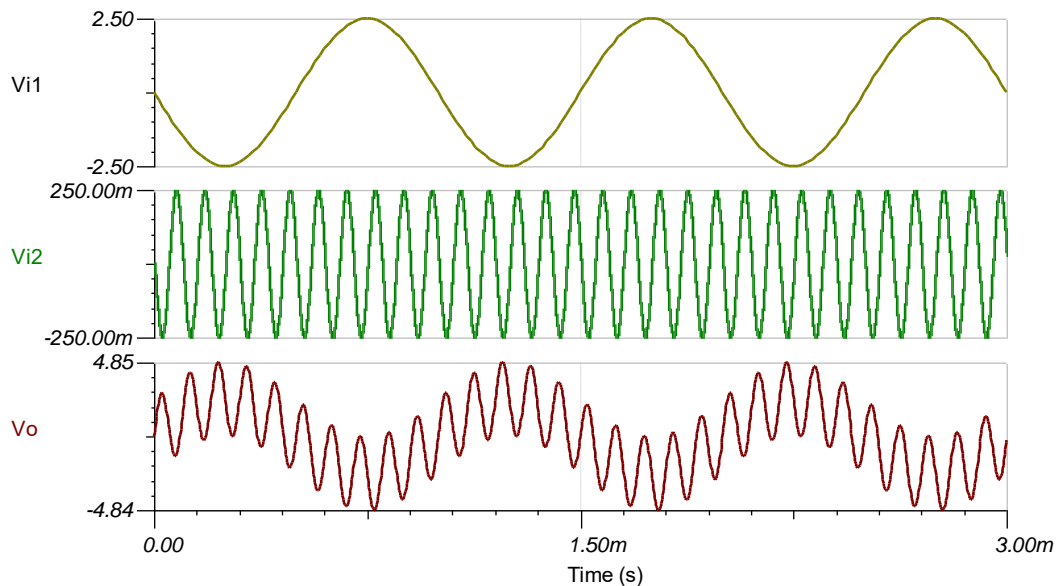
Design References

For more information on many op amp topics including common-mode range, output swing, bandwidth, and how to drive an ADC please visit TI Precision Labs.

Design Featured Op Amp

OPA170	
V_{ss}	2.7V to 36V
V_{inCM}	(Vee-0.1V) to (Vcc-2V)
V_{out}	Rail-to-rail
V_{os}	0.25mV
I_q	110µA
I_b	8pA
UGBW	1.2MHz
SR	0.4V/µs
#Channels	1, 2, 4
www.ti.com/product/opa170	

Design Alternate Op Amp

LMC7101	
V_{ss}	2.7V to 15.5V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	110µV
I_q	0.8mA
I_b	1pA
UGBW	1.1MHz
SR	1.1V/µs
#Channels	1
www.ti.com/product/lmc7101	

Difference Amplifier (Subtractor) Circuit

Design Goals

Input (V_{i2}-V_{i1})		Output		CMRR (min)	Supply		
$V_{idiffMin}$	$V_{idiffMax}$	V_{oMin}	V_{oMax}	dB	V_{cc}	V_{ee}	V_{ref}
−1.25V	1.25V	−2.5V	2.5V	50	2.75V	−2.75V	0V

Design Description

This design inputs two signals, V_{i1} and V_{i2}, and outputs their difference (subtracts). The input signals typically come from low-impedance sources because the input impedance of this circuit is determined by the resistive network. Difference amplifiers are typically used to amplify differential input signals and reject common-mode voltages. A common-mode voltage is the voltage common to both inputs. The effectiveness of the ability of a difference amplifier to reject a common-mode signal is known as common-mode rejection ratio (CMRR). The CMRR of a difference amplifier is dominated by the tolerance of the resistors.
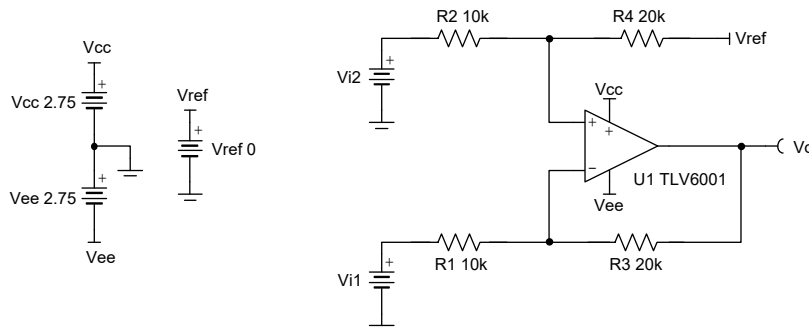
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Design Notes

1. Use the op amp in a linear operating region. Ensure that the inputs of the op amp do not exceed the common-mode range of the device. Linear output swing is usually specified under the A_{OL} test conditions.
2. The input impedance is determined by the input resistive network. Make sure these values are large when compared to the output impedance of the sources.
3. Using high-value resistors can degrade the phase margin of the circuit and introduce additional noise in the circuit.
4. Avoid placing capacitive loads directly on the output of the amplifier to minimize stability issues.
5. Small-signal bandwidth is determined by the noise gain (or non-inverting gain) and op amp gain-bandwidth product (GBP). Additional filtering can be accomplished by adding a capacitors in parallel to R_3 and R_4. Adding capacitors in parallel with R_3 and R_4 will also improve stability of the circuit if high-value resistors are used.
6. Large signal performance may be limited by slew rate. Therefore, check the maximum output swing versus frequency plot in the data sheet to minimize slew-induced distortion.
7. For more information on op amp linear operating region, stability, slew-induced distortion, capacitive load drive, driving ADCs, and bandwidth please see the *Design References* section.

Design Steps

The complete transfer function for this circuit is shown below.

$$V_O = V_{i1} \times \left(-\frac{R_3}{R_1}\right) + V_{i2} \times \left(\frac{R_4}{R_2+R_4}\right) \times \left(1 + \frac{R_3}{R_1}\right) + Vref \times \left(\frac{R_2}{R_2+R_4}\right) \times \left(1 + \frac{R_3}{R_1}\right)$$

If $R_1 = R_2$ and $R_3 = R_4$ the transfer function for this circuit simplifies to the following equation.

$$V_O = (V_{i2} - V_{i1}) \times \frac{R_3}{R_1} + Vref$$

- Where the gain, G, is R_3/R_1.

1. Determine the starting value of R_1 and R_2. The relative size of R_1 and R_2 to the signal impedance of the source affects the gain error.

   $$R_1 = R_2 = 10k\Omega$$

2. Calculate the gain required for the circuit.

   $$G = \frac{V_{oMax} - V_{oMin}}{V_{idiffMax} - V_{idiffMin}} = \frac{2.5V - (-2.5V)}{1.25V - (-1.25V)} = 2\frac{V}{V} = 6.02dB$$

3. Calculate the values for R_3 and R_4.

   $$G = 2\frac{V}{V} = \frac{R_3}{R_1} \rightarrow 2 \times R_1 = R_3 = R_4 = 20k\Omega$$

4. Calculate resistor tolerance to meet the minimum common-mode rejection ratio (CMRR). For minimum (worst-case) CMRR, $\alpha = 4$. For a more probable, or typical value of CMRR, $\alpha = 0.33$.

   $$CMRR_{dB} \cong 20log10\left(\frac{1+G}{\alpha \times \varepsilon}\right)$$

   $$\varepsilon = \frac{1+G}{\alpha \times 10^{\left(\frac{CMRR_{dB}}{20}\right)}} = \frac{3}{4 \times 10^{\left(\frac{50}{20}\right)}} = 0.024 = 0.24\% \rightarrow Use \ 0.1 \ \% \ resistors$$

5. For quick reference, the following table compares resistor tolerance to minimum and typical CMRR values assuming G = 1 or G = 2. As shown above, as gain increases so does CMRR.
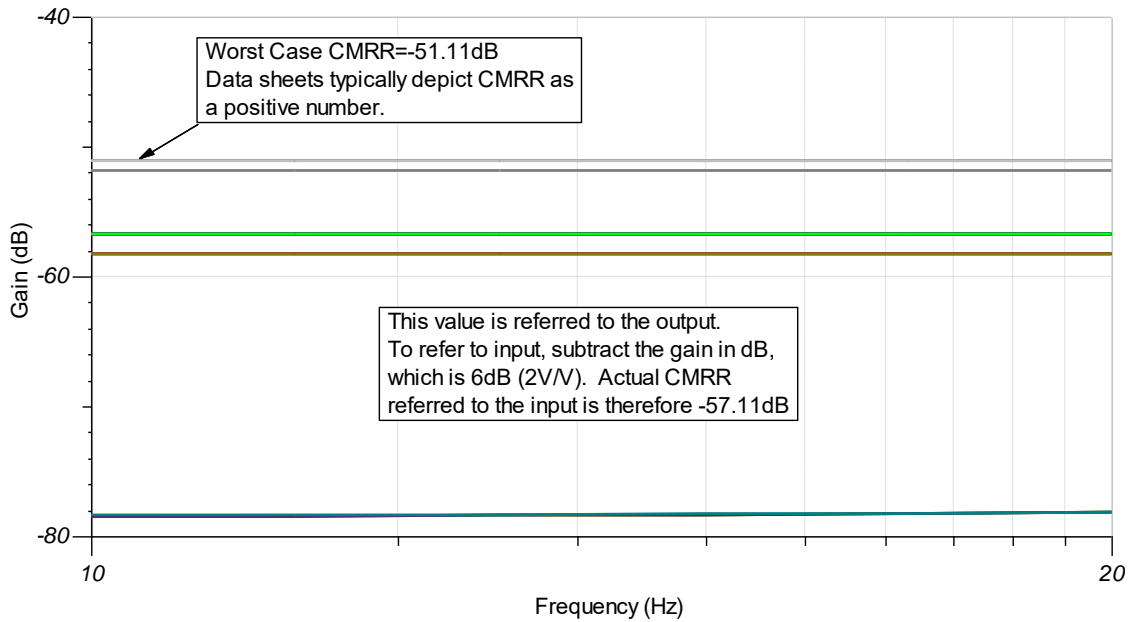
Tolerance	G=1 Minimum (dB)	G=1 Typical (dB)	G=2 Minimum (dB)	G=2 Typical (dB)
0.01%=0.0001	74	95.6	77.5	99.2
0.1%=0.001	54	75.6	57.5	79.2
0.5%=0.005	40	61.6	43.5	65.2
1%=0.01	34	55.6	37.5	59.2
5%=0.05	20	41.6	23.5	45.2

Design Simulations

DC Simulation Results
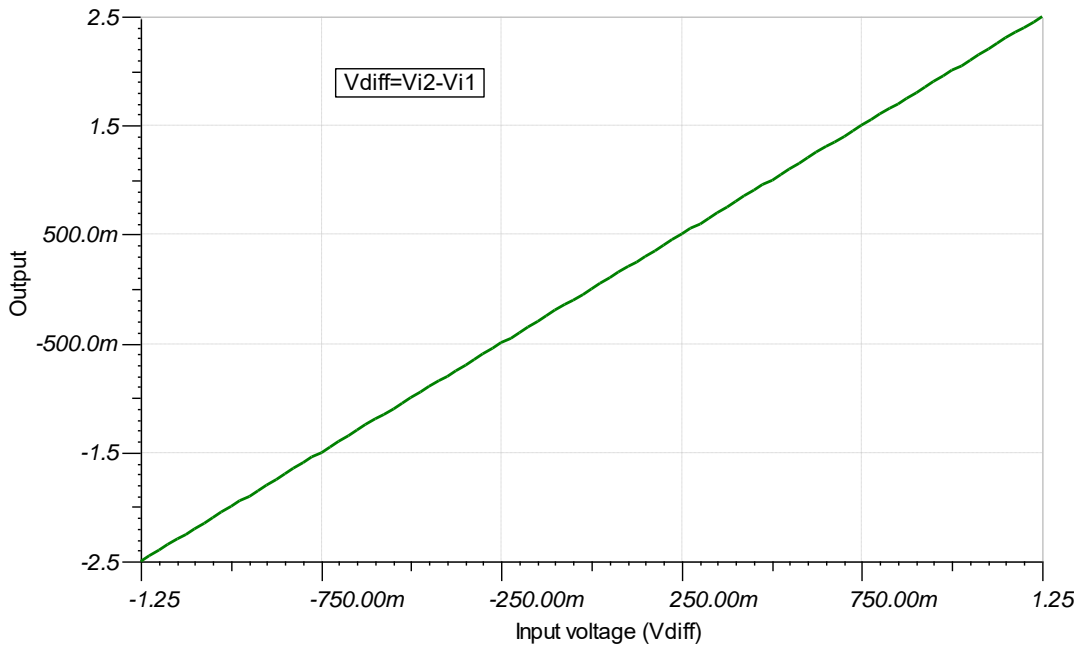
CMRR Simulation Results

Design References

For more information on many op amp topics including common-mode range, output swing, bandwidth, and how to drive an ADC please visit TI Precision Labs. For more information on difference amplifier CMRR, please read *Overlooking the obvious: the input impedance of a difference amplifier* .

Design Featured Op Amp

TLV6001	
V_{ss}	1.8V to 5.5V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	750µV
I_q	75µA
I_b	1pA
UGBW	1MHz
SR	0.5V/µs
#Channels	1, 2, 4
www.ti.com/product/tlv6001	

Design Alternate Op Amp

OPA320	
V_{ss}	1.8V to 5.5V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	40µV
I_q	1.5mA
I_b	0.2pA
UGBW	20MHz
SR	10V/µs
#Channels	1, 2
www.ti.com/product/opa320	

Integrator Circuit

Design Goals

Input			Output		Supply	
f_{Min}	f_{0dB}	f_{Max}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}
100Hz	1kHz	100kHz	−2.45V	2.45V	2.5V	−2.5V

Design Description

The integrator circuit outputs the integral of the input signal over a frequency range based on the circuit time constant and the bandwidth of the amplifier. The input signal is applied to the inverting input so the output is inverted relative to the polarity of the input signal. The ideal integrator circuit will saturate to the supply rails depending on the polarity of the input offset voltage and requires the addition of a feedback resistor, R_2, to provide a stable DC operating point. The feedback resistor limits the lower frequency range over which the integration function is performed. This circuit is most commonly used as part of a larger feedback/servo loop which provides the DC feedback path, thus removing the requirement for a feedback resistor.
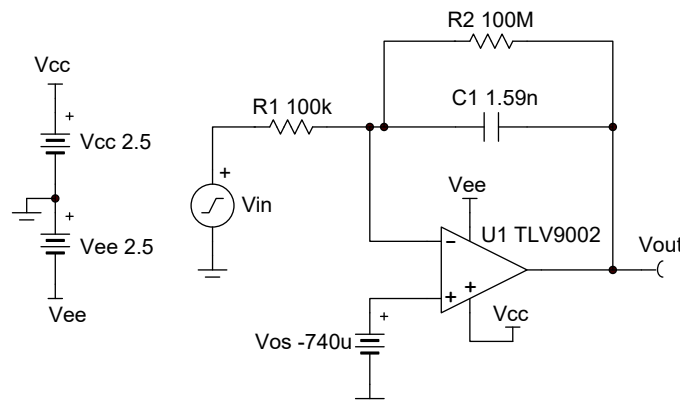
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Design Notes

1. Use as large of a value as practical for the feedback resistor.
2. Select a CMOS op amp to minimize the errors from the input bias current.
3. The gain bandwidth product (GBP) of the amplifier will set the upper frequency range of the integrator function. The effectiveness of the integration function is usually reduced starting about one decade away from the amplifier bandwidth.
4. An adjustable reference needs to be connected to the non-inverting input of the op amp to cancel the input offset voltage or the large DC noise gain will cause the circuit to saturate. Op amps with very low offset voltage may not require this.

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Design Steps

The ideal circuit transfer function is given below.

$$V_{out} = -\frac{1}{R_1 \times C_1} \int_0^t V_{in}(t)\, dt$$

1. Set R_1 to a standard value.
   $R_1 = 100k\Omega$

2. Calculate C_1 to set the unity-gain integration frequency.
   $$C_1 = \frac{1}{2 \times \pi \times R_1 \times f_{0dB}} = \frac{1}{2 \times \pi \times 100k\Omega \times 1\,kHz} = 1.59nF$$

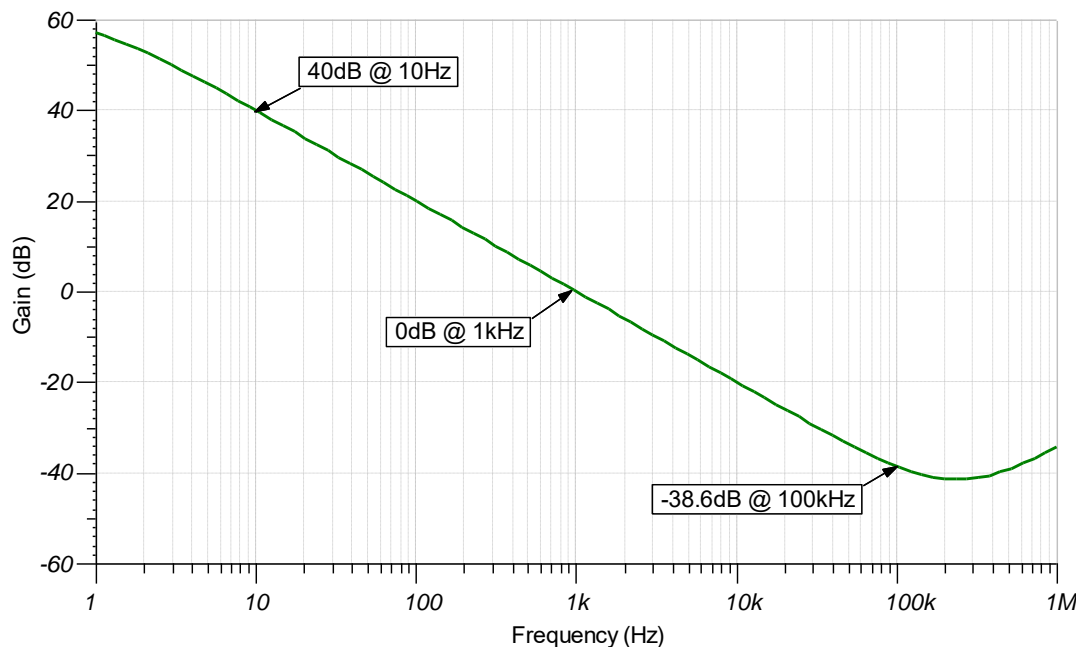3. Calculate R_2 to set the lower cutoff frequency a decade less than the minimum operating frequency.
   $$R_2 \geq \frac{10}{2 \times \pi \times C_1 \times f_{Min}} \geq \frac{10}{2 \times \pi \times 1.59nF \times 10Hz} \geq 100M\Omega$$

4. Select an amplifier with a gain bandwidth at least 10 times the desired maximum operating frequency.
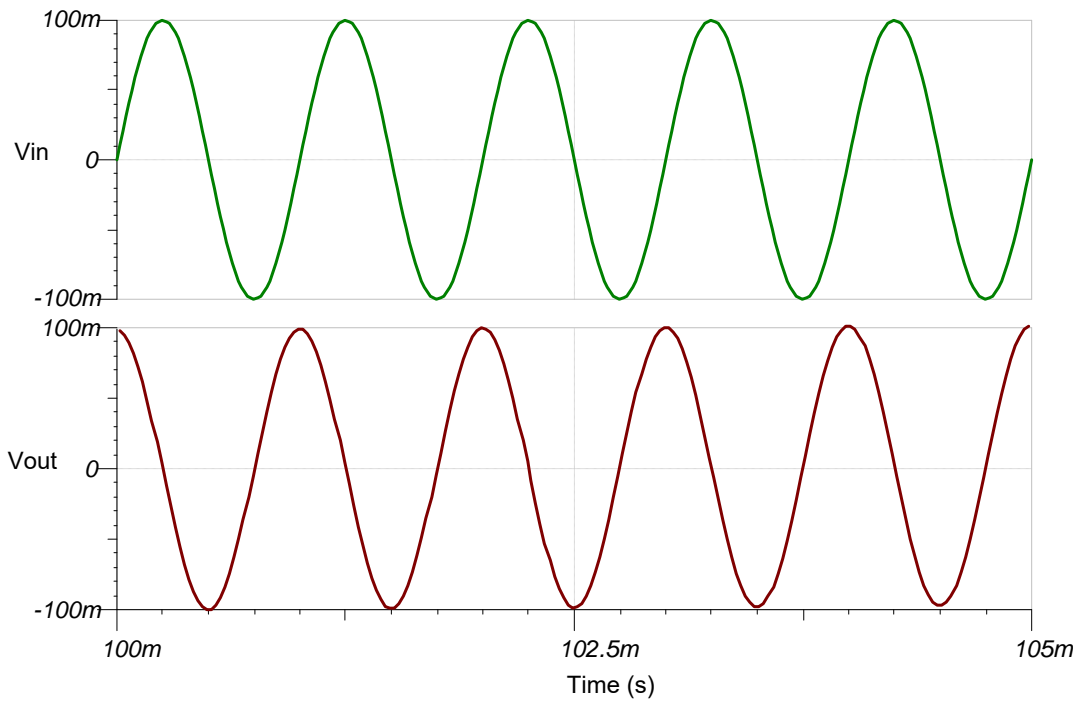 $GBP \geq 10 \times f_{Max} \geq 10 \times 100kHz \geq 1\ MHz$

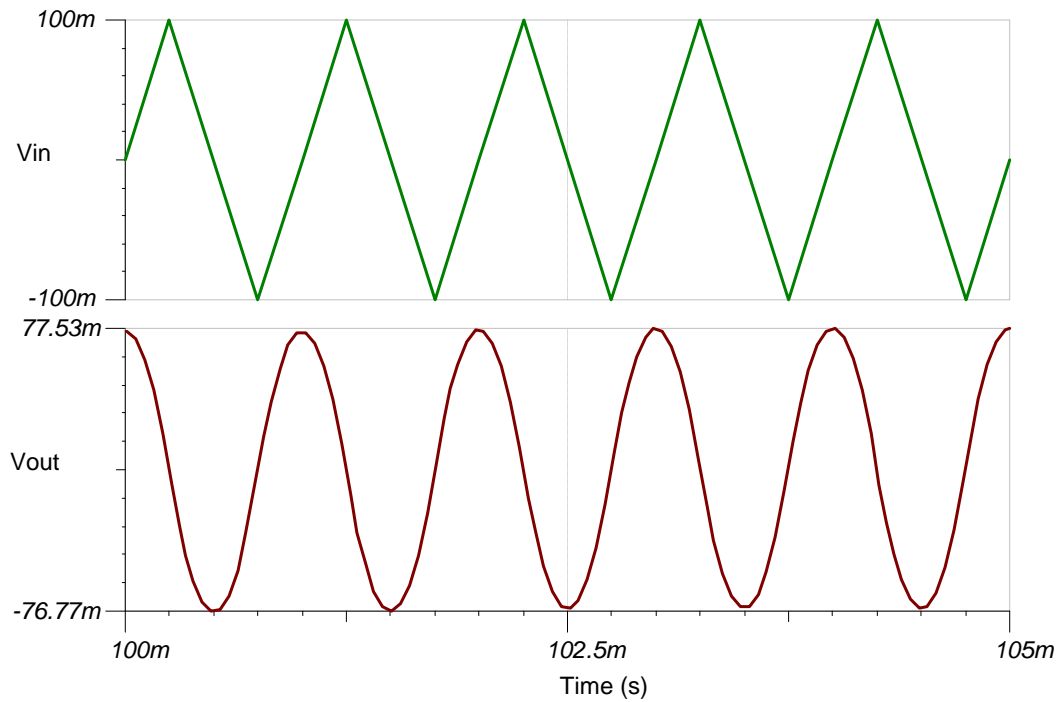## Design Simulations

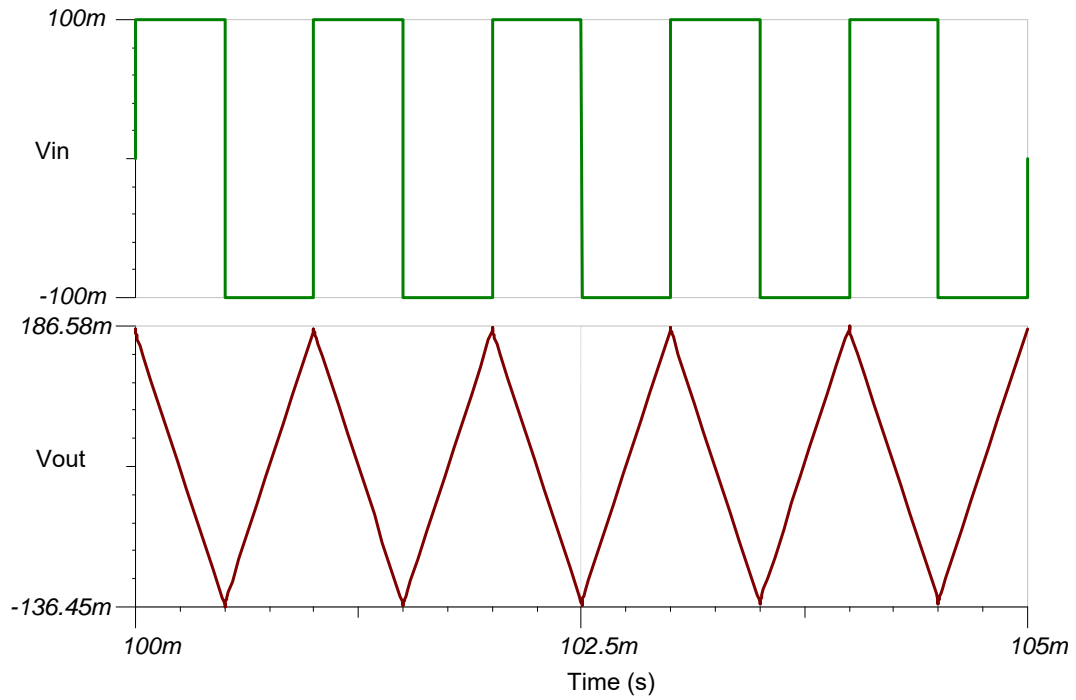## AC Simulation Results

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Transient Simulation Results

A 1-kHz sine wave input yields a 1-kHz cosine output.

A 1-kHz triangle wave input yields a 1-kHz sine wave output.

A 1-kHz square wave input yields a 1-kHz triangle wave output.

Design References

See TIPD191, www.ti.com/tool/tipd191.

Design Featured Op Amp

TLV9002	
V_{cc}	1.8V to 5.5V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	0.4mV
I_q	0.06mA
I_b	5pA
UGBW	1MHz
SR	2V/µs
#Channels	1, 2, 4
www.ti.com/product/tlv9002	

Design Alternate Op Amp

OPA376	
V_{cc}	2.2V to 5.5V
V_{inCM}	$(V_{ee}$-0.1V) to $(V_{cc}$-1.3V)
V_{out}	Rail-to-rail
V_{os}	0.005mV
I_q	0.76mA
I_b	0.2pA
UGBW	5.5MHz
SR	2V/µs
#Channels	1, 2, 4
www.ti.com/product/opa376	

Differentiator Circuit

Design Goals

Input		Output		Supply		
f_{Min}	f_{Max}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}	V_{ref}
100Hz	5kHz	0.1V	4.9V	5V	0V	2.5V

Design Description

The differentiator circuit outputs the derivative of the input signal over a frequency range based on the circuit time constant and the bandwidth of the amplifier. The input signal is applied to the inverting input so the output is inverted relative to the polarity of the input signal. The ideal differentiator circuit is fundamentally unstable and requires the addition of an input resistor, a feedback capacitor, or both, to be stable. The components required for stability limit the bandwidth over which the differentiator function is performed.
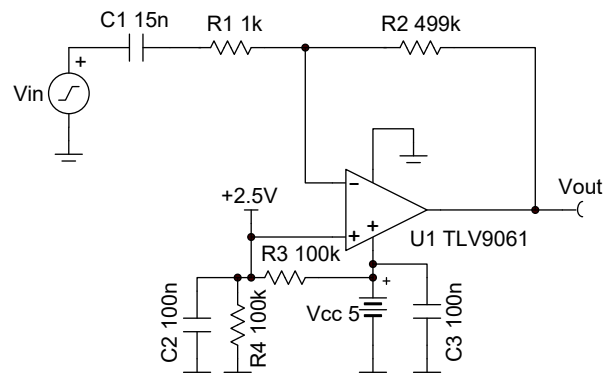
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Design Notes

1. Select a large resistance for R_2 to keep the value of C_1 reasonable.
2. A capacitor can be added in parallel with R_2 to filter the high-frequency noise of the circuit. The capacitor will limit the effectiveness of the differentiator function starting about half a decade (approximately 3.5 times) away from the filter cutoff frequency.
3. A reference voltage can be applied to the non-inverting input to set the DC output voltage which allows the circuit to work single-supply. The reference voltage can be derived from a voltage divider.
4. Operate within the linear output voltage swing (see Aol specification) to minimize non-linearity errors.

Design Steps

The ideal circuit transfer function is given below.

$$\text{Vout} = -R_2 \times C_1 \times \frac{dV_{in}(t)}{dt}$$

1. Set R_2 to a large standard value.
   $$R_2 = 499k\Omega$$

2. Set the minimum differentiation frequency at least half a decade below the minimum operating frequency.
   $$C_1 \geq \frac{3.5}{2 \times \pi \times R_2 \times f_{min}} \geq \frac{3.5}{2 \times \pi \times 499k\Omega \times 100Hz} \geq 11.1 \text{ nF} \approx 15nF \quad (\text{Standard Value})$$

3. Set the upper cutoff frequency at least half a decade above the maximum operating frequency.
   $$R_1 \leq \frac{1}{3.5 \times 2 \times \pi \times C_1 \times f_{Max}} \leq \frac{1}{7 \times \pi \times 15nF \times 2.5kHz} \leq 1.2k\Omega \approx 1 \text{ k}\Omega \quad (\text{Standard Value})$$

4. Calculate the necessary op amp gain bandwidth product (GBP) for the circuit to be stable.
   $$GBP > \frac{R_1 + R_2}{2 \times \pi \times R_1^2 \times C_1} > \frac{499k\Omega + 1 \text{ k}\Omega}{2 \times \pi \times 1 \text{ k}\Omega^2 \times 15nF} > 5.3MHz$$

   • The bandwidth of the TLV9061 is 10MHz, therefore this requirement is met.

5. If a feedback capacitor, C_F, is added in parallel with R_2, the equation to calculate the cutoff frequency follows.
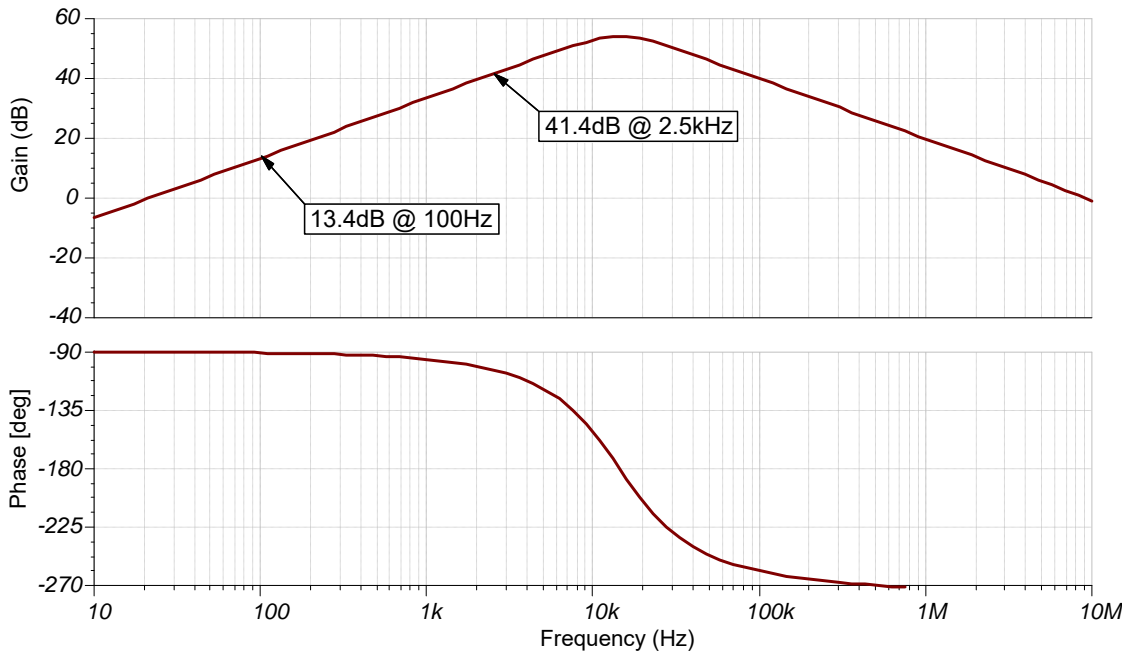 $$f_c = \frac{1}{2 \times \pi \times R_2 \times C_F}$$

6. Calculate the resistor divider values for a 2.5-V reference voltage.
   $$R_3 = \frac{V_{cc} - V_{ref}}{V_{ref}} \times R_4 = \frac{5V - 2.5V}{2.5V} \times R_4 = R_4$$
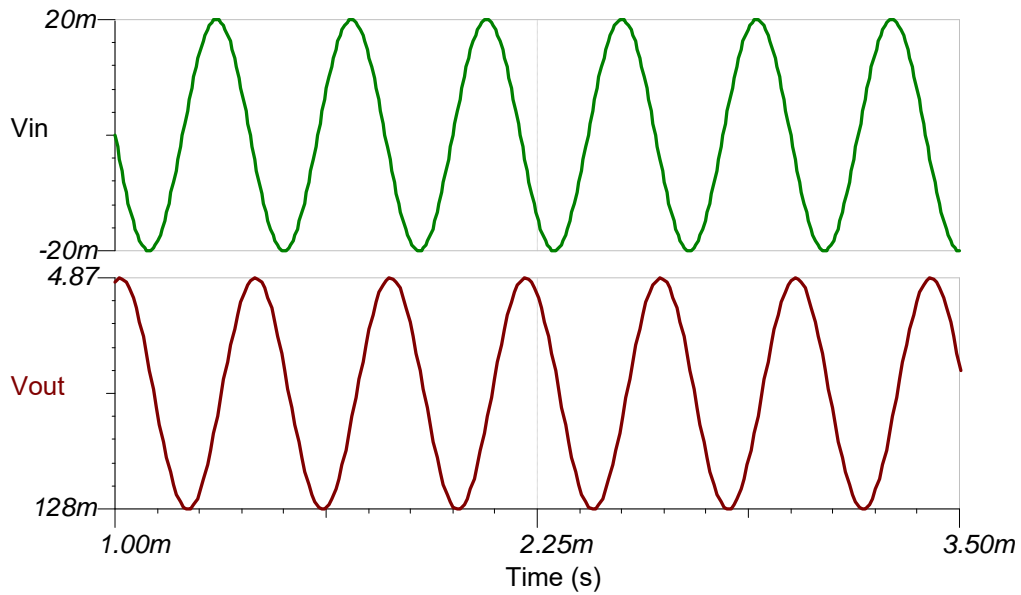 $$R_3 = R_4 = 100k\Omega \quad (\text{Standard Values})$$

Design Simulations
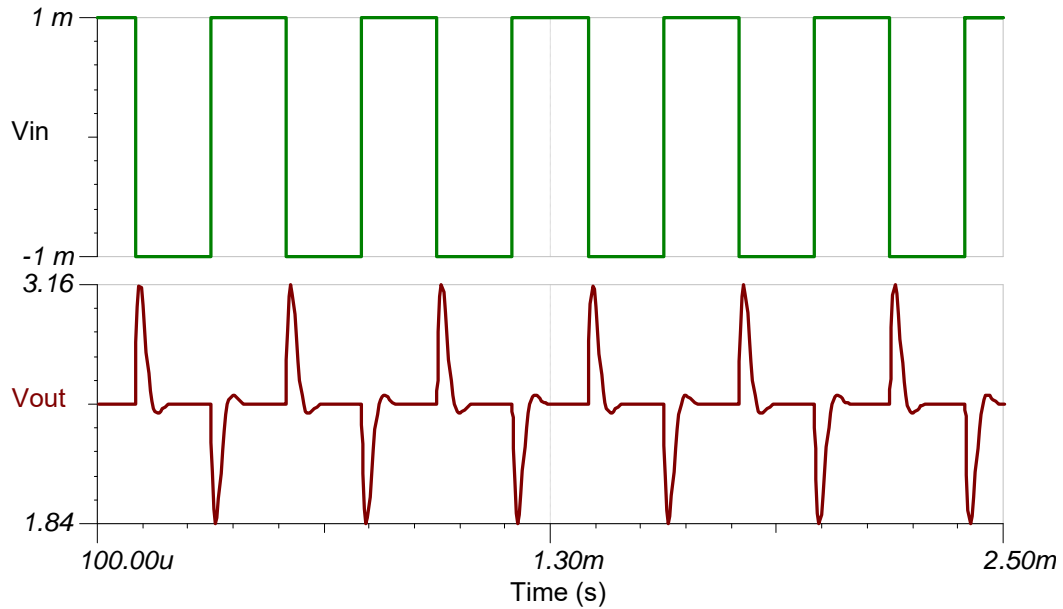
AC Simulation Results

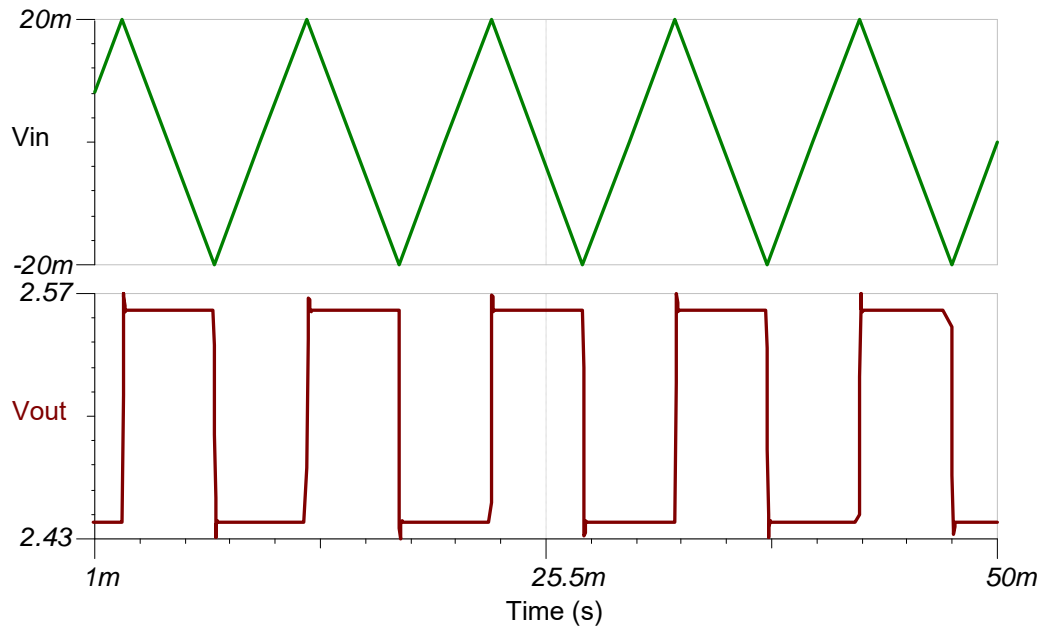### Transient Simulation Results

A 2.5-kHz sine wave input yields a 2.5-kHz cosine output.

A 2.5-kHz square wave input produces an impulse output.

A 100-Hz triangle wave input yields a square wave output.

Design Featured Op Amp

TLV9061	
V_{cc}	1.8V to 5.5V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	0.3mV
I_q	0.538mA
I_b	0.5pA
UGBW	10MHz
SR	6.5V/µs
#Channels	1, 2, 4
www.ti.com/product/tlv9061	

Design Alternate Op Amp

OPA374	
V_{cc}	2.3V to 5V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	1mV
I_q	0.585mA
I_b	0.5pA
UGBW	6.5MHz
SR	0.4V/µs
#Channels	1, 2, 4
www.ti.com/product/opa374	

Transimpedance Amplifier Circuit

Design Goals

Input		Output		BW	Supply	
I_{iMin}	I_{iMax}	V_{oMin}	V_{oMax}	f_p	V_{cc}	V_{ee}
0A	50µA	0V	5V	10kHz	15V	−15V

Design Description

The transimpedance op amp circuit configuration converts an input current source into an output voltage. The current to voltage gain is based on the feedback resistance. The circuit is able to maintain a constant voltage bias across the input source as the input current changes which benefits many sensors.
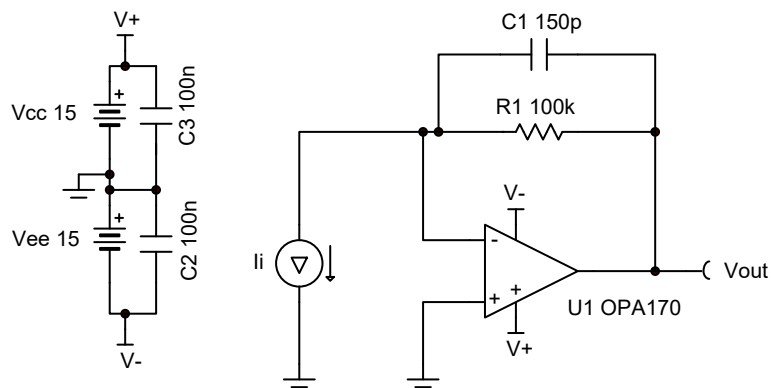
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Design Notes

1. Use a JFET or CMOS input op amp with low bias current to reduce DC errors.
2. A bias voltage can be added to the non-inverting input to set the output voltage for 0-A input currents.
3. Operate within the linear output voltage swing (see A_{ol} specification) to minimize non-linearity errors.

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Design Steps

1. Select the gain resistor.

$$R_1 = \frac{V_{oMax} - V_{oMin}}{I_{iMax}} = \frac{5V - 0V}{50\mu A} = 100k\Omega$$

2. Select the feedback capacitor to meet the circuit bandwidth.

$$C_1 \leq \frac{1}{2 \times \pi \times R_1 \times f_p}$$

$$C_1 \leq \frac{1}{2 \times \pi \times 100k\Omega \times 10kHz} \leq 159pF \approx 150pF \text{ (Standard Value)}$$

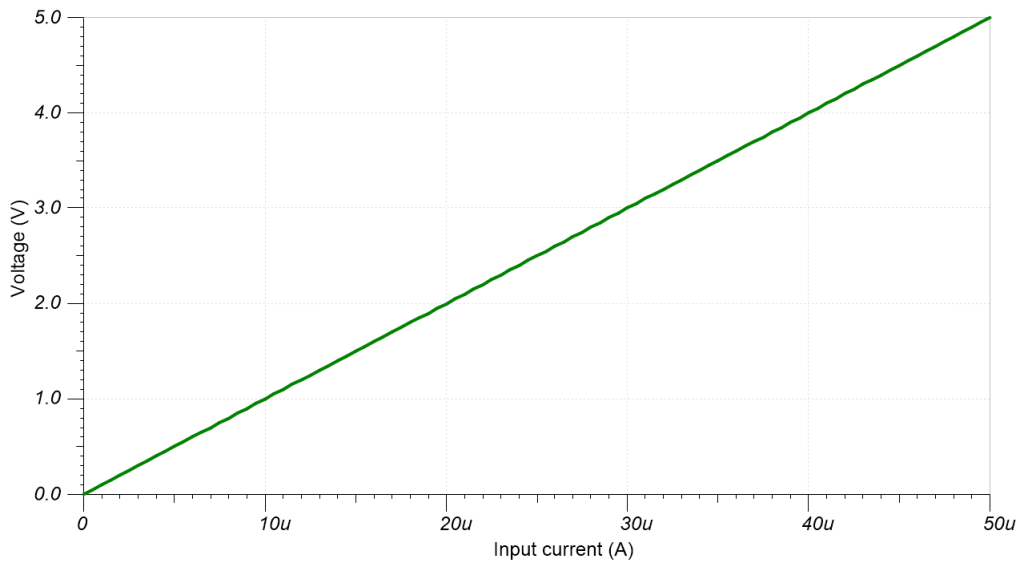3. Calculate the necessary op amp gain bandwidth (GBW) for the circuit to be stable.

$$GBW > \frac{C_i + C_1}{2 \times \pi \times R_1 \times C_1^2} > \frac{6pF + 150pF}{2 \times \pi \times 100k\Omega \times (150pF)^2} > 11.03kHz$$

where $C_i = C_s + C_d + C_{cm} = 0pF + 3pF + 3pF = 6pF$ given

- C_s: Input source capacitance
- C_d: Differential input capacitance of the amplifier
- C_{cm}: Common-mode input capacitance of the inverting input

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Transimpedance Amplifier Circuit

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Submit Documentation Feedback

Design Simulations

DC Simulation Results

AC Simulation Results

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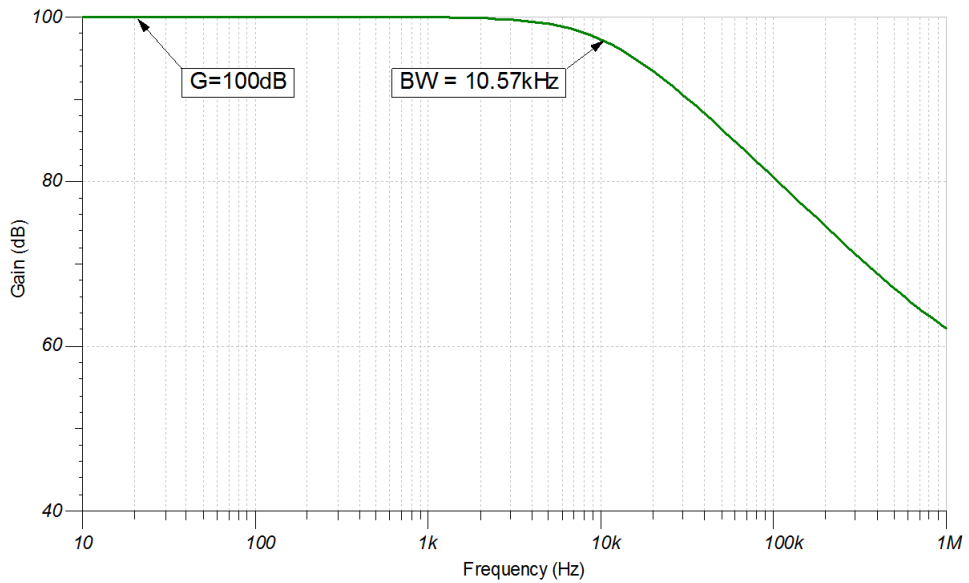
Design References

See TIPD176, www.ti.com/tool/tipd176.

Design Featured Op Amp

OPA170	
V_{cc}	2.7V to 36V
V_{inCM}	(V_{ee}–0.1V) to (V_{cc} –2V)
V_{out}	Rail–to–rail
V_{os}	0.25mV
I_q	0.11mA
I_b	8pA
UGBW	1.2MHz
SR	0.4V/µs
#Channels	1, 2, 4
www.ti.com/product/opa170	

Design Alternate Op Amp

OPA145	
V_{cc}	4.5V to 36V
V_{inCM}	(V_{ee}–0.1V) to (V_{cc} –3.5V)
V_{out}	Rail–to–rail
V_{os}	40µV
I_q	0.445mA
I_b	2pA
UGBW	5.5MHz
SR	20V/µs
#Channels	1, 2, 4
www.ti.com/product/opa145	

TEXAS INSTRUMENTS

Single-Supply, Low-Side, Unidirectional Current-Sensing Solution with Output Swing to GND Circuit

Design Goals

Input		Output		Supply		
I_{iMin}	I_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}	V_{ref}
0A	1A	0V	4.9V	5V	0V	0V

Design Description

This single-supply, low-side, current sensing solution accurately detects load current between 0A to 1A and converts it to a voltage between 0V to 4.9V. The input current range and output voltage range can be scaled as necessary and larger supplies can be used to accommodate larger swings. A negative charge pump (such as the LM7705) is used as the negative supply in this design to maintain linearity for output signals near 0V.
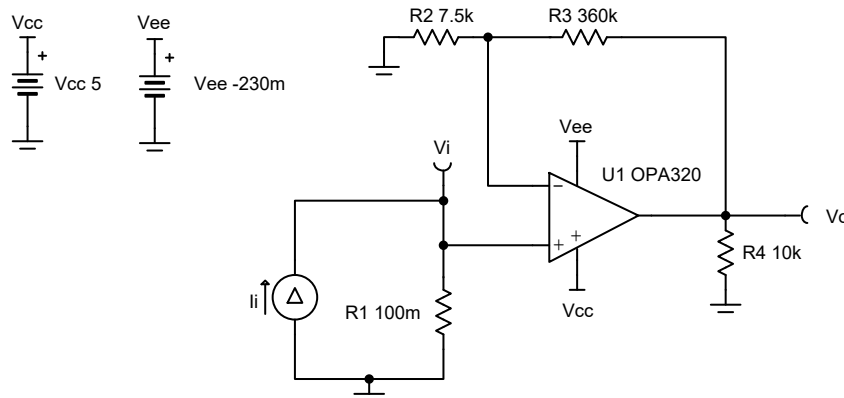
Copyright © 2018, Texas Instruments Incorporated

Design Notes

1. Use precision resistors to minimize gain error.
2. For light load accuracy, the negative supply should extend slightly below ground.
3. A capacitor placed in parallel with the feedback resistor will limit bandwidth and help reduce noise.

Design Steps

1. Determine the transfer function.

$$V_O = I_i \times R_1 \times \left(1 + \frac{R_3}{R_2}\right)$$

2. Define the full-scale shunt voltage and shunt resistance.

$$V_{iMax} = 100mV \text{ at } I_{iMax} = 1A$$

$$R_1 = \frac{V_{iMax}}{I_{iMax}} = \frac{100mV}{1\,A} = 100m\Omega$$

3. Select gain resistors to set the output range.

$$V_{iMax} = 100mV \text{ and } V_{oMax} = 4.9V$$

$$Gain = \frac{V_{oMax}}{V_{iMax}} = \frac{4.9V}{100mV} = 49\frac{V}{V}$$

$$Gain = 1 + \frac{R_3}{R_2} = 49\frac{V}{V}$$

4. Select a standard value for R_2 and R_3.

$$R_2 = 7.5k\Omega \text{ (0.05\% Standard Value)}$$

$$R_3 = 48 \times R_2 = 360k\Omega \text{ (0.05\% Standard Value)}$$

Design Simulations

DC Simulation Results

AC Simulation Results

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Single-Supply, Low-Side, Unidirectional Current-Sensing Solution with Output Swing to GND Circuit
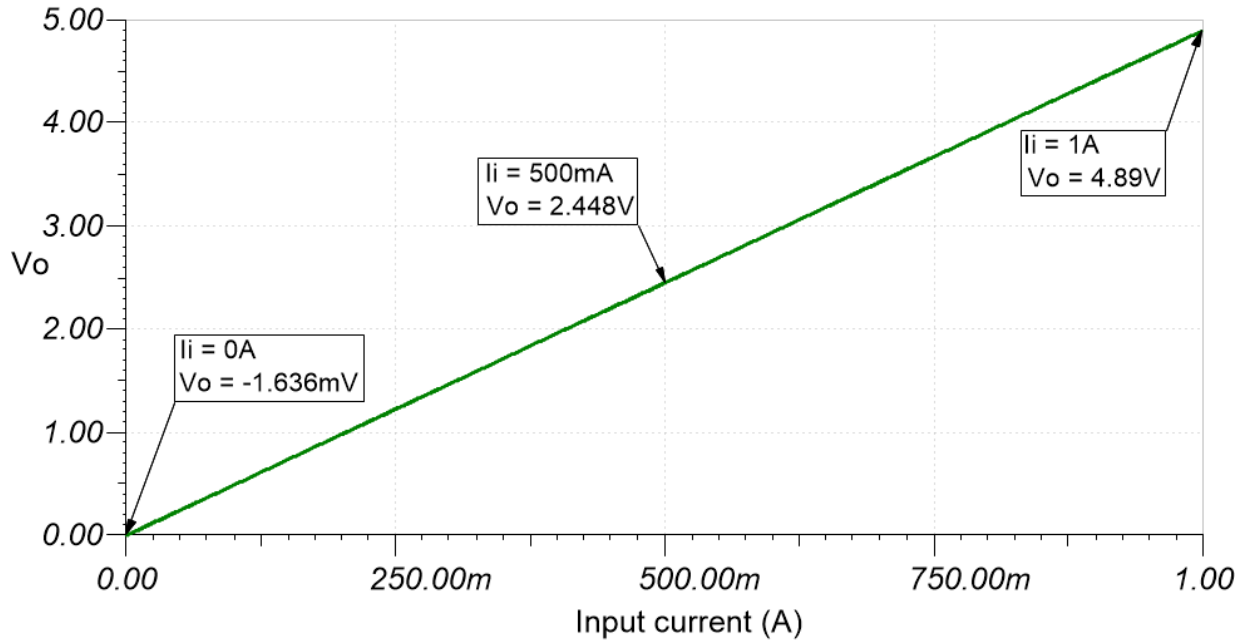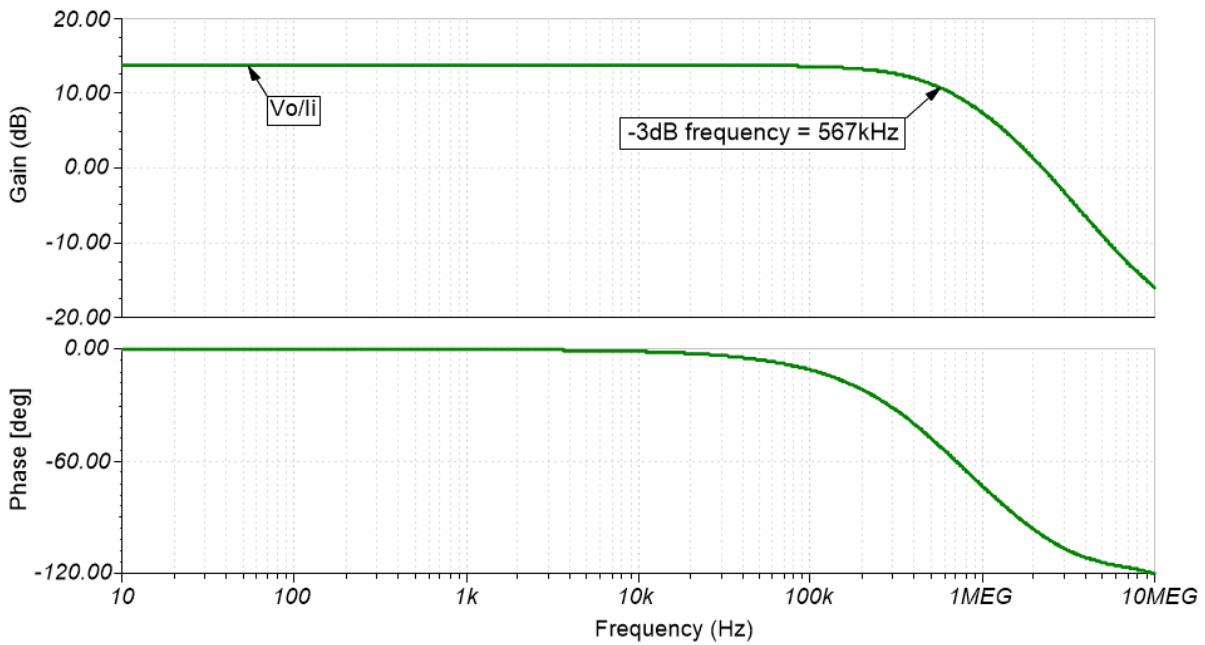
Design References

See TIPD129, www.ti.com/tool/tipd129.

Design Featured Op Amp

OPA320	
V_{cc}	1.8V to 5.5V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	40µV
I_q	1.5mA/Ch
I_b	0.2pA
UGBW	10MHz
SR	10V/µs
#Channels	1, 2
www.ti.com/product/opa320	

Design Alternate Op Amp

TLV9002	
V_{cc}	1.8V to 5.5V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	400µV
I_q	60µA
I_b	5pA
UGBW	1MHz
SR	2V/µs
#Channels	1, 2, 4
www.ti.com/product/tlv9002	

Low-Side, Bidirectional Current Sensing Circuit

Design Goals

Input		Output		Supply		
I_{iMin}	I_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}	V_{ref}
−1A	1A	110mV	3.19V	3.3V	0V	1.65V

Design Description

This single-supply low-side, bidirectional current sensing solution can accurately detect load currents from −1A to 1A. The linear range of the output is from 110mV to 3.19V. Low-side current sensing keeps the common-mode voltage near ground, and is thus most useful in applications with large bus voltages.
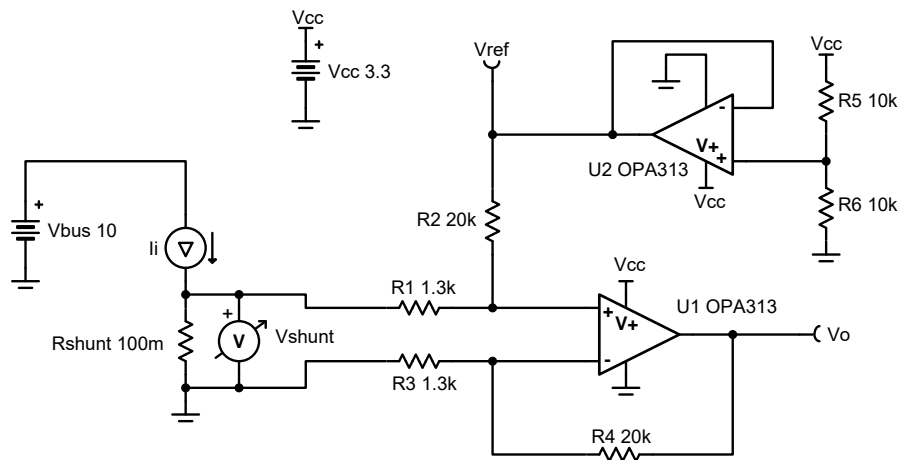
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Design Notes

1. To minimize errors, set $R_3 = R_1$ and $R_4 = R_2$.
2. Use precision resistors for higher accuracy.
3. Set output range based on linear output swing (see A_{ol} specification).
4. Low-side sensing should not be used in applications where the system load cannot withstand small ground disturbances or in applications that need to detect load shorts.

Design Steps

1. Determine the transfer equation given $R_4 = R_2$ and $R_1 = R_3$.

$$V_O = \left(I_i \times R_{shunt} \times \frac{R_4}{R_3} \right) + V_{ref}$$

$$V_{ref} = V_{cc} \times \left(\frac{R_6}{R_5 + R_6} \right)$$

2. Determine the maximum shunt resistance.

$$R_{shunt} = \frac{V_{shunt}}{I_{imax}} = \frac{100mV}{1\,A} = 100m\Omega$$

3. Set reference voltage.

   a. Since the input current range is symmetric, the reference should be set to mid supply. Therefore, make R_5 and R_6 equal.

$$R_5 = R_6 = 10k\Omega$$

4. Set the difference amplifier gain based on the op amp output swing. The op amp output can swing from 100mV to 3.2V, given a 3.3-V supply.

$$Gain = \frac{V_{oMax} - V_{oMin}}{R_{shunt} \times (I_{iMax} - I_{iMin})} = \frac{3.2\,V - 100mV}{100m\Omega \times (1\,A - (-1\,A))} = 15.5\,\frac{V}{V}$$

$$Gain = \frac{R_4}{R_3} = 15.5\,\frac{V}{V}$$

Choose $R_1 = R_3 = 1.3k\Omega$ (Standard Value)

$$R_2 = R_4 = 15.5\frac{V}{V} \times 1.3k\Omega = 20.15\,k\Omega \approx 20k\Omega \text{ (Standard Value)}$$

Design Simulations

DC Simulation Results
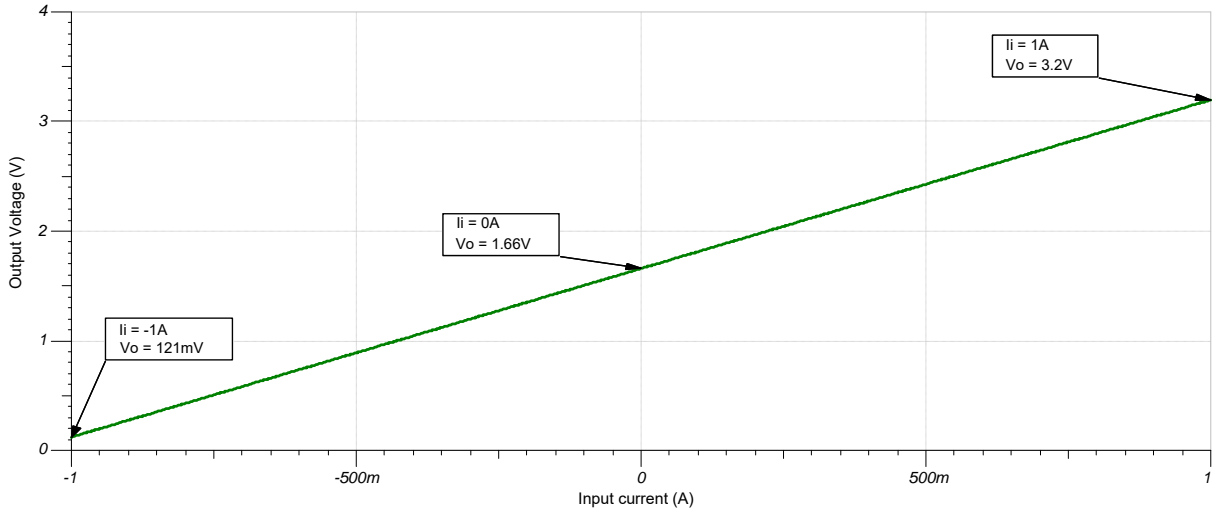
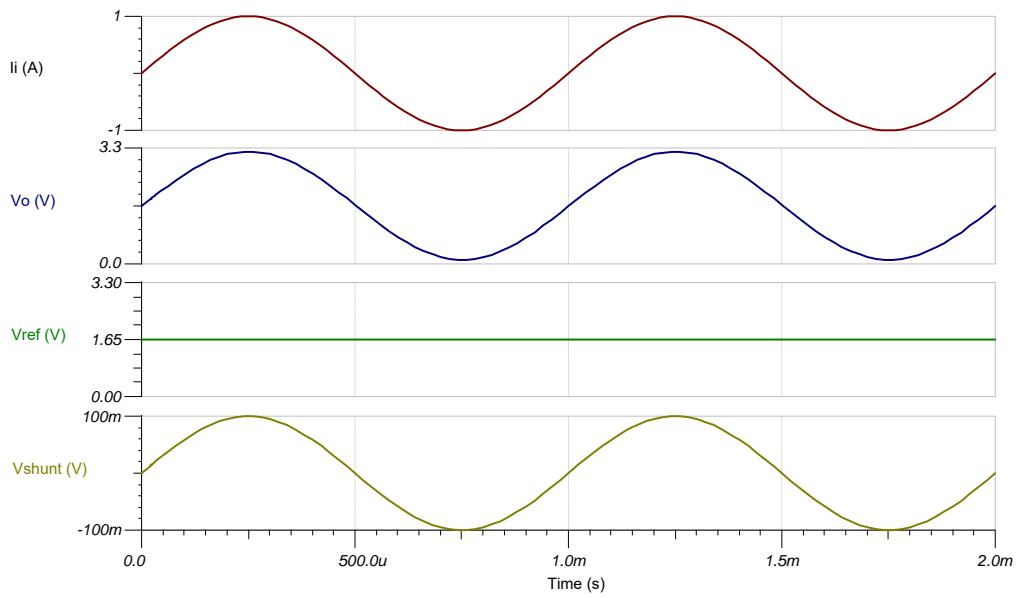
Closed Loop AC Simulation Results

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Low-Side, Bidirectional Current Sensing Circuit
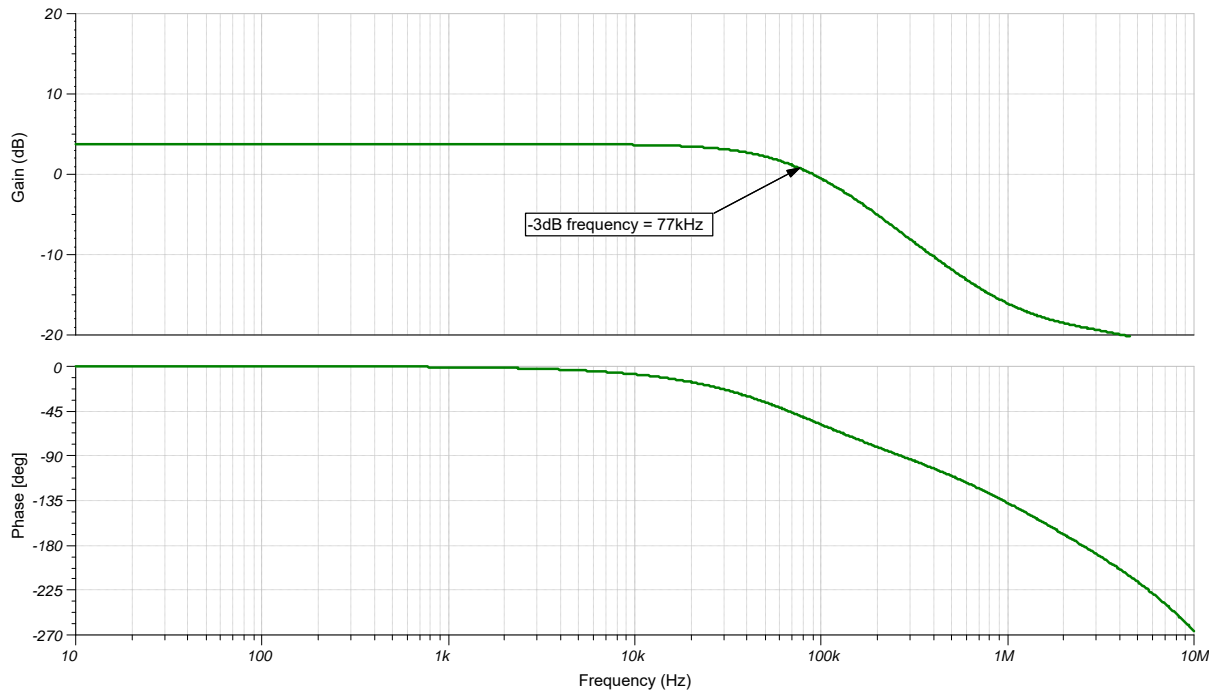
Transient Simulation Results

Design References

See TIPD175, www.ti.com/tipd175.

Design Featured Op Amp

OPA313	
V_{cc}	1.8V to 5.5V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	500µV
I_q	50µA/Ch
I_b	0.2pA
UGBW	1MHz
SR	0.5V/µs
#Channels	1, 2, 4
www.ti.com/product/opa313	

Design Alternate Op Amp

TLV9062	
V_{cc}	1.8V to 5.5V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	300µV
I_q	538µA/Ch
I_b	0.5pA
UGBW	10MHz
SR	6.5V/µs
#Channels	1, 2, 4
www.ti.com/product/tlv9062	

Design Alternate Op Amp

OPA376	
V_{cc}	2.2V to 5.5V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	5µV
I_q	760µA/Ch
I_b	0.2pA
UGBW	5.5MHz
SR	2V/µs
#Channels	1, 2, 4
www.ti.com/product/opa376	

3-Decade, Load-Current Sensing Circuit

Design Goals

Input		Output		Supply		
I_{iMin}	I_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}	V_{ref}
10μA	10mA	100mV	4.9V	5.0V	0V	0V

Design Description

This single-supply, low-side, current-sensing solution accurately detects load current between 10μA and 10mA. A unique yet simple gain switching network was implemented to accurately measure the three-decade load current range.
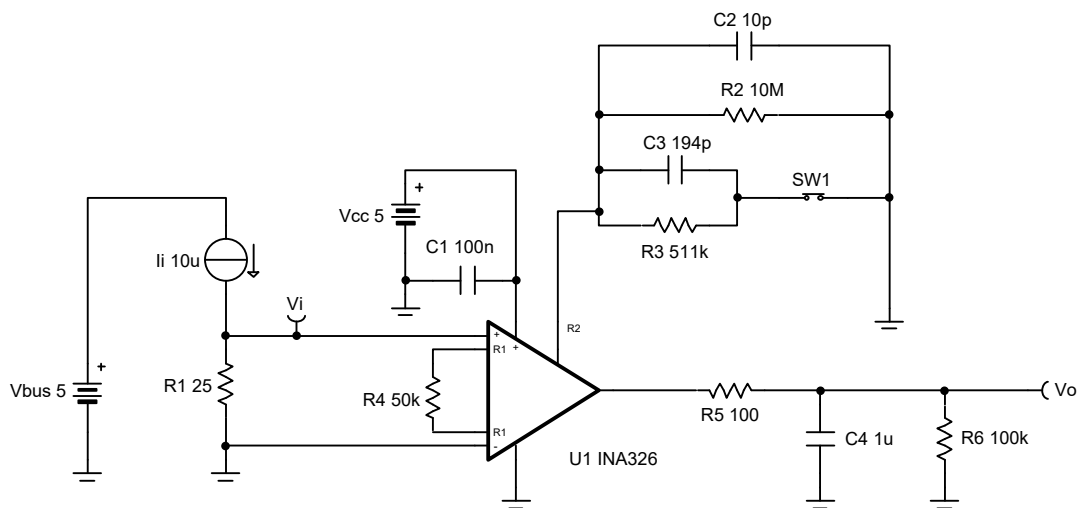
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Design Notes

1. Use a maximum shunt resistance to minimize relative error at minimum load current.
2. Select 0.1% tolerance resistors for R_1, R_2, R_3, and R_4 in order to achieve approximately 0.1% FSR gain error.
3. Use a switch with low on-resistance (R_{on}) to minimize interaction with feedback resistances, preserving gain accuracy.
4. Minimize capacitance on INA326 gain setting pins.
5. Scale the linear output swing based on the gain error specification.

Design Steps

1. Define full-scale shunt resistance.

$$R_1 = \frac{V_{iMax}}{I_{iMax}} = \frac{250mV}{10mA} = 25\Omega$$

2. Select gain resistors to set output range.

$$G_{IiMax} = \frac{V_{oMax}}{V_{iMax}} = \frac{V_{oMax}}{R_1 \times I_{iMax}} = \frac{4.9V}{25\Omega \times 10mA} = 19.6\frac{V}{V}$$

$$G_{IiMin} = \frac{V_{oMin}}{V_{iMin}} = \frac{V_{oMin}}{R_1 \times I_{iMin}} = \frac{100mV}{25\Omega \times 10\mu A} = 400\frac{V}{V}$$

$$R_2 = \frac{R_4 \times G_{IiMin}}{2} = \frac{50k\Omega \times 400\frac{V}{V}}{2} = 10M\Omega$$

$$R_2 \| R_3 = \frac{R_4 \times G_{IiMax}}{2} = \frac{50k\Omega \times 19.6\frac{V}{V}}{2} = 490k\Omega$$

$$R_3 = \frac{490k\Omega \times R_2}{R_2 - 490k\Omega} = 515.25k\Omega \approx 511k\Omega \text{ (Standard Value)}$$

3. Select a capacitor for the output filter.

$$f_p = \frac{1}{2 \times \pi \times R_5 \times C_4} = \frac{1}{2 \times \pi \times 100\Omega \times 1\mu F} = 1.59kHz$$

4. Select a capacitor for gain and filtering network.

$$C_2 = \frac{1}{2 \times \pi \times R_2 \times f_p} = \frac{1}{2 \times \pi \times 10M\Omega \times 1.59kHz} = 10pF$$

$$C_3 = \frac{1}{2 \times \pi \times (R_2 \| R_3) \times f_p} - C_2 = \frac{1}{2 \times \pi \times (10M\Omega \| 511k\Omega) \times 1.59kHz} - 10pF$$

$$C_3 = 196pF \approx 194pF \text{ (Standard Value)}$$

Design Simulations

DC Simulation Results
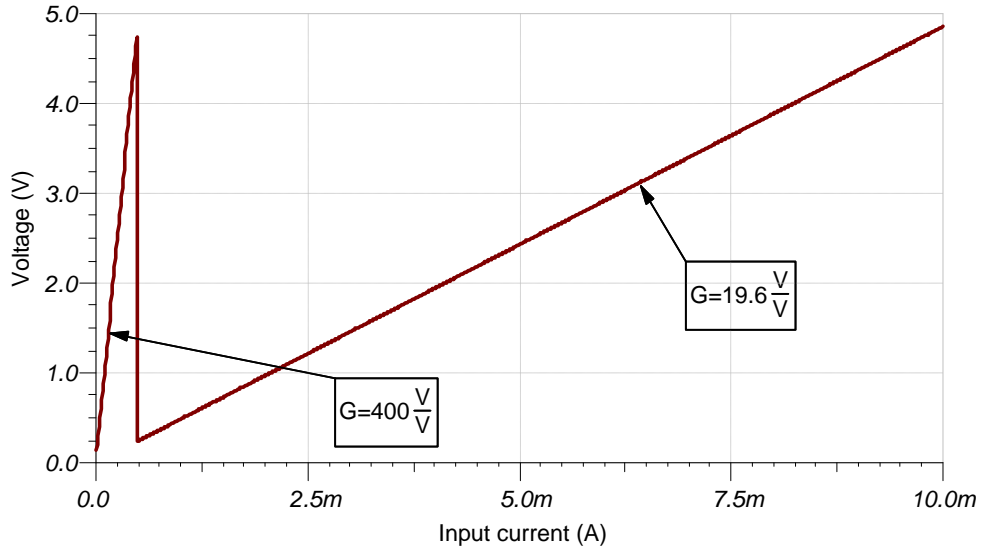
AC Simulation Results
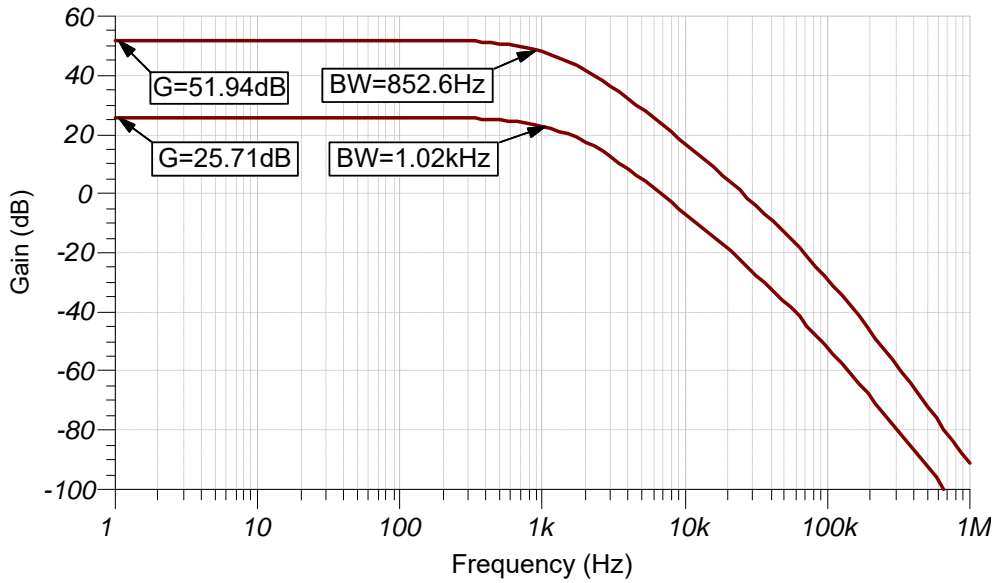
Design References

See TIPD104, www.ti.com/tool/tipd104.

Design Featured Op Amp

INA326	
V_{ss}	1.8V to 5.5V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	0.1mV
I_q	3.4mA
I_b	2nA
UGBW	1kHz
SR	Filter limited
#Channels	1
www.ti.com/product/ina326	

PWM Generator Circuit

Design Goals

Input		Output		Supply		
V_{iMin}	V_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}	V_{ref}
−2.0V	2.0V	0V	5V	5V	0V	2.5V

Design Description

This circuit utilizes a triangle wave generator and comparator to generate a 500 kHz pulse-width-modulated (PWM) waveform with a duty cycle that is inversely proportional to the input voltage. An op amp and comparator (U_3 and U_4) generate a triangle waveform which is applied to the inverting input of a second comparator (U_2). The input voltage is applied to the non-inverting input of U_2. By comparing the input waveform to the triangle wave, a PWM waveform is produced. U_2 is placed in the feedback loop of an error amplifier (U_1) to improve the accuracy and linearity of the output waveform.
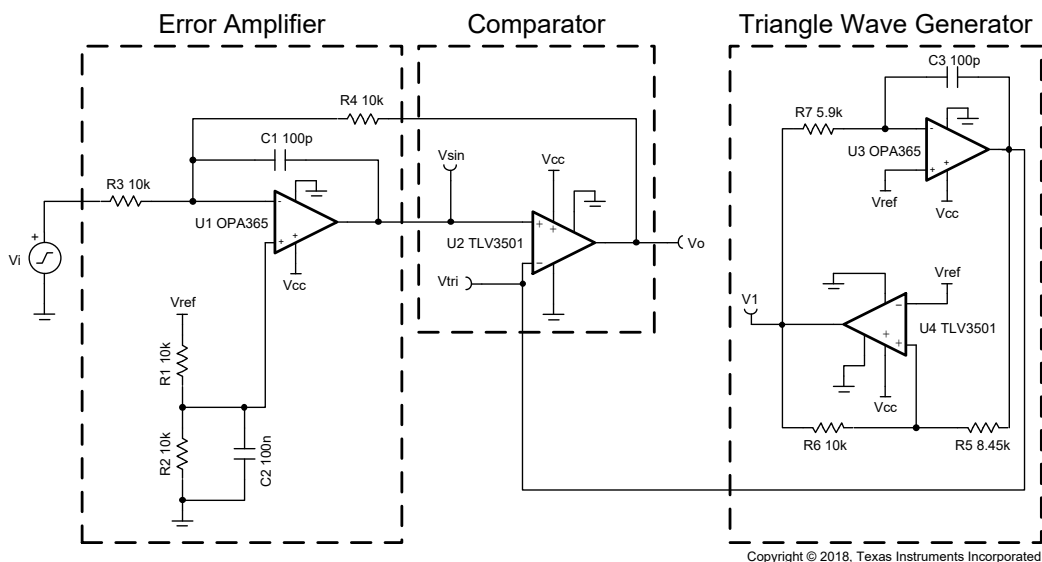
Design Notes

1. Use a comparator with push-pull output and minimal propagation delay.
2. Use an op amp with sufficient slew rate, GBW, and voltage output swing.
3. Place the pole created by C_1 below the switching frequency and well above the audio range.
4. V_{ref} must be low impedance (for example, output of an op amp).

Design Steps

1. Set the error amplifier inverting signal gain.

$$\text{Gain} = -\frac{R_4}{R_3} = -1\frac{V}{V}$$

Select $R_3 = R_4 = 10\text{k}\Omega$

2. Determine R_1 and R_2 to divide V_{ref} to cancel the non-inverting gain.

$$V_{o\_dc} = \left(1 + \frac{R_4}{R_3}\right)\left(\frac{R_2}{R_1 + R_2}\right) \times Vref$$

$R_1 = R_2 = R_3 = R_4 = 10\text{k}\Omega$, $V_{o\_dc} = 2.5\text{V}$

3. The amplitude of V_{tri} must be chosen such that it is greater than the maximum amplitude of V_i (2.0V) to avoid 0% or 100% duty cycle in the PWM output signal. Select V_{tri} to be 2.1V. The amplitude of $V_1 = 2.5\text{V}$.

$$V_{tri} \text{ (Amplitude)} = \frac{R_5}{R_6} \times V_1\text{(Amplitude)}$$

Select R_6 to be 10kΩ,   then compute R_5

$$R_5 = \frac{V_{tri}\text{(Amplitude)} \times R_6}{V_1 \text{ (Amplitude)}} = 8.4\text{k}\Omega \approx 8.45\text{k}\Omega \text{ (Standard Value)}$$

4. Set the oscillation frequency to 500kHz.

$$f_t = \frac{R_6}{4 \times R_7 \times R_5 \times C_3}$$

Set $C_3 = 100\text{pF}$, then compute R_7

$$R_7 = \frac{R_6}{4 \times f_t \times R_5 \times C_3} = 5.92\text{k}\Omega \approx 5.90\text{k}\Omega \text{ (Standard Value)}$$

5. Choose C_1 to limit amplifier bandwidth to below switching frequency.

$$f_p = \frac{1}{2 \times \pi \times R_4 \times C_1}$$

$C_1 = 100\text{pF} \rightarrow f_p = 159\text{kHz}$

6. Select C_2 to filter noise from V_{ref}.

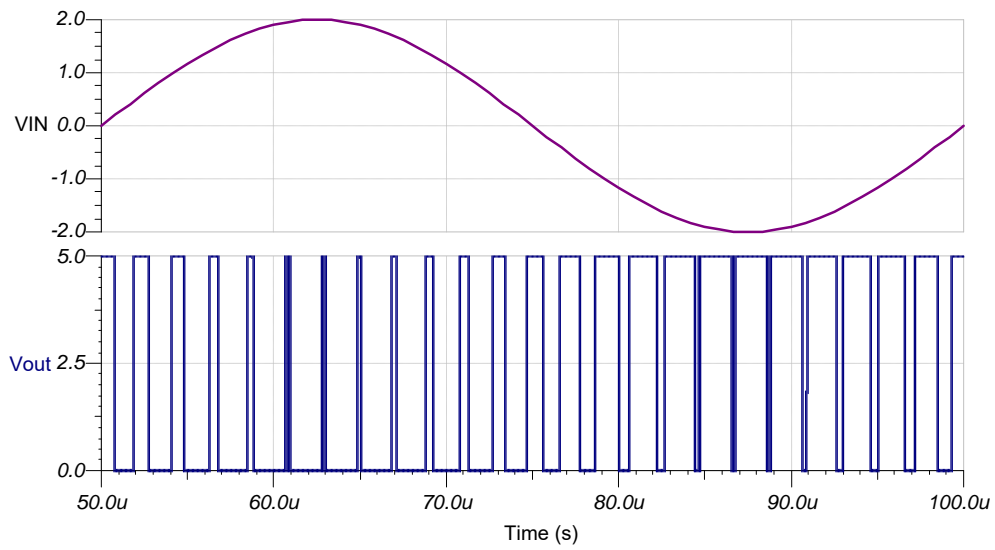$C_2 = 100\text{nF}$ (Standard Value)

$$f_{div} = \frac{1}{2 \times \pi \times C_2 \times \frac{R_1 \times R_2}{R_1 + R_2}} = 320\text{Hz}$$

Design Simulations

DC Simulation Results
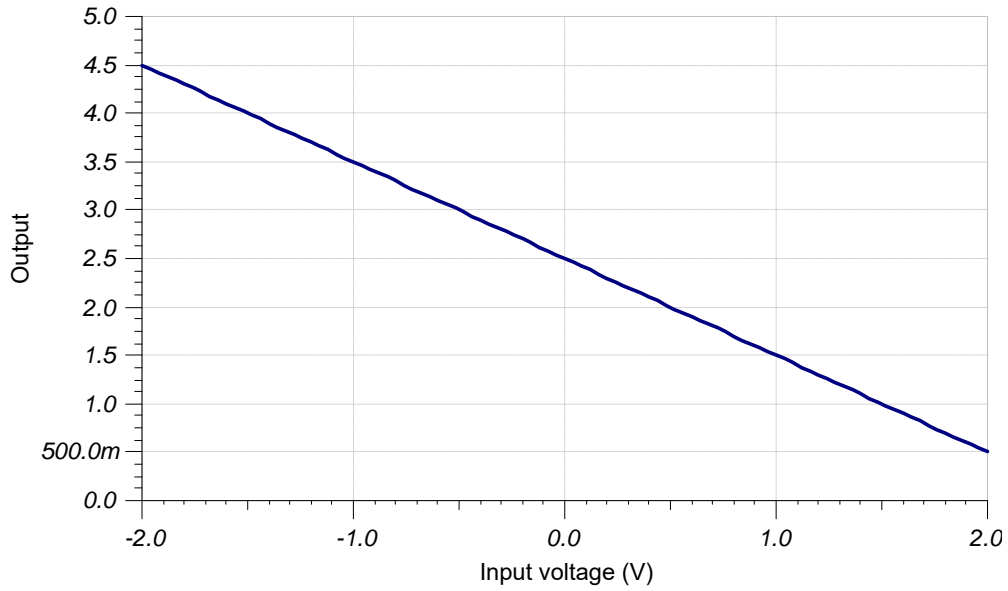
Transient Simulation Results

Design References

See TIPD108, www.ti.com/tool/tipd108

Design Featured Op Amp

OPA2365	
V_{ss}	2.2V to 5.5V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	100µV
I_q	4.6mA
I_b	2pA
UGBW	50MHz
SR	25V/µs
#Channels	2
www.ti.com/product/opa2365	

Design Comparator

TLV3502	
V_{ss}	2.2V to 5.5V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	1mV
I_q	3.2mA
I_b	2pA
UGBW	-
SR	-
#Channels	2
www.ti.com/product/tlv3502	

Design Alternate Op Amp

OPA2353	
V_{ss}	2.7V to 5.5V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	3mV
I_q	5.2mA
I_b	0.5pA
UGBW	44MHz
SR	22V/µs
#Channels	2
www.ti.com/product/opa2353	

AC Coupled (HPF) Inverting Amplifier Circuit

Design Goals

Input		Output		Supply		
V_{iMin}	V_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}	V_{ref}
−240mV	240mV	0.1V	4.9V	5V	0V	5V

Design Description

This circuit amplifies an AC signal and shifts the output signal so that it is centered at half the power supply voltage. Note that the input signal has zero DC offset so it swings above and below ground. The key benefit of this circuit is that it accepts signals which swing below ground even though the amplifier does not have a negative power supply.
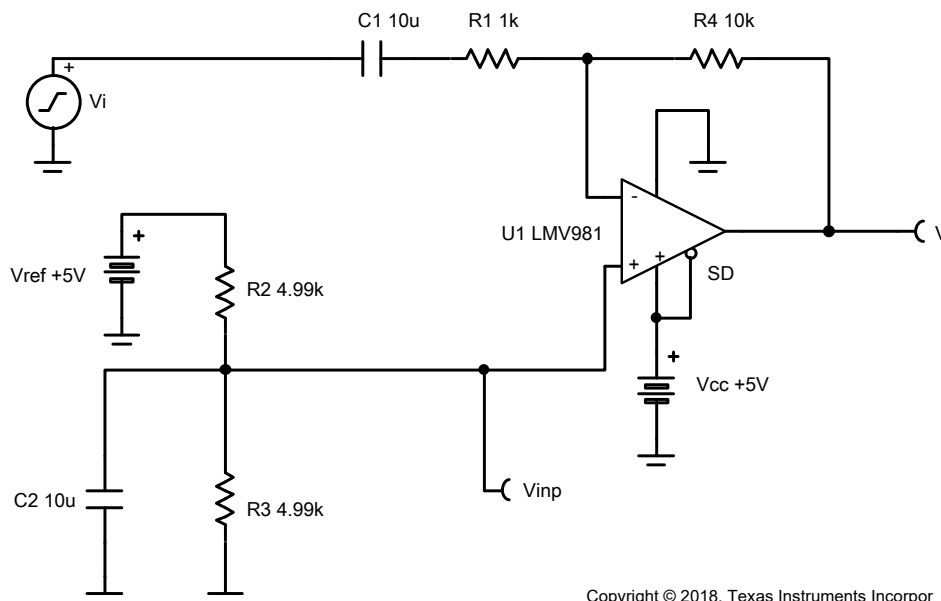
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Design Notes

1. R_1 sets the AC input impedance. R_4 loads the op amp output.
2. Use low feedback resistances to reduce noise and minimize stability concerns.
3. Set the output range based on linear output swing (see A_{ol} specification).
4. The cutoff frequency of the circuit is dependent on the gain bandwidth product (GBP) of the amplifier. Additional filtering can be accomplished by adding a capacitor in parallel to R_4. Adding a capacitor in parallel with R_4 will also improve stability of the circuit if high-value resistors are used.

Design Steps

1. Select R_1 and R_4 to set the AC voltage gain.
   $R_1 = 1 \ k\Omega$ (Standard Value)

   $R_4 = R_1 \times |G_{ac}| = 1 \ k\Omega \times \left| -10\frac{V}{V} \right| = 10k\Omega$ (Standard Value)

2. Select R_2 and R_3 to set the DC output voltage to 2.5V.
   $R_3 = 4.99k\Omega$ (Standard Value)

   $R_2 = \frac{R_3 \times V_{ref}}{V_{DC}} - R_3 = \frac{4.99k\Omega \times 5V}{2.5V} - 4.99k\Omega = 4.99k\Omega$

3. Choose a value for the lower cutoff frequency, f_l, then calculate C_1.
   $f_l = 16Hz$

   $C_1 = \frac{1}{2\times\pi\times R_1\times f_l} = \frac{1}{2\times\pi\times 1 \ k\Omega\times 16Hz} = 9.94\mu F \approx 10\mu F$ (Standard Value)

4. Choose a value for f_{div}, then calculate C_2.
   $f_{div} = 6.4Hz$

   $R_{div} = \frac{R_2 \times R_3}{R_2 + R_3} = \frac{4.99k\Omega \times 4.99k\Omega}{4.99k\Omega + 4.99k\Omega} = 2.495k\Omega$

   $C_2 = \frac{1}{2\times\pi\times R_{div}\times f_{div}} = \frac{1}{2\times\pi\times 2.495k\Omega\times 6.4Hz} = 9.96\mu F \approx 10\mu F$ (Standard Value)

5. The upper cutoff frequency, f_h, is set by the noise gain of this circuit and the gain bandwidth (GBW) of the device (LMV981).
   $GBW = 1.5MHz$

   $G_{noise} = 1 + \frac{R_4}{R_1} = 1 + \frac{10k\Omega}{1 \ k\Omega} = 11\frac{V}{V}$

   $f_h = \frac{GBW}{G_{noise}} = \frac{1.5MHz}{11\frac{V}{V}} = 136.3kHz$

Design Simulations
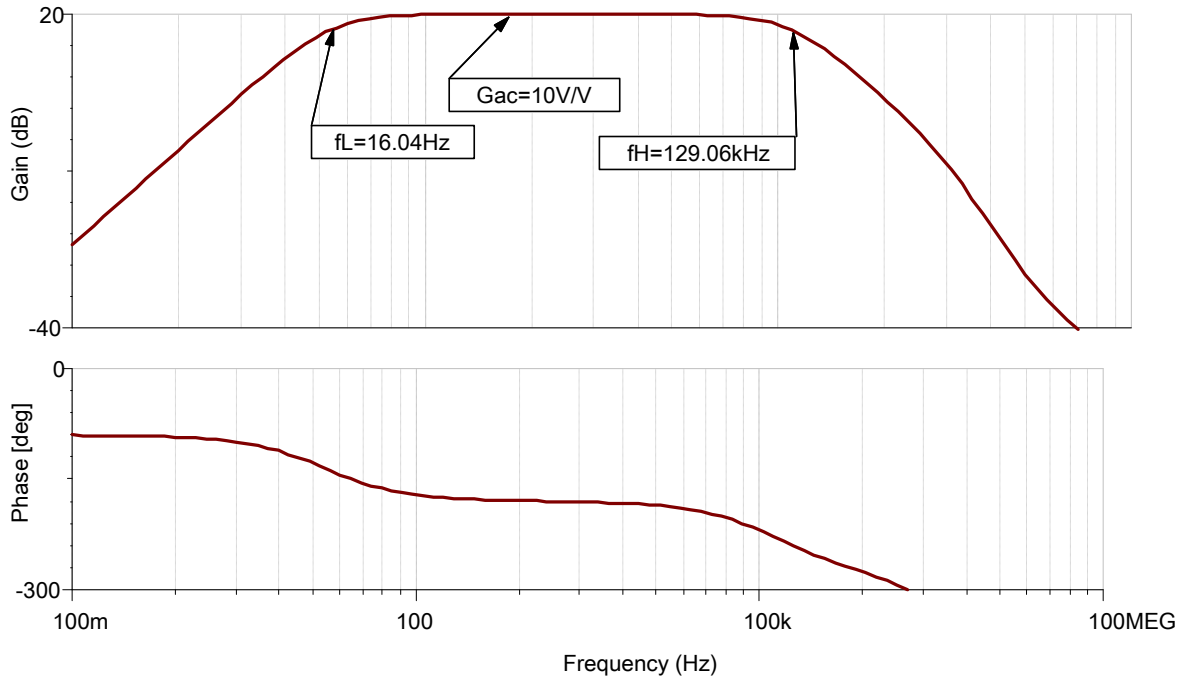
AC Simulation Results

Transient Simulation Results

AC Coupled (HPF) Inverting Amplifier Circuit
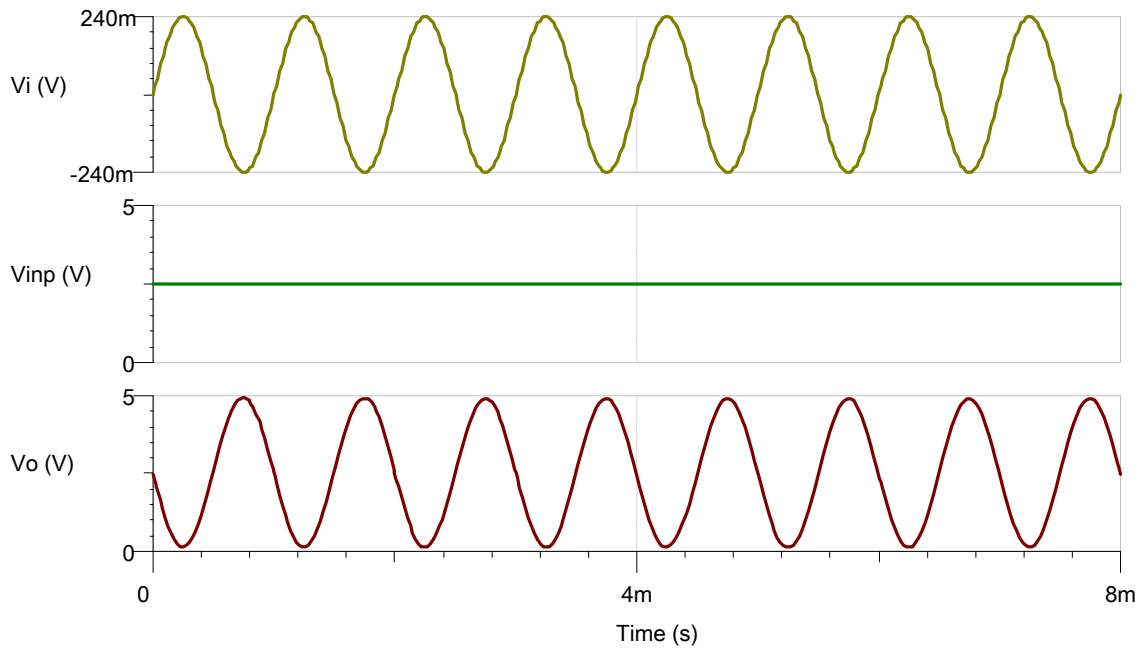
Design References

See TIPD185, www.ti.com/tool/tipd185.

Design Featured Op Amp

LMV981	
V_{cc}	1.8V to 5V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	1mV
I_q	116µA
I_b	14nA
UGBW	1.5MHz
SR	0.42V/µs
#Channels	1, 2
www.ti.com/product/lmv981-n	

Design Alternate Op Amp

LMV771	
V_{cc}	2.7V to 5V
V_{inCM}	V_{ee} to (V_{cc}–0.9V)
V_{out}	Rail-to-rail
V_{os}	0.25mV
I_q	600µA
I_b	–0.23pA
UGBW	3.5MHz
SR	1.5V/µs
#Channels	1, 2
www.ti.com/product/lmv771	

AC Coupled (HPF) Non-Inverting Amplifier Circuit

Design Goals

Input		Output		Supply		
V_{iMin}	V_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}	V_{ref}
−240mV	240mV	0.1V	4.9V	5V	0V	5V

Lower Cutoff Freq. (f_L)	Upper Cutoff Freq. (f_H)	AC Gain (G_{ac})
16Hz	≥ 1MHz	10V/V

Design Description

This circuit amplifies an AC signal, and shifts the output signal so that it is centered at one-half the power supply voltage. Note that the input signal has zero DC offset so it swings above and below ground. The key benefit of this circuit is that it accepts signals which swing below ground even though the amplifier does not have a negative power supply.
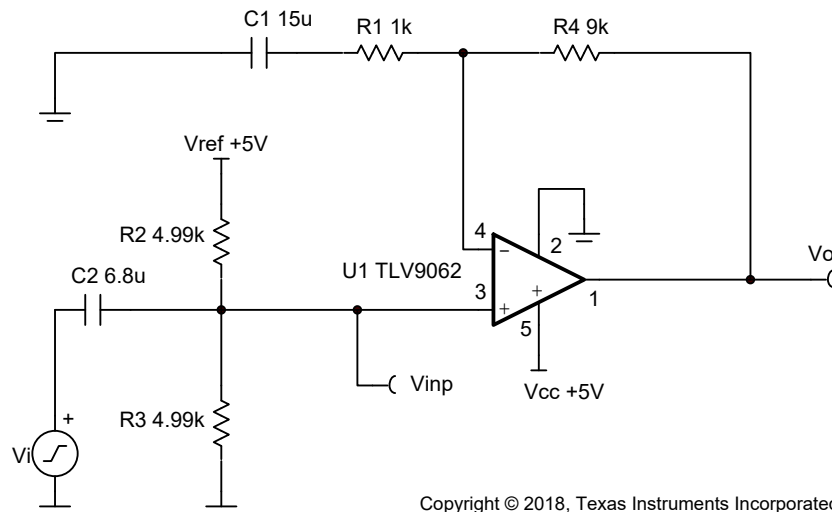
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Design Notes

1. The voltage at V_{inp} sets the input common-mode voltage.
2. R_2 and R_3 load the input signal for AC frequencies.
3. Use low feedback resistance for low noise.
4. Set the output range based on linear output swing (see A_{ol} specification of op amp).
5. The circuit has two real poles that determine the high-pass filter −3dB frequency. Set them both to $f_L/1.557$ to achieve −3dB at the lower cutoff frequency (f_L).

Design Steps

1. Select R_1 and R_4 to set the AC voltage gain.
   $R_1 = 1\ k\Omega$ (Standard Value)

   $$R_4 = R_1 \times (G_{ac} - 1) = 1\ k\Omega \times \left(10\frac{V}{V} - 1\right) = 9k\Omega \text{ (Standard Value)}$$

2. Select R_2 and R_3 to set the DC output voltage (V_{DC}) to 2.5V, or mid–supply.
   $R_3 = 4.99k\Omega$ (Standard Value)

   $$R_2 = \frac{R_3 \times V_{ref}}{V_{DC}} - R_3 = \frac{4.99k\Omega \times 5V}{2.5V} - 4.99k\Omega = 4.99k\Omega$$

3. Select C_1 based on f_L and R_1.
   $f_L = 16Hz$

   $$C_1 = \frac{1}{2\times\pi\times R_1 \times \left(\frac{f_L}{1.557}\right)} = \frac{1}{2\times\pi\times 1\ k\Omega \times 10.3Hz} = 15.5\mu F \approx 15\mu F \text{ (Standard Value)}$$

4. Select C_2 based on f_L, R_2, and R_3.

   $$R_{div} = \frac{R_2 \times R_3}{R_2 + R_3} = \frac{4.99k\Omega \times 4.99k\Omega}{4.99k\Omega + 4.99k\Omega} = 2.495k\Omega$$

   $$C_2 = \frac{1}{2\times\pi\times R_{div} \times \left(\frac{f_L}{1.557}\right)} = \frac{1}{2\times\pi\times 2.495k\Omega \times 10.3Hz} = 6.4\mu F \rightarrow 6.8\mu F (StandardValue)$$

5. The upper cutoff frequency (f_H) is set by the non-inverting gain of this circuit and the gain bandwidth (GBW) of the device (TLV9062).

   $$f_H = \frac{\text{GBW of TLV9062}}{G_{ac}} = \frac{10MHz}{10\frac{V}{V}} = 1\ MHz$$

Design Simulations

AC Simulation Results

fL = 15.6Hz   Gac = 10V/V   fH = 1.02MHz

Transient Simulation Results

Vinp = +/-240mV @ 2.5Vdc

AC Coupled (HPF) Non-Inverting Amplifier Circuit

Design References

See TIPD185, www.ti.com/tool/tipd185.

Design Featured Op Amp

TLV9062	
V_{cc}	1.8V to 5.5V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	300μV
I_q	538μA
I_b	0.5pA
UGBW	10MHz
SR	6.5V/μs
#Channels	1, 2, 4
www.ti.com/product/tlv9062	

Design Alternate Op Amp

OPA192	
V_{cc}	4.5V to 36V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	5μV
I_q	1mA/Ch
I_b	5pA
UGBW	10MHz
SR	20V/μs
#Channels	1, 2, 4
www.ti.com/product/opa192	

Band Pass Filtered Inverting Attenuator Circuit

Design Goals

Input		Output		Supply		
V_{iMin}	V_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}	V_{ref}
$100mV_{pp}$	$50V_{pp}$	$1mV_{pp}$	$500mV_{pp}$	15V	−15V	0V

Design Description

This tunable band-pass attenuator reduces signal level by –40dB over the frequency range from 10Hz to 100kHz. It also allows for independent control of the DC output level. For this design, the pole frequencies were selected outside the pass band to minimize attenuation within the specified bandwidth range.

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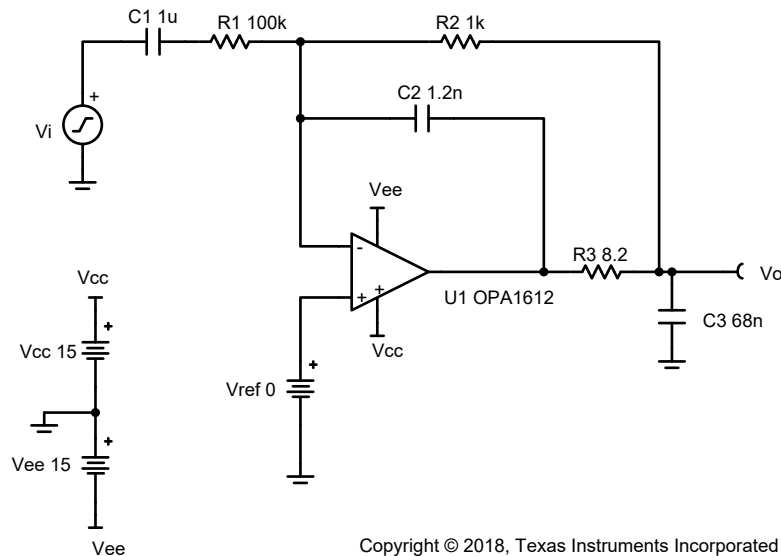
Design Notes

1. If a DC voltage is applied to V_{ref} be sure to check common mode limitations.
2. Keep R_3 as small as possible to avoid loading issues while maintaining stability.
3. Keep the frequency of the second pole in the low-pass filter (f_{p3}) at least twice the frequency of the first low-pass filter pole (f_{p2}).

Design Steps

1. Set the passband gain.

$$\text{Gain} = -\frac{R_2}{R_1} = -0.01 \frac{V}{V} \; (-40\text{dB})$$

$R_1 = 100\text{k}\Omega$

$R_2 = 0.01 \times R_1 = 1 \; \text{k}\Omega$

2. Set high-pass filter pole frequency (f_{p1}) below f_l.

$f_l = 10\text{Hz}, f_{p1} = 2.5 \; \text{Hz}$

3. Set low-pass filter pole frequency (f_{p2} and f_{p3}) above f_h.

$f_h = 100\text{kHz}$

$f_{p2} = 150\text{kHz}$

$f_{p3} \geq 2 \times f_{p2} = 300\text{kHz}$

$f_{p3} = 300\text{kHz}$

4. Calculate C_1 to set the location of f_{p1}.

$$C_1 = \frac{1}{2\pi \times R_1 \times f_{p1}} = \frac{1}{2\pi \times 100\text{k}\Omega \times 2.5\text{Hz}} = 0.636 \; \mu F \approx 1 \; \mu F \text{ (Standard Value)}$$

5. Select components to set f_{p2} and f_{p3}.

$R_3 = 8.2\Omega$ (provides stability for cap loads up to 100nF)

$$C_2 = \frac{1}{2\pi \times (R_2 + R_3) \times f_{p2}} = \frac{1}{2\pi \times 1008.2\Omega \times 150\text{kHz}}$$

$$= 1052\text{pF} \approx 1200\text{pF} \text{ (Standard Value)}$$

$$C_3 = \frac{1}{2\pi \times R_3 \times f_{p3}} = \frac{1}{2\pi \times 8.2\Omega \times 300\text{kHz}} = 64.7 \; \text{nF} \approx 68\text{nF} \text{ (Standard Value)}$$

Design Simulations

DC Simulation Results

The amplifier will pass DC voltages applied to the noninverting pin up to the common mode limitations of the op amp (±13V in this design)

AC Simulation Results
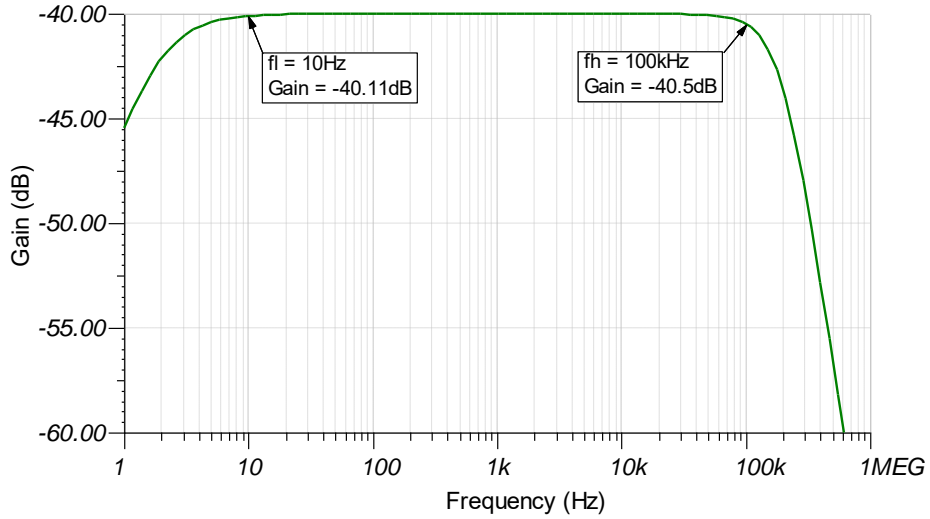
Transient Simulation Results
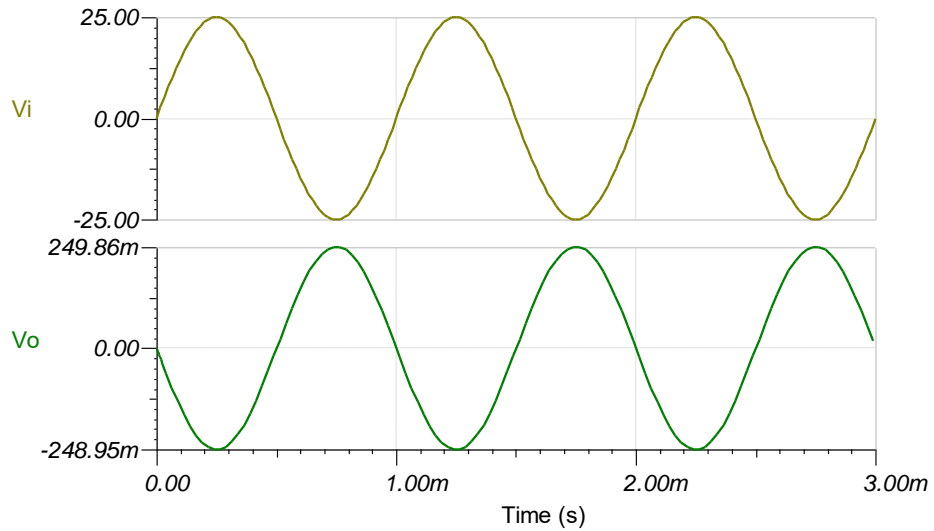
Design References

See TIPD118, www.ti.com/tool/tipd118.

Design Featured Op Amp

OPA1612	
V_{ss}	4.5V to 36V
V_{inCM}	V_{ee}+2V to V_{cc}–2V
V_{out}	V_{ee}+0.2V to V_{cc}–0.2V
V_{os}	100µV
I_q	3.6mA/Ch
I_b	60nA
UGBW	40MHz
SR	27V/µs
#Channels	1, 2
www.ti.com/product/opa1612	

Design Alternate Op Amp

OPA172	
V_{ss}	4.5V to 36V
V_{inCM}	V_{ee}–100mV to V_{cc}–2V
V_{out}	Rail-to-rail
V_{os}	200µV
I_q	1.6mA/Ch
I_b	8pA
UGBW	10MHz
SR	10V/µs
#Channels	1, 2, 4
www.ti.com/product/opa172	

Half-Wave Rectifier Circuit

Design Goals

Input		Output		Supply	
V_{iMin}	V_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}
$\pm0.2mV_{pp}$	$\pm4V_{pp}$	$0.1V_p$	$2V_p$	2.5V	–2.5V

Design Description

The precision half-wave rectifier inverts and transfers only the negative-half input of a time varying input signal (preferably sinusoidal) to its output. By appropriately selecting the feedback resistor values, different gains can be achieved. Precision half-wave rectifiers are commonly used with other op amp circuits such as a peak-detector or bandwidth limited non-inverting amplifier to produce a DC output voltage. This configuration has been designed to work for sinusoidal input signals between $0.2mV_{pp}$ and $4V_{pp}$ at frequencies up to 50kHz.
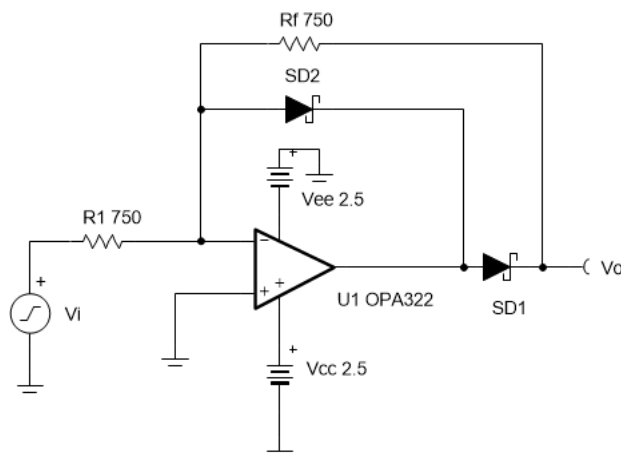
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Design Notes

1. Select an op amp with a high slew rate. When the input signal changes polarities, the amplifier output must slew two diode voltage drops.
2. Set output range based on linear output swing (see A_{ol} specification).
3. Use fast switching diodes. High-frequency input signals will be distorted depending on the speed by which the diodes can transition from blocking to forward conducting mode. Schottky diodes might be a preferable choice, since these have faster transitions than pn-junction diodes at the expense of higher reverse leakage.
4. The resistor tolerance sets the circuit gain error.
5. Minimize noise errors by selecting low-value resistors.

Design Steps

1. Set the desired gain of the half-wave rectifier to select the feedback resistors.

$$V_o = Gain \times V_i$$

$$Gain = -\frac{R_f}{R_1} = -1$$

$$R_f = R_1 = 2 \times R_{eq}$$

- Where R_{eq} is the parallel combination of R_1 and R_f

2. Select the resistors such that the resistor noise is negligible compared to the voltage broadband noise of the op amp.

$$E_{nr} = \sqrt{4 \times k_b \times T \times R_{eq}}$$

$$R_{eq} \leq \frac{E_{nbb}^2}{4 \times k_b \times T \times 3^2} = (Enbb)$$

$$= 7.5 \frac{nV}{\sqrt{Hz}} = \frac{\left(7.5 \times 10^{-9}\right)^2}{4 \times 1.381 \times 10^{-23} \times 298 \times 3^2} = 380\Omega$$

$$R_f = R_1 \leq 760\Omega \rightarrow 750\Omega \text{ (Standard Value)}$$

Design Simulations

DC Simulation Results
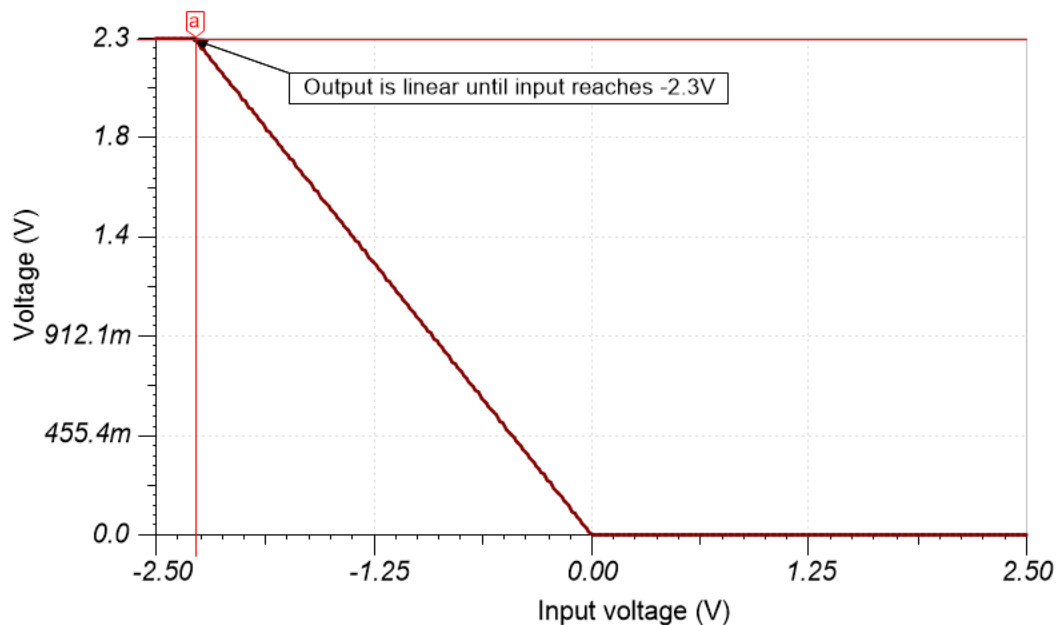
Transient Simulation Results
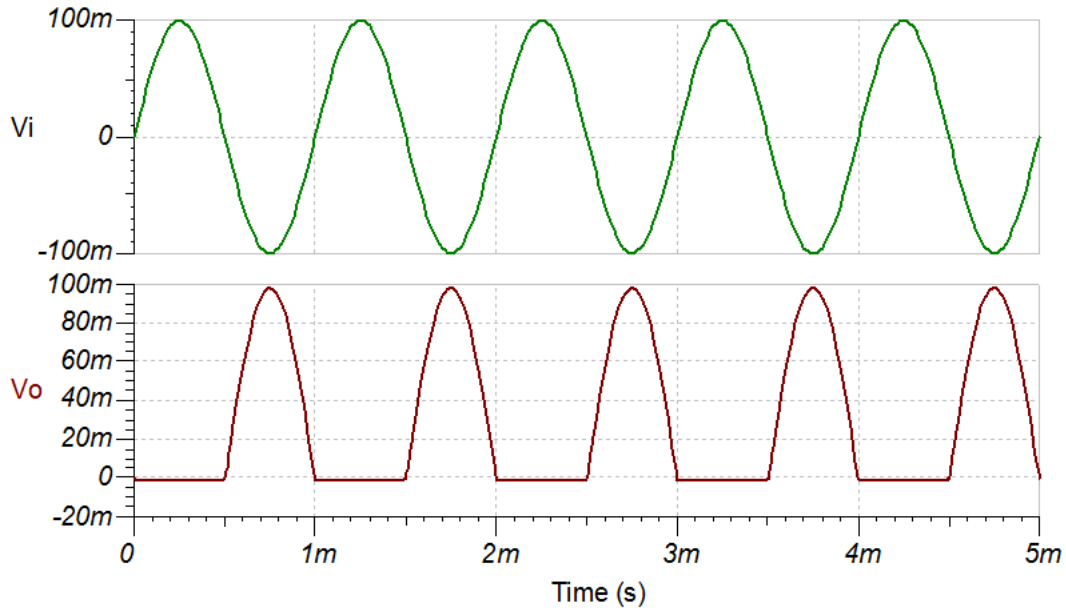
200mV$_{pp}$ at 1kHz

2V$_{pp}$ at 50kHz

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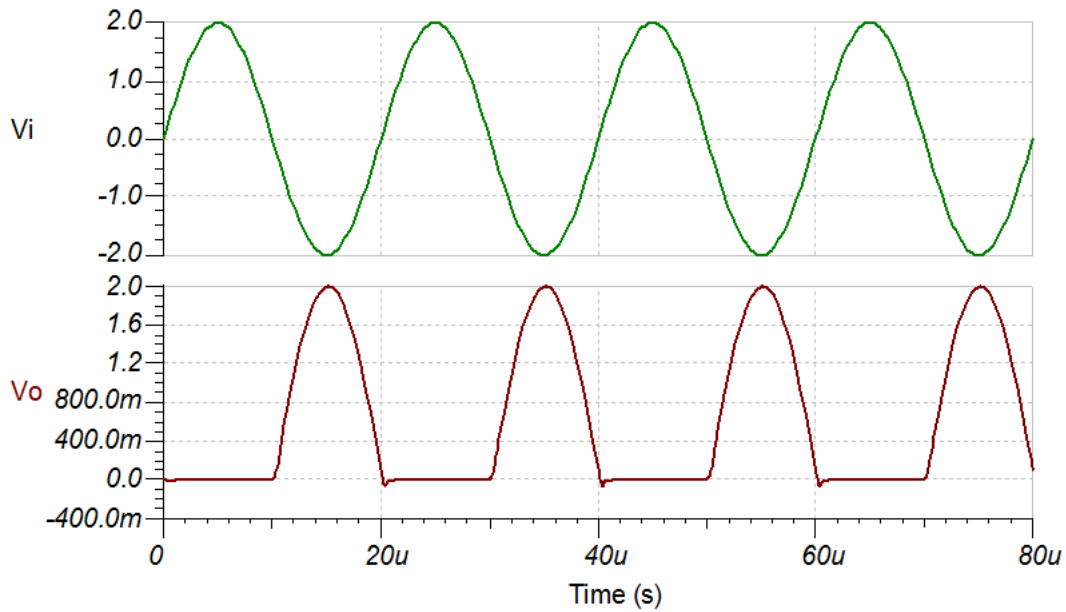
Design Featured Op Amp

OPA322	
V_{ss}	1.8V to 5.5V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	500µV
I_q	1.6mA/Ch
I_b	0.2pA
UGBW	20MHz
SR	10V/µs
#Channels	1, 2, 4
www.ti.com/product/opa322	

Design Alternate Op Amp

OPA2325	
V_{ss}	2.2V to 5.5V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	40µV
I_q	0.65mA/Ch
I_b	0.2pA
UGBW	10MHz
SR	5V/µs
#Channels	2µ
www.ti.com/product/opa2325	

Full-Wave Rectifier Circuit

Design Goals

Input		Output		Supply		
V_{iMin}	V_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}	V_{ref}
±25mV	±10V	25mV	10V	15V	−15V	0V

Design Description

This absolute value circuit can turn alternating current (AC) signals to single polarity signals. This circuit functions with limited distortion for ±10-V input signals at frequencies up to 50kHz and for signals as small as ±25mV at frequencies up to 1kHz.
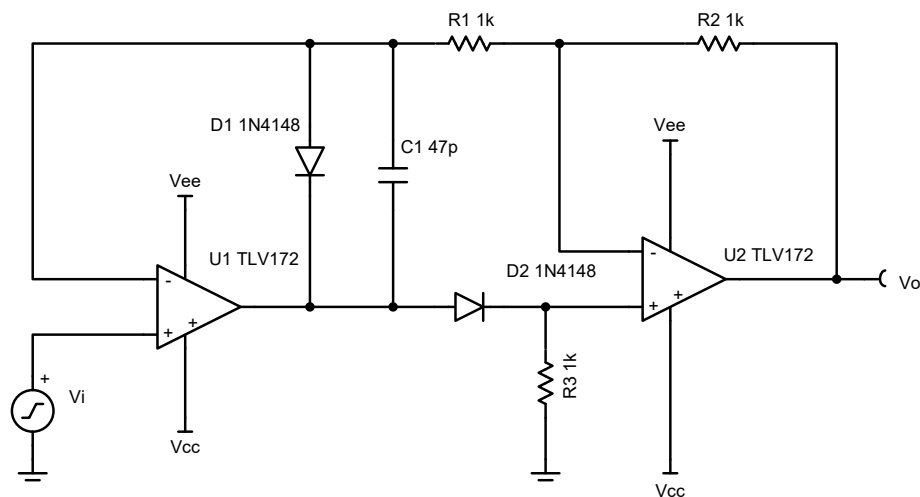
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Design Notes

1. Be sure to select an op amp with sufficient bandwidth and a high slew rate.
2. For greater precision look for an op amp with low offset voltage, low noise, and low total harmonic distortion (THD).
3. The resistors were selected to be 0.1% tolerance to reduce gain error.
4. Selecting too large of a capacitor C_1 will cause large distortion on the transition edges when the input signal changes polarity. C_1 may not be required for all op amps.
5. Use a fast switching diode.

Design Steps

1. Select gain resistors.

   a. Gain for positive input signals.

   $$\frac{V_o}{V_i} = 1\frac{V}{V}$$

   b. Gain for negative input signals.

   $$\frac{V_o}{V_i} = -\frac{R_2}{R_1} = -1\frac{V}{V}$$

2. Select R_1 and R_2 to reduce thermal noise and to minimize voltage drops due to the reverse leakage current of the diode. These resistors will appear as loads to U_1 and U_2 during negative input signals.

   $$R_1 = R_2 = 1 \ k\Omega$$

3. R_3 biases the non-inverting node of U_2 to GND during negative input signals. Select R_3 to be the same value as R_1 and R_2. U_1 must be able to drive the R_3 load during positive input signals.

   $$R_3 = 1 \ k\Omega$$

4. Select C_1 based on the desired transient response. See the *Design Reference* section for more information.

   $$C_1 = 47pF$$

Design Simulations

Transient Simulation Results
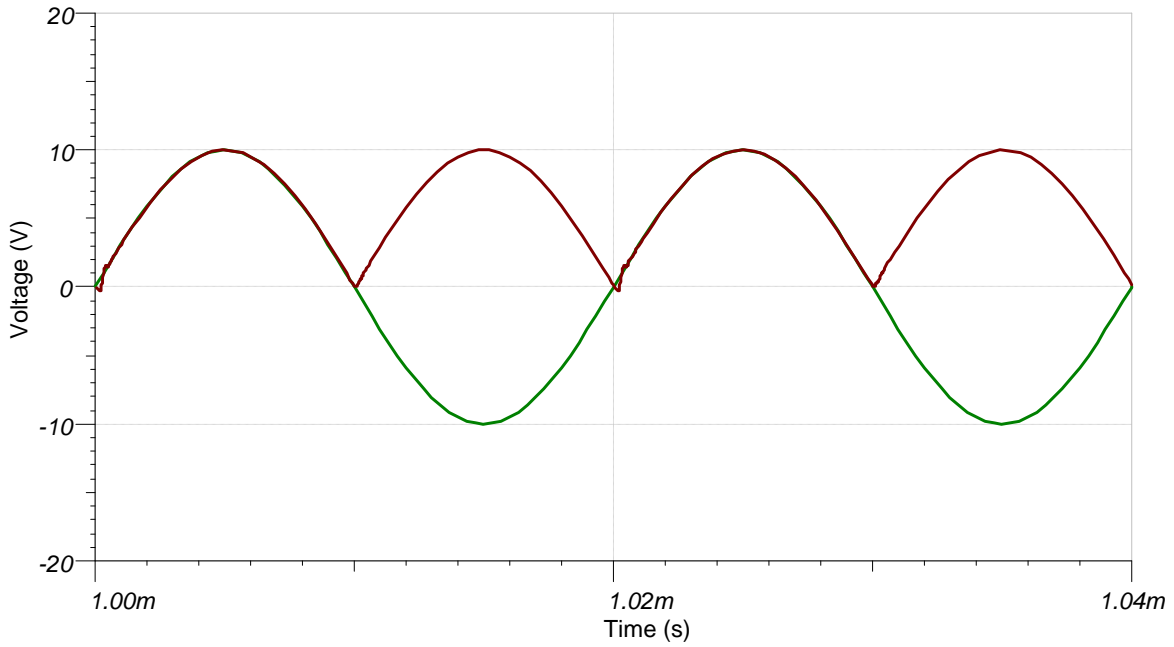
±10V at 50-kHz Input
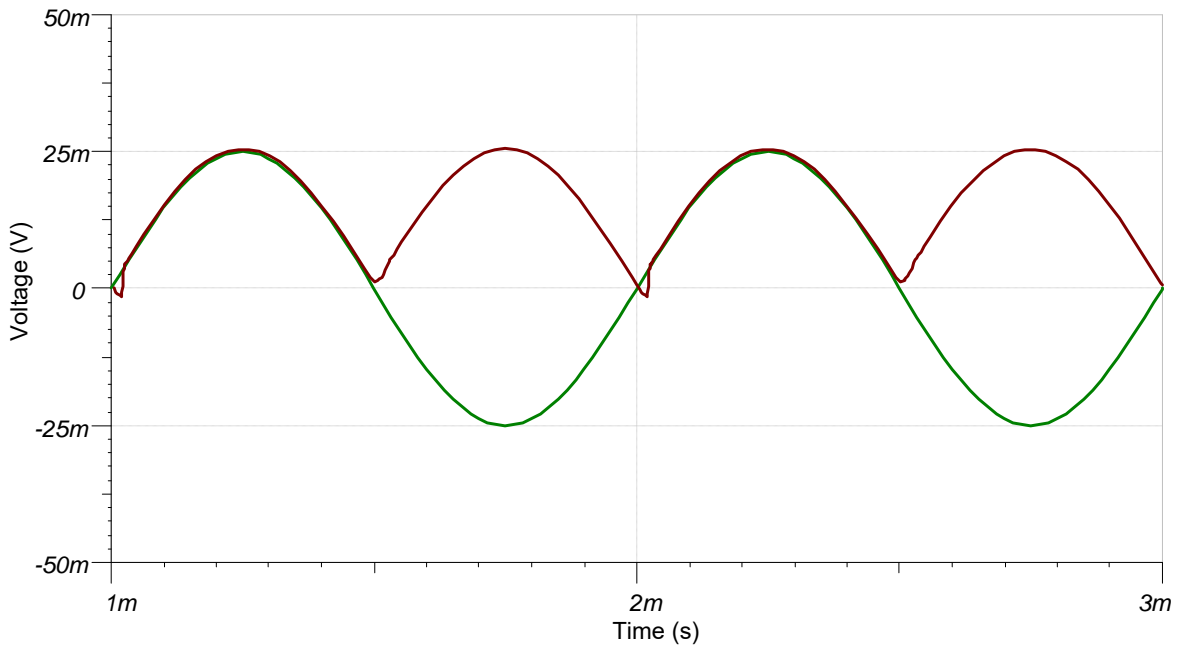
±25mV at 1-kHz Input

Design References

See TIPD139, www.ti.com/tool/tipd139.

Design Featured Op Amp

TLV172	
V_{cc}	4.5V to 36V
V_{inCM}	Vee to (Vcc–2V)
V_{out}	Rail-to-rail
V_{os}	0.5mV
I_q	1.6mA/Ch
I_b	10pA
UGBW	10MHz
SR	10V/µs
#Channels	1, 2, 4
www.ti.com/product/tlv172	

Design Alternate Op Amp

OPA197	
V_{cc}	4.5V to 36V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	25µV
I_q	1mA/Ch
I_b	5pA
UGBW	10MHz
SR	20V/µs
#Channels	1, 2, 4
www.ti.com/product/opa197	

Single-Supply, Low-Input Voltage Full-Wave Rectifier Circuit

Design Goals

Input		Output		Supply		
V_{iMin}	V_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}	V_{ref}
5mVpp	400mVpp	2.5mVpp	200mVpp	5V	−0.23V	0V

Design Description

This single-supply precision absolute value circuit is optimized for low-input voltages. It is designed to function up to 50kHz and has excellent linearity at signal levels as low as 5mVpp. The design uses a negative charge pump (such as LM7705) on the negative op amp supply rails to maintain linearity with signal levels near 0V.
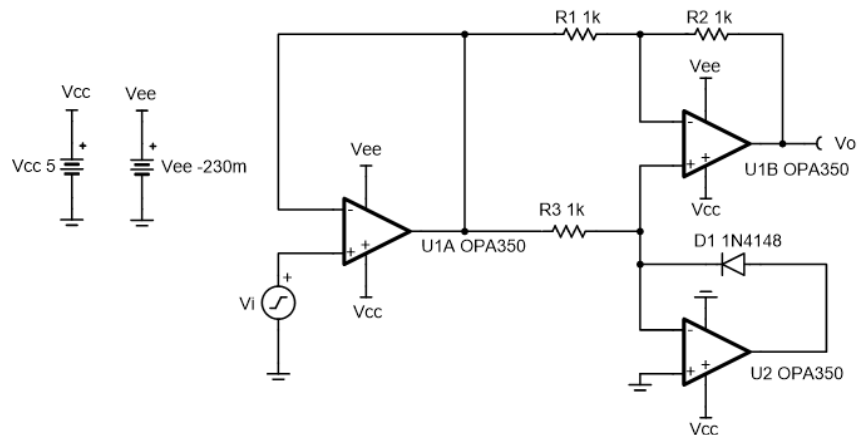
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Design Notes

1. Observe common-mode and output swing limitations of op amps.
2. R_3 should be sized small enough that the leakage current from D_1 does not cause errors in positive input cycles while ensuring the op amp can drive the load.
3. Use a fast switching diode for D_1.
4. Removing the input buffer will allow for input signals with peak-to-peak values twice as large as the supply voltage at the expense of lower input impedance and slight gain error.
5. Use precision resistors to minimize gain error.

Design Steps

1. Circuit analysis for positive input signals.
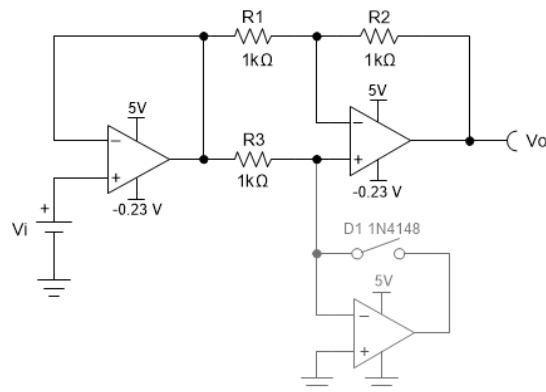
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$$\frac{V_o}{V_i} = \left(-\frac{R_2}{R_1}\right) + \left(1 + \frac{R_2}{R_1}\right) = 1$$

$$V_o = V_i$$

2. Circuit analysis for negative input signals.
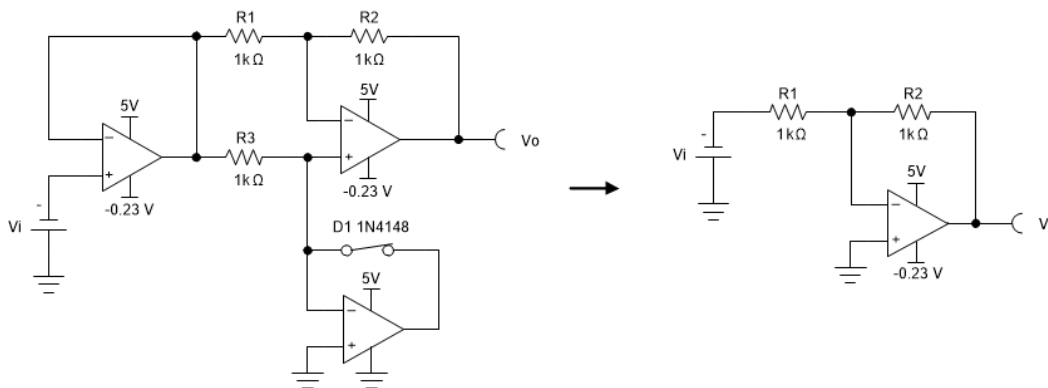
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$$\frac{V_o}{V_i} = \left(-\frac{R_2}{R_1}\right) = -1$$

$$V_o = -V_i$$

3. Select R_1, R_2, and R_3.

$$\frac{V_o}{V_i} = -\frac{R_2}{R_1}$$

If $R_2 = R_1$ then $V_o = -V_i$

Set $R_1 = R_2 = R_3 = 1$ kΩ

Design Simulations

Transient Simulation Results
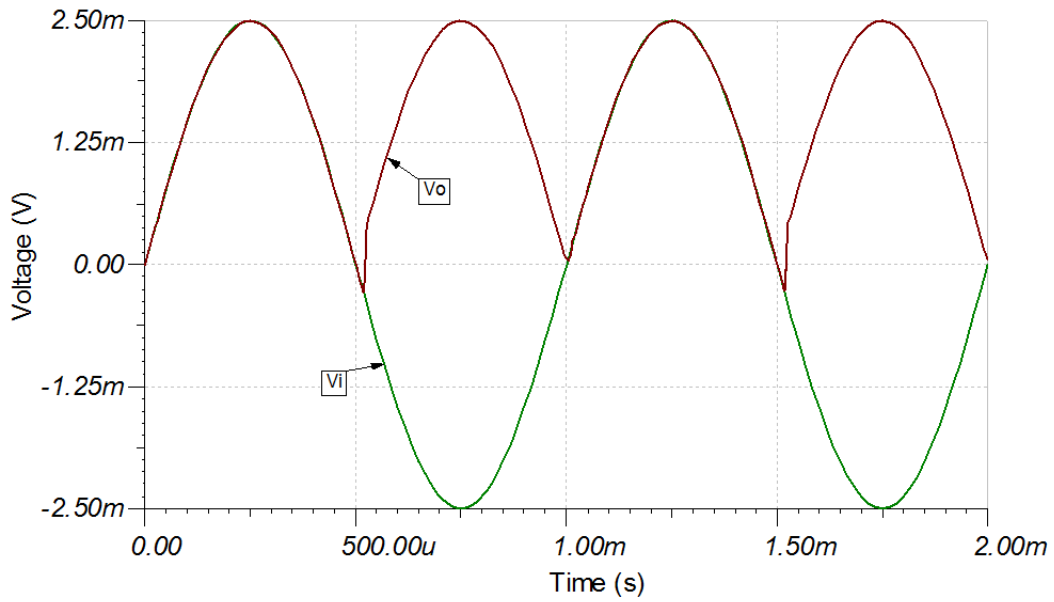
5mVpp at 1-kHz Input
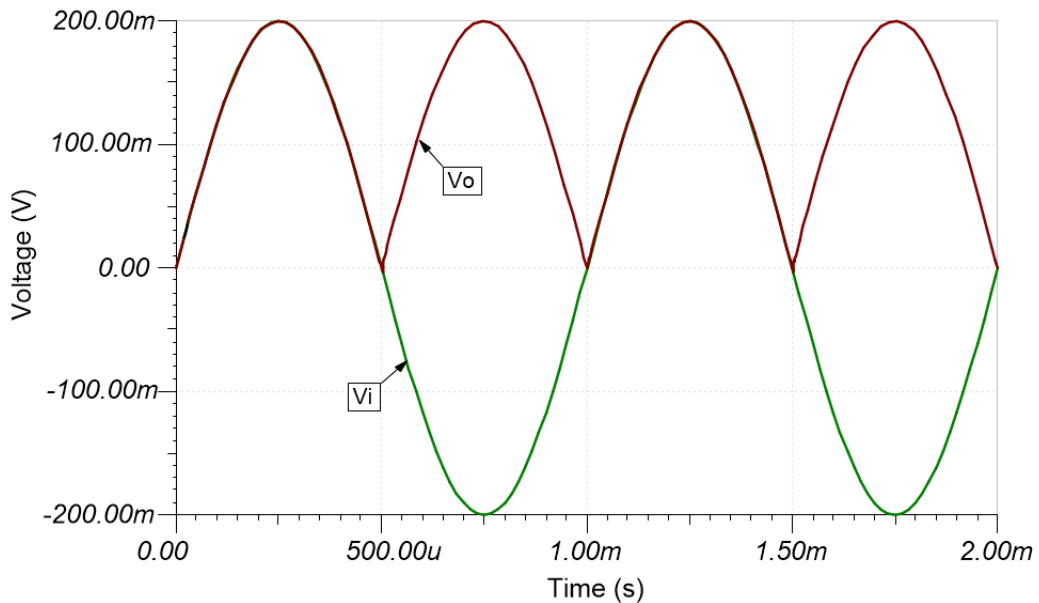
400mVpp at 1-kHz Input

Design References

See TIPD124, www.ti.com/tool/tipd124.

Design Featured Op Amp

OPA350	
V_{ss}	2.7V to 5.5V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	150µV
I_q	5.2mA/Ch
I_b	0.5pA
UGBW	38MHz
SR	22V/µs
#Channels	1, 2, 4
www.ti.com/product/opa350	

Design Alternate Op Amp

OPA353	
V_{ss}	2.7V to 5.5V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	3mV
I_q	5.2mA
I_b	0.5pA
UGBW	44MHz
SR	22V/µs
#Channels	1, 2, 4
www.ti.com/product/opa353	

Slew Rate Limiter Circuit

Design Goals

Input		Output		Supply		
V_{iMin}	V_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}	V_{ref}
−10V	10V	−10V	10V	15V	−15V	0V

Design Description

This circuit controls the slew rate of an analog gain stage. This circuit is intended for symmetrical slew rate applications. The desired slew rate must be slower than that of the op amp chosen to implement the slew rate limiter.
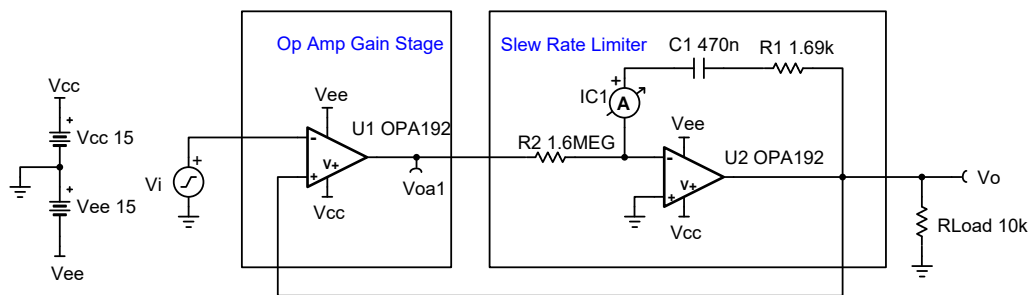
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Design Notes

1. The gain stage op-amp and slew rate limiting op amp should both be checked for stability.
2. Verify that the current demands for charging or discharging C_1 plus any load current out of U_2 will not limit the voltage swing of U_2.

Design Steps

1. Set slew rate and choose a standard value for the feedback capacitor, C_1.

$$C_1 = 470nF$$

$$SR = 20\frac{V}{s}$$

2. Choose the value of R_2 to set the capacitor current necessary for the desired slew rate.

$$SR = \frac{I_{C_1}}{C_1}$$

$$20\frac{V}{s} = \frac{I_{C_1}}{470nF} \text{ where } I_{C_1} = 9.4\ \mu A$$

Gain stage op amp $V_{sat} = \pm 14.995$ (typical)

$$I_{C_1} = \frac{V_{sat}}{R_2}$$

$$9.4\ \mu A = \frac{14.995V}{R_2}, \text{ so } R_2 = 1.595\ M\Omega \approx 1.6M\Omega \text{ (Standard Value)}$$

3. Compensate feedback network for stability. R_1 adds a pole to the $1/\beta$ network. This pole should be placed so that the $1/\beta$ curve levels off a decade before it intersects the open loop gain curve (200Hz, for this example).

$$f_p = \frac{1}{2\pi \times R_1 \times C_1} = 200Hz$$

$$200Hz = \frac{1}{2\pi \times R_1 \times 470nF}, \text{ so } R_1 = 1.693\ k\Omega \approx 1.69k\Omega \text{ (Standard Value)}$$

Design Simulations

Transient Simulation Results
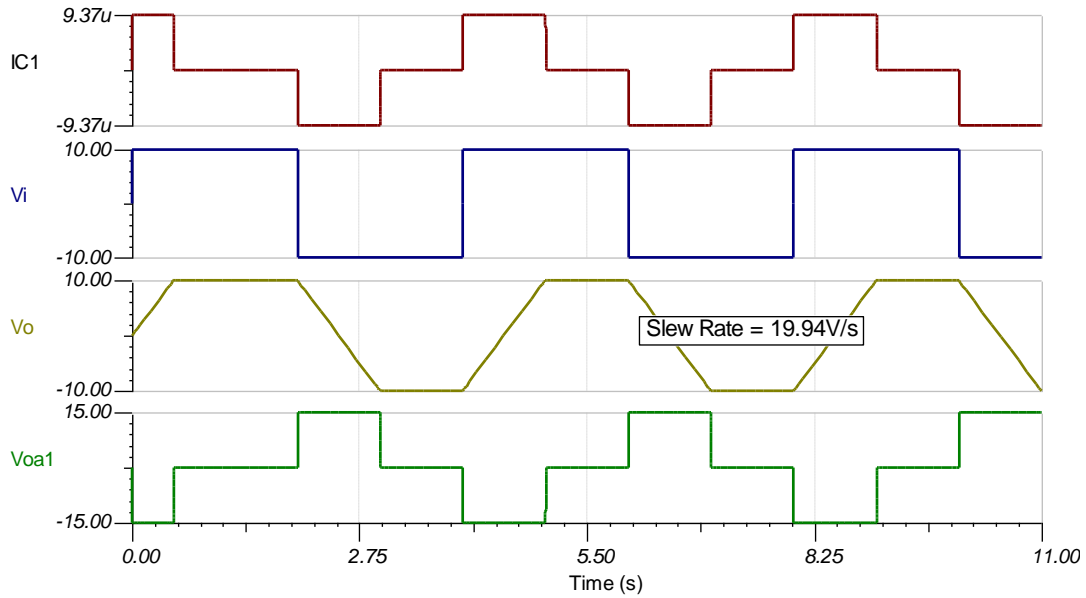
AC Simulation Results
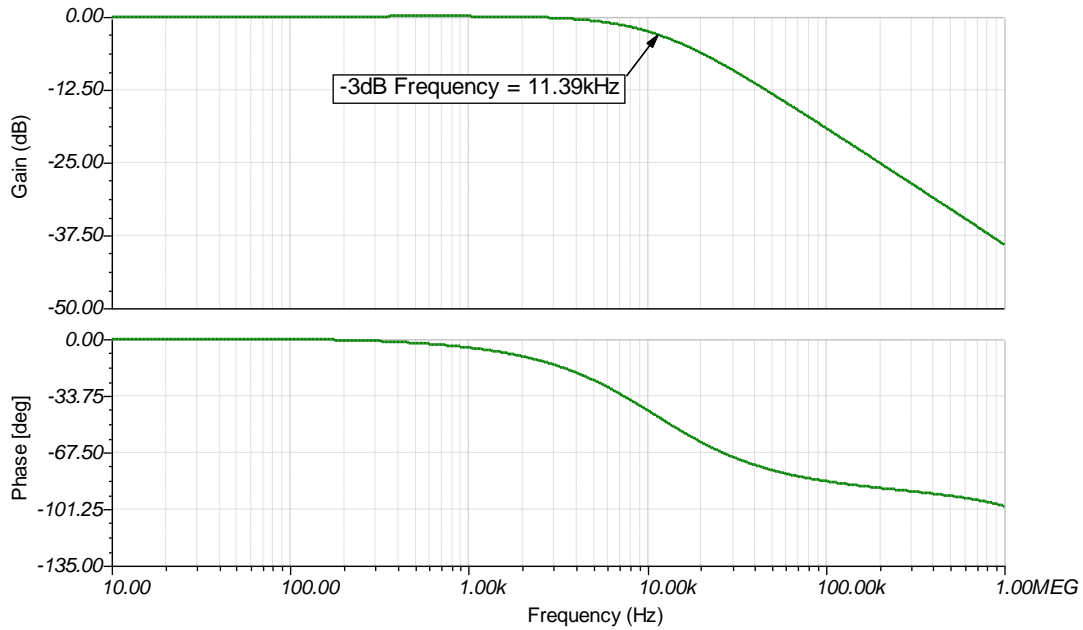
Design References

See TIPD140, www.ti.com/tool/tipd140.

Design Featured Op Amp

OPA192	
V_{cc}	4.5V to 36V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	5µV
I_q	1mA/Ch
I_b	5pA
UGBW	10MHz
SR	20V/µs
#Channels	1, 2, 4
www.ti.com/product/opa192	

Design Alternate Op Amp

TLV2372	
V_{cc}	2.7V to 16V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	2mV
I_q	750µA/Ch
I_b	1pA
UGBW	3MHz
SR	2.1V/µs
#Channels	1, 2, 4
www.ti.com/product/tlv2372	

Single-Ended Input to Differential Output Circuit

Design Goals

Input		Output		Supply		
V_{iMin}	V_{iMax}	$V_{oDiffMin}$	$V_{oDiffMax}$	V_{cc}	V_{ee}	V_{ref}
0.1V	2.4V	−2.3V	2.3V	2.7V	0V	2.5V

Design Description

This circuit converts a single ended input of 0.1V to 2.4V into a differential output of ±2.3V on a single 2.7-V supply. The input and output ranges can be scaled as necessary as long as the op amp input common-mode range and output swing limits are met.
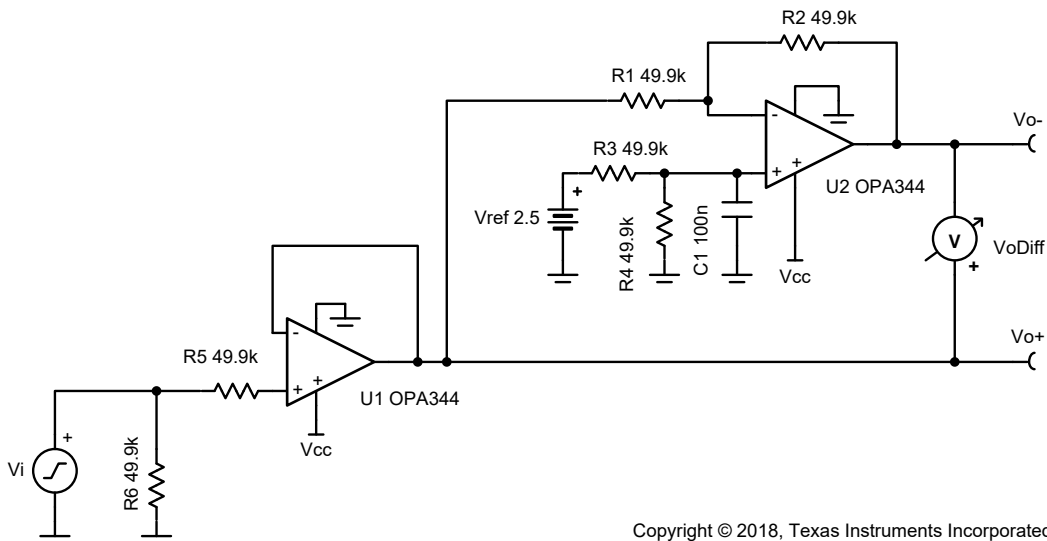
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Design Notes

1. Op amps with rail-to-rail input and output will maximize the input and output range of the circuit.
2. Op amps with low V_{os} and offset drift will reduce DC errors.
3. Use low tolerance resistors to minimize gain error.
4. Set output range based on linear output swing (see A_{ol} specification).
5. Keep feedback resistors low or add capacitor in parallel with R_2 for stability.

Design Steps

1. Buffer V_i signal to generate V_{o+}.

$$V_{O+} = V_i$$

2. Invert and level shift V_{o+} using a difference amplifier to create V_{o-}.

$$V_{O-} = (V_{ref} - V_{O+}) \times \left(\frac{R_2}{R_1}\right)$$

3. Select resistances so that the resistor noise is smaller than the amplifier broadband noise.

$$E_{nv} = 30 \frac{nV}{\sqrt{Hz}} \text{ (Voltage noise from op amp)}$$

If $R_1 = R_2 = R_3 = R_4 = 49.9k\Omega$ then

$$E_{nr} = \sqrt{\left(\sqrt{4 \times kB \times T \times (R_1 \| R_2)}\right)^2 + \left(\sqrt{4 \times kB \times T \times (R_3 \| R_4)}\right)^2} = 28.7 \frac{nV}{\sqrt{Hz}} \; (< E_{nv})$$

4. Select resistances that protect the input of the amplifier and prevents floating inputs. To simplify the bill of materials (BOM), select $R_5 = R_6$.

$$R_5 = R_6 = 49.9k\Omega$$

Design Simulations

DC Simulation Results

AC Simulation Results

Single-Ended Input to Differential Output Circuit
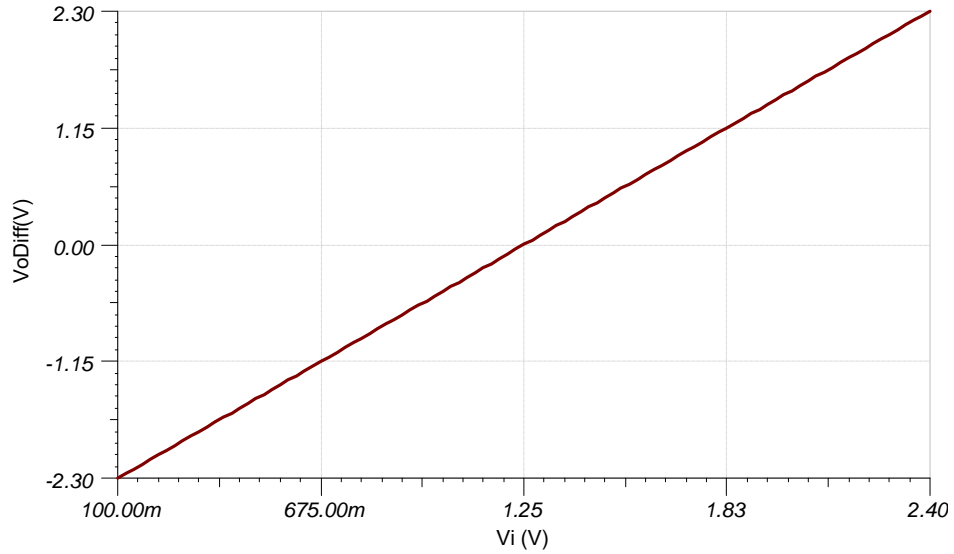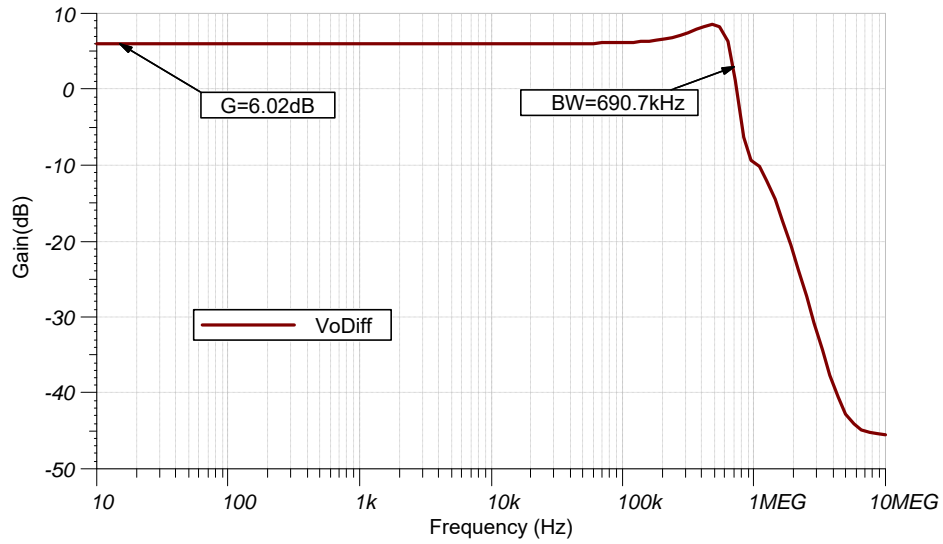
Design References

See TIPD131, www.ti.com/tool/tipd131.

Design Featured Op Amp

OPA344	
V_{ss}	1.8V to 5.5V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	0.2mV
I_q	150µA
I_b	0.2pA
UGBW	1MHz
SR	0.8V/µs
#Channels	1, 2, 4
www.ti.com/product/opa344	

Design Alternate Op Amp

OPA335	
V_{ss}	2.7V to 5.5V
V_{inCM}	V_{ee}–0.1V to V_{cc}–1.5V
V_{out}	Rail-to-rail
V_{os}	1µV
I_q	285µA/Ch
I_b	70pA
UGBW	2MHz
SR	1.6V/µs
#Channels	1, 2
www.ti.com/product/opa335	

![Texas Instruments Logo]

Inverting Op Amp With Inverting Positive Reference Voltage Circuit

Design Goals

Input		Output		Supply		
V_{iMin}	V_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}	V_{ref}
–5V	–1V	0.05V	3.3V	5V	0V	5V

Design Description

This design uses an inverting amplifier with an inverting positive reference to translate an input signal of –5V to –1V to an output voltage of 3.3V to 0.05V. This circuit can be used to translate a negative sensor output voltage to a usable ADC input voltage range.
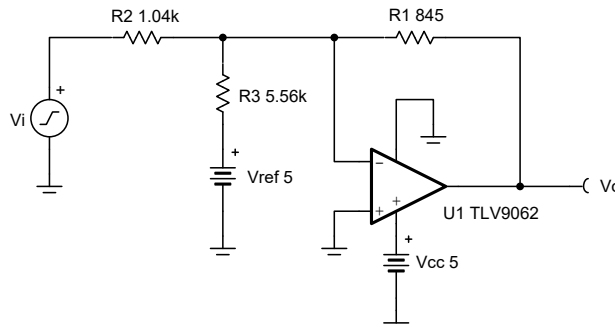
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Design Notes

1. Use op amp linear output operating range. Usually specified under A_{OL} test conditions.
2. Common mode range must extend down to or below ground.
3. V_{ref} output must be low impedance.
4. Input impedance of the circuit is equal to R_2.
5. Choose low-value resistors to use in the feedback. It is recommended to use resistor values less than 100kΩ. Using high-value resistors can degrade the phase margin of the amplifier and introduce additional noise in the circuit.
6. The cutoff frequency of the circuit is dependent on the gain bandwidth product (GBP) of the amplifier. Additional filtering can be accomplished by adding a capacitor in parallel to R_1. Adding a capacitor in parallel with R_1 will also improve stability of the circuit if high-value resistors are used.

Design Steps

$$V_o = -V_i \times \left(\frac{R_1}{R_2}\right) - V_{ref} \times \left(\frac{R_1}{R_3}\right)$$

1. Calculate the gain of the input signal.

$$G_{input} = \frac{V_{o\_max} - V_{o\_min}}{V_{i\_max} - V_{i\_min}} = \frac{3.3V - 0.05V}{-1V - (-5\ V)} = 0.8125\frac{V}{V}$$

2. Calculate R_1 and R_2.

Choose $R_1 = 845\Omega$

$$R_2 = \frac{R_1}{G_{input}} = \frac{R_1}{0.8125\frac{V}{V}} = 1.04\ \ k\Omega$$

3. Calculate the gain of the reference voltage required to offset the output.

$$G_{ref} = \frac{R_1}{R_3}$$

$$-V_{i\_min} \times \left(\frac{R_1}{R_2}\right) - V_{ref} \times \left(\frac{R_1}{R_3}\right) = V_{o\_min}$$

$$\frac{R_1}{R_3} = \frac{V_{o\_min} + V_{i\_min} \times \left(\frac{R_1}{R_2}\right)}{-V_{ref}} = \frac{0.05V + (-1\ V)\left(\frac{845\Omega}{1.04k\Omega}\right)}{-5} = 0.1525\frac{V}{V}$$

4. Calculate R_3.

$$R_3 = \frac{R_1}{G_{ref}} = \frac{845\Omega}{0.1525\frac{V}{V}} = 5.54\ \ k\Omega \approx 5.56\ \ k\Omega$$

Design Simulations
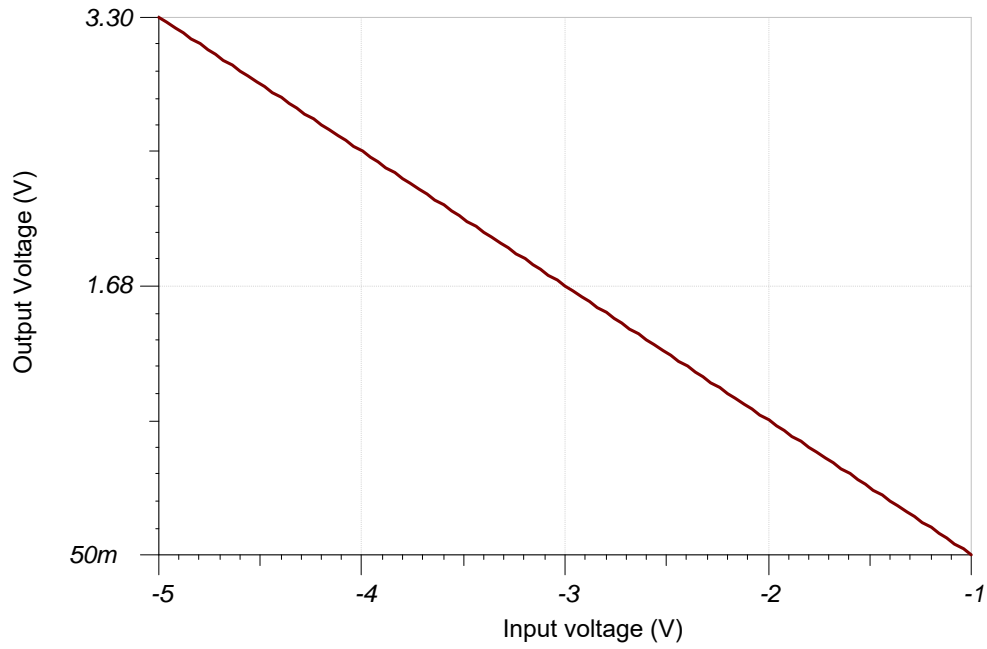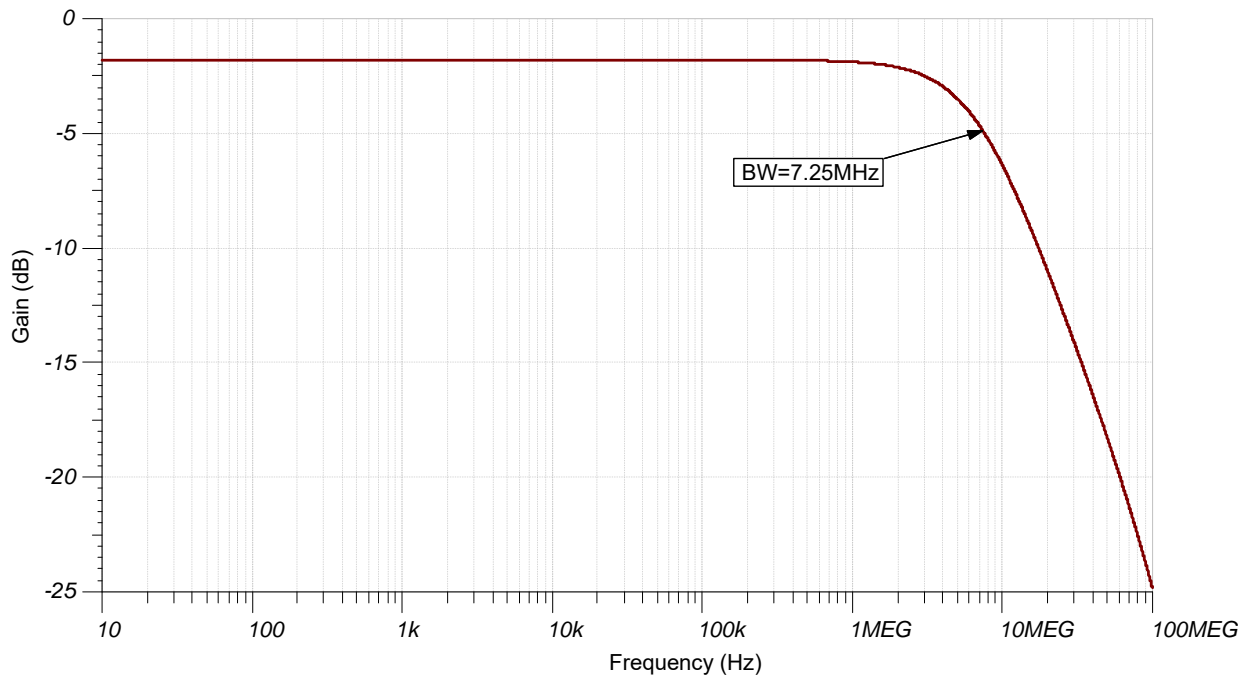
DC Simulation Results

AC Simulation Results

92
Inverting Op Amp With Inverting Positive Reference Voltage Circuit

Design References

See *Designing Gain and Offset in Thirty Seconds*.

Design Featured Op Amp

TLV9062	
V_{ss}	1.8V to 5.5V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	0.3mV
I_q	538µA
I_b	0.5pA
UGBW	10MHz
SR	6.5V/µs
#Channels	1, 2, 4
www.ti.com/product/tlv9062	

Design Alternate Op Amp

OPA197	
V_{ss}	4.5V to 36V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	25µV
I_q	1mA
I_b	5pA
UGBW	10MHz
SR	20V/µs
#Channels	1, 2, 4
www.ti.com/product/opa197	

Non-Inverting Op Amp With Inverting Positive Reference Voltage Circuit

Design Goals

Input		Output		Supply		
V_{iMin}	V_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}	V_{ref}
2V	5V	0.05V	4.95V	5V	0V	2.5V

Design Description

This design uses a non-inverting amplifier with an inverting positive reference to translate an input signal of 2V to 5V to an output voltage of 0.05V to 4.95V. This circuit can be used to translate a sensor output voltage with a positive slope and offset to a usable ADC input voltage range.
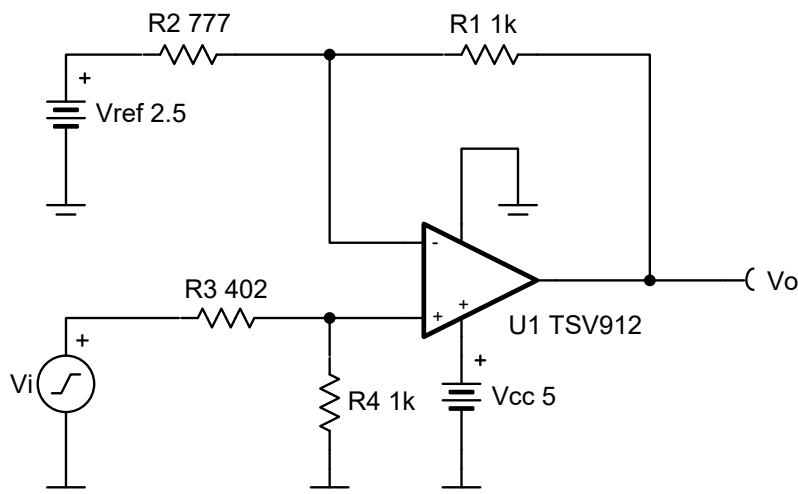
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Design Notes

1. Use op amp linear output operating range. Usually specified under A_{OL} test conditions.
2. Check op amp input common mode voltage range. The common mode voltage varies with the input voltage.
3. V_{ref} must be low impedance.
4. Input impedance of the circuit is equal to the sum of R_3 and R_4.
5. Choose low-value resistors to use in the feedback. It is recommended to use resistor values less than 100kΩ. Using high-value resistors can degrade the phase margin of the amplifier and introduce additional noise in the circuit.
6. The cutoff frequency of the circuit is dependent on the gain bandwidth product (GBP) of the amplifier.
7. Adding a capacitor in parallel with R_1 will improve stability of the circuit if high-value resistors are used.

Design Steps

$$V_o = V_i \times \left(\frac{R_4}{R_3+R_4}\right)\left(\frac{R_1+R_2}{R_2}\right) - V_{ref} \times \left(\frac{R_1}{R_2}\right)$$

1. Calculate the gain of the input to produce the largest output swing.

$$V_{o\_max} - V_{o\_min} = (V_{i\_max} - V_{i\_min})\left(\frac{R_4}{R_3+R_4}\right)\left(\frac{R_1+R_2}{R_2}\right)$$

$$\frac{V_{o\_max}-V_{o\_min}}{V_{i\_max}-V_{i\_min}} = \left(\frac{R_4}{R_3+R_4}\right)\left(\frac{R_1+R_2}{R_2}\right)$$

$$\frac{4.95V-0.05V}{5V-2V} = \left(\frac{R_4}{R_3+R_4}\right)\left(\frac{R_1+R_2}{R_2}\right)$$

$$1.633\frac{V}{V} = \left(\frac{R_4}{R_3+R_4}\right)\left(\frac{R_1+R_2}{R_2}\right)$$

2. Select a value for R_1 and R_4 and insert the values into the previous equation. The other two resistor values must be solved using a system of equations. The proper output swing and offset voltage cannot be calculated if more than two variables are selected.

$$R_1 = R_4 = 1 \text{ k}\Omega$$

$$1.633\frac{V}{V} = \left(\frac{1\,k\Omega}{R_3+1\,k\Omega}\right)\left(\frac{1\,k\Omega+R_2}{R_2}\right)$$

3. Solve the previous equation for R_3 in terms of R_2.

$$R_3 = \frac{1\,M\Omega+(1\,k\Omega \times R_2)}{1.633 \times R_2} - 1 \text{ k}\Omega$$

4. Select any point along the transfer function within the linear output range of the amplifier to set the proper offset voltage at the output (for example, the minimum input and output voltage).

$$V_{o\_min} = V_{i\_min} \times \left(\frac{R_4}{R_3+R_4}\right)\left(\frac{R_1+R_2}{R_2}\right) - V_{ref} \times \left(\frac{R_1}{R_2}\right)$$

$$0.05V = 2V \times \left(\frac{1\,k\Omega}{R_3+1\,k\Omega}\right)\left(\frac{1\,k\Omega+R_2}{R_2}\right) - V_{ref} \times \left(\frac{1\,k\Omega}{R_2}\right)$$

5. Insert R_3 from step 3 into the equation from step 4 and solve for R_2.

$$0.05V = 2V \times \left(\frac{1\,k\Omega}{\frac{1\,M\Omega+1\,k\Omega\times R_2}{1.633 \times R_2}-1\,k\Omega+1\,k\Omega}\right)\left(\frac{1\,k\Omega+R_2}{R_2}\right) - V_{ref} \times \left(\frac{1\,k\Omega}{R_2}\right)$$

$$R_2 = 777.2\Omega \approx 777\Omega$$

6. Insert R_2 calculation from step 5, and solve for R_3.

$$R_3 = \frac{1\,M\Omega+(1\,k\Omega \times R_2)}{1.633 \times R_2} - 1 \text{ k}\Omega$$

$$R_3 = \frac{1\,M\Omega+1\,k\Omega\times(777\Omega)}{1.633\times(777\Omega)} - 1 \text{ k}\Omega = 400.49\Omega \approx 402\Omega$$

Design Simulations

DC Simulation Results

AC Simulation Results

96
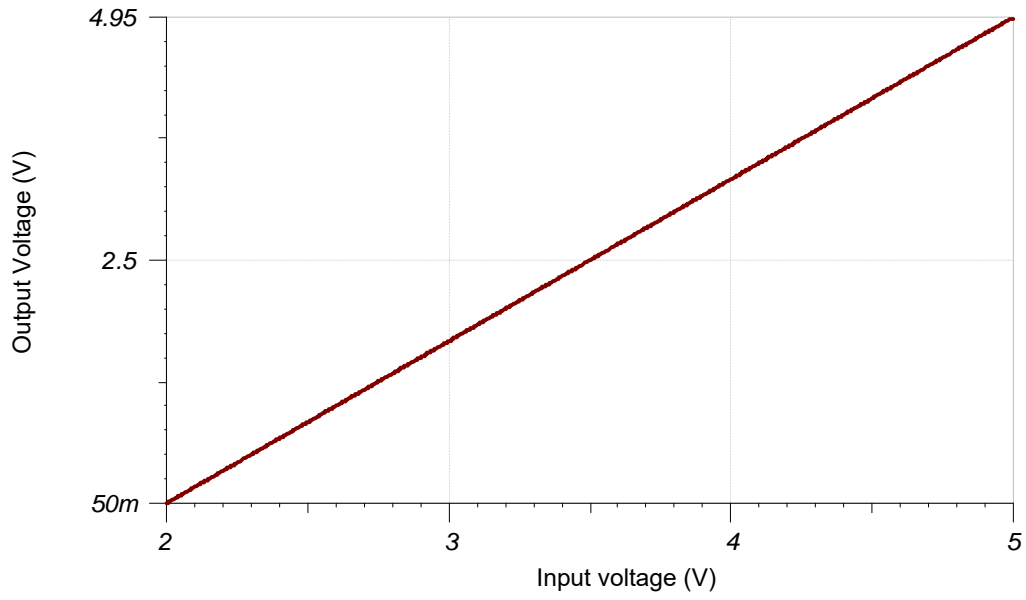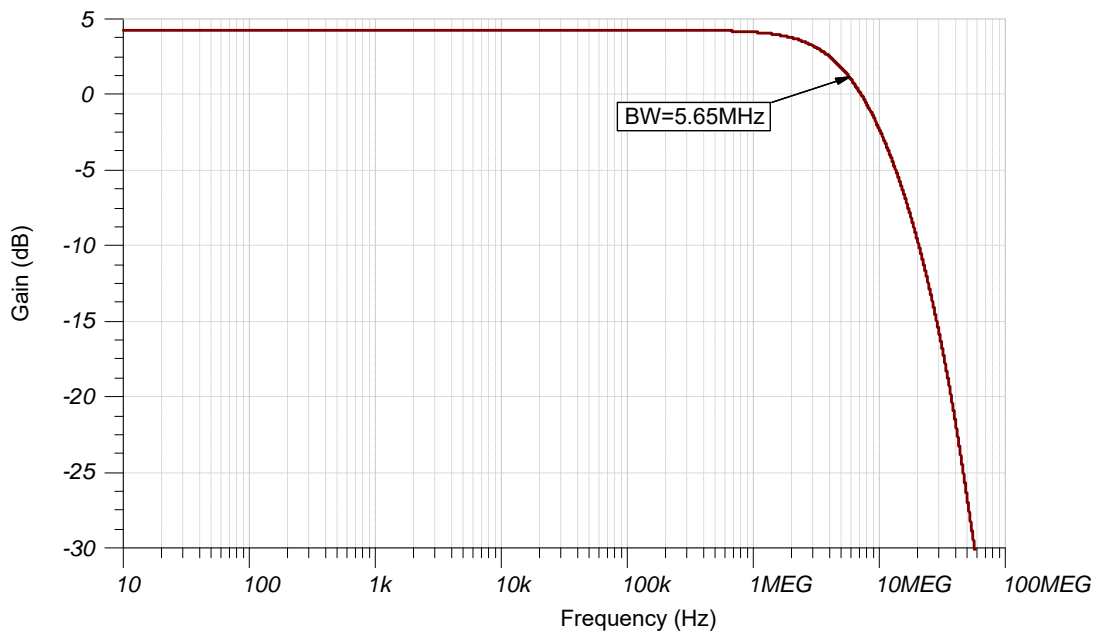
Design References

See *TI Precision Lab Videos on Input and Output Limitations*.

Design Featured Op Amp

TSV912	
V_{ss}	2.5V to 5.5V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	0.3mV
I_q	550µA
I_b	1pA
UGBW	8MHz
SR	4.5V/µs
#Channels	1, 2, 4
www.ti.com/product/tsv912	

Design Alternate Op Amp

OPA191	
V_{ss}	4.5V to 36V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	5µV
I_q	140µA/Ch
I_b	5pA
UGBW	2.5MHz
SR	5.5V/µs
#Channels	1, 2, 4
www.ti.com/product/opa191	

Non-Inverting Op Amp With Non-Inverting Positive Reference Voltage Circuit

Design Goals

Input		Output		Supply		
V_{iMin}	V_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}	V_{ref}
−1V	3V	0.05V	4.95V	5V	0V	2.5V

Design Description

This design uses a non-inverting amplifier with a non-inverting positive reference to translate an input signal of −1V to 3V to an output voltage of 0.05V to 4.95V. This circuit can be used to translate a sensor output voltage with a positive slope and negative offset to a usable ADC input voltage range.
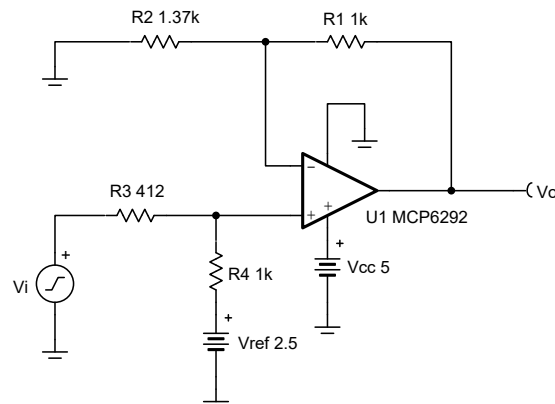
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Design Notes

1. Use op amp linear output operating range. Usually specified under A_{OL} test conditions.
2. Check op amp input common mode voltage range.
3. V_{ref} output must be low impedance.
4. Input impedance of the circuit is equal to the sum of R_3 and R_4.
5. Choose low-value resistors to use in the feedback. It is recommended to use resistor values less than 100kΩ. Using high-value resistors can degrade the phase margin of the amplifier and introduce additional noise in the circuit.
6. The cutoff frequency of the circuit is dependent on the gain bandwidth product (GBP) of the amplifier.
7. Adding a capacitor in parallel with R_1 will improve stability of the circuit if high-value resistors are used.

Design Steps

$$V_o = V_i \times \left(\frac{R_4}{R_3+R_4}\right)\left(\frac{R_1+R_2}{R_2}\right) + V_{ref} \times \left(\frac{R_3}{R_3+R_4}\right)\left(\frac{R_1+R_2}{R_2}\right)$$

1. Calculate the gain of the input voltage to produce the desired output swing.

$$G_{input} = \left(\frac{R_4}{R_3+R_4}\right)\left(\frac{R_1+R_2}{R_2}\right)$$

$$V_{o\_max} - V_{o\_min} = (V_{i\_max} - V_{i\_min})\left(\frac{R_4}{R_3+R_4}\right)\left(\frac{R_1+R_2}{R_2}\right)$$

$$\frac{V_{o\_max}-V_{o\_min}}{V_{i\_max}-V_{i\_min}} = \left(\frac{R_4}{R_3+R_4}\right)\left(\frac{R_1+R_2}{R_2}\right)$$

$$\frac{4.95V-0.05V}{3V-(-1V)} = \left(\frac{R_4}{R_3+R_4}\right)\left(\frac{R_1+R_2}{R_2}\right)$$

$$1.225V = \left(\frac{R_4}{R_3+R_4}\right)\left(\frac{R_1+R_2}{R_2}\right)$$

2. Select a value for R_1 and R_4 and insert the values into the previous equation. The other two resistor values must be solved using a system of equations. The proper output swing and offset voltage cannot be calculated if more than two variables are selected.

$$R_1 = R_4 = 1\ k\Omega$$

$$1.225V = \left(\frac{1\,k\Omega}{R_3+1\,k\Omega}\right)\left(\frac{1\,k\Omega+R_2}{R_2}\right)$$

3. Solve the previous equation for R_3 in terms of R_2.

$$R_3 = \frac{1\,M\Omega+(1\,k\Omega \times R_2)}{1.225 \times R_2} - 1\ k\Omega$$

4. Select any point along the transfer function within the linear output range of the amplifier to set the proper offset voltage at the output (for example, the minimum input and output voltage).

$$V_{o\_min} = V_{i\_min} \times \left(\frac{R_4}{R_3+R_4}\right)\left(\frac{R_1+R_2}{R_2}\right) + V_{ref} \times \left(\frac{R_3}{R_3+R_4}\right)\left(\frac{R_1+R_2}{R_2}\right)$$

$$0.05V = -1\ V \times \left(\frac{1\,k\Omega}{R_3+1\,k\Omega}\right)\left(\frac{1\,k\Omega+R_2}{R_2}\right) + 2.5V \times \left(\frac{R_3}{R_3+1\,k\Omega}\right)\left(\frac{1\,k\Omega+R_2}{R_2}\right)$$

5. Insert R_3 into the equation from step 1 and solve for R_2.

$$0.05V = -1\ V \times \left(\frac{1\,k\Omega}{\frac{1\,M\Omega+1\,k\Omega \times R_2}{1.225 \times R_2}-1\,k\Omega+1\,k\Omega}\right)\left(\frac{1\,k\Omega+R_2}{R_2}\right) + 2.5V \times \left(\frac{\frac{1\,M\Omega+1\,k\Omega \times R_2}{1.225 \times R_2}-1\,k\Omega}{\frac{1\,M\Omega+1\,k\Omega \times R_2}{1.225 \times R_2}-1\,k\Omega+1\,k\Omega}\right)\left(\frac{1\,k\Omega+R_2}{R_2}\right)$$

$$R_2 = 1360.5\Omega \approx 1370\Omega$$

6. Insert R_2 into the equation from step 1 to solve for R_3.

$$R_3 = \frac{1\,M\Omega+1\,k\Omega \times (1370\Omega)}{1.225 \times (1370\Omega)} - 1\ k\Omega$$

$$R_3 = 412.18\Omega \approx 412\Omega$$

Design Simulations
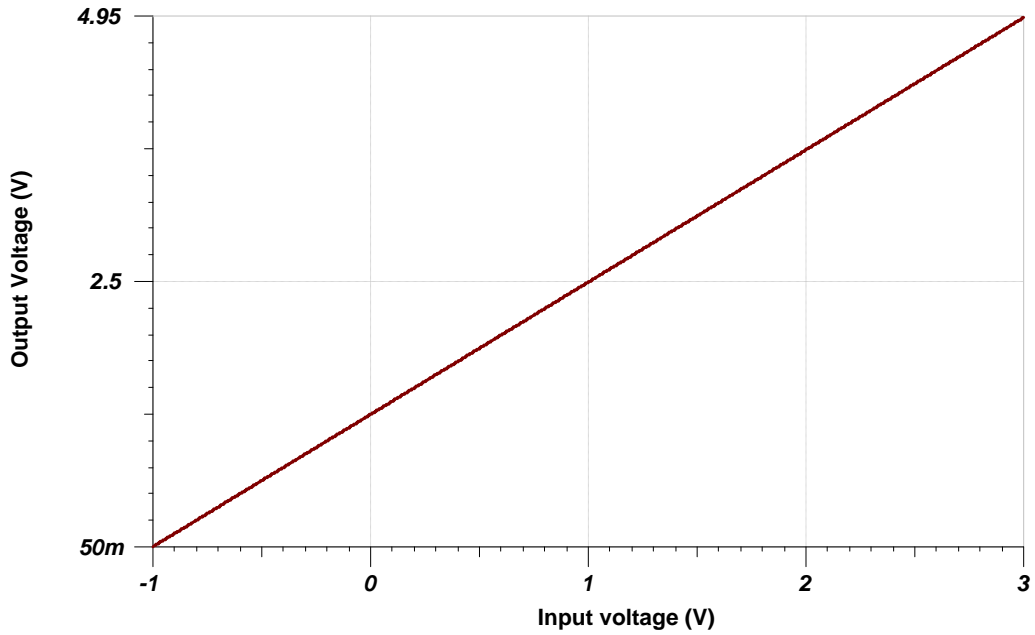
DC Simulation Results

AC Simulation Results

Non-Inverting Op Amp With Non-Inverting Positive
Reference Voltage Circuit

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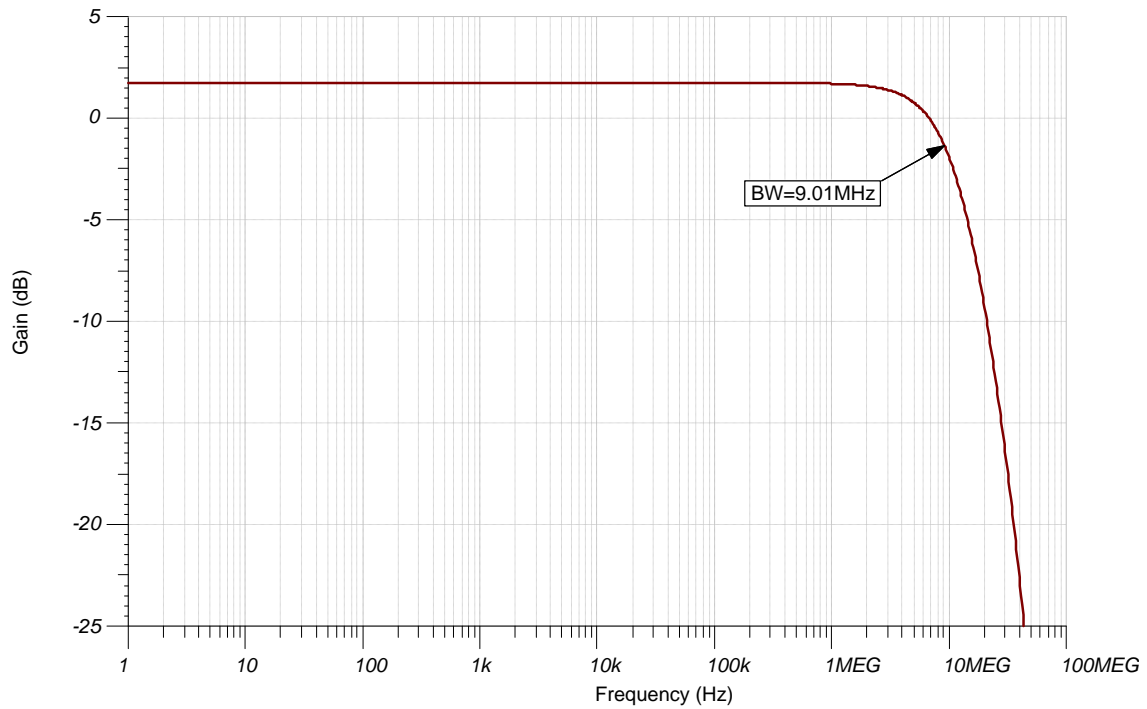
Design References

See *Designing Gain and Offset in Thirty Seconds*.

Design Featured Op Amp

MCP6292	
V_{ss}	2.4V to 5.5V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	0.3mV
I_q	600µA
I_b	1pA
UGBW	10MHz
SR	6.5V/µs
#Channels	1, 2, 4
www.ti.com/product/MCP6292	

Design Alternate Op Amp

OPA388	
V_{ss}	2.5V to 5.5V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	0.25µV
I_q	1.9mA
I_b	30pA
UGBW	10MHz
SR	5V/µs
#Channels	1, 2, 4
www.ti.com/product/opa388	

Inverting Op Amp With Non-Inverting Positive Reference Voltage Circuit

Design Goals

Input		Output		Supply		
V_{iMin}	V_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}	V_{ref}
−1V	2V	0.05V	4.95V	5V	0V	1.259V

Design Description

This design uses an inverting amplifier with a non-inverting positive reference voltage to translate an input signal of −1V to 2V to an output voltage of 0.05V to 4.95V. This circuit can be used to translate a sensor output voltage with a positive slope and negative offset to a usable ADC input voltage range.
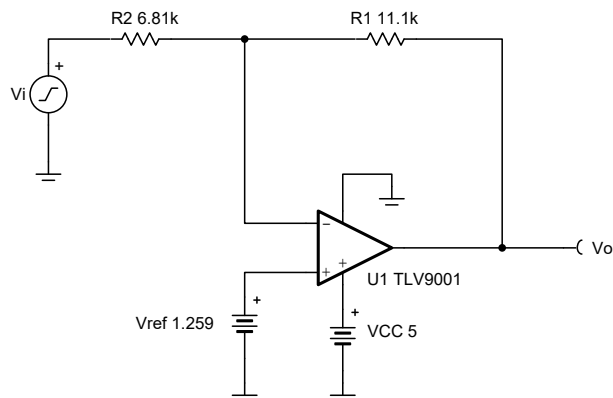
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Design Notes

1. Use op amp linear output operating range. Usually specified under A_{OL} test conditions.
2. Amplifier common mode voltage is equal to the reference voltage.
3. V_{ref} can be created with a voltage divider.
4. Input impedance of the circuit is equal to R_2.
5. Choose low-value resistors to use in the feedback. It is recommended to use resistor values less than 100kΩ. Using high-value resistors can degrade the phase margin of the amplifier and introduce additional noise in the circuit.
6. The cutoff frequency of the circuit is dependent on the gain bandwidth product (GBP) of the amplifier. Additional filtering can be accomplished by adding a capacitor in parallel to R_1. Adding a capacitor in parallel with R_1 will also improve stability of the circuit, if high-value resistors are used.

Design Steps

$$V_o = -V_i \times \left(\frac{R_1}{R_2}\right) + V_{ref} \times \left(1 + \frac{R_1}{R_2}\right)$$

1. Calculate the gain of the input signal.

$$G_{input} = -\frac{R_1}{R_2}$$

$$V_{o\_max} - V_{o\_min} = (V_{i\_max} - V_{i\_min})\left(-\frac{R_1}{R_2}\right)$$

$$-\frac{R_1}{R_2} = -\frac{V_{o\_max} - V_{o\_min}}{V_{i\_max} - V_{i\_min}} = -\frac{4.95V - 0.05V}{2V - (-1\ V)} = -1.633\frac{V}{V}$$

2. Select R_2 and calculate R_1.

$$R_2 = 6.81\ k\Omega$$

$$R_1 = G_{input} \times R_2 = 1.633\frac{V}{V} \times 6.81\ k\Omega = 11.123k\Omega \approx 11.1\ k\Omega\ \text{(Standard Value)}$$

3. Calculate the reference voltage.

$$V_{o\_min} = -V_{i\_max} \times \left(\frac{R_1}{R_2}\right) + V_{ref} \times \left(1 + \frac{R_1}{R_2}\right)$$

$$0.05V = -2V \times \left(\frac{11.11\ k\Omega}{6.81\ k\Omega}\right) + V_{ref} \times \left(1 + \frac{11.11\ k\Omega}{6.81\ k\Omega}\right)$$

$$V_{ref} = \frac{V_{o\_min} + V_{i\_max} \times \left(\frac{R_1}{R_2}\right)}{\left(1 + \frac{R_1}{R_2}\right)} \frac{0.05V + 2V \times \left(\frac{11.11\ k\Omega}{6.81\ k\Omega}\right)}{\left(1 + \frac{11.11\ k\Omega}{6.81\ k\Omega}\right)} = 1.259V$$

Design Simulations
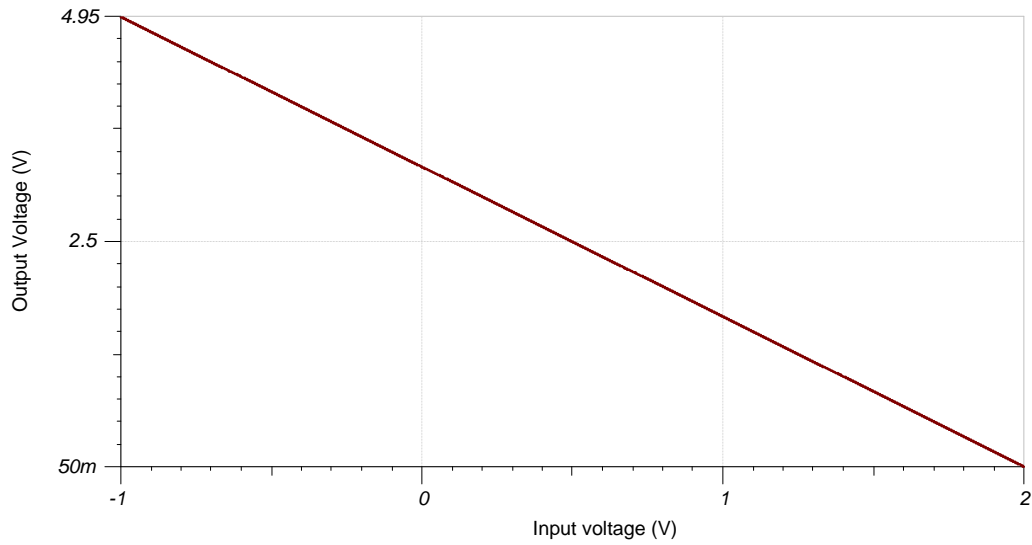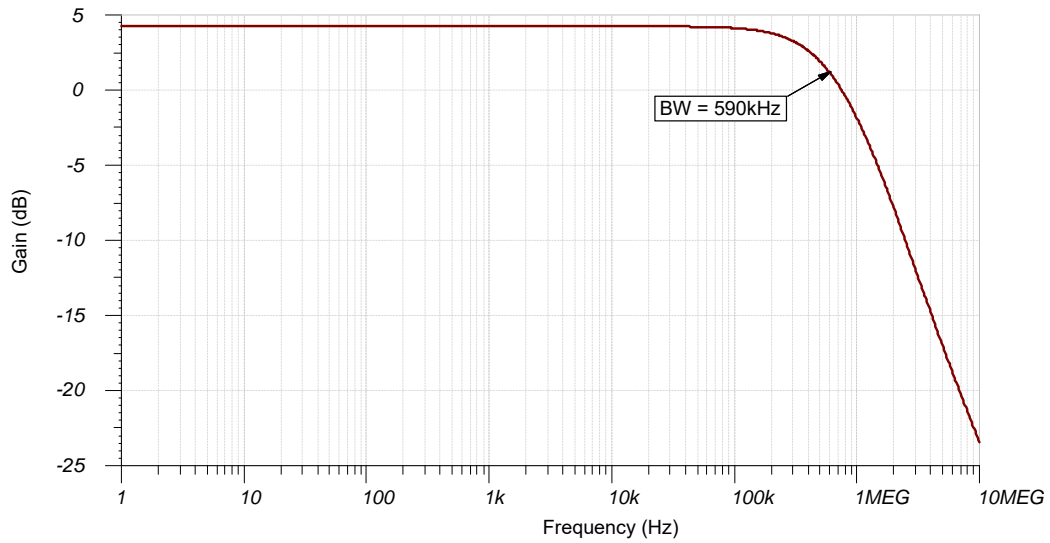
DC Simulation Results

AC Simulation Results

BW = 590kHz

104

Design References

See *Designing Gain and Offset in Thirty Seconds*.

Design Featured Op Amp

TLV9001	
V_{ss}	1.8V to 5.5V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	0.4mV
I_q	60µA
I_b	5pA
UGBW	1MHz
SR	2V/µs
#Channels	1, 2, 4
www.ti.com/product/tlv9002	

Design Alternate Op Amp

OPA376	
V_{ss}	2.2V to 5.5V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	5µV
I_q	760µA
I_b	0.2pA
UGBW	5.5MHz
SR	2V/µs
#Channels	1, 2, 4
www.ti.com/product/opa376	

Comparator With and Without Hysteresis Circuit

Design Goals

Input		Output		Supply		
V_{iMin}	V_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}	V_{ref}
0V	5V	0V	5V	5V	0V	5V

V_L (Lower Threshold)	V_H (Upper Threshold)	$V_H - V_L$
2.3V	2.7V	0.4V

Design Description

Comparators are used to compare two different signal levels and create an output based on the input with the higher input voltage. Noise or signal variation at the comparison threshold will cause the comparator output to have multiple output transitions. Hysteresis sets upper- and lower-threshold voltages to eliminate the multiple transitions caused by noise.
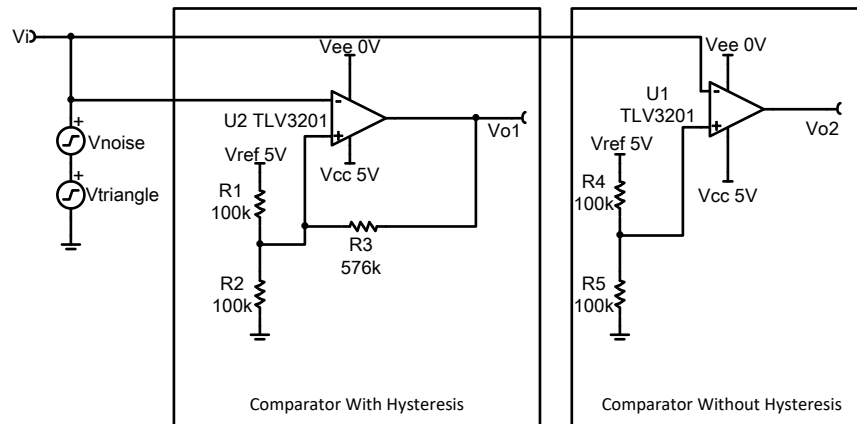
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Design Notes

1. Use a comparator with low quiescent current to reduce power consumption.
2. The accuracy of the hysteresis threshold voltages are related to the tolerance of the resistors used in the circuit.
3. The propagation delay is based on the specifications of the selected comparator.

Design Steps

1. Select components for the comparator with hysteresis.

   a. Select V_L, V_H, and R_1.

   $V_L = 2.3V$

   $V_H = 2.7V$

   $R_1 = 100k\Omega$ (Standard Value)

   b. Calculate R_2.

   $$R_2 = \frac{V_L}{V_{cc} - V_H} \times R_1 = \frac{2.3V}{5V - 2.7V} \times 100k\Omega = 100k\Omega \text{ (Standard Value)}$$

   c. Calculate R_3.

   $$R_3 = \frac{V_L}{V_H - V_L} \times R_1 = \frac{2.3V}{2.7V - 2.3V} \times 100k\Omega = 575k\Omega \approx 576k\Omega \text{ (Standard Value)}$$

   d. Verify hysteresis width.

   $$V_H - V_L = \frac{R_1 \times R_2}{(R_3 \times R_1) + (R_3 \times R_2) + (R_1 \times R_2)} \times V_{cc}$$

   $$= \frac{100k\Omega \times 100k\Omega}{(576k\Omega \times 100k\Omega) + (576k\Omega \times 100k\Omega) + (100k\Omega \times 100k\Omega)} \times 5V = 0.399V$$

2. Select components for comparator without hysteresis.

   a. Select V_{th} and R_4.

   $V_{th} = 2.5V$

   $R_4 = 100k\Omega$ (Standard Value)

   b. Calculate R_5.

   $$R_5 = \frac{V_{th}}{V_{cc} - V_{th}} \times R_4 = \frac{2.5V}{5V - 2.5V} \times 100k\Omega = 100k\Omega \text{ (Standard Value)}$$

Design Simulations

Transient Simulation Results
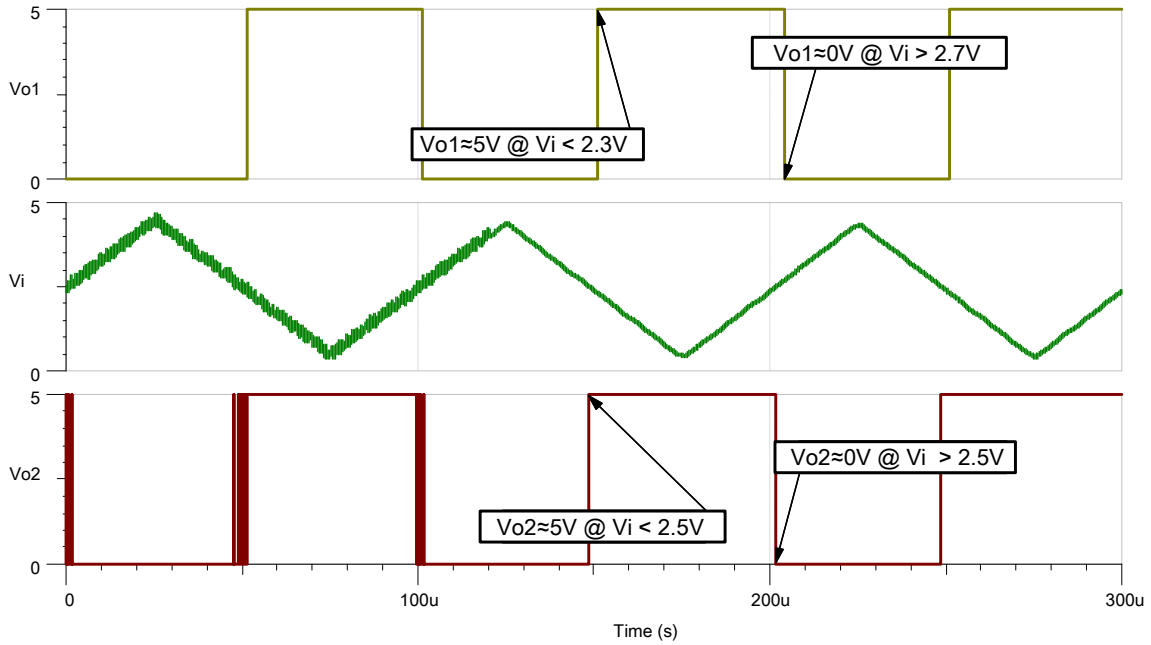
Noise Only Present From 0s to 120µs
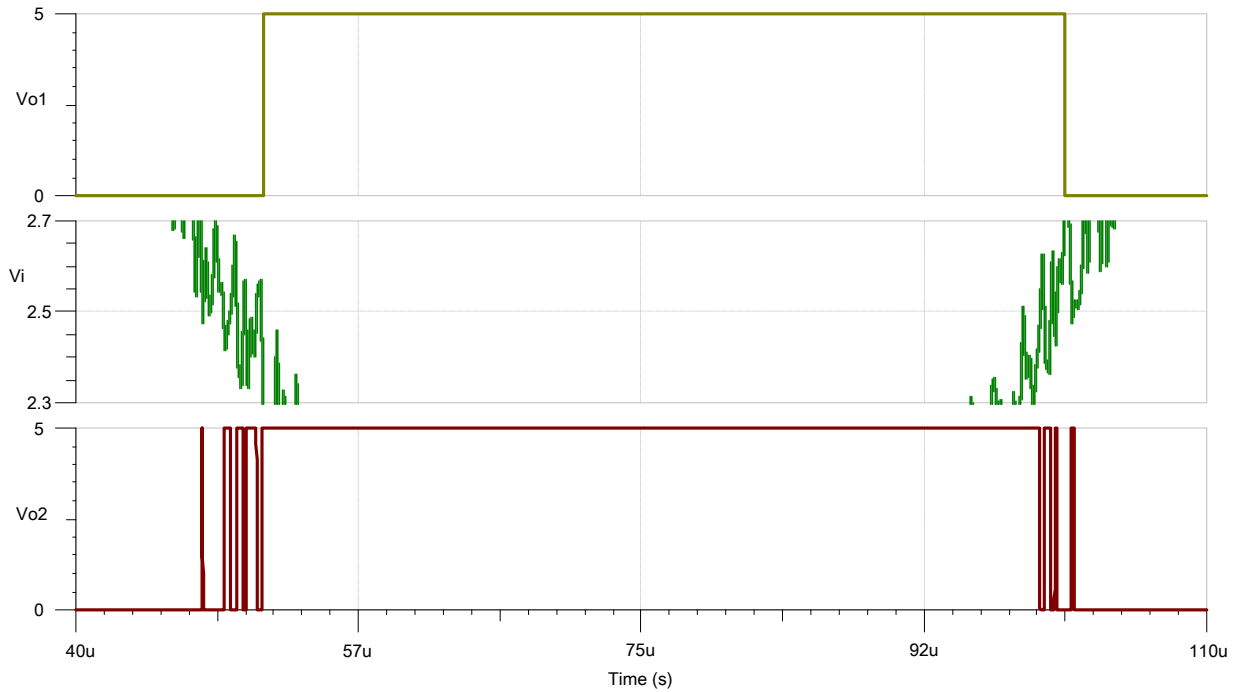
Zoomed in From 40µs to 110µs

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Comparator With and Without Hysteresis Circuit

Design References

See TIPD144, www.ti.com/tool/tipd144.

Design Featured Comparator

TLV3201	
V_{cc}	2.7V to 5.5V
V_{inCM}	Extends 200mV beyond either rail
V_{out}	(V_{ee}+230mV) to (V_{cc}–210mV) @ 4mA
V_{os}	1mV
I_q	40µA
I_b	1pA
UGBW	-
SR	-
#Channels	1, 2
www.ti.com/product/tlv3201	

Comparator With and Without Hysteresis Circuit   SBOA219–January 2018
Submit Documentation Feedback

Window Comparator Circuit

Design Goals

Input		Output		Supply		
V_{iMin}	V_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}	V_{ref}
0V	5V	0V	36V	5V	0V	2.5V

V_L (Lower Threshold)	V_H (Upper Threshold)	Upper to Lower Threshold Ratio
1.66V	3.33V	2

Design Description

This circuit utilizes two comparators in parallel to determine if a signal is between two reference voltages. If the signal is within the window, the output is high. If the signal level is outside of the window, the output is low. For this design, the reference voltages are generated from a single supply with voltage dividers.

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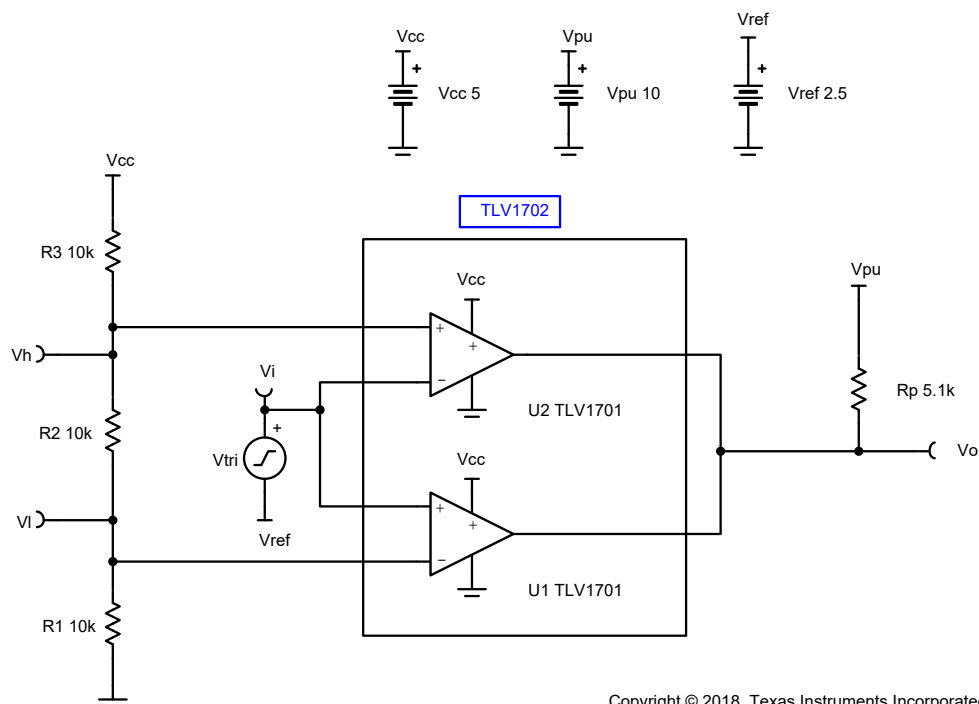
Design Notes

1. The input should not exceed the common mode limitations of the comparators.
2. If higher pullup voltages are used, R_p should be sized accordingly to prevent large current draw. The TLV1701 supports pullup voltages up to 36V.
3. Comparator must be open-drain or open-collector to allow for the ORed output.

Design Steps

1. Define the upper (V_H) and lower (V_L) window voltages.

$$V_H = V_{cc} \times \frac{R_1 + R_2}{R_1 + R_2 + R_3} = 3.33 \text{ V}$$

$$V_L = V_{cc} \times \frac{R_1}{R_1 + R_2 + R_3} = 1.66 \text{ V}$$

$$\frac{V_H}{V_L} = 1 + \frac{R_2}{R_1} = \frac{3.33V}{1.66V} = 2$$

2. Choose resistor values to achieve the desired window voltages.

$$\frac{V_H}{V_L} = 1 + \frac{R_2}{R_1} = 2, \text{ so } R_2 = R_1$$

$$R_1 = R_2 = 10k\Omega \text{ (Selected standard values)}$$

$$R_3 = \frac{R_1 \times V_{cc}}{V_L} - (R_1 + R_2)$$

$$R_3 = \frac{10k\Omega \times 5V}{1.66V} - 20k\Omega = 10.12 \text{ k}\Omega \approx 10k\Omega \text{ (Standard Value)}$$

Design Simulations

Transient Simulation Results
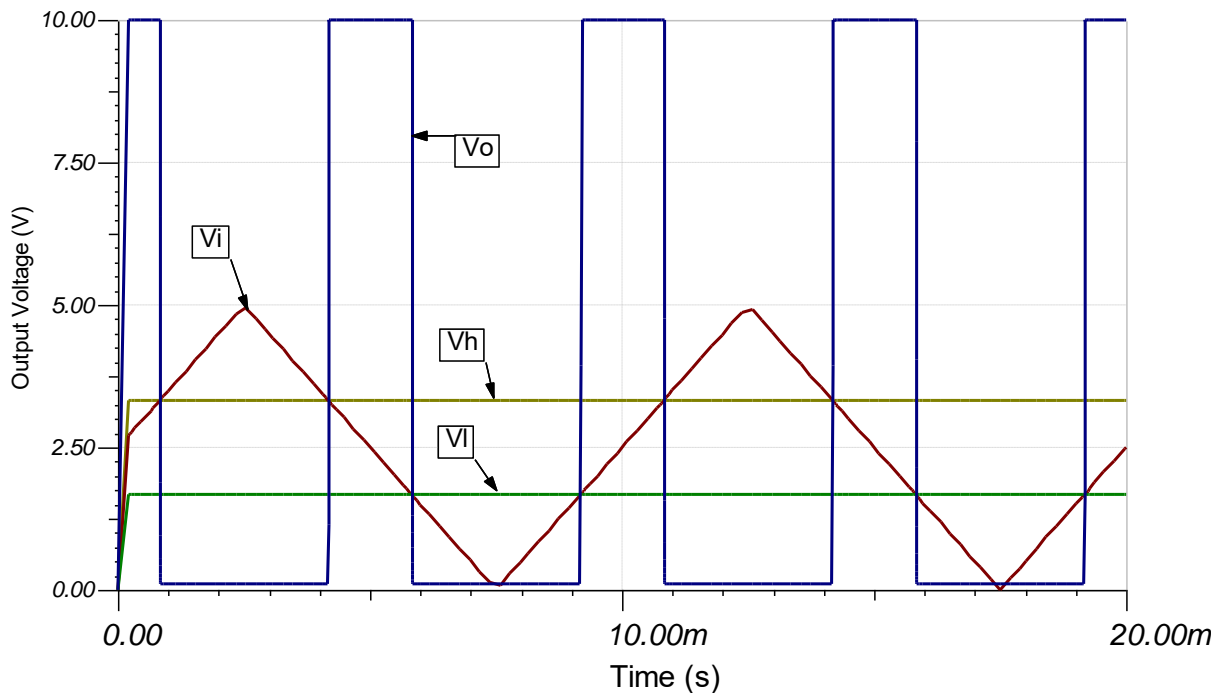
Design References

See TIPD178, www.ti.com/tool/tipd178.

Design Featured Op Amp

TLV1702	
V_{cc}	2.2V to 36V
V_{inCM}	Rail-to-rail
V_{out}	Open Collector (36V Max)
V_{os}	2.5mV
I_q	75µA/Ch
I_b	15nA
Rise Time	365ns
Fall Time	240ns
#Channels	1, 2, 4
www.ti.com/product/tlv1702	

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Photodiode Amplifier Circuit

Design Goals

Input		Output		BW	Supply		
I_{iMin}	I_{iMax}	V_{oMin}	V_{oMax}	f_p	V_{cc}	V_{ee}	V_{ref}
0A	2.4µA	100mV	4.9V	20kHz	5V	0V	0.1V

Design Description

This circuit consists of an op amp configured as a transimpedance amplifier for amplifying the light-dependent current of a photodiode.
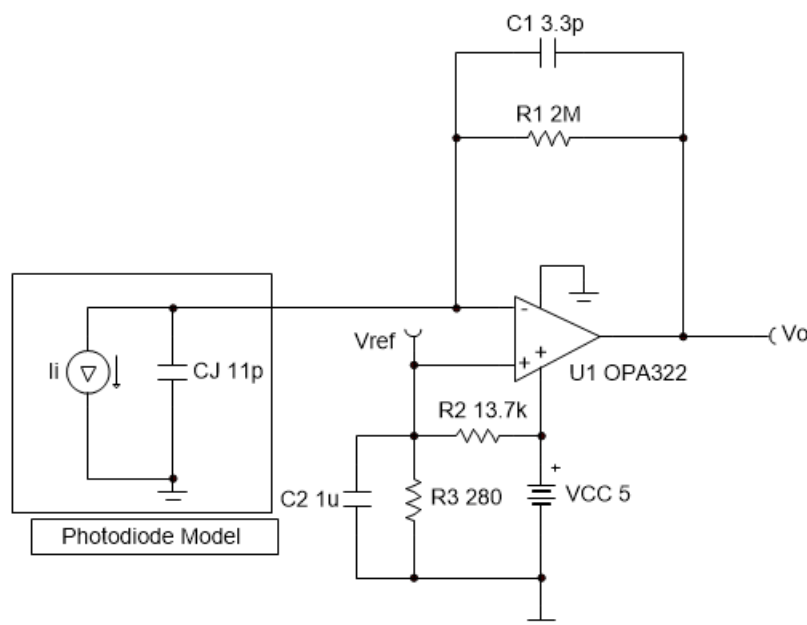
Design Notes

1. A bias voltage (V_{ref}) prevents the output from saturating at the negative power supply rail when the input current is 0A.
2. Use a JFET or CMOS input op amp with low bias current to reduce DC errors.
3. Set output range based on linear output swing (see A_{ol} specification).

Design Steps

1. Select the gain resistor.

$$R_1 = \frac{V_{oMax} - V_{oMin}}{I_{iMax}} = \frac{4.9V - 0.1V}{2.4\mu A} = 2M\Omega$$

2. Select the feedback capacitor to meet the circuit bandwidth.

$$C_1 \leq \frac{1}{2 \times \pi \times R_1 \times f_p}$$

$$C_1 \leq \frac{1}{2 \times \pi \times 2M\Omega \times 20kHz} \leq 3.97pF \approx 3.3pF \text{ (Standard Value)}$$

3. Calculate the necessary op amp gain bandwidth (GBW) for the circuit to be stable.

$$GBW > \frac{C_i + C_1}{2 \times \pi \times R_1 \times C_1^2} > \frac{20pF + 3.3pF}{2 \times \pi \times 2M\Omega \times (3.3pF)^2} > 170kHz$$

where $C_i = C_j + C_d + C_{cm} = 11pF + 5pF + 4pF = 20pF$ given

  - C_j: Junction capacitance of photodiode
  - C_d: Differential input capacitance of the amplifier
  - C_{cm}: Common-mode input capacitance of the inverting input

4. Calculate the bias network for a 0.1-V bias voltage.

$$R_2 = \frac{V_{cc} - V_{ref}}{V_{ref}} \times R_3$$

$$R_2 = \frac{5V - 0.1V}{0.1V} \times R_3$$

$$R_2 = 49 \times R_3$$

Closest 1% resistor values that yield this relationship are
$R_2 = 13.7k\Omega$ and $R_3 = 280\Omega$

5. Select C_2 to be 1µF to filter the V_{ref} voltage. The resulting cutoff frequency is:

$$f_p = \frac{1}{2 \times \pi \times C_2 \times (R_2 \| R_3)} = \frac{1}{2 \times \pi \times 1\mu F \times (13.7k \| 280)} = 580Hz$$

Design Simulations
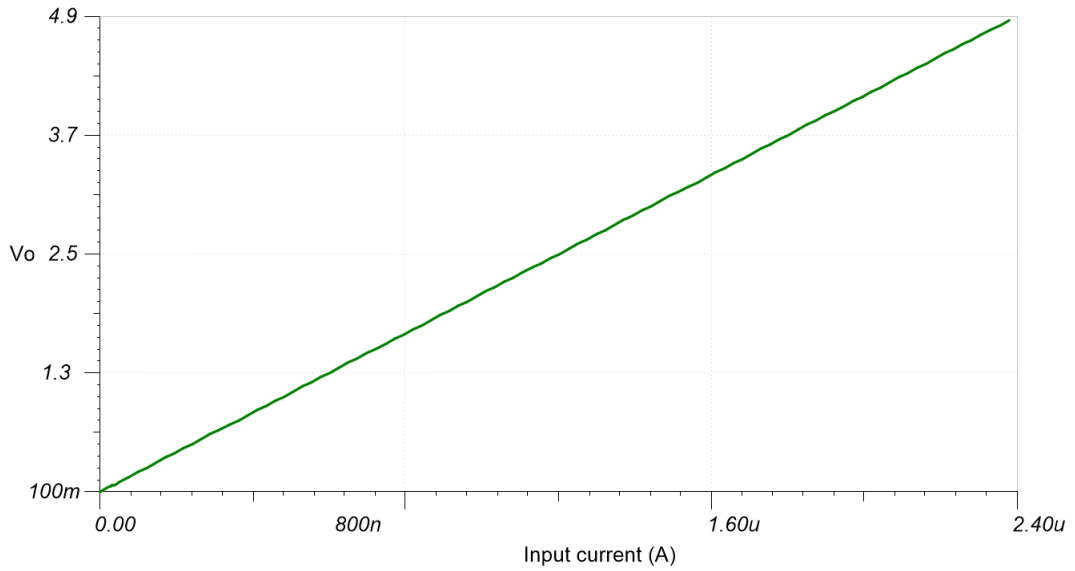
DC Simulation Results

AC Simulation Results

115
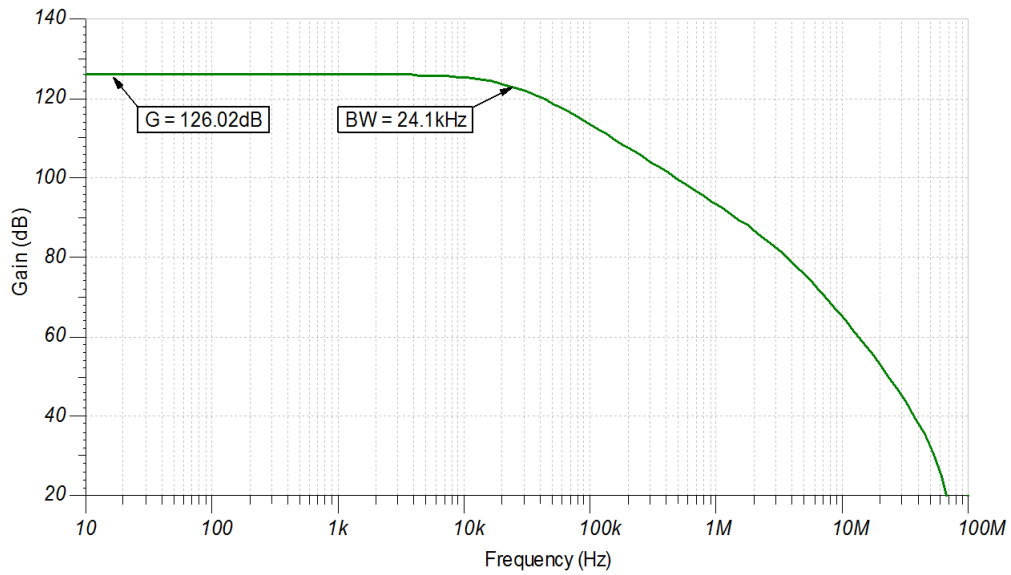
Design References

See TIPD176, www.ti.com/tool/tipd176.

Design Featured Op Amp

OPA322	
V_{cc}	1.8V to 5.5V
V_{inCM}	Rail–to–rail
V_{out}	Rail–to–rail
V_{os}	0.5mV
I_q	1.6mA/Ch
I_b	0.2pA
UGBW	20MHz
SR	10V/µs
#Channels	1, 2, 4
www.ti.com/product/opa322	

Design Alternate Op Amp

LMP7721	
V_{cc}	1.8V to 5.5V
V_{inCM}	V_{ee} to (V_{cc} –1V)
V_{out}	Rail–to–rail
V_{os}	26µV
I_q	1.3mA/Ch
I_b	3fA
UGBW	17MHz
SR	10.43V/µs
#Channels	1
www.ti.com/product/lmp7721	