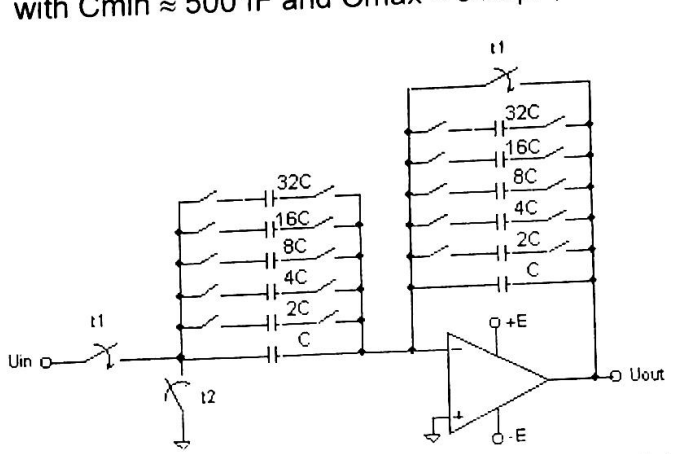
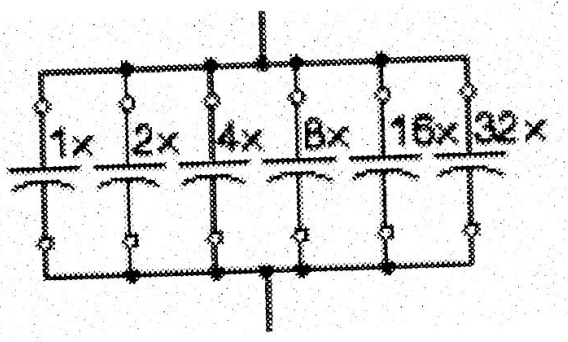
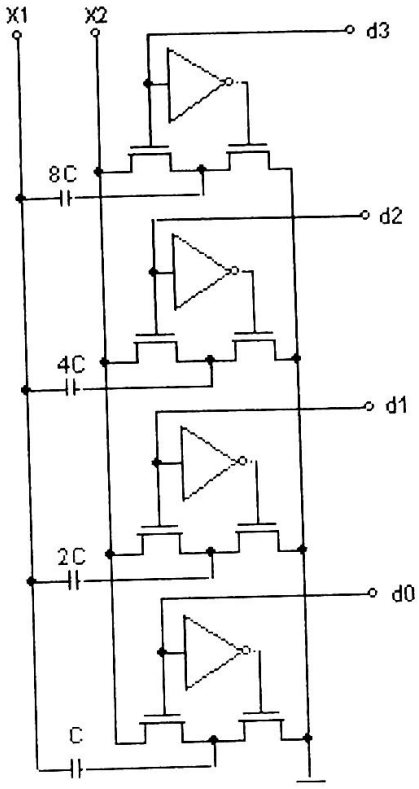
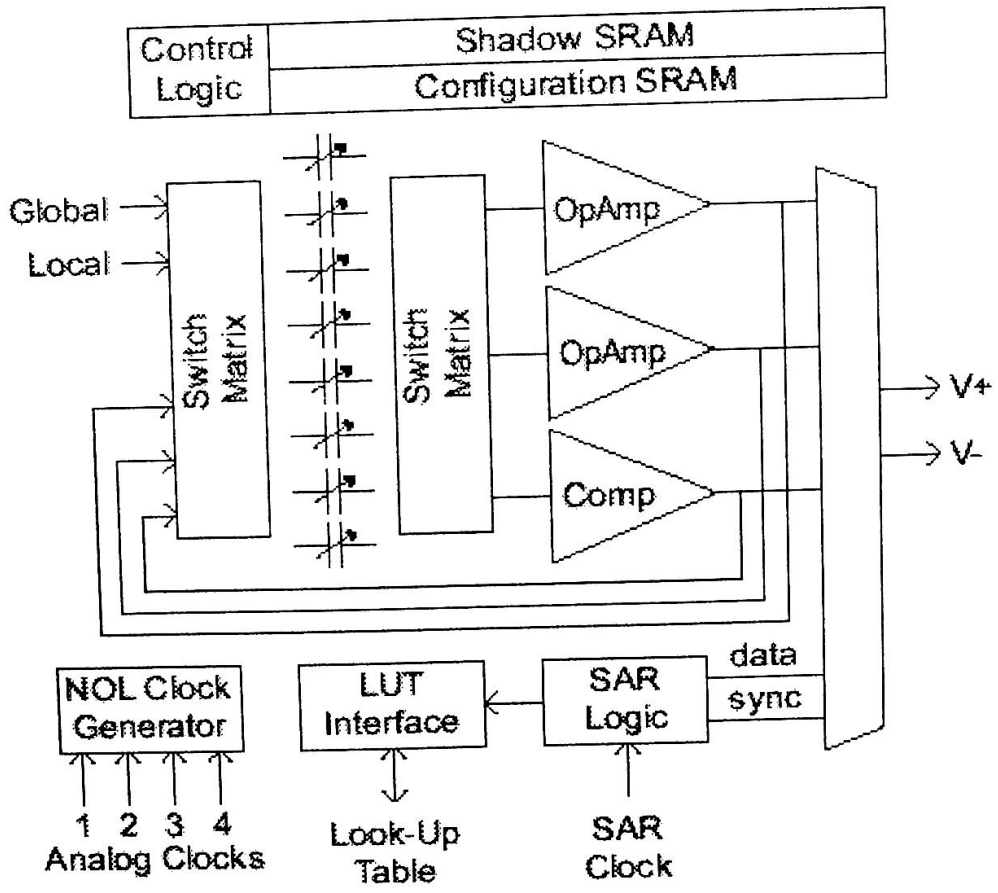
Programmable Gain Amplifier Uses two 6-bit Programmable Capacitor Arrays with Cmin ≈ 500 fF and Cmax ≈ 31.5pF; *Gmin* = 1/64, *Gmax*=64.

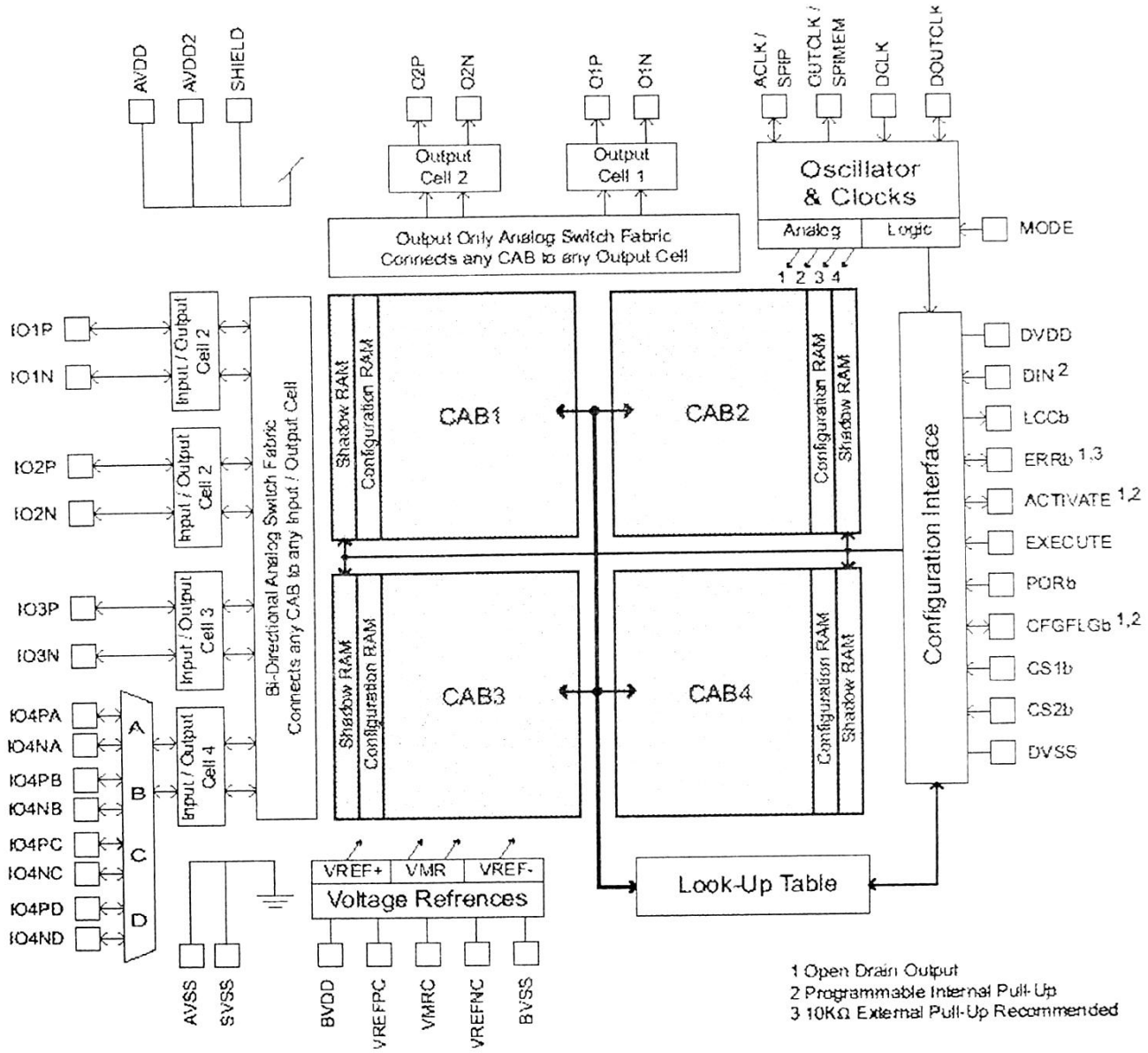








Inverting & Non-inverting Gain Stages; • Half Cycle Gain Stage; • Half Cycle Inverting Gain Stage with Hold; • Gain Polarity Stage; Inverting & Non-inverting Comparator; • Inverting & Non-inverting Differentiator; • Bilinear Filter; • Biquadratic Filter; • Sample and Hold; • Integrator; • Multiplier/Divider; • Sinewave Oscillator; • Arbitrary Periodic Waveform Generator; • Rectifiers; • Half Cycle Sum/Difference Stage; • Inverting Sum Stage; • User-defined Voltage Transfer Function; • DC Voltage Source; • Sum/Difference Stage with Low Pass Filter; etc.



The most attractive applications:

- sensor interfacing and signal conditioning;
- analog control circuits;
- complex filtering;
- photodiode interfacing;
- audio signal processing;
- ultra low-frequency analog processing for medical purposes;
- programmable analog front-end;
- compression and expansion;
- laser control;
- PID control;
- differential equations solving.

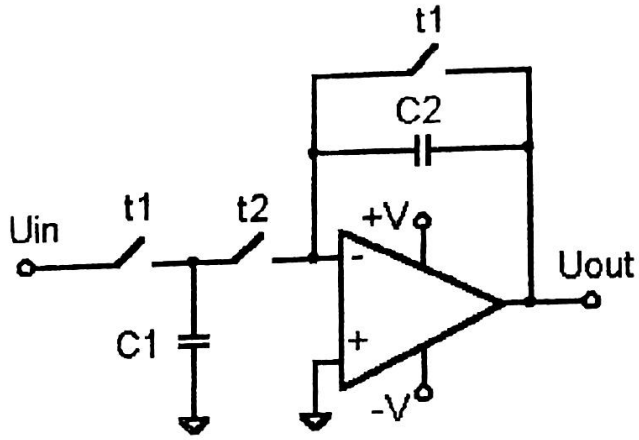


Figure 1 a. SC inverting amplifier.

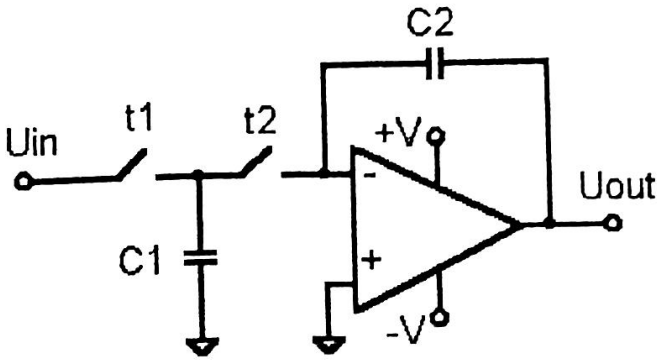


Figure 2a. Inverting SC integrator

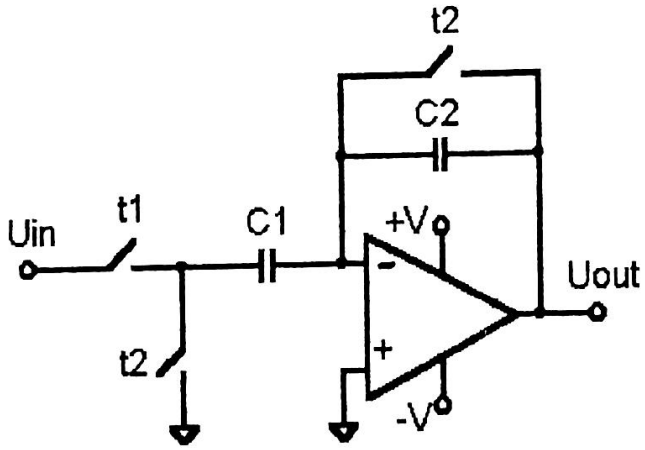


Figure 3a. Another configuration of SC inverting amplifier.

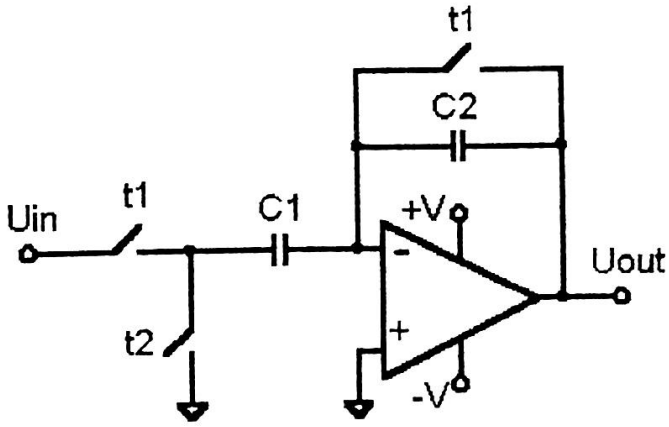


Figure 4a Non-inverting amplifier

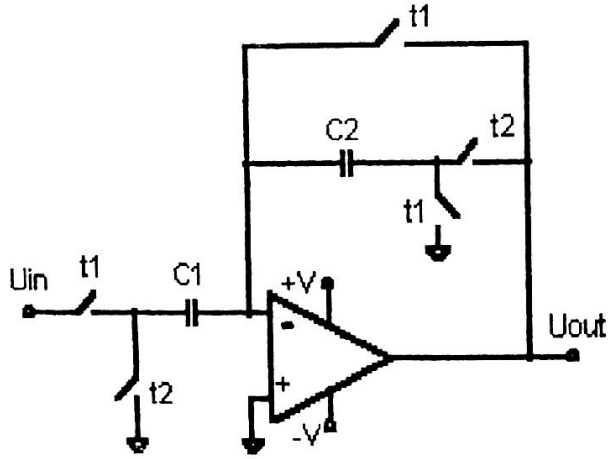


Figure 5a. Non-inverting amplifier with offset voltage compensation.

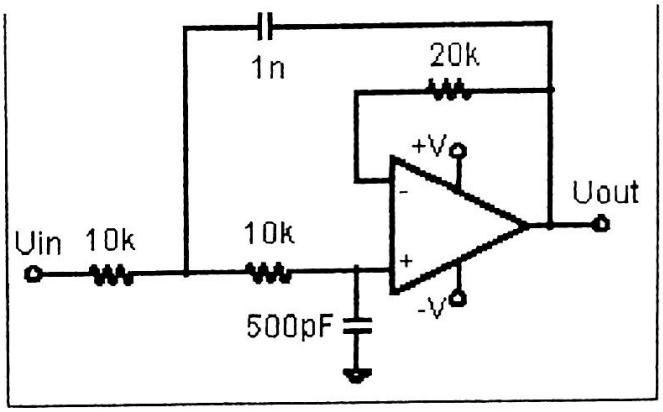
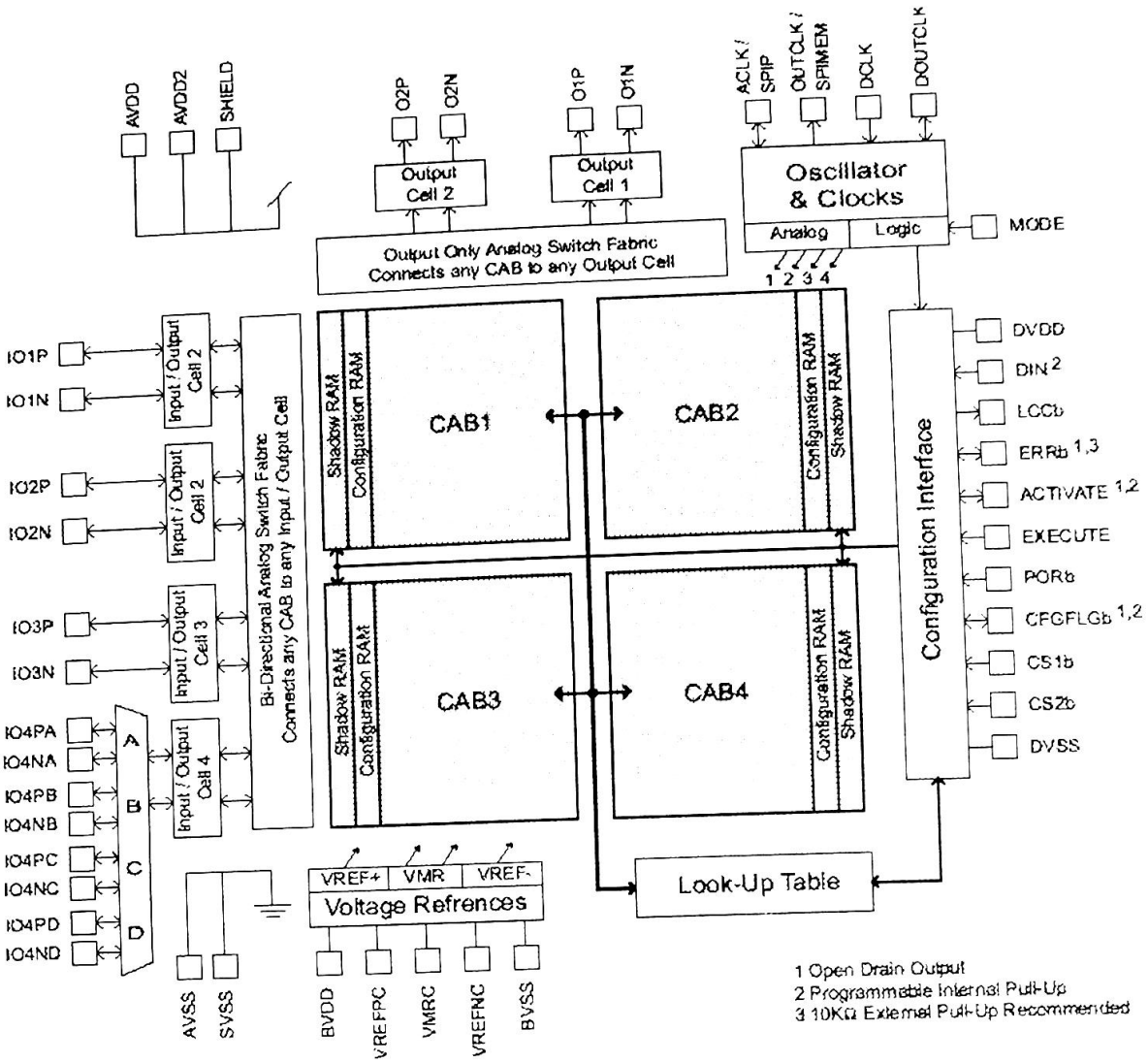
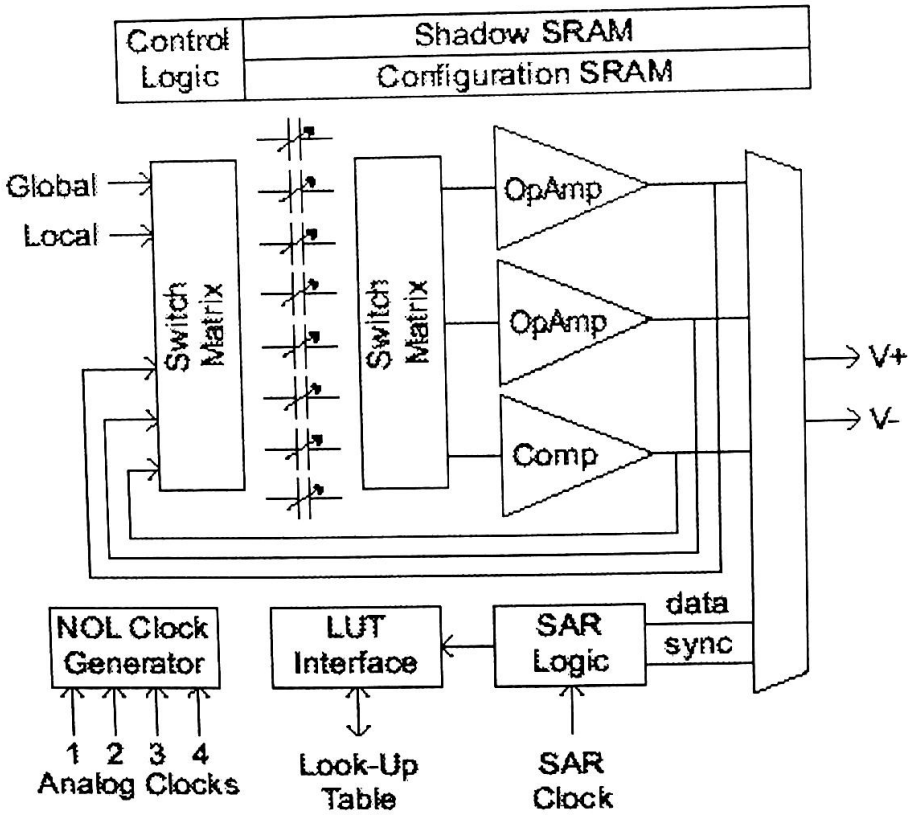
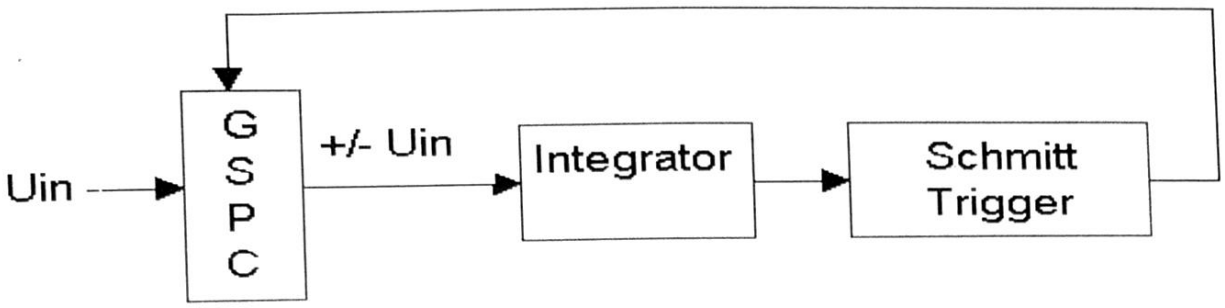
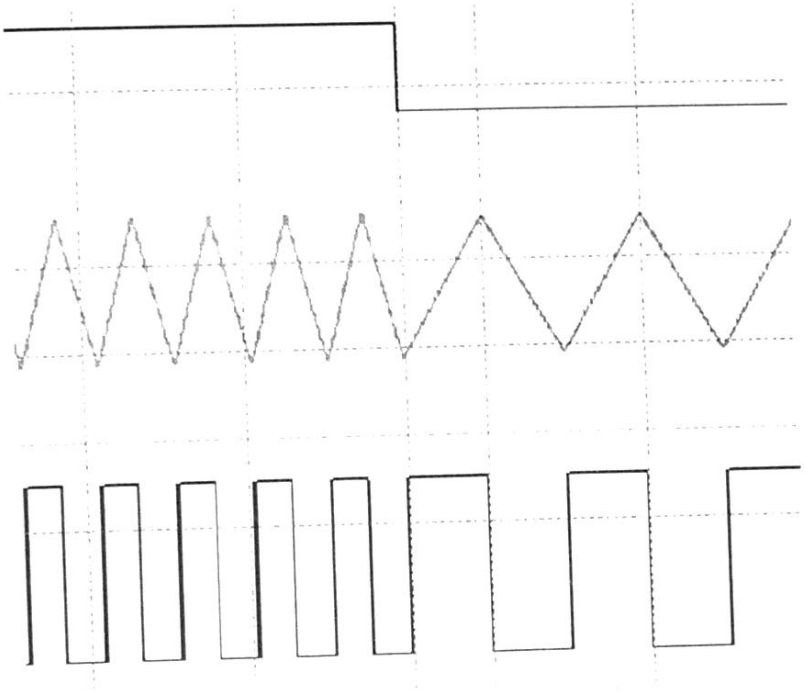


Figure 7. Low-pass output filter.


AVDD
AVDD2
SHIELD
O2P
O2N
O1P
O1N
ACLK / SPIP
OUTCLK / SPIMEM
DCLK
DOUTCLK
Output Cell 2
Output Cell 1
Oscillator & Clocks
Analog
Logic
MODE
1 2 3 4
Output Only Analog Switch Fabric
Connects any CAB to any Output Cell
IO1P
IO1N
IO2P
IO2N
IO3P
IO3N
IO4PA
IO4NA
IO4PB
IO4NB
IO4PC
IO4NC
IO4PD
IO4ND
Input / Output Cell 2
Input / Output Cell 3
Input / Output Cell 4
A
B
C
D
Bi-Directional Analog Switch Fabric
Connects any CAB to any Input / Output Cell
Shadow RAM
Configuration RAM
CAB1
CAB2
CAB3
CAB4
Configuration Interface
DVDD
DIN 2
LCCb
ERRb 1,3
ACTIVATE 1,2
EXECUTE
PORb
CFGFLGb 1,2
CS1b
CS2b
DVSS
VREF+
VMR
VREF-
Voltage Refrences
Look-Up Table
AVSS
SVSS
BVDD
VREFPC
VMRC
VREFNC
BVSS
1 Open Drain Output
2 Programmable Internal Pull-Up
3 10KΩ External Pull-Up Recommended

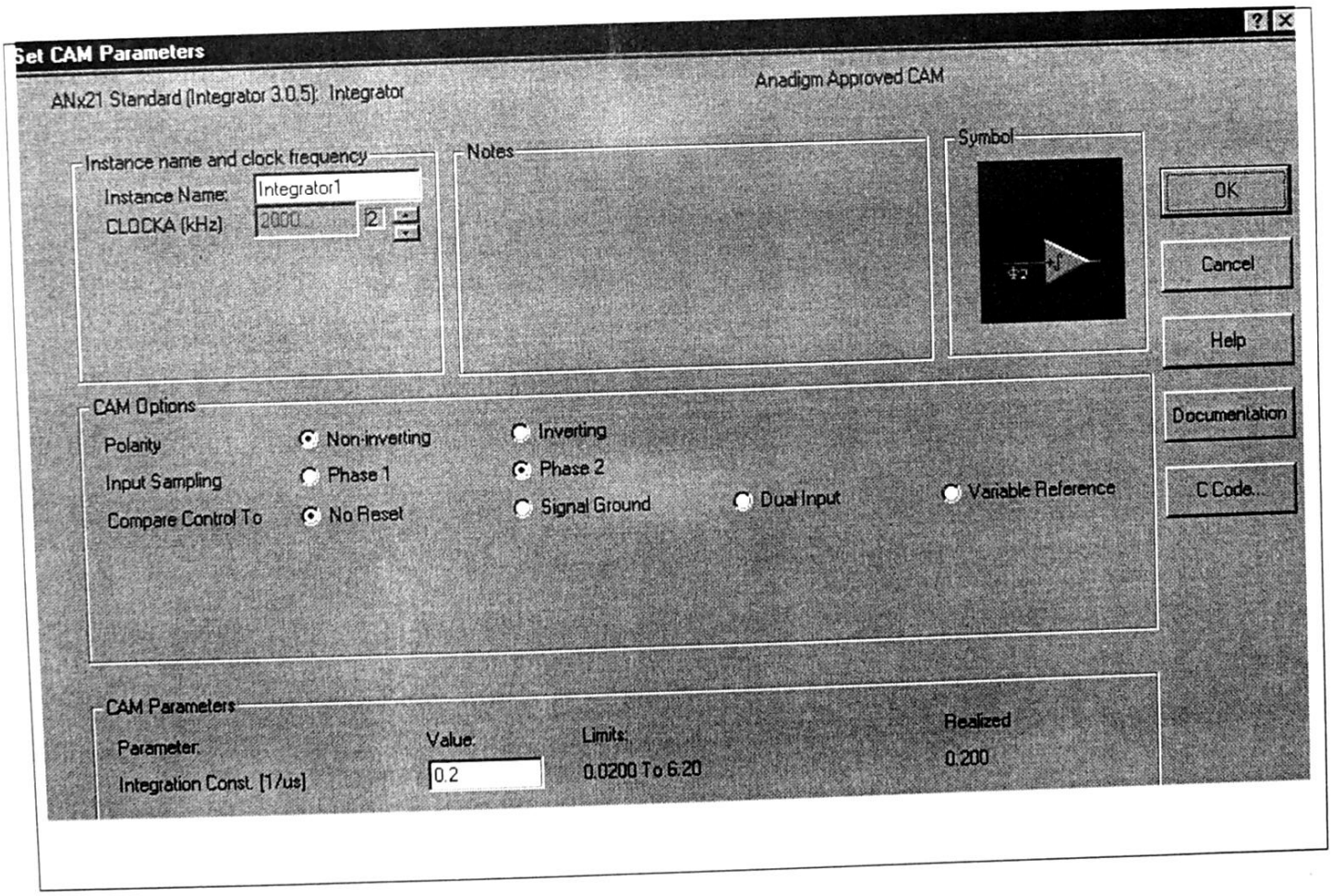

Control Logic
Shadow SRAM
Configuration SRAM
Global
Local
Switch Matrix
Switch Matrix
OpAmp
OpAmp
Comp
V+
V-
NOL Clock Generator
LUT Interface
SAR Logic
data
sync
1 2 3 4
Analog Clocks
Look-Up Table
SAR Clock

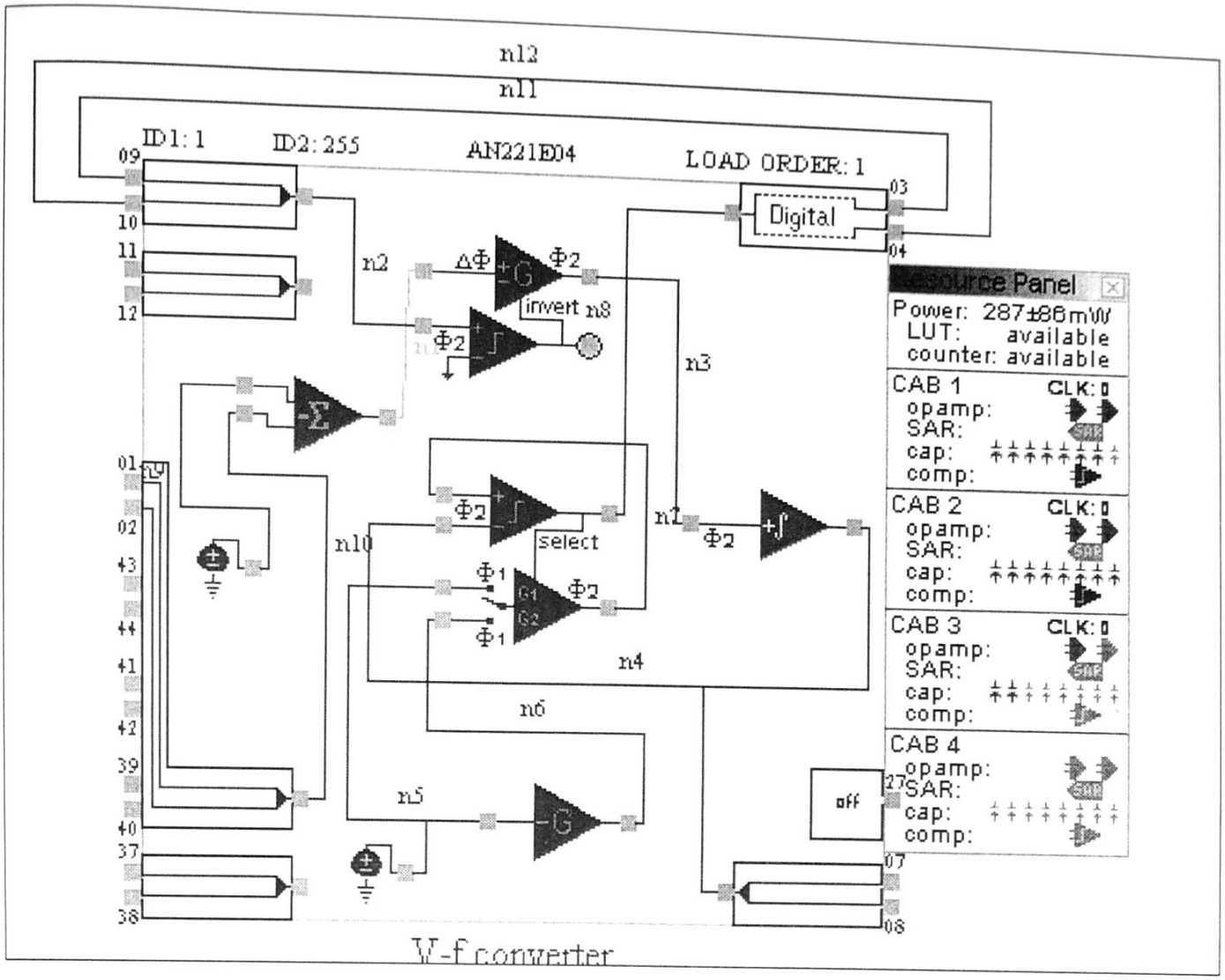


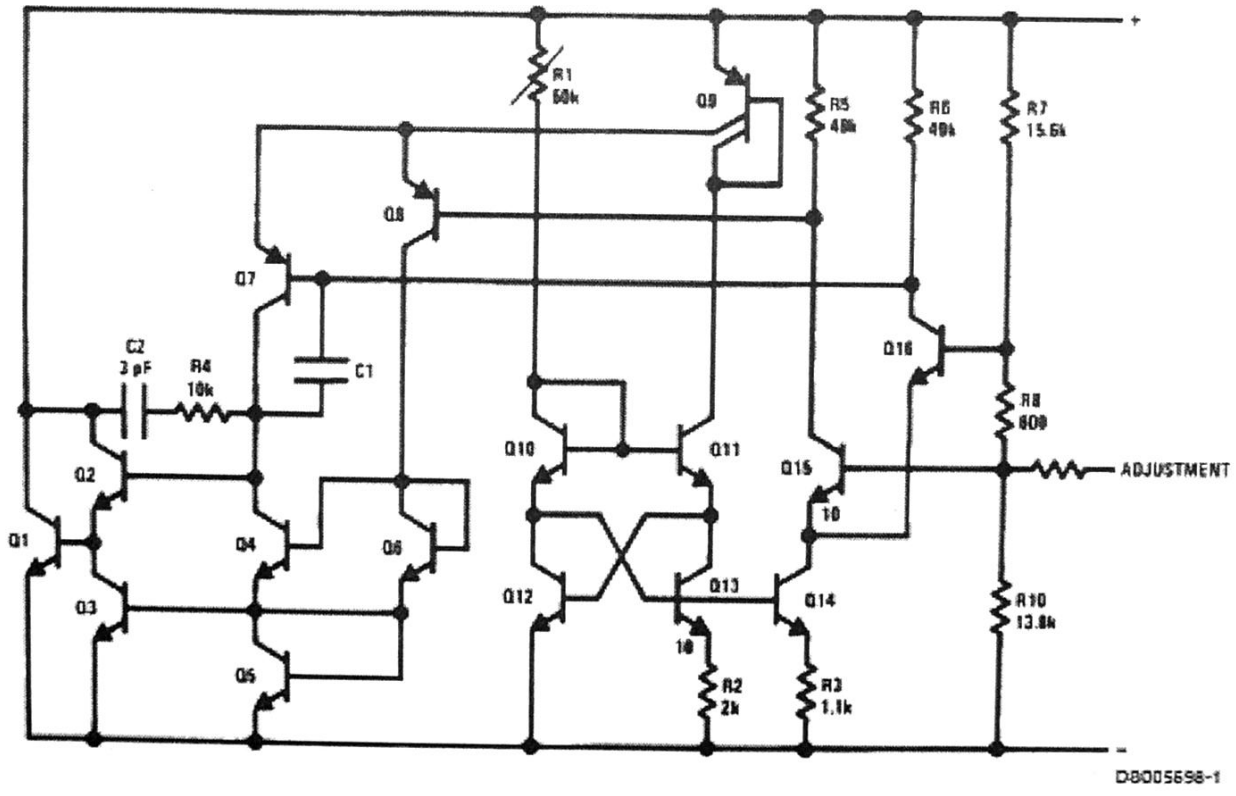


$$T = \frac{k}{2} \frac{U_{in}}{(UTP - LTP)}$$

GSPC - Gain Stage with Polarity Control




n12
n11
ID1: 1
ID2: 255
AN221E04
LOAD ORDER: 1
Digital
Source Panel
Power: 287±86mW
LUT: available
counter: available
CAB 1
CAB 2
CAB 3
CAB 4
CLK:
opamp:
SAR:
cap:
comp:
invert n8
select
off
n1
n2
n3
n4
n5
n6
n10
W-f converter


R1 50k
R5 40k
R6 40k
R7 15.6k
R8 800
R10 13.8k
R2 2k
R3 1.1k
R4 10k
C1
C2 3 pF
ADJUSTMENT
D8005698-1